

# ZCU216 Evaluation Board

## *User Guide*

UG1390 (v1.1) July 10, 2020



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# Revision History

The following table shows the revision history for this document.

| Section                                    | Revision Summary                 |
|--|----------------------------------|
| <b>07/10/2020 Version 1.1</b>              |                                  |
| <a href="#">XM650/655 Connector Pinout</a> | Revised connector pinout tables. |
| <b>03/17/2020 Version 1.0</b>              |                                  |
| Initial release.                           | N/A                              |



# Introduction

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## Overview

The ZCU216 is an evaluation board featuring the ZU49DR Zynq<sup>®</sup> UltraScale+™ RFSoc Gen3 device. This board enables evaluation of applications requiring sub-6 GHz Bands for Radio, mmWave, and full L-band and S-Band in Phased Array Radar. The ZCU216 board is equipped with all the common board-level features needed for design development like DDR4 memory, networking interfaces, an FMC+ expansion port as well as access to the RFMC 2.0 interface.

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## Document Audience and Scope

The purpose of this guide is to familiarize system architects, software developers, and hardware designers with the ZCU216 evaluation board. The ZCU216 evaluation board features the Zynq UltraScale+ RFSoc ZU49DR. The ZCU216 board enables the demonstration, evaluation, and development of numerous applications.

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## Additional Resources

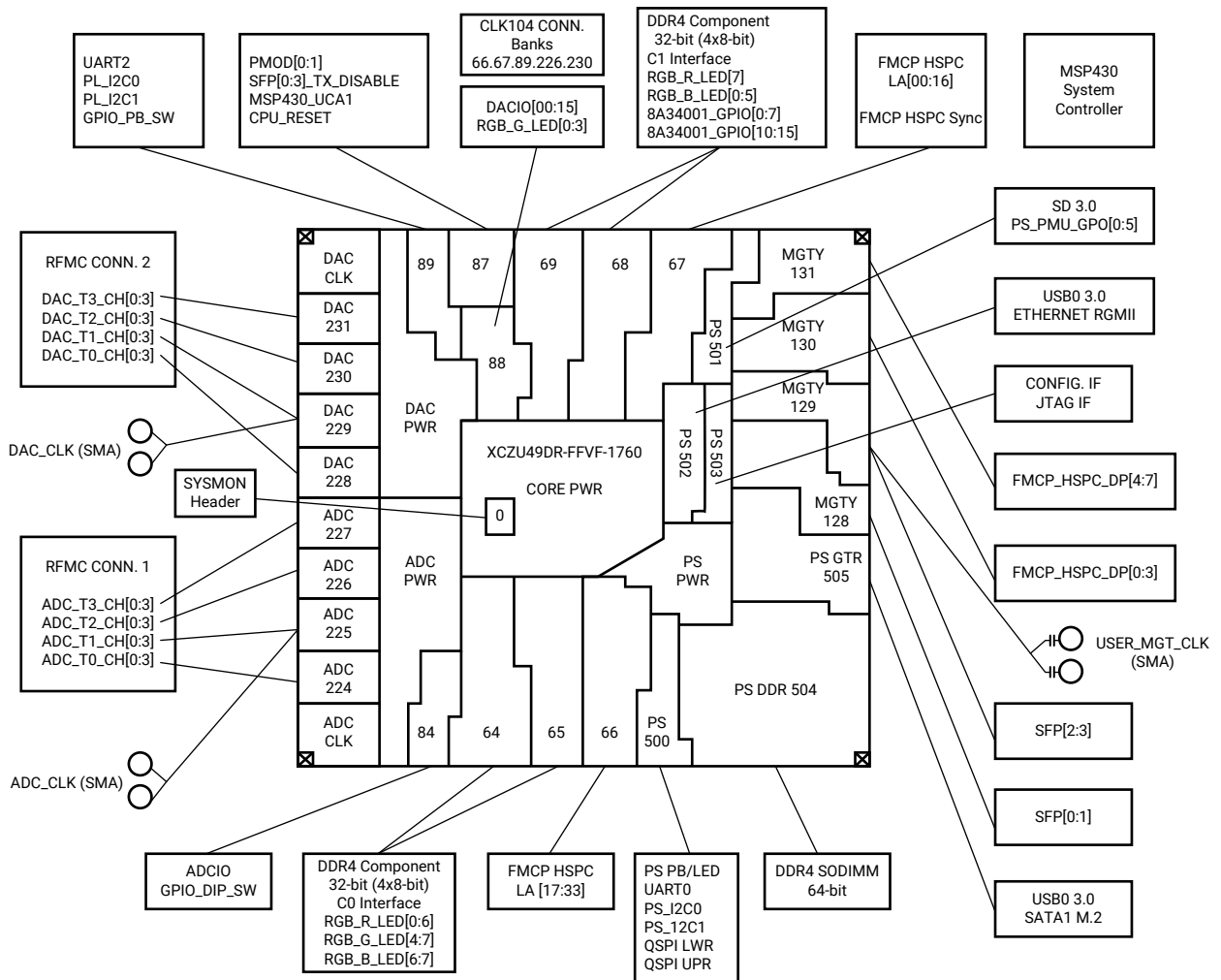
See [Appendix E: Additional Resources and Legal Notices](#) for references to documents, files, and resources relevant to the ZCU216 evaluation board.

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## Block Diagram

A block diagram of the ZCU216 evaluation board is shown in the following figure.

Figure 1: ZCU216 Evaluation Board Block Diagram



X23316-103119

## Board Features

The ZCU216 evaluation board features are listed here. Detailed information for each feature is provided in [Chapter 3: Board Component Descriptions](#).

- XCZU49DR-2, FFVF1760 package
- Form factor: See [Board Specifications](#)
- Configuration from:
  - Dual QSPI
  - Micro-SD card

- USB-to-JTAG Bridge
- PC4 2x7 2 mm JTAG pod flat cable header
- Clocks
  - GTR\_REF\_CLK\_USB3 26 MHz
  - GTR\_REF\_CLK\_SATA 125 MHz
  - CLK104 (various frequencies):
    - CLK104\_PL\_CLK
    - CLK104\_PL\_SYSREF
    - CLK104\_AMS\_SYSREF
    - CLK104\_DDR\_PLY\_CAP\_SYNC
    - CLK104\_ADC\_REFCLK
    - CLK104\_DAC\_REFCLK
  - 8A34001 1588 eCPRI (various frequencies):
    - 8A34001\_Q1\_OUT
    - 8A34001\_Q2\_OUT
    - 8A34001\_Q3\_OUT
    - 8A34001\_Q7\_OUT
    - 8A34001\_Q8\_OUT
    - 8A34001\_Q11\_OUT
  - CLK\_100 100 MHz
  - CLK\_125 125 MHz
  - PS\_REF\_CLK 33.33 MHz
  - USER\_MGT\_SI570 (default 156.25 MHz)
  - USER\_SI570\_C0 (default 300 MHz)
  - USER\_SI570\_C1 (default 300 MHz)
  - ADC\_CLK\_225 (direct connect SMAs)
  - DAC\_CLK\_229 (direct connect SMAs)
  - USER\_MGT\_SMA\_CLK (series capacitor connected SMAs)
- PS DDR4 4 GB 64-bit SODIMM
- PL DDR4 C0 I/F 2 GB 32-bit Component (4x8-bit)

- PL DDR4 C1 I/F 2 GB 32-bit Component (4x8-bit)
- PS GTR (Bank505) assignment
  - USB3 (1 GTR)
  - SATA w/M2 Connector (1 GTR)
  - 2 GTR not used
- PL GTY assignment (4 Quads, 16 total GTY)
  - zSFP+ (4 GTY, 2 on quad GTY128 and 2 on quad GTY129)
  - 8A34001 (1 GTY, quad GTY128)
  - Carlisle CoreHC2 J128 (1 GTY, quad GTY129)
  - FMCP HSCP DP (4 GTY, bank GTY130)
  - FMCP HSCP DP (4 GTY, bank GTY131)
  - 1 GTY not used (quad GTY128)
  - 1 GTY not used (quad GTY129)
- PL FMCP HSCP (FMC+) Connectivity - Full LA[00:33] Bus
- PS MIO Connectivity
  - PS MIO[0:5, 7:12]: Dual QSPI
  - PS MIO[13]: PS\_GPIO2
  - PS MIO[14:17]: 2 channels of I2C
  - PS MIO[18:19]: UART0 (1 of 3 FT4232 UART channels)
  - PS MIO[22:23]: PS\_PB, PS\_LED I/F
  - PS MIO[26]: PMU
  - PS MIO[32:37]: PMU\_GPO[0:5]
  - PS MIO[38]: PS\_GPIO1
  - PS MIO[40:42, 45:51]: SD I/F
  - PS MIO[52:63]: USB3.0
  - PS MIO[64:77]: Ethernet RGMII
- PL I/O Connections:
  - PL User DIP switch (8-position)
  - PL User pushbuttons (5, Geographic N, S, E, W, C)

- PL CPU reset pushbutton
- PL User RGB LEDs (24 total, 8 each R, G, B)
- PL PMOD0/1 (2 R.A. 2x6 Receptacles)
- Security—PSBATT button battery backup
- SYSMON Header
- Operational Switches (Power on/off, PS\_PROG\_B, Boot mode DIP switch)
- Operational Status LEDs (INIT, DONE, PS STATUS, PGOOD)
- Power Management
- System Controller (MSP430)

The ZCU216 provides designers a rapid prototyping platform that uses the XCZU49DR-2FFVF1760 device. The ZU49DR contains many useful processor system (PS) hard block peripherals exposed through the multi-use I/O (MIO) interface and a variety of FPGA programmable logic. The following table lists a brief summary of the resources available within the ZU49DR. A feature set overview, description, and ordering information is provided in the [Zynq UltraScale+ RFSoc Data Sheet: Overview \(DS889\)](#).

**Table 1: Zynq UltraScale+ RFSoc ZU49DR Features and Resources**

| Feature  | Resource Count            |
|--|---------------------------|
| 14-bit 2.5 GSPS RF-DAC with DDC                        | 16                        |
| 14-bit 10 GSPS RF-DAC with DUC                         | 16                        |
| APU: Quad-core Arm® Cortex™-A53 MPCore with CoreSight™ | 1                         |
| RTPU: Dual-core Arm® Cortex™-R5F MPCore with CoreSight | 1                         |
| HD I/O   | 96                        |
| HP I/O   | 312                       |
| MIO banks  | 3 banks, total of 78 pins |
| PS GTR 6 Gb/s transceivers                             | 4 PS-GTRs                 |
| PL GTY 28 Gb/s transceivers                            | 16 GTYs                   |
| System Logic Cells                                     | 930, 300                  |
| CLB Flip-Flops   | 850, 560                  |
| CLB LUTs   | 425, 280                  |
| Max. Distributed RAM (Mb)                              | 13.0                      |
| Block RAM Blocks                                       | 1080 (38 Mb)              |
| UltraRAM Blocks  | 80 (22.5 Mb)              |
| DSP Slices   | 4,272                     |
| PCIe® Gen3 x16 / Gen4 x8 / CCIX (3)                    | 2                         |
| 150G Interlaken  | 1                         |
| 100G Ethernet w/ RS-FEC                                | 2                         |

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# Board Specifications

## Dimensions

Height: 12.225 inches (31.05 cm)

Width: 10.675 inches (27.11 cm)

Thickness: 0.119 inches (0.302 cm)

**Note:** A 3D model of this board is not available.

See the [ZCU216 evaluation board](#) website for the XDC listing and board schematics.

## Environmental

- **Temperature:**

Operating: 0°C to +45°C

Storage: -25°C to +60°C

- **Humidity:** 10% to 90% non-condensing

## Operating Voltage

+12 V<sub>DC</sub>

# Board Setup and Configuration

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## Standard ESD Measures



**CAUTION!** ESD can damage electronic components when they are improperly handled, and can result in total or intermittent failures. Always follow ESD-prevention procedures when removing and replacing components.

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To prevent ESD damage:

- Attach a wrist strap to an unpainted metal surface of your hardware to prevent electrostatic discharge from damaging your hardware.
- When you are using a wrist strap, follow all electrical safety procedures. A wrist strap is for static control. It does not increase or decrease your risk of receiving electric shock when you are using or working on electrical equipment.
- If you do not have a wrist strap, before you remove the product from ESD packaging and installing or replacing hardware, touch an unpainted metal surface of the system for a minimum of five seconds.
- Do not remove the device from the antistatic bag until you are ready to install the device in the system.
- With the device still in its antistatic bag, touch it to the metal frame of the system.
- Grasp cards and boards by the edges. Avoid touching the components and gold connectors on the adapter.
- If you need to lay the device down while it is out of the antistatic bag, lay it on the antistatic bag. Before you pick it up again, touch the antistatic bag and the metal frame of the system at the same time.
- Handle the devices carefully to prevent permanent damage.

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## Board Component Location

The following figure shows the ZCU216 board component locations. Each numbered component shown in the figure is keyed to [Table 2](#).



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**IMPORTANT!** *The following figure is for visual reference only and might not reflect the current revision of the board.*

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**IMPORTANT!** *There could be multiple revisions of this board. The specific details concerning the differences between revisions are not captured in this document. This document is not intended to be a reference design guide and the information herein should not be used as such. Always refer to the schematic, layout, and XDC files of the specific ZCU216 version of interest for such details.*

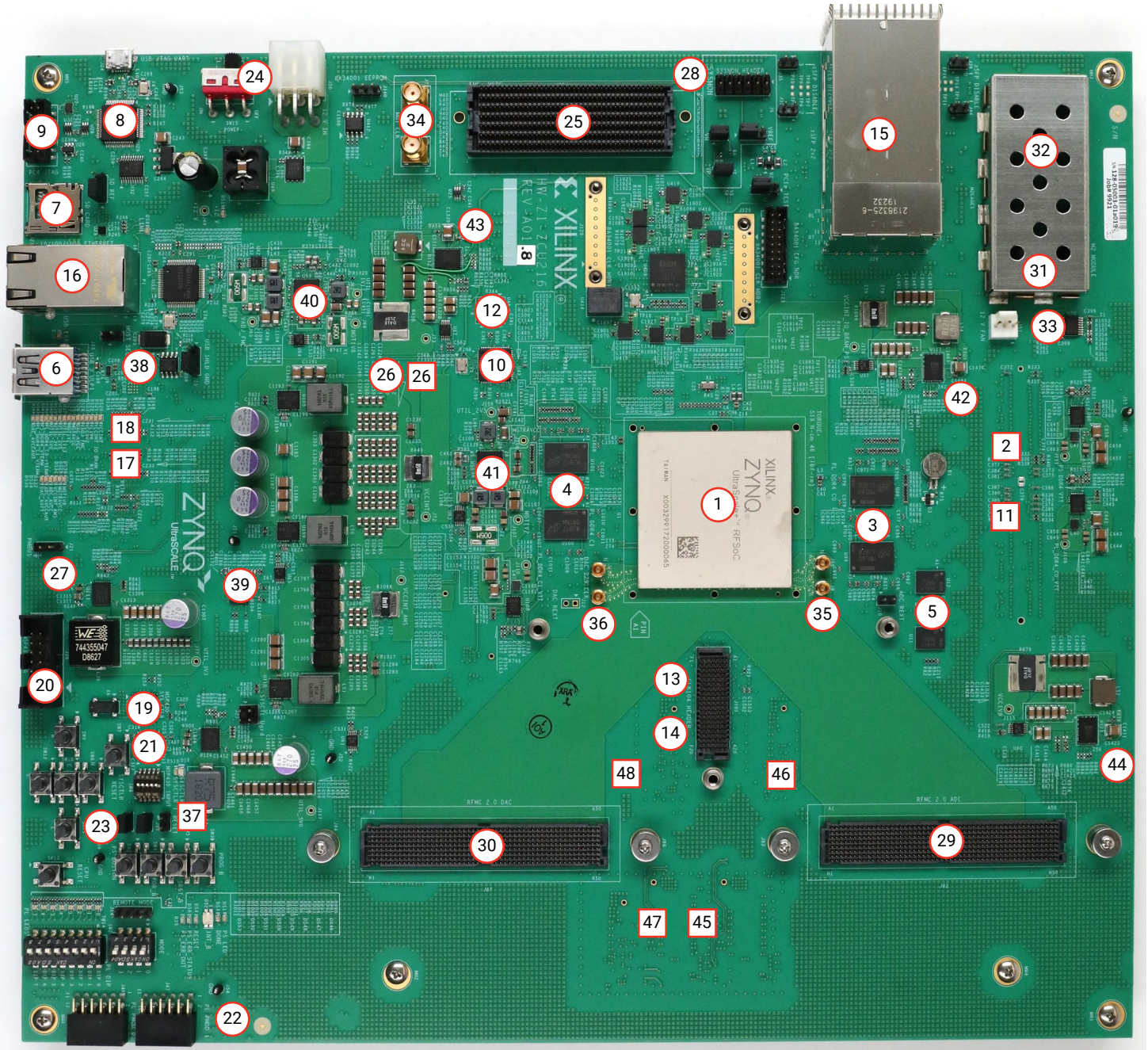
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**Figure 2: ZCU216 Component Locations**

**00** Round callout references a component on the front side of the board

**00** Square callout references a component on the back side of the board



X23462-111419

## Board Component Descriptions

The following table identifies the components and references the respective schematic (038-05003-01) page numbers.

**Table 2: ZCU216 Board Component Locations**

| Callout | Ref. Des.           | Feature<br>[B]=Bottom                                   | Notes   | Schematic Page |
|---------|---------------------|---|---|----------------|
| 1       | U1                  | Zynq® UltraScale+™ RFSoc Fansink                        | XCZU49DR-2FFVF1760<br>COFAN 30-4988-10  |                |
| 2       | J48                 | DDR4 SODIMM SOCKET w/64-bit DDR4 SODIMM                 | LOTES ADDR0067-P001A w/MICRON MTA4ATF51264HZ-2G6E1<br><b>Note:</b> J48 is bottomside. | 43             |
| 3       | U96-U99             | DDR4 C0 4x8-bit Clamshell Component Memory (4 GB)       | Micron MT40A1G8WE-075E<br><b>Note:</b> U96 and U97 are bottomside.                    | 68-71          |
| 4       | U100-U103           | DDR4 C1 4x8-bit Clamshell Component Memory (4 GB)       | Micron MT40A1G8WE-075E<br><b>Note:</b> U102 and U103 are bottomside.                  | 72-75          |
| 5       | U11, U12            | Dual Quad SPI Flash Memory (4 Gb total)                 | Micron MT25QU02CBB8E12-0SIT   | 23             |
| 6       | U6, J18             | USB 3 ULPI Transceiver [B], USB Micro-AB Connector      | SMSC USB3320-EZK, WURTH 692122030100  | 22             |
| 7       | J23                 | SD Card Interface Connector                             | Hirose DMIAA-SF-PET(21)   | 26             |
| 8       | U29, J24            | Quad USB_UART, USB micro-B Connector                    | FTDI FT4232Hx-REEL, Hirose ZX62D-AB-5P8   | 27             |
| 9       | J25                 | JTAG 2 mm 2x7 Flat-Cable Connector                      | Molex 87832-1420  | 27             |
| 10      | U43                 | Fixed Freq. Clock Gen. [B]                              | Silicon Labs SI5341B-D07833-GM  | 39             |
| 11      | U47 (C0), U130 (C1) | User Clock, 300 MHz, 3.3V LVDS [B]                      | Silicon Labs SI570BAB001614DG   | 45             |
| 12      | U48                 | User MGT Clock, 156.250 MHz, 3.3V LVDS                  | Silicon Labs SI570BAB000544DG   | 45             |
| 13      | External            | SFP Jitter Attenuated Clock                             | CLK104 module function (J101)   | 67             |
| 14      | J101                | CLK104 Module Connector                                 | Samtec LPAF-20-03.0-L-06-2-K-TR   | 67             |
| 15      | J29                 | Quad zSFP/zSFP+ Connector                               | TE Connectivity/AMP 2198325-5   | 36             |
| 16      | U33, P1             | 10/100/1000 MHz Ethernet PHY, RJ45 w/Mag                | TI DP83867IRPAP, Wurth 7499111221A  | 28             |
| 17      | U17, U15            | I2C0 Bus Switch, Expander [B]                           | TI PCA9544ARGYR, TI TCA6416APWR   | 24             |
| 18      | U20, U22            | I2C1 Bus Switches [B]                                   | 2 ea. TI TCA9548APWR  | 25             |
| 19      | U38                 | System Controller (SC)                                  | TI MSP430F5342  | 30             |
| 20      | J24                 | MSP430 SC Emulation Cable Connector                     | TYCO 5103308-2  | 30             |
| 21      | SW6, SW7            | System Controller 5-pole DIP Switch and Reset PB Switch | 5-pole C&K SDA05H1SBD, E-Switch TL3301EP100QG   | 30             |
| 22      | J46, J47            | PMOD0/1 RA Receptacles                                  | SULLINS PPC062LJBN-RC   | 42             |



Table 2: ZCU216 Board Component Locations (cont'd)

| Callout | Ref. Des. | Feature<br>[B]=Bottom                 | Notes                                      | Schematic Page |
|---------|-----------|---------------------------------------|--|----------------|
| 23      | SW8-SW12  | User Pushbutton Switches, active-High | E-Switch TL3301EP100QG (N,W,C,E,S pattern) | 40             |
|         | SW14      | User 8-pole DIP Switch, active-High   | C&K SDA08H1SBD                             | 40             |
|         | SW13      | CPU_RESET Pushbutton, active-High     | E-Switch TL3301EP100QG                     | 40             |
|         | DS46-DS53 | Eight RGB LEDs, active-High           | PL GPIO LEDs, Rohm SMLP36RGB2W3R           | 41             |
|         | SW1       | PS (MIO22) Pushbutton                 | E-Switch TL3301EP100QG                     | 11             |
|         | SW3       | PS_PROG Pushbutton                    | E-Switch TL3301EP100QG                     | 12             |
|         | SW4, SW5  | PS_POR_B, PS_SRST_B Pushbuttons       | E-Switch TL3301EP100QG                     | 12             |
|         | J15       | 2-PIN HDR PS_POR_B                    | SULLINS PBC02SAAN                          | 12             |
|         | J16       | 2-PIN HDR PS_SRST_B                   | SULLINS PBC02SAAN                          | 12             |
|         | J17       | 2-PIN HDR MR_B (U5 RST)               | SULLINS PBC02SAAN                          | 12             |
| 24      | SW15      | Power ON/OFF Slide Switch             | C&K 1201M2S3AQE2                           | 46             |
|         | J50       | Power Connector                       | MOLEX 39-30-1060                           | 46             |
| 25      | J28       | FMCP HSPC Connector                   | Samtec ASP_184329_01                       | 31-35          |
| 26      | -         | Power Management System (top, [B])    | Infineon Regulators                        | 47-63          |
| 27      | J21       | PMBUS Connector                       | SULLINS PBC03SAAN                          | 24             |
| 23      | SW2       | FPGA MODE 4-pole DIP Switch           | 4-pole C and K SDA04H1SBD                  | 12             |
| 28      | J5        | SYSMON 2X6 Vertical Male Pin Header   | SULLINS PBC06DAAN                          | 3              |
| 29      | J82       | RFMC 2.0 Connector 1                  | Samtec LPAF-50-030-L-08-2-K-TR             | 64             |
| 30      | J87       | RFMC 2.0 Connector 2                  | Samtec LPAF-50-030-L-08-2-K-TR             | 65             |
| 31      | U36       | SATA M.2 Connector                    | Amphenol MDT420M02001                      | 29             |
| 32      | M2CAGE1   | M.2 Conn. EMI Cage                    | Leader Tech 20S-CBSFNSV-1.0x2.25x0.40      | 29             |
| 33      | U50       | Fan Controller                        | Maxim MAX6643LBBAEE++                      | 46             |
|         | J57       | Fan Header (Keyed 3-pin)              | Molex 22-11-2032                           | 46             |
| 34      | J6, J7    | SMA USER_SMA_MGT_CLOCK                | Rosenberger 32K10K-400L5                   | 8              |
| 35      | J8, J98   | ADC Clock Connectors                  | CARLISLE TM14-0084-00                      | 9              |
| 36      | J99, J100 | DAC Clock Connectors                  | CARLISLE TM14-0084-00                      | 10             |
| 37      | U5        | PWR-ON RESET IC [B]                   | Maxim MAX16025TE+                          | 12             |
| 38      | U7        | USB3 PWR. SWITCH                      | Micrel MIC2544A-1YM                        | 22             |
|         | J20       | USB 3.0 J18 Shield Header             | SULLINS PBC03SAAN                          | 22             |
|         | J19       | VBUS_SEL Option Header                | SULLINS PBC05SAAN                          | 22             |
| 39      | U104      | INFINEON PMIC1                        | Infineon IR35215MTRPBF                     | 47             |
| 40      | U53       | INFINEON PMIC2                        | Infineon IRPS5401MXI04TRP                  | 50             |
| 41      | U55       | INFINEON PMIC3                        | Infineon IRPS5401MXI04TRP                  | 52             |
| 42      | U127      | VCCINT PS/BRAM 18A Regulator          | Infineon IR38164                           | 53             |
| 43      | U112      | MGTAVCC 4A Regulator                  | Infineon IR38164                           | 54             |
| 44      | U123      | VCC1V8 8A Regulator                   | Infineon IR38164                           | 55             |

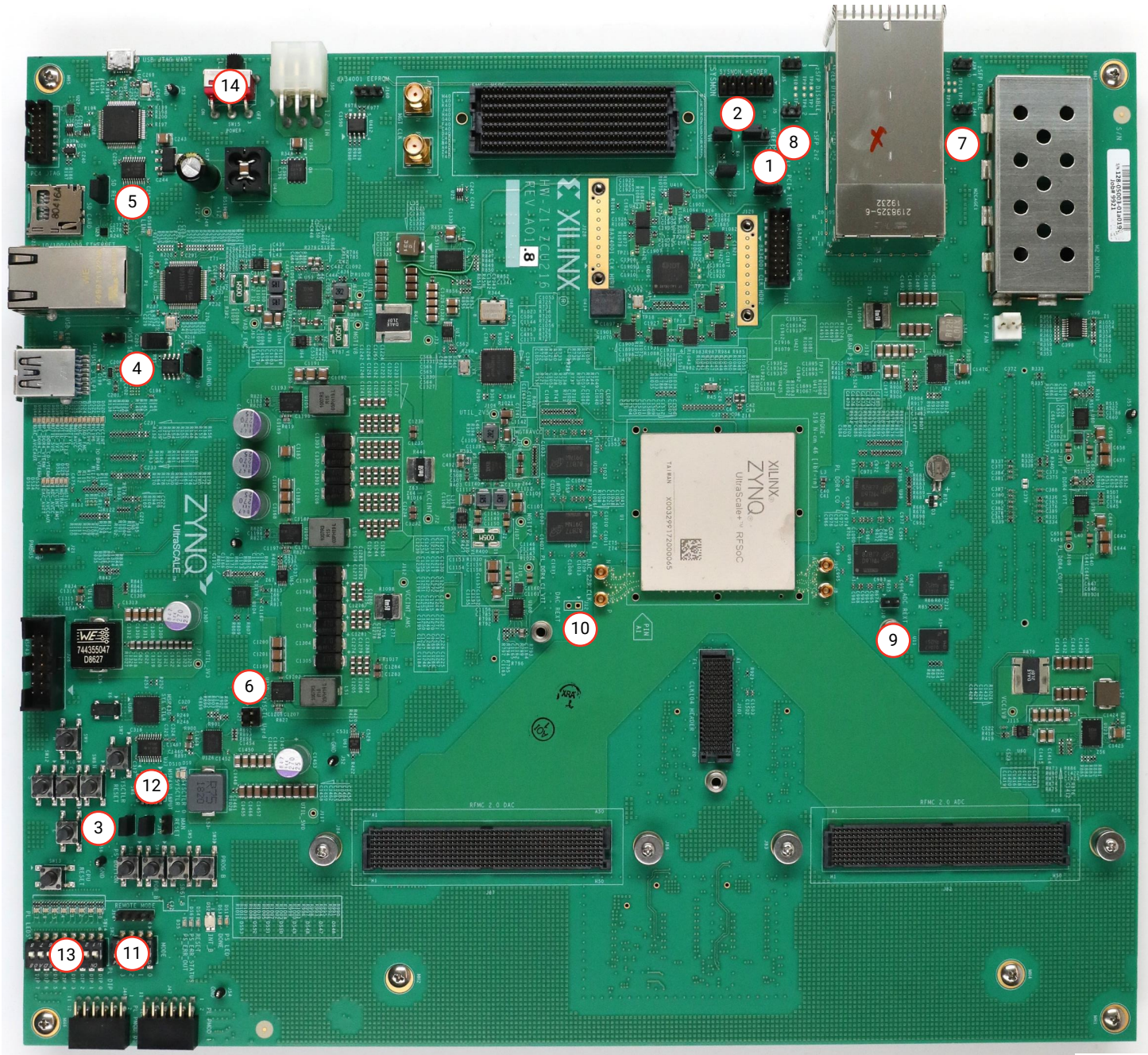
Table 2: ZCU216 Board Component Locations (cont'd)

| Callout | Ref. Des.     | Feature<br>[B]=Bottom        | Notes         | Schematic Page |
|---------|---------------|------------------------------|---------------|----------------|
| 45      | U115,<br>U116 | ADC/DAC AVCC Regulators [B]  | MPS MPM3683-7 | 56             |
| 46      | U114          | ADC AVCCAUX 2A Regulator [B] | MPS MPM3833C  | 57             |
| 47      | U125          | DAC AVCCAUX Regulator [B]    | MPS MPM3833C  | 58             |
| 48      | U118          | DAC AVTT Regulator [B]       | MPS MPM3833C  | 58             |

## Default Jumper and Switch Settings

The following figure shows the ZCU216 board jumper header and switch locations. Each numbered component shown in the figure is keyed to the applicable table in this section. Both tables reference the respective schematic page numbers.

Figure 3: Board Jumper Header and Switch Locations



X23508-111119

## Jumpers

The following table lists the default jumper settings.



Table 3: Default Jumper Settings

| Callout                         | Reference Design                   | Function   | Default | Schematic Page |
|---------------------------------|------------------------------------|--|---------|----------------|
| 1                               | J1                                 | POR_OVERRIDE   | 2-3     | 3              |
|                                 |                                    | 1-2: Enable  |         |                |
|                                 |                                    | 2-3: Disable   |         |                |
| 2                               | J2                                 | SYSMON I2C Address                                     | ON      | 3              |
|                                 |                                    | OFF: SYSMON_VP_R floating                              |         |                |
|                                 |                                    | ON: SYSMON_VP_P pulled down                            |         |                |
|                                 | J3                                 | SYSMON I2C Address                                     | ON      | 3              |
|                                 |                                    | OFF: SYSMON_VN_R floating                              |         |                |
|                                 |                                    | ON: SYSMON_VP_N pulled down                            |         |                |
| J4                              | SYSMON VREFP                       | 1-2  | 3       |                |
|                                 | 1-2: 1.25V VREFP connected to fpga |  |         |                |
|                                 | 2-3: VREFP connected to GND        |  |         |                |
| 3                               | J15                                | Reset Sequencer PS_POR_B                               | ON      | 12             |
|                                 |                                    | OFF: Sequencer does not control PS_POR_B               |         |                |
|                                 |                                    | ON: Sequencer can control PS_POR_B                     |         |                |
|                                 | J16                                | Reset Sequencer PS_SRST_B                              | ON      | 12             |
|                                 |                                    | OFF: Sequencer does not control PS_SRST_B              |         |                |
|                                 |                                    | ON: Sequencer can control PS_SRST_B                    |         |                |
|                                 | J17                                | Reset Sequencer inhibit                                | OFF     | 12             |
|                                 |                                    | OFF: Sequencer normal operation                        |         |                |
|                                 |                                    | ON: Sequencer inhibit (resets will stay asserted)      |         |                |
| 4                               |                                    | ULPI USB3320 U6 ULPIO_VBUS_SEL option jumper           | OFF     | 22             |
|                                 | J19                                | ON: Selects U17 MIC2544A switch 5V for VBUS            |         |                |
|                                 |                                    | OFF: Normal operation, VBUS from J18 USB3.0 conn.      |         |                |
|                                 | J20                                | USB 3.0 Connector J18 Shield connection options        | 2-3     | 22             |
|                                 |                                    | 1-2: J20 shield capacitor C171 to GND                  |         |                |
| 2-3: J20 shield directly to GND |                                    |  |         |                |
| 5                               | J22                                | SD3.0 U107 IP4856CX25 level-trans. ref. voltage select | 1-2     | 26             |
|                                 |                                    | 1-2: Track SD3.0 J12 socket UTIL_3V3 3.3V              |         |                |
|                                 |                                    | 2-3: GND = revert to internal voltage reference        |         |                |
| 6                               | J27                                | MPS430 U38 RST_B and TEST pin options                  | open    | 30             |
|                                 |                                    | 1-2: MSP430_RST_B connected to PMOD1_0                 |         |                |
|                                 |                                    | 3-4: MSP430_TEST connected to PMOD1_1                  |         |                |

Table 3: Default Jumper Settings (cont'd)

| Callout | Reference Design | Function                                      | Default | Schematic Page |
|---------|------------------|---|---------|----------------|
| 7       | J39              | zSFP0 J29 LT enable jumper                    | OFF     | 38             |
|         |                  | ON: zSFP0 TX_DISABLE = GND = enabled          |         |                |
|         |                  | OFF: zSFP0 TX_DISABLE = high = disabled       |         |                |
|         | J44              | zSFP1 J29 LL enable jumper                    | OFF     | 38             |
|         |                  | ON: zSFP1 TX_DISABLE = GND = enabled          |         |                |
|         |                  | OFF: zSFP1 TX_DISABLE = high = disabled       |         |                |
| 8       | J32              | zSFP2 J29 RT enable jumper                    | OFF     | 38             |
|         |                  | ON: zSFP2 TX_DISABLE = GND = enabled          |         |                |
|         |                  | OFF: zSFP2 TX_DISABLE = high = disabled       |         |                |
|         | J35              | zSFP3 J29 RL enable jumper                    | OFF     | 38             |
|         |                  | ON: zSFP3 TX_DISABLE = GND = enabled          |         |                |
|         |                  | OFF: zSFP3 TX_DISABLE = high = disabled       |         |                |
| 9       | J10              | ZU49DR RFSoc U1 ADC Bank 224 ADC_REXT select  | OFF     | 9              |
|         |                  | ON: Bank 224 ADC_REXT pin AF9 = GND           |         |                |
|         |                  | OFF: Bank 224 ADC_REXT pin AF9 = 2.49K to GND |         |                |
| 10      | J12              | ZU49DR RFSoc U1 DAC Bank 228 DAC_REXT select  | OFF     | 10             |
|         |                  | ON: Bank 228 DAC_REXT pin U9 = GND            |         |                |
|         |                  | OFF: Bank 228 DAC_REXT pin U9 = 2.49K to GND  |         |                |

## Switches

The following table lists the default switch settings.

Table 4: Default Switch Settings

| Callout | Reference Design | Function                            | Default  | Schematic Page |
|---------|------------------|-------------------------------------|----------|----------------|
| 11      | SW2              | RFSoc U1 Mode 4-Pole DIP Switch     | 0010     | 12             |
|         |                  | Switch OFF = 1 = High; ON = 0 = Low |          |                |
|         |                  | Mode = SW1[4:1] = Mode[3:0]         |          |                |
|         |                  | JTAG = ON,ON,ON,ON = 0000           |          |                |
|         |                  | QSPI32 = ON,ON,OFF,ON = 0010        |          |                |
|         |                  | SD = OFF,OFF,OFF,ON = 1110          |          |                |
| 12      | SW6              | MSP432 U38 5-Pole GPIO DIP Switch   | 11111    | 30             |
|         |                  | Switch OFF = 1 = High; ON = 0 = Low |          |                |
| 13      | SW14             | GPIO 8-Pole DIP Switch              | 00000000 | 40             |
|         |                  | Switch OFF = 0 = Low; ON = 1 = High |          |                |
| 14      | SW15             | Main Power Slide Switch             | OFF      | 46             |



**CAUTION!** Do NOT plug a PC ATX power supply 6-pin connector into the ZCU216 board power connector J50. The ATX 6-pin connector has a different pinout than J50. Connecting an ATX 6-pin connector into J50 damages the ZCU216 board and voids the board warranty.

See [Power On/Off Slide Switch](#) for more information.

## Zynq UltraScale+ RFSoc XCZU49DR Configuration

Zynq UltraScale+ RFSoc ZU49DR uses a multi-stage boot process documented in the Boot and Configuration chapter of the *Zynq UltraScale+ Device Technical Reference Manual* ([UG1085](#)).

Switch SW2 configuration option settings are identified in the following table.

**Table 5: Mode Switch SW2 Configuration Option Settings**

| Mode   | Mode Pins [3:0]   | Mode SW2 [4:1] <sup>2</sup> |
|--------|-------------------|-----------------------------|
| JTAG   | 0000              | ON,ON,ON,ON                 |
| QSPI32 | 0010 <sup>1</sup> | ON,ON,OFF,ON                |
| SD     | 1110              | OFF,OFF,OFF,ON              |

**Notes:**

1. Default switch setting.
2. Switch OFF = 1 = High; ON = 0 = Low. See callout 11 in [Table 4](#).

### JTAG

Vivado® Design Suite or third-party tools can establish a JTAG connection to the Zynq UltraScale+ RFSoc through the FTDI FT4232 USB-to-JTAG/USB UART device (U29) connected to micro-USB connector (J24).

### QSPI

Use the following steps to boot from the dual QSPI non-volatile configuration memory.

1. Store a valid Zynq UltraScale+ RFSoc boot image into the QSPI flash devices (U11, U12, MIO[0:12] QSPI interface).
2. Set the boot mode pins SW2 [4:1] as indicated in the table above for QSPI32.
3. Either power-cycle or press the power-on reset (POR) pushbutton. SW2 is callout 11 in [Figure 3](#).



## SD

Use the following steps to boot from an SD card.

1. Store a valid Zynq UltraScale+ RFSoc boot image file onto an SD card (plugged into SD socket J23) connected to the MIO[39:51] SD interface.
2. Set the boot mode pins SW3 [4:1] as indicated in the table above for SD.
3. Either power-cycle or press the power-on reset (POR) pushbutton. SW2 is callout 11 in [Figure 3](#).

See the *Zynq UltraScale+ Device Technical Reference Manual* ([UG1085](#)) for more information about Zynq UltraScale+ RFSoc configuration options.

# Board Component Descriptions

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## Overview

This chapter provides a description of the board's components and features. [Table 2](#) identifies the components and references the respective schematic page numbers. Component locations are shown in [Figure 2](#).

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## Component Descriptions

### Zynq UltraScale+ RFSoc XCZU49DR

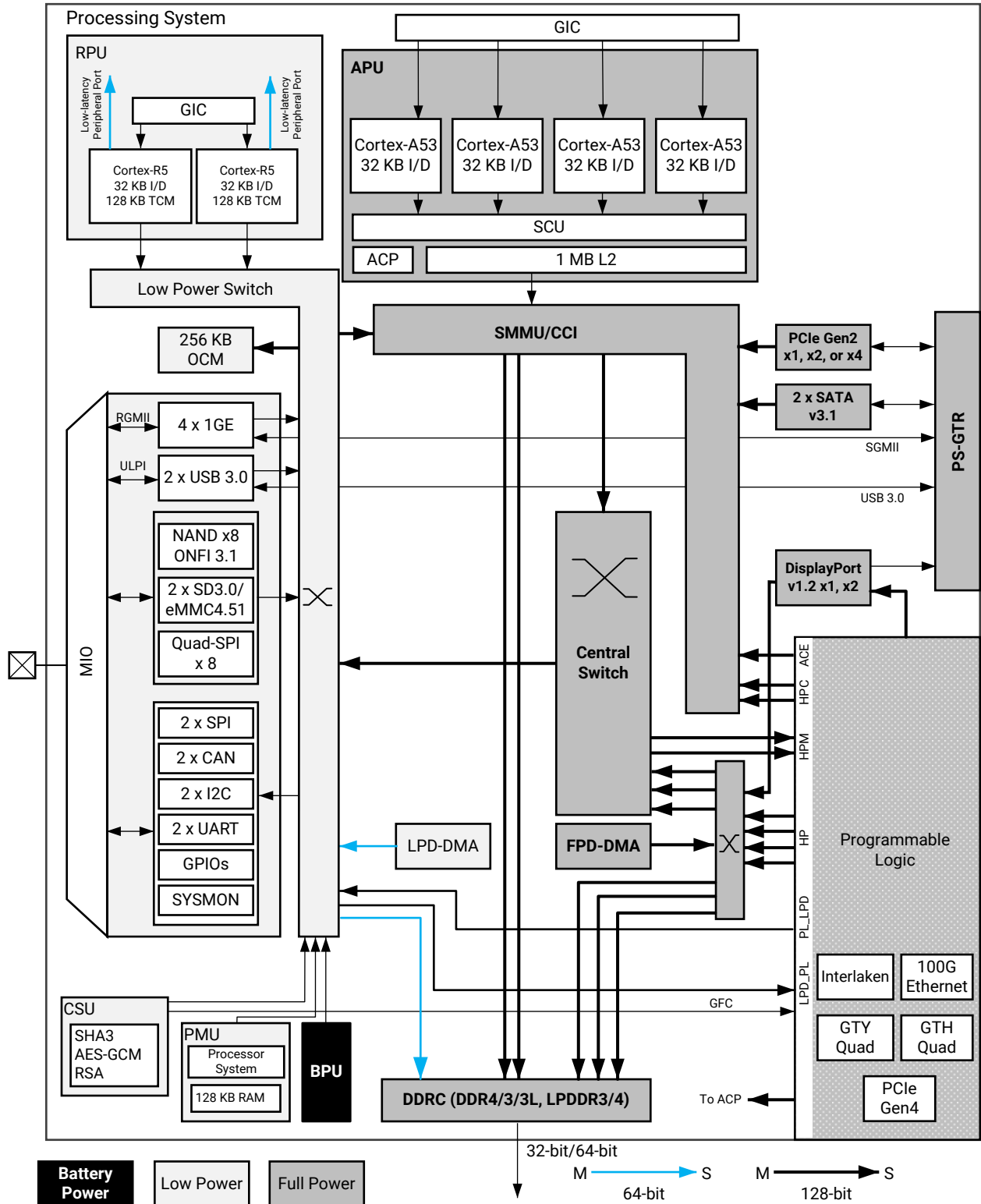
[[Figure 2](#), callout 1]

The ZCU216 board is populated with the Zynq<sup>®</sup> UltraScale+<sup>™</sup> RFSoc XCZU49DR-2FFVF1760 which combines a powerful processing system (PS) and user-programmable logic (PL) in the same device. The processing system in a Zynq UltraScale+ RFSoc features the Arm<sup>®</sup> flagship Cortex<sup>™</sup>-A53 64-bit quad-core processor and Cortex<sup>™</sup>-R5F dual-core real-time processor.

The  $V_{CCINT}$  supplies are user adjustable through PMBUS with the voltage ranges to support whichever Zynq UltraScale+ RFSoc speed grade is on the evaluation board. See the *Zynq UltraScale+ RFSoc Data Sheet: DC and AC Switching Characteristics* ([DS926](#)) for more information.

### Top-Level Block Diagram

Figure 4: Zynq UltraScale+ RFSoc Top-Level Block Diagram



X23309-031220

The Zynq UltraScale+ RFSoc PS block has two major processing units:

- Cortex-A53 application processing unit (APU)-ARM v8 architecture-based 64-bit quad-core multiprocessing CPU.
- Cortex-R5F real-time processing unit (RPU)-ARM v7 architecture-based 32-bit dual real-time processing unit with dedicated tightly coupled memory (TCM).

The Zynq UltraScale+ RFSoc PS has four high-speed serial I/O (HSSIO) interfaces supporting the following protocols:

- Integrated block for PCI Express® interface-PCIe® base specification version 2.1 compliant.
- SATA 3.1 specification compliant interface.
- USB 3.0 interface-compliant to USB 3.0 specification implementing a 5 Gb/s line rate.
- Serial GMII interface-supports a 1 Gb/s SGMII interface.

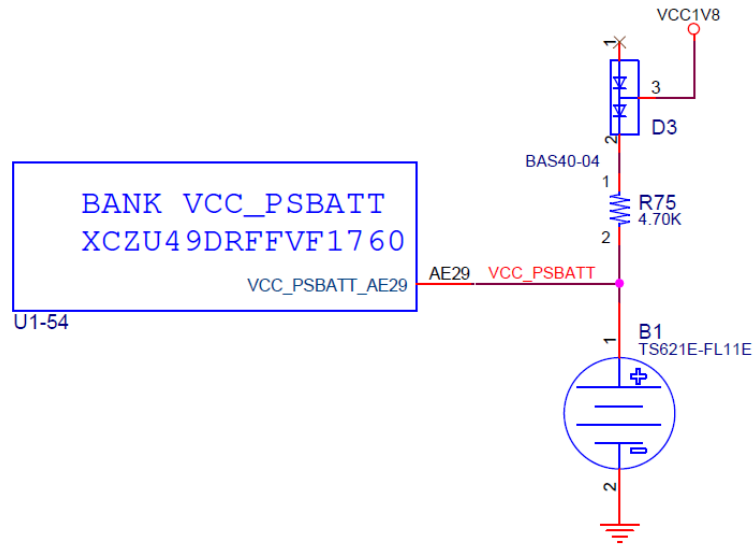
The PS and PL can be coupled with multiple interfaces and other signals to effectively integrate user-created hardware accelerators and other functions in the PL logic that are accessible to the processors. They can also access memory resources in the processing system. The PS I/O peripherals, including the static/flash memory interfaces share a multiplexed I/O (MIO) of up to 78 MIO pins. Zynq UltraScale+ RFSocPs can also use the I/O in the PL domain for many of the PS I/O peripherals. This is done through an extended multiplexed I/O interface (EMIO) and boots at power-up or reset.

For additional information on Zynq UltraScale+ RFSoc, see the *Zynq UltraScale+ RFSoc Data Sheet: Overview* ([DS889](#)) and the *Zynq UltraScale+ Device Technical Reference Manual* ([UG1085](#)) for more information about configuration options for the Zynq UltraScale+ RFSoc.

## Encryption Key Battery Backup Circuit

The Zynq UltraScale+ RFSoc ZU49DR U1 implements bit stream encryption key technology. The ZCU216 board provides the encryption key backup battery circuit shown in the figure below.

Figure 5: Encryption Key Battery Backup Circuit



The Seiko TS621E rechargeable 1.5V lithium button-type battery B1 is soldered to the board with the positive output connected to the ZU49DR RFSoc U1 VCC\_PSBATT pin AE29. The battery supply current IBATT specification is 150 nA maximum when board power is off. B1 is charged from the VCC1V8 1.8V rail through a series diode with a typical forward voltage drop of 0.38V and 4.7  $\Omega$ K current limit resistor. The nominal charging voltage is 1.42V.

## I/O Voltage Rails

The ZU49DR RFSoc PL I/O bank voltages on the ZCU216 board are listed in the following table.

Table 6: I/O Voltage Rails

| ZU49DR      | Power Net Name        | Voltage | Connected To  |
|-------------|-----------------------|---------|---|
| PL Bank 64  | VCC1V2                | 1.2V    | PL_C0_DDR4_DQ[0:31]                                       |
| PL Bank 65  | VCC1V2                | 1.2V    | PL_C0_DDR4_ADDR/CTL, SYSMON_SDA/SCL, MSP430_GPIO[0:3]     |
| PL Bank 66  | VADJ_FMC <sup>1</sup> | 1.8V    | FMCP_HSPC LA BUS [17:33]                                  |
| PL Bank 67  | VADJ_FMC <sup>1</sup> | 1.8V    | FMCP_HSPC LA BUS [00:16]                                  |
| PL Bank 68  | VCCIV2                | 1.2V    | PL_C1_DDR4_DQ[0:31]                                       |
| PL Bank 69  | VCC1V2                | 1.2V    | PL_C1_DDR4_ADDR/CTL, 8A34001_GPIO[0:15]                   |
| PL Bank 84  | VCC1V8                | 1.8V    | ADCIO[00:15], GPIO_DIP_SW[0:7]                            |
| PL Bank 87  | VCC1V8                | 1.8V    | DACIO[0:15], RGB_G_LED[0:3]                               |
| PL Bank 88  | VCC1V8                | 1.8V    | PMOD0&1[0:7], SFP[0:3]_TX_DISABLE_B, CPU_RESET            |
| PL Bank 89  | VCC1V8                | 1.8V    | UART2, PL_I2C0/1, CLK104 I/F, CLK_100, GPIO_SW[N,W,C,E,S] |
| PS Bank 500 | VCC1V8                | 1.8V    | QSPI LWR/UPR, PS_GPIO2, MIO_I2C0/1, UART0, MIO_LED/PB     |
| PS Bank 501 | VCC1V8                | 1.8V    | PMU_INPUT, PMU_GPO[0:5], SDIO I/F, PS_GPIO1               |
| PS Bank 502 | VCC1V8                | 1.8V    | USB (3.0) I/F, ENET I/F                                   |

Table 6: I/O Voltage Rails (cont'd)

| ZU49DR      | Power Net Name | Voltage | Connected To                |
|-------------|----------------|---------|-----------------------------|
| PS Bank 503 | VCC1V8         | 1.8V    | PS CONFIG I/F               |
| PS Bank 504 | VCC1V2         | 1.2V    | PS_DDR4_SODIMM (64-BIT) I/F |

**Notes:**

- The ZCU216 board is shipped with VADJ\_FMC set to 1.8V by the MSP430 system controller.

## PS DDR4 SODIMM Socket

[Figure 2, callout 2]

The PS-side memory is wired to the Zynq UltraScale+ RFSoc DDRC Bank 504 hard memory controller. A 64-bit single rank DDR4 SODIMM is inserted into socket J48. The ZCU216 is shipped with a DDR4 SODIMM installed:

- Manufacturer: Micron
- Part Number: MTA4ATF51264HZ-2G6E1
- Description:
  - 4 GByte DDR4 260-Pin SODIMM
  - Single Rank (x 16-bit components)
  - 512 Mb x 64-bit
  - 2666 MT/s

The ZCU216 ZU49DR RFSoc (ZU49DR supports 2400MT/s) PS DDR interface performance is documented in the *Zynq UltraScale+ RFSoc Data Sheet: DC and AC Switching Characteristics (DS926)*.

The ZCU216 DDR4 SODIMM interface adheres to the constraints guidelines documented in the PCB guidelines for DDR4 section of the *UltraScale Architecture PCB Design User Guide (UG583)*. The DDR4 SODIMM interface is a 40Ω impedance implementation. Other memory interface details are also available in the *UltraScale Architecture-Based FPGAs Memory IP LogiCORE IP Product Guide (PG150)*.

For additional details, see the Micron MTA4ATF51264HZ-2G6E1 data sheet on the [Micron Technology](#) website.

The detailed RFSoc connections for the feature described in this section are documented in the ZCU216 board XDC file, referenced in [Appendix B: Xilinx Design Constraints](#).

## PL C0 I/F DDR4 Component Memory

[Figure 2, callout 3]

The 4 GB, 32-bit wide DDR4 memory system is comprised of four 1 Gb x 8 SDRAM (Micron MT40A1G8WE-075E), U96-U99. This memory system is connected to PL-side ZU49DR banks 64 and 65. The DDR4 0.6V PL\_DDR4\_C0\_VTT termination voltage is supplied from IR3897 sink-source regulator U79.

- Manufacturer: Micron
- Part Number: MT40A1G8WE-075E
- Description:
  - 8 Gb (1 Gb x 8)
  - 1.2V 78-ball FBGA
  - DDR4-2666

The ZCU216 ZU49DR RFSoc PL DDR interface performance is documented in the *Zynq UltraScale+ RFSoc Data Sheet: DC and AC Switching Characteristics* (DS926).

The ZCU216 board DDR4 32-bit component memory interface adheres to the constraints guidelines documented in the PCB guidelines for DDR4 section of *UltraScale Architecture PCB Design User Guide* (UG583). The ZCU216 DDR4 component interface is a 40Ω impedance implementation. Other memory interface details are also available in the *UltraScale Architecture-Based FPGAs Memory IP LogiCORE IP Product Guide* (PG150).

For additional details, see the Micron MT40A1GWE-075E data sheet on the [Micron Technology](#) website.

The detailed RFSoc connections for the feature described in this section are documented in the ZCU216 board XDC file, referenced in [Appendix B: Xilinx Design Constraints](#).

## PL C1 I/F DDR4 Component Memory

[Figure 2, callout 4]

The 4 GB, 32-bit wide DDR4 memory system is comprised of four 1 Gb x 8 SDRAM (Micron MT40A1G8WE-075E), U100-U103. This memory system is connected to PL-side ZU49DR banks 68 and 69. The DDR4 0.6V PL\_DDR4\_C1\_VTT termination voltage is supplied from IR3897 sink-source regulator U80.

- Manufacturer: Micron
- Part Number: MT40A1G8WE-075E

- Description:
  - 8 Gb (1 Gb x 8)
  - 1.2V 78-ball FBGA
  - DDR4-2666

The ZCU216 ZU49DR RFSoc PL DDR interface performance is documented in the *Zynq UltraScale+ RFSoc Data Sheet: DC and AC Switching Characteristics* ([DS926](#)).

The ZCU216 board DDR4 32-bit component memory interface adheres to the constraints guidelines documented in the PCB guidelines for DDR4 section of *UltraScale Architecture PCB Design User Guide* ([UG583](#)). The ZCU216 DDR4 component interface is a 40Ω impedance implementation. Other memory interface details are also available in the *UltraScale Architecture-Based FPGAs Memory IP LogiCORE IP Product Guide* ([PG150](#)).

For additional details, see the Micron MT40A1GWE-075E data sheet on the [Micron Technology](#) website.

The detailed RFSoc connections for the feature described in this section are documented in the ZCU216 board XDC file, referenced in [Appendix B: Xilinx Design Constraints](#).

## PSMIO

The following table provides PS MIO peripheral mapping implemented on the ZCU216 board. See the *Zynq UltraScale+ Device Technical Reference Manual* ([UG1085](#)) for more information on PS MIO peripheral mapping.

*Table 7: MIO Peripheral Mapping*

| MIO[0:25] Bank 500 |                         | MIO[26:51] Bank 501 |                         | MIO[52:77] Bank 502 |      |
|--------------------|-------------------------|---------------------|-------------------------|---------------------|------|
| 0                  | QSPI_LWR                | 26                  | PMU IN                  | 52                  | USB0 |
| 1                  | QSPI_LWR                | 27                  | Not assigned/no connect | 53                  | USB0 |
| 2                  | QSPI_LWR                | 28                  | Not assigned/no connect | 54                  | USB0 |
| 3                  | QSPI_LWR                | 29                  | Not assigned/no connect | 55                  | USB0 |
| 4                  | QSPI_LWR                | 30                  | Not assigned/no connect | 56                  | USB0 |
| 5                  | QSPI_LWR                | 31                  | Not assigned/no connect | 57                  | USB0 |
| 6                  | Not assigned/no connect | 32                  | PMU GPO                 | 58                  | USB0 |
| 7                  | QSPI_UPR                | 33                  | PMU GPO                 | 59                  | USB0 |
| 8                  | QSPI_UPR                | 34                  | PMU GPO                 | 60                  | USB0 |
| 9                  | QSPI_UPR                | 35                  | PMU GPO                 | 61                  | USB0 |
| 10                 | QSPI_UPR                | 36                  | PMU GPO                 | 62                  | USB0 |
| 11                 | QSPI_UPR                | 37                  | PMU GPO                 | 63                  | USB0 |
| 12                 | QSPI_UPR                | 38                  | GPIO                    | 64                  | GEM3 |
| 13                 | GPIO                    | 39                  | SD1                     | 65                  | GEM3 |



Table 7: MIO Peripheral Mapping (cont'd)

| MIO[0:25] Bank 500 |                         | MIO[26:51] Bank 501 |                         | MIO[52:77] Bank 502 |       |
|--------------------|-------------------------|---------------------|-------------------------|---------------------|-------|
| 14                 | I2C0                    | 40                  | SD1                     | 66                  | GEM3  |
| 15                 | I2C0                    | 41                  | SD1                     | 67                  | GEM3  |
| 16                 | I2C1                    | 42                  | SD1                     | 68                  | GEM3  |
| 17                 | I2C1                    | 43                  | Not assigned/no connect | 69                  | GEM3  |
| 18                 | UART0                   | 44                  | Not assigned/no connect | 70                  | GEM3  |
| 19                 | UART0                   | 45                  | SD1                     | 71                  | GEM3  |
| 20                 | Not assigned/no connect | 46                  | SD1                     | 72                  | GEM3  |
| 21                 | Not assigned/no connect | 47                  | SD1                     | 73                  | GEM3  |
| 22                 | GPIO                    | 48                  | SD1                     | 74                  | GEM3  |
| 23                 | GPIO                    | 49                  | SD1                     | 75                  | GEM3  |
| 24                 | Not assigned/no connect | 50                  | SD1                     | 76                  | MDIO3 |
| 25                 | Not assigned/no connect | 51                  | SD1                     | 77                  | MDIO3 |

## Quad-SPI Flash Memory (MIO 0–12)

[Figure 2, callout 5]

The Micron dual MT25QU02GCBB8E12-0SIT serial NOR flash Quad-SPI memories are capable of holding the boot image for the Zynq UltraScale+ RFSoc. This interface is used to support QSPI32 boot mode as defined in the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085).

The dual Quad-SPI flash memory located at U11/U12 provides 4 Gb of non-volatile storage that can be used for configuration and data storage.

- Part number: MT25QU02GCBB8E12-0SIT (Micron)
- Description:
  - 2 Gb/256 MB
  - 2.7V – 3.6V 24-ball TBGA
  - 90 MHz DTR/133 MHz STR
- Datapath width: 8 bits
- Data rate: Various depending on Single/Dual/Quad mode

The configuration and Quad-SPI section of the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085) provides details on using the Quad-SPI flash memory. For more QSPI details, see the Micron MT25QU02GCBB8E12-0SIT data sheet on the [Micron Technology](https://www.micron.com) website.

The detailed RFSoc connections for the feature described in this section are documented in the ZCU216 board XDC file, referenced in [Appendix B: Xilinx Design Constraints](#).

## GPIO (MIO 13, 38)

These two (2) GPIO bits are connected to the U38 MSP430 system controller for general purpose signaling or communications between the Zynq UltraScale+ RFSoc and the MSP430 system controller. These signals are level-shifted by TSX0108E U37. The connections between the U38 system controller and the ZU49DR RFSoc are listed in following table.

*Table 8: System Controller U38 GPIO Connections to ZU49DR U1*

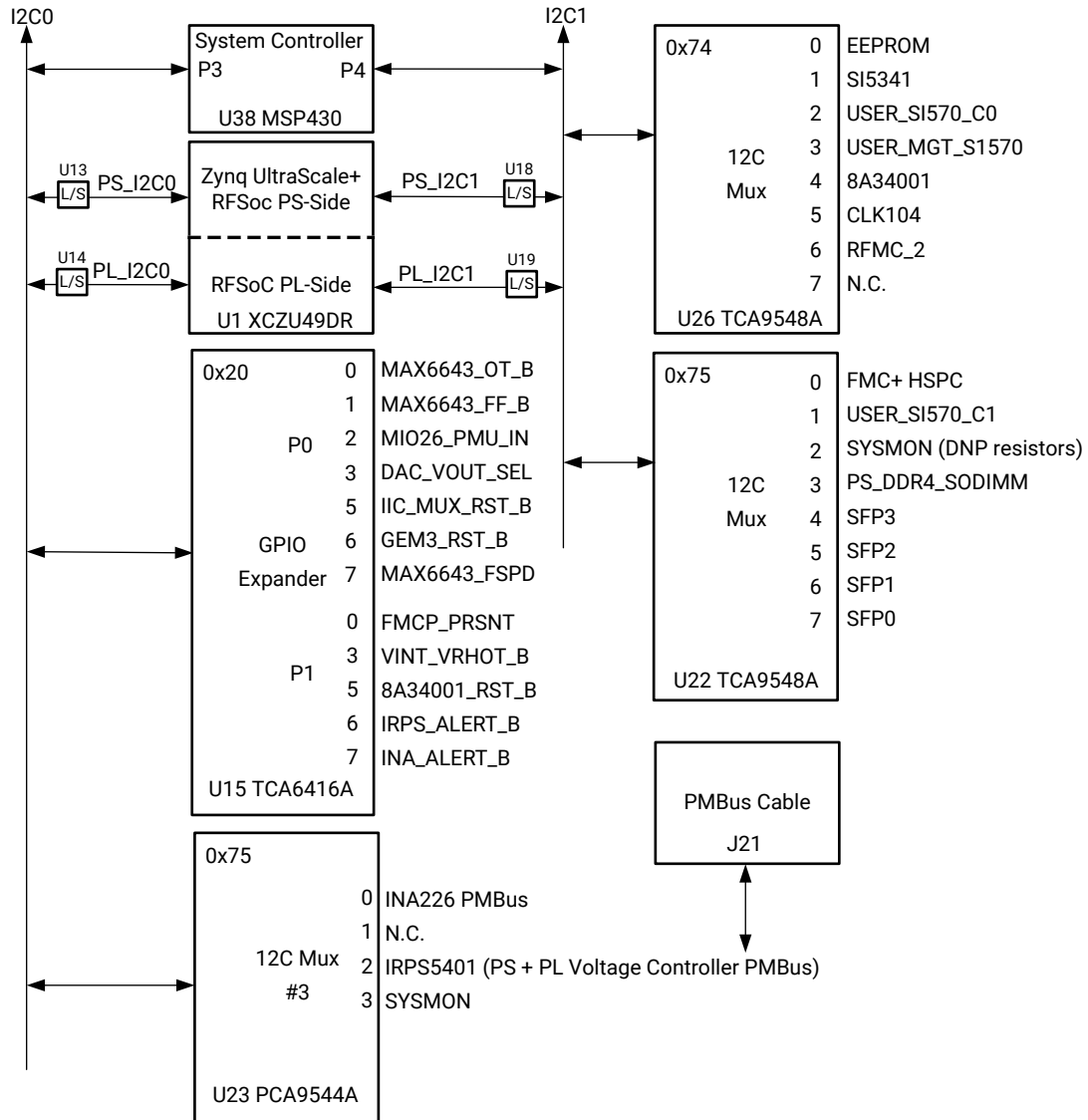
| ZU49DR U1 Pin | Net Name       | MSP430 U38 |            |
|---------------|----------------|------------|------------|
|               |                | Pin Name   | Pin Number |
| G32           | MIO38_PS_GPIO1 | P1_6       | 19         |
| AU26          | MIO13_PS_GPIO2 | P1_7       | 20         |

## I2C Bus Topology Overview

### *I2C0 (MIO 14-15), I2C1 (MIO 16-17)*

The following figure shows a high-level view of the I2C0 and I2C1 bus connectivity.

Figure 6: I2C0 and I2C1 Bus Connectivity Overview



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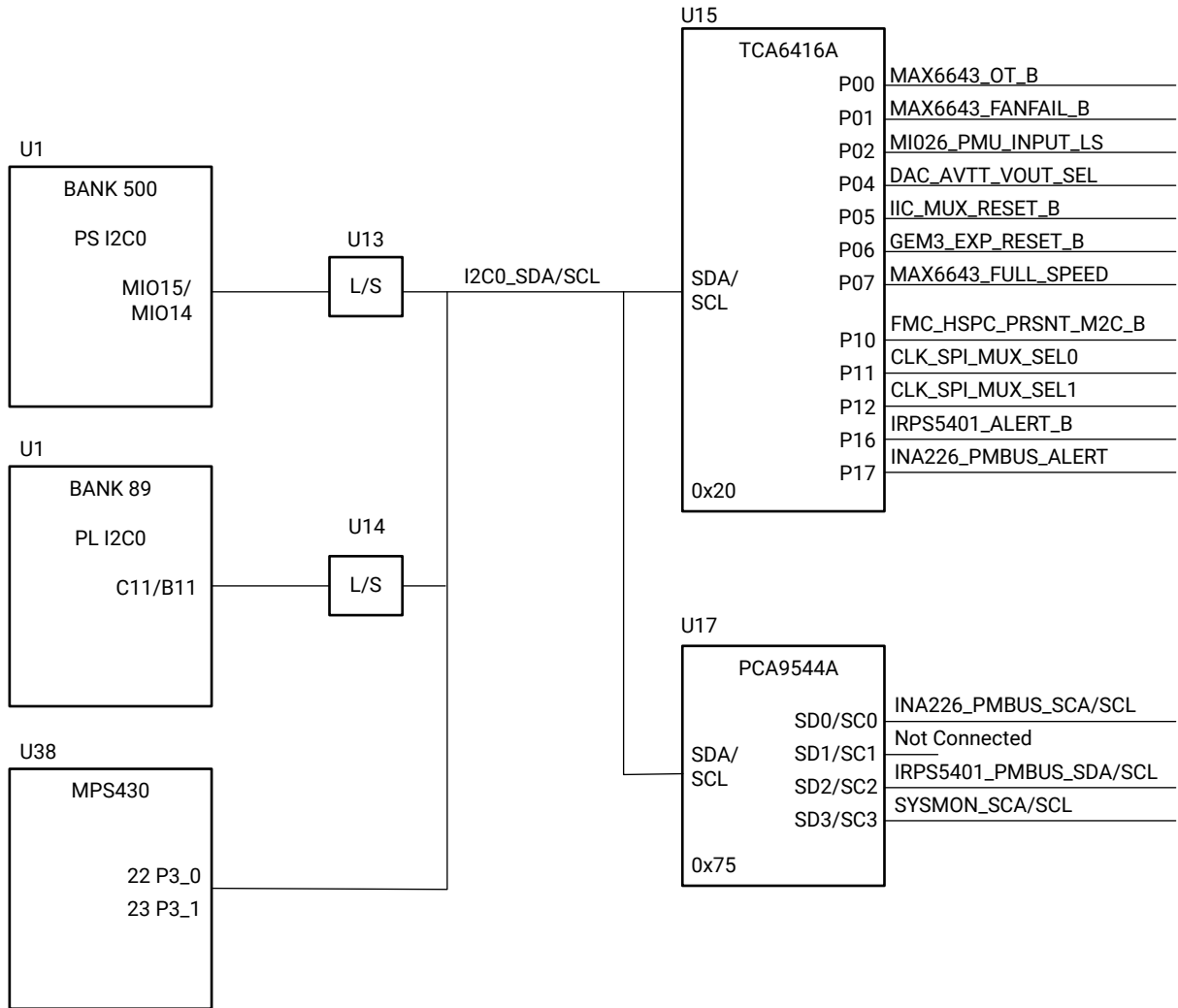
## I2C0 (MIO 14-15)

[Figure 2, callout 17]

I2C bus I2C0 connects Zynq UltraScale+ RFSoc U1 PS Bank 500, PL bank 89, and the system controller U38 to a GPIO 16-bit port expander (TCA6416A U15) and I2C switch (PCA9544A U17). The port expander enables controlling resets and power system enable pins, and accepting various alarm inputs without requiring the PL-side to be configured. The I2C0 bus also provides access to the PMBUS power controllers and INA226 power monitors through the U17 PCA9544A switch. TCA6416A U15 is pin-strapped to respond to I2C address 0x20. The PCA9544A U17 switch is set to 0x75.

The following figure shows a high-level view of the I2C0 bus connectivity.

Figure 7: I2C0 Bus Topology



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The following table identifies the devices on each port of the I2C0 U15 TCA6416A port expander.

Table 9: I2C0 Port Expander TCA6416A U15 Connections

| TCA6416A U15 |         | Schematic Net Name | Connected To   |           |                      |         |
|--------------|---------|--------------------|--|-----------|----------------------|---------|
| Pin Name     | Pin No. |                    | Pin No.  | Pin Name  | Reference Designator | Device  |
| SDA          | 23      | I2C0_SDA           | Refer to connections shown in the figure above.<br>TCA6416A U15 Addr. 0x20 |           |                      |         |
| SCL          | 22      | I2C0_SCL           |  |           |                      |         |
| P00          | 4       | MAX6643_OT_B       | 9  | OT_B      | U50                  | MAX6643 |
| P01          | 5       | MAX6643_FANFAIL_B  | 4  | FANFAIL_B | U50                  | MAX6643 |

Table 9: I2C0 Port Expander TCA6416A U15 Connections (cont'd)

| TCA6416A U15 |         | Schematic Net Name    | Connected To |               |   |               |
|--------------|---------|-----------------------|--------------|---------------|---|---------------|
| Pin Name     | Pin No. |                       | Pin No.      | Pin Name      | Reference Designator  | Device        |
| P02          | 6       | MIO26_PMU_INPUT_LS    | A34          | PS_MIO26      | U1  | XCZU49DR      |
| P04          | 8       | DAC_AVTT_VOUT_SEL     | 1            | G             | Q36   | NDS331N       |
| P05          | 9       | IIC_MUX_RESET_B       | 3            | RESET_B       | U20   | TCA9548A      |
| P06          | 10      | GEN3_EXP_RESET_B      | 2            | B             | U34   | SN74LVC1G08   |
| P07          | 11      | MAX6643_FULL_SPEED    | 6            | FULLSPD       | U50   | MAX6643       |
| P10          | 13      | FMCP_HSPC_PRSNT_M2C_B | H2           | PRSNT_M2C_L   | J28(H)  | ASP_184329_01 |
|              |         |                       | Z1           | PRSNT_M2C_L   | J28(N)  | ASP_184329_01 |
| P13          | 16      | VCCINT_VRHOT_B        | 14           | VRHOT_ICRIT # | U104  | IR35215       |
| P15          | 18      | 8A34001_EXP_RST_B     | 1            | A             | U415  | SN74LVC1G08   |
| P16          | 19      | IRPS5401_ALERT_B      | 11           | SM_ALERT#     | U104  | IR35215       |
|              |         |                       | 17           | ALERT_B       | U53, U55  | IRPS5401      |
|              |         |                       | 17           | SALERT#       | U112, U123, U127  | IR38164       |
| P17          | 20      | INA226_PMBUS_ALERT    | 3            | ALERT         | U57, U58, U59, U60, U61, U62, U63, U64, U65, U67, U71, U75, U77, U124 | INA226        |

The addresses of each target device on the I2C0 U17 PCA9544A switch are identified in the following table.

Table 10: I2C0 Multiplexer PCA9544A U17 Target Device Addresses

| PCA9544A U17 (Addr 0x75) Port | I2C0 Bus Device                     | Target Device Address              |
|-------------------------------|-------------------------------------|------------------------------------|
| 0                             | INA226_PMBus (Power Monitors)       | 0X40-0x43, 0x45-0x4E               |
| 1                             | Not Connected                       | N/A                                |
| 2                             | IRPS5401_PMBus (Voltage Regulators) | 0X40, 0x43, 0x44, 0x45, 0x4B, 0x4C |
| 3                             | SYSMON U1 bank 65                   | 0X32                               |

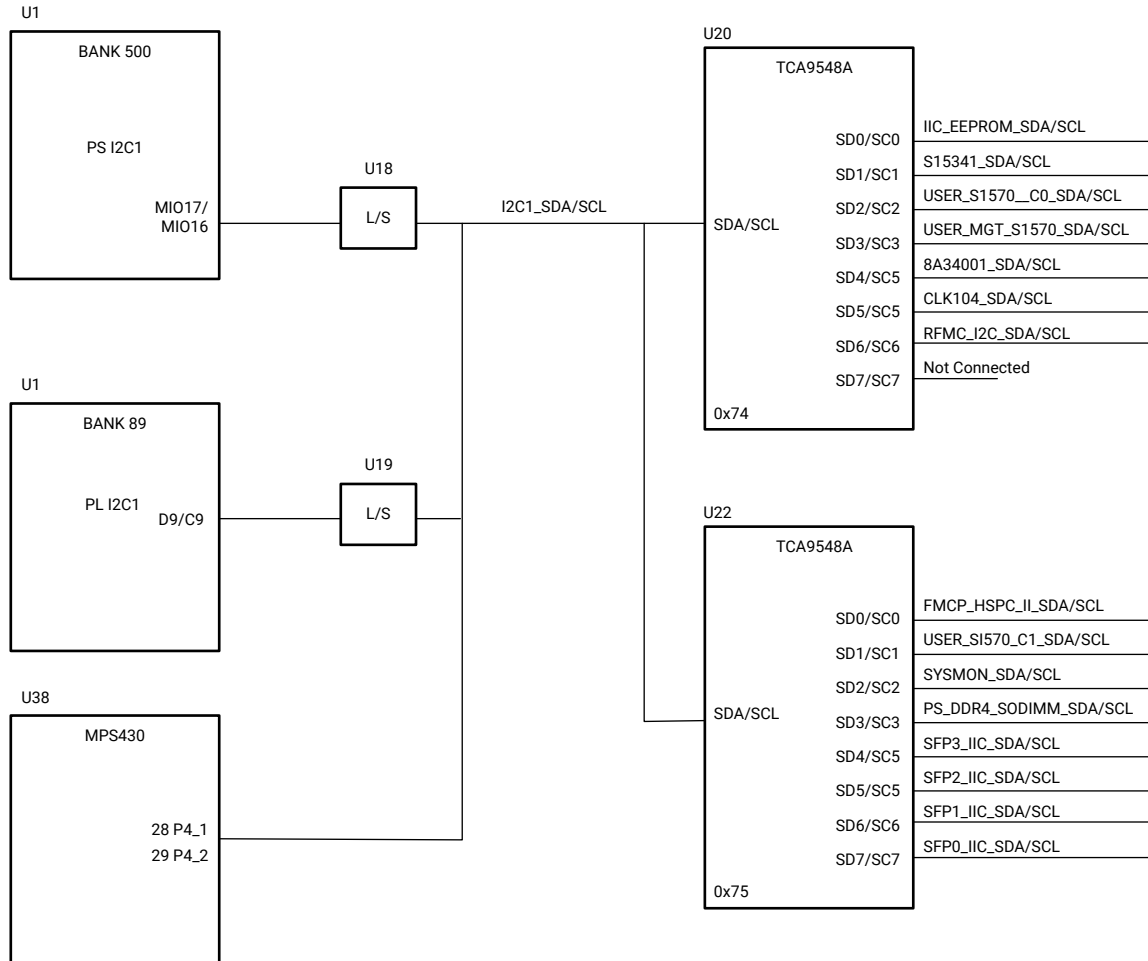
## I2C1 (MIO 16-17)

[Figure 2, callout 18]

I2C bus I2C1 connects RFSoc U1 PS Bank 500, PL bank 89, and system controller U38 to two I2C switches (TCA9548A U20 and U22). These I2C1 connections enable I2C communications with various I2C capable target devices. TCA9548A U20 is pin-strapped to respond to I2C address 0x74. TCA9548A U22 is pin-strapped to respond to I2C address 0x75.

The following figure shows a high-level view of the I2C1 bus connectivity.

Figure 8: I2C1 Bus Topology



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The addresses of each target device on the I2C1 U20 and U22 PCA9548A switches are identified in the following tables.

Table 11: I2C1 TCA9548A U20 Target Device Addresses

| TCA9548A U20 (Addr 0x74) Port | I2C1 Bus Device                  | Target Device Address |
|-------------------------------|----------------------------------|-----------------------|
| 0                             | EEPROM U16                       | 0X54                  |
| 1                             | Si5341 Clock U43                 | 0x76                  |
| 2                             | USER Si570 C0 Clock U47          | 0X5D                  |
| 3                             | USER MGT Si570 Clock U48         | 0X5D                  |
| 4                             | 8A34001 (zSFP Clk Recovery) U409 | 0x58                  |
| 5                             | CLK104 Connector J101            | 0x2F                  |
| 6                             | RFMC LPAF-50 Connector J82       | USER                  |

Table 11: I2C1 TCA9548A U20 Target Device Addresses (cont'd)

| TCA9548A U20 (Addr 0x74) Port | I2C1 Bus Device | Target Device Address |
|-------------------------------|-----------------|-----------------------|
| 7                             | No Connection   | NA                    |

Table 12: I2C1 TCA9548A U22 Target Device Addresses

| TCA9548A U22 (Addr 0x75) Port | I2C1 Bus Device          | Target Device Address |
|-------------------------------|--------------------------|-----------------------|
| 0                             | FMCP HSPC J28            | 0x##                  |
| 1                             | USER Si570 C1 Clock U130 | 0X5D                  |
| 2                             | SYSMON U1 BANK 65        | 0x32                  |
| 3                             | PS DDR4 SODIMM SKT. J48  | 0x51                  |
| 4                             | SFP3 P3                  | 0x50                  |
| 5                             | SFP2 P2                  | 0x50                  |
| 6                             | SFP1 P1                  | 0x50                  |
| 7                             | SFP0 P0                  | 0x50                  |

For more information on the TCA9548A, TCA6416A, and PCA9544A, see the [Texas Instruments website](#).

The detailed Zynq UltraScale+ RFSoc connections for the feature described in this section are documented in the ZCU216 board XDC file, referenced in [Appendix B: Xilinx Design Constraints](#).

## UART0 (MIO 18-19)

[Figure 2, callout 8]

This is the primary Zynq UltraScale+ RFSoc PS-side UART interface and is connected to the FTDI U29 FT4232HL USB-to-Quad-UART Bridge port B through TXS0108E level-shifter U32.

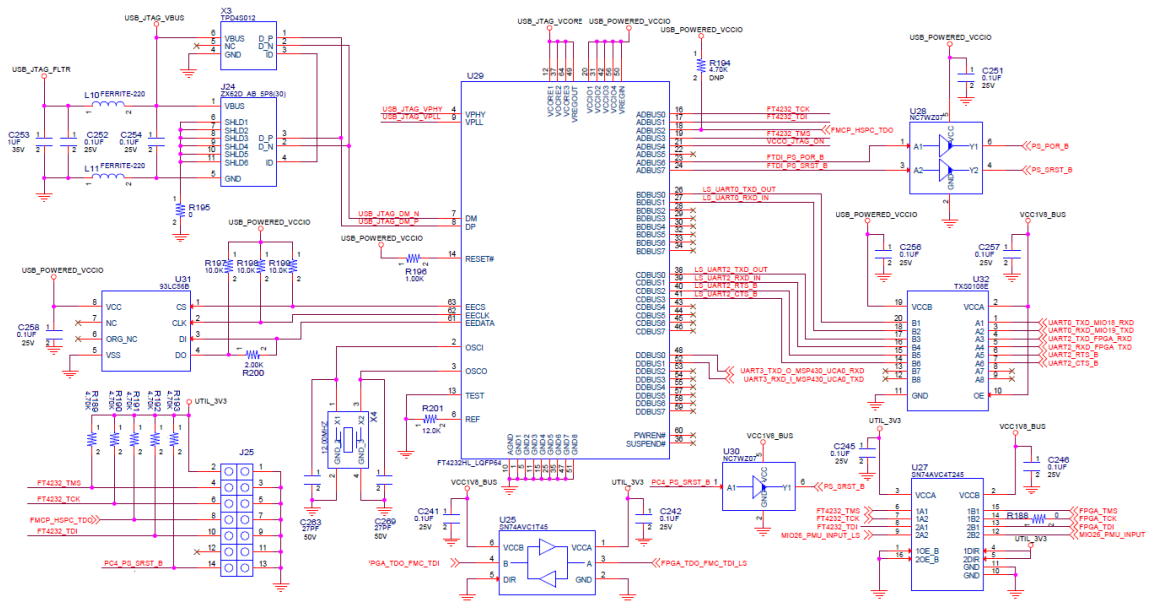
The FT4232HL U29 port assignments are listed in the following table.

Table 13: FT4232HL Port Assignments

| FT4232HL U29 | Zynq UltraScale+ RFSoc U1  |
|--------------|----------------------------|
| Port A JTAG  | ZCU216 JTAG Chain          |
| Port B UART0 | PS_UART0 (MIO 18-19)       |
| Port C UART2 | PL_UART2 Bank 89           |
| Port D UART3 | U38 System Controller UART |

The FT4232HL interface circuit connectivity is shown in the following figure.

Figure 9: ZCU216 FT4232HL Connectivity



For more information on the FT4232HL, see the [Future Technology Devices International Ltd.](https://www.future-technology.com/) website.

The detailed RFSoc connections for the feature described in this section are documented in the ZCU216 board XDC file, referenced in [Appendix B: Xilinx Design Constraints](#).

## GPIO (MIO 22-23)

PS-side pushbutton SW1 is connected to MIO22 (pin U1.AL27). PS-side LED DS1, physically placed adjacent to the pushbutton, is connected to MIO23 (pin U1.AM27).

## PMU GPI (MIO 26)

PS-side MIO 26 is reserved as an input to the PMU for indicating a warm boot. PS bank 501 MIO26 (U1.A34) is connected to the I2C0 U15 TCA6416A bus expander (port P02 U15.6) through level-shifter U27. Refer to the *Zynq UltraScale+ Device Technical Reference Manual (UG1085)* for details about the PMU interface.

## PMU GPO (MIO 32-37)

The platform management unit (PMU) within the Zynq UltraScale+ RFSoc signals power domain changes using the PMU output pins for deep-sleep mode. The Zynq UltraScale+ RFSoc PMU GPO pins are connected to inputs of the MSP430 system controller through the TXS0108E level-shifter U37. The RFSoc U1 Bank 501 and MSP430 U38 pin numbers are listed in the following table.



Table 14: XCZU49DR to MSP430 Connections

| XCZU49DR (U1) Pin | Net Name       | MSP430 U38 |            |
|-------------------|----------------|------------|------------|
|                   |                | Pin Name   | Pin Number |
| E32               | MIO37_PMU_GPO5 | P1_0       | 13         |
| E31               | MIO36_PMU_GPO4 | P1_1       | 14         |
| C33               | MIO35_PMU_GPO3 | P1_2       | 15         |
| D31               | MIO34_PMU_GPO2 | P1_3       | 16         |
| D32               | MIO33_PMU_GPO1 | P1_4       | 17         |
| D34               | MIO32_PMU_GPO0 | P1_5       | 18         |

Through the I2C0 bus U1 PS-side MIO[14:15] pins, the PMU has access to the board power controller PMBus bus (IRPS5401\_SDA/SCL) and power monitor PMBus (INA226\_PMBUS\_SDA/SCL). See [Figure 7](#) for additional details.

Refer the *Zynq UltraScale+ Device Technical Reference Manual (UG1085)* for details about the PMU interface.

The detailed RFSoc connections for the feature described in this section are documented in the ZCU216 board XDC file, referenced in [Appendix B: Xilinx Design Constraints](#).

## SDIO (MIO 39-51)

A PS-side interface to an SD card connector is provided for booting and file system storage. This interface is used for the SD boot mode and supports SD3.0 access post boot.

## SD Card Interface

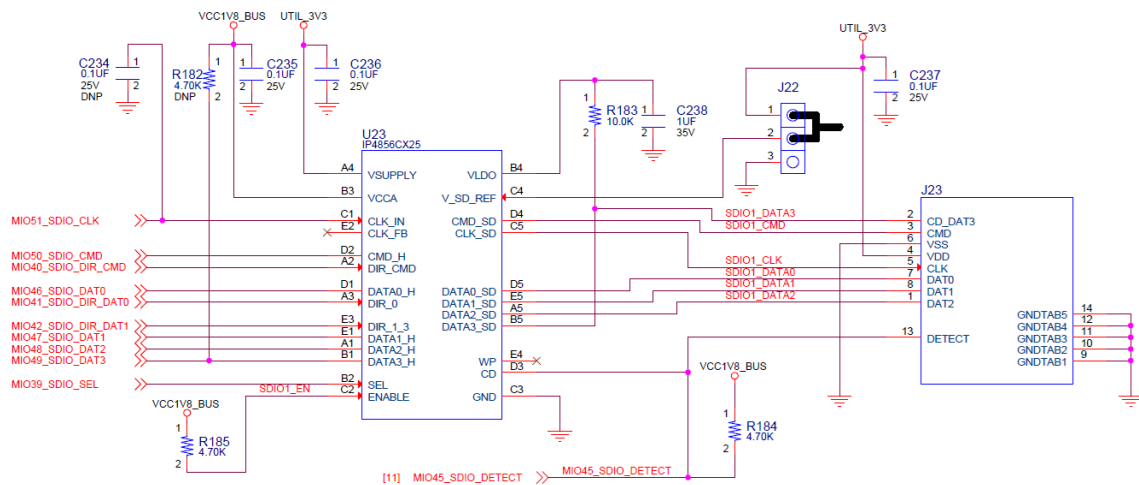
[[Figure 2](#), callout 7]

The ZCU216 board includes a secure digital input/output (SDIO) interface to provide access to general purpose non-volatile SDIO memory cards and peripherals. Information for the SD I/O card specification can be found on the [SanDisk Corporation](#) or [SD Association](#) websites. The ZCU216 SD card interface supports the SD1\_LS configuration boot mode documented in the *Zynq UltraScale+ Device Technical Reference Manual (UG1085)*.

The SDIO signals are connected to ZU49DR RFSoc PS bank 501 which has its VCCMIO set to 1.8V. The six SD interface nets MIO[46:49]\_SDIO\_DAT[0:3], MIO50\_SDIO\_CMD, and MIO51\_SDIO\_CLK each have a series 30Ω resistor at the Bank 501 source. An NXP IP4856CX25 SD 3.0-compliant voltage level-translator U23 is present between the ZU49DR RFSoc and the SD card connector (J23). The NXP IP4856CX25 U23 device provides SD3.0 capability with SDR104 performance.

The following figure shows the connections of the SD card interface on the ZCU216 board.

Figure 10: SD Card Interface



The NXP SD3.0 level shifter is mounted on an Aries adapter board that has the pin mapping shown in the following table.

Table 15: IP4856CX25 U23 Adapter Pinout

| Aries Adapter Pin Number | IP4856CX25 U23 Pin Number | IP4856CX25 U23 Pin Name |
|--------------------------|---------------------------|-------------------------|
| 1                        | C1                        | CLK_IN                  |
| 2                        | C3                        | GND                     |
| 3                        | D3                        | CD                      |
| 4                        | D2                        | CMD_H                   |
| 5                        | E2                        | CLK_FB                  |
| 6                        | E4                        | WP                      |
| 7                        | B4                        | VLDO                    |
| 8                        | C4                        | VSD_REF                 |
| 9                        | A3                        | DIR_0                   |
| 10                       | A4                        | VSUPPLY                 |
| 11                       | B3                        | VCCA                    |
| 12                       | A2                        | DIR_CMD                 |
| 13                       | D1                        | DATA0_H                 |
| 14                       | B2                        | SEL                     |
| 15                       | B1                        | DATA3_H                 |
| 16                       | E1                        | DATA1_H                 |
| 17                       | E3                        | DIR_1_3                 |
| 18                       | A1                        | DATA2_H                 |
| 19                       | E5                        | DATA1_SD                |
| 20                       | D5                        | DATA0_SD                |
| 21                       | C5                        | CLK_SD                  |

Table 15: IP4856CX25 U23 Adapter Pinout (cont'd)

| Aires Adapter Pin Number | IP4856CX25 U23 Pin Number | IP4856CX25 U23 Pin Name |
|--------------------------|---------------------------|-------------------------|
| 22                       | D4                        | CMD_SD                  |
| 23                       | B5                        | DATA3_SD                |
| 24                       | A5                        | DATA2_SD                |
| 25                       | C2                        | ENABLE                  |

For more information on the IP4856CX25, see the [NXP](#) website.

The detailed RFSoc connections for the feature described in this section are documented in the ZCU216 board XDC file, referenced in [Appendix B: Xilinx Design Constraints](#).

## USB0 (MIO 52-63) USB 3.0 Transceiver and USB 2.0 ULPI PHY

The USB interface on the PS-side serves multiple roles as a host or device controller. The USB 3.0 interface (host mode only) is supported by the RFSoc GTR interface while the USB 2.0 (host and device modes) capabilities of the SMSC USB3320C controller are shared on a common USB 3.0 micro USB type A connector (J18).

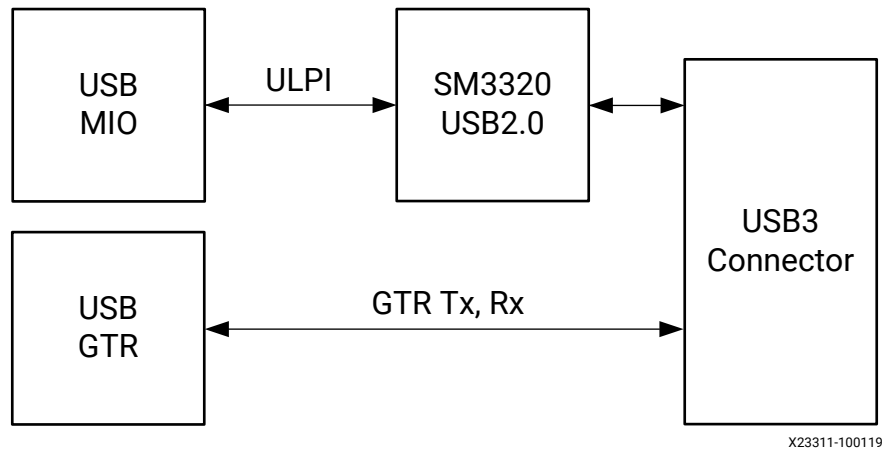
### USB 3.0 Transceiver and USB 2.0 ULPI PHY

[[Figure 2](#), callout 6]

The ZCU216 board uses a Standard Microsystems Corporation USB3320 USB 2.0 ULPI Transceiver (U6) to support a USB connection to the host computer. A USB cable is supplied in the ZCU216 Evaluation Kit (standard-A connector to host computer, USB 3.0 A connector to ZCU216 board connector J18). The USB3320 is a high-speed USB 2.0 PHY supporting the UTMI + low pin interface (ULPI) interface standard. The ULPI standard defines the interface between the USB controller IP and the PHY device which drives the physical USB bus. Use of the ULPI standard reduces the interface pin count between the USB controller IP and the PHY device.

The following figure shows the USB 3.0 interface. USB 3.0 is host mode only.

Figure 11: USB Interface



The USB3320 is clocked by a 24 MHz crystal (X2). See the [Standard Microsystems Corporation USB3320 data sheet](#) for clocking mode details.

The interface to the USB3320 PHY is implemented through the IP in the ZU49DR RFSoc Processor System (PS). USB OTG support is available for USB 2.0. Refer to [Table 3](#) for USB 2.0 jumper settings.

**Note:** The shield for the USB 3.0 micro-B connector (J18) can be tied to GND by a jumper on header J20 pins 2-3 (default). The USB shield can optionally be connected through a series capacitor to GND by installing a capacitor (body size 0402) at location C204 and jumping pins 1-2 on header J20.

The USB3320 ULPI U6 transceiver circuit (see the following figure) has a Micrel MIC2544 high-side programmable current limit switch (U7). This switch has an open-drain output fault flag on pin 2, which will turn on LED DS7 if overcurrent or thermal shutdown conditions are detected. DS7 is located adjacent to the USB J18 connector ([Figure 2](#), callout 6).

The following figure shows the ULPI U6 transceiver circuit.



## 10/100/1000 MHz Tri-Speed Ethernet PHY

[Figure 2, callout 16]

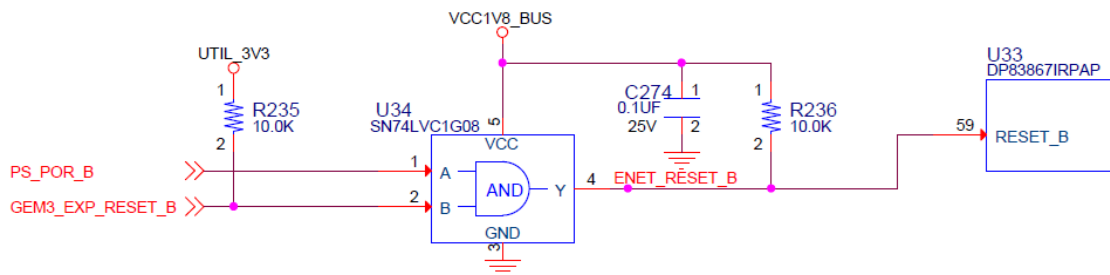
The ZCU216 board uses the TI DP83867IRPAP Ethernet RGMII PHY (U33) (see [Texas Instruments](#) website) for Ethernet communications at 10 Mb/s, 100 Mb/s, or 1000 Mb/s. The board supports RGMII mode only. The PHY connection to a user-provided Ethernet cable is through a Würth 7499111221A RJ-45 connector (P1) with built-in magnetics.

### Ethernet PHY Reset

The DP83867IRPAP PHY U33 reset circuit is shown in the following figure. The DP83867IRPAP can be reset by the GEN3\_EXP\_RESET\_B signal through the I2C0 TCA6416A U15 bus expander P06 pin 10 or the PS\_POR\_B signal generated by the MAX16025 U6 POR device pin 11.

SW4 pushbutton at the MAX16025 U5 pin 6 input also triggers a PS\_POR\_B signal.

Figure 14: Ethernet PHY Reset Circuit



### Ethernet PHY LED Interface

[Figure 2, callout 16]

The DP83867IRPAP PHY U33 LED interface (LED\_0, LED\_2) uses the two LEDs embedded in the P1 RJ45 connector bezel. The LED functional description is as shown in the following table.

Table 16: Ethernet PHY LED Functional Description

| Pin   |        | Type       | Description   |
|-------|--------|------------|---|
| Name  | Number |            |   |
| LED_2 | 61     | S, I/O, PD | By default, this pin indicates receive or transmit activity. Additional functionality is configurable by means of LEDCR1[11:8] register bits.<br><b>Note:</b> This pin is a strap configuration pin for RGZ devices only. |
| LED_1 | 62     | S, I/O, PD | By default, this pin indicates that 100BASE-T link is established. Additional functionality is configurable by means of LEDCR1[7:4] register bits.  |

Table 16: Ethernet PHY LED Functional Description (cont'd)

| Pin   |        | Type       | Description  |
|-------|--------|------------|--|
| Name  | Number |            |  |
| LED_0 | 63     | S, I/O, PD | By default, this pin indicates that link is established. Additional functionality is configurable by means of LEDCR1[3:0] register bits. |

The LED functions can be re-purposed with a LEDCR1 register write available through the PHYs management data interface, MDIO/MDC. LED\_2 is assigned to ACT (activity indicator) and LED\_0 indicates link established.

LED\_1 (100BASE-T link established) is a separate LED DS8 located on the top side of the board near the RJ45 P1 connector (Figure 2, callout 16).

For more Ethernet PHY details, see the TI DS83867 data sheet on the [Texas Instruments](#) website.

The detailed RFSoc connections for the feature described in this section are documented in the ZCU216 board XDC file, referenced in [Appendix B: Xilinx Design Constraints](#).

## Programmable Logic JTAG Programming Options

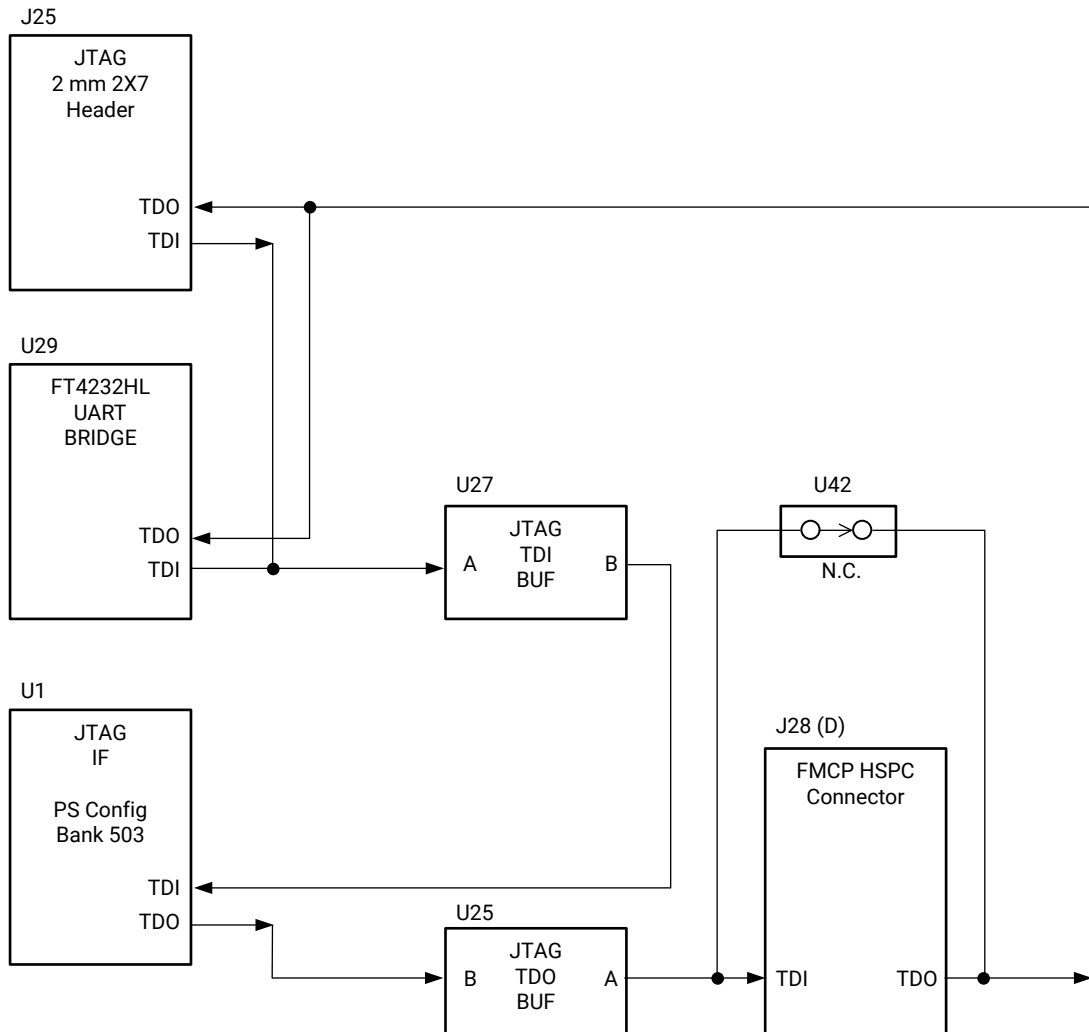
[Figure 2, callouts 8 and 9]

ZCU216 JTAG chain:

- J24 USB micro AB connector connected to U29 FT4232HL USB-JTAG bridge
- J25 2x7 2 mm shrouded, keyed JTAG pod flat cable connector

The ZCU216 board JTAG chain is shown in the following figure.

Figure 15: JTAG Chain Block Diagram



X23321-100119

## Clock Generation

The ZCU216 board provides fixed and variable clock sources for the ZU49DR Zynq UltraScale+ RFSoc. The following table lists the source devices for each clock.



Table 17: ZCU216 Board Clock Sources

| Clock (Net) Name                     | Frequency            | Clock Source                       |
|--------------------------------------|----------------------|------------------------------------|
| <b>Fixed Frequency Clocks</b>        |                      |                                    |
| PS_REF_CLK                           | 33.33 MHz            | U43 SI5341B Clock Generator (0x76) |
| CLK_100                              | 100 MHz              |                                    |
| CLK_125                              | 125 MHz              |                                    |
| GTR_REF_CLK_SATA                     | 125 MHz              |                                    |
| GTR_REF_CLK_USB3                     | 26 MHz               |                                    |
| <b>Programmable Frequency Clocks</b> |                      |                                    |
| USER_SI570_C0                        | 300 MHz (Default)    | U47 SI570 I2C PROG. OSC. (0x5D)    |
| USER_SI570_C1                        | 300 MHz (Default)    | U130 SI570 I2C PROG. OSC. (0x5D)   |
| USER_MGT_SI570_CLOCK                 | 156.25 MHz (Default) | U48 SI570 I2C PROG. OSC. (0x5D)    |
| USER_SMA_MGT_CLOCK                   | User-Provided Source | J6 (P)/J7 (N) SMA CONN.            |
| Various 8A34001 eCPRI Clocks         | Various              | U409 8A34001 (0x58)                |

The following table lists the connections for each clock.

Table 18: Clock Connections to ZU49DR U1

| Clock Source Ref. Des. and Pin                                       | Net Name                 | I/O Standard | ZU49DR (U1) Pin |
|--|--------------------------|--------------|-----------------|
| <b>U43 SI5341B Clock Generator</b>                                   |                          |              |                 |
| U43.59   | PS_REF_CLK (series R300) | 1            | U32             |
| U43.45   | CLK_125_P                | LVDS         | A13             |
| U43.44   | CLK_125_N                | LVDS         | A12             |
| U43.42   | CLK_100_P                | LVDS         | G12             |
| U43.41   | CLK_100_N                | LVDS         | G11             |
| U43.35   | GTR_REF_CLK_SATA_P       | 2            | AB34            |
| U43.34   | GTR_REF_CLK_SATA_N       | 2            | AB35            |
| U43.31   | GTR_REF_CLK_USB3_P       | 2            | AC36            |
| U43.30   | GTR_REF_CLK_USB3_N       | 2            | AC37            |
| <b>U47 SI570 I2C Prog. Oscillator DDR4 C0 I/F (300 MHz default)</b>  |                          |              |                 |
| U47.4  | USER_SI570_C0_P          | LVDS         | AR20            |
| U47.5  | USER_SI570_C0_N          | LVDS         | AR19            |
| <b>U130 SI570 I2C Prog. Oscillator DDR4 C1 I/F (300 MHz default)</b> |                          |              |                 |
| U130.4   | USER_SI570_C1_P          | LVDS         | G17             |
| U130.5   | USER_SI570_C1_N          | LVDS         | F17             |
| <b>U49 SI570 I2C Prog. Oscillator (156.250 MHz default)</b>          |                          |              |                 |
| U48.4  | USER_MGT_SI570_CLOCK_P   | 2            | H34             |
| U48.5  | USER_MGT_SI570_CLOCK_N   | 2            | H35             |
| <b>J79 (P)/J80 (N) SMA Connectors</b>                                |                          |              |                 |
| J6   | USER_SMA_MGT_CLOCK_P     | 2            | M34             |

Table 18: Clock Connections to ZU49DR U1 (cont'd)

| Clock Source Ref. Des. and Pin  | Net Name             | I/O Standard | ZU49DR (U1) Pin |
|---------------------------------|----------------------|--------------|-----------------|
| J7                              | USER_SMA_MGT_CLOCK_N | 2            | M35             |
| <b>U409 8A34001 eCPRI Clock</b> |                      |              |                 |
| U409.A9 (Q1)                    | 8A34001_Q1_OUT_P     | 2            | Y39             |
| U409.B9 (Q1)                    | 8A34001_Q1_OUT_N     | 2            | Y40             |
| U409.A11 (Q2)                   | 8A34001_Q2_OUT_P     | LVDS         | AT23            |
| U409.B11 (Q2)                   | 8A34001_Q2_OUT_N     | LVDS         | AT24            |
| U409.A12 (Q3)                   | 8A34001_Q3_OUT_P     | LVDS         | H30             |
| U409.B12 (Q3)                   | 8A34001_Q3_OUT_N     | LVDS         | G30             |
| U409.M8 (Q7)                    | 8A34001_Q7_OUT_P     | 2            | T34             |
| U409.L8 (Q7)                    | 8A34001_Q7_OUT_N     | 2            | T35             |
| U409.A6 (Q8)                    | 8A34001_Q8_OUT_P     | LVDS         | J21             |
| U409.B6 (Q8)                    | 8A34001_Q8_OUT_N     | LVDS         | H21             |
| U409.M6 (Q11)                   | 8A34001_Q11_OUT_P    | 2            | Y34             |
| U409.L6 (Q11)                   | 8A34001_Q11_OUT_N    | 2            | Y35             |

**Notes:**

1. U1 ZU49DR Bank 503 supports LVCMOS18 level inputs.
2. Series capacitor coupled, U1 MGT (I/O standards do not apply).
3. Series capacitor coupled.

## SI5341B 10 Independent Output Any-Frequency Clock Generator U43

[Figure 2, callout 10]

- Clock generator: Silicon Labs SI5341B-D07833-GM
- Jitter: <100 fs RMS typical
- Differential and single-ended outputs

The SI5341B data sheet addendum for the Silicon Labs SI5341B-D07833-GM documents the pre-programmed output frequencies:

- Inputs:
  - XAXB: 48 MHz
  - Crystal Mode
  - IN0: Unused
  - IN1: Unused
  - IN2: Unused
  - FB\_IN: Unused

- Outputs:
  - OUT0: 27 MHz
  - Enabled, LVDS 3.3 V
  - OUT1: Unused
  - OUT2: 26 MHz
  - Enabled, LVDS 3.3 V
  - OUT3: 125 MHz
  - Enabled, LVDS 3.3 V
  - OUT4: 100 MHz
  - Enabled, HCSL 3.3 V
  - OUT5: 100 MHz
  - Enabled, LVDS 3.3 V
  - OUT6: 125 MHz
  - Enabled, LVDS 3.3 V
  - OUT7: 74.25 MHz [ 74 + 1/4 MHz ]
  - Enabled, LVDS 3.3 V
  - OUT8: Unused
  - OUT9: 33.33333333333333... MHz [ 33 + 1/3 MHz ]
  - Enabled, LVCMOS In-Phase 1.8V

### ***Programmable User SI570 Clocks***

[Figure 2, callouts 11 and 12]

The ZCU216 board has three I2C programmable SI570 low-jitter 3.3V LVDS differential oscillators, two assigned to the DDR4 component memory interface banks (Bank 65 I/F C0: U47 and Bank 69 I/F C1: U130) and one assigned to GTY131 (U48).

On power-up the user clocks default to a pre-programmed output frequency: DDR4 I/F U47 and U130 to 300.000 MHz and GTY I/F U48 to 156.250 MHz.

User applications can change the output frequency of each SI570 within the range of 10 MHz to 810 MHz through the I2C1 bus interface. Power cycling the ZCU216 board reverts user clocks to their default settings.

These oscillators can also be reprogrammed from MSP430 system controller U38 (see TI MSP430 System Controller on the [Texas Instruments](#) website for more system controller information and the ZCU216 web page for the *ZCU216 System Controller GUI Tutorial (XTP\_TBD)*).

DDR4 Memory Interface C0 (U47) and C1 (U130) SI570:

- Programmable oscillator: Silicon Labs Si570BAB001614DG (10 MHz-810 MHz, 300 MHz default)
- I2C 0x5D
- LVDS differential output
- Total Stability: 61.5 ppm

GTY SI570:

- Programmable oscillator: Silicon Labs Si570BAB000544DG (10 MHz-810 MHz, 156.250 MHz default)
- I2C 0x5D
- LVDS differential output
- Total stability: 61.5 ppm

The SI5341B and SI570 data sheets can be found on the [Silicon Labs](#) website.

## User SMA MGT Clock

[[Figure 2](#), callout 34]

The ZCU216 board provides a pair of SMAs (J6, J7) for differential AC coupled user MGT clock input into Zynq UltraScale+ RFSoc U1 GTY Bank 130. This differential signal pair is series-capacitor coupled. The P-side SMA J6 signal USER\_SMA\_MGT\_CLOCK\_P is connected to U1 MGTREFCLK1P pin M34, and the N-side SMA J7 signal USER\_SMA\_MGT\_CLOCK\_N is connected to U1 MGTREFCLK1N pin M35. The user SMA MGT clock differential signal amplitude must not exceed -0.5V (Min) to 1.30V (Max).

The detailed RFSoc connections for the feature described in this section are documented in the ZCU216 board XDC file, referenced in [Appendix B: Xilinx Design Constraints](#).

## zSFP/zSFP+ Module Connectors

[[Figure 2](#), callout 15]

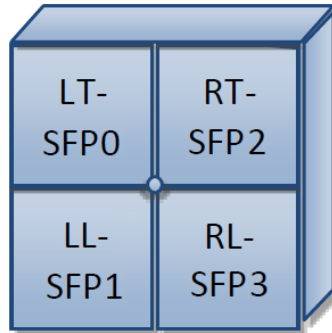
The ZCU216 board hosts a quad zSFP/zSFP+ connector (J29) that accept zSFP or zSFP+ modules. The connectors are housed within a single 2x2 zSFP cage assembly. The following figure shows the zSFP/zSFP+ module locations within J29.

Figure 16: Quad-zSFP Connector zSFP Locations

Looking at the J29 front opening:

1<sup>st</sup> character: L= Left, R= Right,

2<sup>nd</sup> character: T = Top, L= Lower



The detailed RFSoc connections for the feature described in this section are documented in the ZCU216 board XDC file, referenced in [Appendix B: Xilinx Design Constraints](#).

The following table lists the zSFP+ module control and status connections.

Table 19: zSFP Control and Status Board Connections

| zSFP Control/ Status Signal      | Board Connection               |   |
|----------------------------------|--------------------------------|---|
| <b>SFP0 J29 LT<sup>1,2</sup></b> |                                |   |
| SFP_TX_FAULT                     | Test Point TP11                | High = Fault<br>Low = Normal Operation                        |
| SFP_TX_DISABLE                   | Jumper J39<br>Switch Q6 U1.K16 | Off = SFP Disabled<br>On = SFP Enabled                        |
| SFP_MOD_DETECT                   | Test Point J12                 | High = Module not present<br>Low = Module Present             |
| SFP_RS0                          | PU R262 / PD R269              | PU R262 = Full RX bandwidth<br>PD R269 = Reduced RX bandwidth |
| SFP_RS1                          | PU R263 / PD R264              | PU R263 = Full TX bandwidth<br>PD R264 = Reduced TX bandwidth |
| SFP_LOS                          | Test Point TP13                | High = Loss of receiver signal<br>Low = Normal operation      |
| <b>SFP1 J29 LL<sup>1,2</sup></b> |                                |   |
| SFP_TX_FAULT                     | Test Point TP14                | High = Fault<br>Low = Normal Operation                        |
| SFP_TX_DISABLE                   | Jumper J44<br>Switch Q7 U1.K17 | Off = SFP Disabled<br>On = SFP Enabled                        |
| SFP_MOD_DETECT                   | Test Point TP15                | High = Module not present<br>Low = Module Present             |

Table 19: zSFP Control and Status Board Connections (cont'd)

| zSFP Control/ Status Signal      | Board Connection               |                                |
|----------------------------------|--------------------------------|--------------------------------|
| SFP_RS0                          | PU R270 / PD R273              | PU R270 = Full RX bandwidth    |
|                                  |                                | PD R273 = Reduced RX bandwidth |
| SFP_RS1                          | PU R271 / PD R274              | PU R271 = Full TX bandwidth    |
|                                  |                                | PD R274 = Reduced TX bandwidth |
| SFP_LOS                          | Test Point TP16                | High = Loss of receiver signal |
|                                  |                                | Low = Normal operation         |
| <b>SFP2 J29 RT<sup>1,2</sup></b> |                                |                                |
| SFP_TX_FAULT                     | Test Point TP5                 | High = Fault                   |
|                                  |                                | Low = Normal Operation         |
| SFP_TX_DISABLE                   | Jumper J32<br>Switch Q4 U1.K14 | Off = SFP Disabled             |
|                                  |                                | On = SFP Enabled               |
| SFP_MOD_DETECT                   | Test Point TP6                 | High = Module not present      |
|                                  |                                | Low = Module Present           |
| SFP_RS0                          | PU R279 / PD R281              | PU R279 = Full RX bandwidth    |
|                                  |                                | PD R281 = Reduced RX bandwidth |
| SFP_RS1                          | PU R280 / PD R282              | PU R280 = Full TX bandwidth    |
|                                  |                                | PD R282 = Reduced TX bandwidth |
| SFP_LOS                          | Test Point TP7                 | High = Loss of receiver signal |
|                                  |                                | Low = Normal operation         |
| <b>SFP3 J29 RL<sup>1,2</sup></b> |                                |                                |
| SFP_TX_FAULT                     | Test Point TP8                 | High = Fault                   |
|                                  |                                | Low = Normal Operation         |
| SFP_TX_DISABLE                   | Jumper J35<br>Switch Q5 U1.K15 | Off = SFP Disabled             |
|                                  |                                | On = SFP Enabled               |
| SFP_MOD_DETECT                   | Test Point TP9                 | High = Module not present      |
|                                  |                                | Low = Module Present           |
| SFP_RS0                          | PU R284 / PD R290              | PU R284 = Full RX bandwidth    |
|                                  |                                | PD R290 = Reduced RX bandwidth |
| SFP_RS1                          | PU R285 / PD R291              | PU R285 = Full TX bandwidth    |
|                                  |                                | PD R291 = Reduced TX bandwidth |
| SFP_LOS                          | Test Point TP10                | High = Loss of receiver signal |
|                                  |                                | Low = Normal operation         |

**Notes:**

1. The RS0/RS1 PU/PD resistors are not populated. There are pull-down resistors built into the zSFP modules that select the lower bandwidth mode of the module.
2. BW selection is also available through I2C control.

For additional information about the zSFP module, see SFF-8402 and SFF-8432 on the [SNIA Technology Affiliates](#) website.

## User PMOD GPIO Headers

[Figure 2, callout 22]

The ZCU216 evaluation board supports two right-angle PMOD GPIO receptacles J46 and J47. The 3.3V PMOD nets are level-shifted and are wired to the ZU49DR device U1 bank 88.

For more information on the pmod interface, visit the [Digilent](#) website.

The detailed RFSoc connections for the feature described in this section are documented in the ZCU216 board XDC file, referenced in [Appendix B: Xilinx Design Constraints](#).

## User I/O

[Figure 2, callout 23, 24, and 25]

The ZCU216 board provides these user and general purpose I/O capabilities:

- Eight sets of 3 RGB LEDs (24 LEDs total) (callout 23)
  - RGB\_[R,G,B]\_LED\_0: DS46
  - RGB\_[R,G,B]\_LED\_1: DS47
  - RGB\_[R,G,B]\_LED\_2: DS48
  - RGB\_[R,G,B]\_LED\_3: DS49
  - RGB\_[R,G,B]\_LED\_4: DS50
  - RGB\_[R,G,B]\_LED\_5: DS51
  - RGB\_[R,G,B]\_LED\_6: DS52
  - RGB\_[R,G,B]\_LED\_7: DS53
- 8-position user DIP switch (callout 23)
  - GPIO\_DIP\_SW[7:0]: SW14
- Five user pushbuttons and a CPU reset PB switch (callouts 24 and 25)
  - GPIO\_SW\_[NWCES]: SW8, SW9, SW10, SW11, SW12
  - CPU\_RESET: SW13

The detailed RFSoc connections for the feature described in this section are documented in the ZCU216 board XDC file, referenced in [Appendix B: Xilinx Design Constraints](#).

## Power and Status LEDs

[Figure 2, area of callouts 17 and 18]

The following table defines the power and status LEDs. For user controlled GPIO LED details, see [User I/O](#).

Table 20: Power and Status LEDs

| Ref. Des. | Schematic Net Name   | LED Color  | Description  |
|-----------|----------------------|------------|--|
| DS1       | MIO23_LED            | Green      | RFSoc U1 Bank 500 GPIO LED   |
| DS2       | PS_INIT_B            | Green/ Red | Green: FPGA initialization was successful<br>Red: FPGA initialization is in progress   |
| DS3       | PS_DONE              | Green      | RFSoc U1 bit file download is complete   |
| DS4       | PS_RESET_B           | Red        | POR U5 asserts RESET_B low when any of the monitored voltages (IN_) falls below its respective threshold, any EN_ goes low, or MR is asserted. |
| DS5       | PS_ERR_OUT           | Red        | PS error out is asserted for accidental loss of power, an error in the PMU that holds the CSU in reset, or an exception in the PMU.            |
| DS6       | PS_ERR_STATUS        | Red        | PS error status indicates a secure lockdown state. Alternatively, it can be used by the PMU firmware to indicate system status.                |
| DS7       | USB3 MIC2544 U7 FLG  | Green      | PS USB 3.0 ULPI VBUS Power Error   |
| P1-R      | ENET_LED_0           | Green      | EPHY U33 link established (all speeds) (RJ45 bezel right)  |
| DS8       | ENET_LED_1           | Green      | EPHY U33 1000BASE-T link established   |
| P1-L      | ENET_LED_2           | Green      | EPHY U33 link activity (RJ45 bezel left)   |
| DS9       | MSP430_LED0          | Blue       | MSP430 U38 GPIO LED  |
| DS10      | MSP430_LED1          | Green      | MSP430 U38 GPIO LED  |
| DS19      | VCC12_SW             | Green      | 12VDC Power ON   |
| DS20      | VCCINT_PG            | Green      | VCCINT 0.85VDC Power ON  |
| DS21      | VCCINT_IO_BRAM_PS_PG | Green      | VCCPSINTFP/LP/BRAM/IO 0.85VDC Power ON   |
| DS22      | VCC1V8_PG            | Green      | VCC1V8 1.8VDC Power ON   |
| DS23      | VCC1V2_PG            | Green      | VCC1V2 1.2VDC Power ON   |
| DS24      | VADJ_FMC_PG          | Green      | VADJ_FMC 1.8VDC (Nom.) Power ON  |
| DS25      | MGTAVCC_PG           | Green      | MGTAVCC 0.9VDC Power ON  |
| DS26      | DAC_AVCC_PG          | Green      | ADC_AVCC 0.925V Power ON   |
| DS27      | MGT1V2_PG            | Green      | MGT1V2 1.2VDC Power ON   |
| DS29      | MGTRAVCC_PG          | Green      | MGTRAVCC 0.85VDC Power ON  |
| DS30      | MGT1V8_PG            | Green      | MGT1V8 1.8VDC Power ON   |
| DS31      | VCCINT_AMS_PG        | Green      | VCCINT_AMS 0.85VDC Power ON  |
| DS32      | ADC_AVCC_PG          | Green      | ADC_AVCC 0.925VDC Power ON   |
| DS34      | ADC_AVCCAUX_PG       | Green      | ADC_AVCCAUX 1.8VDC Power ON  |
| DS36      | DAC_AVTT_PG          | Green      | DAC_AVTT 2.5VDC Power ON   |
| DS37      | UTIL_1V13_PG         | Green      | UTIL_1V13 1.13VDC Power ON   |

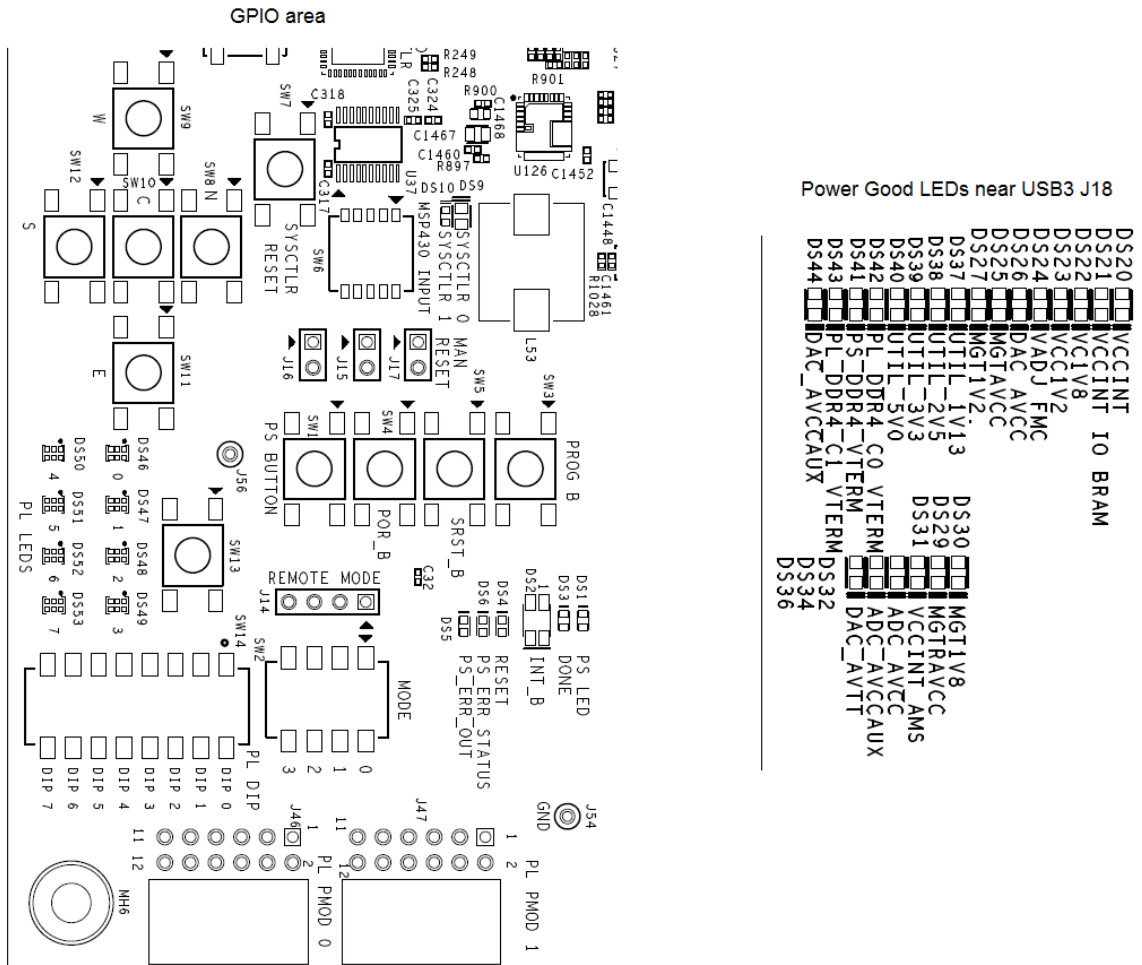


Table 20: Power and Status LEDs (cont'd)

| Ref. Des. | Schematic Net Name       | LED Color | Description                      |
|-----------|--------------------------|-----------|----------------------------------|
| DS38      | UTIL_2V5_PG              | Green     | UTIL_2V5 2.5VDC Power ON         |
| DS39      | UTIL_3V3_PG              | Green     | UTIL_3V3 3.3VDC Power ON         |
| DS40      | UTIL_5V0_PG              | Green     | UTIL_5V0 5VDC Power ON           |
| DS41      | PS_DDR4_VTERM_0V60_PG    | Green     | PS_DDR4_VTERM 0.6VDC Power ON    |
| DS42      | PL_C0_DDR4_VTERM_0V60_PG | Green     | PL_C0_DDR4_VTERM 0.6VDC Power ON |
| DS43      | PL_C1_DDR4_VTERM_0V60_PG | Green     | PL_C1_DDR4_VTERM 0.6VDC Power ON |
| DS44      | DAC_AVCCAUX_ON           | Green     | DAC_AVCCAUX 1.8VDC Power ON      |
| DS46      | RGB_[R,G,B]_LED_0        | R,G,B     | USER GPIO RGB LED_0              |
| DS47      | RGB_[R,G,B]_LED_1        | R,G,B     | USER GPIO RGB LED_1              |
| DS48      | RGB_[R,G,B]_LED_2        | R,G,B     | USER GPIO RGB LED_2              |
| DS49      | RGB_[R,G,B]_LED_3        | R,G,B     | USER GPIO RGB LED_3              |
| DS50      | RGB_[R,G,B]_LED_4        | R,G,B     | USER GPIO RGB LED_4              |
| DS51      | RGB_[R,G,B]_LED_5        | R,G,B     | USER GPIO RGB LED_5              |
| DS52      | RGB_[R,G,B]_LED_6        | R,G,B     | USER GPIO RGB LED_6              |
| DS53      | RGB_[R,G,B]_LED_7        | R,G,B     | USER GPIO RGB LED_7              |

The following figure shows the GPIO and power status LED areas of the board.

Figure 17: GPIO and Power Status LED areas



## Multi-Gigabit Transceivers

The ZU49DR Zynq UltraScale+ RFSoc has 4 GTR gigabit transceivers (6 Gb/s capable) on the PS-side and 16 GTY gigabit transceivers (28 Gb/s capable) on the PL-side. Two of four GTR transceivers are used. All 16 GTY transceivers are used.

## GTY Transceivers

The GTY transceivers in the ZU49DR are grouped into four channels or quads. The reference clock for a quad can be sourced from the quad above or the quad below the GTY quad of interest. The 4 GTY quads used on the ZCU216 board have the connectivity listed below. The following table shows the MGTY assignments.

Table 21: ZCU216 ZU49DR GTY Mapping

| ZCU216 ZU49DR-FFVF1760 GTY Mapping |                          |         |              |       |
|------------------------------------|--------------------------|---------|--------------|-------|
| ZU49DR-FFVF1760                    | 8A34001 CLK1_IN - Q1_OUT | ch3     | GTY Quad 128 | PCIe4 |
|                                    | NO CONNECT               | ch2     |              |       |
|                                    | zSFP1                    | ch1     |              |       |
|                                    | zSFP0                    | ch0     |              |       |
|                                    | 8A34001 Q11_OUT          | refclk1 |              |       |
|                                    | 8A34001 CLK5_IN          | refclk0 |              |       |
|                                    | CoreHC2 1x8 Connector    | ch3     | GTY Quad 129 | CMAC  |
|                                    | NO CONNECT               | ch2     |              |       |
|                                    | zSFP3                    | ch1     |              |       |
|                                    | zSFP2                    | ch0     |              |       |
|                                    | 8A34001 Q7_OUT           | refclk1 |              |       |
|                                    | 8A34001 CLK6_IN          | refclk0 |              |       |
|                                    | FMC DP3                  | ch3     | GTY Quad 130 | ILKN  |
|                                    | FMC DP2                  | ch2     |              |       |
|                                    | FMC DP1                  | ch1     |              |       |
|                                    | FMC DP0                  | ch0     |              |       |
|                                    | USER_SMA_MGT_CLOCK       | refclk1 |              |       |
|                                    | FMC GBTCLK0 M2C          | refclk0 |              |       |
|                                    | FMC DP7                  | ch3     | GTY Quad 131 | PCIe4 |
|                                    | FMC DP6                  | ch2     |              |       |
|                                    | FMC DP5                  | ch1     |              |       |
|                                    | FMC DP4                  | ch0     |              |       |
|                                    | USER_MGT_SI570_CLOCK     | refclk1 |              |       |
|                                    | FMC GBTCLK1 M2C          | refclk0 |              |       |

### FMCP HSPC

Eight MGTs are provided by PL-side MGT banks 130 and 131. Available MGT reference clocks include the FMC defined GBT clocks 0 and 1, a programmable SI570 clock and a differential SMA clock.

### zSFP+

Four MGTs are provided by PL-side MGT banks 128 and 129 for the quad (2x2 connector) zSFP+ interface. Available GTY reference clocks include two sets of clocks to/from IDT 8A34001 U409. Each zSFP+ connector provides an I2C based control interface. This I2C interface is accessible for each individual zSFP+ module through the I2C multiplexer topology on the ZCU216.

For additional information on GTY transceivers, see the *UltraScale Architecture GTY Transceivers User Guide* ([UG578](#)).

The detailed RFSoc connections for the feature described in this section are documented in the ZCU216 board XDC file, referenced in [Appendix B: Xilinx Design Constraints](#).

## PS GTR Transceivers

The PS-side GTR transceiver Bank 505 supports USB (3.0) and SATA, with two channels not used.

Bank 505 USB0 lane 2 supports the USB0 (USB3.0) interface documented in the USB 3.0 Transceiver and USB 2.0 ULPI PHY section. The PS-Side GTR transceiver is used to provide USB 3.0 Host-Only connectivity.

Bank 505 SATA lane 3 supports SATA connector U36 shown in [Figure 18: M.2 Connector](#).

Bank 505 reference clocks are connected to the U43 SI5341B clock generator as detailed in [SI5341B 10 Independent Output Any-Frequency Clock Generator U43](#).

The detailed RFSoc connections for the feature described in this section are documented in the ZCU216 board XDC file, referenced in [Appendix B: Xilinx Design Constraints](#).

## PS M.2 SATA Connector

[[Figure 2](#), callout 31 and 32]

The M.2 SATA interface is provided for SATA SSD access using the PS-Side bank 505 GTR transceiver. The following figure shows M.2 connector U36.

The Socket 2 SATA adapter pinout with Key M is shown in the table below. SATA-A data connection is used for TX and SATA-B for RX. The M.2 connector U36 is a type 2242 (active component section 22 mm wide with overall length 42 mm form factor) used on Socket 2.

Figure 18: M.2 Connector

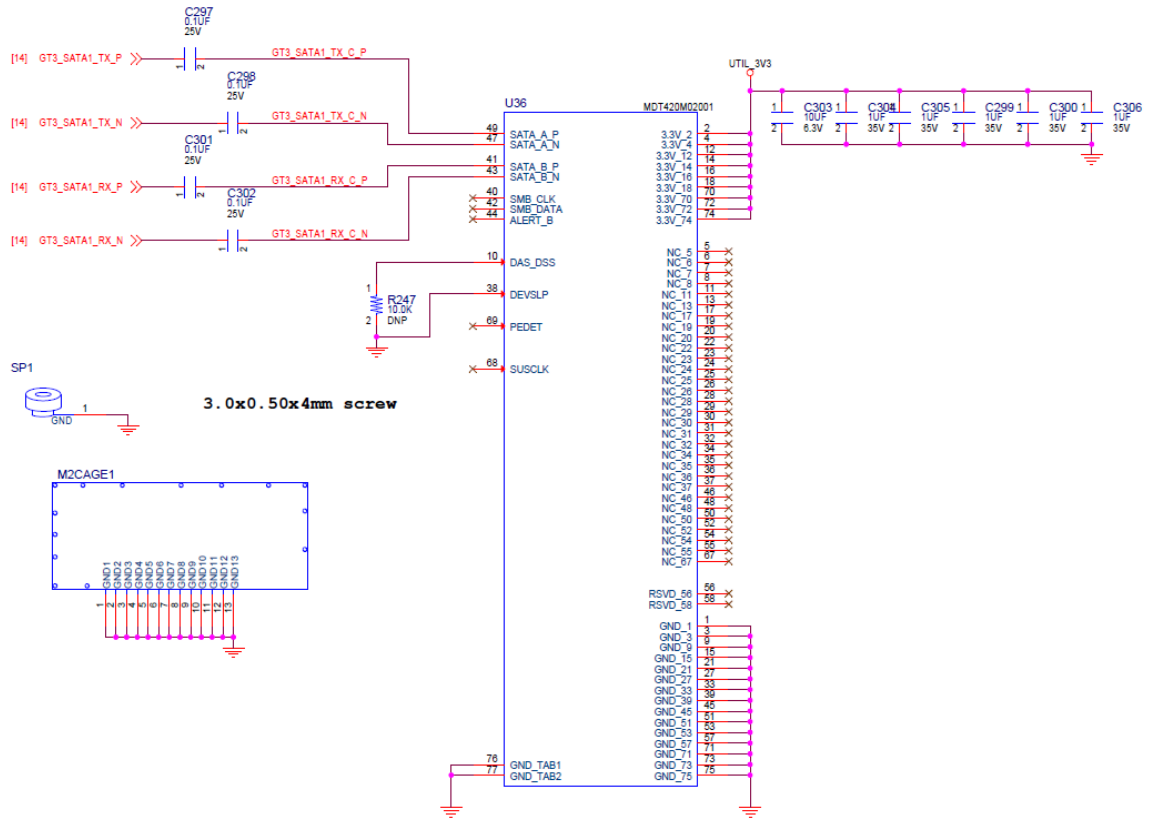


Table 22: M.2 Connector U40 Pinout

| Pin | Signal                     | Signal            | Pin |
|-----|----------------------------|-------------------|-----|
| 74  | 3.3V                       | GND               | 75  |
| 72  | 3.3V                       | GND               | 73  |
| 70  | 3.3V                       | GND               | 71  |
| 68  | SUSCLK(32 kHz) (I)(0/3.3V) | PEDET (GND-SATA)  | 69  |
|     | ADD_IN CARD KEY M          | NC                | 67  |
|     | ADD_IN CARD KEY M          | ADD_IN CARD KEY M |     |
|     | ADD_IN CARD KEY M          | ADD_IN CARD KEY M |     |
|     | ADD_IN CARD KEY M          | ADD_IN CARD KEY M |     |
| 58  | Reserved for MFG_CLOCK     | ADD_IN CARD KEY M |     |
| 56  | Reserved for MFG_DATA      | GND               | 57  |
| 54  | NC                         | NC                | 55  |
| 52  | NC                         | NC                | 53  |
| 50  | NC                         | GND               | 51  |
| 48  | NC                         | SATA-A+           | 49  |
| 46  | NC                         | SATA-A-           | 47  |
| 44  | ALERT# (O) (0/1.8V)        | GND               | 45  |

Table 22: M.2 Connector U40 Pinout (cont'd)

| Pin | Signal                  | Signal  | Pin |
|-----|-------------------------|---------|-----|
| 42  | SMB_DATA (I/O) (0/1.8V) | SATA-B- | 43  |
| 40  | SMB_CLK (I/O) (0/1.8V)  | SATA-B+ | 41  |
| 38  | DEVSLP (I)              | GND     | 39  |
| 36  | NC                      | NC      | 37  |
| 34  | NC                      | NC      | 35  |
| 32  | NC                      | GND     | 33  |
| 30  | NC                      | NC      | 31  |
| 28  | NC                      | NC      | 29  |
| 26  | NC                      | GND     | 27  |
| 24  | NC                      | NC      | 25  |
| 22  | NC                      | NC      | 23  |
| 20  | NC                      | GND     | 21  |
| 18  | 3.3V                    | NC      | 19  |
| 16  | 3.3V                    | NC      | 17  |
| 14  | 3.3V                    | GND     | 15  |
| 12  | 3.3V                    | NC      | 13  |
| 10  | DAS/DSS (I/O)           | NC      | 11  |
| 8   | NC                      | GND     | 9   |
| 6   | NC                      | NC      | 7   |
| 4   | 3.3V                    | NC      | 5   |
| 2   | 3.3V                    | GND     | 3   |
| -   | -                       | GND     | 1   |

The M.2 adapter tie-offs as implemented on the ZCU216 board are listed in the following table.

Table 23: ZCU216 M.2 U40 Connector Tie-offs

| M.2 Signal Name | ZCU104 Tie-Off | U40 Pin |
|-----------------|----------------|---------|
| SUSCLK          | No Connect     | 68      |
| ALERT#          | No Connect     | 44      |
| SMB_DATA        | No Connect     | 42      |
| SMB_CLK         | No Connect     | 40      |
| DEVSLP          | GND            | 38      |
| DAS/DSS         | DNP Res to GND | 10      |
| PEDET           | No Connect     | 69      |
| SATA-A          | GTR TX         | 49, 47  |
| SATA-B          | GTR RX         | 43, 41  |

The M.2 U40 connector to RFSoc connections are listed in the following table.

Table 24: M.2 U40 Connections to the XCZU49DR Zynq UltraScale+ RFSoc

| XCZU49DR (U1) Pin | Net Name       | I/O Standard | M.2 Connector U40 |          |
|-------------------|----------------|--------------|-------------------|----------|
|                   |                |              | Pin Number        | Pin Name |
| AD36              | GT3_SATA1_TX_P | 1            | 49                | SATA-A+  |
| AD37              | GT3_SATA1_TX_N | 1            | 47                | SATA-A-  |
| AC38              | GT3_SATA1_RX_P | 1            | 41                | SATA-B+  |
| AC39              | GT3_SATA1_RX_N | 1            | 43                | SATA-B-  |

**Notes:**

1. Series capacitor coupled, MGT I/F and I/O standards do not apply.

For more information, see [PCI\\_Express\\_M.2\\_Specification\\_Rev1.1\\_TS\\_12092016\\_NCB](#) on the [PCI-SIG](#) website.

The detailed RFSoc connections for the feature described in this section are documented in the ZCU216 board XDC file, referenced in [Appendix B: Xilinx Design Constraints](#).

## FPGA Mezzanine Card Interface

The ZCU216 evaluation board supports the VITA 57.4 FPGA mezzanine card plus (FMC+ or FMCP) specification by providing a subset implementation of the high pin count connector at J28 (HSPC). FMC+ connectors use a 14 x 40 form factor, populated with 560 pins. The connector is keyed so that a mezzanine card, when installed on the ZCU216 evaluation board, faces away from the board.

### FMCP Connector J28

Samtec SEAF series, 1.27 mm (0.050 in) pitch. Mates with SEAM series connector. More information about SEAF series connectors is available on the [Samtec, Inc.](#) website. More information about the VITA 57.4 FMC+ specification is available on the [VITA FMC Marketing Alliance](#) website.

The 560-pin FMC+ connector defined by the FMC specification (see [Appendix A: VITA 57.4 FMCP Connector Pinout](#)) provides connectivity for up to:

- 160 single-ended or 80 differential user-defined signals
- 24 transceiver differential pairs
- 6 transceiver differential clocks
- 4 differential clocks
- 239 ground and 19 power connections

## FMCP Connector J28

[Figure 2, callout 25]

The HSPC connector J28 implements a subset of the full FMCP connectivity:

- 68 single-ended or 34 differential user-defined pairs (34 LA pairs: LA[00:33])
- 8 transceiver differential pairs
- 2 transceiver differential clocks
- 2 differential clocks
- 239 ground and 16 power connections

See the FPGA Mezzanine Card (FMC) VITA 57.4 specification on the [VITA FMC Marketing Alliance](#) website for additional information on the FMCP HSPC connector.

The detailed RFSoc connections for the feature described in this section are documented in the ZCU216 board XDC file, referenced in [Appendix B: Xilinx Design Constraints](#).

## Cooling Fan Connector

[Figure 2, near callout 33]

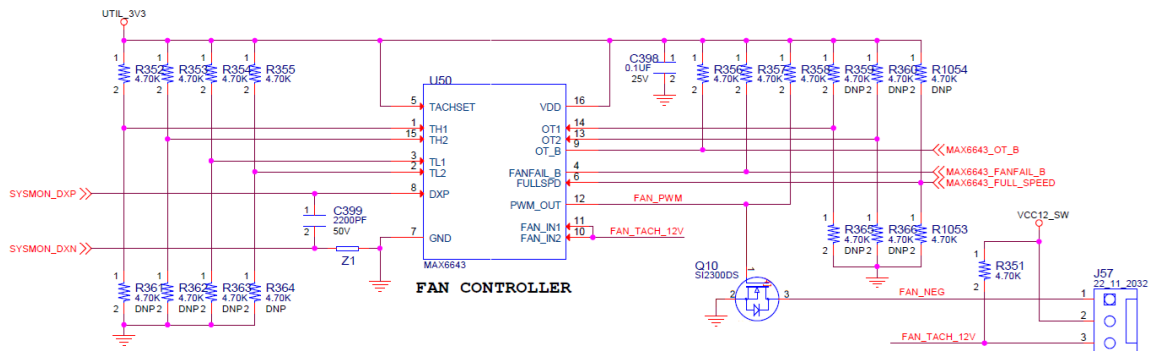
The ZCU216 cooling fan circuit is shown in the figure below.

The ZCU216 uses the Infineon MAX6643 (U50) fan controller, which autonomously controls the fan speed by controlling the pulse width modulation (PWM) signal to the fan based on the die temperature sensed via the FPGA's DXP and DXN pins. The fan rotates slowly (acoustically quiet) when the RFSoc is cool and rotates faster as the FPGA heats up (acoustically noisy). The fan speed (PWM) versus the RFSoc die temperature algorithm along with the over temperature set point and fan failure alarm mechanisms are defined by the strapping resistors on the MAX6643 device. The over temperature and fan failures alarms can be monitored by any available processor in the RFSoc by polling the I2C expander U15 on the I2C0 bus. See the MAX6643 data sheet on the [Maxim Integrated Circuits](#) website for more information on the device circuit implementation on this board.

**Note:** At initial power On, it is normal for the fan controller to energize at full speed for a few seconds.



Figure 19: ZCU216 Cooling Fan Circuit



## VADJ\_FMC Power Rail

The ZCU216 evaluation board implements the ANSI/VITA 57.1 section 5.5.1 IPMI support functionality. The power control of the VADJ\_FMC power rail is managed by the U38 system controller. This rail powers the FMCP HSPC (J28) VADJ pins, as well as the ZU49DR HP banks 66 and 67. The valid values of the VADJ\_FMC rail are 1.2V, 1.5V, and 1.8V.

At power On, the system controller detects if an FMC module is installed on J28:

- If no card is attached to the FMCP connector, the VADJ voltage is set to 1.8V.
- When an FMC card is attached, its IIC EEPROM is read to find a VADJ voltage supported by both the ZCU216 board and the FMC module, within the available choices of 0.0V, 1.2V, 1.5V, and 1.8V.
- If no valid information is found in an FMC card IIC EEPROM, the VADJ\_FMC rail is set to 0.0V.

The system controller user interface allows the FMC IPMI routine to be overridden and an explicit value can be set for the VADJ\_FMC rail. Override mode is useful for FMC mezzanine cards that do not contain valid IPMI EPROM data defined by the ANSI/VITA57.1 specification.

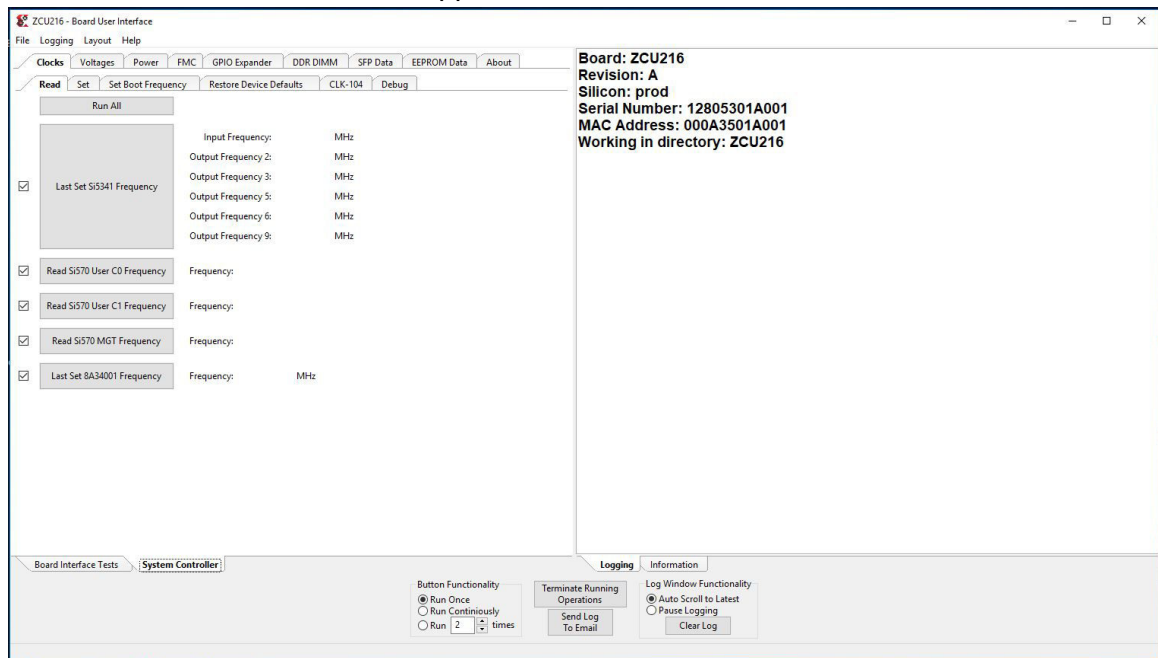
## ZCU216 MSP430 System Controller

[Figure 2, callout 19]

The ZCU216 board includes an on-board MSP430 (U38) with integrated Power Advantage demo and System Controller firmware. A Host PC resident system controller board user interface is provided on the [ZCU216 documentation web page](#). The board user interface enables you to query and control select programmable features such as clocks, FMC functionality, and power system parameters. The ZCU216 web page also includes the [ZCU216 System Controller GUI Tutorial \(XTP\\_TBD\)](#) and [ZCU216 Software Install and Board Setup Tutorial \(XTP\\_TBD\)](#).

The following briefly summarizes these instructions:

1. Ensure that the Silicon Labs VCP USB-UART drivers are installed *Silicon Labs CP210x USB-to-UART Installation Guide (UG1033)*.
2. Download the board user interface Host PC application from the board documentation web page.
3. Connect the micro-USB cable to ZCU216 USB-UART connector (J24).
4. Power-cycle the ZCU216.
5. Observe that SYSCTLR LED0 (DS9) blinks and LED1 (DS10) is illuminated.
6. Launch the board user interface application.



On first use of the board user interface, go to the **FMC → Set VADJ → Boot-up** tab and click **USE FMC EEPROM Voltage**. The board user interface buttons grey-out during command execution and return to their original appearance when ready to accept a new command.

See the ZCU216 System Controller GUI Tutorial (XTP\_TBD) and the ZCU216 Software Install and Board Setup Tutorial (XTP\_TBD) for more information on installing and using the System Controller board user interface utility.

## Switches

[Figure 2, callouts 23 and 24]

The ZCU216 board includes the following power, configuration, and reset switches:

- SW15 Power On/Off slide switch (callout 24)
- SW3 (PS\_PROG\_B), active-Low pushbutton (callout 23)

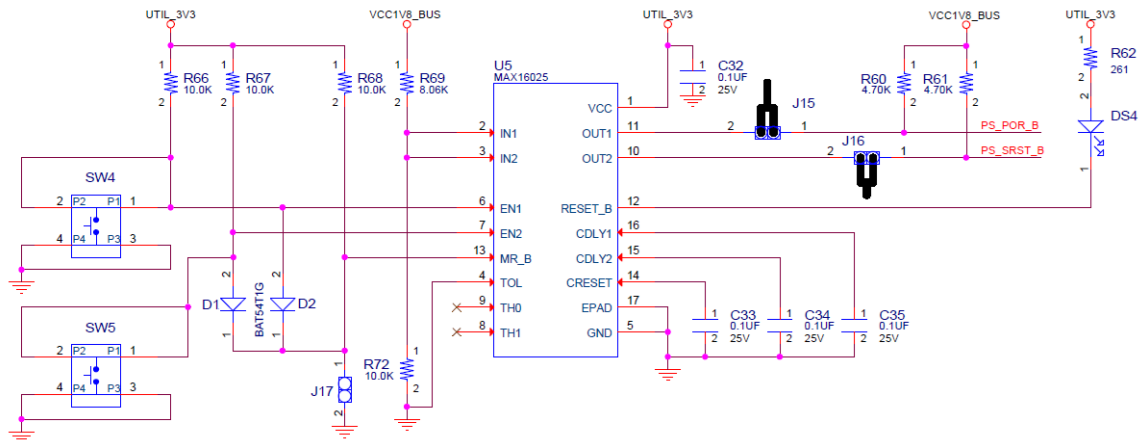


## System Reset Pushbuttons

[Figure 2, callout 23]

The following figure shows the reset circuitry for the processing system.

Figure 21: POR\_B SW4 and PS SRST\_B SW5 Pushbutton Switches



### PS\_POR\_B Reset

Depressing and then releasing pushbutton SW4 causes net PS\_POR\_B to strobe Low. This reset is used to hold the PS in reset until all PS power supplies are at the required voltage levels. It must be held Low through PS power-up. PS\_POR\_B must be generated by the power supply power-good signal. When the voltage at IN1 is below its threshold or EN1 (P.B. switch SW4 is pressed) goes Low, OUT1 (PS\_POR\_B) goes Low.

### PS\_SRST\_B Reset

Depressing and then releasing pushbutton SW5 causes net PS\_SRST\_B to strobe Low. This reset is used to force a system reset. It can be tied or pulled High, and can be High during the PS supply power ramps. When the voltage at IN2 is below its threshold or EN2 (P.B. switch SW5 is pressed) goes Low, OUT2 (PS\_SRST\_B) goes Low.

Active-Low Reset Output RESET\_B asserts when any of the monitored voltages (IN\_) falls below its respective threshold, any EN\_ goes Low, or MR is asserted. RST\_B remains asserted for the reset time-out period after all of the monitored voltages exceed their respective threshold, all EN\_ are High, all OUT\_ are high, and MR is de-asserted. See the *Zynq UltraScale+ Device Technical Reference Manual (UG1085)* for more information about resets.

## Board Power System

[Figure 2, callout 39, 40, and 41]

The ZCU216 evaluation board uses power management ICs (PMIC) and regulators from [Infineon Integrated Circuits](#) and [MPS](#) to supply the core and auxiliary voltages listed in the following table. Reference schematic 038-05003-01.

**Table 25: ZCU216 Power System Devices**

| Ref. Des., PMBUS ADDR | Controller or Regulator | Rail Name                     | Voltage (V) | Max. Current (A) | INA226 Power Monitor | INA226 PMBUS ADDR | Sense Resistor ( $\Omega$ ) | Schem. Page |
|-----------------------|-------------------------|-------------------------------|-------------|------------------|----------------------|-------------------|-----------------------------|-------------|
| PMIC1 U104 (0X40)     | IR35215_PWM1/2          | V <sub>CCINT</sub>            | 0.85        | 60               | U65                  | 0x40              | R440: 0.0005                | 47          |
|                       | IR35215_PWM1_L2         | V <sub>CCINT_AMS</sub>        | 0.85        | 28               | U61                  | 0x49              | R1098: 0.0005               |             |
| PMIC2 U53 (0X44)      | IRPS5401_A              | V <sub>CC1V2</sub>            | 1.2         | 6                | U58                  | 0x43              | R408: 0.005                 | 50          |
|                       | IRPS5401_B              | UTIL_1V13                     | 1.13        | 500 mA           | NA                   | NA                | NA                          |             |
|                       | IRPS5401_C              | VADJ_FMC                      | 1.8         | 6                | U62                  | 0x45              | R382: 0.005                 |             |
|                       | IRPS5401_D              | Tied to channel C             |             |                  |                      |                   |                             |             |
|                       | IRPS5401_LDO            | MGT1V8                        | 1.8         | 500 mA           | U64                  | 0x48              | R787: 0.005                 |             |
| PMIC3 U55 (0X45)      | IRPS5401_A              | NC                            | NA          | NA               | NA                   | NA                | NA                          | 52          |
|                       | IRPS5401_B              | UTIL_2V5                      | 2.5         | 500 mA           | NA                   | NA                | NA                          |             |
|                       | IRPS5401_C              | MGT1V2                        | 1.2         | 7                | U63                  | 0x47              | R400: 0.005                 |             |
|                       | IRPS5401_D              | Tied to 3C                    |             |                  |                      |                   |                             |             |
|                       | IRPS5401_LDO            | MGTRAVCC                      | 0.85        | 500 mA           | NA                   | NA                | NA                          |             |
| U127 (0X4B)           | IR38164                 | V <sub>CCINT_IO_BRAM_PS</sub> | 0.85        | 18               | U57                  | 0x41              | R1099: 0.0005               | 53          |
| U112 (0x43)           | IR38164                 | MGTAVCC                       | 0.9         | 4                | U67                  | 0x46              | R455: 0.002                 | 54          |
| U123 (0x4C)           | IR38164                 | VCC1V8                        | 1.8         | 8                | U60                  | 0x42              | R879: 0.002                 | 55          |
| U115                  | MPM3683-7               | ADC_AVCC                      | 0.925       | 4                | U75                  | 0x4C              | R499: 0.005                 | 56          |
| U116                  | MPM3683-7               | DAC_AVCC                      | 0.925       | 6                | U77                  | 0x4E              | R504: 0.005                 | 56          |
| U114                  | MPM3833C                | ADC_AVCCAUX                   | 1.8         | 2                | U71                  | 0x4D              | R475: 0.005                 | 57          |
| U125                  | MPM3833C                | DAC_AVCCAUX                   | 1.8         | 1.5              | U124                 | 0x4B              | R889: 0.005                 | 58          |
| U118                  | MPM3833C                | DAC_AVCCAUX                   | 2.5/3.0     | 1.5              | U59                  | 0x4A              | R869: 0.005                 | 58          |
| U111                  | IR3889                  | UTIL_3V3                      | 3.3         | 15               | NA                   | NA                | NA                          | 60          |
| U126                  | IR3889                  | UTIL_5V0                      | 5           | 10               | NA                   | NA                | NA                          | 61          |
| U79                   | IR3897                  | PL_DDR4_C0_VT                 | 0.6         | +/- 3.0          | NA                   | NA                | NA                          | 61          |
| U108                  | IR3897                  | PL_DDR4_C1_VT                 | 0.6         | +/- 3.0          | NA                   | NA                | NA                          | 61          |
| U80                   | IR3897                  | PS_DDR4_VTT                   | 0.6         | +/- 3.0          | NA                   | NA                | NA                          | 62          |

The FMCP HSPC (J28) V<sub>ADJ</sub> pins and RFSoc U1 banks 66 and 67 V<sub>CCO</sub> pins are wired to the programmable rail VADJ\_FMC. The VADJ\_FMC rail is programmed to 1.80V by default.

Documentation describing PMBUS programming for the Infineon power controllers as well as PMIC and voltage regulator data sheets are available on the [Infineon Integrated Circuits](#) website.

Non-PMBus ADC and DAC voltage regulator data sheets can be viewed on the [MPS](#) website.

The PCB layout and power system design meet the recommended criteria described in the *UltraScale Architecture PCB Design User Guide (UG583)*.



**RECOMMENDED:** To ensure reliable operation, Xilinx recommends running the `report_power` command in the Vivado tools for designs targeting this board. The reported rail current requirements must not exceed the values listed in the following table.

Table 26: Device Rail Maximum Current

| Device Rail   | Maximum Current (Amps) |
|---|------------------------|
| V <sub>CCINT</sub>  | 60                     |
| V <sub>CCINT_IO</sub> + V <sub>CCBRAM</sub> + V <sub>CC_PSINTLP</sub> + V <sub>CC_PSINTFP</sub> + V <sub>CC_PSINTFP_DDR</sub>   | 18                     |
| MGTYV <sub>CCAUX</sub> + V <sub>PS_MGTRAVTT</sub>   | 0.5                    |
| MGTYA <sub>VCC</sub>  | 4                      |
| V <sub>PS_MGTRAVCC</sub>  | 0.5                    |
| MGTYA <sub>VTT</sub> + V <sub>CC_PSPLL</sub>  | 7                      |
| V <sub>CCINT_AMS</sub>  | 28                     |
| V <sub>ADC_AVCC</sub>   | 4                      |
| V <sub>ADC_AVCCAUX</sub>  | 2                      |
| V <sub>DAC_AVCC</sub>   | 6                      |
| V <sub>DAC_AVCCAUX</sub>  | 1.5                    |
| V <sub>DAC_AVTT</sub>   | 1.5                    |
| V <sub>CCAUX</sub> + V <sub>CCAUX_IO</sub> + V <sub>CCO 1.8V</sub> + V <sub>CCAUX_IO</sub> + V <sub>CC_PSAUX</sub> + V <sub>CC_PSDDR_PLL</sub> + V <sub>CCO_PSIO0_500</sub> + V <sub>CCO_PSIO1_501</sub> + V <sub>CCO_PSIO2_502</sub> + V <sub>CCO_PSIO3_503</sub> + V <sub>CCADC</sub> + V <sub>CC_PSADC</sub> | 8                      |
| V <sub>CCO 1.2V</sub> + V <sub>CCO_PSDDR_504</sub>  | 6                      |
| V <sub>CCO #V</sub> (# corresponds to VADJ programmed voltage)  | 6                      |

The total device power must remain under 50W. To assist the Vivado tools in reporting when power exceeds this amount, add this XDC constraint:

```
set_operating_conditions -design_power_budget 50 ;# (50W max power)
```

## Monitoring Voltage and Current

Voltage and current monitoring and control are available for the Infineon power system controllers through the Infineon PowIRCenter graphical user interface. The PMBus interface controllers and regulators are accessed through 1x3 PMBus connector J21, that is provided for use with the Infineon PowIRCenter USB cable (Infineon part number USB005) and can be ordered from the [Infineon Integrated Circuits](https://www.infineon.com) website. The associated Infineon PowerTool GUI can be downloaded from the Infineon website. This is the simplest and most convenient way to monitor the voltage and current values for the Infineon PMBus programmed power rails listed in [Table 25](#).

Each Infineon PMIC controller is capable of reporting the voltage and current of its controlled rail to the Infineon GUI for display to the user. Fourteen rails have a TI INA226 PMBus power monitor circuit with connections to the rail series current sense resistor. This arrangement permits the INA226 to report the sensed parameters separately on the INA226\_PMBUS. The rails configured with the INA226 power monitors are shown in [Table 25](#).

As described in [I2C0 \(MIO 14-15\)](#), the I2C0 bus provides access to the PMBus power controllers and the INA226 power monitors through the U17 PCA9544A bus switch. All PMBus controlled Infineon regulators are tied to the IRPS5401\_SDA/SCL PMBUS, while the INA226 power monitors are separated on to INA226\_PMBUS.

[Figure 7](#) and [Table 10](#) document the I2C0 bus access path to the Infineon PMBus controllers and INA226 power monitor op amps. Also refer to schematic 038-05003-01. Power rail measurements are accessible to the system controller and RFSoc PL logic through their respective I2C0 bus connections.

# VITA 57.4 FMCP Connector Pinout

## Overview

The following figure shows the pinout of the FPGA plus mezzanine card (FMCP) high pin count (HSPC) connector defined by the VITA 57.4 FMC specification. For a description of how the ZCU216 evaluation board implements the FMCP specification, see [FPGA Mezzanine Card Interface](#).

Figure 22: FMCP HSPC Connector Pinout

| 10 x 40 | K            | J            | H           | G          | F         | E         | D             | C         | B             | A         |
|---------|--------------|--------------|-------------|------------|-----------|-----------|---------------|-----------|---------------|-----------|
| 1       | VREF_B_M2C   | GND          | VREF_A_M2C  | GND        | PG_M2C    | GND       | PG_C2M        | GND       | RES1          | GND       |
| 2       | GND          | CLK3_BIDIR_P | PRSNT_M2C_L | CLK1_M2C_P | GND       | HA01_P_CC | GND           | DP0_C2M_P | GND           | DP1_M2C_P |
| 3       | GND          | CLK3_BIDIR_N | GND         | CLK1_M2C_N | GND       | HA01_N_CC | GND           | DP0_C2M_N | GND           | DP1_M2C_N |
| 4       | CLK2_BIDIR_P | GND          | CLK0_M2C_P  | GND        | HA00_P_CC | GND       | 6BTCLK0_M2C_F | GND       | DP9_M2C_P     | GND       |
| 5       | CLK2_BIDIR_N | GND          | CLK0_M2C_N  | GND        | HA00_N_CC | GND       | 6BTCLK0_M2C_N | GND       | DP9_M2C_N     | GND       |
| 6       | GND          | HA03_P       | GND         | LA00_P_CC  | GND       | HA05_P    | GND           | DP0_M2C_P | GND           | DP2_M2C_P |
| 7       | HA02_P       | HA03_N       | LA02_P      | LA00_N_CC  | HA04_P    | HA05_N    | GND           | DP0_M2C_N | GND           | DP2_M2C_N |
| 8       | HA02_N       | GND          | LA02_N      | GND        | HA04_N    | GND       | LA01_P_CC     | GND       | DP8_M2C_P     | GND       |
| 9       | GND          | HA07_P       | GND         | LA03_P     | GND       | HA09_P    | LA01_N_CC     | GND       | DP8_M2C_N     | GND       |
| 10      | HA06_P       | HA07_N       | LA04_P      | LA03_N     | HA08_P    | HA09_N    | GND           | LA06_P    | GND           | DP3_M2C_P |
| 11      | HA06_N       | GND          | LA04_N      | GND        | HA08_N    | GND       | LA05_P        | LA06_N    | GND           | DP3_M2C_N |
| 12      | GND          | HA11_P       | GND         | LA08_P     | GND       | HA13_P    | LA05_N        | GND       | DP7_M2C_P     | GND       |
| 13      | HA10_P       | HA11_N       | LA07_P      | LA08_N     | HA12_P    | HA13_N    | GND           | GND       | DP7_M2C_N     | GND       |
| 14      | HA10_N       | GND          | LA07_N      | GND        | HA12_N    | GND       | LA09_P        | LA10_P    | GND           | DP4_M2C_P |
| 15      | GND          | HA14_P       | GND         | LA12_P     | GND       | HA16_P    | LA09_N        | LA10_N    | GND           | DP4_M2C_N |
| 16      | HA17_P_CC    | HA14_N       | LA11_P      | LA12_N     | HA15_P    | HA16_N    | GND           | GND       | DP8_M2C_P     | GND       |
| 17      | HA17_N_CC    | GND          | LA11_N      | GND        | HA15_N    | GND       | LA13_P        | GND       | DP8_M2C_N     | GND       |
| 18      | GND          | HA18_P       | GND         | LA16_P     | GND       | HA20_P    | LA13_N        | LA14_P    | GND           | DP5_M2C_P |
| 19      | HA21_P       | HA18_N       | LA15_P      | LA16_N     | HA19_P    | HA20_N    | GND           | LA14_N    | GND           | DP5_M2C_N |
| 20      | HA21_N       | GND          | LA15_N      | GND        | HA19_N    | GND       | LA17_P_CC     | GND       | 6BTCLK1_M2C_F | GND       |
| 21      | GND          | HA22_P       | GND         | LA20_P     | GND       | HB03_P    | LA17_N_CC     | GND       | 6BTCLK1_M2C_N | GND       |
| 22      | HA23_P       | HA22_N       | LA19_P      | LA20_N     | HB02_P    | HB03_N    | GND           | LA18_P_CC | GND           | DP1_C2M_P |
| 23      | HA23_N       | GND          | LA19_N      | GND        | HB02_N    | GND       | LA23_P        | LA18_N_CC | GND           | DP1_C2M_N |
| 24      | GND          | HB01_P       | GND         | LA22_P     | GND       | HB05_P    | LA23_N        | GND       | DP9_C2M_P     | GND       |
| 25      | HB00_P_CC    | HB01_N       | LA21_P      | LA22_N     | HB04_P    | HB05_N    | GND           | GND       | DP9_C2M_N     | GND       |
| 26      | HB00_N_CC    | GND          | LA21_N      | GND        | HB04_N    | GND       | LA26_P        | LA27_P    | GND           | DP2_C2M_P |
| 27      | GND          | HB07_P       | GND         | LA25_P     | GND       | HB09_P    | LA26_N        | LA27_N    | GND           | DP2_C2M_N |
| 28      | HB06_P_CC    | HB07_N       | LA24_P      | LA25_N     | HB08_P    | HB09_N    | GND           | GND       | DP8_C2M_P     | GND       |
| 29      | HB06_N_CC    | GND          | LA24_N      | GND        | HB08_N    | GND       | TCK           | GND       | DP8_C2M_N     | GND       |
| 30      | GND          | HB11_P       | GND         | LA29_P     | GND       | HB13_P    | TDI           | SCL       | GND           | DP3_C2M_P |
| 31      | HB10_P       | HB11_N       | LA28_P      | LA29_N     | HB12_P    | HB13_N    | TDO           | SDA       | GND           | DP3_C2M_N |
| 32      | HB10_N       | GND          | LA28_N      | GND        | HB12_N    | GND       | 3P3VAUX       | GND       | DP7_C2M_P     | GND       |
| 33      | GND          | HB15_P       | GND         | LA31_P     | GND       | HB19_P    | TMS           | GND       | DP7_C2M_N     | GND       |
| 34      | HB14_P       | HB15_N       | LA30_P      | LA31_N     | HB16_P    | HB19_N    | TRST_L        | GA0       | GND           | DP4_C2M_P |
| 35      | HB14_N       | GND          | LA30_N      | GND        | HB16_N    | GND       | GA1           | 12P0V     | GND           | DP4_C2M_N |
| 36      | GND          | HB18_P       | GND         | LA33_P     | GND       | HB21_P    | 3P3V          | GND       | DP6_C2M_P     | GND       |
| 37      | HB17_P_CC    | HB18_N       | LA32_P      | LA33_N     | HB20_P    | HB21_N    | GND           | 12P0V     | DP6_C2M_N     | GND       |
| 38      | HB17_N_CC    | GND          | LA32_N      | GND        | HB20_N    | GND       | 3P3V          | GND       | GND           | DP5_C2M_P |
| 39      | GND          | VIO_B_M2C    | GND         | VADJ       | GND       | VADJ      | GND           | 3P3V      | GND           | DP5_C2M_N |
| 40      | VIO_B_M2C    | GND          | VADJ        | GND        | VADJ      | GND       | 3P3V          | GND       | RES0          | GND       |



# Xilinx Design Constraints

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## Overview

The Xilinx design constraints (XDC) file template for the ZCU216 board provides for designs targeting the ZCU216 evaluation board. Net names in the constraints listed correlate with net names on the latest ZCU216 evaluation board schematic. Identify the appropriate pins and replace the net names with net names in the user RTL. See the *Vivado Design Suite User Guide: Using Constraints* ([UG903](#)) for more information.

The HSPC FMCP connector J28 is connected to Zynq® UltraScale+™ RFSoc U1 banks powered by the variable voltage VADJ\_FMC. The FMC bank I/O standards must be uniquely defined by each customer because different FMC cards implement different circuitry.



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**IMPORTANT!** See the [ZCU216 board documentation](#) ("Board Files" check box) for the XDC file.

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# XM650/XM655 Balun Add-on Cards for RFSoc EVM

## Overview

XM650 and XM655 are the RFMC 2.0 add-on cards for use with the Zynq UltraScale+ RFSoc Gen3 ZCU216 evaluation board. These add-on cards enable ZCU216 connectivity from the DAC and ADC for loopback evaluation and for instrumentation use cases.

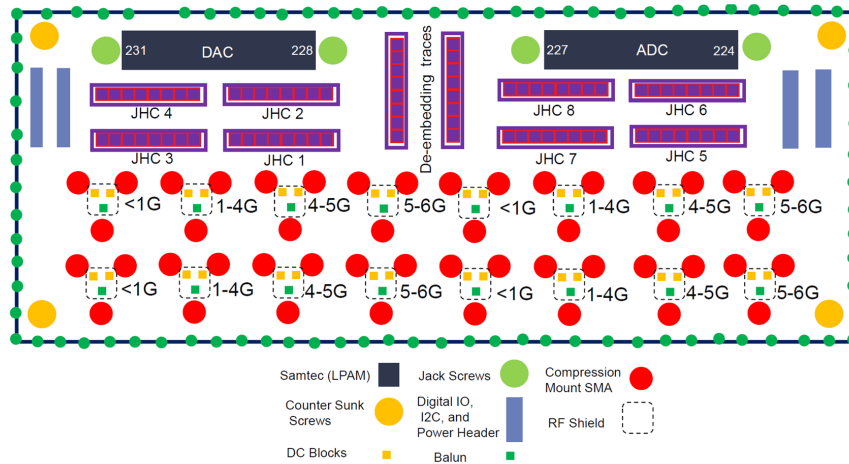
- The XM650 add-on card is a DAC to ADC loopback evaluation with N79 band baluns and filters, no external connectivity.
- The XM655 add-on card is a full break-out of 16 DAC channels x 16 ADC channels to SMA connectivity using Carlisle-CoreHC2 assembly connections.

|                 |   |
|-----------------|---|
| Base Board      | ZCU216  |
| ADC Channels    | 16  |
| DAC Channels    | 16  |
| Balun           | XM650: N79 or B46 band with BOM change<br>XM655: Low/Mid/High Frequency |
| Filter          | XM650: N79 or B46 band with BOM change<br>XM655: No                     |
| Interconnection | 2x Samtec LPAM 8x50   |

# Block Diagram

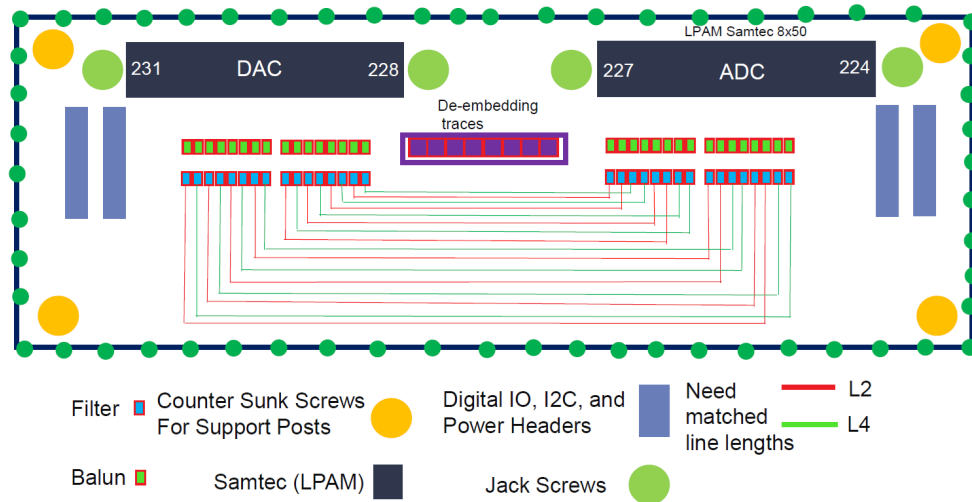
## XM655: 16T16R Breakout Add-on Card

Figure 23: XM655 Block Diagram



## XM650: 16T16R N79 Band Loopback Demo Add-on Card

Figure 24: XM650 Block Diagram



## Connector

Table 28: RFMC 2.0 Connector Parameters

| Parameter      | Value   |
|----------------|---|
| Part Number    | LPAM-50-01.0-L-08-2-K-TR                            |
| Data Rate      | 18 Gb/s   |
| Connector Type | LP Array (.050"/1.27 mm pitch)                      |
| IO pins        | 8x50  |
| Stack Height   | .157"/4.00 mm (Mated with LPAF-50-03.0-L-08-2-K-TR) |
| Make           | SAMTEC  |
| Description    | Low Profile Open Pin Field Array, male connector    |
| Data Sheet     | See the <a href="#">Samtec</a> website.             |

Figure 25: LPAM-50-01.0-L-08-2-K-TR 3D View

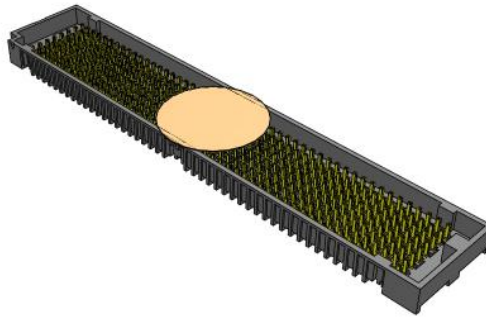
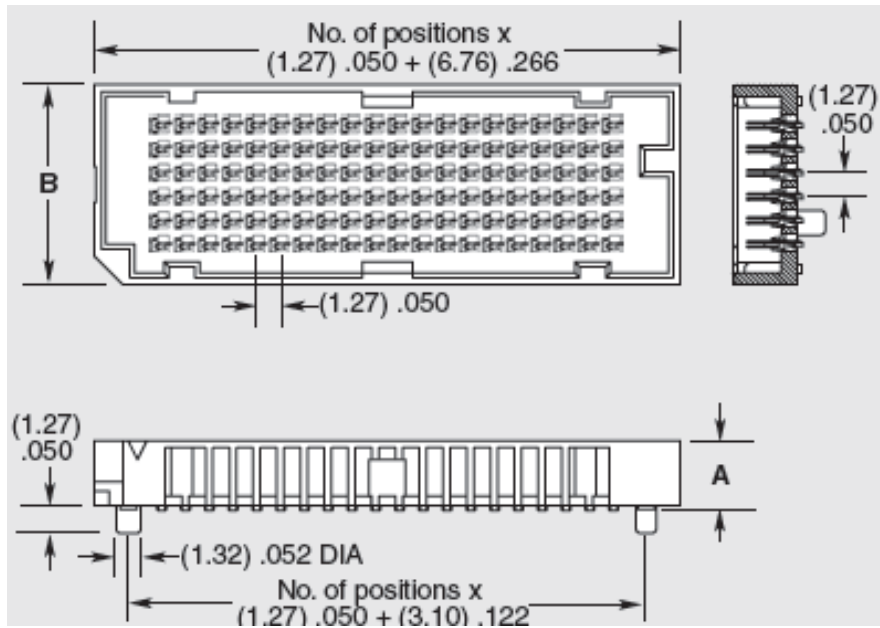


Figure 26: LPAM Connector Drawing



## XM650/655 Connector Pinout

| J55 DAC |          |                 |                 |            |          |                 |                 |          |
|---------|----------|-----------------|-----------------|------------|----------|-----------------|-----------------|----------|
|         | A        | B               | C               | D          | E        | F               | G               | H        |
| 1       | GND      | DACIO_VADJ      | GND             | DACIO_VADJ | GND      | DAC_AVTT        | GND             | Spare 1  |
| 2       | DACIO_00 | GND             | DACIO_04        | GND        | DACIO_08 | GND             | DACIO_12        | GND      |
| 3       | GND      | DACIO_02        | GND             | DACIO_06   | GND      | DACIO_10        | GND             | DACIO_14 |
| 4       | DACIO_01 | GND             | DACIO_05        | GND        | DACIO_09 | GND             | DACIO_13        | GND      |
| 5       | GND      | DACIO_03        | GND             | DACIO_07   | GND      | DACIO_11        | GND             | DACIO_15 |
| 6       | 12V      | GND             | 12V             | GND        | 12V      | GND             | 12V             | GND      |
| 7       | GND      | 12V             | GND             | 12V        | GND      | 12V             | GND             | 12V      |
| 8       | 5v0      | GND             | 5v0             | GND        | 5v0      | GND             | 5v0             | GND      |
| 9       | GND      | 5v0             | GND             | 5v0        | GND      | 5v0             | GND             | 5v0      |
| 10      | GND      | GND             | GND             | GND        | GND      | GND             | GND             | GND      |
| 11      | GND      | DAC231_T3_CH3_N | DAC231_T3_CH3_P | GND        | GND      | GND             | GND             | GND      |
| 12      | GND      | GND             | GND             | GND        | GND      | GND             | GND             | GND      |
| 13      | GND      | GND             | GND             | GND        | GND      | GND             | GND             | GND      |
| 14      | GND      | GND             | GND             | GND        | GND      | DAC231_T3_CH2_N | DAC231_T3_CH2_P | GND      |
| 15      | GND      | GND             | GND             | GND        | GND      | GND             | GND             | GND      |

| J55 DAC |     |                 |                 |     |     |                 |                 |     |
|---------|-----|-----------------|-----------------|-----|-----|-----------------|-----------------|-----|
| 16      | GND | DAC231_T3_CH1_N | DAC231_T3_CH1_P | GND | GND | GND             | GND             | GND |
| 17      | GND | GND             | GND             | GND | GND | GND             | GND             | GND |
| 18      | GND | GND             | GND             | GND | GND | GND             | GND             | GND |
| 19      | GND | GND             | GND             | GND | GND | DAC231_T3_CH0_N | DAC231_T3_CH0_P | GND |
| 20      | GND | GND             | GND             | GND | GND | GND             | GND             | GND |
| 21      | GND | DAC230_T2_CH3_N | DAC230_T2_CH3_P | GND | GND | GND             | GND             | GND |
| 22      | GND | GND             | GND             | GND | GND | GND             | GND             | GND |
| 23      | GND | GND             | GND             | GND | GND | GND             | GND             | GND |
| 24      | GND | GND             | GND             | GND | GND | DAC230_T2_CH2_N | DAC230_T2_CH2_P | GND |
| 25      | GND | GND             | GND             | GND | GND | GND             | GND             | GND |
| 26      | GND | DAC230_T2_CH1_N | DAC230_T2_CH1_P | GND | GND | GND             | GND             | GND |
| 27      | GND | GND             | GND             | GND | GND | GND             | GND             | GND |
| 28      | GND | GND             | GND             | GND | GND | GND             | GND             | GND |
| 29      | GND | GND             | GND             | GND | GND | DAC230_T2_CH0_N | DAC230_T2_CH0_P | GND |
| 30      | GND | GND             | GND             | GND | GND | GND             | GND             | GND |
| 31      | GND | DAC229_T1_CH3_N | DAC229_T1_CH3_P | GND | GND | GND             | GND             | GND |
| 32      | GND | GND             | GND             | GND | GND | GND             | GND             | GND |
| 33      | GND | GND             | GND             | GND | GND | GND             | GND             | GND |
| 34      | GND | GND             | GND             | GND | GND | DAC229_T1_CH2_N | DAC229_T1_CH2_P | GND |
| 35      | GND | GND             | GND             | GND | GND | GND             | GND             | GND |
| 36      | GND | DAC229_T1_CH1_N | DAC229_T1_CH1_P | GND | GND | GND             | GND             | GND |
| 37      | GND | GND             | GND             | GND | GND | GND             | GND             | GND |
| 38      | GND | GND             | GND             | GND | GND | GND             | GND             | GND |
| 39      | GND | GND             | GND             | GND | GND | DAC229_T1_CH0_N | DAC229_T1_CH0_P | GND |
| 40      | GND | GND             | GND             | GND | GND | GND             | GND             | GND |
| 41      | GND | DAC228_T0_CH3_N | DAC228_T0_CH3_P | GND | GND | GND             | GND             | GND |
| 42      | GND | GND             | GND             | GND | GND | GND             | GND             | GND |
| 43      | GND | GND             | GND             | GND | GND | GND             | GND             | GND |
| 44      | GND | GND             | GND             | GND | GND | DAC228_T0_CH2_N | DAC228_T0_CH2_P | GND |
| 45      | GND | GND             | GND             | GND | GND | GND             | GND             | GND |
| 46      | GND | DAC228_T0_CH1_N | DAC228_T0_CH1_P | GND | GND | GND             | GND             | GND |
| 47      | GND | GND             | GND             | GND | GND | GND             | GND             | GND |

| J55 DAC |     |     |     |     |     |                 |                 |     |
|---------|-----|-----|-----|-----|-----|-----------------|-----------------|-----|
| 48      | GND | GND | GND | GND | GND | GND             | GND             | GND |
| 49      | GND | GND | GND | GND | GND | DAC228_T0_CH0_N | DAC228_T0_CH0_P | GND |
| 50      | GND | GND | GND | GND | GND | GND             | GND             | GND |

| J49 ADC |     |                 |                 |     |     |                 |                 |     |
|---------|-----|-----------------|-----------------|-----|-----|-----------------|-----------------|-----|
|         | A   | B               | C               | D   | E   | F               | G               | H   |
| 1       | GND | GND             | GND             | GND | GND | GND             | GND             | GND |
| 2       | GND | ADC227_T3_CH3_N | ADC227_T3_CH3_P | GND | GND | GND             | GND             | GND |
| 3       | GND | GND             | GND             | GND | GND | GND             | GND             | GND |
| 4       | GND | GND             | GND             | GND | GND | GND             | GND             | GND |
| 5       | GND | GND             | GND             | GND | GND | ADC227_T3_CH2_N | ADC227_T3_CH2_P | GND |
| 6       | GND | GND             | GND             | GND | GND | GND             | GND             | GND |
| 7       | GND | ADC227_T3_CH1_N | ADC227_T3_CH1_P | GND | GND | GND             | GND             | GND |
| 8       | GND | GND             | GND             | GND | GND | GND             | GND             | GND |
| 9       | GND | GND             | GND             | GND | GND | GND             | GND             | GND |
| 10      | GND | GND             | GND             | GND | GND | ADC227_T3_CH0_N | ADC227_T3_CH0_P | GND |
| 11      | GND | GND             | GND             | GND | GND | GND             | GND             | GND |
| 12      | GND | ADC226_T2_CH3_N | ADC226_T2_CH3_P | GND | GND | GND             | GND             | GND |
| 13      | GND | GND             | GND             | GND | GND | GND             | GND             | GND |
| 14      | GND | GND             | GND             | GND | GND | GND             | GND             | GND |
| 15      | GND | GND             | GND             | GND | GND | ADC226_T2_CH2_N | ADC226_T2_CH2_P | GND |
| 16      | GND | GND             | GND             | GND | GND | GND             | GND             | GND |
| 17      | GND | ADC226_T2_CH1_N | ADC226_T2_CH1_P | GND | GND | GND             | GND             | GND |
| 18      | GND | GND             | GND             | GND | GND | GND             | GND             | GND |
| 19      | GND | GND             | GND             | GND | GND | GND             | GND             | GND |
| 20      | GND | GND             | GND             | GND | GND | ADC226_T2_CH0_N | ADC226_T2_CH0_P | GND |
| 21      | GND | GND             | GND             | GND | GND | GND             | GND             | GND |
| 22      | GND | ADC225_T1_CH3_N | ADC225_T1_CH3_P | GND | GND | GND             | GND             | GND |
| 23      | GND | GND             | GND             | GND | GND | GND             | GND             | GND |
| 24      | GND | GND             | GND             | GND | GND | GND             | GND             | GND |
| 25      | GND | GND             | GND             | GND | GND | ADC225_T1_CH2_N | ADC225_T1_CH2_P | GND |
| 26      | GND | GND             | GND             | GND | GND | GND             | GND             | GND |
| 27      | GND | ADC225_T1_CH1_N | ADC225_T1_CH1_P | GND | GND | GND             | GND             | GND |

| J49 ADC |                     |                     |                     |                     |                     |                     |                     |                     |
|---------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|
| 28      | GND                 | GND                 | GND                 | GND                 | GND                 | GND                 | GND                 | GND                 |
| 29      | GND                 | GND                 | GND                 | GND                 | GND                 | GND                 | GND                 | GND                 |
| 30      | GND                 | GND                 | GND                 | GND                 | GND                 | ADC225_T1_CH0_N     | ADC225_T1_CH0_P     | GND                 |
| 31      | GND                 | GND                 | GND                 | GND                 | GND                 | GND                 | GND                 | GND                 |
| 32      | GND                 | ADC224_T0_CH3_N     | ADC224_T0_CH3_P     | GND                 | GND                 | GND                 | GND                 | GND                 |
| 33      | GND                 | GND                 | GND                 | GND                 | GND                 | GND                 | GND                 | GND                 |
| 34      | GND                 | GND                 | GND                 | GND                 | GND                 | GND                 | GND                 | GND                 |
| 35      | GND                 | GND                 | GND                 | GND                 | GND                 | ADC224_T0_CH2_N     | ADC224_T0_CH2_P     | GND                 |
| 36      | GND                 | GND                 | GND                 | GND                 | GND                 | GND                 | GND                 | GND                 |
| 37      | GND                 | ADC224_T0_CH1_N     | ADC224_T0_CH1_P     | GND                 | GND                 | GND                 | GND                 | GND                 |
| 38      | GND                 | GND                 | GND                 | GND                 | GND                 | GND                 | GND                 | GND                 |
| 39      | GND                 | GND                 | GND                 | GND                 | GND                 | GND                 | GND                 | GND                 |
| 40      | GND                 | GND                 | GND                 | GND                 | GND                 | ADC224_T0_CH0_N     | ADC224_T0_CH0_P     | GND                 |
| 41      | GND                 | GND                 | GND                 | GND                 | GND                 | GND                 | GND                 | GND                 |
| 42      | GND                 | VCM_ADC22_4_T0_CH23 | GND                 | VCM_ADC22_5_T1_CH23 | GND                 | VCM_ADC22_6_T2_CH23 | GND                 | VCM_ADC22_7_T3_CH23 |
| 43      | VCM_ADC22_4_T0_CH01 | GND                 | VCM_ADC22_5_T1_CH01 | GND                 | VCM_ADC22_6_T2_CH01 | GND                 | VCM_ADC22_7_T3_CH01 | GND                 |
| 44      | GND                 | 3V3                 | GND                 | 3V3                 | GND                 | 3V3                 | GND                 | 3V3                 |
| 45      | 3V3                 | GND                 | 3V3                 | GND                 | 3V3                 | GND                 | 3V3                 | GND                 |
| 46      | GND                 | ADCIO_02            | GND                 | ADCIO_06            | GND                 | ADCIO_10            | GND                 | ADCIO_14            |
| 47      | ADCIO_00            | GND                 | ADCIO_04            | GND                 | ADCIO_08            | GND                 | ADCIO_12            | GND                 |
| 48      | GND                 | ADCIO_03            | GND                 | ADCIO_07            | GND                 | ADCIO_11            | GND                 | ADCIO_15            |
| 49      | ADCIO_01            | GND                 | ADCIO_05            | GND                 | ADCIO_09            | GND                 | ADCIO_13            | GND                 |
| 50      | GND                 | I2C_SCL             | GND                 | I2C_SDA             | GND                 | ADCIO_VADJ          | GND                 | ADCIO_VADJ          |



# CoreHC2 Connector Pinout (XM655 Only)

Figure 27: ADC 16 Lanes

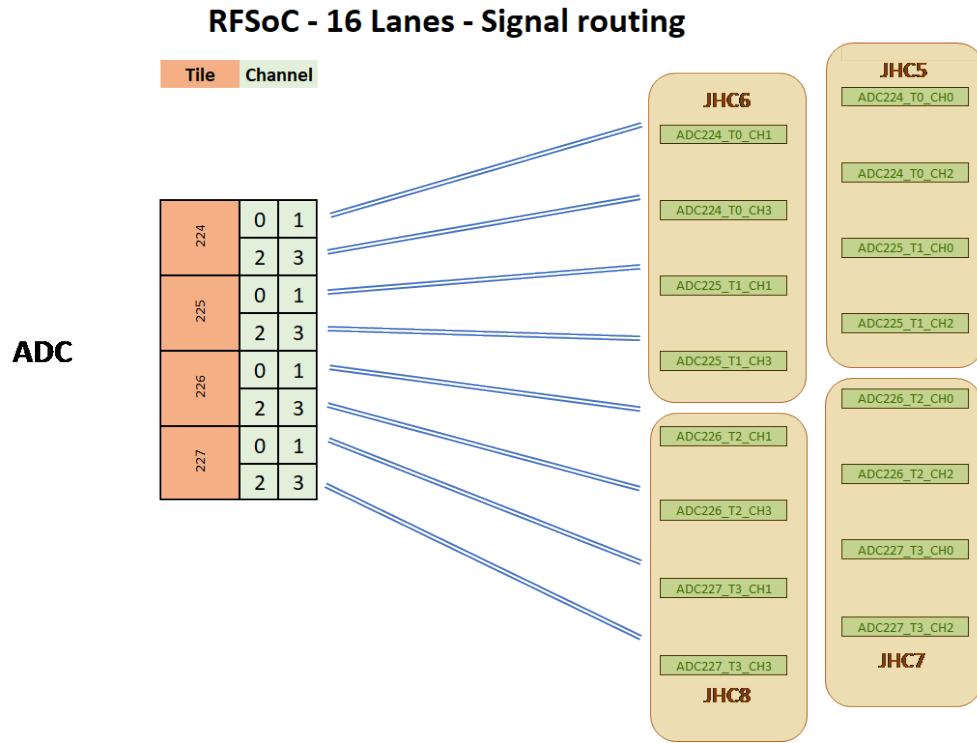
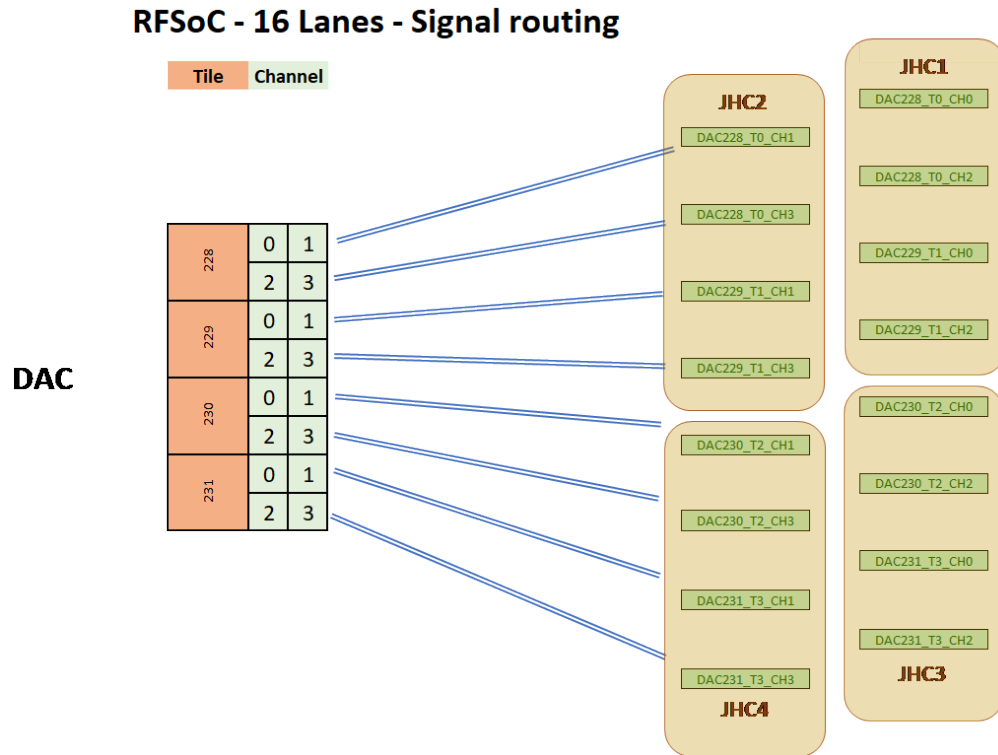


Figure 28: DAC 16 Lanes



## Features

- The XM655 balun add-on card uses the 8 x 50 x 2 female LPAM-50-01.0-L-08-2-K-TR connectors and pinout as defined in [XM650/655 Connector Pinout](#). For signal break-out Carlisle CoreHC2 connectors and cable assemblies are used. Digital IO and I2C are supported on headers.

Following are the features of XM655 module:

- 16 ADC differential signals to 4 male Carlisle CoreHC2 connector pads
- 16 DACs differential signals to 4 male Carlisle CoreHC2 connector pads
- 2 ADC inputs – compression mount SMAs through low frequency baluns – Minicircuits TCM2-33WX+
- 2 ADC inputs – compression mount SMAs through mid frequency baluns – Anaren BD1631J50100AHF
- 2 ADC inputs – compression mount SMAs through high frequency baluns – Anaren BD3150N50100AHF

- 2 ADC inputs - compression mount SMAs through high freq baluns – Anaren BD4859N50100AHF
- 2 DAC outputs compression mount SMAs through low frequency baluns – Minicircuits TCM2-33WX+
- 2 DAC outputs compression mount SMAs through mid frequency baluns – Anaren BD1631J50100AHF
- 2 DAC outputs compression mount SMAs through high frequency baluns – Anaren BD3150N50100AHF
- 2 DAC outputs - compression mount SMAs through high freq baluns – Anaren BD4859N50100AHF
- 20 DACIO digital I/O pins on a header strip
- 20 ADCIO digital I/O pins on a header strip
- 12V, 5V0, 3V3, VCCADJ DAC, VCCADJ\_ADC, DAV\_AVTT, and GND, I2C signals access on a header strip.

The XM650 balun add-on card demonstrations DAC to ADC loopback with a 16T16R configuration of N79 baluns and filters. There is no external connectivity to the ADC or DAC signals. Digital IO and I2C are supported on headers.

Following are the features of XM650 module:

- 16 DAC outputs looped back to 16 ADC inputs
- 32 N79 baluns and filters on the card
  - B46 or N77 band baluns can be supported with BOM change or re-work by customers.
- 20 DACIO digital I/O pins on a header strip
- 20 ADCIO digital I/O pins on a header strip

12V, 5V0, 3V3, VCCADJ DAC, VCCADJ\_ADC, DAV\_AVTT, and GND access on a header strip.

## Board Specifications

### Board Dimensions/Form Factor

When the module is mated with ZCU216 RFMC 2.0 connectors (Samtec LPAF-50-03.0-L-08-2-K-TR), the mated height between the boards will be 4.0 mm. No component is placed on the bottom side of the module.

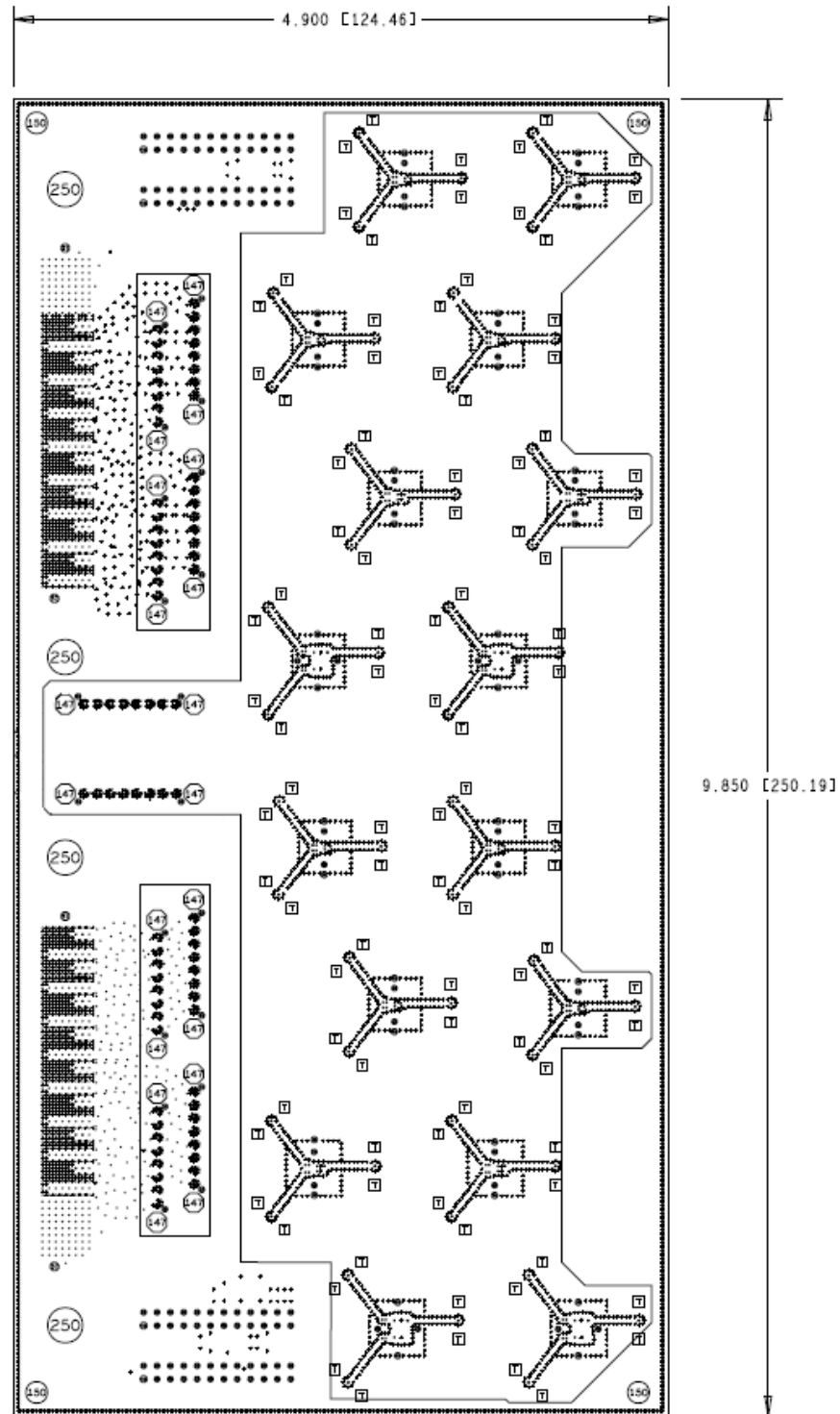
- **XM655 Dimensions:**

Length: 9.85" (250.19 mm)

Width: 4.90" (124.46 mm)

Thickness: 0.065" (1.651 mm)

Figure 29: XM655 Board Dimensions



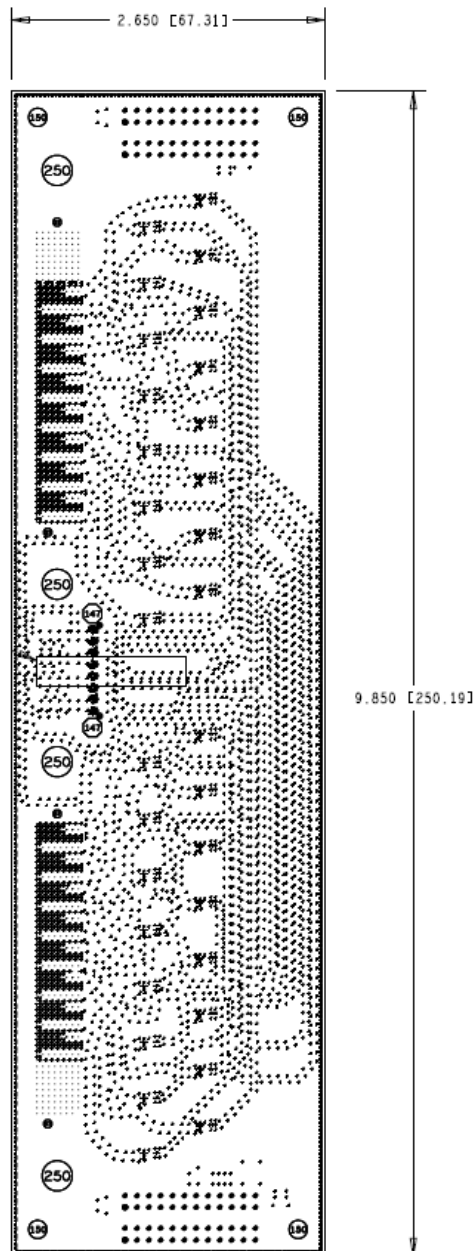
- **XM650 Dimensions:**

Length: 9.85" (250.19 mm)

Width: 2.65" (67.31 mm)

Thickness: 0.065" (1.651 mm)

*Figure 30: XM650 Board Dimensions*



## Mounting Holes/Keepouts

There are four Jack screws on the module and two edge standoff, as shown in the figure above. The boards are screwed to the ZCU216 board.

*Table 29: Mounting Screws and Standoff Details*

| Parameters           | Screw                                   | Standoff                   |
|----------------------|---|----------------------------|
| Part number          | JSO-0415-01                             | KEYSTONE 1894              |
| Length               | 4 mm board stack height                 | 0.625" + Rubber bumper     |
| Ordering Part Number | JSO-0415-01                             | 1894                       |
| Description          | Jack screw press-in standoff            | #4-40 0.625" ALUM STANDOFF |
| Data Sheet           | See the <a href="#">Samtec</a> website. | -                          |

## Functional Description

### Cables/SMAs

#### XM655

Cables: Carlisle Core HC2 8 Channel – Male, 3.5 mm TM40-0157-00

*Figure 31: Carlisle Core HC2 8 Channel–Male Cable*

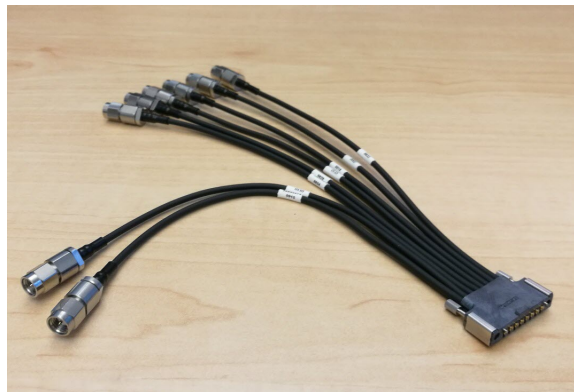
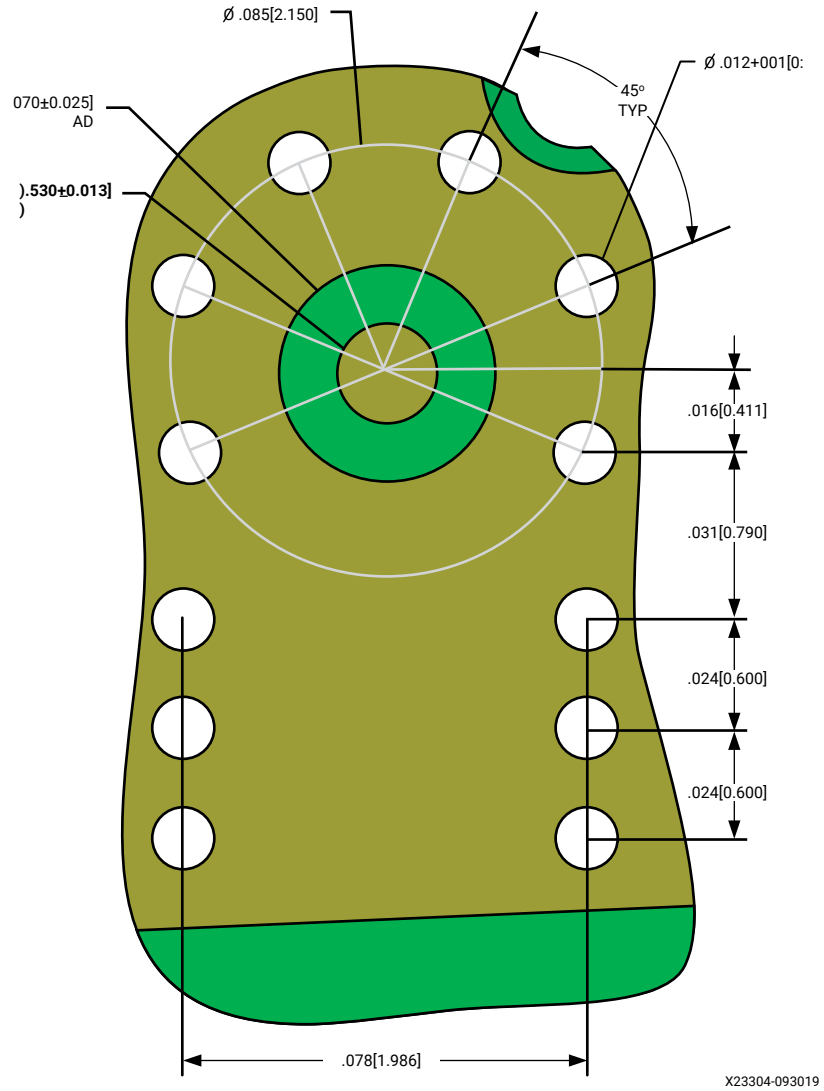


Figure 32: TM40-0157-00 Landing Pad



SMA: Carlisle Compression – Mount SMA, TMB-V5F2-1L1

Figure 33: TMB-V5F2-1L1 SMA Drawing

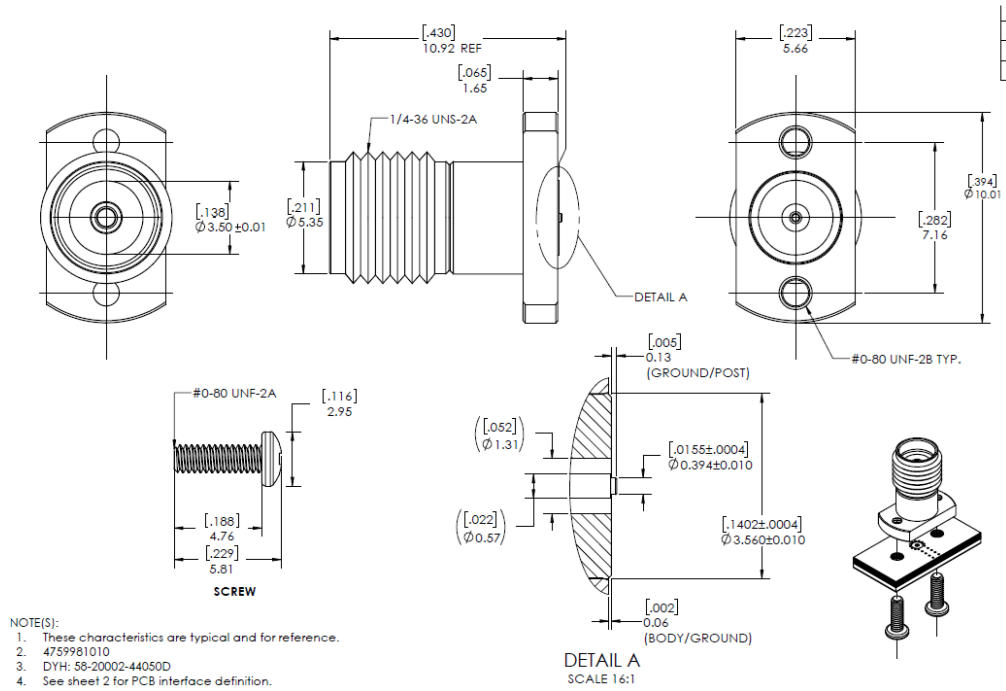


Figure 34: SMA to SMA Cable: Carlisle TM40-0159-00 6"





**XM650: No Cable or SMAs on Module**

## Balun/Filter

### XM655

#### Low Frequency Baluns

Table 30: Low Frequency Balun Part Number

| Parameter    | Value   |
|--------------|---|
| Part Number  | TCM2-33WX+                                    |
| Manufacturer | Minicircuits                                  |
| Order P/N    | TCM2-33WX+                                    |
| Vendor       | Minicircuits                                  |
| Description  | 10 to 3 GHz RF Transformer                    |
| Data Sheet   | See the <a href="#">Minicircuits</a> website. |

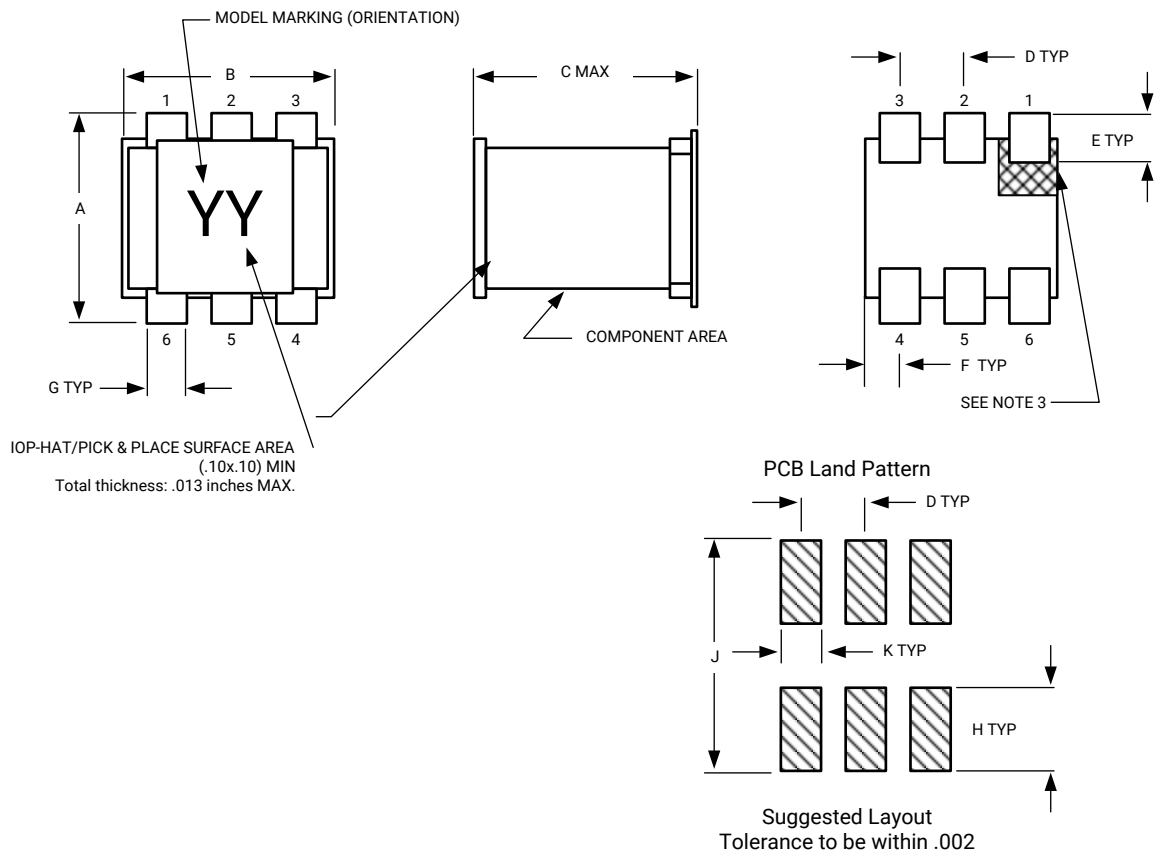
Figure 35: Low Frequency Balun Specifications

#### Electrical Specifications at 25°C

| Parameter                                  | Frequency (MHz) | Min. | Typ. | Max. | Unit   |
|--|-----------------|------|------|------|--------|
| <b>Impedance Ratio</b> (secondary/primary) |                 |      | 2    |      |        |
| <b>Frequency Range</b>                     |                 | 10   | —    | 3000 | MHz    |
| <b>Insertion Loss*</b>                     | 10 - 3000       | —    | 1.5  | 3.0  | dB     |
| <b>Amplitude Unbalance</b>                 | 10 - 3000       | —    | 0.7  | —    | dB     |
| <b>Phase Unbalance</b>                     | 10 - 3000       | —    | 4    | —    | Degree |

\*Insertion Loss is reference to mid-band loss, 0.8 dB typ.

Figure 36: Low Frequency Balun Drawing



X23306-093019

The following table lists the outline dimensions for the figure above.

Table 31: Outline Dimensions (mm)

| A     | B     | C     | D     | E     | F     | G     | H     | J     | K     | wt    |
|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| 0.160 | 0.150 | 0.160 | 0.050 | 0.040 | 0.025 | 0.028 | 0.065 | 0.190 | 0.030 | grams |
| 4.06  | 3.81  | 4.06  | 1.27  | 1.02  | 0.64  | 0.71  | 1.65  | 4.83  | 0.76  | 0.15  |

## Medium Frequency Baluns

Table 32: Medium Frequency Balun Part Number

| Parameter    | Value                             |
|--------------|-----------------------------------|
| Part Number  | BD1631J50100AHF                   |
| Manufacturer | Anaren                            |
| Order P/N    | 1173-1059-2-ND                    |
| Vendor       | Digikey                           |
| Description  | Balun 1.6 GHz-3.1 GHz 50/100 0805 |

Table 32: Medium Frequency Balun Part Number (cont'd)

| Parameter  | Value                                   |
|------------|---|
| Data Sheet | See the <a href="#">Anaren</a> website. |

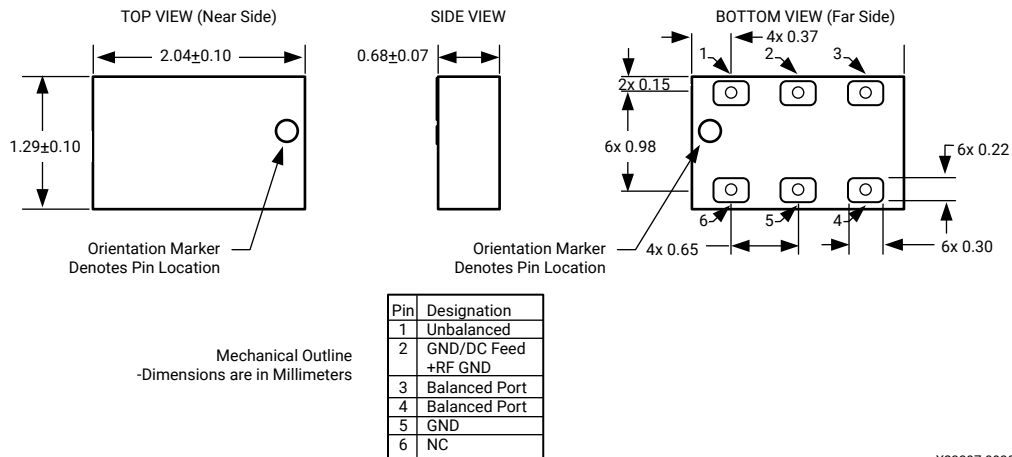
Figure 37: Medium Frequency Balun Specifications

**Detailed Electrical Specifications\*:** Specifications subject to change without notice.

| Features:                      | Parameter             | ROOM (25°C) |      |      |      |      |      | Unit    |
|--------------------------------|-----------------------|-------------|------|------|------|------|------|---------|
|                                |                       | Min.        | Typ. | Max  | Min. | Typ. | Max  |         |
| • 1.6 – 3.1 GHz                | Frequency             | 2.0         |      | 2.5  | 1.6  |      | 3.1  | GHz     |
| • 0.7mm Height Profile         | Unbalanced Port Imp.  |             | 50   |      |      | 50   |      | Ω       |
| • 50 Ohm to 2 x 50 Ohm         | Balanced Port Imp.**  |             | 100  |      |      | 100  |      | Ω       |
| • 802.11 b & g +n Compliant    | Return Loss           | 14          | 17   |      | 10   | 13   |      | dB      |
| • Low Insertion Loss           | Insertion Loss***     |             | 0.6  | 0.8  |      | 0.7  | 1.0  | dB      |
| • DCS, PCS & UMTS Compliant    | Amplitude Balance     |             | 0.15 | 0.6  |      | 0.7  | 1.0  | dB      |
| • Input to Output DC Isolation | Phase Balance         |             | 2.3  | 4.8  |      | 2.3  | 4.8  | Degrees |
| • Surface Mountable            | Power Handling @85C   |             |      | 0.8  |      |      | 0.8  | Watts   |
| • Tape & Reel                  | Power Handling @100C  |             |      | 0.55 |      |      | 0.55 | Watts   |
| • Non-conductive Surface       | Power Handling @105C  |             |      | 0.48 |      |      | 0.48 | Watts   |
| • RoHS Compliant               | Operating Temperature | -55         |      | +105 | -55  |      | +105 | °C      |
| • Halogen Free                 |                       |             |      |      |      |      |      |         |

\* Insertion Loss stated at room temperature (Insertion Loss is approximately 0.1 dB higher at +85 °C)

Figure 38: Medium Frequency Balun Drawing



X23307-093019

## High Frequency Baluns

### High Frequency Balun (4-5 GHz)

Table 33: High Frequency Balun (4-5 GHz) Part Number

| Parameter    | Value           |
|--------------|-----------------|
| Part Number  | BD3150N50100AHF |
| Manufacturer | Anaren          |
| Order P/N    | 1173-1069-2-ND  |

Table 33: High Frequency Balun (4-5 GHz) Part Number (cont'd)

| Parameter   | Value                                   |
|-------------|---|
| Vendor      | Digikey                                 |
| Description | Balun 3.1 GHz-5 GHz 50/100 0404         |
| Data Sheet  | See the <a href="#">Anaren</a> website. |

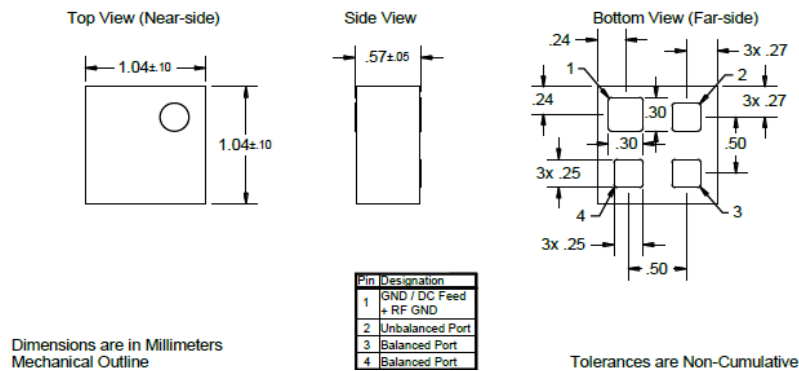
Figure 39: High Frequency Balun Specifications

**Detailed Electrical Specifications:** Specifications subject to change without notice.

| Features:  | Parameter                 | ROOM (25°C) |      |      |      |      |      | Unit    |
|--|---------------------------|-------------|------|------|------|------|------|---------|
|  |                           | Min.        | Typ. | Max  | Min. | Typ. | Max  |         |
| <ul style="list-style-type: none"> <li>• 3100 – 5000 MHz</li> <li>• 0.57mm Height Profile</li> <li>• 50 Ohm to 2 x 50 Ohm</li> <li>• Low Insertion Loss</li> <li>• UWB &amp; MMDS</li> <li>• Surface Mountable</li> <li>• Tape &amp; Reel</li> <li>• Non-conductive Surface</li> <li>• RoHS Compliant</li> <li>• Halogen Free</li> </ul> | Frequency                 | 3100        |      | 5000 | 5000 |      | 7000 | MHz     |
|  | Unbalanced Port Impedance |             | 50   |      |      | 50   |      | Ω       |
|  | Balanced Port Impedance   |             |      | 100  |      |      | 100  | Ω       |
|  | Return Loss               | 13          | 15   |      | 10   | 14   |      | dB      |
|  | Insertion Loss*           |             | 0.7  | 0.9  |      | 0.7  | 0.9  | dB      |
|  | Amplitude Balance         |             | 0.8  | 1.5  |      | 0.8  | 1.3  | dB      |
|  | Phase Balance             |             | 3    | 7    |      | 15   | 20   | Degrees |
|  | CMRR                      |             |      | 26   |      |      | 17   | dB      |
|  | Power Handling @85C       |             |      |      |      |      | 1.0  | Watts   |
|  | Power Handling @105C      |             |      |      |      |      | 0.6  | Watts   |
|  | Operating Temperature     |             | -55  |      | +105 | -55  |      | +105    |

\* Insertion Loss stated at room temperature (Insertion Loss is approximately 0.1 dB higher at +85 °C)

Figure 40: High Frequency Balun Drawing



### High Frequency Balun (5-6 GHz)

Table 34: High Frequency Balun (5-6 GHz) Part Number

| Parameter    | Value                                   |
|--------------|---|
| Part Number  | BD4859N50100AHF                         |
| Manufacturer | Anaren                                  |
| Order P/N    | 1173-1070-2-ND                          |
| Vendor       | Digikey                                 |
| Description  | BALUN 4.8 GHz-5.9 GHz 50/100 0404       |
| Data Sheet   | See the <a href="#">Anaren</a> website. |

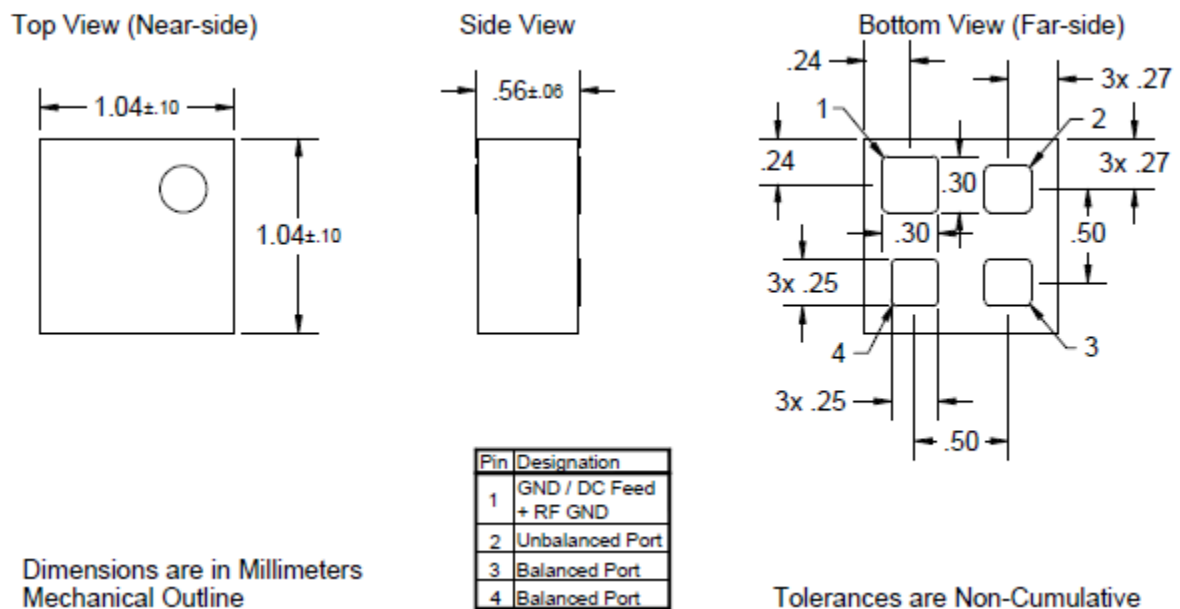
Figure 41: High Frequency Balun Specifications

**Detailed Electrical Specifications:** Specifications subject to change without notice.

| Features:   | Parameter                 | ROOM (25°C) |      |      | Unit    |
|---|---------------------------|-------------|------|------|---------|
|   |                           | Min.        | Typ. | Max  |         |
| <ul style="list-style-type: none"> <li>• 4800 – 5900 MHz</li> <li>• 0.57 mm Height Profile</li> <li>• 50 Ohm to 2 x 50 Ohm</li> <li>• Low Insertion Loss</li> <li>• 802.11a Uni-Band II &amp; III</li> <li>• Home Cordless Compliant</li> <li>• Surface Mountable</li> <li>• Tape &amp; Reel</li> <li>• Non-conductive Surface</li> <li>• RoHS Compliant</li> <li>• Halogen Free</li> </ul> | Frequency                 | 4800        |      | 5900 | MHz     |
|   | Unbalanced Port Impedance |             | 50   |      | Ω       |
|   | Balanced Port Impedance   |             | 100  |      | Ω       |
|   | Return Loss               | 14          | 20   |      | dB      |
|   | Insertion Loss*           |             | 0.6  | 0.8  | dB      |
|   | Amplitude Balance         |             | 0.9  | 1.5  | dB      |
|   | Phase Balance             |             | 3    | 8    | Degrees |
|   | CMRR                      |             | 26   |      | dB      |
|   | Power Handling            |             |      | 1    | Watts   |
|   | Operating Temperature     | -55         |      | +85  | °C      |

\* Insertion Loss stated at room temperature (Insertion Loss is approximately 0.1 dB higher at +85 °C)

Figure 42: High Frequency Balun Drawing



## RF Cages

Table 35: RF Cages

| Parameter    | Value  |
|--------------|--|
| Part Number  | LT-7925                                      |
| Manufacturer | Leader Tech                                  |
| Order P/N    | LT-7925                                      |
| Vendor       | Leader Tech                                  |
| Description  | EMI Cage                                     |
| Data Sheet   | See the <a href="#">Leader Tech</a> website. |

## XM650

### N79 Band Balun/Filter

Table 36: Band Pass Filter

| Parameter    | Value  |
|--------------|--|
| Part Number  | LFB184G70CT6F122TEMP                         |
| Manufacturer | Murata                                       |
| Order P/N    | LFB184G70CT6F122TEMP                         |
| Vendor       | Murata                                       |
| Description  | Band Pass Filter 4.4 GHz~5 GHz               |
| Data Sheet   | Refer to the <a href="#">Murata</a> website. |

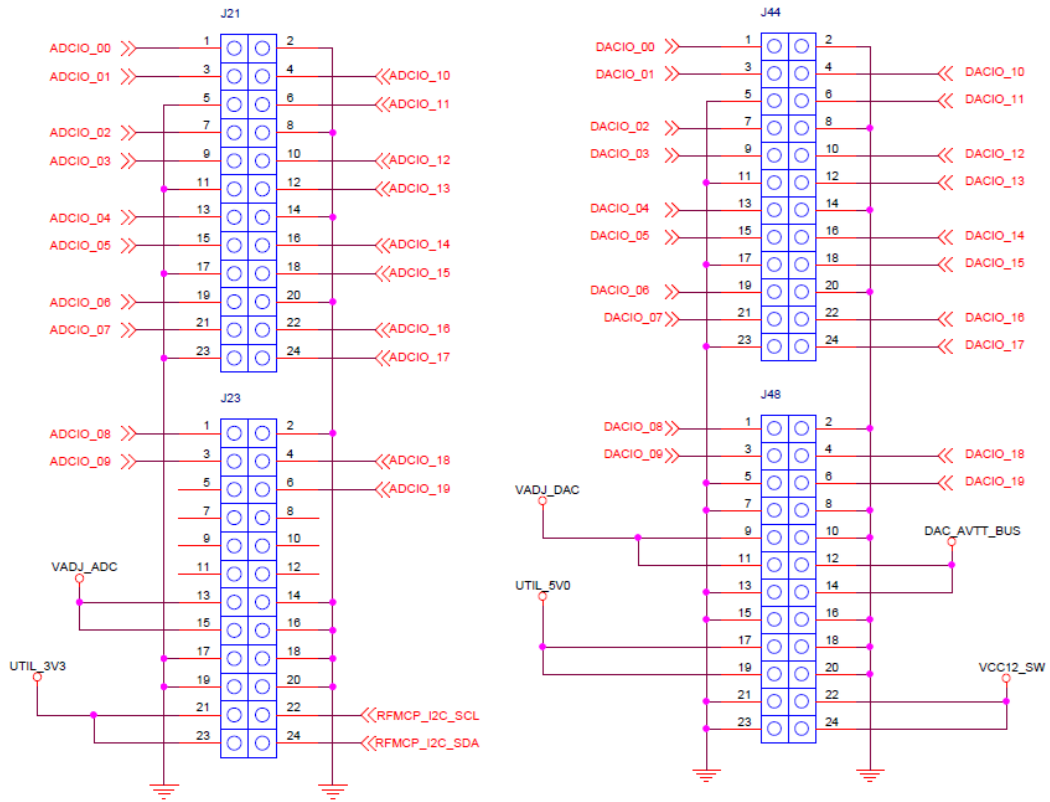
Table 37: N79 Balun

| Parameter    | Value  |
|--------------|--|
| Part Number  | LDB184G7BAAFA065TEMP                         |
| Manufacturer | Murata                                       |
| Order P/N    | LDB184G7BAAFA065TEMP                         |
| Vendor       | Murata                                       |
| Description  | Chip Multilayer Balun 4.4 GHz~5 GHz          |
| Data Sheet   | Refer to the <a href="#">Murata</a> website. |

## Header

There are a total of 20 DACIO and 20 ADCIO digital I/O pins on the header strips.

Figure 43: High ADCIO and DACIO Digital I/O Header Pins



# Regulatory and Compliance Information

This product is designed and tested to conform to the European Union directives and standards described in this section.

For Technical Support, open a [Support Service Request](#).

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## CE Information

### CE Directives

2006/95/EC, *Low Voltage Directive (LVD)*

2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*

### CE Standards

EN standards are maintained by the European Committee for Electrotechnical Standardization (CENELEC). IEC standards are maintained by the International Electrotechnical Commission (IEC).

### CE Electromagnetic Compatibility

EN 55022:2010, *Information Technology Equipment Radio Disturbance Characteristics – Limits and Methods of Measurement*

EN 55024:2010, *Information Technology Equipment Immunity Characteristics – Limits and Methods of Measurement*

This is a Class A product. In a domestic environment, this product can cause radio interference, in which case the user might be required to take adequate measures.

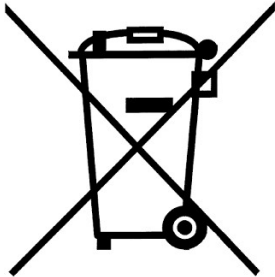
### CE Safety

IEC 60950-1:2005, *Information technology equipment – Safety, Part 1: General requirements*

EN 60950-1:2006, *Information technology equipment – Safety, Part 1: General requirements*



## Compliance Markings



In August of 2005, the European Union (EU) implemented the EU Waste Electrical and Electronic Equipment (WEEE) Directive 2002/96/EC and later the WEEE Recast Directive 2012/19/EU. These directives require Producers of electronic and electrical equipment (EEE) to manage and finance the collection, reuse, recycling and to appropriately treat WEEE that the Producer places on the EU market after August 13, 2005. The goal of this directive is to minimize the volume of electrical and electronic waste disposal and to encourage re-use and recycling at the end of life.

Xilinx has met its national obligations to the EU WEEE Directive by registering in those countries to which Xilinx is an importer. Xilinx has also elected to join WEEE Compliance Schemes in some countries to help manage customer returns at end-of-life.

If you have purchased Xilinx-branded electrical or electronic products in the EU and are intending to discard these products at the end of their useful life, please do not dispose of them with your other household or municipal waste. Xilinx has labeled its branded electronic products with the WEEE Symbol to alert our customers that products bearing this label should not be disposed of in a landfill or with municipal or household waste in the EU.

This product complies with Directive 2002/95/EC on the restriction of hazardous substances (RoHS) in electrical and electronic equipment.

This product complies with CE Directives 2006/95/EC, *Low Voltage Directive (LVD)* and 2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*.

# Additional Resources and Legal Notices

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## Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see [Xilinx Support](#).

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## Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator (DocNav) provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the Vivado® IDE, select **Help** → **Documentation and Tutorials**.
- On Windows, select **Start** → **All Programs** → **Xilinx Design Tools** → **DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.
- On the Xilinx website, see the [Design Hubs](#) page.

**Note:** For more information on DocNav, see the [Documentation Navigator](#) page on the Xilinx website.

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## References

ZCU216 Evaluation Kit—[Master Answer Record 72741](#)

These documents provide supplemental material useful with this guide:

1. [Zynq UltraScale+ RFSoc Data Sheet: Overview \(DS889\)](#)
2. [Zynq UltraScale+ RFSoc Data Sheet: DC and AC Switching Characteristics \(DS926\)](#)
3. [Zynq UltraScale+ Device Technical Reference Manual \(UG1085\)](#)
4. [UltraScale Architecture PCB Design User Guide \(UG583\)](#)
5. [UltraScale Architecture-Based FPGAs Memory IP LogiCORE IP Product Guide \(PG150\)](#)
6. [UltraScale Architecture GTY Transceivers User Guide \(UG578\)](#)
7. [Vivado Design Suite User Guide: Using Constraints \(UG903\)](#)
8. [Tera Term Terminal Emulator Installation Guide \(UG1036\)](#)
9. [UltraScale Architecture System Monitor User Guide \(UG580\)](#)
10. ZCU216 System Controller Tutorial (XTP\_TBD)
11. ZCU216 Software Install and Board Setup Tutorial (XTP\_TBD)
12. [Micron Technology](#) (MTA4ATF51264HZ-2G6E1, MT40A512M16JY-075E, MT25QU02GCBB8E12-OSIT data sheets)
13. [Standard Microsystems Corporation \(SMSC\)](#) (USB3320 data sheet)
14. [SanDisk Corporation](#)
15. [SD Association](#)
16. [Silicon Labs](#) (SI570, SI5341B, SI5382A)
17. [Texas Instruments](#) (TCA9548A, PCA9544A, TCA6416A, DP83867, MSP430FS342)
18. [PCI-SIG](#)
19. [Samtec, Inc.](#) (SEAF, LPAF series connectors)
20. [VITA FMC Marketing Alliance](#) (FPGA Mezzanine Card (FMC) VITA 57.1, 57.4 specifications)
21. [Maxim Integrated Circuits](#) (MAX16025TE+, MAX6643)
22. [Infineon Integrated Circuits](#) (IR35215, IRPS5401, IR38164, IR3889, IR3897)
23. [Monolithic Power Systems](#) (MPM3683, MPM3833)
24. [Future Technology Devices International Ltd.](#) (FT4232HL)
25. [Digilent](#) (Pmod peripheral modules)
26. [SNIA Technology Affiliates](#) (SFF-8402, SFF-8432)
27. [Nexperia/NXP Semiconductors](#) (IP4856CX25, SC18IS602)

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