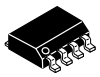
Fixed Frequency Current Mode Controller for Flyback Converters

NCP12400



SOIC−7
CASE 751U

The NCP12400 is a new fixed−frequency current−mode controller featuring the Dynamic Self−Supply. This function greatly simplifies the design of the auxiliary supply and the V_{CC} capacitor by activating the internal startup current source to supply the controller during start−up, transients, latch, stand−by etc. This device contains a special HV detector which detects the application unplug from the ac input line and triggers the X2 discharge current. This HV structure allows the brown−out detection as well.

It features a timer−based fault detection that ensures the detection of overload and an adjustable compensation to help keep the maximum power independent of the input voltage.

Due to frequency foldback, the controller exhibits excellent efficiency in light load condition while still achieving very low standby power consumption. Internal frequency jittering, ramp compensation, and a versatile latch input make this controller an excellent candidate for the robust power supply designs.

A dedicated Off Mode allows to reach the extremely low no load input power consumption via “sleeping” whole device and thus minimize the power consumption of the control circuitry.

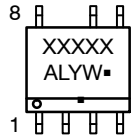
Features

- Fixed−Frequency Current−Mode Operation 65 kHz or 100 kHz Frequency Options
- Frequency Foldback then Skip Mode for Maximized Performance in Light Load and Standby Conditions
- Timer−Based Overload Protection with Latched (Option A) or Autorecovery (Option B) Operation
- High−Voltage Current Source with Brown−Out Detection and Dynamic Self−Supply, Simplifying the Design of the V_{CC} Circuitry
- Frequency Modulation for Softened EMI Signature
- Adjustable Overpower Protection Dependant on the Mains Voltage
- Fault Input for Overvoltage and Over Temperature Protection
- V_{CC} Operation up to 28 V, with Overvoltage Detection
- 300/500 mA Source/Sink Drive Peak Current Capability
- 4/10 ms Soft−Start
- Internal Thermal Shutdown
- No−Load Standby Power < 30 mW
- X2 Capacitor in EMI Filter Discharging Feature
- These are Pb−Free Devices

Typical Applications

- Offline Adapters for Notebooks, LCD, and Printers
- Offline Battery Chargers
- Consumer Electronic Power Supplies
- Auxiliary/Housekeeping Power Supplies
- Offline Adapters for Notebooks

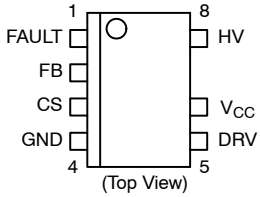
MARKING DIAGRAM



400VWXYZf = Specific Device Code (see page 2)
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 44 of this data sheet.

TYPICAL APPLICATION SCHEMATIC

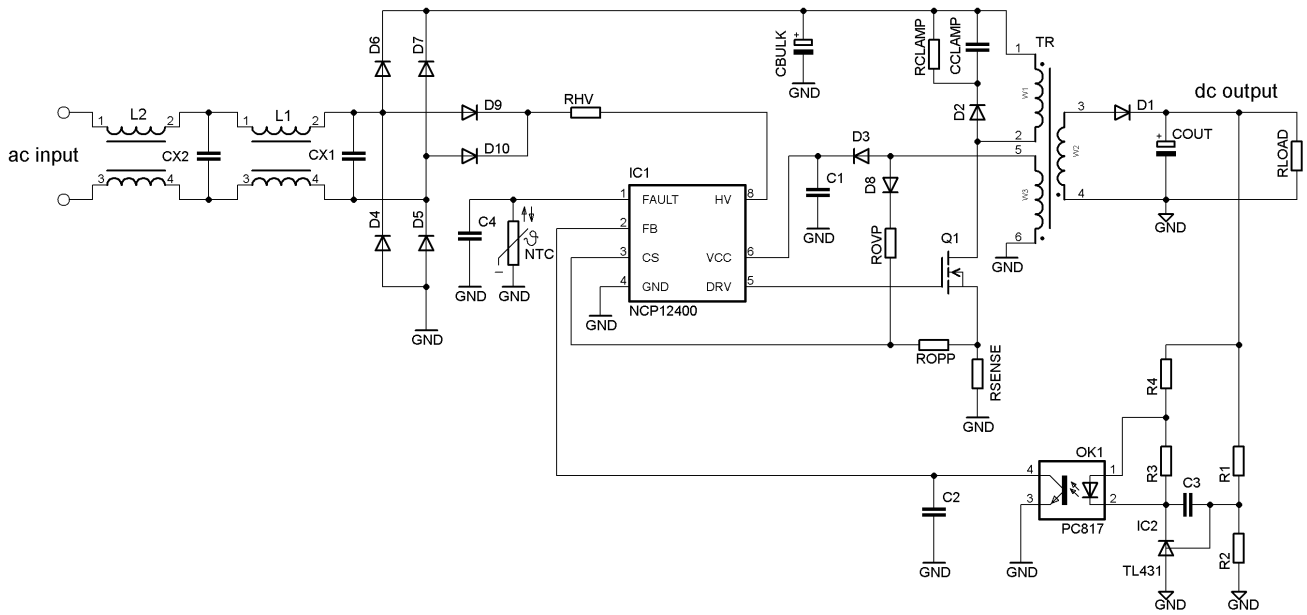


Figure 1. Flyback Converter Application using the NCP12400

Table 1. OPTIONS

Part	OPN	Brown Out Start – Stop	OCP Fault	Frozen Current Setpoint	Quiet skip	Soft Start	Frequency	OTP/OVP
NCP12400	NCP12400BAHAB0DR2G	103 – 100 V	Latched	300 mV	No, min. 3 pulses only	4 ms	65 kHz	Latched
	NCP12400BAHBB0DR2G	111 – 103 V	Latched	300 mV	Yes, min. 3 pulses, 800 Hz burst	4 ms	65 kHz	Latched
	NCP12400BBBBB2DR2G	111 – 103 V	Autorecovery	150 mV	Yes, min. 3 pulses, 800 Hz burst	4 ms	65 → 100 kHz	Latched
	NCP12400BBHAA1DR2G	111 – 103 V	Autorecovery	300 mV	No, min. 3 pulses only	10 ms	100 kHz	Autorecovery
	NCP12400CAHAB0DR2G	95 – 93 V	Latched	300 mV	No, min. 3 pulses only	4 ms	65 kHz	Latched
	NCP12400CBAAB0DR2G	95 – 93 V	Autorecovery	No	No, min. 3 pulses only	4 ms	65 kHz	Latched
	NCP12400CBBAB0DR2G	95 – 93 V	Autorecovery	150 mV	No, min. 3 pulses only	4 ms	65 kHz	Latched
	NCP12400CBHAA0DR2G	95 – 93 V	Autorecovery	300 mV	No, min. 3 pulses only	10 ms	65 kHz	Autorecovery
	NCP12400EAHBB0DR2G	Brown In, No BO	Latched	300 mV	Yes, min. 3 pulses, 800 Hz burst	4 ms	65 kHz	Latched
	NCP12400BBBBA0DR2G	111 – 103 V	Autorecovery	150 mV	Yes, min. 3 pulses, 800 Hz burst	10 ms	65 kHz	Latched
	NCP12400BBHAB0DR2G	111 – 103 V	Autorecovery	300 mV	No, min. 3 pulses only	4 ms	65 kHz	Latched
	NCP12400BBEBA0DR2G	111 – 103 V	Autorecovery	210 mV	Yes, min. 3 pulses, 800 Hz burst	10 ms	65 kHz	Latched
	NCP12400BBAAA0DR2G	111 – 103 V	Autorecovery	No	No	10 ms	65 kHz	Latched

Table 2. SPECIFIC DEVICE CODE KEY

400	V	W	X	Y	Z	f
Part	BO	OCP Fault	Frozen Current Setpoint	Quiet Skip	Soft Start	Frequency
	A – 229–211 V B – 111–103 V C – 95–93 V D – No BO E – Brown In, no BO	A – Latched B – Autorecovery	A –No B – 150 mV C – 170 mV D – 190 mV E – 210 mV F – 230 mV G – 250 mV H – 300 mV	A – No, min. 3 pulses B – Yes, min. 3 pulses, 800 Hz burst	A – 10 ms B – 4 ms	0 – 65 kHz 1 – 100 kHz 2 – 65 → 100 kHz

Table 3. PIN FUNCTION DESCRIPTION

Pin #	Pin Name	Function	Pin Description
1	FAULT	FAULT Input	Pull the pin up or down to stop the controller. An internal current source allows the direct connection of an NTC for over temperature detection. Device can restart in autorecovery mode or can be latched depending on the option.
2	FB	Feedback + Shutdown Pin	An optocoupler connected to ground controls the output regulation. The part goes to the low consumption Off mode if the FB input pin is pulled to GND.
3	CS	Current Sense	This input senses the primary current for current−mode operation, and offers an overpower compensation adjustment. This pin implements over voltage protection as well.
4	GND		The controller ground.
5	DRV	Drive Output	Drives external MOSFET.
6	V_{CC}	V_{CC} Input	This supply pin accepts up to 28 Vdc, with overvoltage detection. The pin is connected to an external auxiliary voltage.
8	HV	High−Voltage Pin	Connects to the rectified ac line to perform the functions of start−up current source, Self−Supply, brown−out detection and X2 capacitor discharge function and the HV sensing for the overpower protection purposes. **It is not allowed to connect this pin to a dc voltage.**

SIMPLIFIED INTERNAL BLOCK SCHEMATIC

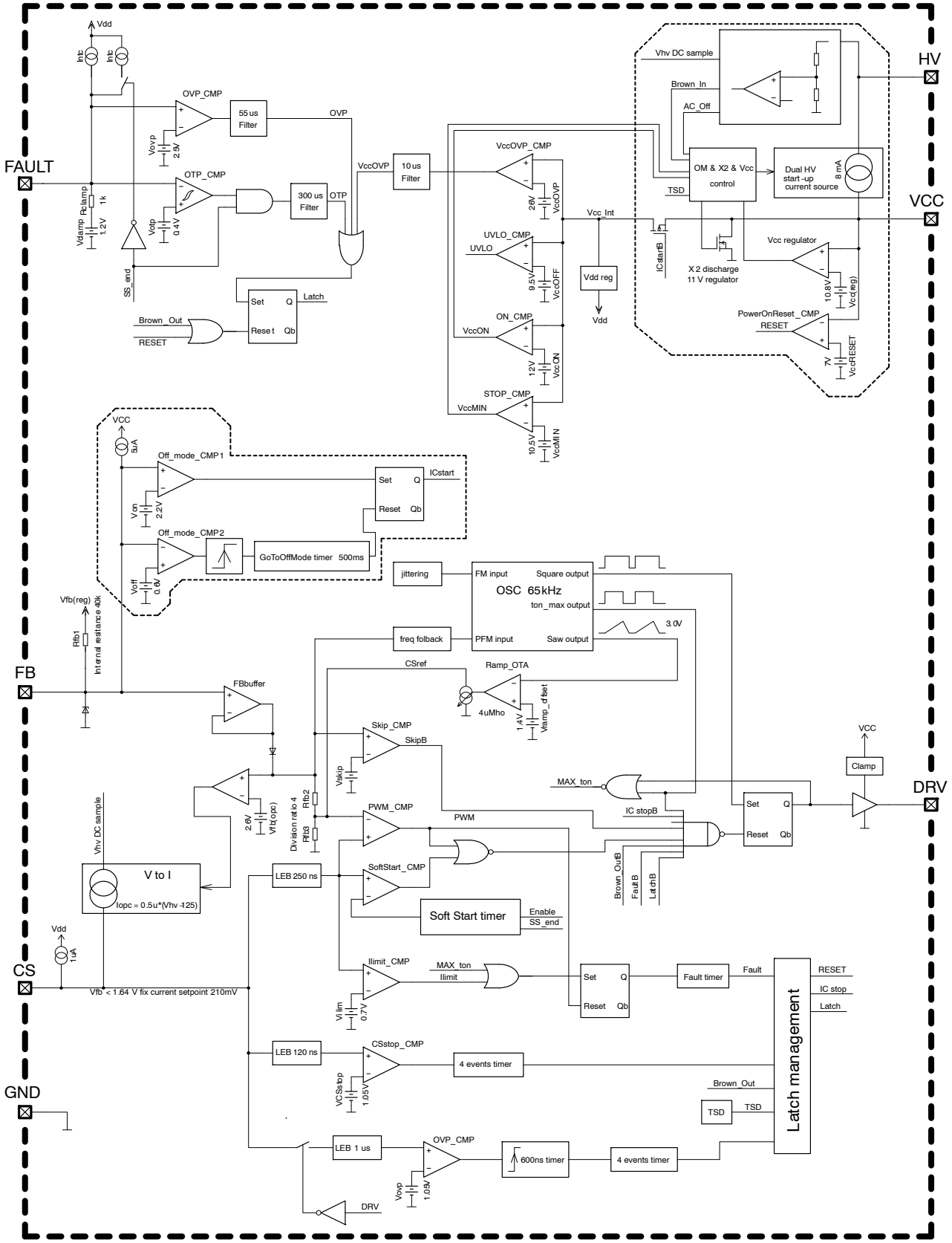


Figure 2. Simplified Internal Block Schematic

Table 4. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DRV (pin 5)	Maximum voltage on DRV pin (Dc−Current self−limited if operated within the allowed range) (Note 2)	−0.3 to 20 ±1000 (peak)	V mA
V_{CC} (pin 6)	V_{CC}Power Supply voltage, V_{CC} pin, continuous voltage Power Supply voltage, V_{CC} pin, continuous voltage (Note 2)	−0.3 to 36 ±30 (peak)	V mA
HV (pin 8)	Maximum voltage on HV pin (Dc−Current self−limited if operated within the allowed range)	−0.3 to 750 ±20	V mA
V_{max}	Maximum voltage on low power pins (except pin 5, pin 6 and pin 8) (Dc−Current self−limited if operated within the allowed range) (Note 2)	−0.3 to 5.5 ±10 (peak)	V mA
$R_{\theta J-A}$	Thermal Resistance SOIC−7 Junction-to-Air, low conductivity PCB (Note 3) Junction-to-Air, medium conductivity PCB (Note 4) Junction-to-Air, high conductivity PCB (Note 5)	 162 147 115	°C/W
$R_{\theta J-C}$	Thermal Resistance Junction−to−Case	73	°C/W
T_{JMAX}	Operating Junction Temperature	−40 to +150	°C
$T_{STRGMAX}$	Storage Temperature Range	−60 to +150	°C
	ESD Capability, HBM model (All pins except HV) (Note 1)	> 4000	V
	ESD Capability, HBM model (pin 8, HV)	> 2000	V
	ESD Capability, Charge Discharge Model (Note 1)	> 500	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model 4000 V per JEDEC standard JESD22, Method A114E
   Charge Discharge Model Method 500 V per JEDEC standard JESD22, Method C101E
2. This device contains latch-up protection and exceeds 100 mA per JEDEC Standard JESD78.
3. As mounted on a 80 x 100 x 1.5 mm FR4 substrate with a single layer of 50 mm^2 of 2 oz copper traces and heat spreading area. As specified for a JEDEC 51-1 conductivity test PCB. Test conditions were under natural convection or zero air flow.
4. As mounted on a 80 x 100 x 1.5 mm FR4 substrate with a single layer of 100 mm^2 of 2 oz copper traces and heat spreading area. As specified for a JEDEC 51-2 conductivity test PCB. Test conditions were under natural convection or zero air flow.
5. As mounted on a 80 x 100 x 1.5 mm FR4 substrate with a single layer of 650 mm^2 of 2 oz copper traces and heat spreading area. As specified for a JEDEC 51-3 conductivity test PCB. Test conditions were under natural convection or zero air flow.

Table 5. ELECTRICAL CHARACTERISTICS
(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{HV} = 125 V, V_{CC} = 11 V unless otherwise noted)

Characteristics	Test Condition	Symbol	Min	Typ	Max	Unit
HIGH VOLTAGE CURRENT SOURCE						
Minimum voltage for current source operation		$V_{HV(min)}$	−	30	40	V
Current flowing out of V_{CC} pin	V_{CC} = 0 V V_{CC} = $V_{CC(on)}$ − 0.5 V	I_{start1} I_{start2}	0.2 5	0.5 8	0.8 11	mA
Off−state leakage current	V_{HV} = 750 V, V_{CC} = 15 V	$I_{start(off)}$	−	2	6	μA
SUPPLY						
Turn−on threshold level, V_{CC} going up HV current source stop threshold (depending on the version)		$V_{CC(on)}$	11.0 15.0	12.0 16.2	13.0 17.5	V
HV current source restart threshold		$V_{CC(min)}$	9.5	10.5	11.5	V
Turn−off threshold		$V_{CC(off)}$	8.4	8.9	9.3	V
Overvoltage threshold Overvoltage threshold (option EAHBB, BBBBB)		$V_{CC(ovp)}$	25 30	26.5 32	28 34	V
Blanking duration on $V_{CC(off)}$ and $V_{CC(ovp)}$ detection		$t_{VCC(blank)}$	−	10	−	μs

6. Guaranteed by design.
7. CS pin source current is a sum of I_{bias} and I_{OPC}, thus at V_{HV} = 125 V is observed the I_{bias} only, because I_{OPC} is switched off.

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(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{HV} = 125 V, V_{CC} = 11 V unless otherwise noted)

Characteristics	Test Condition	Symbol	Min	Typ	Max	Unit
SUPPLY						
V_{CC} decreasing level at which the internal logic resets		$V_{CC(reset)}$	4.8	7.0	7.7	V
V_{CC} level for I_{START1} to I_{START2} transition		$V_{CC(inhibit)}$	1.0	2.1	3.0	V
Internal current consumption	DRV open, V_{FB} = 3 V, 65 kHz DRV open, V_{FB} = 3 V, 100 kHz	I_{CC1}	1.0 1.1	1.3 1.4	2.0 2.1	mA mA
	Cdrv = 1 nF, V_{FB} = 3 V, 65 kHz Cdrv = 1 nF, V_{FB} = 3 V, 100 kHz	I_{CC2}	1.5 2.0	2.1 2.6	2.9 3.4	mA mA
	Skip or before start−up	I_{CC3}	400	500	650	μA
	Fault mode (fault or latch)	I_{CC4}	300	430	550	μA
	Off−mode	I_{CC5}	−	25	−	μA
BROWN−OUT						
Brown−out thresholds (option A)	V_{HV} going up V_{HV} going down	$V_{HV(start)}$ $V_{HV(stop)}$	210 194	229 211	248 228	V
Brown−out thresholds (option B)	V_{HV} going up V_{HV} going down	$V_{HV(start)}$ $V_{HV(stop)}$	102 94	111 103	120 116	V
Brown−out thresholds (option BAHAB)	V_{HV} going up V_{HV} going down	$V_{HV(start)}$ $V_{HV(stop)}$	93 90	103 100	113 110	V
Brown−out thresholds (option C)	V_{HV} going up V_{HV} going down	$V_{HV(start)}$ $V_{HV(stop)}$	87 85	95 93	103 101	V
Brown−out thresholds (option E)	V_{HV} going up	$V_{HV(start)}$	90	100	110	V
Timer duration for line cycle drop−out (depending on the version)		t_{HV}	42 48	64 73	86 98	ms
X2 DISCHARGE						
Comparator hysteresis observed at HV pin		$V_{HV(hyst)}$	2.0	3.0	4.0	V
HV signal sampling period		t_{sample}	−	1.0	−	ms
Timer duration for no line detection		t_{DET}	21	32	43	ms
Discharge timer duration		t_{DIS}	21	32	43	ms
Shunt regulator voltage at VCC pin during X2 discharge event		$V_{CC(dis)}$	10.0	11.0	12.0	V
OSCILLATOR						
Oscillator frequency 65 kHz version Oscillator frequency 100 kHz version		f_{OSC}	61 94	65 100	69 110	kHz
Maximum duty−ratio (corresponding to maximum on time at maximum switching frequency)		D_{MAX}	75	80	85	%
Frequency jittering amplitude, in percentage of F_{OSC}		A_{jitter}	±3.0	±4.0	±5.0	kHz
Frequency jittering modulation frequency		F_{jitter}	85	125	165	Hz
FREQUENCY FOLDBACK						
Feedback voltage threshold below which frequency foldback starts	T_J = 25°C	$V_{FB(foldS)}$	2.4	2.5	2.6	V
Feedback voltage threshold below which frequency foldback is complete	T_J = 25°C	$V_{FB(foldE)}$	2.05	2.15	2.25	V
Minimum switching frequency	$V_{FB} = V_{skip(in)} + 0.1$	$f_{OSC(min)}$	25	28	31	kHz

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7. CS pin source current is a sum of I_{bias} and I_{OPC}, thus at V_{HV} = 125 V is observed the I_{bias} only, because I_{OPC} is switched off.

Table 5. ELECTRICAL CHARACTERISTICS
(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{HV} = 125 V, V_{CC} = 11 V unless otherwise noted)

Characteristics	Test Condition	Symbol	Min	Typ	Max	Unit
OUTPUT DRIVER						
Rise time, 10 to 90% of V_{CC}	V_{CC} = $V_{CC(off)}$ + 0.2 V, C_{DRV} = 1 nF	t_{rise}	–	40	70	ns
Fall time, 90 to 10% of V_{CC}	V_{CC} = $V_{CC(off)}$ + 0.2 V, C_{DRV} = 1 nF	t_{fall}	–	30	60	ns
Current capability	V_{CC} = $V_{CC(off)}$ + 0.2 V, C_{DRV} = 1 nF DRV high, V_{DRV} = 0 V DRV low, V_{DRV} = V_{CC}	 $I_{DRV(source)}$ $I_{DRV(sink)}$	 – –	 300 500	 – –	mA
Clamping voltage (maximum gate voltage)	V_{CC} = $V_{CC(ovp)}$ − 0.2 V, DRV high, R_{DRV} = 33 kΩ, C_{load} = 220 pF	$V_{DRV(clamp)}$	10	12	14	V
High−state voltage drop	V_{CC} = $V_{CC(min)}$ + 0.2 V, R_{DRV} = 33 kΩ, DRV high	$V_{DRV(drop)}$	–	–	1	V
CURRENT SENSE						
Input Pull−up Current	V_{CS} = 0.7 V	I_{bias}	–	1	–	μA
Maximum internal current setpoint	V_{FB} > 3.5 V	V_{ILIM}	0.66	0.70	0.74	V
Propagation delay from V_{Ilimit} detection to DRV off	V_{CS} = V_{ILIM}	t_{delay}	–	50	70	ns
Leading Edge Blanking Duration for V_{ILIM}		t_{LEB}	180	250	320	ns
Threshold for immediate fault protection activation		$V_{CS(stop)}$	0.95	1.05	1.15	V
Leading Edge Blanking Duration for $V_{CS(stop)}$ (Note 6)		t_{BCS}	75	120	150	ns
Soft−start duration (option A) Soft−start duration (option B)	From 1st pulse to V_{CS} = V_{ILIM}	t_{SSTART}	– 3.2	10 4.0	13 4.8	ms
Frozen current setpoint (option B) Frozen current setpoint (option D) Frozen current setpoint (option E) Frozen current setpoint (option H)		$V_{I(freeze)}$	100 140 145 250	150 190 210 300	200 240 270 350	mV
Over voltage protection threshold when DRV is low	V_{CS} going up	$V_{OVP(CS)}$	1.00	1.05	1.10	V
Blanking duration on OVP detection		$t_{OVP,CS}$	0.7	1.0	1.3	μs
Delay time constant before OTP confirmation		$t_{OVP,del}$	–	600	–	ns
INTERNAL SLOPE COMPENSATION						
Slope of the compensation ramp		$S_{comp(65kHz)}$ $S_{comp(100kHz)}$	– –	−32.5 −50	– –	mV / μs
FEEDBACK						
Internal pull−up resistor	T_J = 25°C	$R_{FB(up)}$	30	40	50	kΩ
V_{FB} to internal current setpoint division ratio (Note 6)		K_{FB}	–	4	–	–
Internal pull−up voltage on the FB pin		$V_{FB(ref)}$	4.5	5	5.5	V
Offset between FB pin and internal FB divider	T_J = 25°C	$V_{FB(off)}$	–	0.8	–	V
SKIP CYCLE MODE						
Feedback voltage thresholds for skip mode	V_{FB} going down, T_J = 25°C V_{FB} going up, T_J = 25°C	$V_{skip(in)}$ $V_{skip(out)}$	0.9 1.05	1.0 1.15	1.1 1.25	V
Minimum number of pulses in burst		$n_{P,skip}$	3	–	–	
Skip out delay		t_{skip}	–	–	38	μs

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Table 5. ELECTRICAL CHARACTERISTICS
(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{HV} = 125 V, V_{CC} = 11 V unless otherwise noted)

Characteristics	Test Condition	Symbol	Min	Typ	Max	Unit
REMOTE CONTROL ON FB PIN						
The voltage above which the part enters the on mode	$V_{CC} > V_{CC(off)}$, V_{HV} = 60 V	V_{ON}	–	2.2	–	V
The voltage below which the part enters the off mode	$V_{CC} > V_{CC(off)}$	V_{OFF}	0.5	0.6	0.7	V
Minimum hysteresis between the V_{ON} and V_{OFF}	$V_{CC} > V_{CC(off)}$, V_{HV} = 60 V	V_{HYST}	500	–	–	mV
Pull−up current in off mode	$V_{CC} > V_{CC(off)}$	I_{OFF}	–	5	–	μA
Go To Off mode timer	$V_{CC} > V_{CC(off)}$	t_{GTOM}	400	500	600	ms
OVERLOAD PROTECTION						
Fault timer duration		t_{fault}	108	128	178	ms
Fault timer reset time	V_{CS} < 0.7 V, D < 90% D_{MAX}	$t_{fault,res}$	150	200	250	μs
Autorecovery mode latch−off time duration		$t_{autorec}$	0.85	1.00	1.35	s
OVERPOWER PROTECTION						
V_{HV} to I_{OPC} conversion ratio		K_{OPC}	–	0.54	–	μA / V
Current flowing out of CS pin (Note 7)	V_{HV} = 125 V V_{HV} = 162 V V_{HV} = 325 V V_{HV} = 365 V	$I_{OPC(125)}$ $I_{OPC(162)}$ $I_{OPC(325)}$ $I_{OPC(365)}$	– – – 105	0 20 110 130	– – – 150	μA
FB voltage above which I_{OPC} is applied	V_{HV} = 365 V	$V_{FB(OPCF)}$	–	2.6	–	V
FB voltage below which is no I_{OPC} applied	V_{HV} = 365 V	$V_{FB(OPCE)}$	–	1.6	–	V
FAULT INPUT						
High threshold	V_{Latch} going up	V_{OVP}	2.43	2.50	2.57	V
Low threshold	V_{Latch} going down, T_J = 25°C	V_{OTP}	0.380	0.400	0.420	V
OTP resistance threshold (T_J = 25°C)	External NTC resistance is going down	R_{OTP}	7.6	8.0	8.5	kΩ
OTP resistance threshold (T_J = 80°C)	External NTC resistance is going down	R_{OTP}	–	8.5	–	kΩ
OTP resistance threshold (T_J = 110°C)	External NTC resistance is going down	R_{OTP}	–	9.5	–	kΩ
Current source for direct NTC connection During normal operation During soft−start	V_{Latch} = 0.2 V	 I_{NTC} $I_{NTC(SSTART)}$	 30 60	 50 100	 70 140	μA
Current source for direct NTC connection During normal operation	V_{Latch} = 0.2 V, T_J = 25°C	I_{NTC}	47	50	53	μA
Blanking duration on high latch detection		$t_{Latch(OVP)}$	35	50	70	μs
Blanking duration on low latch detection		$t_{Latch(OTP)}$	–	350	–	μs
Clamping voltage	I_{Latch} = 0 mA I_{Latch} = 1 mA	$V_{clamp0(Latch)}$ $V_{clamp1(Latch)}$	1.0 1.8	1.2 2.4	1.4 3.0	V
TEMPERATURE SHUTDOWN						
Temperature shutdown	T_J going up	T_{TSD}	–	150	–	°C
Temperature shutdown hysteresis	T_J going down	$T_{TSD(HYS)}$	–	30	–	°C

6. Guaranteed by design.
7. CS pin source current is a sum of I_{bias} and I_{OPC}, thus at V_{HV} = 125 V is observed the I_{bias} only, because I_{OPC} is switched off.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTIC

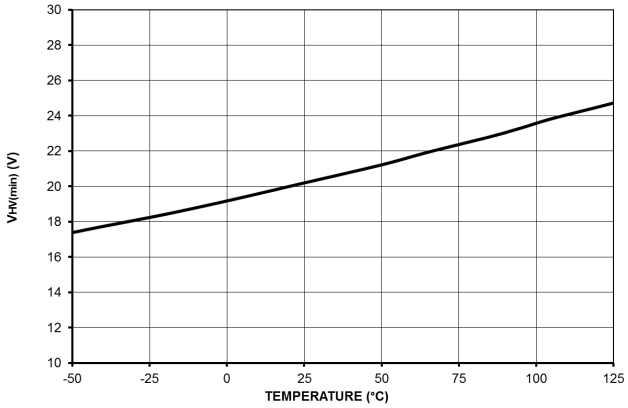


Figure 3. Minimum Voltage for HV Current Source Operation $V_{HV(min)}$

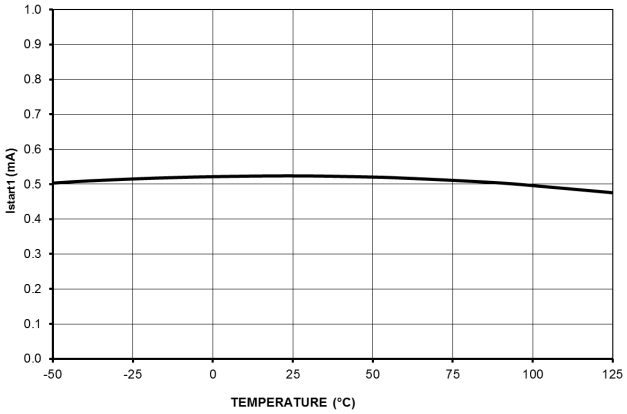


Figure 4. High Voltage Startup Current Flowing Out of V_{CC} Pin I_{start1} of V_{CC} Pin Fault/Short

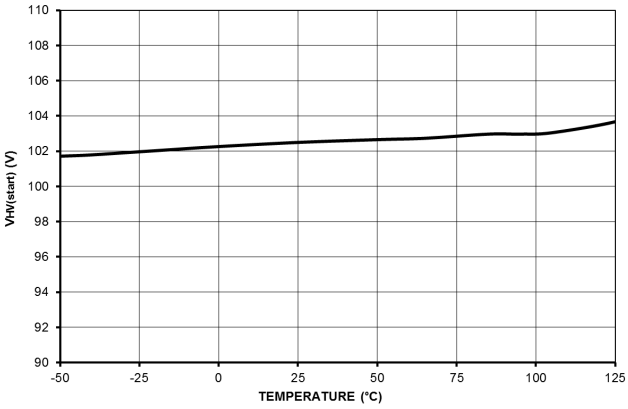


Figure 5. HV Pin Device Startup Threshold $V_{HV(start)}$

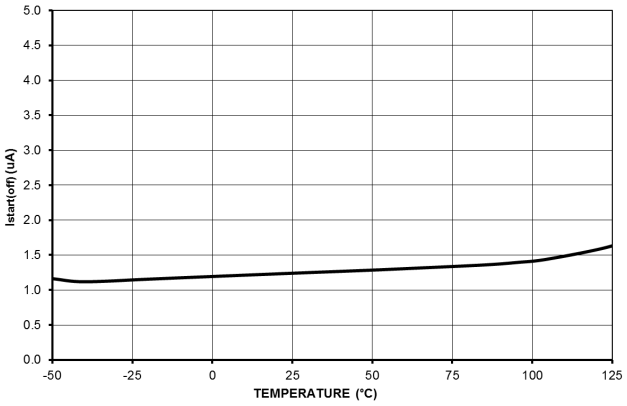


Figure 6. Off−state Leakage Current from HV Pin $I_{start(off)}$

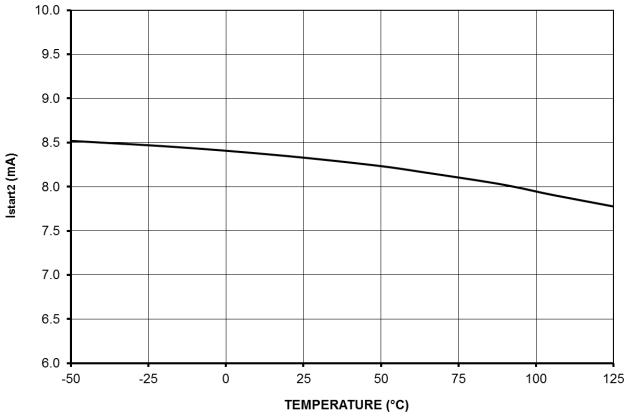


Figure 7. High Voltage Startup Current Flowing Out of V_{CC} Pin I_{start2}

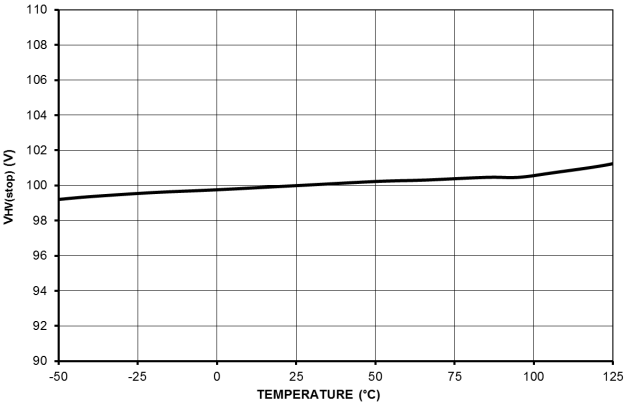


Figure 8. HV Pin Device Stop Threshold $V_{HV(stop)}$

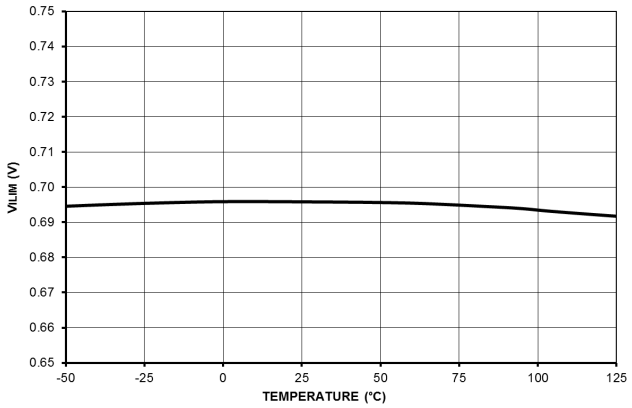


Figure 9. Maximum Internal Current Setpoint V_{ILIM}

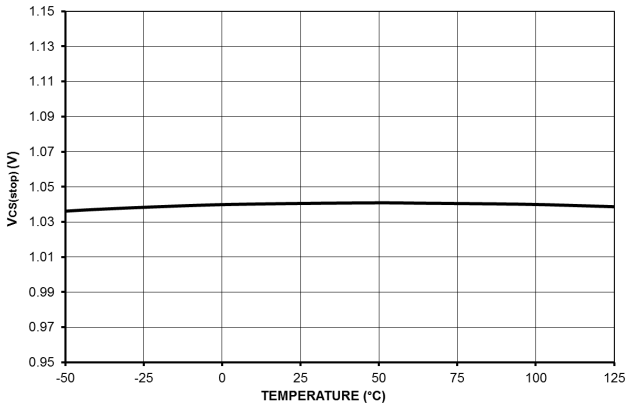


Figure 10. Threshold for the Very Fast Fault Protection Activation $V_{CS(stop)}$

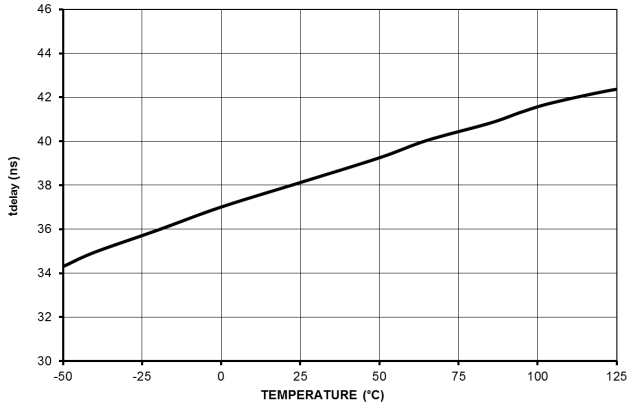


Figure 11. Propagation Delay t_{delay}

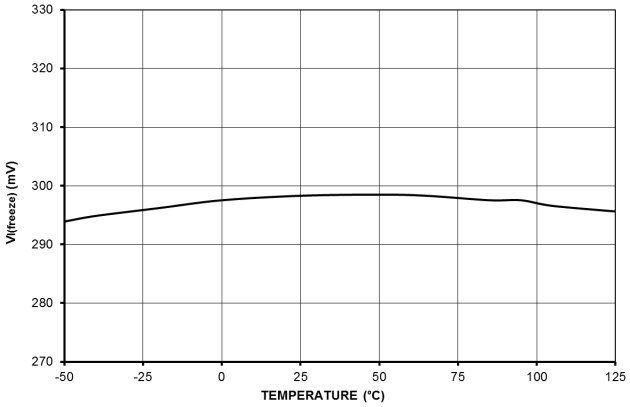


Figure 12. Frozen Current Setpoint $V_{I(freeze)}$ for the Light Load Operation

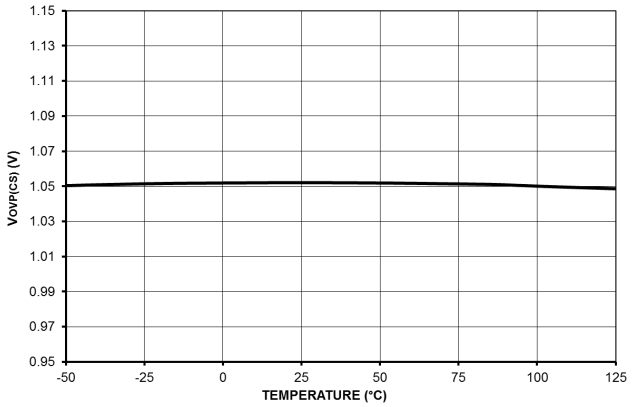


Figure 13. Over Voltage Protection Threshold at CS Pin $V_{OVP(CS)}$

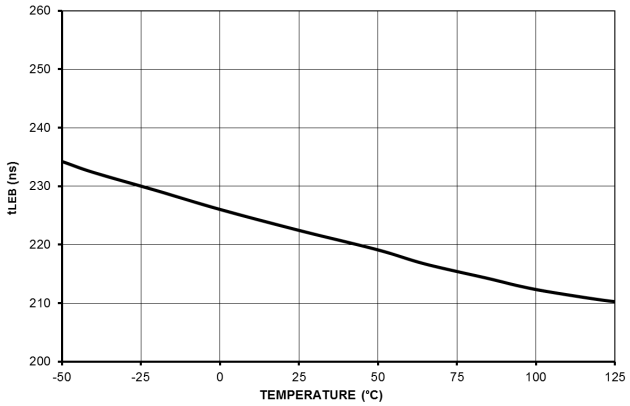


Figure 14. Leading Edge Blanking Duration t_{LEB}

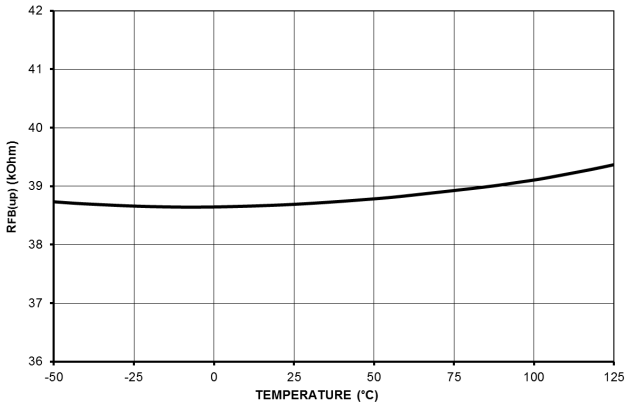


Figure 15. FB Pin Internal Pull−up Resistor $R_{FB(up)}$

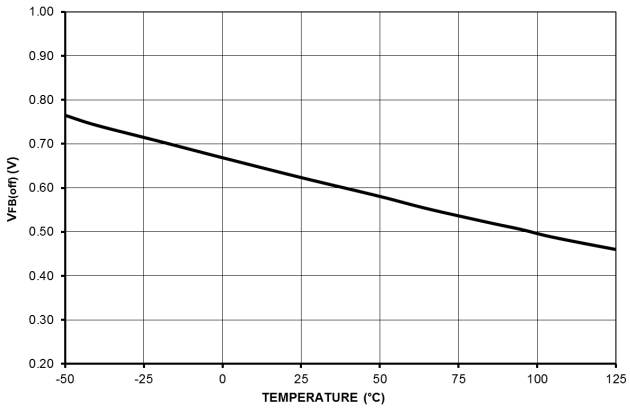


Figure 16. Built in Offset between FB Pin and Internal Divider $V_{FB(off)}$

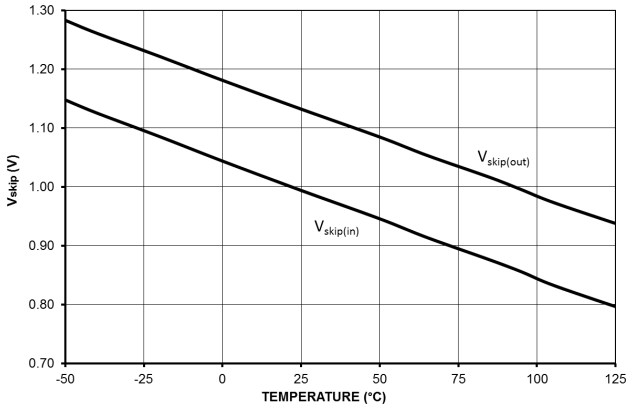


Figure 17. FB Pin Skip−In and Skip−Out Levels $V_{skip(in)}$ and $V_{skip(out)}$

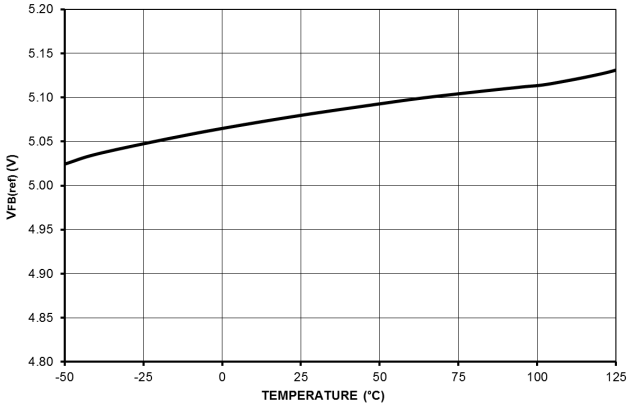


Figure 18. FB Pin Open Voltage $V_{FB(ref)}$

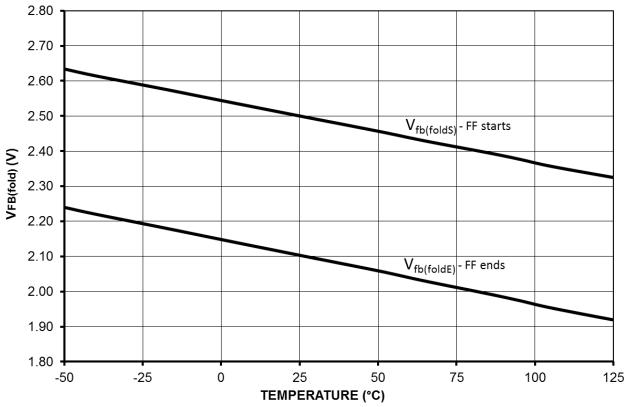


Figure 19. FB Pin Frequency Foldback Thresholds $V_{FB(foldS)}$ and $V_{FB(foldE)}$

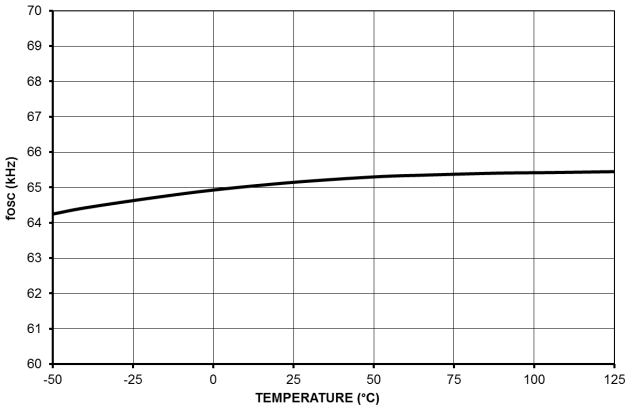


Figure 20. Oscillator Switching Frequency f_{OSC}

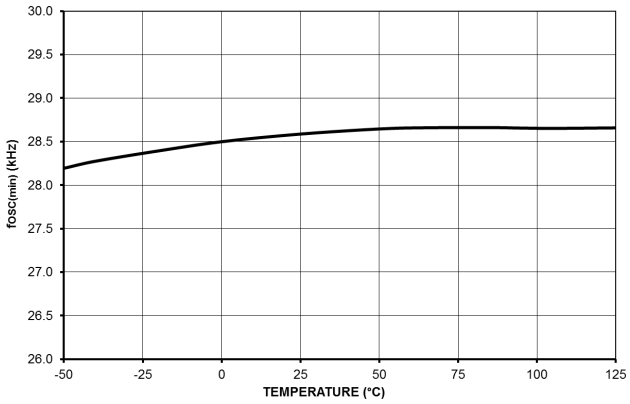


Figure 21. Minimum Switching Frequency $f_{OSC(min)}$

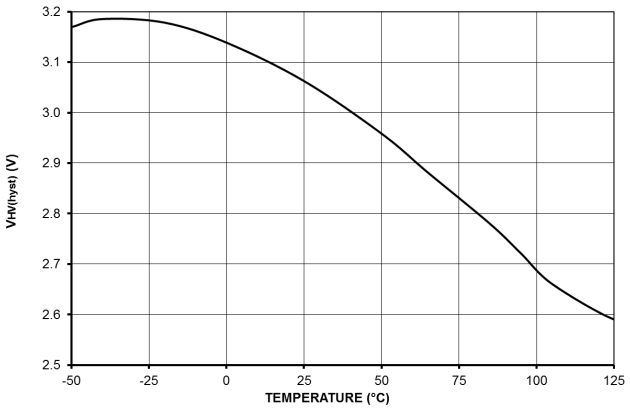


Figure 22. X2 Discharge Comparator Hysteresis Observed at HV Pin $V_{HV(hyst)}$

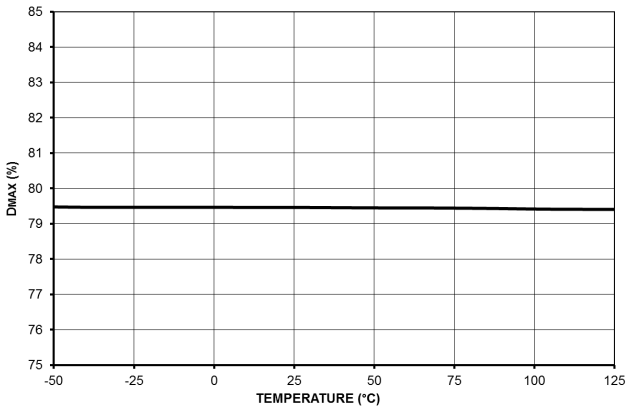


Figure 23. Maximum Duty Cycle D_{MAX}

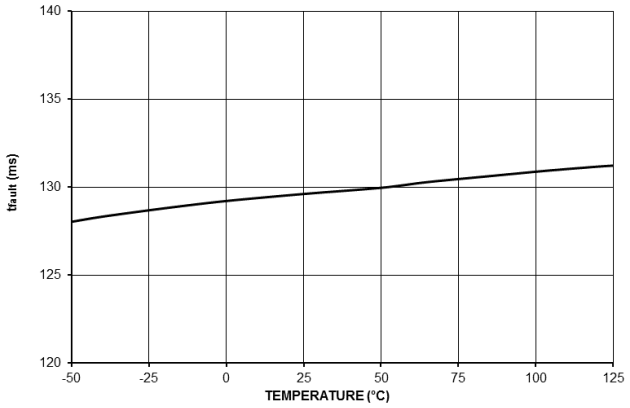


Figure 24. The Fault Timer Duration t_{fault}

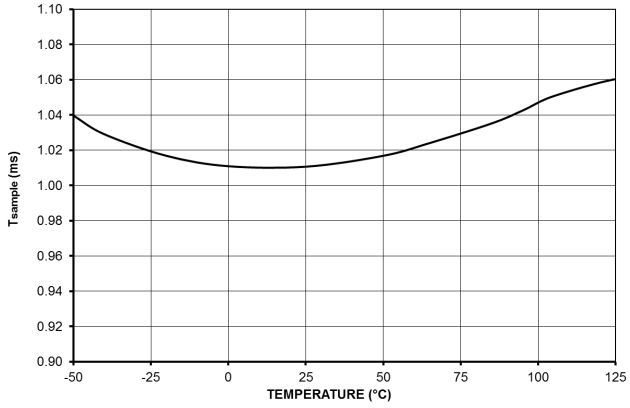


Figure 25. HV Signal Sampling Period T_{sample}

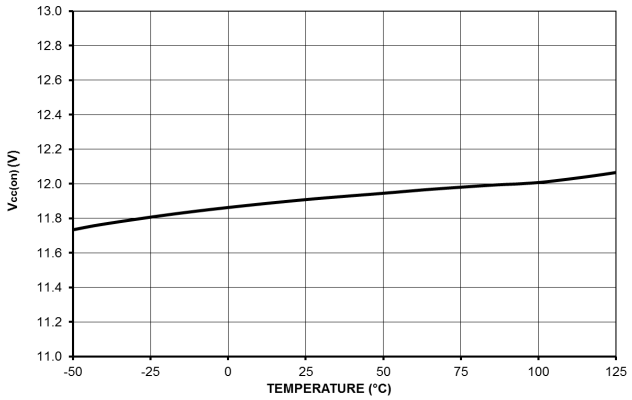


Figure 26. V_{CC} Turn−on Threshold Level, V_{CC} Going Up HV Current Source Stop Threshold $V_{CC(on)}$

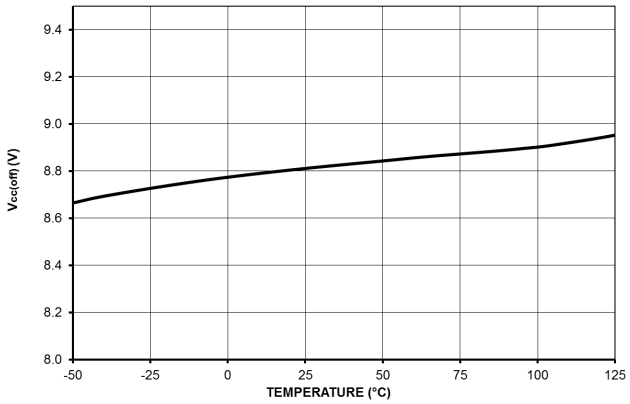


Figure 27. VCC Turn−off Threshold (UVLO) $V_{CC(off)}$

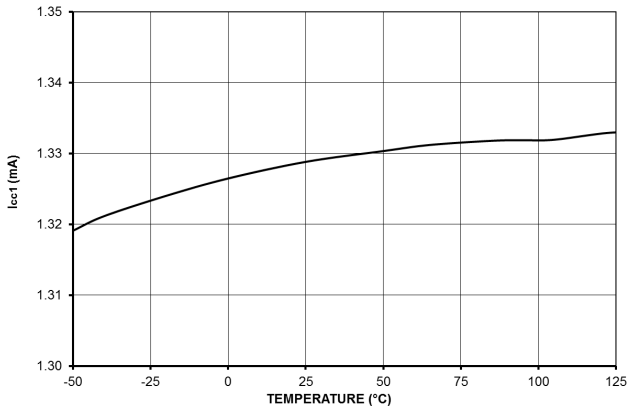


Figure 28. Internal Current Consumption when DRV Pin is Unloaded I_{CC1}

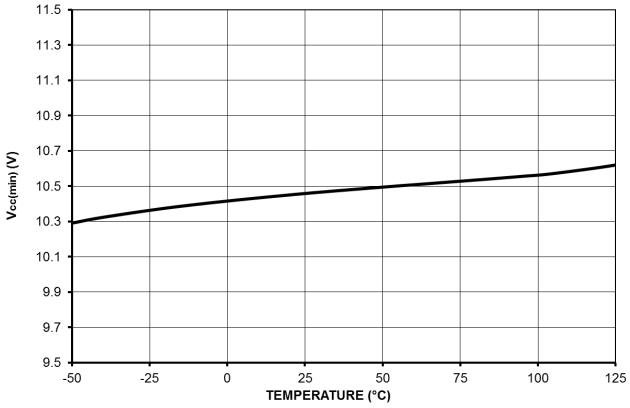


Figure 29. HV Current Source Restart Threshold $V_{CC(min)}$

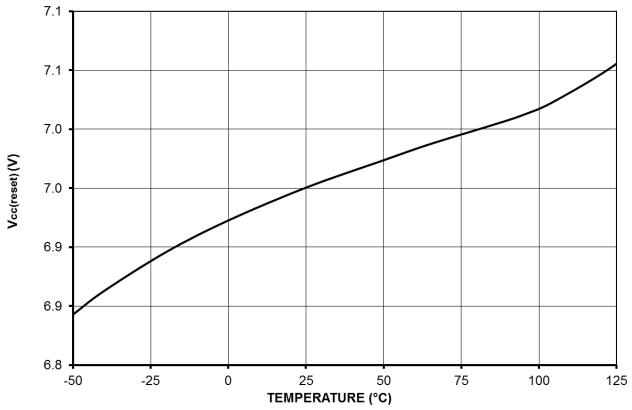


Figure 30. V_{CC} Decreasing Level at which the Internal Logic Resets $V_{CC(reset)}$

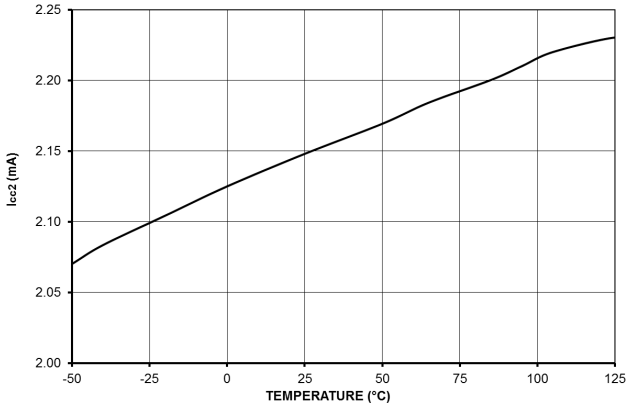


Figure 31. Internal Current Consumption when DRV Pin is Loaded by 1 nF Capacitance I_{CC2}

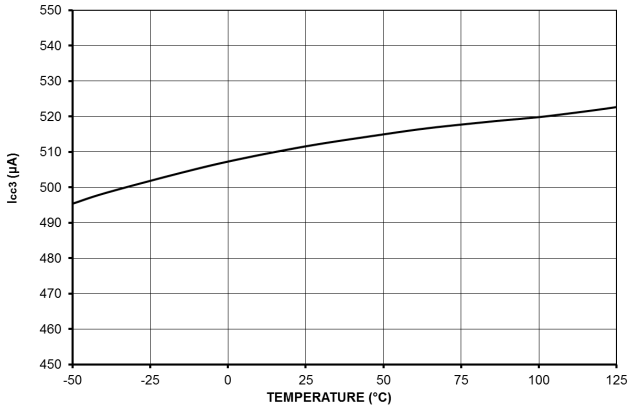


Figure 32. Internal Current Consumption in Skip Mode I_{CC3}

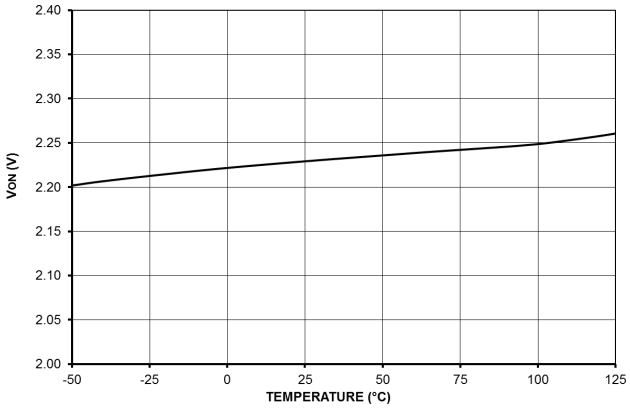


Figure 33. FB Pin Voltage Level Above which is Entered Normal Operating Mode V_{ON}

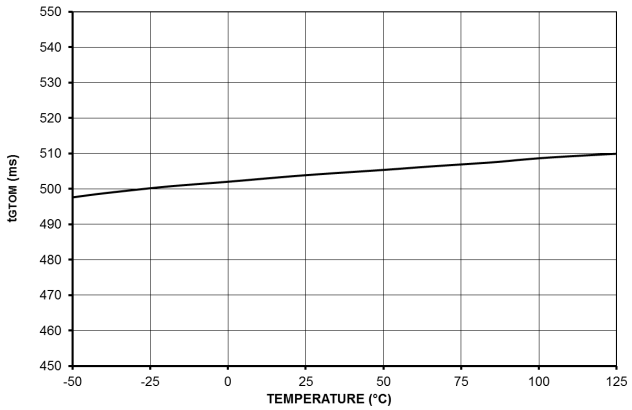


Figure 34. Go To Off Mode Timer Duration t_{GTOM}

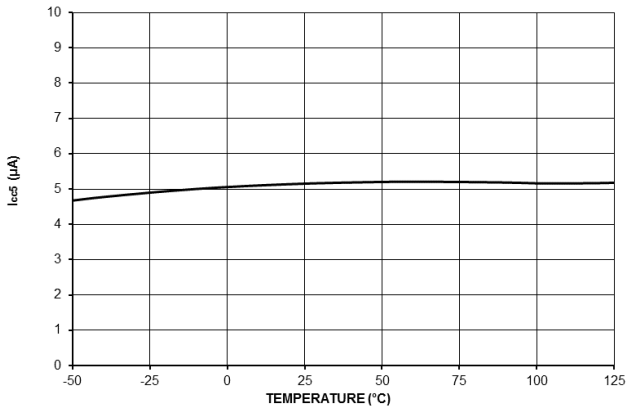


Figure 35. Internal Current Consumption in Off Mode I_{CC5}

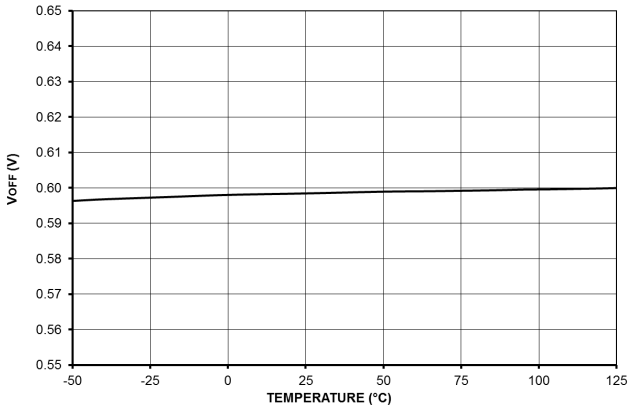


Figure 36. FB Pin Voltage Level Below which is Entered Off Mode V_{OFF}

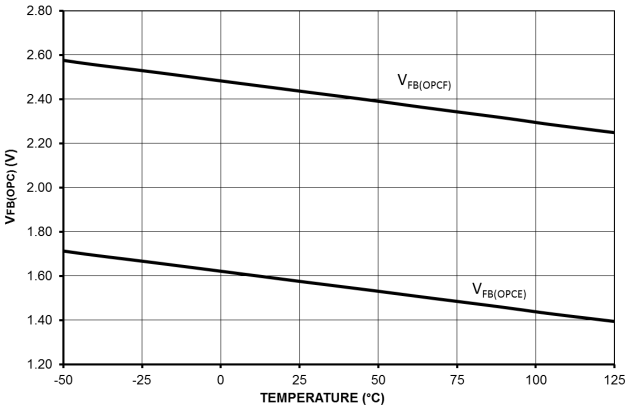


Figure 37. FB Pin Voltage Thresholds for Overpower Compensation

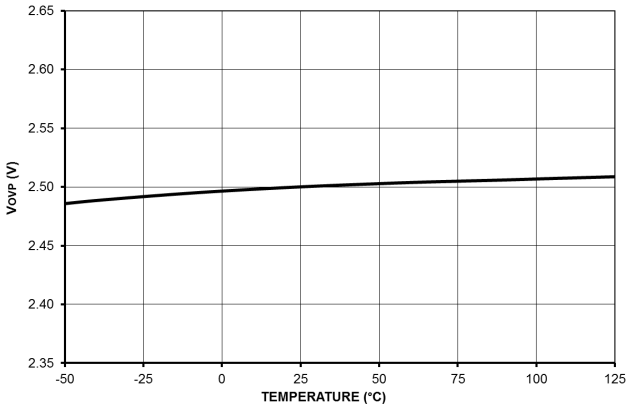


Figure 38. Fault Pin High Threshold for OVP V_{OVP}

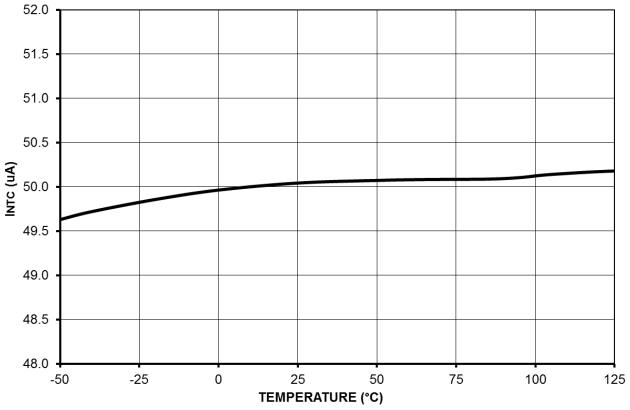


Figure 39. Current I_{NTC} Sourced Out from the Fault Pin, allowing Direct NTC Connection

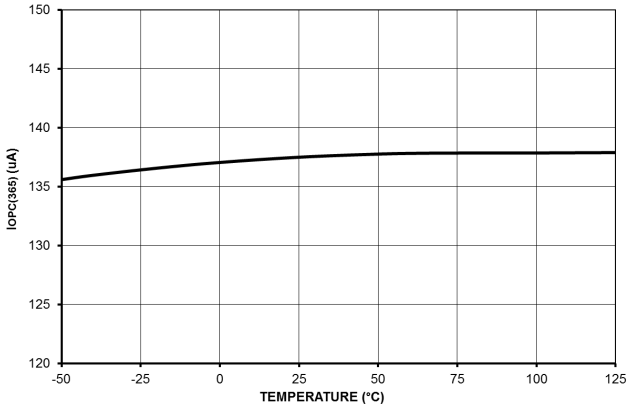


Figure 40. Current Flowing Out from CS Pin for Over Power Compensation @ 365 V at HV Pin $I_{OPC(365)}$

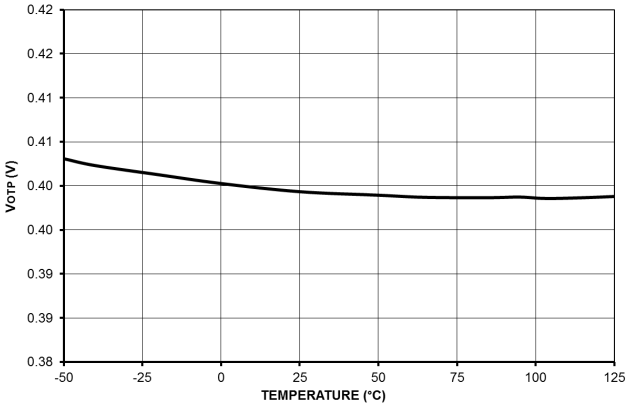
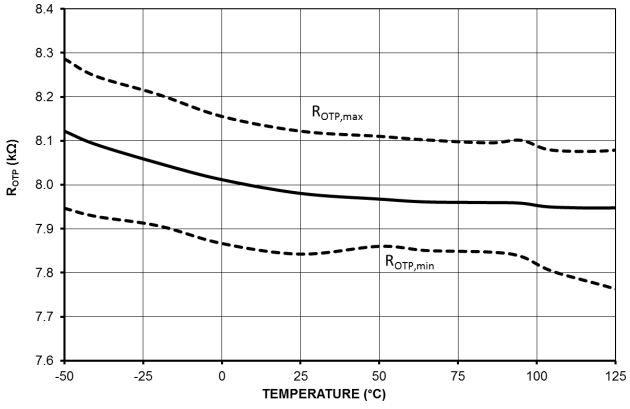


Figure 41. Fault Pin Low Threshold for OTP V_{OTP}



NOTE: The OTP resistance maximum and minimum courses are not the guaranteed limits, but the maximum and minimum measured data values from the device characterization.

Figure 42. The OTP Resistance Threshold R_{OTP}

APPLICATION INFORMATION

Functional Description

The NCP12400 includes all necessary features to build a safe and efficient power supply based on a fixed−frequency flyback converter. The NCP12400 is a multimode controller as illustrated in Figure 43. The mode of operation depends upon line and load condition. Under all modes of operation, the NCP12400 terminates the DRV signal based on the switch current. Thus, the NCP12400 always operates in current mode control so that the power MOSFET current is always limited.

Under normal operating conditions, the FB pin commands the operating mode of the NCP12400 at the voltage thresholds shown in Figure 43. At normal rated operating loads (from 100% to approximately 33% full rated power) the NCP12400 controls the converter in a fixed−frequency PWM mode. It can operate in the continuous conduction mode (CCM) or discontinuous conduction mode (DCM) depending upon the input voltage and loading conditions. If the controller is used in CCM with a wide input voltage range, the duty−ratio may increase up to 50%. The build−in slope compensation prevents the appearance of sub−harmonic oscillations in this operating area.

For loads that are between approximately 32% and 10% of full rated power, the converter operates in frequency foldback mode (FFM). If the feedback pin voltage is lower than 1.4 V the peak switch current is kept constant and the output voltage is regulated by modulating the switching frequency for a given and fixed input voltage V_{HV}.

Effectively, operation in FFM results in the application of constant volt−seconds to the flyback transformer each switching cycle. Voltage regulation in FFM is achieved by varying the switching frequency in the range from 65 kHz to 28 kHz. For extremely light loads (below approximately 6% full rated power), the converter is controlled using bursts of 28 kHz pulses. This mode is known as skip mode. The FFM, keeping constant peak current and skip mode allows design of the power supplies with increased efficiency under the light loading conditions. Keep in mind that the aforementioned boundaries of steady−state operation are approximate because they are subject to converter design parameters.

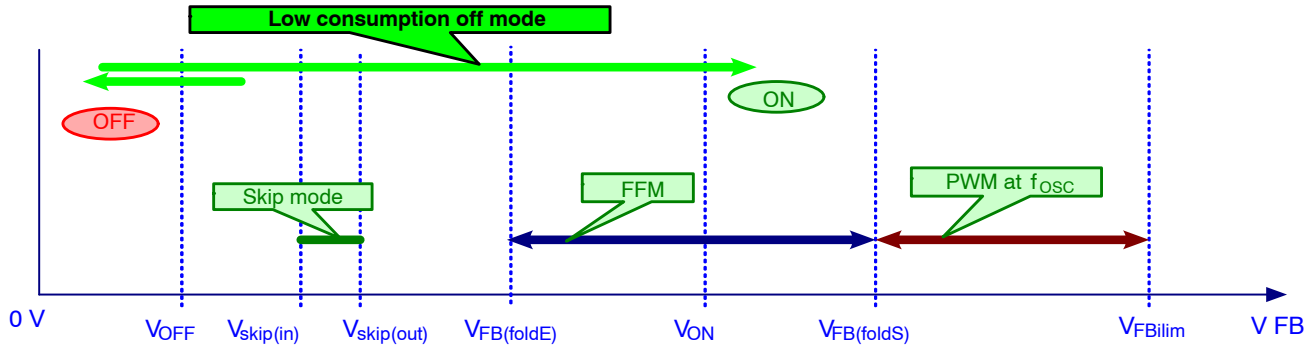
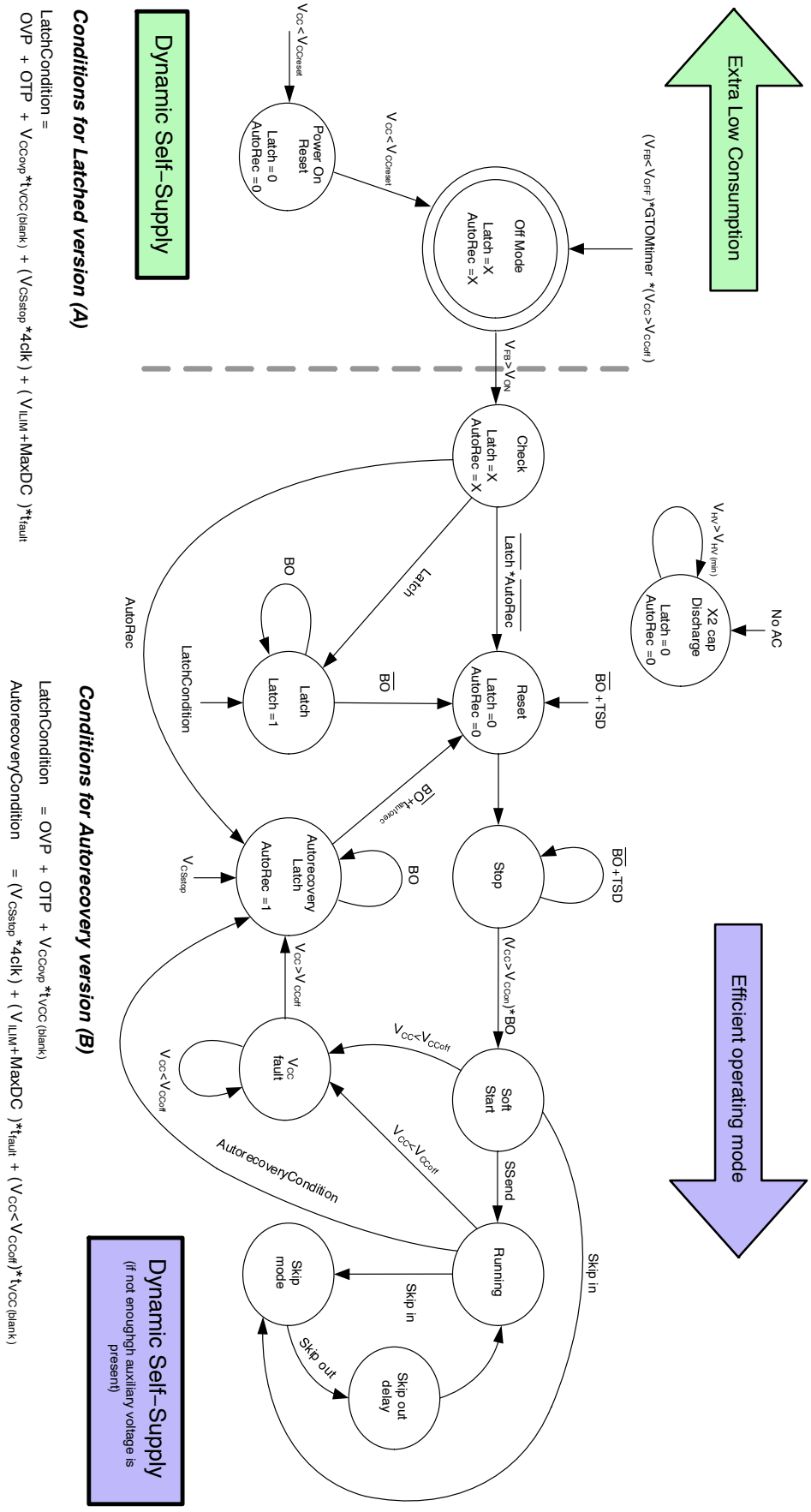


Figure 43. Mode Control with FB Pin Voltage

There was implemented the low consumption off mode allowing to reach extremely low no load input power. This mode is controlled by the FB pin and allows the remote control (or secondary side control) of the power supply shut−down. Most of the device internal circuitry is unbiased in the low consumption off mode. Only the FB pin control circuitry and X2 cap discharging circuitry is operating in the low consumption off mode. If the voltage at feedback pin decreases below the 0.6 V the controller will enter the low consumption off mode. The controller can start if the FB pin voltage increases above the 2.2 V level.

See the detailed status diagrams for the both versions fully latched A and the autorecovery B on the following figures. The basic status of the device after wake−up by the V_{CC} is the off mode and mode is used for the overheating protection mode if the thermal shutdown protection is activated.



Conditions for Latched version (A)

LatchCondition =
OVP + OTP + V_{CCovp}*$t_{VCC\ (blank)}$ + (V_{CSstop}*4clk) + (V_{ILIM}+MaxDC)*t_{fault}

Conditions for Autorecovery version (B)

LatchCondition = OVP + OTP + V_{CCovp}*$t_{VCC\ (blank)}$

AutorecoveryCondition = (V_{CSstop}*4clk) + (V_{ILIM}+MaxDC)*t_{fault} + (V_{CC}<V_{CCoff})*$t_{VCC\ (blank)}$

Figure 44. Operating Status Diagram of the Device

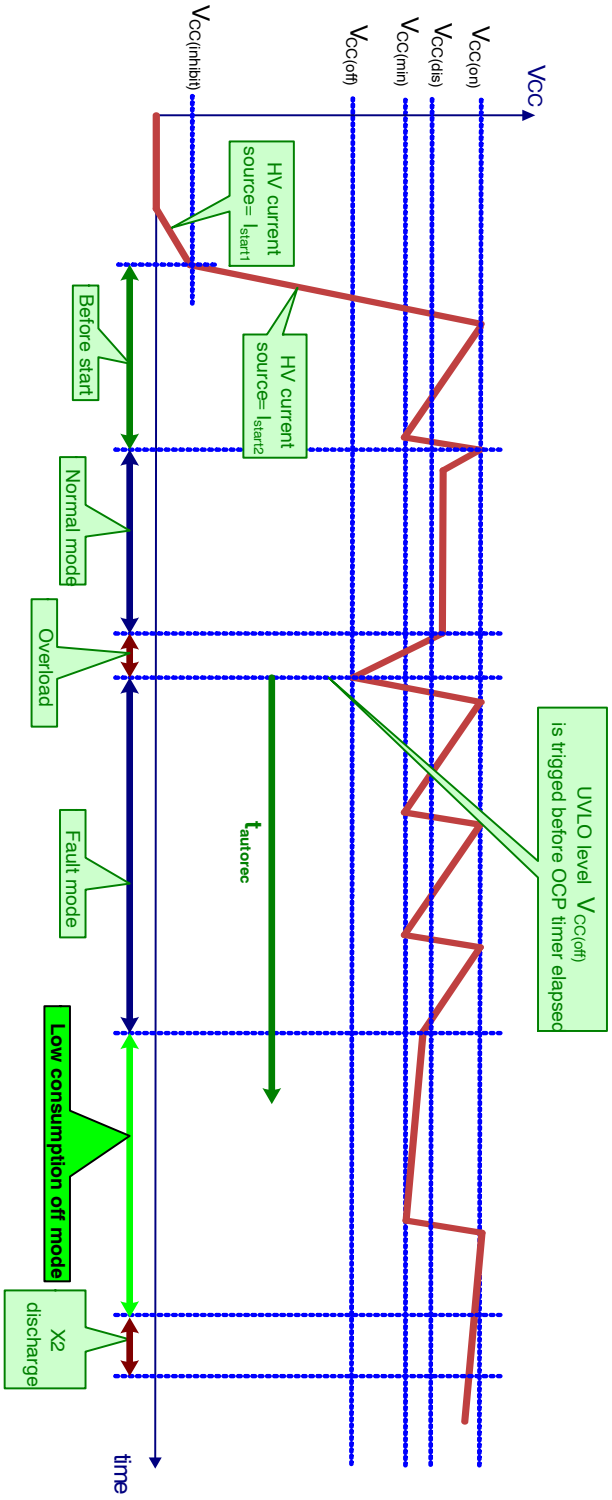


Figure 45. V_{CC} Management Timing Diagram

The information about the fault (permanent Latch or Autorecovery) is kept during the low consumption off mode due the safety reason. The reason is not to allow unlatch the device by the remote control being in off mode.

Start−up of the Controller

At start−up, the current source turns on when the voltage on the HV pin is higher than $V_{HV(min)}$, and turns off when V_{CC} reaches $V_{CC(on)}$, then turns on again when V_{CC} reaches

$V_{CC(min)}$, until the input voltage is high enough to ensure a proper start−up, i.e. when V_{HV} reaches $V_{HV(start)}$. The controller actually starts the next time V_{CC} reaches $V_{CC(on)}$. The controller then delivers pulses, starting with a soft−start period t_{SSTART} during which the peak current linearly increases before the current−mode control takes over.

Even though the Dynamic Self−Supply is able to maintain the V_{CC} voltage between $V_{CC(on)}$ and $V_{CC(min)}$ by turning the HV start−up current source on and off, it can only be used in light load condition, otherwise the power dissipation on the die would be too much. As a result, an auxiliary voltage source is needed to supply V_{CC} during normal operation.

The Dynamic Self−Supply is useful to keep the controller alive when no switching pulses are delivered, e.g. in brown−out condition, or to prevent the controller from stopping during load transients when the V_{CC} might drop. The NCP12400 accepts a supply voltage as high as 28 V, with an overvoltage threshold $V_{CC(ovp)}$ that latches the controller off.

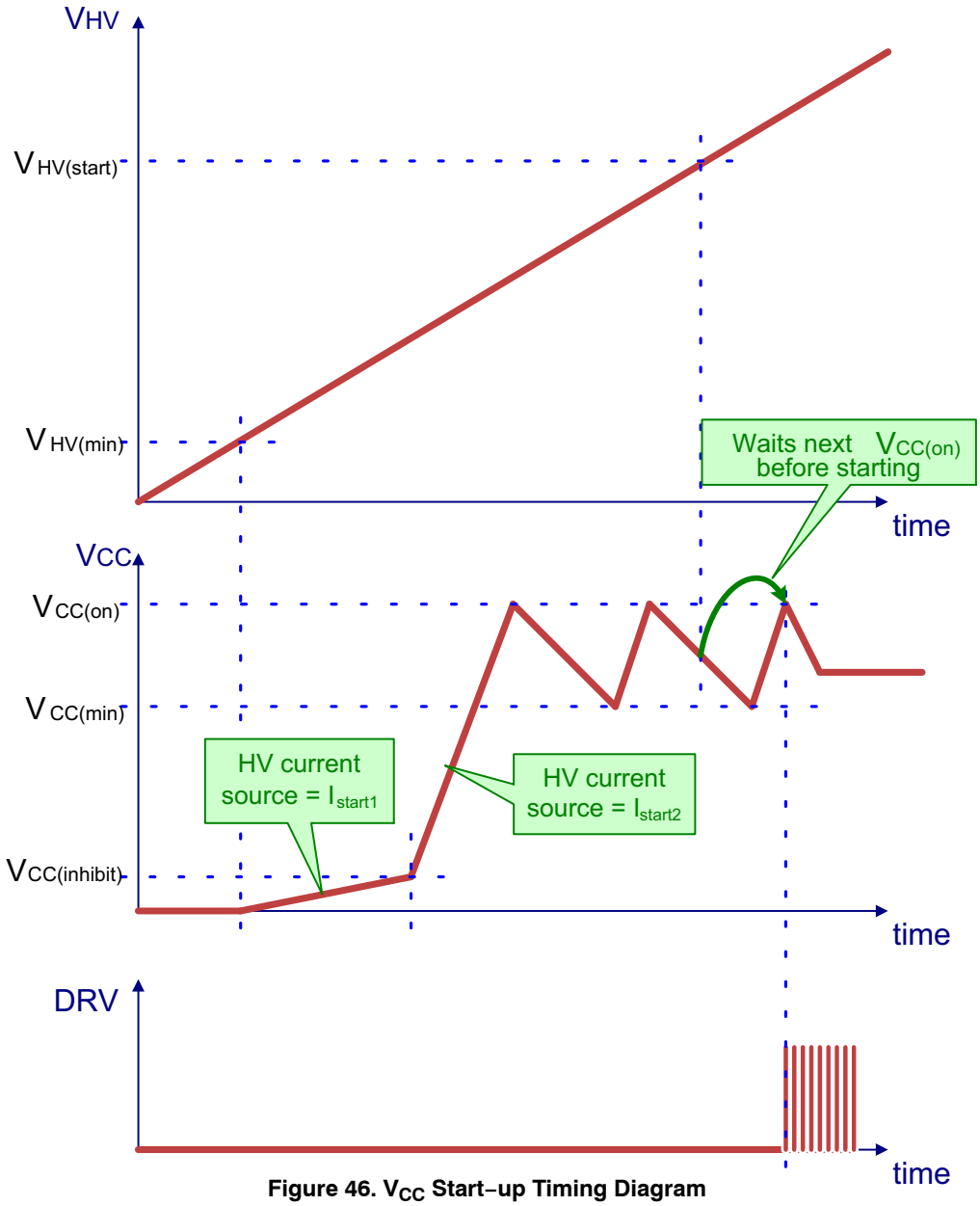


Figure 46. V_{CC} Start−up Timing Diagram

For safety reasons, the start−up current is lowered when V_{CC} is below $V_{CC(inhibit)}$, to reduce the power dissipation in case the V_{CC} pin is shorted to GND (in case of V_{CC} capacitor failure, or external pull−down on V_{CC} to disable the controller). There is only one condition for which the current source doesn't turn on when V_{CC} reaches $V_{CC(inhibit)}$: the voltage on HV pin is too low (below $V_{HV(min)}$).

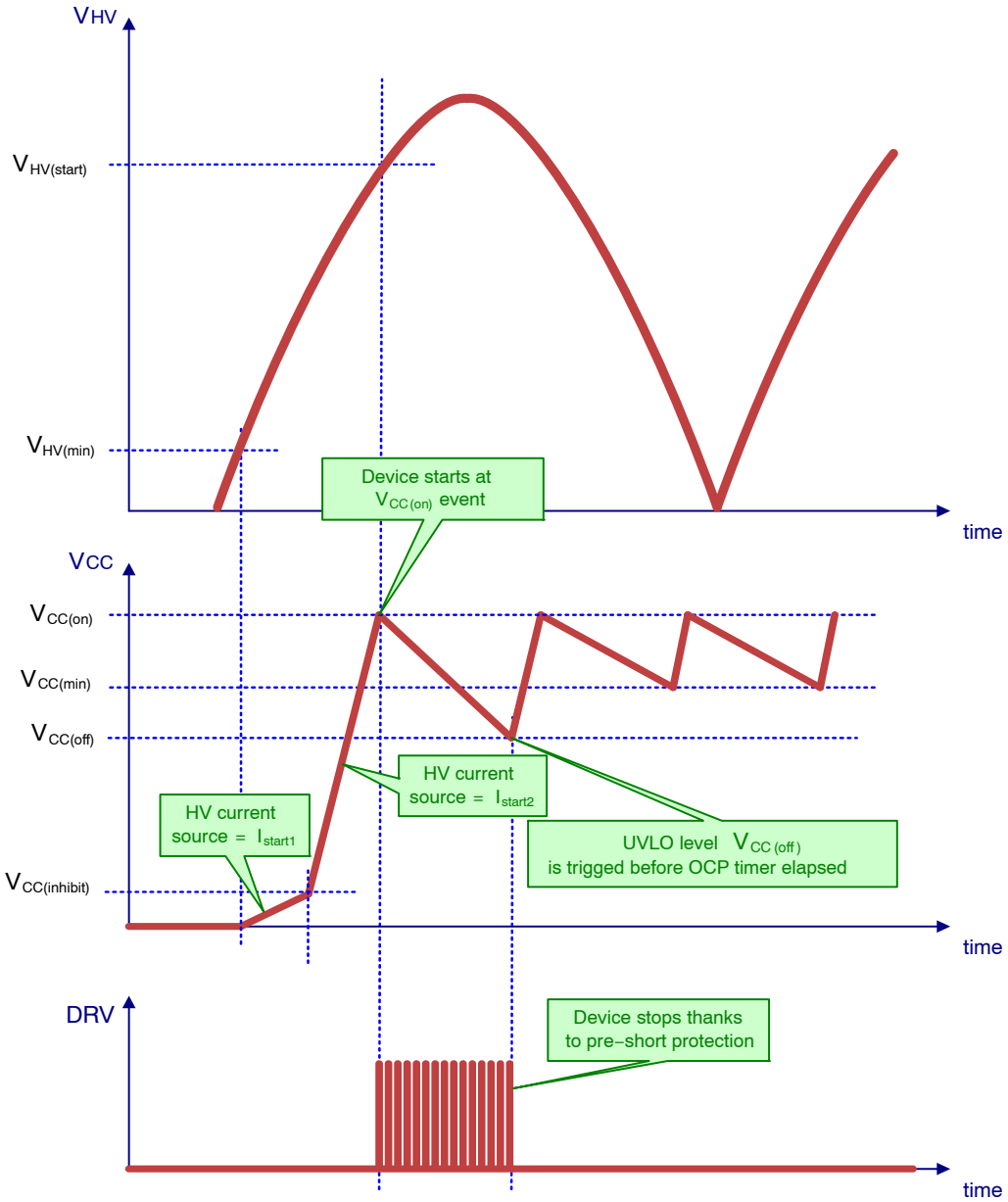


Figure 47. Latch After the Preshort

HV Sensing of Rectified AC Voltage

The NCP12400 features on its HV pin a true ac line monitoring circuitry. It includes a minimum start−up threshold and an autorecovery brown−out protection; both of them independent of the ripple on the input voltage. It is allowed only to work with an unfiltered, rectified ac input to ensure the X2 capacitor discharge function as well, which is described in following. The brown−out protection thresholds are fixed, but they are designed to fit most of the standard ac−dc conversion applications.

When the input voltage goes below $V_{HV(stop)}$, a brown−out condition is detected, and the controller stops. The HV current source maintains V_{CC} between $V_{CC(on)}$ and $V_{CC(min)}$ levels until the input voltage is back above $V_{HV(start)}$.

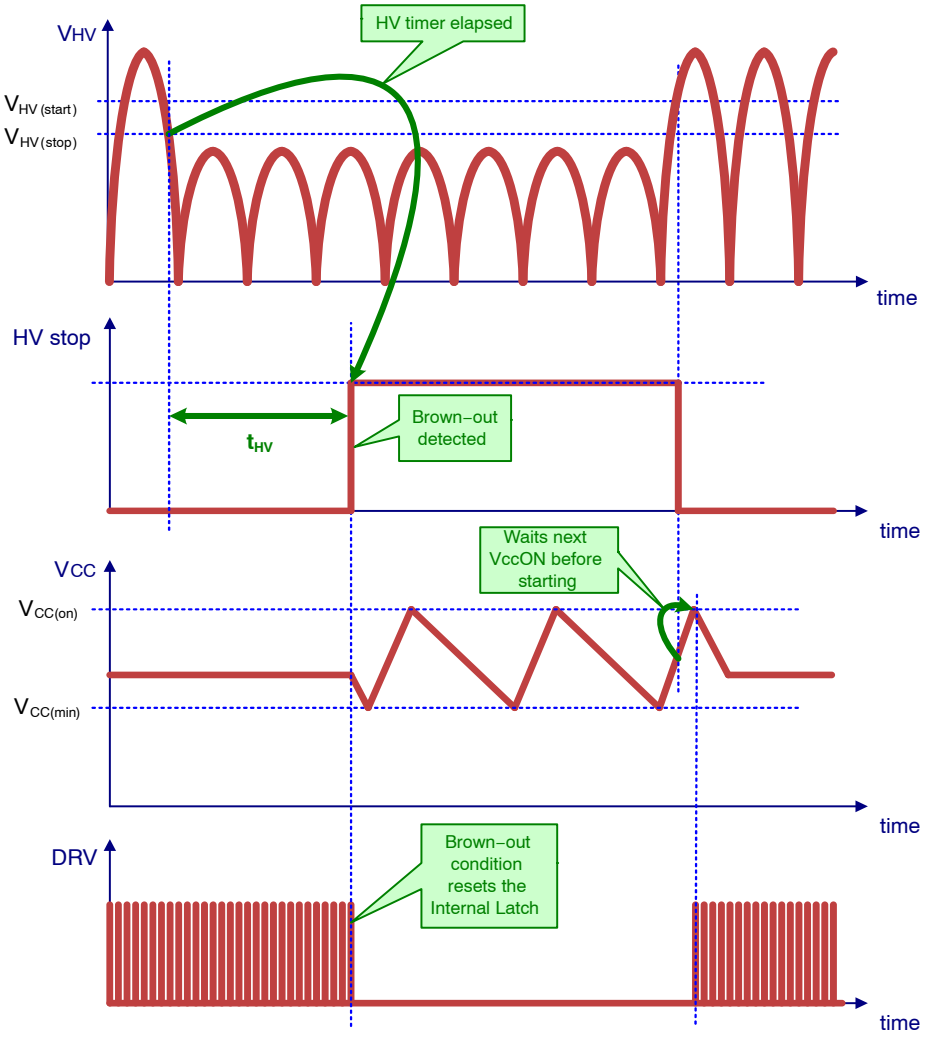


Figure 48. Ac Line Drop−out Timing Diagram

When V_{HV} crosses the $V_{HV(start)}$ threshold, the controller can start immediately. When it crosses $V_{HV(stop)}$, it triggers a timer of duration t_{HV}, this ensures that the controller doesn't stop in case of line cycle drop−out.

When V_{HV} crosses the $V_{HV(start)}$ threshold, the controller starts when the V_{CC} crosses the next $V_{CC(on)}$ event. When it crosses $V_{HV(stop)}$, it triggers a timer of duration t_{HV}, this ensures that the controller doesn't stop in case of line cycle drop−out. The device restart after the ac line voltage drop−out is protected to the parasitic restart initiated e.g. the spikes induced at HV pin immediately after the device is stopped by the residual energy in the EMI filter. The device restart is allowed only after the 1st watch dog signal event. The basic principle is shown at Figure 49 and detail of the device restart is shown at Figure 50.

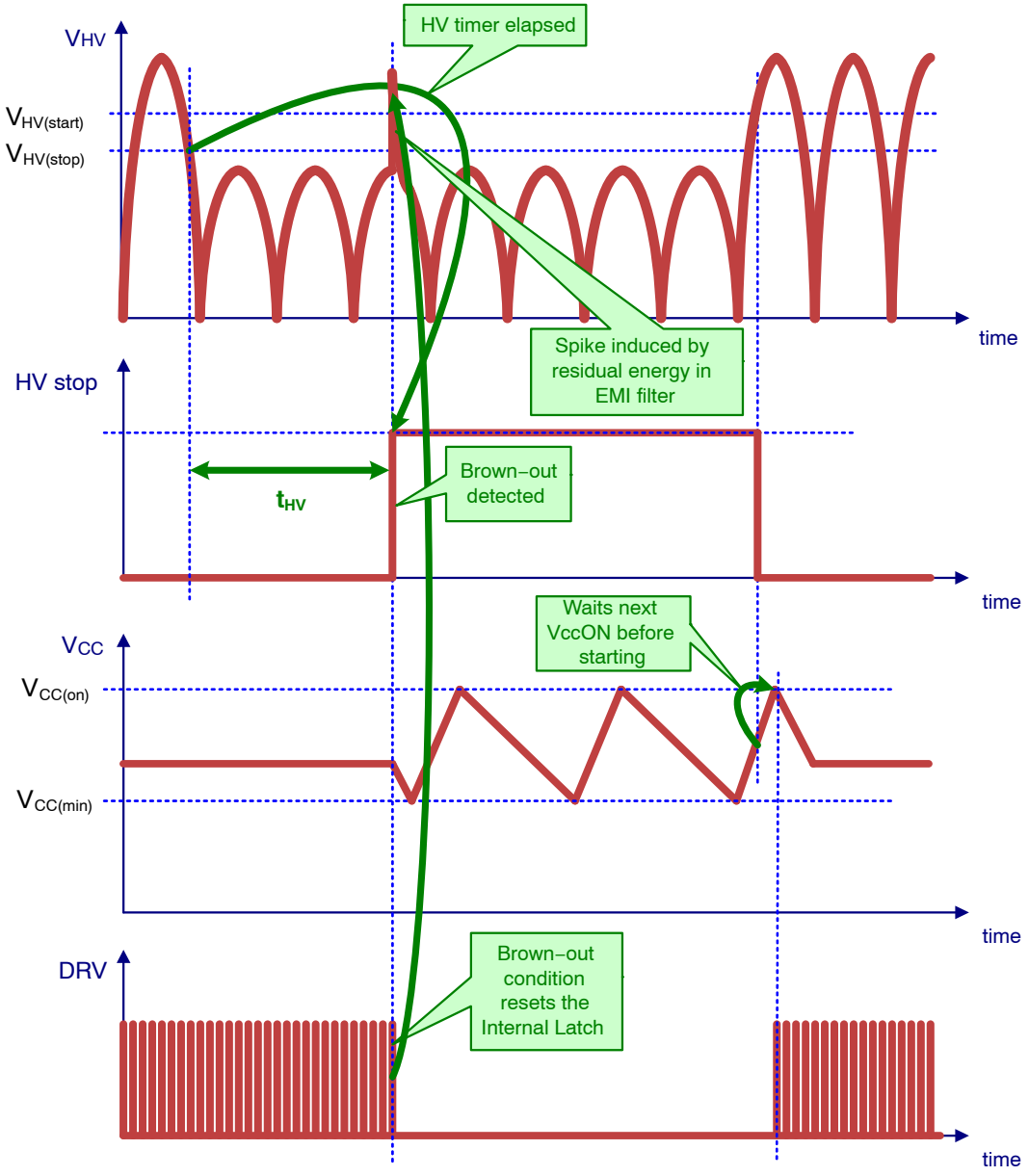


Figure 49. Ac Line Drop−out Timing Diagram with the Parasitic Spike

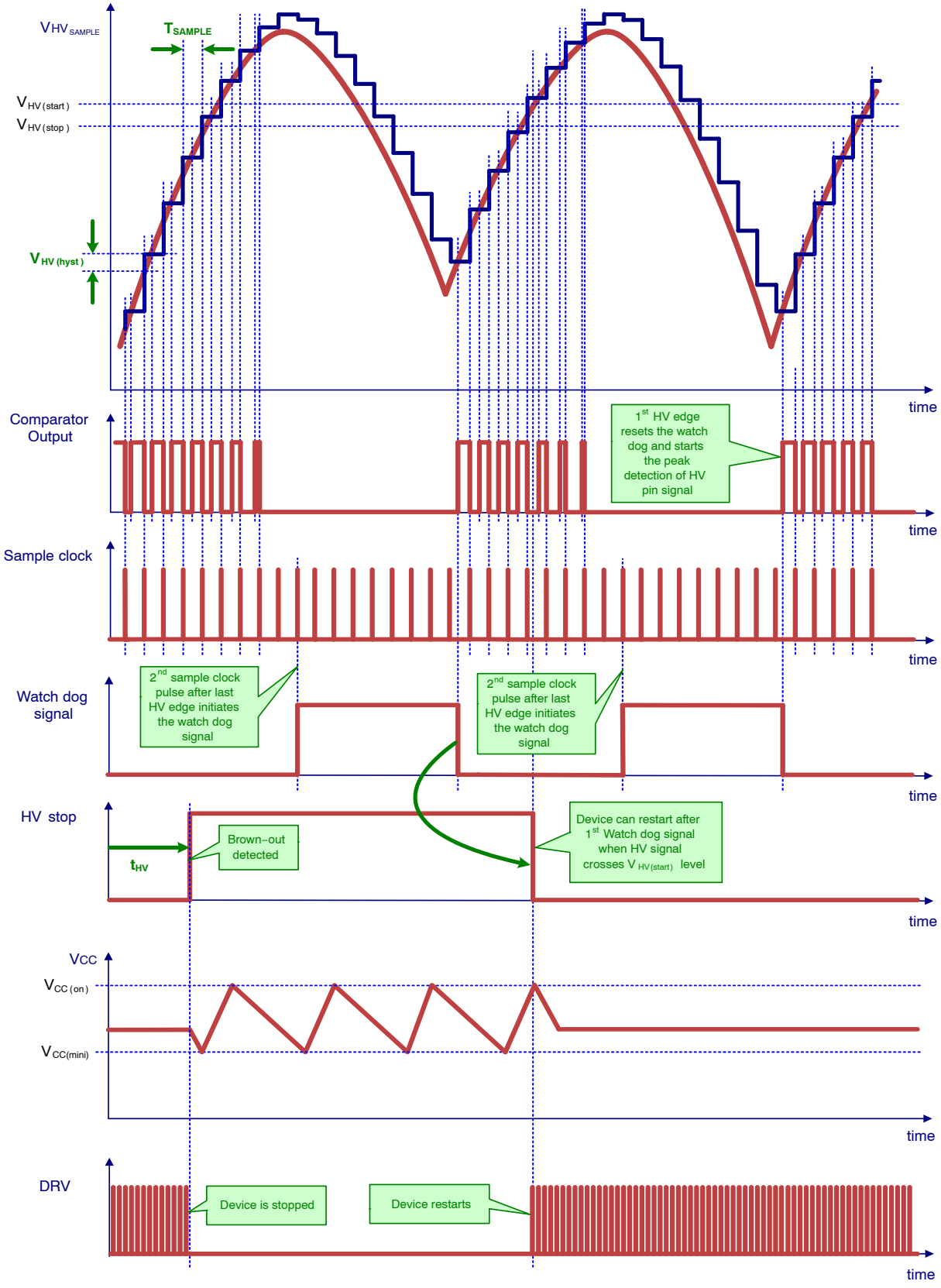


Figure 50. Detailed Timing Diagram of the Device Restart after the Short ac Line Drop−out

X2 Cap Discharge Feature

The X2 capacitor discharging feature is offered by usage of the NCP12400. This feature save approx. 16 mW – 25 mW input power depending on the EMI filter X2 capacitors volume and it saves the external components count as well. The discharge feature is ensured via the start−up current source with a dedicated control circuitry for this function. The X2 capacitors are being discharged by current defined as I_{start2} when this need is detected.

There is used a dedicated structure called ac line unplug detector inside the X2 capacitor discharge control circuitry. See the Figure 51 for the block diagram for this structure and Figures 52, 53, 54 and 55 for the timing diagrams. The basic idea of ac line unplug detector lies in comparison of the direct sample of the high voltage obtained via the high voltage sensing structure with the delayed sample of the high voltage. The delayed signal is created by the sample & hold structure.

The comparator used for the comparison of these signals is without hysteresis inside. The resolution between the slopes of the ac signal and dc signal is defined by the sampling time T_{SAMPLE} and additional internal offset N_{OS}. These parameters ensure the noise immunity as well. The additional offset is added to the picture of the sampled HV signal and its analog sum is stored in the C_1 storage capacitor. If the voltage level of the HV sensing structure output crosses this level the comparator CMP output signal resets the detection timer and no dc signal is detected. The additional offset N_{OS} can be measured as the $V_{HV(hyst)}$ on the HV pin. If the comparator output produces pulses it means that the slope of input signal is higher than set resolution level and the slope is positive. If the comparator output produces the low level it means that the slope of input signal is lower than set resolution level or the slope is negative. There is used the detection timer which is reset by any edge of the comparator output. It means if no edge comes before the timer elapses there is present only dc signal or signal with the small ac ripple at the HV pin. This type of the ac detector detects only the positive slope, which fulfils the requirements for the ac line presence detection.

In case of the dc signal presence on the high voltage input, the direct sample of the high voltage obtained via the high voltage sensing structure and the delayed sample of the high voltage are equivalent and the comparator produces the low level signal during the presence of this signal. No edges are present at the output of the comparator, that's why the detection timer is not reset and dc detect signal appears.

The minimum detectable slope by this ac detector is given by the ration between the maximum hysteresis observed at HV pin $V_{HV(hyst),max}$ and the sampling time:

$$S_{min} = \frac{V_{HV(hyst),max}}{T_{sample}} \qquad \text{(eq. 1)}$$

Than it can be derived the relationship between the minimum detectable slope and the amplitude and frequency of the sinusoidal input voltage:

$$V_{max} = \frac{V_{HV(hyst),max}}{2 \cdot \pi \cdot f \cdot T_{sample}} = \frac{5}{2 \cdot \pi \cdot 35 \cdot 1 \cdot 10^{-3}} =$$

$$= 22.7\ V \qquad \text{(eq. 2)}$$

The minimum detectable AC RMS voltage is 16 V at frequency 35 Hz, if the maximum hysteresis is 5 V and sampling time is 1 ms.

The X2 capacitor discharge feature is available in any controller operation mode to ensure this safety feature. The detection timer is reused for the time limiting of the discharge phase, to protect the device against overheating. The discharging process is cyclic and continues until the ac line is detected again or the voltage across the X2 capacitor is lower than $V_{HV(min)}$. This feature ensures to discharge quite big X2 capacitors used in the input line filter to the safe level. **It is important to note that it is not allowed to connect HV pin to any dc voltage due this feature. e.g. directly to bulk capacitor.**

During the HV sensing or X2 cap discharging the V_{CC} net is kept above the $V_{CC(off)}$ voltage by the Self−Supply in any mode of device operation to supply the control circuitry. During the discharge sequence is not allowed to start−up the device.

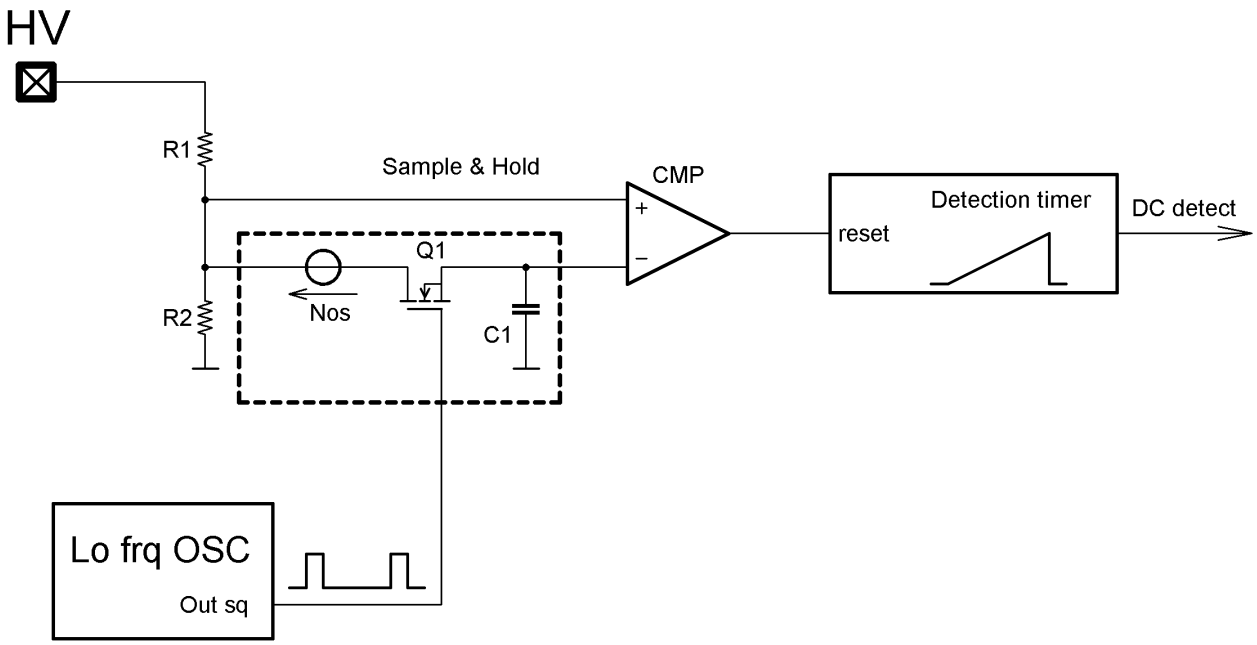


Figure 51. The ac Line Unplug Detector Structure Used for X2 Capacitor Discharge System

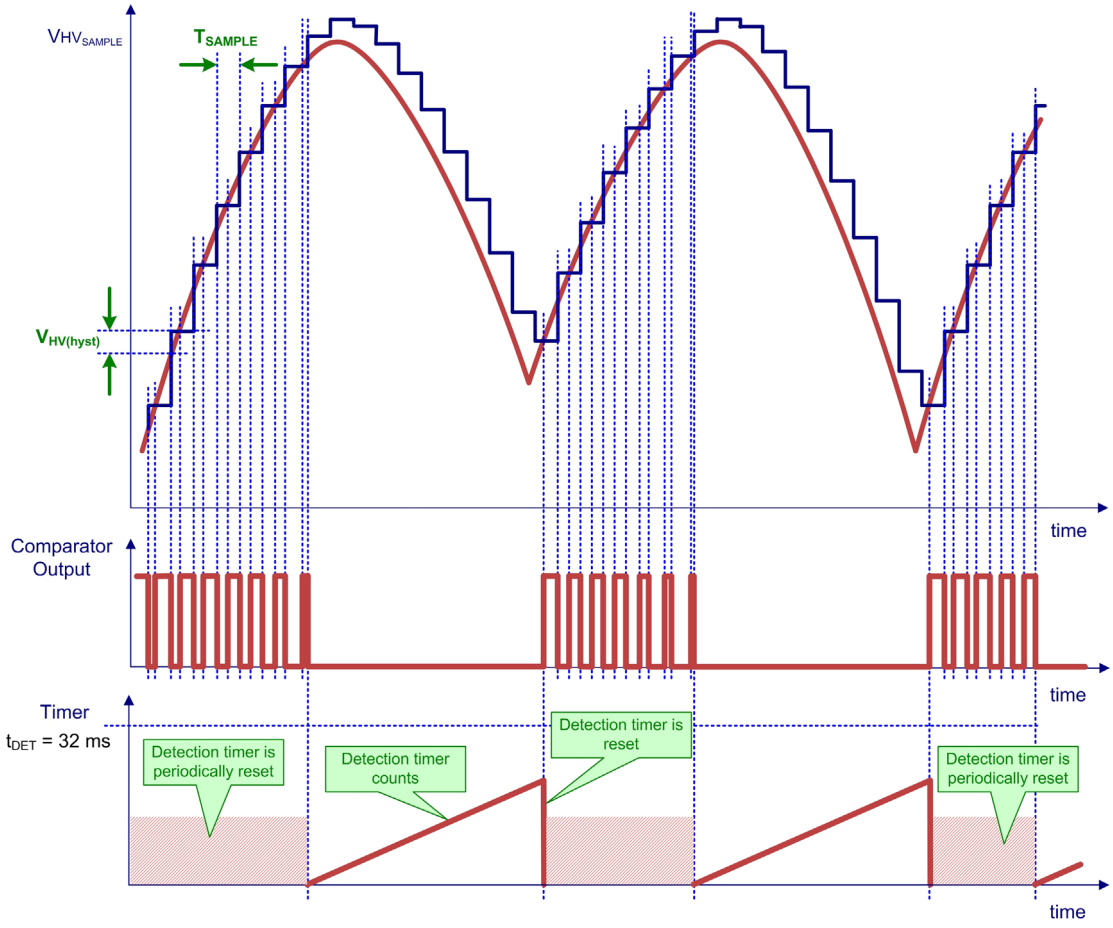


Figure 52. The ac Line Unplug Detector Timing Diagram

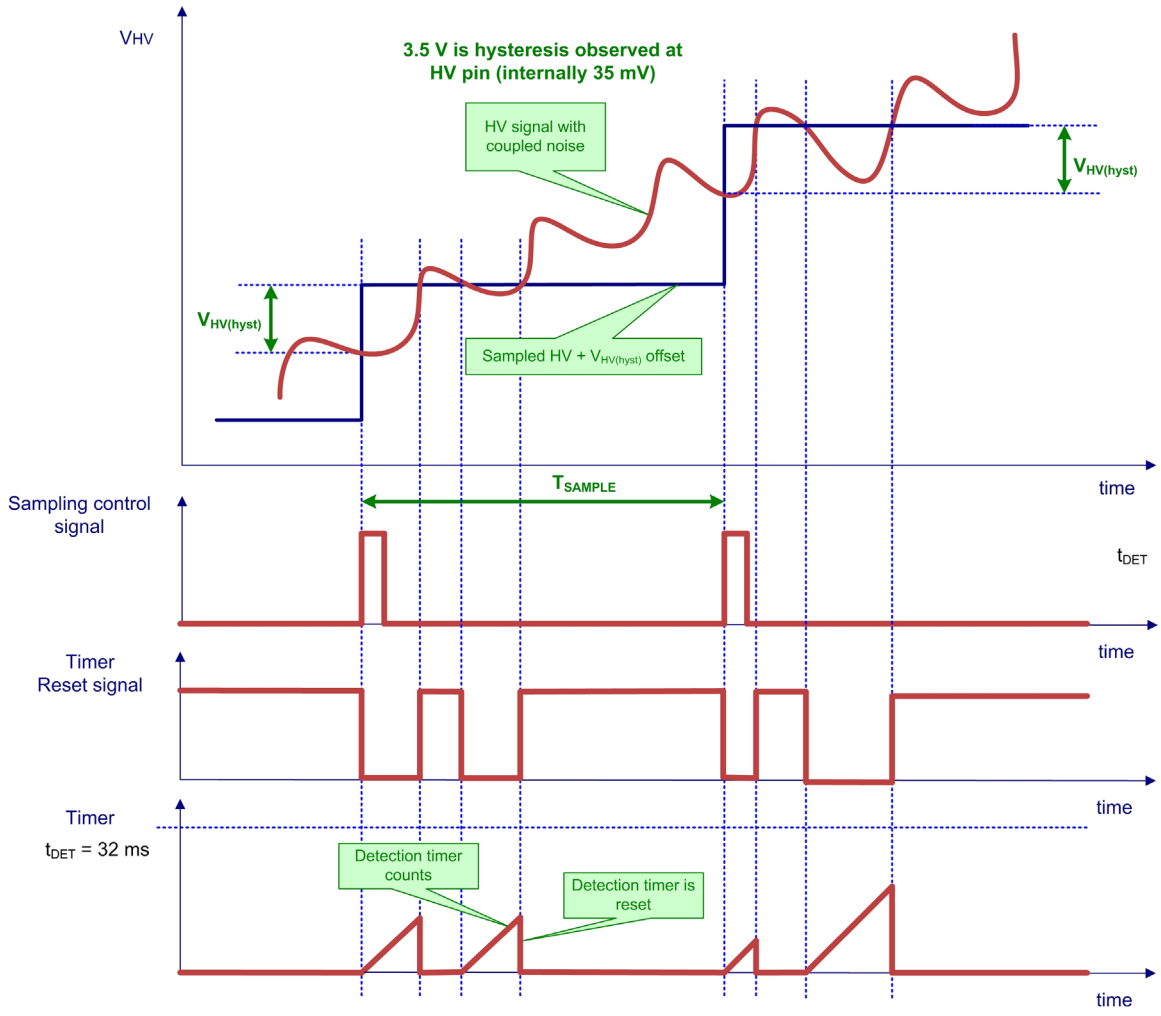


Figure 53. The ac Line Unplug Detector Timing Diagram Detail with Noise Effects

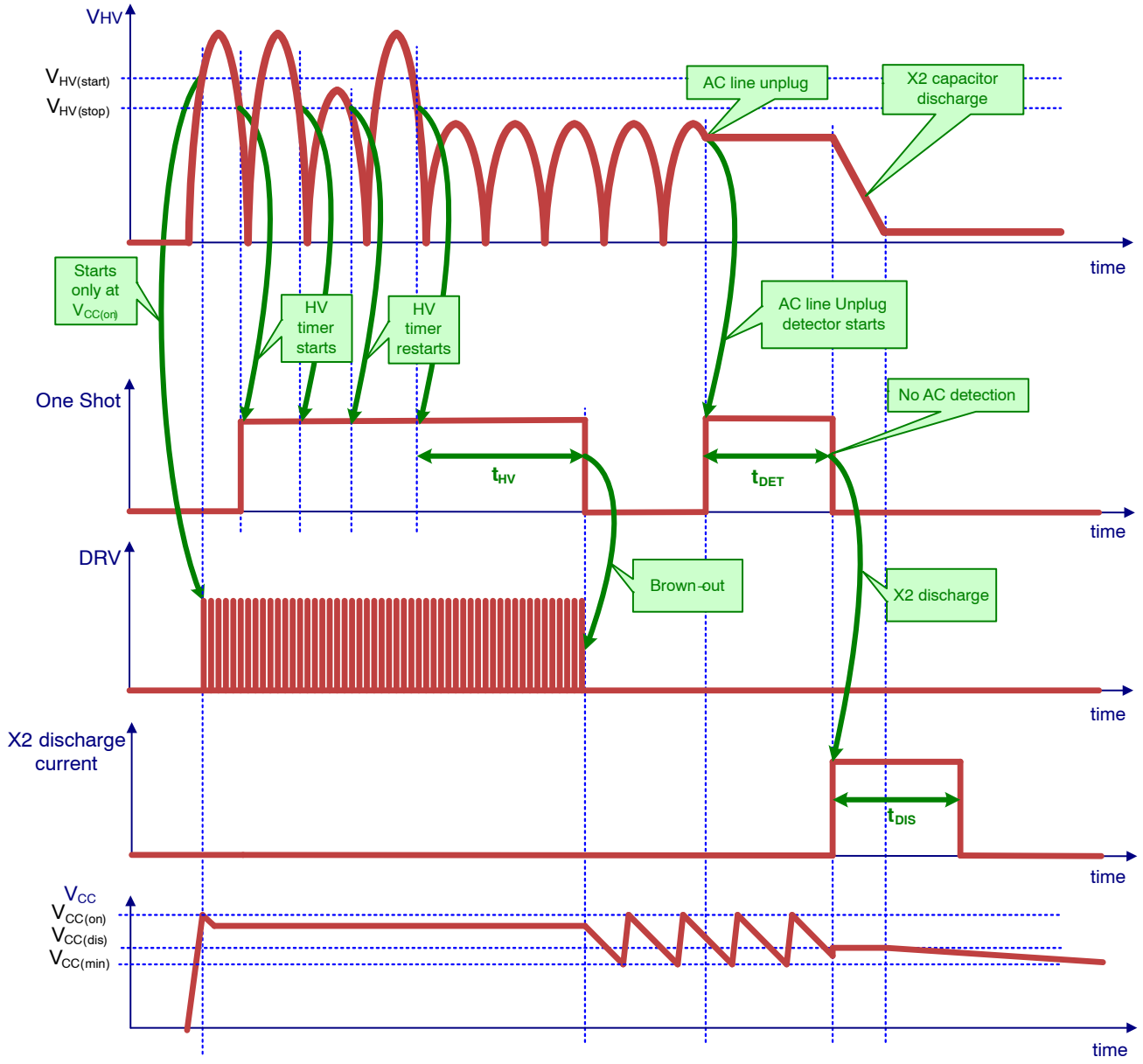


Figure 54. HV Pin ac Input Timing Diagram with X2 Capacitor Discharge Sequence when the Application is Unplugged Under Extremely Low Line Condition

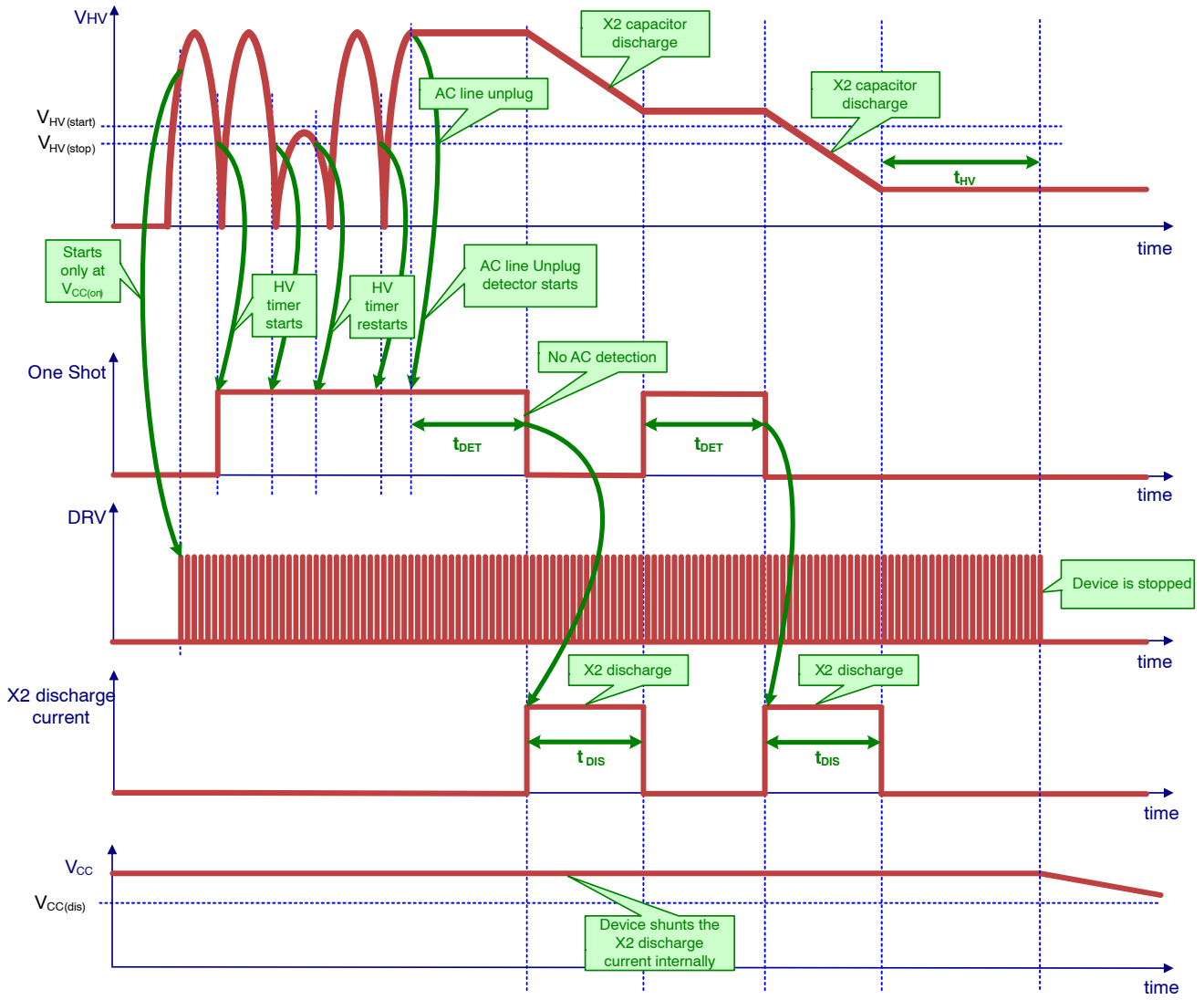


Figure 55. HV Pin ac Input Timing Diagram with X2 Capacitor Discharge Sequence When the Application is Unplugged Under High Line Condition

The Low Consumption Off Mode

There was implemented the low consumption off mode allowing to reach extremely low no load input power as described in previous chapters. If the voltage at feedback pin decreases below the 0.6 V the controller enters the off mode. The internal V_{CC} is turned−off, the IC consumes extremely low V_{CC} current and only the voltage at external V_{CC} capacitor is maintained by the Dynamic Self−Supply circuit. The Dynamic Self−Supply circuit keeps the V_{CC} voltage between the $V_{CC(on)}$ and $V_{CC(off)}$ levels. The supply for the FB pin watch dog circuitry and FB pin bias is provided via the low consumption current sources from the external V_{CC} capacitor. The controller can only start, if the FB pin voltage increases above the 2.2 V level. See Figure 56 for timing diagrams.

Only the X2 cap discharge and Self−Supply features is enabled in the low consumption off mode. The X2 cap discharging feature is enable due the safety reasons and the Self−Supply is enabled to keep the V_{CC} supply, but only very low V_{CC} consumption appears in this mode. Any other features are disabled in this mode.

The information about the latch status of the device is kept in the low consumption off mode and this mode is used for the TSD protection as well. The protection timer GoToOffMode t_{GTOM} is used to protect the application against the false activation of the low consumption off mode by the fast drop outs of the FB pin voltage below the 0.4 V level. E.g. in case when is present high FB pin voltage ripple during the skip mode.

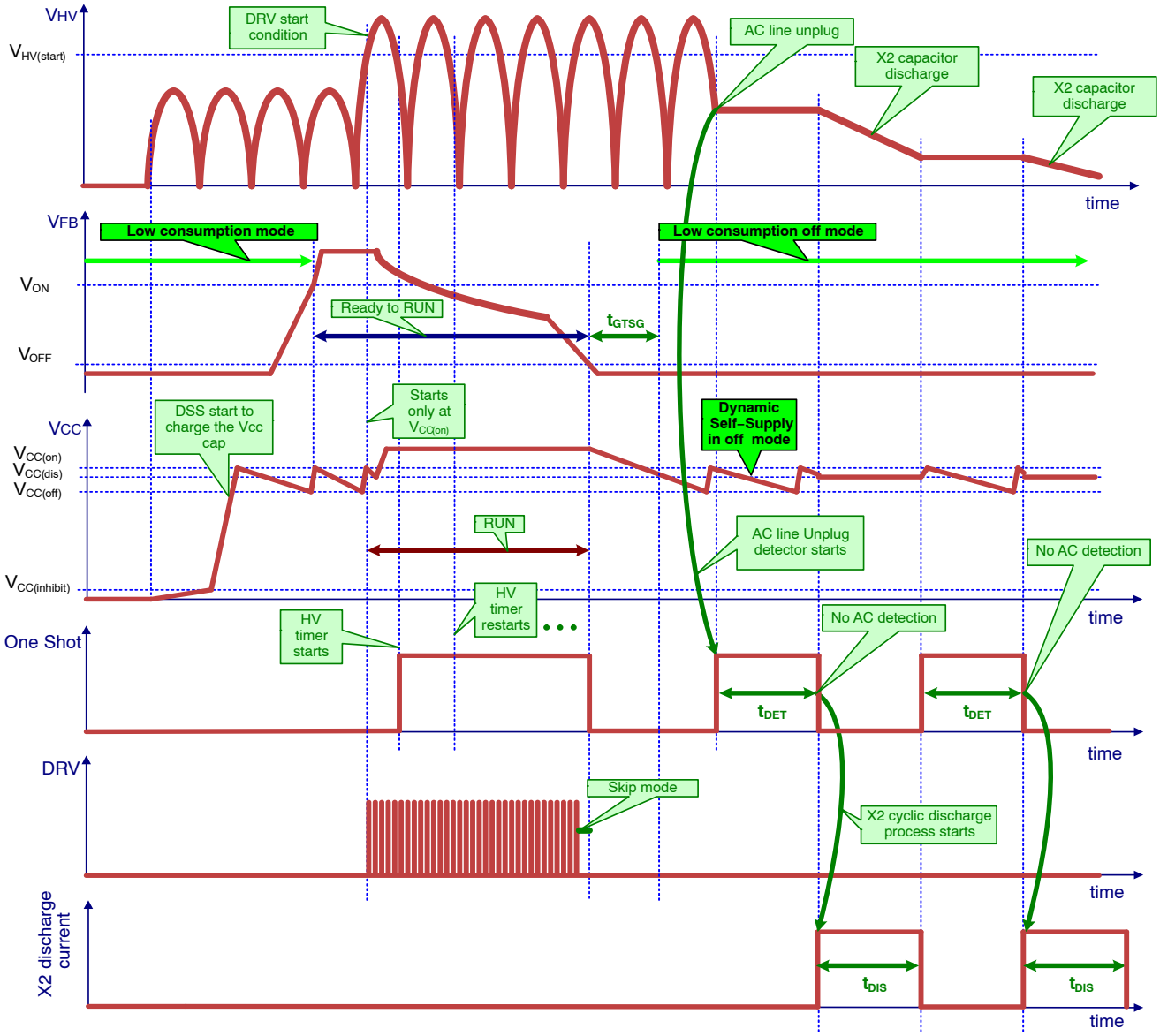


Figure 56. Start−up, Shut−down and AC Line Unplug Time Diagram

Oscillator with Frequency Jittering

The NCP12400 includes an oscillator that sets the switching frequency 65 kHz or 100 kHz depending on the version. The maximum duty−ratio of the DRV pin is 80%. In order to improve the EMI signature, the switching frequency jitters ±4 kHz around its nominal value, with a triangle−wave shape and at a frequency of 125 Hz. This frequency jittering is active even when the frequency is decreased to improve the efficiency in light load condition.

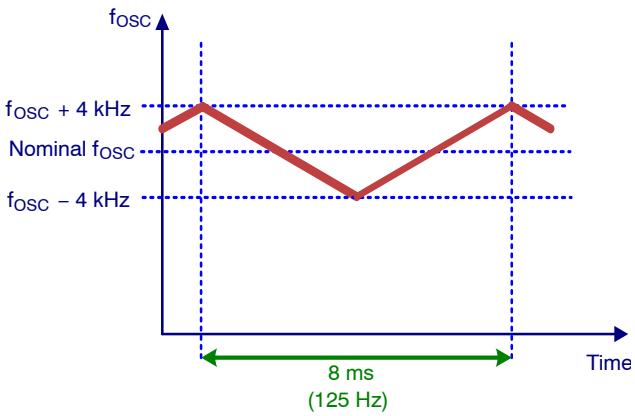


Figure 57. Frequency Modulation of the Maximum Switching Frequency

Low Load Operation Modes: Frequency Foldback Mode (FFM) and Skip Mode

In order to improve the efficiency in light load conditions, the frequency of the internal oscillator is linearly reduced from its nominal value down to $f_{OSC(min)}$. This frequency foldback starts when the voltage on FB pin goes below Vfb(foldS), and is complete when Vfb reaches Vfb(foldE). The maximum on−time duration control is kept during the frequency foldback mode to provide the natural transformer core anti−saturation protection. The frequency jittering is still active while the oscillator frequency decreases as well. The current setpoint is fixed to 300 mV in the frequency foldback mode if the feedback voltage decreases below the Vfb(freeze) level. This feature increases efficiency under the light loads conditions as well.

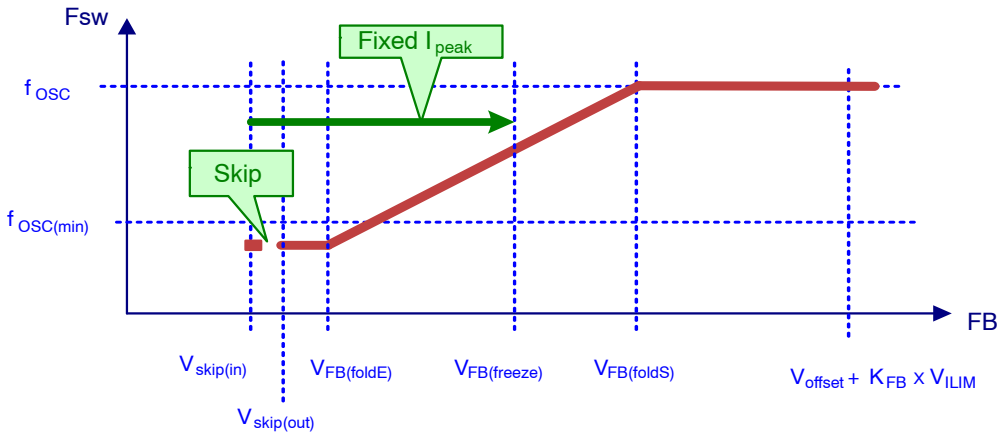


Figure 58. Frequency Foldback Mode Characteristic

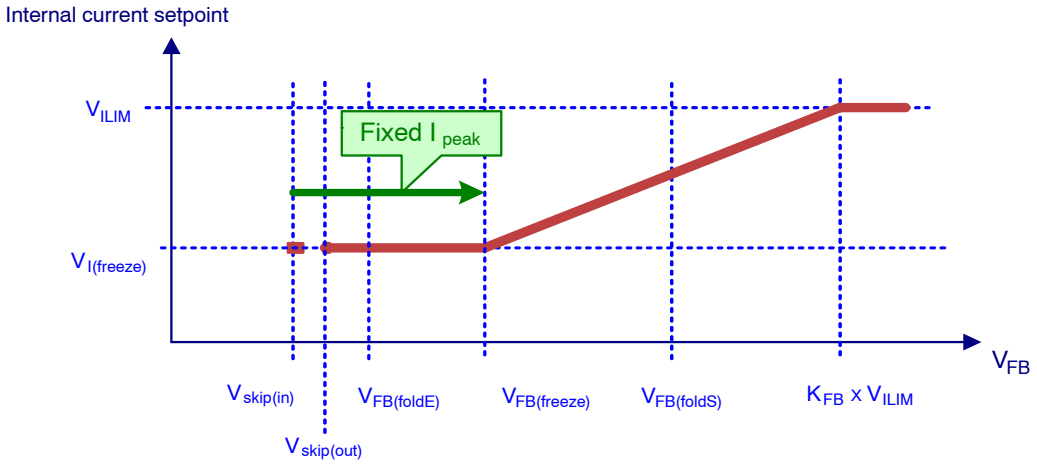


Figure 59. Current Setpoint Dependency on the Feedback Pin Voltage

When the FB voltage reaches $V_{skip(in)}$ while decreasing, skip mode is activated: the driver stops, and the internal consumption of the controller is decreased. While V_{FB} is below $V_{skip(out)}$, the controller remains in this state; but as soon as V_{FB} crosses the skip out threshold, the DRV pin starts to pulse again.

The NCP12400 device includes logic which allows going into skip mode after the DRV cycle is finished by reaching of the peak current value. This technique eliminates the last short pulses in skip mode, which increases the system efficiency at light loads and makes easier the application of active secondary rectification circuitry.

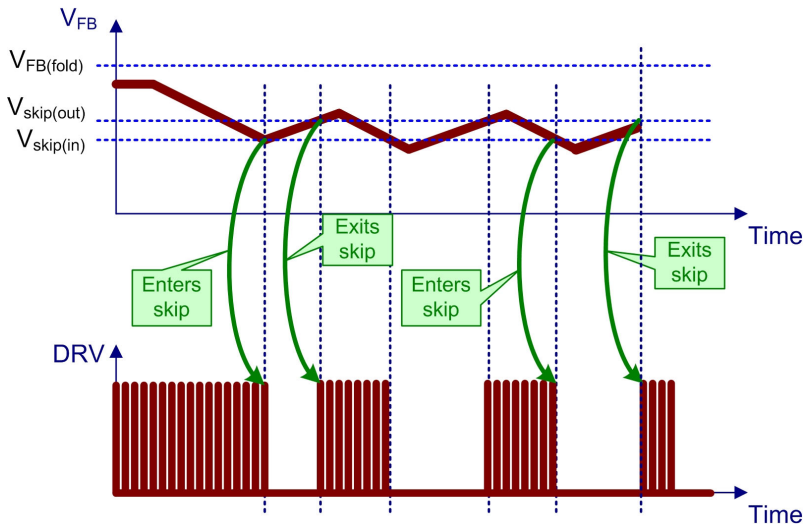


Figure 60. Skip Mode Timing Diagram

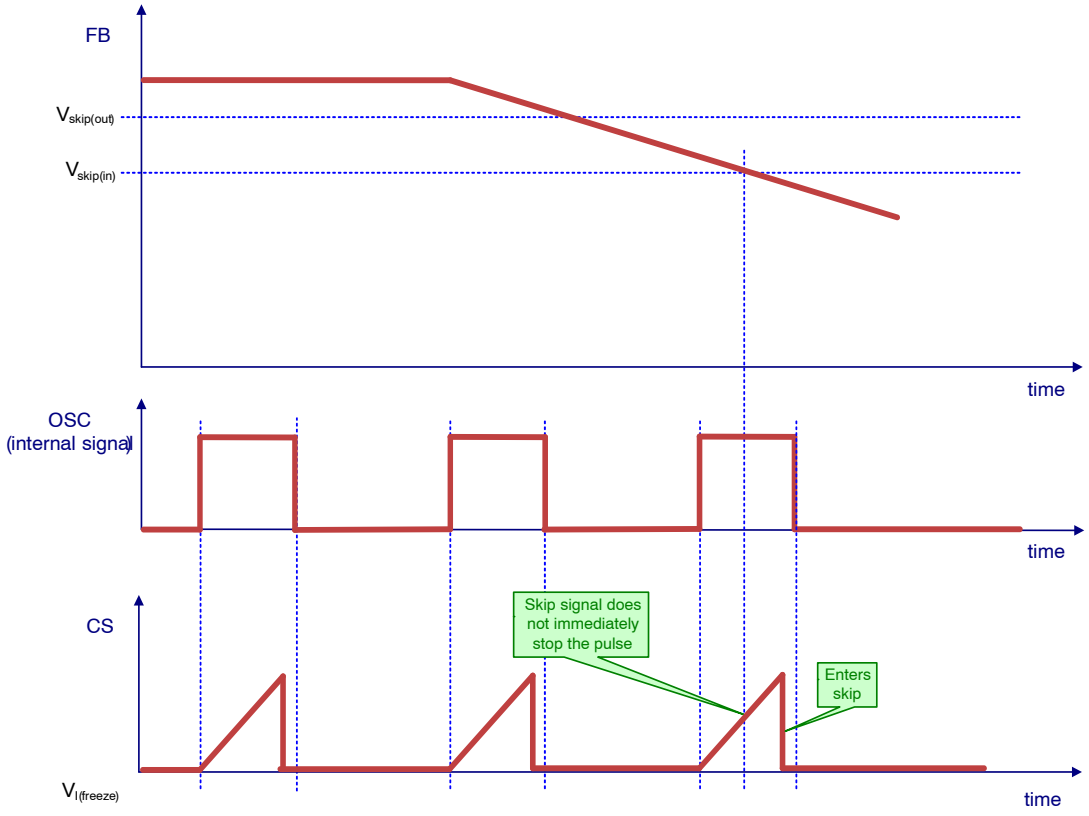


Figure 61. Technique Preventing Short Pulses in Skip Mode

Quiet−Skip

To further avoid acoustic noise, the circuit prevents the burst frequency during skip mode from entering the audible range by limiting it to a maximum of 800 Hz. This is achieved via a timer t_{quiet} that is activated during Quiet−Skip. The start of the next burst cycle is prevented until this timer has expired. As the output power decreases, the switching frequency decreases. Once it hits minimum switching frequency $f_{OSC(min)}$, the skip−in threshold is reached and burst mode is entered – switching stops as soon as the current drive pulses ends – it does not stop immediately.

Once switching stops, FB will rise. As soon as FB crosses the skip−exit threshold, drive pulses will resume, but the controller remains in burst mode. At this point, a 1250 μs (typ) timer t_{quiet} is started together with a count to $n_{P,skip}$ pulses counter. This $n_{P,skip}$ pulses counter ensures the minimum number of DRV signal pulses in burst. The next time the FB voltage drops below the skip−in threshold, DRV pulses stop at the end of the current pulse as long as $n_{P,skip}$ drive pulses have been counted (if not, they do not stop until the end of the $n_{P,skip}$ −th pulse). They are not allowed to start again until the timer expires, even if the skip−exit threshold is reached first. It is important to note that the timer will not force the next cycle to begin – i.e. if the natural skip frequency is such that skip−exit is reached after the timer expires, the drive pulses will wait for the skip−exit threshold.

This means that during no−load, there will be a minimum of $n_{P,skip}$ drive pulses, and the burst−cycle period will likely be much longer than 1250 μs. This operation helps to improve efficiency at no−load conditions.

In order to exit burst mode, the FB voltage must rise higher than $V_{skip(tran)}$ level. If this occurs before t_{quiet} expires, the drive pulses will resume immediately – i.e. the controller won't wait for the timer to expire. Figure 63 provides an example of how Quiet−Skip works, while Figure 62 shows the immediate leaving the quiet skip mode by crossing the transient enhancement level $V_{skip(tran)}$.

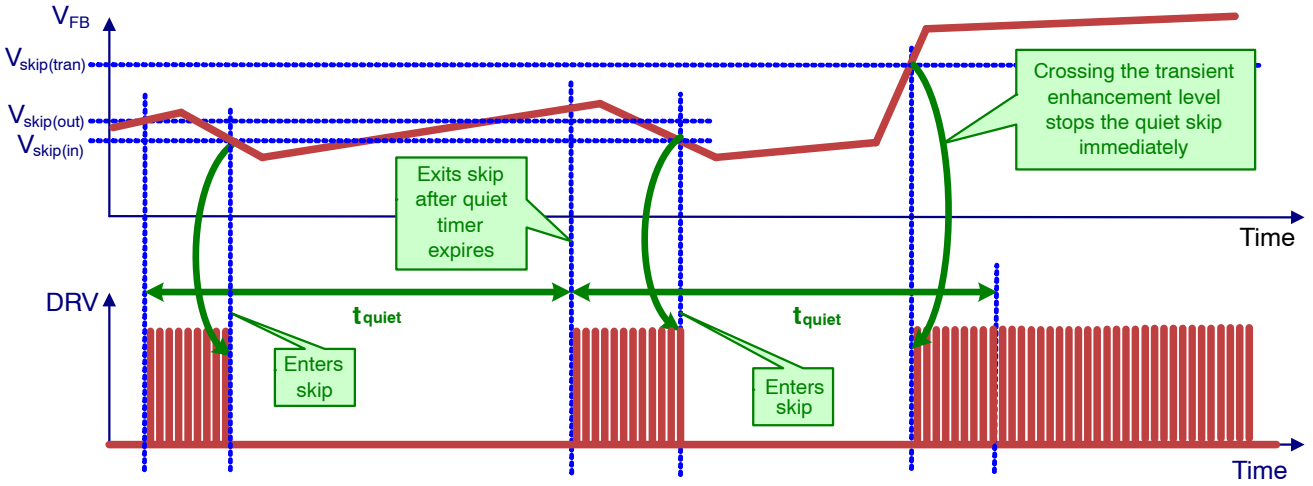


Figure 62. Leaving the Quiet−Skip Mode during Load Transient

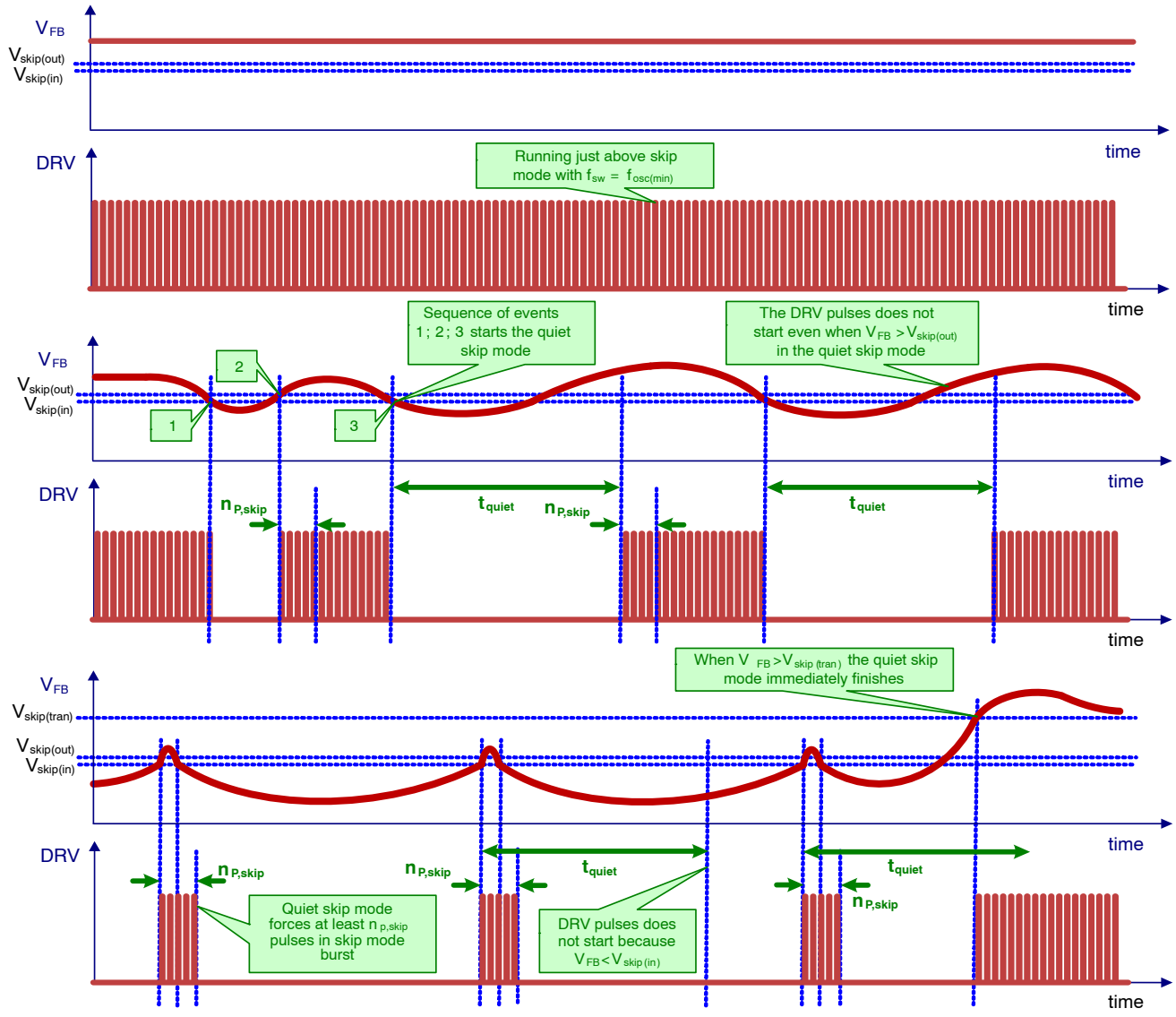


Figure 63. Quiet−Skip Timing Diagram − option

Clamped Driver

The supply voltage for the NCP12400 can be as high as 36 V, but most of the MOSFETs that will be connected to the DRV pin cannot accept more than 20 V on their gate. The driver pin is therefore safely clamped below 16 V. This driver has a typical capability of 500 mA for source current and 800 mA for sink current.

Current−Mode Control With Slope Compensation and Soft−Start

NCP12400 is a current−mode controller, which means that the FB voltage sets the peak current flowing in the transformer primary inductance and the MOSFET. This is done through a PWM comparator: the current is sensed across a resistor and the resulting voltage is applied to the CS pin. It is applied to one input of the PWM comparator through a 250 ns LEB block. On the other input the FB voltage subducted by offset typically 0.8 V and divided by 4 sets the threshold: when the voltage ramp reaches this threshold, the output driver is turned off. The maximum value for the current sense is 0.7 V, and it is set by a dedicated comparator.

Each time the controller is starting, i.e. the controller was off and starts – or restarts – when V_{CC} reaches $V_{CC(on)}$, a soft−start is applied: the current sense set−point is increased by 32 discrete steps from 0 (the minimum level can be higher than 0 because of the LEB and propagation delay) until it reaches V_{ILIM} (after a duration of t_{SSTART}), or until the FB loop imposes a setpoint lower than the one imposed by the soft−start (the 2 comparators outputs are OR'ed).

During the soft−start the oscillator frequency increase from the minimum switching frequency to the maximum switching frequency following the ramp applied to current sense set−point.

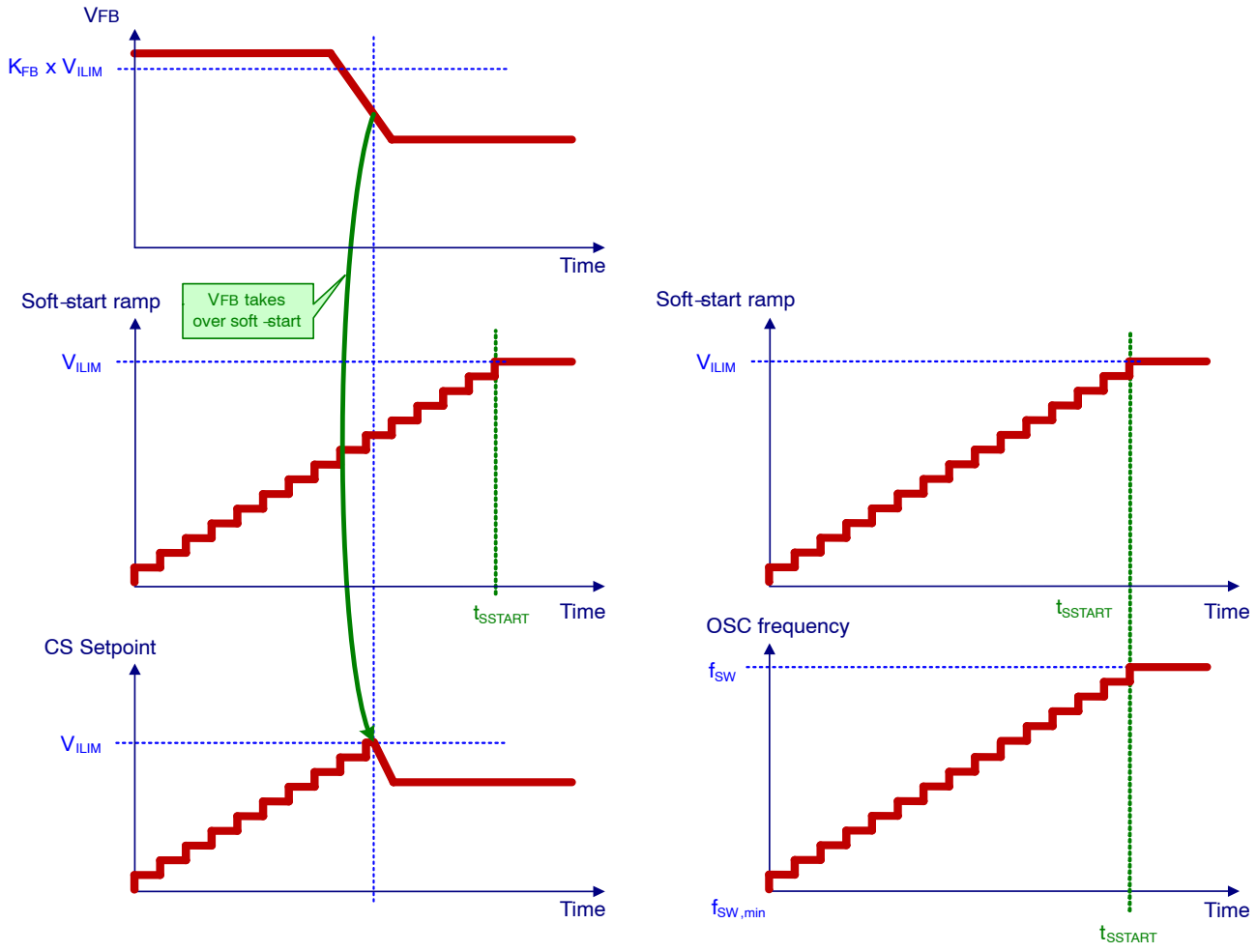


Figure 64. Soft−Start Feature

Under some conditions, like a winding short−circuit for instance, not all the energy stored during the on−time is transferred to the output during the off−time, even if the on−time duration is at its minimum (imposed by the propagation delay of the detector added to the LEB duration). As a result, the current sense voltage keeps on increasing above V_{ILIM}, because the controller is blind during the LEB blanking time. Dangerously high current can grow in the system if nothing is done to stop the controller. That's what the additional comparator, that senses when the current sense voltage on CS pin reaches $V_{CS(stop)}$ (= 1.5 x V_{ILIM}), does: as soon as this comparator toggles, the controller immediately enters the protection mode.

In order to allow the NCP12400 to operate in CCM with a duty−ratio above 50%, the fixed slope compensation is internally applied to the current−mode control. The slope appearing on the internal voltage setpoint for the PWM comparator is −32.5 mV/μs typical. The slope compensation can be observable as a value of the peak current at CS pin. The internal slope compensation circuitry uses a saw−tooth signal synchronized with the internal oscillator is subtracted from the FB voltage divided by K_{FB}.

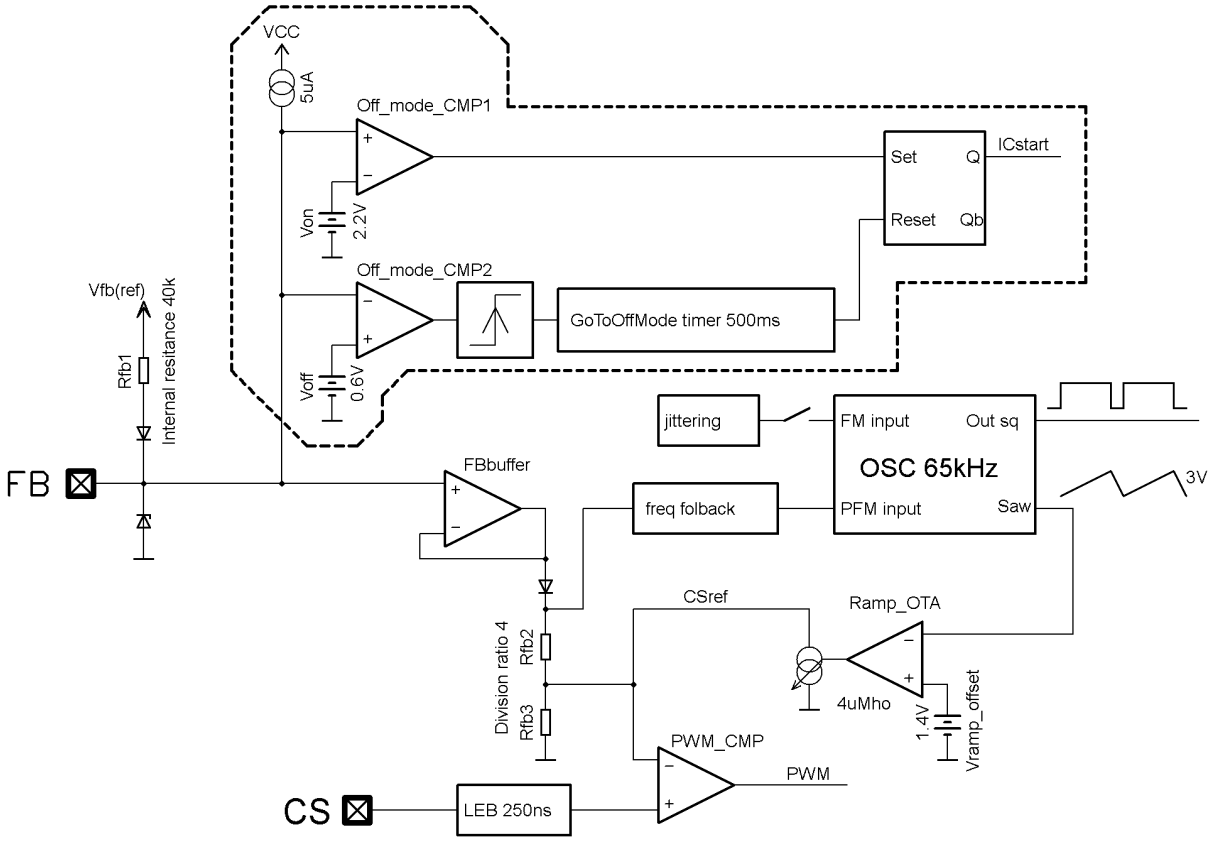


Figure 65. Slope Compensation Block Diagram

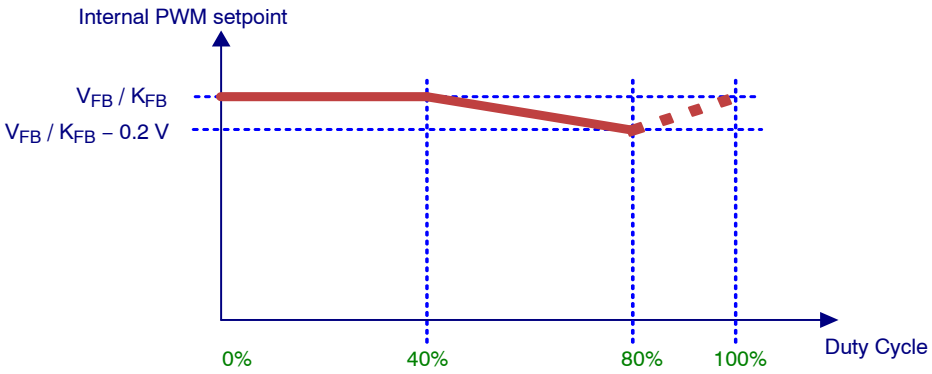


Figure 66. Slope Compensation Timing Diagram

Internal Overpower Protection

The power delivered by a flyback power supply is proportional to the square of the peak current in discontinuous conduction mode:

$$P_{OUT} = \frac{1}{2} \cdot \eta \cdot L_P \cdot F_{SW} \cdot I_P{}^2 \quad \text{(eq. 3)}$$

Unfortunately, due to the inherent propagation delay of the logic, the actual peak current is higher at high input voltage than at low input voltage, leading to a significant difference in the maximum output power delivered by the power supply.

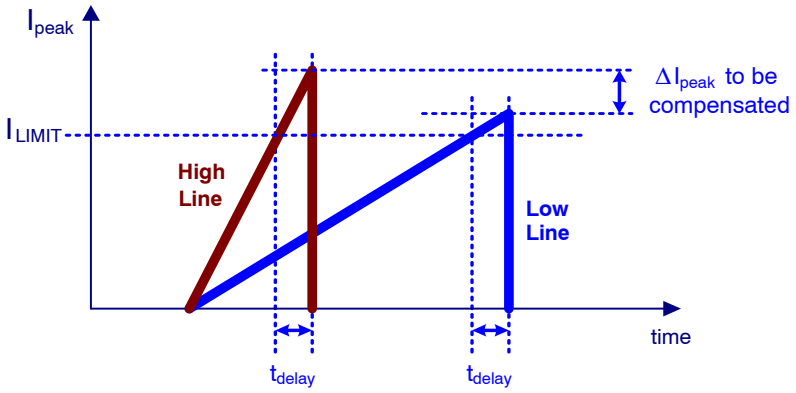


Figure 67. Needs for Line Compensation For True Overpower Protection

To compensate this and have an accurate overpower protection, an offset proportional to the input voltage is added on the CS signal by turning on an internal current source: by adding an external resistor in series between the sense resistor and the CS pin, a voltage offset is created across it by the current. The compensation can be adjusted by changing the value of the resistor.

But this offset is unwanted to appear when the current sense signal is small, i.e. in light load conditions, where it would be in the same order of magnitude. Therefore the compensation current is only added when the FB voltage is higher than $V_{FB(OPCE)}$. However, because the HV pin is being connected to ac voltage, there is needed an additional circuitry to read or at least closely estimate the actual voltage on the bulk capacitor.

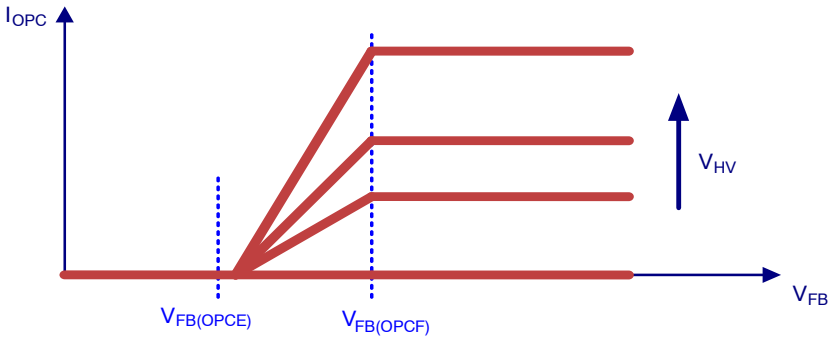


Figure 68. Overpower Protection Current Relation to Feedback Voltage

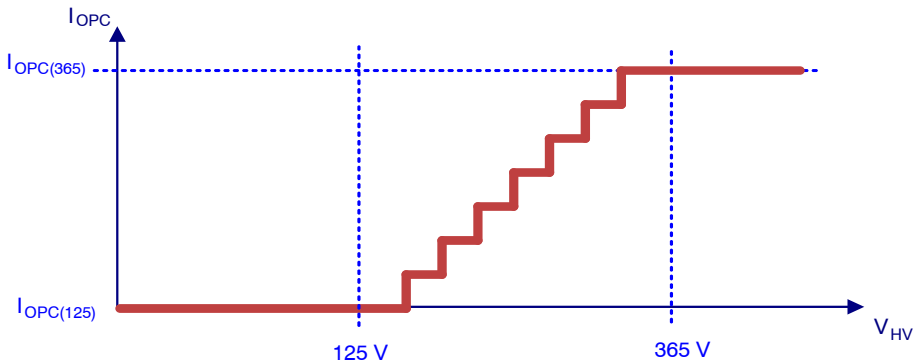


Figure 69. Overpower Protection Current Relation to Peak of Rectified Input Line AC voltage

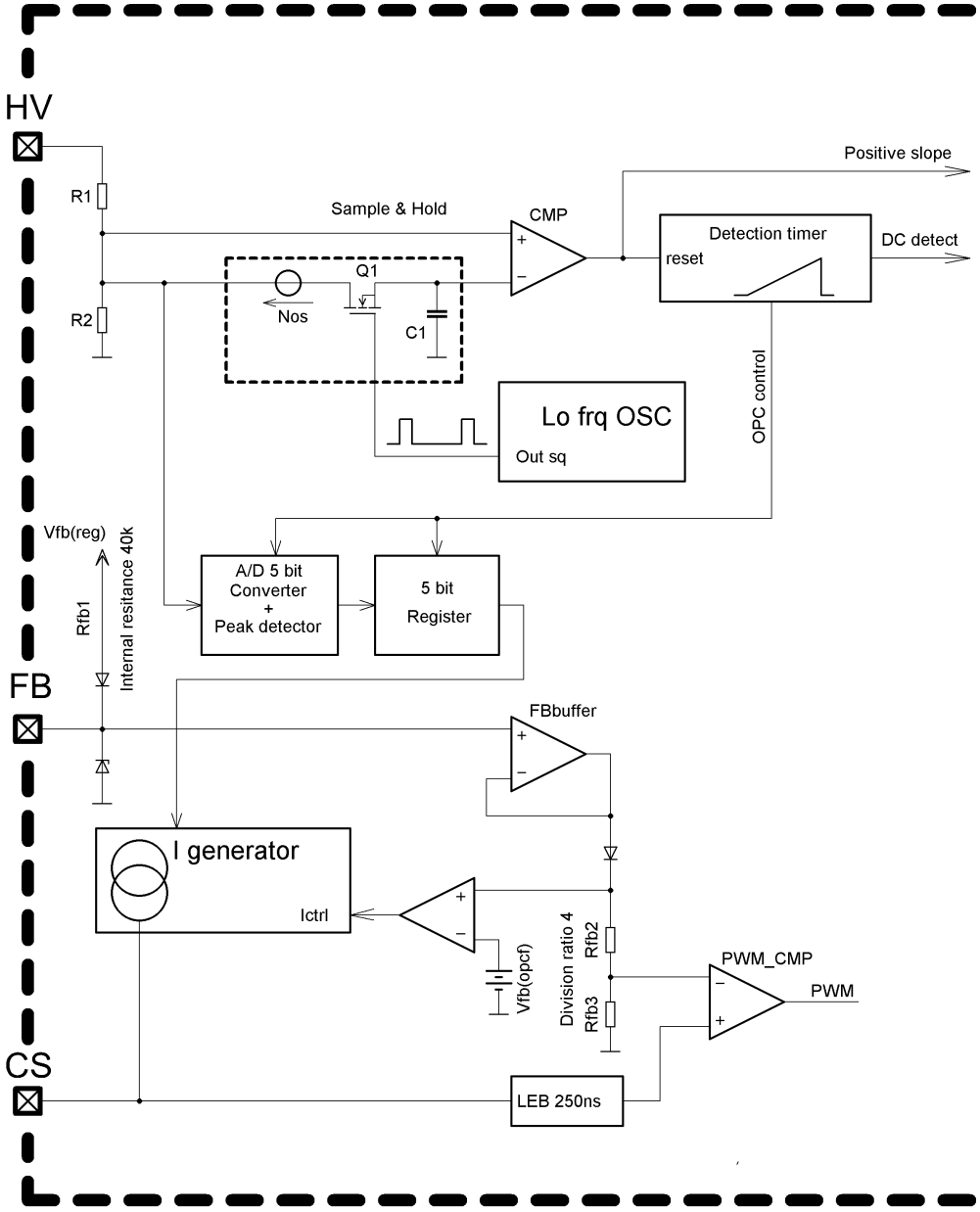


Figure 70. Block Schematic of Overpower Protection Circuit

A 5−bit A/D converter with the peak detector senses the ac input, and its output is periodically sampled and reset, in order to follow closely the input voltage variations. The sample and reset events are given by the output from the ac line unplug detector. The sensed HV pin voltage peak value is validated when no HV edges from comparator are present after last falling edge during 2 sample clocks. See Figure 71 for details.

Overcurrent Protection with Fault Timer

The overload protection depends only on the current sensing signal, making it able to work with any transformer, even with very poor coupling or high leakage inductance.

When an overcurrent occurs on the output of the power supply, the FB loop asks for more power than the controller can deliver, and the CS set−point reaches V_{ILIM}. When this event occurs, an internal t_{fault} timer is started: once the timer times out, DRV pulses are stopped and the controller is either latched off. This latch is released in autorecovery mode. The controller tries to restart after $t_{autorec}$. The other possibilities of the latch release are the brown−out condition or the VCC power on reset. The timer is reset when the CS set−point goes back below VILIM before the timer elapses. The fault timer is also started if the driver signal is reset by the maximum on time. The controller also enters the same protection mode if the voltage on the CS pin reaches 1.5 times the maximum internal set−point $V_{CS(stop)}$ (allows to detect winding short−circuits) or there appears low V_{CC} supply. See Figure 71 for the timing diagram.

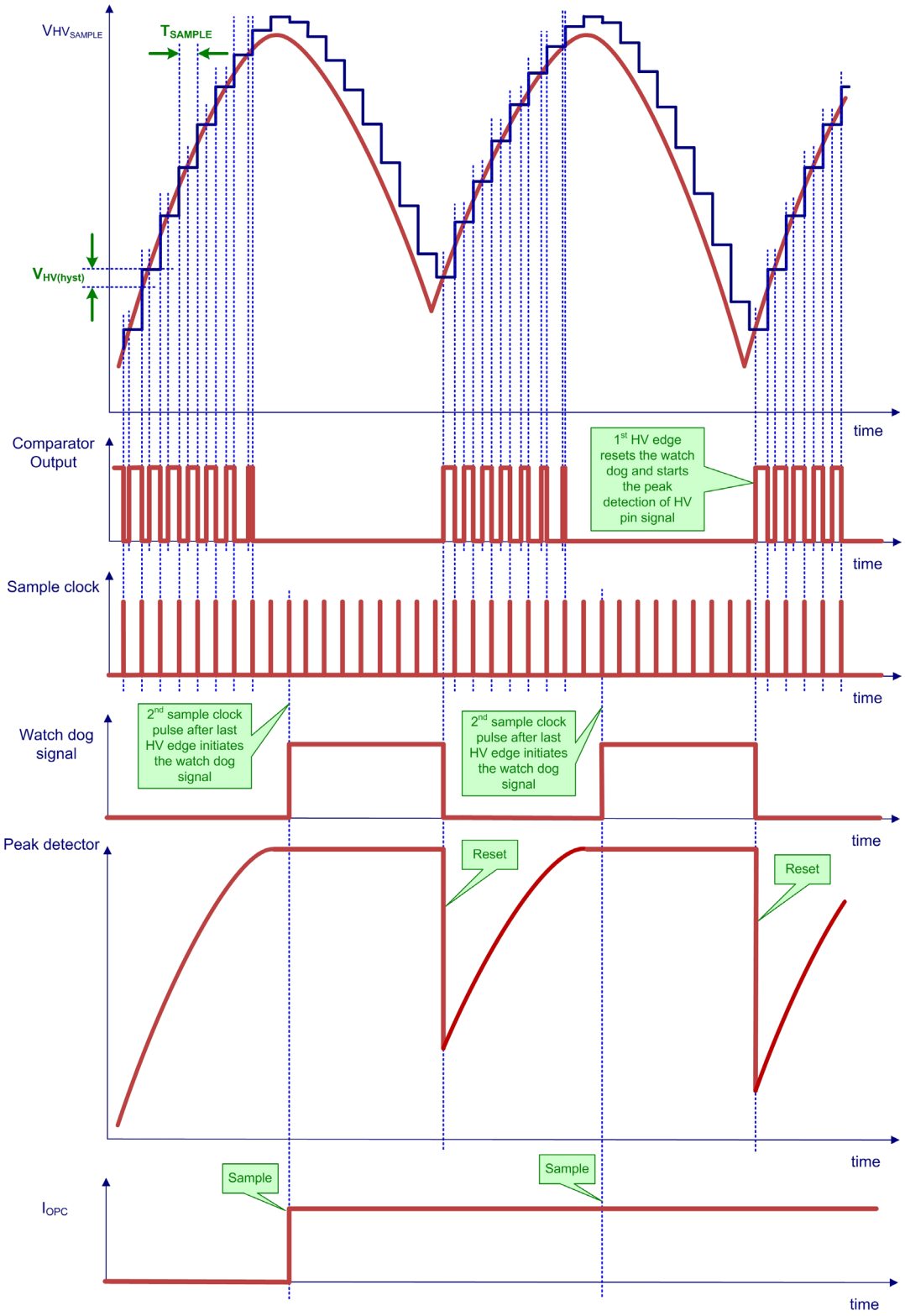


Figure 71. Overpower Compensation Timing Diagram

Table 6. PROTECTION MODES AND THE LATCH MODE RELEASES

Event	Timer Protection	Next Device Status	Release to Normal Operation Mode
Overcurrent $V_{CS} > V_{ILIM}$	Fault timer	Latch	Autorecovery Brown−out $V_{CC} < V_{CC(reset)}$
Maximum on time	Fault timer	Latch	Brown−out $V_{CC} < V_{CC(reset)}$
Maximum duty cycle	Fault timer	Latch	Brown−out $V_{CC} < V_{CC(reset)}$
Winding short $V_{CS} > V_{CS(stop)}$	4 consecutive pulses	Latch	Autorecovery Brown−out $V_{CC} < V_{CC(reset)}$
Low supply $V_{CC} < V_{CC(off)}$	10 μs timer	Latch	Autorecovery Brown−out $V_{CC} < V_{CC(reset)}$
External OTP, OVP	55 μs	Latch	Brown−out $V_{CC} < V_{CC(reset)}$
High supply $V_{CC} > V_{CC(ovp)}$	10 μs timer	Latch	Brown−out $V_{CC} < V_{CC(reset)}$
Brown−out $V_{HV} < V_{HV(stop)}$	HV timer	Device stops	$(V_{HV} > V_{HV(start)})$ & $(V_{CC} > V_{CC(on)})$
Internal TSD	10 μs timer	Device stops, HV start−up current source stops	$(V_{HV} > V_{HV(start)})$ & $(V_{CC} > V_{CC(on)})$ & TSDb
Off mode $V_{FB} < V_{OFF}$	500 ms timer	Device stops and internal V_{CC} is turned off	$(V_{HV} > V_{HV(start)})$ & $(V_{CC} > V_{CC(on)})$ & $(V_{FB} > V_{ON})$

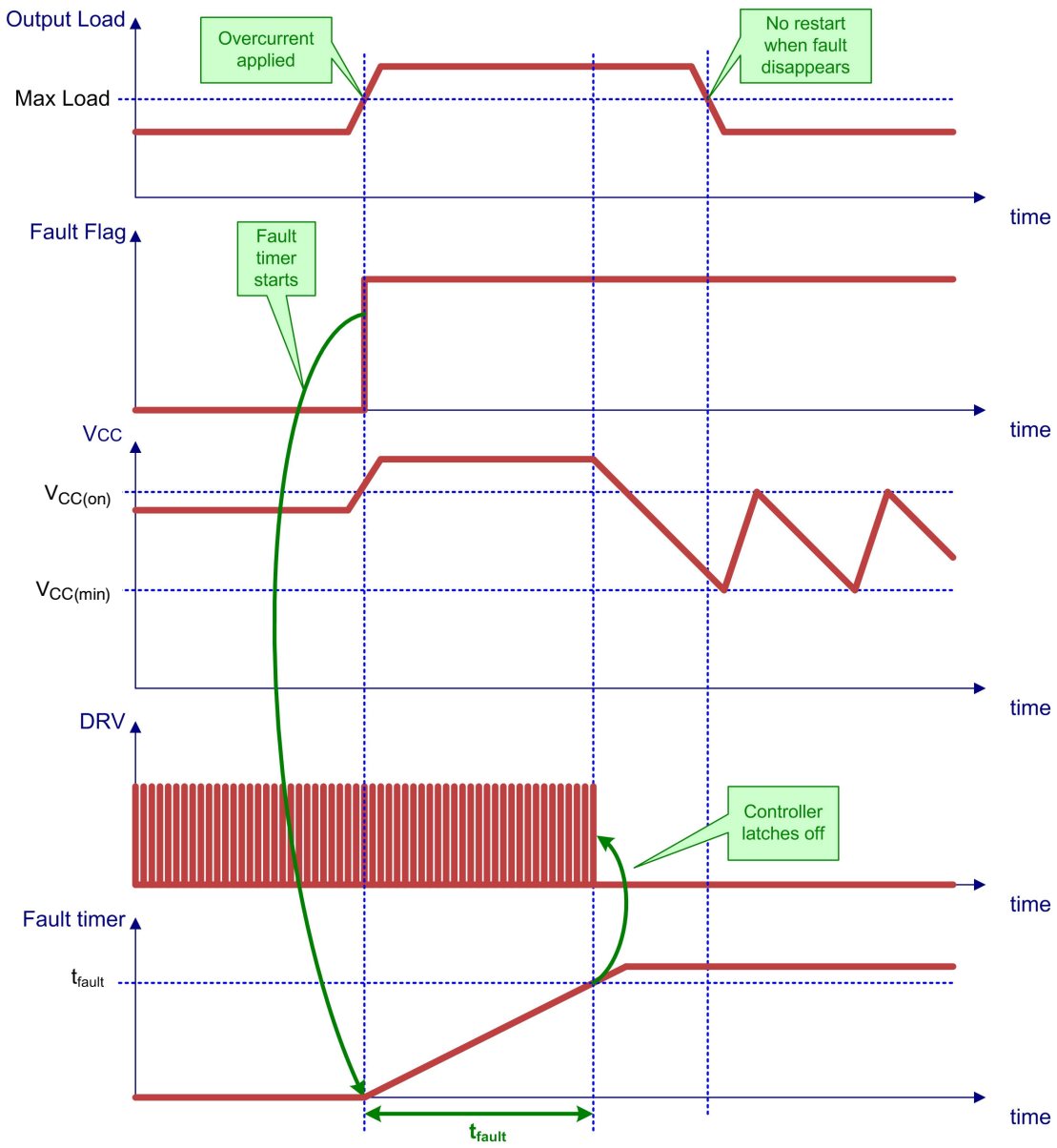


Figure 72. Latched Timer−Based Overcurrent Protection

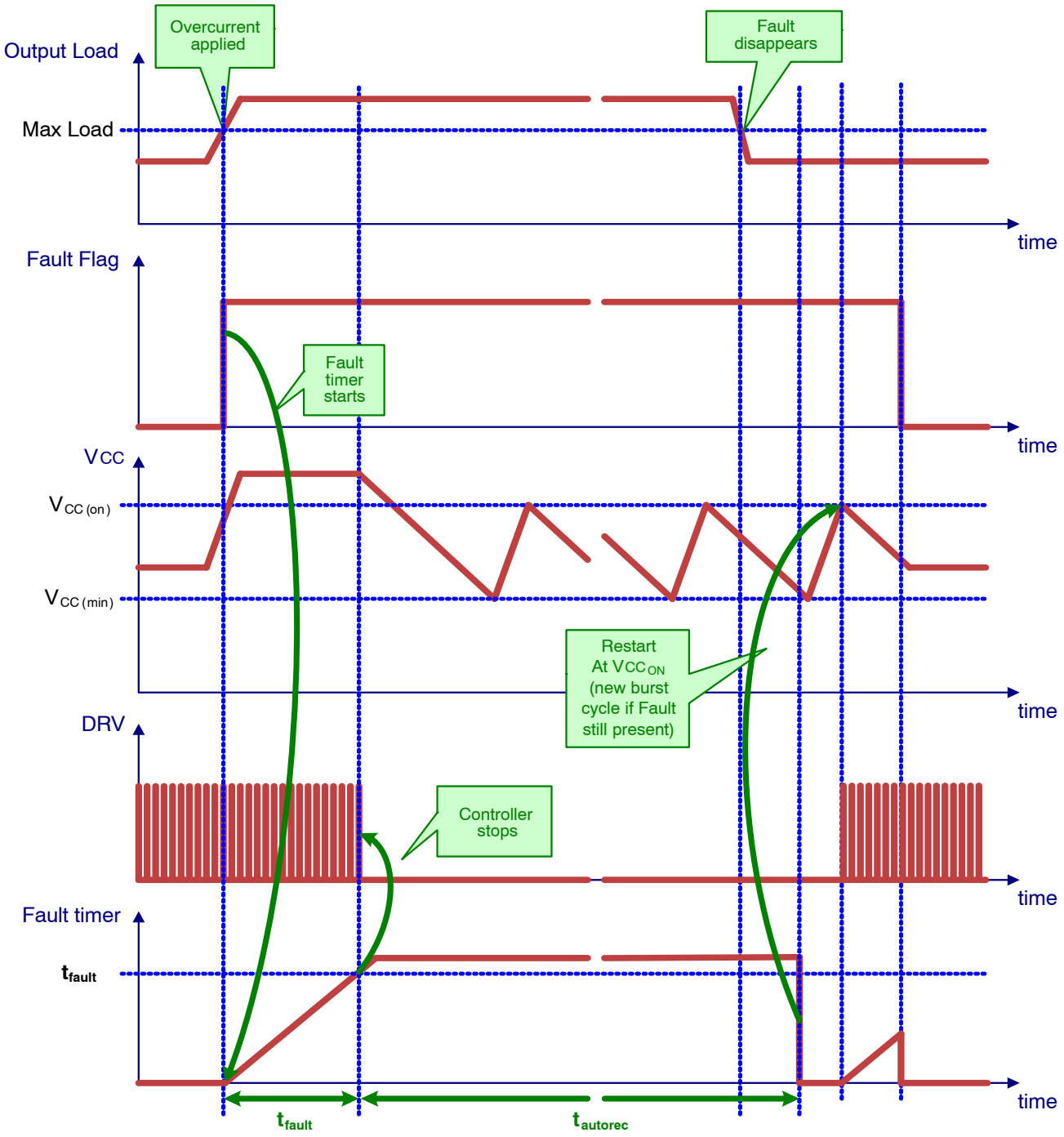


Figure 73. Timer−based Protection Mode with Autorecovery Release from Latch−off

FAULT Input

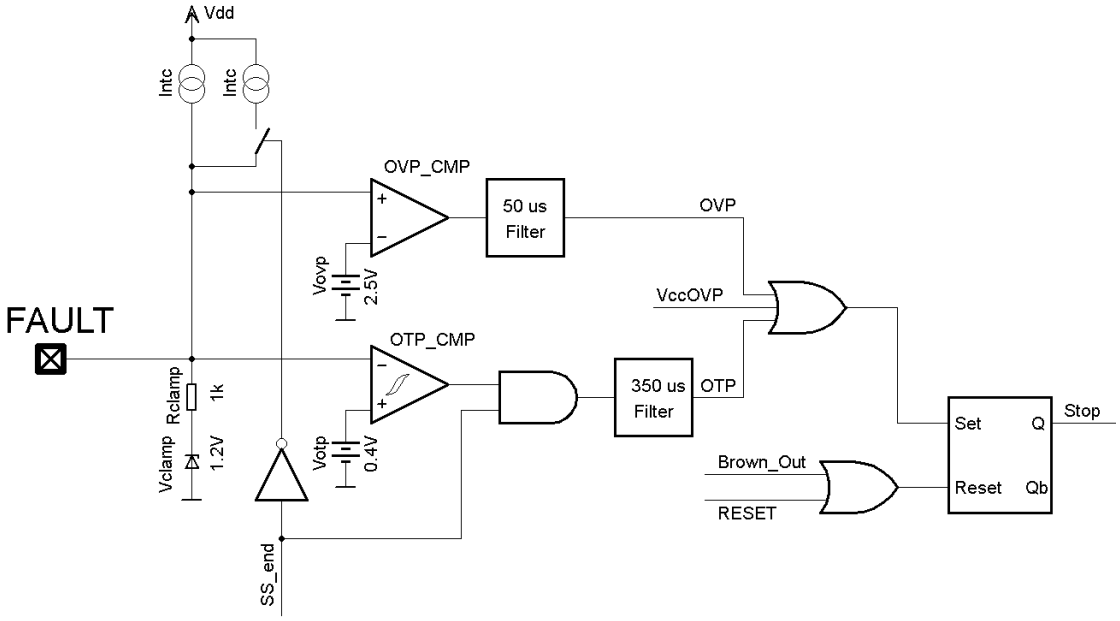


Figure 74. OVP/OTP Detection Schematic

The FAULT input pin is dedicated to the latch−off function: it includes 2 levels of detection that define a working window, between a high latch and a low latch: within these 2 thresholds, the controller is allowed to run, but as soon as either the low or the high threshold is crossed, the controller is latched off. The controller can be released from the latch mode by the autorecovery, but it depends on the version of the product. The lower threshold is intended to be used with an NTC thermistor, thanks to an internal current source I_{NTC}.

An active clamp prevents the voltage from reaching the high threshold if it is only pulled up by the I_{NTC} current. To reach the high threshold, the pull−up current has to be higher than the pull−down capability of the clamp (typically 1.5 mA at V_{OVP}).

To avoid any false triggering, spikes shorter than 50 μs (for the high latch and 65 kHz version) or 350 μs (for the low latch) are blanked and only longer signals can actually latch the controller.

Reset occurs when a brown−out condition is detected or the V_{CC} is cycled down to a reset voltage, which in a real application can only happen if the power supply is unplugged from the ac line.

Upon startup, the internal references take some time before being at their nominal values; so one of the comparators could toggle even if it should not. Therefore the internal logic does not take the latch signal into account before the controller is ready to start: once V_{CC} reaches $V_{CC(on)}$, the latch pin High latch state is taken into account and the DRV switching starts only if it is allowed; whereas the Low latch (typically sensing an over temperature) is taken into account only after the soft−start is finished. In addition, the NTC current is doubled to $I_{NTC(SSTART)}$ during the soft−start period, to speed up the charging of the FAULT pin capacitor The maximum value of FAULT pin capacitor is given by the following formula (The standard start−up condition is considered and the NTC current is neglected):

$$C_{FAULT\ max} = \frac{t_{SSTART\ min} \cdot I_{NTC(SSTART)\ min}}{V_{OTP\ max}} = \frac{3.2 \cdot 10^{-3} \cdot 60 \cdot 10^{-6}}{0.420} F = 457\ nF \quad \text{(eq. 4)}$$

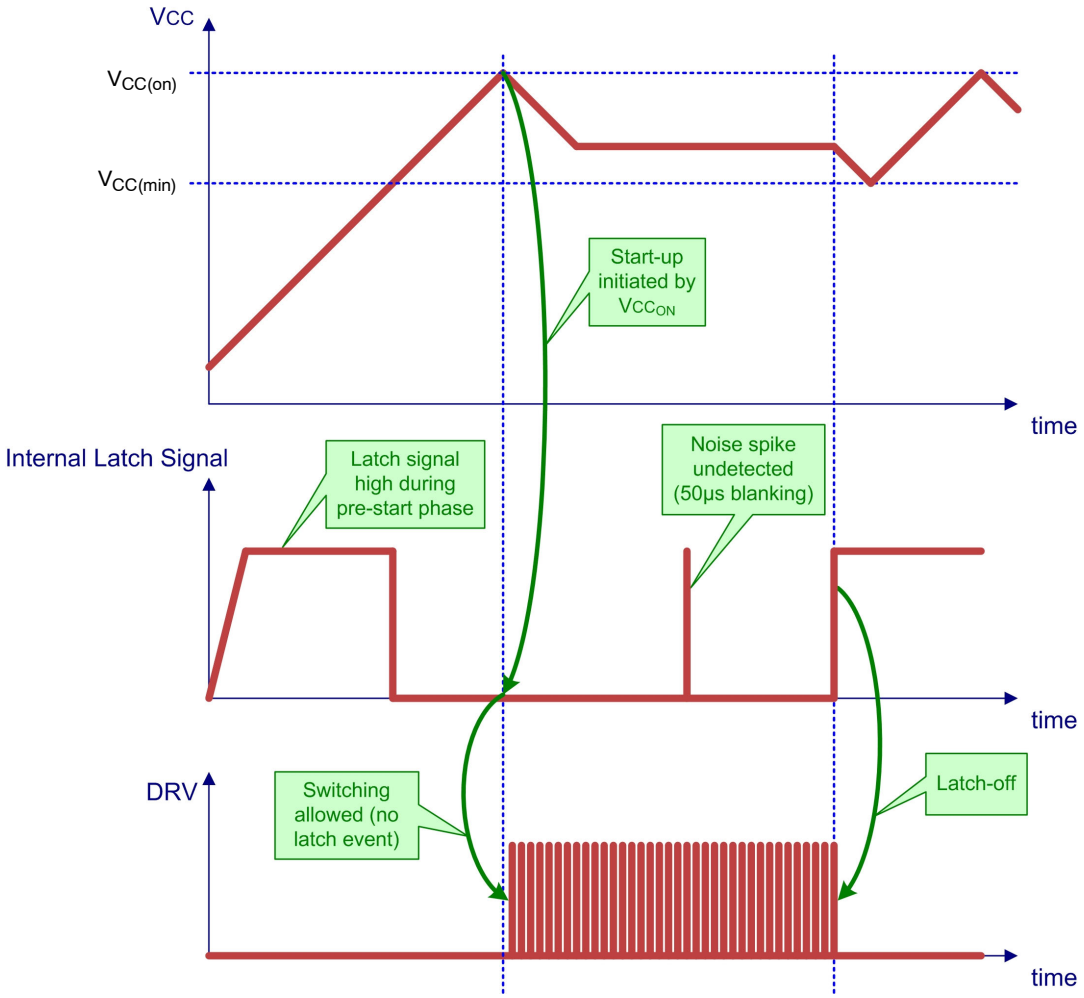


Figure 75. Latch Timing Diagram

Temperature Shutdown

The NCP12400 includes a temperature shutdown protection with a trip point typically at 150°C and the typical hysteresis of 30°C. When the temperature rises above the high threshold, the controller stops switching instantaneously, and goes to the off mode with extremely low power consumption. There is kept the V_{CC} supply to keep the TSD information. When the temperature falls below the low threshold, the start−up of the device is enabled again, and a regular start−up sequence takes place. See the status diagrams at the Figure 44.

ORDERING INFORMATION

Ordering Part No.	Overload Protection	Switching Frequency	Package	Shipping†
NCP12400BAHAB0DR2G	Latched	65 kHz	SOIC−7 (Pb−Free)	2500 / Tape & Reel
NCP12400BAHBB0DR2G	Latched	65 kHz		
NCP12400BBBBB2DR2G	Autorecovery	65 → 100 kHz		
NCP12400BBHAA1DR2G	Autorecovery	100 kHz		
NCP12400CAHAB0DR2G	Latched	65 kHz		
NCP12400CBAAB0DR2G	Autorecovery	65 kHz		
NCP12400CBBAB0DR2G	Autorecovery	65 kHz		
NCP12400CBHAA0DR2G	Autorecovery	65 kHz		
NCP12400EAHBB0DR2G	Latched	65 kHz		
NCP12400BBBBA0DR2G	Autorecovery	65 kHz		
NCP12400BBHAB0DR2G	Autorecovery	65 kHz		
NCP12400BBEBA0DR2G	Autorecovery	65 kHz		
NCP12400BBAAA0DR2G	Autorecovery	65 kHz		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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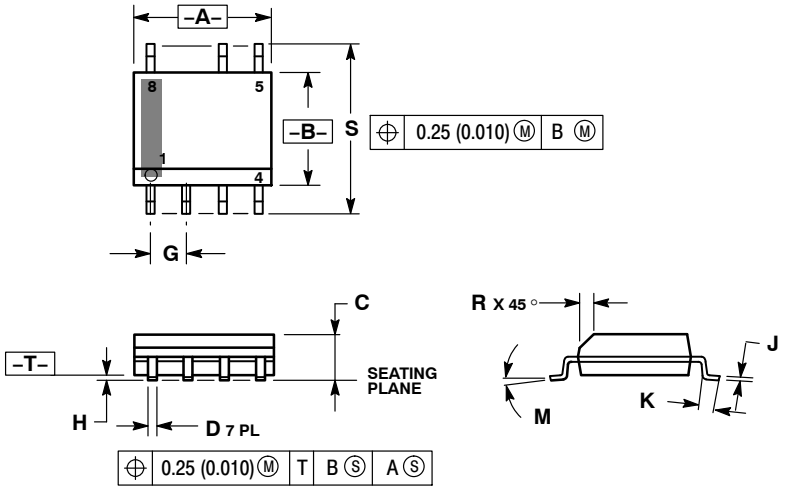
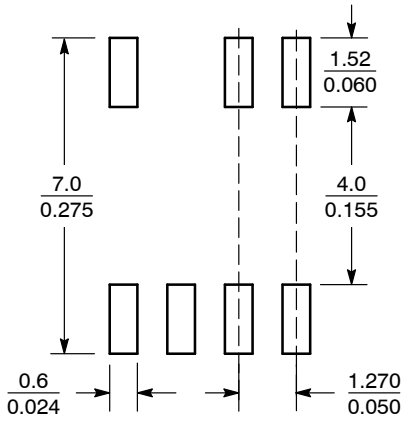
SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B ARE DATUMS AND T IS A DATUM SURFACE.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

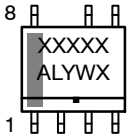
SOLDERING FOOTPRINT*



SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM



XXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLES ON PAGE 2

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STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6.
7. NOT USED
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. NOT USED
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. NOT USED
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. NOT USED
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5.
6.
7. NOT USED
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6.
7. NOT USED
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. NOT USED
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR (DIE 1)
2. BASE (DIE 1)
3. BASE (DIE 2)
4. COLLECTOR (DIE 2)
5. COLLECTOR (DIE 2)
6. EMITTER (DIE 2)
7. NOT USED
8. COLLECTOR (DIE 1)

STYLE 9:
PIN 1. EMITTER (COMMON)
2. COLLECTOR (DIE 1)
3. COLLECTOR (DIE 2)
4. EMITTER (COMMON)
5. EMITTER (COMMON)
6. BASE (DIE 2)
7. NOT USED
8. EMITTER (COMMON)

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. NOT USED
8. GROUND

STYLE 11:
PIN 1. SOURCE (DIE 1)
2. GATE (DIE 1)
3. SOURCE (DIE 2)
4. GATE (DIE 2)
5. DRAIN (DIE 2)
6. DRAIN (DIE 2)
7. NOT USED
8. DRAIN (DIE 1)

PUBLICATION ORDERING INFORMATION

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