

- U\_B12  
B12.SchDoc
- U\_B13  
B13.SchDoc
- U\_B14  
B14.SchDoc
- U\_B15  
B15.SchDoc
- U\_B16  
B16.SchDoc
- U\_B34  
B34.SchDoc

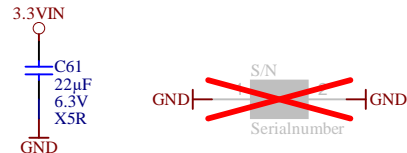
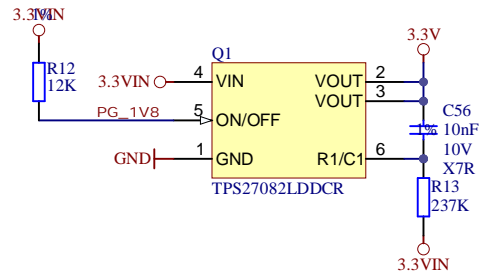
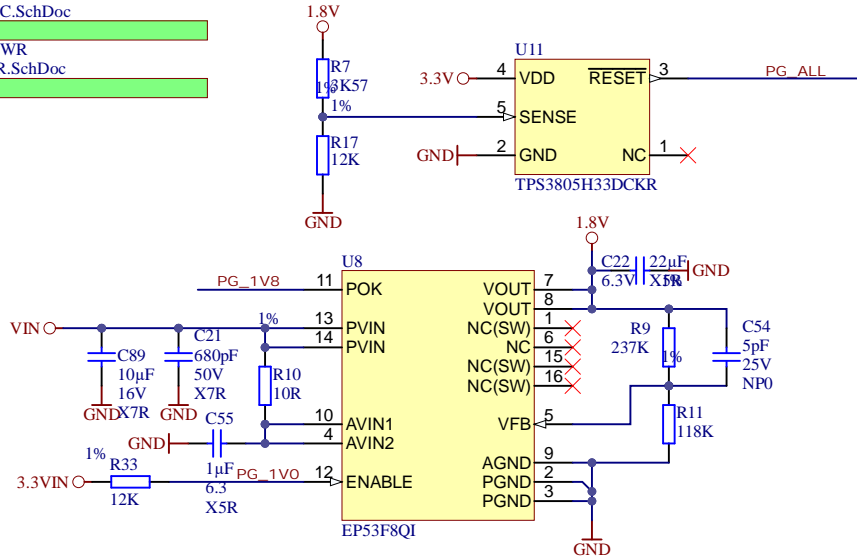
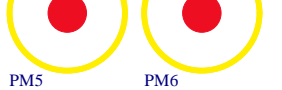
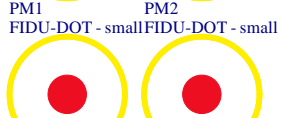
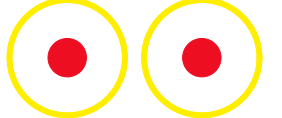
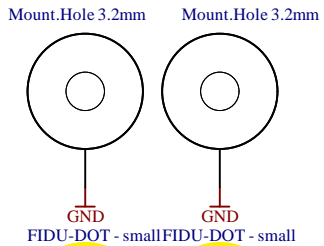
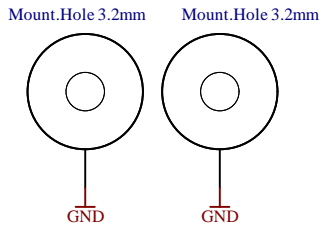
- U\_FPGA-MGT  
FPGA-MGT.SchDoc
- U\_FPGA-CFG  
FPGA-CFG.SchDoc
- U\_FPGA-MISC  
FPGA-MISC.SchDoc
- U\_FPGA-PWR  
FPGA-PWR.SchDoc

- U\_PWR1  
PWR1.SchDoc
- U\_PWR2  
PWR2.SchDoc

- U\_Clock  
Clock.SchDoc

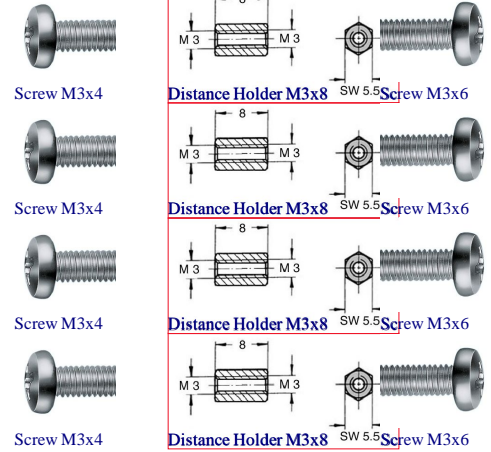
- U\_B2B-Connectors  
B2B-Connectors.SchDoc

- U\_B33  
B33.SchDoc



Serial  
Serial  
Serialnumber 6,3 x 6,3mm

Top of Board



Assembly variant	160-2CF
Created by	VT
Modified by	VT
Modified at	2017-01-23
SVN Revision	8679

Title: **TE0741**

A4	Number: <b>TE0741 160-2CF</b>	Rev. <b>03</b>
Date: 2016-10-25	Copyright: 2013 Trenz Electronic GmbH	Page1 of 17
Filename: <b>TE0741.SchDoc</b>		

1

2

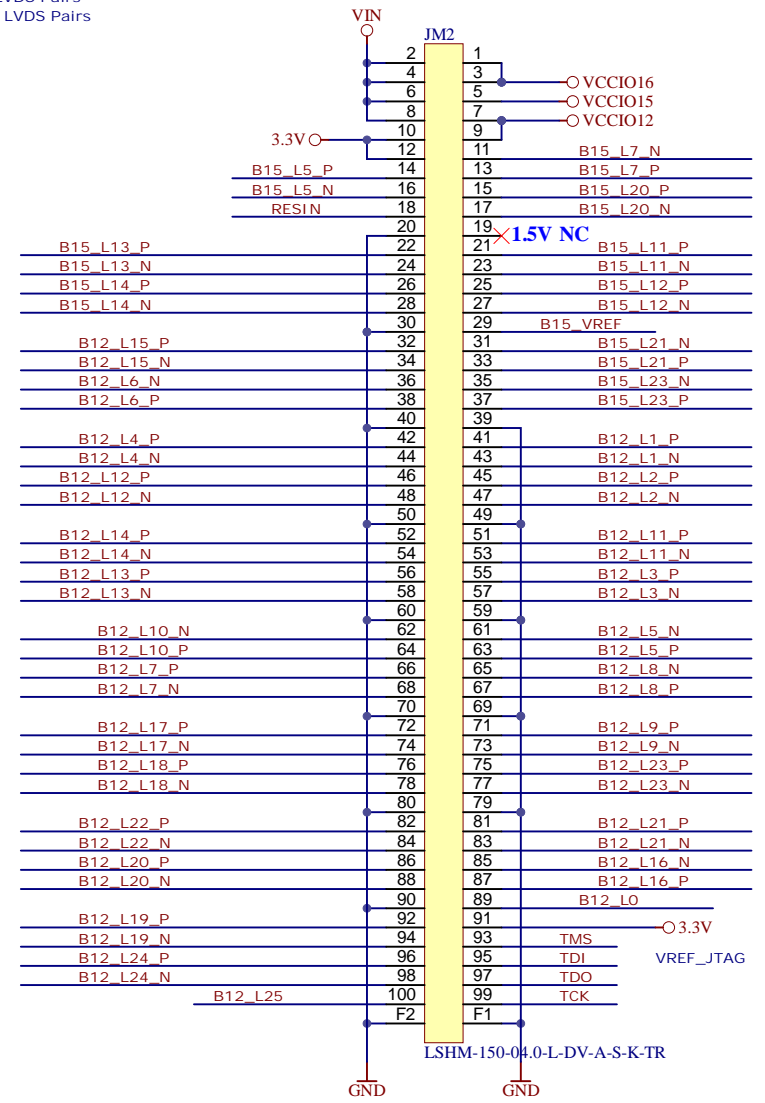
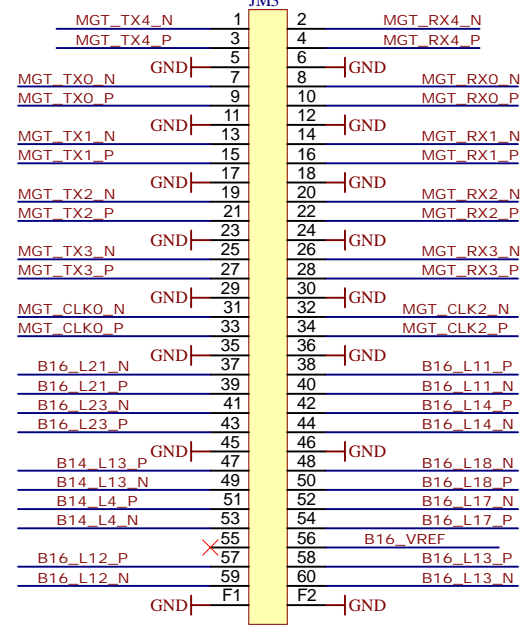
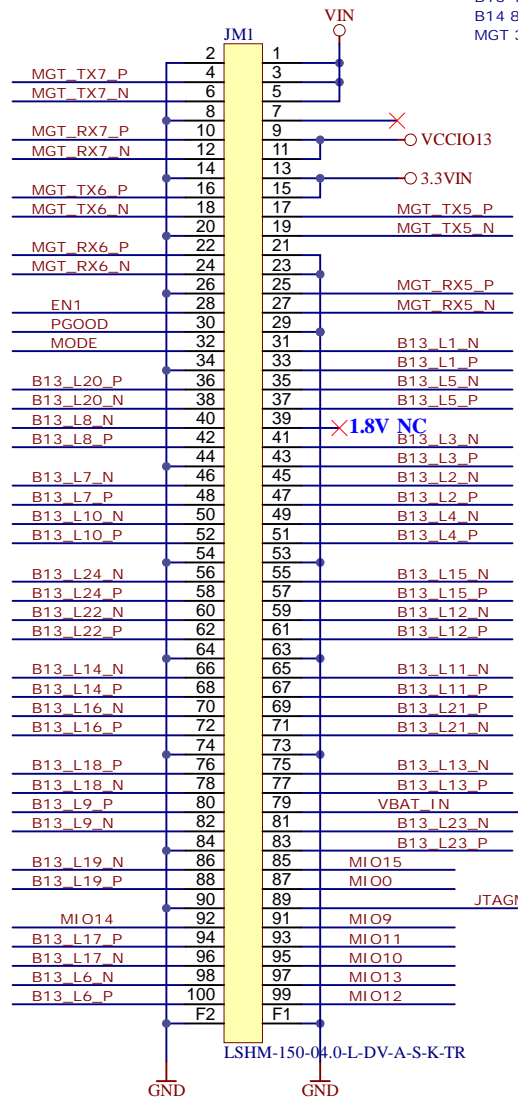
3

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B13 48 IO, 24 LVDS Pairs  
 B14 8 IO, 3.3V  
 MGT 3 Lanes

B16 16 IO, 8 LVDS Pairs  
 MGT 4 + 1 Lanes  
 B14 4 IO, 3.3V

B15 18 IO, 9 LVDS Pairs  
 B12 48 IO, 24 LVDS Pairs  
 B12 2 IO



VIN

3.3V

1.8V NC

NC

JTAGMODE

LSHM-150-04.0-L-DV-A-S-K-TR

LSHM-130-04.0-L-DV-A-S-K-TR

VIN

3.3V

1.5V NC

3.3V

VREF\_JTAG

LSHM-150-04.0-L-DV-A-S-K-TR

TE0720 Compatibility

MIO0 8 pins => 8 IO B14  
 USB D+,D-, vbusen,otg\_id => 4 IO B14  
 SGMII => MGT  
 MIO1(SDCARD) => MGT  
 ETH MD1 => MGT  
 B34 => B16, MGT  
 B35 => B13  
 B13 => B12  
 B33 => B15

Clock Capable I/O  
 All pins named  
 Bxx\_11\_X  
 Bxx\_12\_X  
 Bxx\_13\_X  
 Bxx\_14\_X  
 Are Clock Capable I/O's



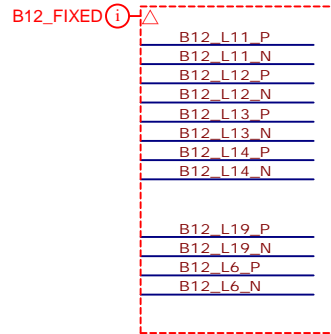
Title: TE0741		
A4	Number: TE0741 160-2CF	Rev. 03
Date: 2016-10-25	Copyright: 2013 Trenz Electronic GmbH	Page2 of 17
Filename: B2B-Connectors.SchDoc		

1

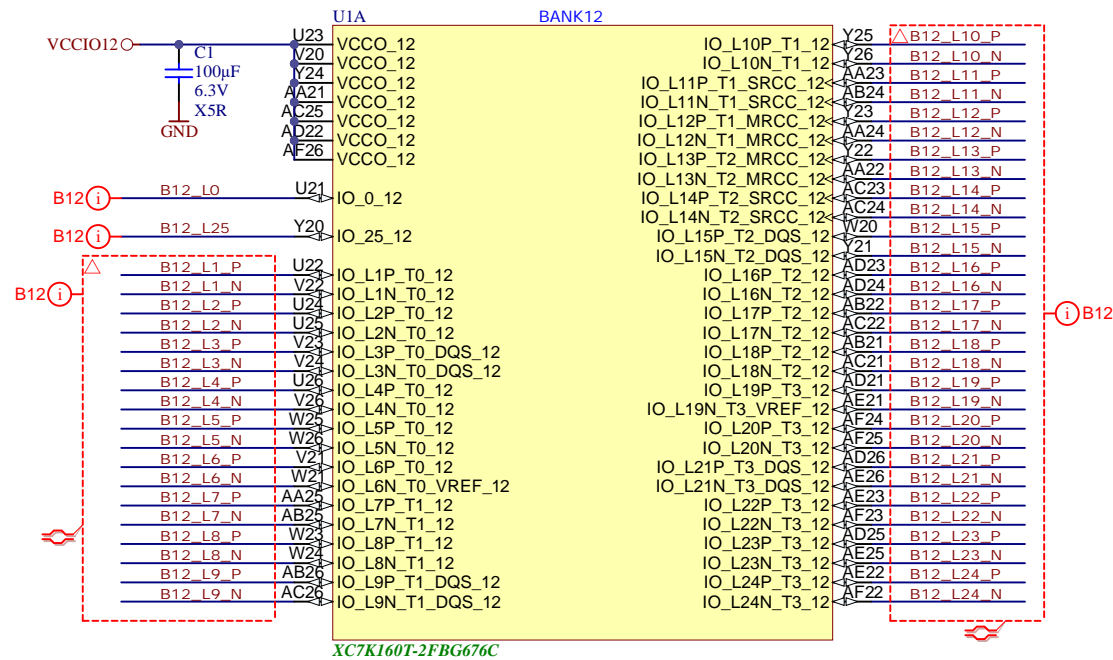
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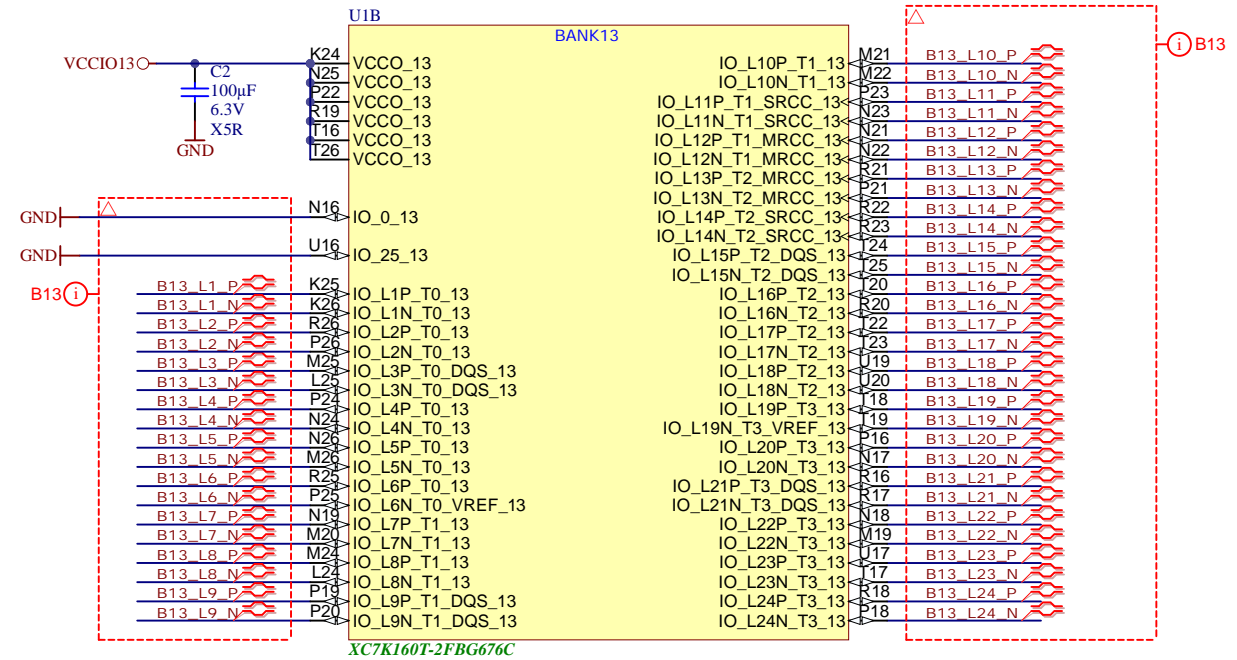
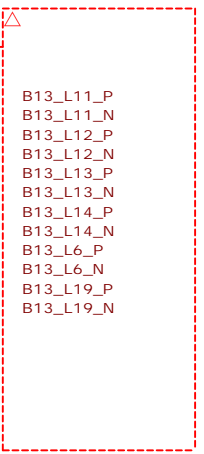


**K70T version does not have this bank!**



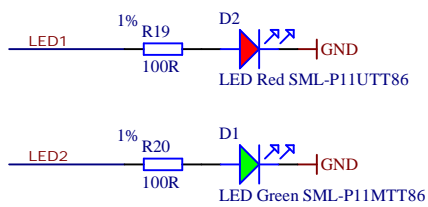
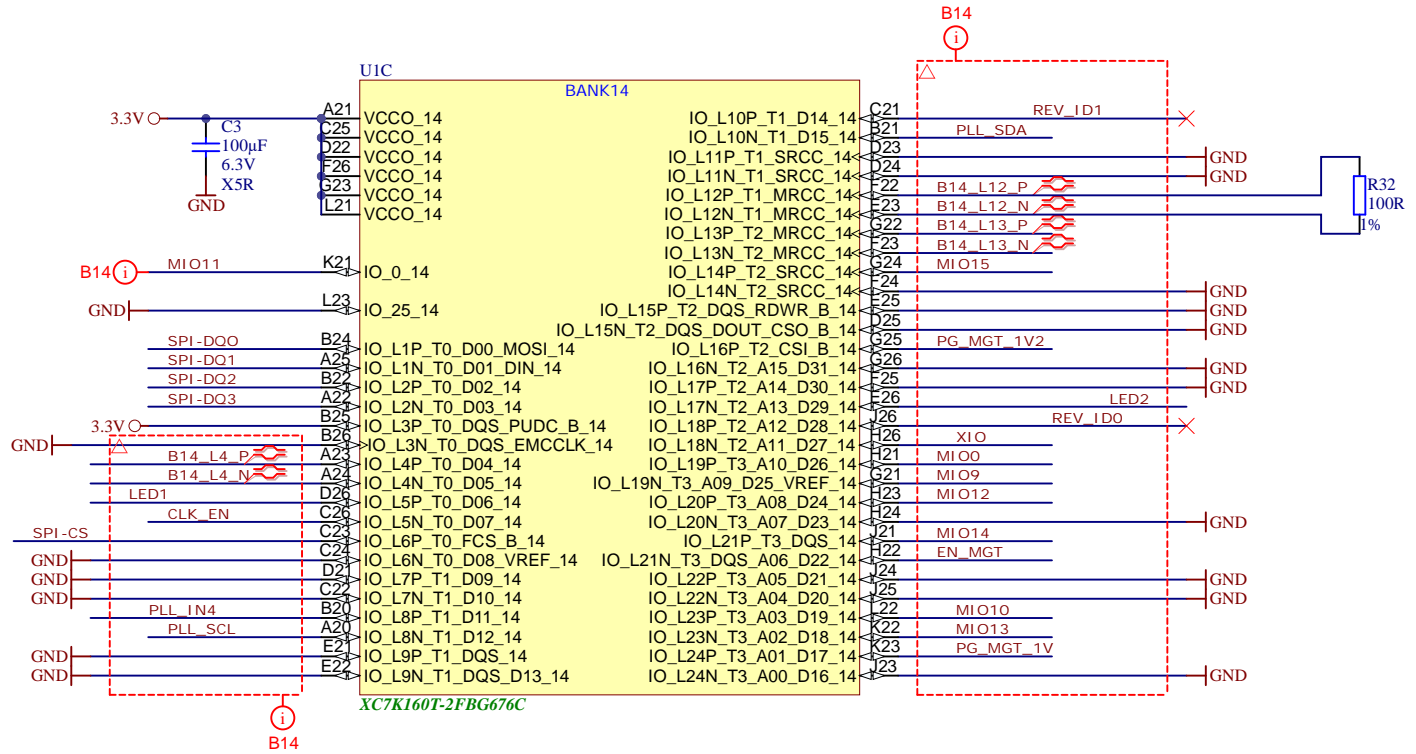
	Title: TE0741	
	A4	Number: TE0741 160-2CF
	Date: 2016-10-25	Rev. 03
	Page3 of 17	
Copyright: 2013 Trenz Electronic GmbH		Page3 of 17
Filename: B12.SchDoc		


B13\_FIXED (i)

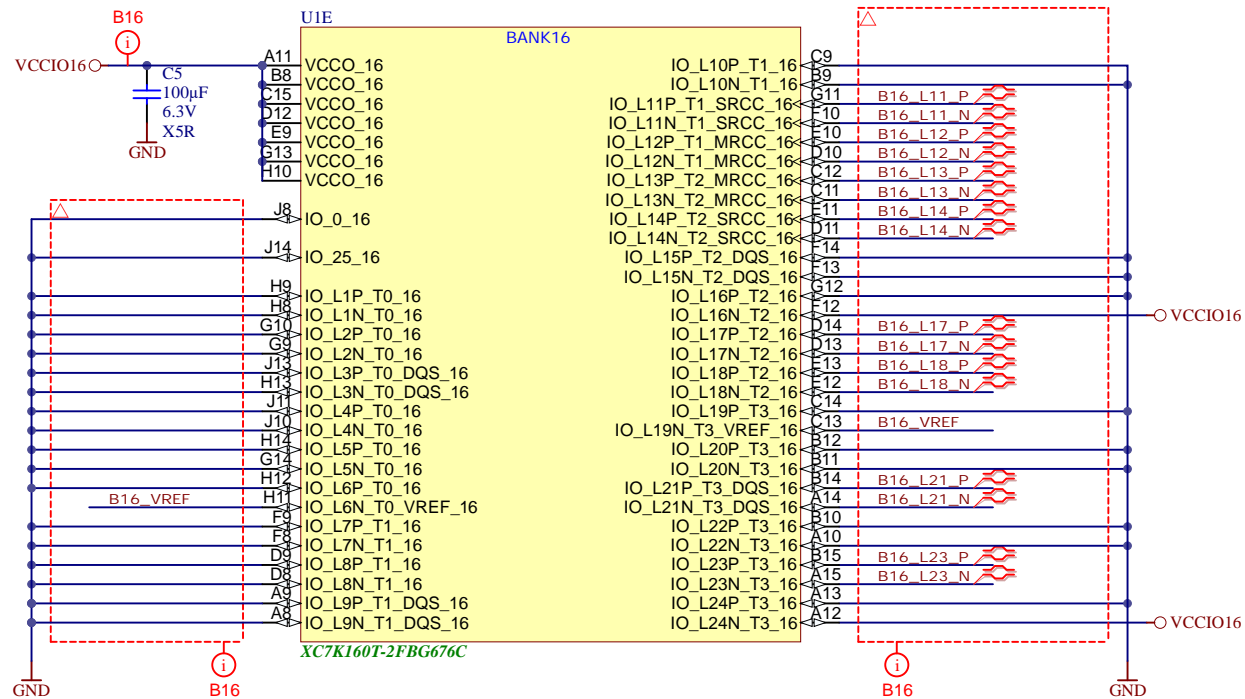


XC7K160T-2FBG676C

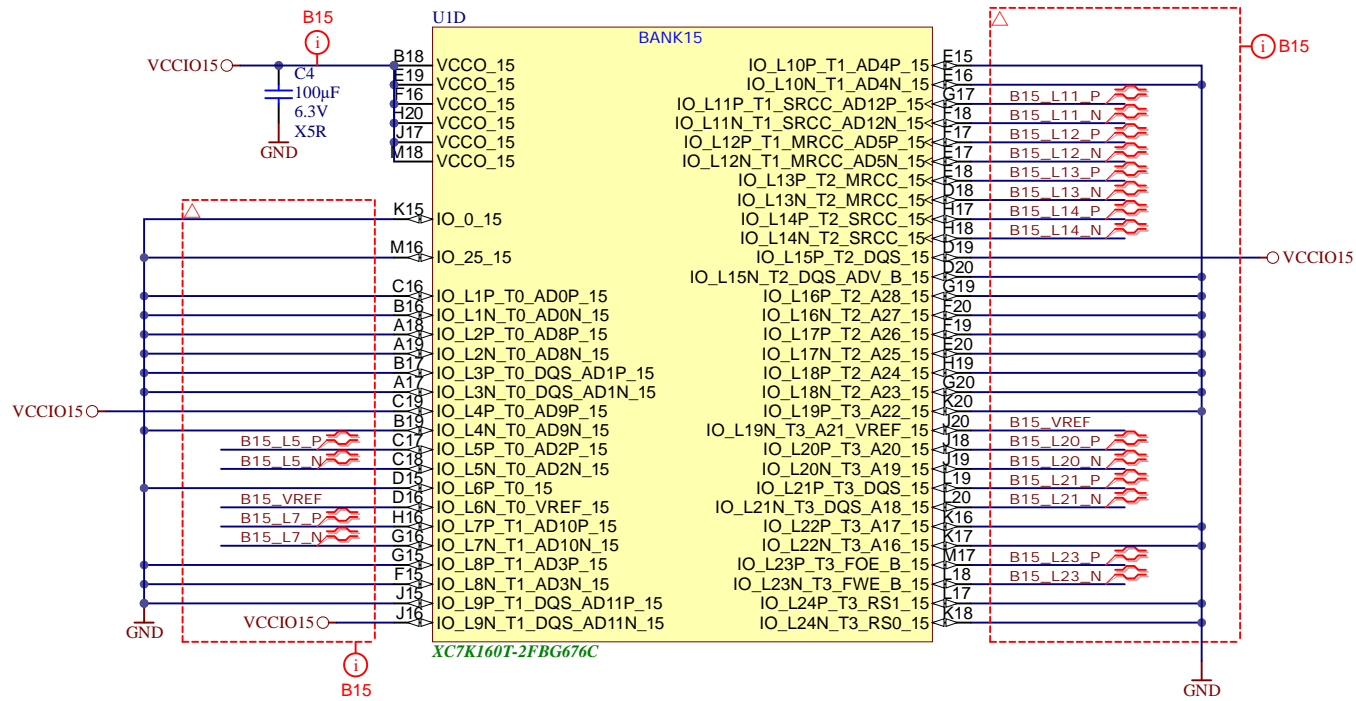
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	A4	Number: TE0741 160-2CF	Rev. 03
	Date: 2016-10-25	Copyright: 2013 Trenz Electronic GmbH	Page4 of 17
	Filename: B13.SchDoc		



		Title: TE0741	
		A4	Number: TE0741 160-2CF
Date: 2016-10-25		Copyright: 2013 Trenz Electronic GmbH	
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Filename: B14.SchDoc			



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A4	Number: <b>TE0741 160-2CF</b>	Rev. <b>03</b>
Date: <b>2016-10-25</b>	Copyright: <b>2013 Trenz Electronic GmbH</b>	Page <b>6</b> of <b>17</b>
Filename: <b>B16.SchDoc</b>		



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A4	Number: <b>TE0741 160-2CF</b>	Rev. <b>03</b>
Date: <b>2016-10-25</b>	Copyright: <b>2013 Trenz Electronic GmbH</b>	Page <b>7</b> of <b>17</b>
Filename: <b>B15.SchDoc</b>		

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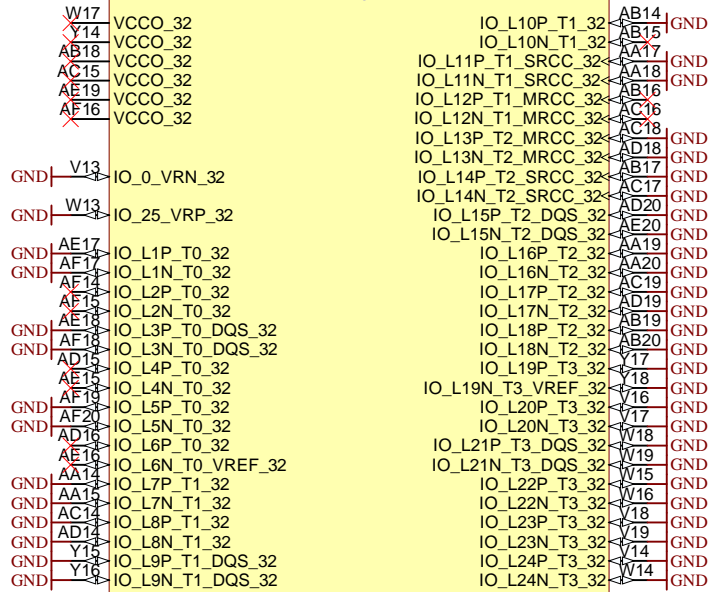
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D

D

UIF

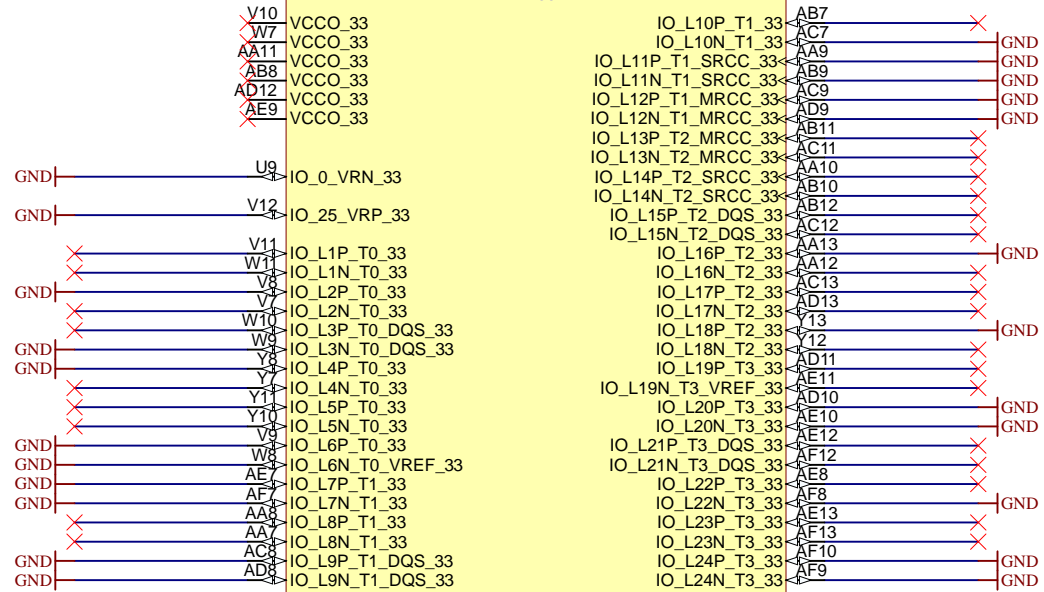
BANK32




XC7K160T-2FBG676C

UIG

BANK33



XC7K160T-2FBG676C



Title: TE0741		
A4	Number: TE0741 160-2CF	Rev. 03
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Filename: B33.SchDoc		

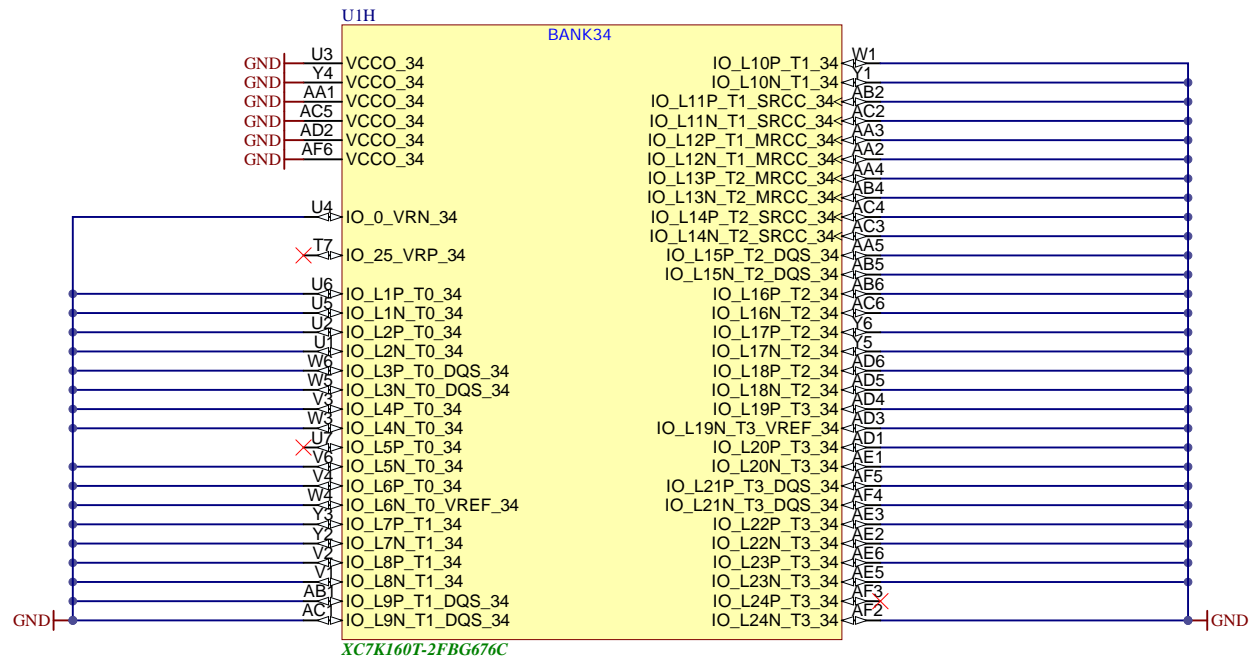
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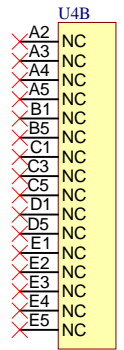
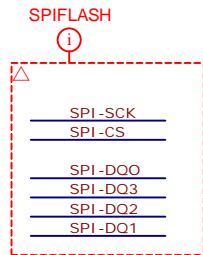
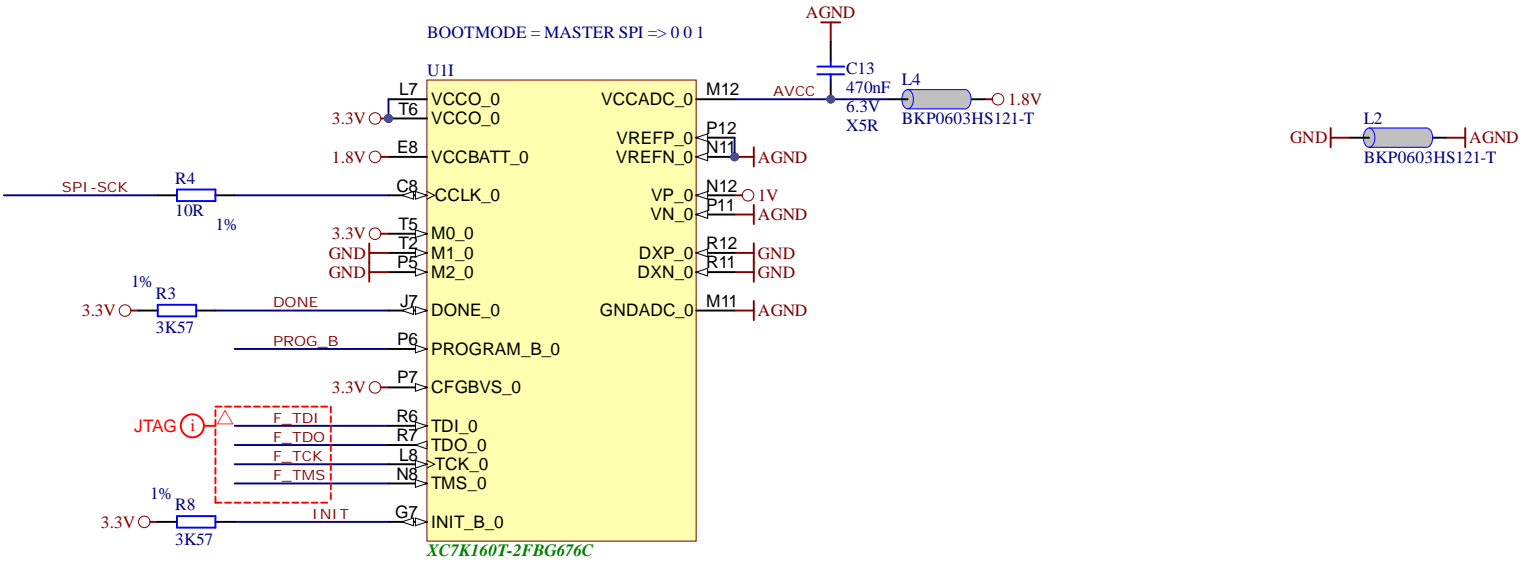




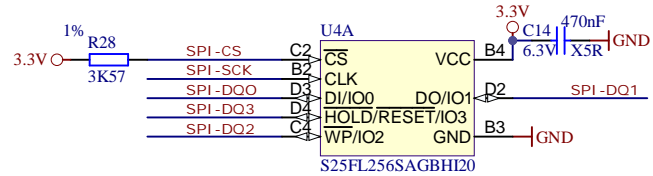
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	A4	Number: TE0741 160-2CF	Rev. 03
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	Filename: B34.SchDoc		



BOOTMODE = MASTER SPI => 0 0 1



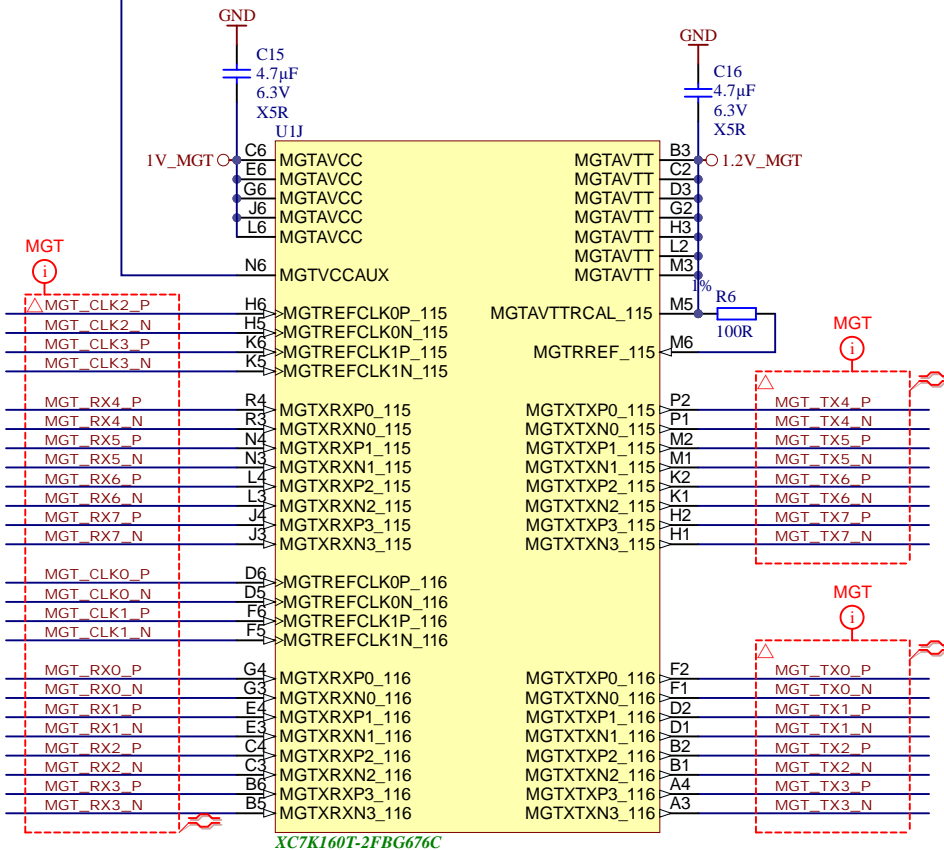
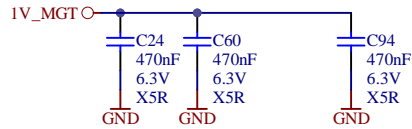
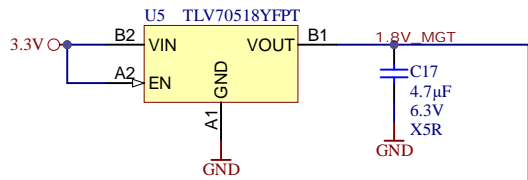
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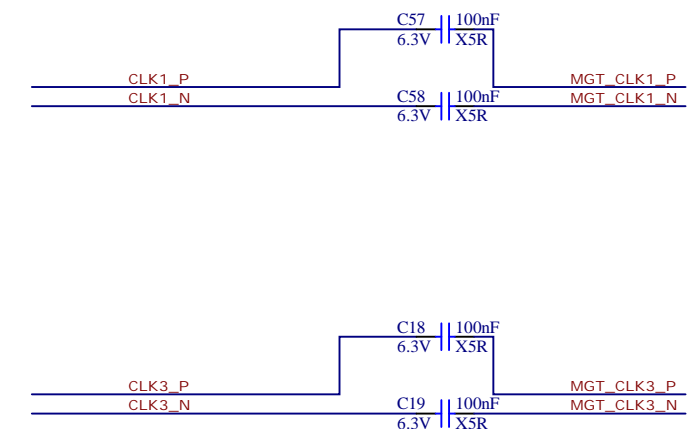
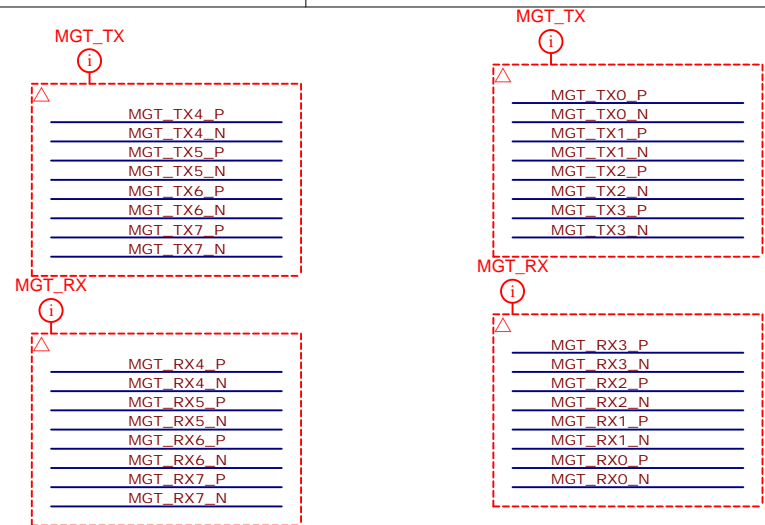
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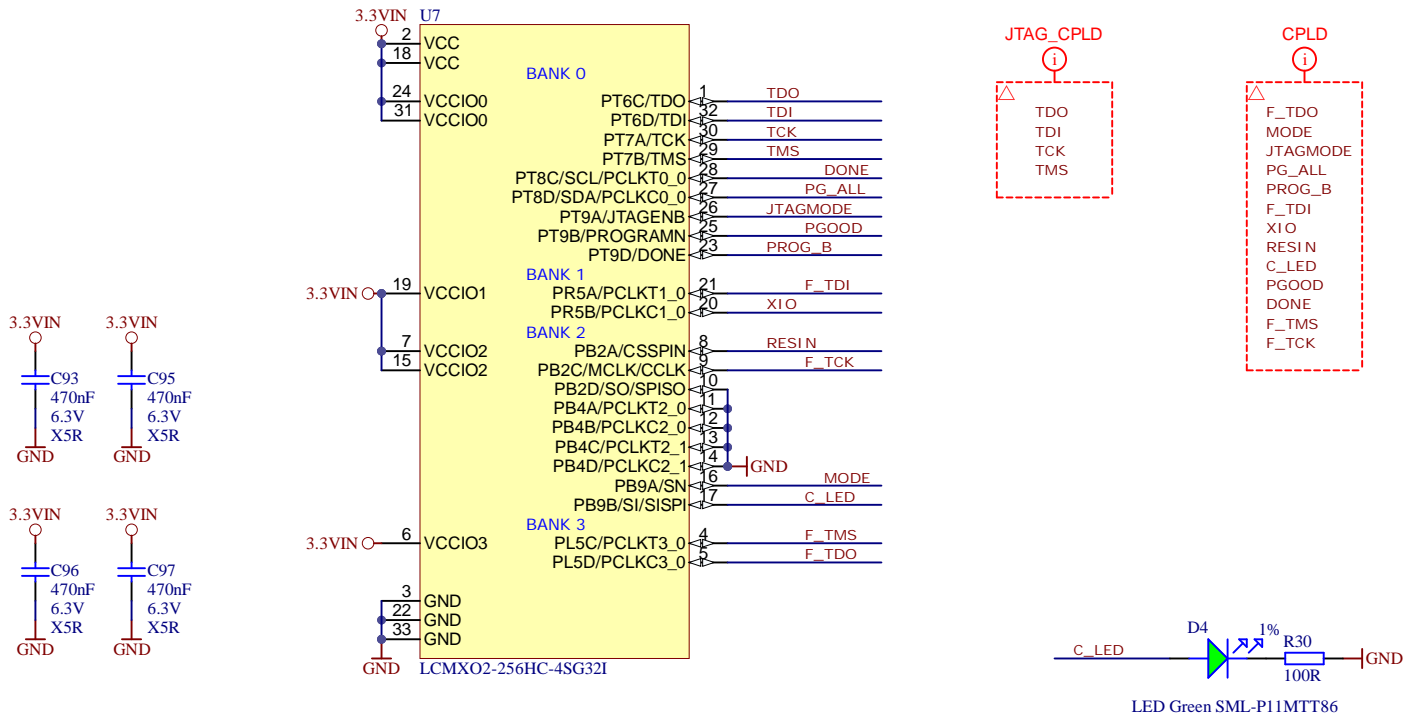
Title: TE0741		
A4	Number: TE0741 160-2CF	Rev. 03
Date: 2016-10-25	Copyright: 2013 Trenz Electronic GmbH	Page 11 of 17
Filename: FPGA-CFG.SchDoc		




XC7K160T-2FBG676C



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Filename: <b>FPGA-MGT.SchDoc</b>		



		Title: TE0741	
		A4	Number: TE0741 160-2CF
Date: 2016-10-25		Copyright: 2013 Trenz Electronic GmbH	
Page 13 of 17		Filename: FPGA-MISC.SchDoc	

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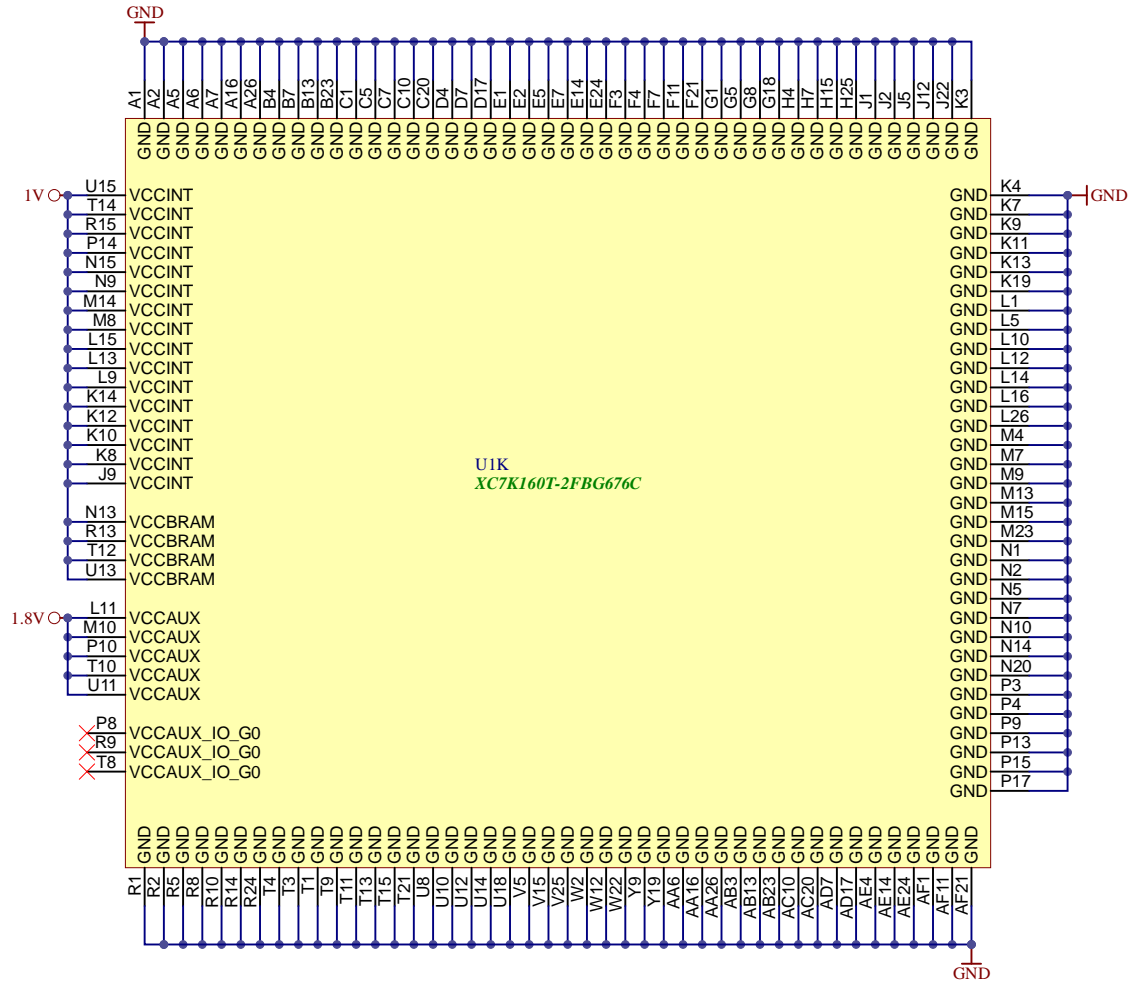
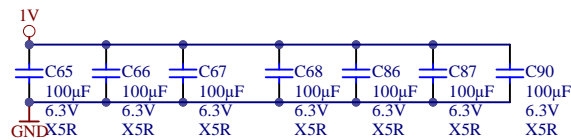
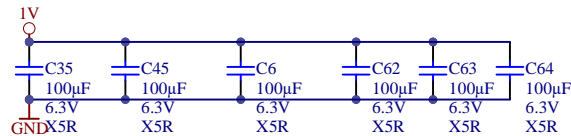
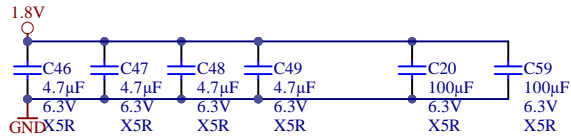
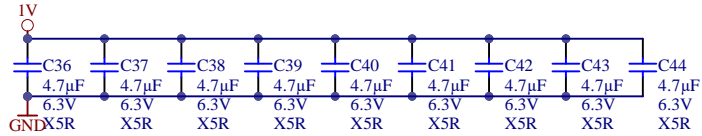
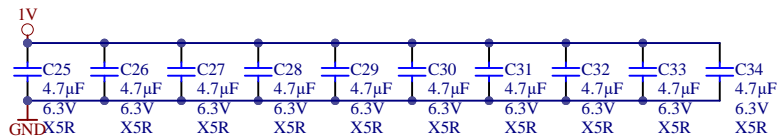
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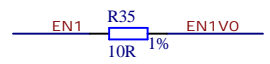
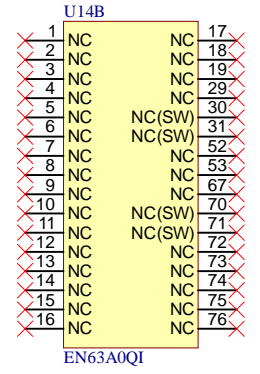
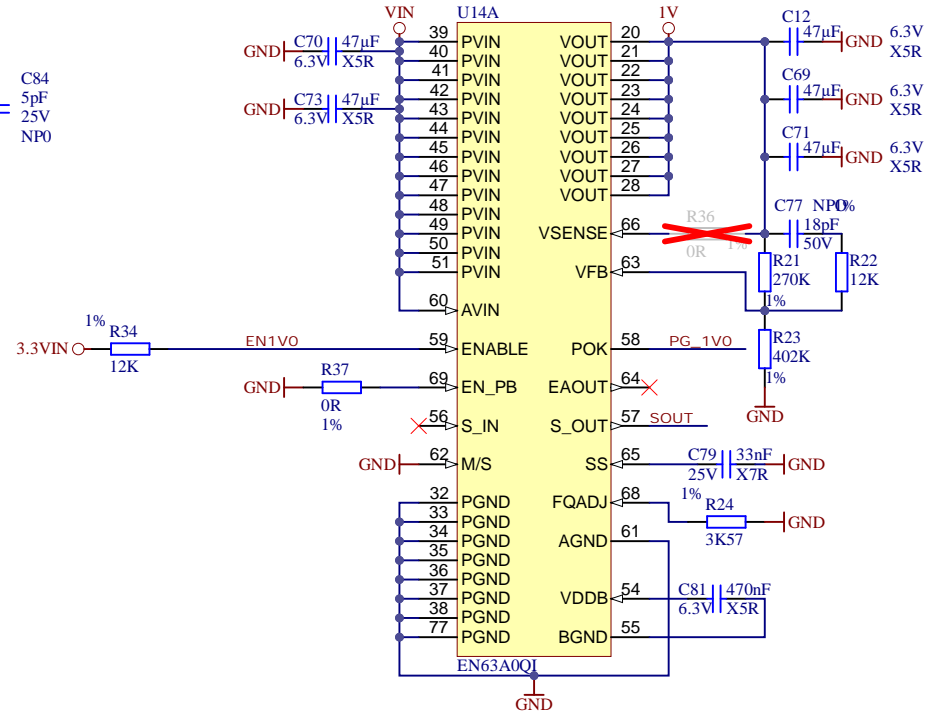
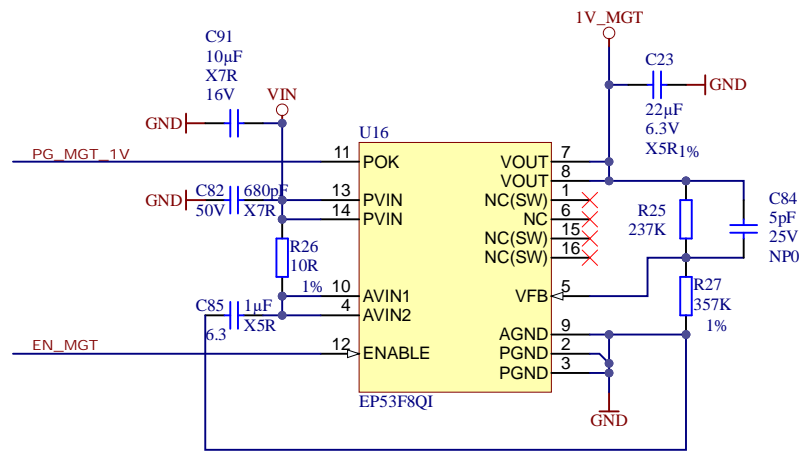
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Title: TE0741		
A4	Number: TE0741 160-2CF	Rev. 03
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Filename: FPGA-PWR.SchDoc		

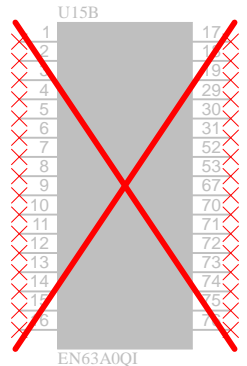
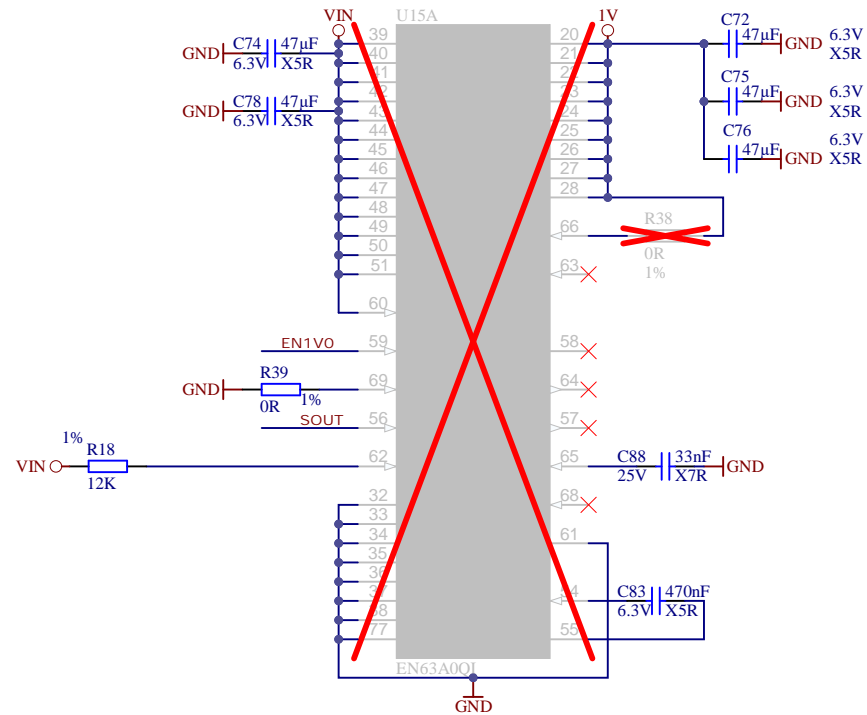
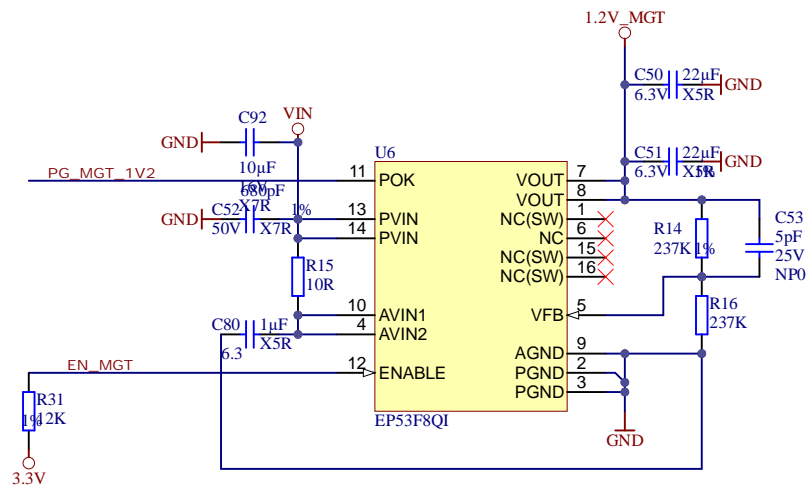


**A** Not mount if baseboard EN1 circuit cause problems

Pre-bias feature is not available for parallel operations

R36 R37 MODE EN63A0QI  
 -----  
 OK X | enable pre-bias start-up (available when U14 or U15 as DNP )  
 X OK | disable pre-bias start-up

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	Filename: <b>PWR1.SchDoc</b>		



Pre-bias feature is not available for parallel operations

R38	R39	MODE	EN63A0QI
OK	X		enable pre-bias start-up (available when U14 or U15 as DNP )
X	OK		disable pre-bias start-up



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Filename: PWR2.SchDoc		



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CHANGES REV02 to REV03

- 1) fixed connection DCDC for parallel operations
- 2) update Razorbeam Connectors, full update lib
- 3) added serial number (traceability pad)
- 4) changed ferrite beads L1..L4 size 0402 on BKP0603HS121-T
- 5) added thermal vias to mounting holes

A

A

B

B

C

C

D

D



Title: <b>TE0741 - Changes list</b>		
A4	Number: <b>TE0741 160-2CF</b>	Rev. <b>03</b>
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Filename: <b>Revision_Changes.SchDoc</b>		

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