Microsemi Corporation

September 28, 2016

Customer Notification No: 156287

Notification Only – No action required

Subject: Updates to Datasheets for MAX24205 / MAX24210 / MAX24305 / MAX24310 / MAX24605 / MAX24610 / MAX24705 / MAX24710

Description of Change:

There is no change to the product, but Microsemi is informing customers of the following updates in the data sheets.

Instructions have been added to the datasheets to provide setup information for using a non-zero value in the OFFSET[15:0] field in the OFFSET1 and OFFSET2 registers.

The register description for the DPLL Phase Offset Register 1, OFFSET1 is being changed to include the following note in applicable datasheets:

> Note: The DPLL cannot support a non-zero OFFSET value when transitioning *to* the Free-Run state. See the DPLL state diagram in Figure 5 9 for the one state transition to the Free-Run state from the Prelocked state. To avoid this state transition when OFFSET≠0 do one of the following:
>
> 1. First step after device reset, with MCR2.IC1EN and MCR2.IC2EN both left at default values of 0, force the DPLL into the Digital Hold state (DPLLCR2.STATE=010) and then back to automatic state transitions (DPLLCR2.STATE=000). After reset the Digital Hold state behaves exactly the same as the Free-Run state (0ppm offset vs. the local oscillator).
> 2. Do not set the OFFSET field to a non-zero value until the DPLL is in one of these states: Locked, Loss-of-Lock, Digital Hold, Prelocked2 (PLL1SR.STATE=010, 100, 101 or 111). After the DPLL has reached one of these states it cannot return to the Free-Run state unless forced.
>
> Also do not force the DPLL to the Free-Run state during operation when OFFSET≠0.

Complete data sheet revision history can be found at the end of the data sheet.

There is no change to form, fit, function or reliability of the products.

Reason for Change:

The listed devices can enter a state that results in improper input-to-output signal alignment and/or higher than normal output jitter when a non-zero phase offset is specified in the DPLL's OFFSET 1 Register and the DPLL transitions to its Free-Run state.

Application Impact:

There is no change to product form, fit or function. This is a datasheet update only, in order to provide more instruction on using the DPLL Phase Offset feature.

Products Affected by this Change:

MAX24205EXG+, MAX24210EXG+

MAX24305EXG+, MAX24310EXG+

MAX24605EXG+, MAX24610EXG+

MAX24705EXG+, MAX24710EXG+

Note: This is a list of Ordering Part Numbers (OPNs) as are found in product datasheets. Customers may track additional part number variants in their systems, so please consider this a base part list.

Datasheet Availability:

Copies of the datasheets can be accessed via the Microsemi.com website via the following URLs:

MAX24205/MAX24210:
http://www.microsemi.com/products/timing-and-synchronization/clock-synthesis/max24205-max24210

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MAX24305/MAX23210:
http://www.microsemi.com/products/timing-and-synchronization/synchronous-ethernet/max24305-max24310

MAX24605/MAX24610:
http://www.microsemi.com/products/timing-and-synchronization/frequency-conversion/max24605-max24610

MAX24705/MAX24710:
http://www.microsemi.com/products/timing-and-synchronization/synchronous-ethernet/max24705-max24710

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Regards,

Microsemi Corporation