



# FSA8039

## Audio Jack Detection and Configuration Switch with Moisture Sensing

### Features

<b>Detection</b>	Accessory Plug-In 3-Pole or 4-Pole Audio Jack Send / End Key Pressed Moisture
<b>Switch Type</b>	MIC
<b>V<sub>DD</sub></b>	2.5 V to 4.5 V
<b>V<sub>IO</sub></b>	1.6 to V <sub>DD</sub>
<b>THD (MIC)</b>	0.01% Typical
<b>ESD (Air Gap)</b>	15 kV
<b>Operating Temperature</b>	-40°C to 85°C
<b>Package</b>	10-Lead UMLP, 1.4 mm × 1.8 mm × 0.5 mm, 0.4 mm Pitch
<b>Top Mark</b>	NF
<b>Ordering Information</b>	FSA8039UMSX_F106

### Applications

- 3.5 mm and 2.5 mm Audio Jacks
- Cellular Phones, Smart Phones
- MP3 and PMP

### Description

The FSA8039 is an audio jack detection switch for 3-pole and 4-pole accessories. The FSA8039 features moisture sensing, which prevents false positive detection of accessories in the audio jack. The FSA8039 also features an integrated MIC switch that allows a processor to configure attached accessories. The architecture is designed to allow common third-party headphones to be used for listening to music from mobile handsets, personal media players, and portable peripheral devices.

- Prevents False Detection of Accessories in the Audio Jack when Moisture is Present
- Removes Audio Jack Pop & Click Caused by MIC Bias
- Detects Audio Jack Accessories:
  - Standard Headphones
  - Send / End Button Presses
- Integrates a MIC Switch for 4-Pole Configuration

### Related Resources

- [FSA8039 Evaluation Board](#)
- *For samples and questions, please contact:*  
[Analog.Switch@fairchildsemi.com](mailto:Analog.Switch@fairchildsemi.com)

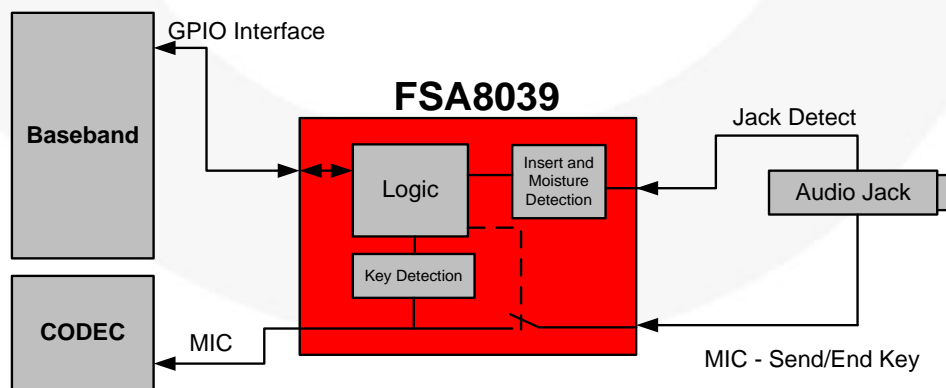


Figure 1. System Diagram

## Typical Application Diagram

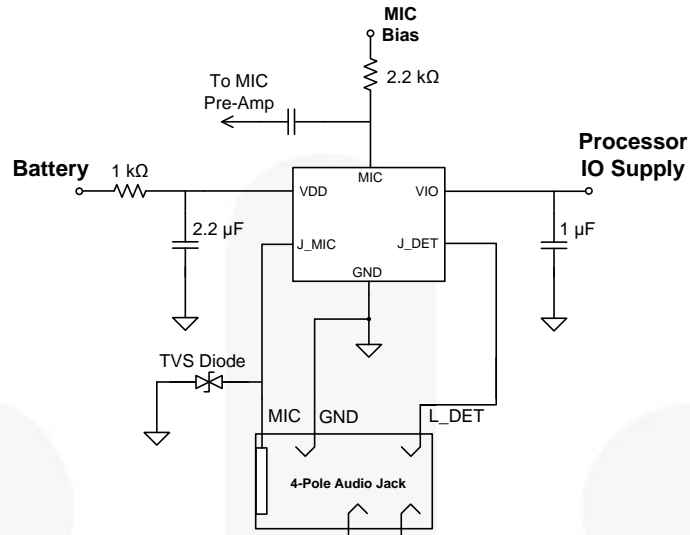


Figure 2. Typical Application

## Pin Configuration

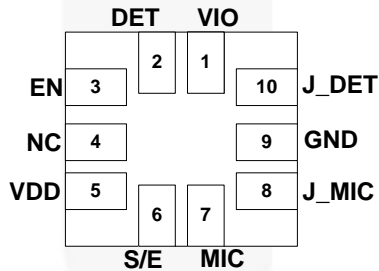


Figure 3. Pin Assignment (Through View)

## Pin Definitions

Name	Pin #	Type	Description	
V <sub>IO</sub>	1	Power	Baseband I/O supply voltage	
DET	2	Output	De-bounced output of J_DET; Indicates if audio accessory is plugged in.	DET=L, Plugged DET=H, Unplugged
EN	3	Input	Internal microphone switch control input	EN=L, Switch is Open EN=H, Switch is Closed
NC	4	N/C	No connect; connect to ground for improved solder stability	
V <sub>DD</sub>	5	Power	Core supply voltage	
S/E	6	Output	De-bounced output for a connected 4-pole accessory; Indicates when an accessory key has been pressed	S/E=L, No Key Press S/E=H, Key Press
MIC	7	Switch	System-side microphone switch pin	EN=L, Switch Open EN=H, Switch Closed
J_MIC	8	Switch	Accessory-side microphone switch pin	
GND	9	Ground	Ground for both the audio jack and PCB	
J_DET	10	Input	Input from the audio jack mechanical plug insert/removal detection pin.	J_DET=H, Unplugged J_DET=L, Plugged

### Note:

1. L=LOW, H=HIGH.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit	
$V_{DD}, V_{IO}$	DC Supply Voltages	-0.5	6.0	V	
$V_{SW}$	MIC Switch I/O Voltage and All Input Voltages Except J_DET	-0.5	$V_{DD}+0.5$	V	
$V_{JD}$	Input Voltage for J_DET Input	-1.5	$V_{DD}+0.5$	V	
$I_{IK}$	Input Clamp Diode Current	-50		mA	
$I_{SW}$	Switch I/O Current (Continuous) <sup>(2)</sup>		50	mA	
$T_{STG}$	Storage Temperature Range	-65	+150	°C	
$T_J$	Maximum Junction Temperature		+150	°C	
$T_L$	Lead Temperature (Soldering, 10 Seconds)		+260	°C	
ESD	IEC 61000-4-2 System ESD	Air Gap	15.0		kV
		Contact	8.0		
	Human Body Model, JEDEC JESD22-A114,	J_DET, J_MIC, $V_{DD}$ , $V_{IO}$ , GND	13.0		
		All Other Pins	8.0		
	Charged Device Model, JEDEC JESD22-C101	All Pins	2.0		

### Note:

- The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
$V_{DD}$	Battery Supply Voltage	2.5	4.5	V
$V_{IO}$	Parallel I/O Supply Voltage	1.6	$V_{DD}$	V
$T_A$	Operating Temperature	-40	+85	°C

## DC Electrical Characteristics

All typical values are at  $T_A=25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	$V_{DD}$ (V)	Condition	$T_A=-40$ to $+85^\circ\text{C}$			Unit
				Min.	Typ.	Max.	
<b>MIC Switch</b>							
$V_{IN}$	Switch Input Voltage Range	2.5 to 4.5		0		$V_{DD}$	V
$R_{ON}$	MIC Switch On Resistance	2.8	$I_{OUT}=30\text{ mA},$ $V_{IN}=2.2\text{ V}$		0.85	2.00	$\Omega$
		3.0			0.70	2.00	
		3.3			0.50	2.00	
		3.8			0.40	2.00	
$R_{FLAT(ON)}$	On Resistance Flatness	2.8	$I_{OUT}=30\text{ mA},$ $V_{IN}=1.6$ to $2.8\text{ V}$		0.45	1.50	$\Omega$
		3.0			0.40	1.50	
		3.3			0.35	1.50	
		3.8			0.30	1.50	
<b>J_DET</b>							
$J\_DET_{AudioV}$	Audio Voltage on J_DET Pin	2.5 to 4.5	DET=LOW	-1		1	V
$J\_DET_{Audiof}$	Audio Frequency on J_DET Pin	2.5 to 4.5	DET=LOW	20		20000	Hz
$J\_DET_{RGND}$	Detection Resistance to Ground	2.5 to 4.5	Audio Accessory Inserted	0		500	k $\Omega$
$J\_DET_{HYS}$	Hysteresis of J_DET				200		mV
$J\_DET_{VIH}$	J_DET Input High Voltage			$0.7 \times V_{DD}$		$V_{DD}$	V
$J\_DET_{VIL}$	J_DET Input Low Voltage			-1		$0.4 \times V_{DD}$	V
<b>Parallel I/O</b>							
$V_{IH}$	EN Input High Voltage			$0.7 \times V_{IO}$		$V_{IO}$	$V$
$V_{IL}$	EN Input Low Voltage					$0.3 \times V_{IO}$	
$V_{OH}$	DET, S/E Output High Voltage		$I_{OH}=-100\ \mu\text{A}$	$0.8 \times V_{IO}$			
$V_{OL}$	DET, S/E Output Low Voltage		$I_{OL}=+100\ \mu\text{A}$			$0.2 \times V_{IO}$	
<b>Comparator</b>							
$V_{COMP\_S/E}$	Comparator Threshold for SEND/END Sensing	2.8 to 4.5	J_DET, EN=LOW		780		mV
<b>Current</b>							
$I_{OFF}$	Power-Off Leakage Current Through Switch	0	MIC=4.3 V			1	$\mu\text{A}$
$I_{IN}$	Input Leakage Current	0	EN=4.3 V			1	$\mu\text{A}$
$I_{CC\_SLNA}$	$V_{DD}$ Supply Sleep Mode Current (No Accessory Attached)	2.5 to 4.5	EN=LOW		1.5	3.0	$\mu\text{A}$
$I_{CC\_SLWA}$	$V_{DD}$ Supply Active Mode Current (Accessory Attached)	2.5 to 4.5	DET=LOW, EN=HIGH		20	27	$\mu\text{A}$

## AC Electrical Characteristics

All typical values are for  $V_{CC}=3.3$  V at  $T_A=25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	$V_{DD}$ (V)	Conditions	Typical	Unit
<b>MIC Switch</b>					
THD+N	Total Harmonic Distortion + Noise	3.8	$R_T=600\ \Omega$ , $f=20$ Hz to 20 kHz, $V_{MIC}=2.2$ VDC + $0.5V_{PP}$ Sine	0.01	%
$O_{IRR}$	Off Isolation	3.8	$f=20$ Hz to 20 kHz, $R_S=R_T=32\ \Omega$ , $C_L=0$ pF	-85	dB
$C_{ON}$	MIC and J_MIC Switch ON Capacitance	3.8	$f=1$ MHz	60	pF
$C_{OFF}$	MIC and J_MIC Switch OFF Capacitance	3.8	$f=1$ MHz	35	pF
<b>Parallel I/O</b>					
$t_R, t_F$	Output Edge Rates (DET, S/E)	3.8	$C_L=5$ pF, 20% to 80%,	20	ns
$t_{POLL}$	On Time of MIC Switch for Sensing SEND/END Button Press	2.5 to 4.5	DET= LOW, EN= LOW	1	ms
$t_{WAIT}$	Period of MIC Switching Time for Sensing SEND/END Button Press	2.5 to 4.5	DET= LOW, EN= LOW	10	ms
$t_{DET\_IN}$	Debounce Time after J_DET Changes State from HIGH to LOW	2.5 to 4.5		70	ms
$t_{DET\_REM}$	Debounce Time after J_DET Changes State from LOW to HIGH	2.5 to 4.5		30	$\mu\text{s}$
$t_{KBK}$	SEND/END Button Press/Release Debounce Time	2.5 to 4.5		30	ms
<b>Power</b>					
PSRR	Power Supply Rejection Ratio	3.8	Power Supply Noise $300$ mV <sub>PP</sub> , $f=217$ Hz	-90	dB

## Application Information

### Design/Layout Best Practices

System-level Electrostatic Discharge (ESD) events often occur in the audio path of a mobile device, typically when inserting or removing an accessory from the audio jack. The audio path from the audio jack to the audio codec or microphone pre-amplifier is typically designed for relatively low frequencies (<100 kHz). However, an ESD event is a high-frequency event with fast edge rates (<100 ns/V). Because of this, the audio signal paths represent a high-frequency transmission line to the ESD signal.

Use the following PCB design and layout best practices when designing a system audio path.

### Audio Path Layout Guidelines for ESD

For the MIC and ground signals between the audio jack and FSA8039, decrease the spacing between these traces to increase the inductive coupling of these signals. In effect, this creates a low-frequency band-pass filter that shunts ESD energy to ground before it reaches internal components. Where feasible, lay the MIC trace as a shielded stripline; an example is shown in Figure 4.

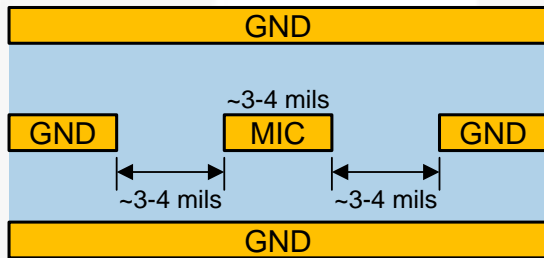


Figure 4. MIC PCB Trace as Shielded Stripline

### Ground Layout Guidelines

Ground layout for audio path devices should consider high-frequency effects. During an ESD event, parasitic inductance and resistance in the ground path reduces its ability to shunt the fast transient energy. Use the following techniques to improve grounding effectiveness:

- Use “star” ground connections (not daisy-chain).
- Use ground vias to minimize ground path impedance and ground loops.
- Stitch ground traces to the ground plane at the device, where possible (see Figure 4).
- Flood ground, where possible (see Figure 4).
- Avoid ground “islands” or “peninsulas” if possible.
- If using a modular audio jack assembly that is not soldered to the main PCB, use a ground pad on the jack with an ohmic connection to battery ground.

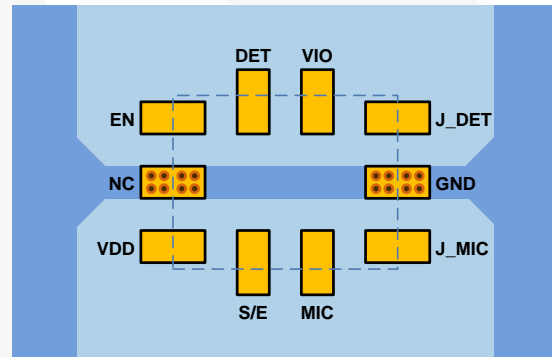
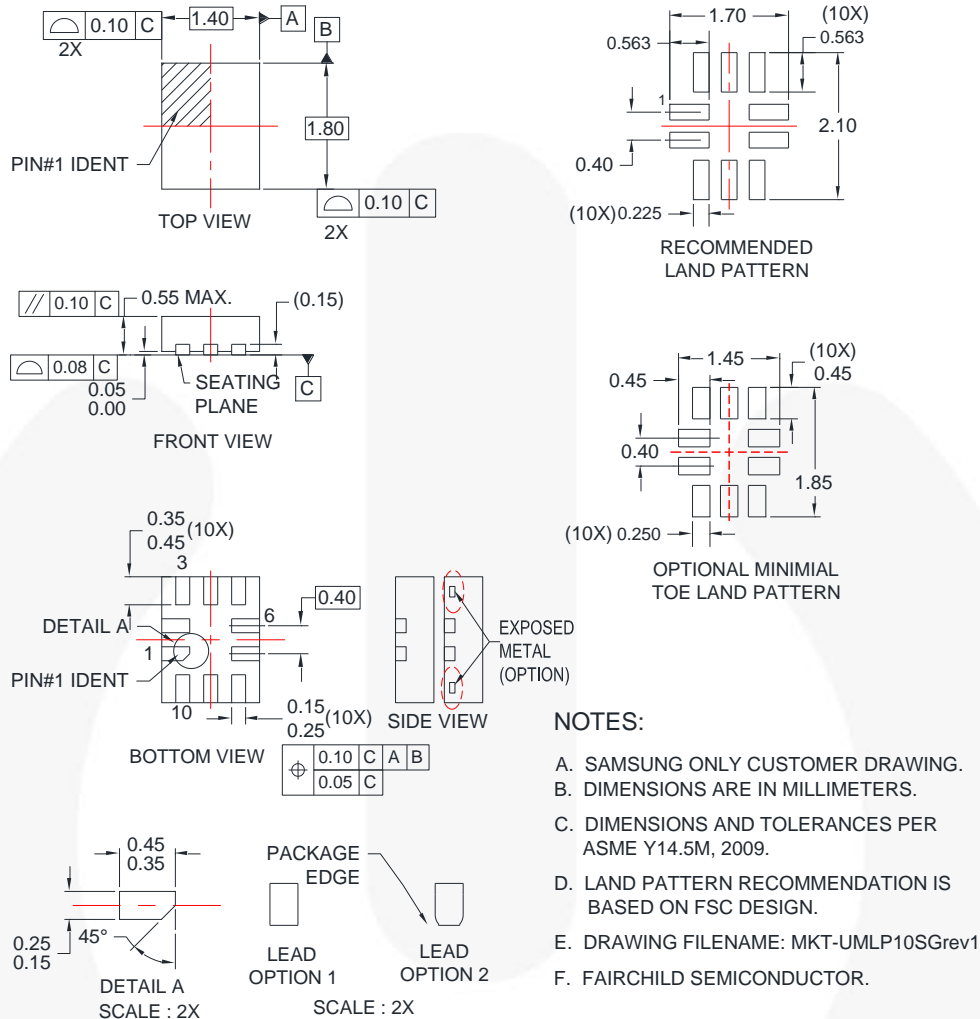


Figure 5. PCB Layout/Grounding

In addition to ESD robustness, these techniques can improve audio signal performance by reducing audio cross-talk and echo due to resistive voltage drops in the audio ground path.

## Physical Dimensions



**Figure 6. 10-Lead, Quad Ultrathin MLP (UMLP), 1.4 × 1.8 mm Body**

**Table 1. Nominal Values**

JEDEC Symbol	Description	Nominal Values (mm)
A	Overall Height	0.5
A1	Package Standoff	0.026
A3	Lead Thickness	0.152
b	Lead Width	0.2
L	Lead Length	0.4
e	Lead Pitch	0.4
D	Body Length (Y)	1.8
E	Body Width (X)	1.4

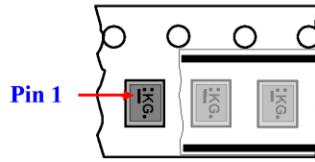
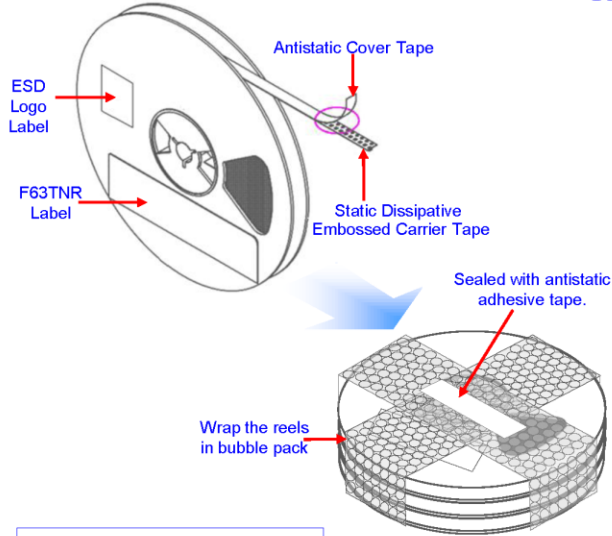
Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/dwg/UM/UMLP10SG.pdf>.

## Packing Specifications

### UMLP10A Packing Configuration: Figure 1.0



Unit Orientation

#### Packing Description:

UMLP 10 pins products are classified under Moisture Sensitive Level 1 at 260°C peak package body temperature.

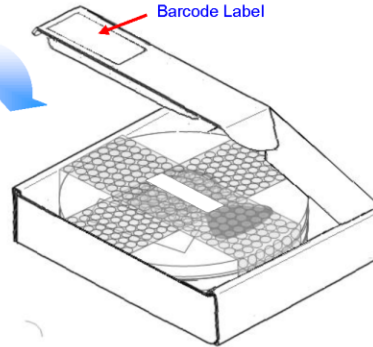
The carrier tape is made from dissipative polystyrene or polycarbonate resin. The cover tape is a multilayer film primarily composed of polyester film, adhesive layer, heat activated sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 5000 units per 178 mm diameter reel. Up to three reels are packed in each intermediate box. The reels are made of polystyrene plastic (anti-static coated or intrinsic).

These full reels are individually barcode labeled and placed inside a pizza box made of recyclable corrugated brown paper with a Fairchild logo printing. These pizza boxes are placed inside a barcode labeled shipping box which comes in different sizes depending on the number of parts shipped.

UMLP10A Packing Information	
Packaging Option	Standard (no flow code)
Packaging type	TNR
Qty per Reel	5000
Reel Size	7" Dia
Box Dimension (mm)	193X183X80
Max qty per Box	15,000

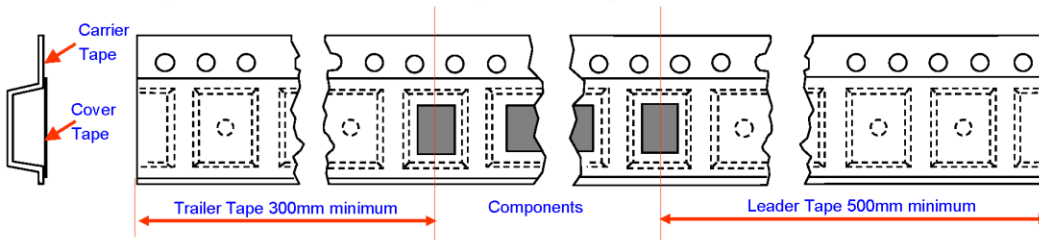
#### F63TNR Label Sample

LOT: PMH01008888	QTY: 5000
FSD: xxxxxxxxxxxxUMX	SPEC:
D/C1: P1338AB QTY1:	SPEC REV: 2 <sup>nd</sup> Level Interconnect
D/C2: QTY2:	1. Category G4
	2. Maximum safe temperature 260 deg C
	3. MSL 1
	FAIRCHILD SEMICONDUCTOR



Standard Intermediate Box

### UMLP10A Tape Leader and Trailer Configuration: Figure 2.0



#### NOTES:

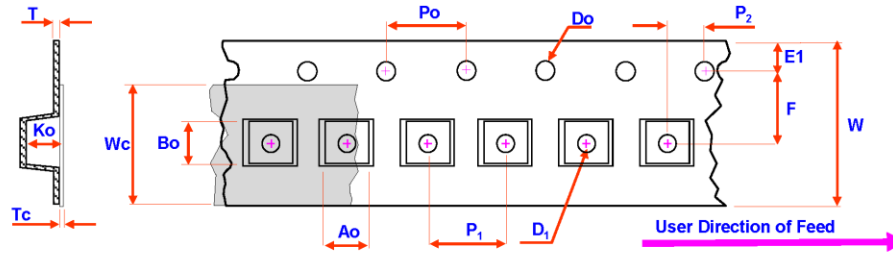
- A : ALL DIMENSION ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED
- B : DRAWING FILE NAME : PKG-UMLP10AREV2
- C : PLASTIC REEL W/1 DIMENSION CONTROL LIMIT OF:  
8MM REEL=±1.0MM AND 12MM REEL AND ABOVE =±1.5MM

Figure 7. 10-Lead, Quad Ultrathin MLP (UMLP), Packing Specification, Page 1



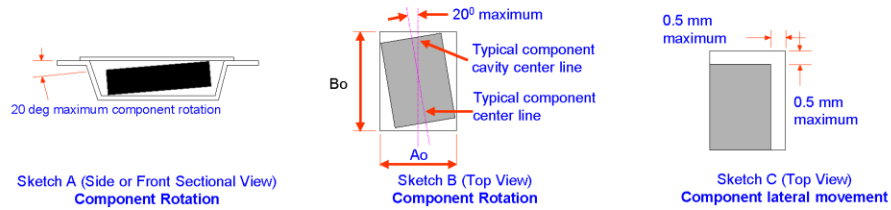
## Packing Specifications

**Embossed Carrier Tape Configuration: Figure 3.0**

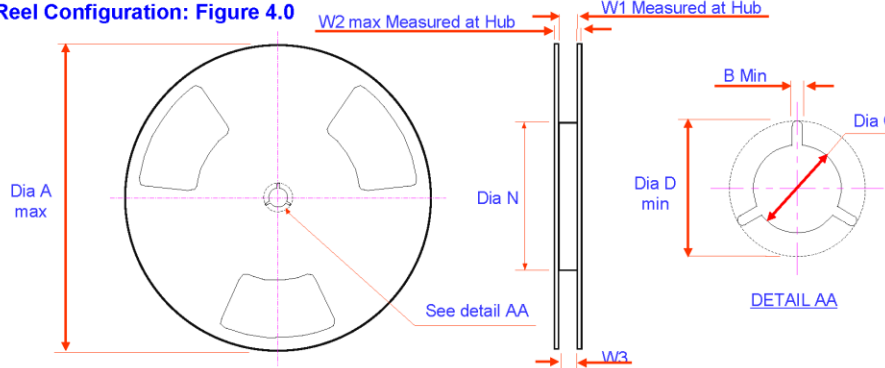


Dimensions are in millimeters															
Package	Ao ±0.05	Bo ±0.05	Do ±0.10	D1 Min	E1 ±0.10	F ±0.10	Ko ±0.05	P1 TYP	Po TYP	P2 ±0.05	T TYP	Tc ±0.05	W ±0.30	Wc TYP	
UMLP1.4x1.8	1.60	2.00	1.50	0.5	1.75	3.5	0.70	4.0	4.0	2.0	0.254	0.06	8.0	5.3	

Notes: Ao, Bo, and Ko dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



**Reel Configuration: Figure 4.0**



Dimensions are in millimeters									
Tape Width	Reel Option	Dia A max	Dia B min	Dia C +0.5/-0.2	Dia D min	Dim N min	Dim W1 +2/-0	Dim W2 Max	Dim W3 (LSL-USL)
8 mm	7" Dia	178.0	1.5	13.0	20.2	55.0	8.4	14.4	7.9~10.9

NOTES:  
 A : ALL DIMENSION ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED  
 B : DRAWING FILE NAME : PKG-UMLP10AREV2  
 C : PLASTIC REEL W1 DIMENSION CONTROL LIMIT OF:  
 8MM REEL=±1.0MM AND 12MM REEL AND ABOVE =±1.5MM

**Figure 8. 10-Lead, Quad Ultrathin MLP (UMLP), Packing Specification, Page 2**

Always visit Fairchild Semiconductor's online packaging area for the most recent drawings:  
 For current packing container specifications, visit Fairchild Semiconductor's online packaging area:  
<http://www.fairchildsemi.com/package/>.



**TRADEMARKS**

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

- |   |  |   |   |
|---|--|---|---|
| AccuPower™  | F-PFST™  |  | Sync-Lock™  |
| AX-CAP®*  | FRFET®   | PowerTrench®  |  SYSTEM GENERAL® |
| BitSiC™   | Global Power Resource™                         | PowerXS™  | TinyBoost®  |
| Build it Now™   | GreenBridge™                                   | Programmable Active Droop™  | TinyBuck®   |
| CorePLUS™   | Green FPS™                                     | QFET®   | TinyCalc™   |
| CorePOWER™  | Green FPS™ e-Series™                           | QST™  | TinyLogic®  |
| CROSSVOLT™  | Gmax™  | Quiet Series™   | TINYOPTO™   |
| CTL™  | GTO™   | RapidConfigure™   | TinyPower™  |
| Current Transfer Logic™   | IntelliMAX™                                    |  | TinyPWM™  |
| DEUXPEED®   | ISOPLANAR™                                     | Saving our world, 1mW/kW at a time™   | TinyWire™   |
| Dual Cool™  | Making Small Speakers Sound Louder and Better™ | SignalMise™   | TransiC™  |
| EcoSPARK®   | MegaBuck™                                      | SmartMax™   | TriFault Detect™  |
| EfficientMax™   | MICROCOUPLER™                                  | SMART START™  | TRUECURRENT®*   |
| ESBC™   | MicroFET™                                      | Solutions for Your Success™   | µSerDes™  |
|  | MicroPak™                                      | SPM®  |  SerDes®         |
| Fairchild®  | MicroPak2™                                     | STEALTH™  | UHC®  |
| Fairchild Semiconductor®  | MillerDrive™                                   | SuperFET®   | Ultra FRFET™  |
| FACT Quiet Series™  | MotionMax™                                     | SuperSOT™-3   | UniFET™   |
| FACT®   | mWSaver®                                       | SuperSOT™-6   | VCM™  |
| FAST®   | OptoHi™  | SuperSOT™-8   | VisualMax™  |
| FastvCore™  | OPTOLOGIC®                                     | SupreMOS®   | VoltagePlus™  |
| FETBench™   | OPTOPLANAR®                                    | SyncFET™  | XST™  |
| FPS™  |  |   |   |

\* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

**DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**ANTI-COUNTERFEITING POLICY**

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, [www.fairchildsemi.com](http://www.fairchildsemi.com), under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

**PRODUCT STATUS DEFINITIONS**

**Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. 166