

CMS35N04V8-HF

N-Channel
RoHS Device
Halogen Free

Features

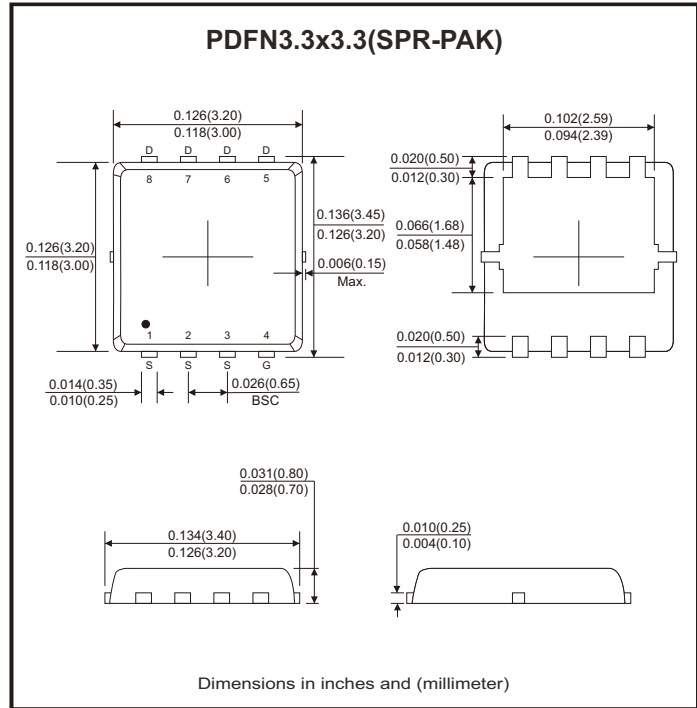
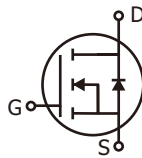
- Advanced DMOS trench technology.
- Fast switching.
- Improve dv/dt capability.
- Green device available.
- 100% EAS guaranteed.

Mechanical data

- Case: PDFN3.3x3.3/SPR-PAK standard package, molded plastic.

Circuit diagram

- G : Gate
- S : Source
- D : Drain



Maximum Ratings

Parameter	Conditions	Symbol	Value	Unit
Drain-source voltage		V_{DS}	40	V
Gate-source voltage		V_{GS}	± 20	V
Continuous drain current (Note 1)	$I_D @ T_C = 25^\circ C$		35	A
	$I_D @ T_C = 100^\circ C$		22.1	
Pulsed drain current (Note 1, 2)		I_{DM}	140	A
Total power dissipation (Note 4)	$P_D @ T_C = 25^\circ C$		44	W
	$P_D @ T_A = 25^\circ C$		2	
Single pulse avalanche energy, L=0.1mH (Note 3)		E_{AS}	61	mJ
Single pulse avalanche current, L=0.1mH (Note 3)		I_{AS}	35	A
Operating junction temperature range		T_J	-55 to +150	$^\circ C$
Storage temperature range		T_{STG}	-55 to +150	$^\circ C$
Thermal resistance junction-ambient (Note 1)	Steady state	$R_{\theta JA}$	62.5	$^\circ C/W$
Thermal resistance junction-case (Note 1)	Steady state	$R_{\theta JC}$	2.8	$^\circ C/W$

Electrical Characteristics (at T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source breakdown voltage	BV _{DSS}	V _{GS} = 0V, I _D = 250μA	40			V
Gate threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1.2	1.7	2.5	
Gate-source leakage current	I _{GSS}	V _{GS} = ±20V			±100	nA
Drain-source leakage current (T _J =25°C)	I _{DSS}	V _{DS} = 40V, V _{GS} = 0V			1	μA
Drain-source leakage current (T _J =85°C)		V _{DS} = 32V, V _{GS} = 0V			10	
Static drain-source on-resistance (Note 2)	R _{DS(on)}	V _{GS} = 10V, I _D = 10A		7.5	9	mΩ
		V _{GS} = 4.5V, I _D = 8A		11	13.5	
Total gate charge (Note 2)	Q _g	I _D = 8A, V _{DS} = 20V, V _{GS} = 10V		19.7		nC
Gate-source charge	Q _{gs}		2.8			
Gate-drain ("miller") charge	Q _{gd}		5.1			
Turn-on delay time (Note 2)	t _{d(on)}	V _{DS} = 15V, V _{GS} = 10V I _D = 1A, R _G = 3.3Ω		13.2		nS
Rise time	t _r		2.2			
Turn-off delay time	t _{d(off)}		72			
Fall time	t _f		4.5			
Input capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = 25V, f = 1MHz		1220		pF
Output capacitance	C _{oss}		130			
Reverse transfer capacitance	C _{rss}		55			
Gate resistance	R _g	f = 1MHz		2.2		Ω
Source-drain diode						
Diode forward voltage (Note 2)	V _{SD}	I _S = 10A, V _{GS} = 0V, T _J =25°C			1.2	V
Continuous source current (Note 1, 6)	I _S	V _G = V _D = 0V, Force current			35	A
Pulsed source current (Note 2, 6)	I _{SM}				70	A
Guaranteed avalanche characteristics						
Single pulse avalanche energy (Note 5)	EAS	V _{DD} = 25V, L=0.1mH, I _{AS} = 18A	16.2			mJ

- Notes: 1. The data tested by surface mounted on a 1 inch² FR-4 board with 2 oz copper.
 2. The data tested by pulsed, pulse width ≤300μs, duty cycle ≤ 2%.
 3. The EAS data shows max. rating. The test condition is V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=35A.
 4. The power dissipation is limited by 150°C junction temperature.
 5. The min. value is 100% EAS tested guarantee.
 6. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

Rating and Characteristic Curves (CMS35N04V8-HF)

Fig.1 - Drain Current vs. T_c

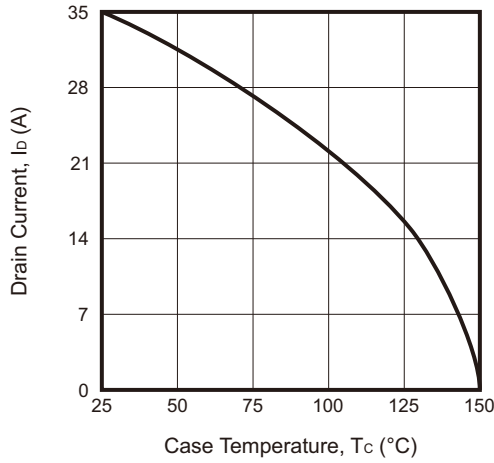


Fig.2 - Gate Charge Characteristics

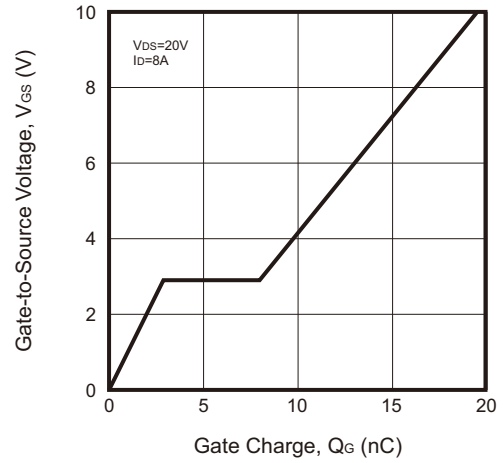


Fig.3 - Normalized $V_{GS(th)}$ vs. T_J

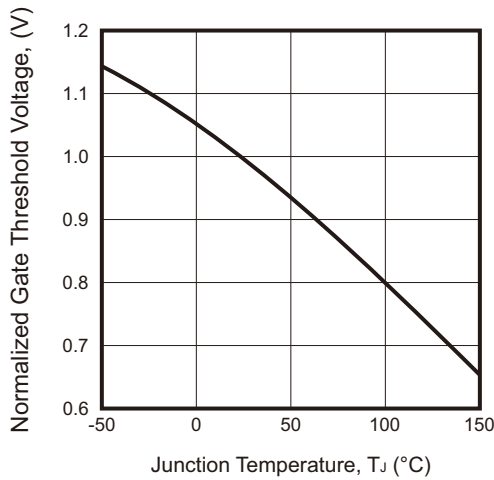


Fig.4 - Normalized $R_{DS(on)}$ vs. T_J

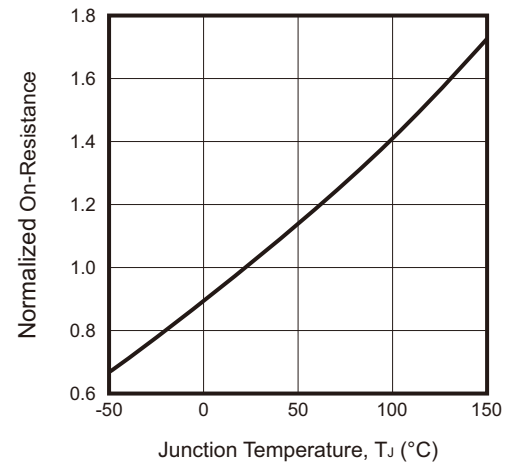
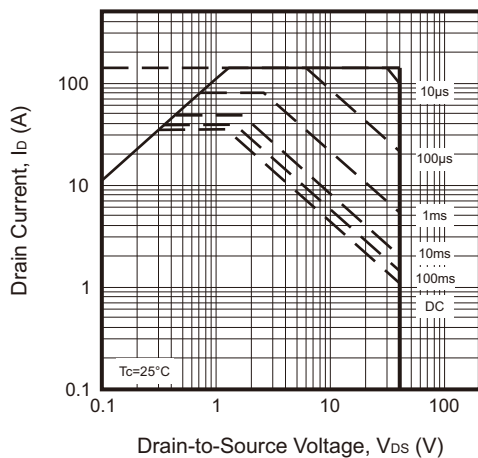
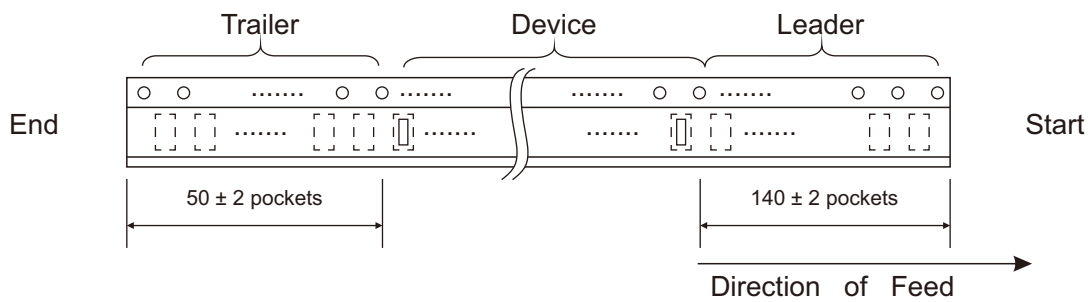
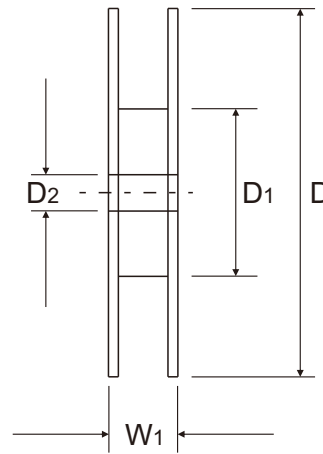
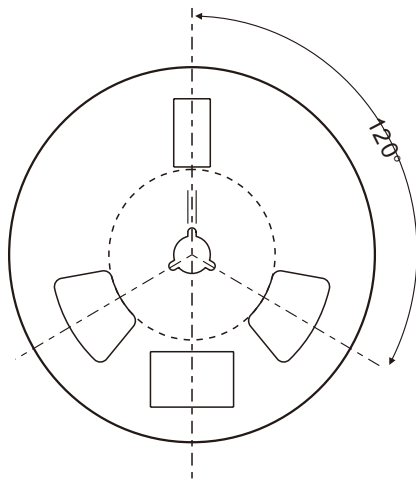
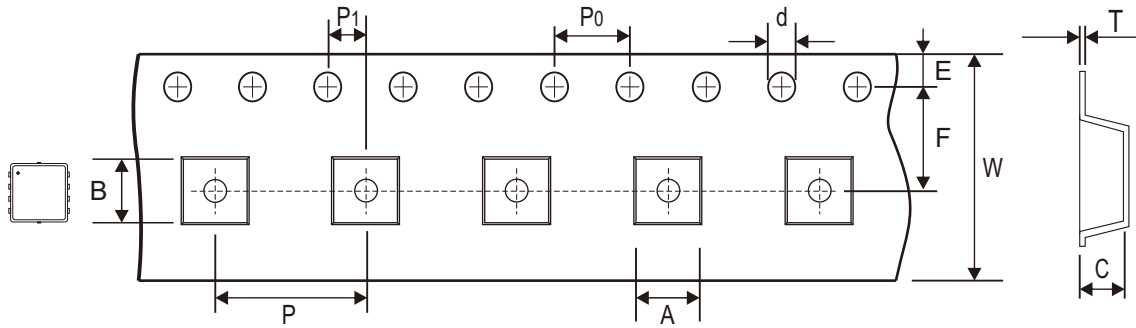


Fig.5 - Safe Operating Area



Reel Taping Specification



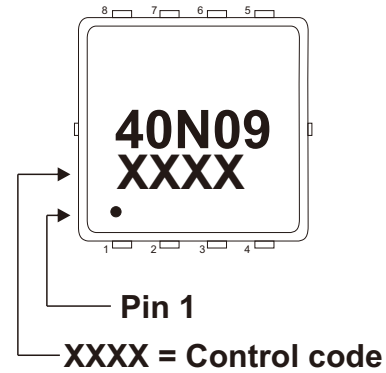
SPR-PAK	SYMBOL	A	B	C	d	D	D1	D2
	(mm)	3.55 ± 0.10	3.55 ± 0.10	1.10 + 0.10 - 0.05	1.50 + 0.10 - 0.00	330.00 ± 1.00	178.00 + 0.00 - 2.00	13.00 min.
	(inch)	0.140 ± 0.004	0.140 ± 0.004	0.043 + 0.004 - 0.002	0.059 + 0.004 - 0.000	12.992 ± 0.039	7.008 + 0.000 - 0.079	0.512 min.

SPR-PAK	SYMBOL	E	F	P	P0	P1	T	W	W1
	(mm)	1.75 ± 0.10	5.50 ± 0.05	8.00 ± 0.10	4.00 ± 0.10	2.00 ± 0.05	0.30 ± 0.05	12.00 + 0.30 - 0.10	18.40 ref.
	(inch)	0.069 ± 0.004	0.217 ± 0.002	0.315 ± 0.004	0.157 ± 0.004	0.079 ± 0.002	0.012 ± 0.002	0.472 + 0.012 - 0.004	0.724 ref.

Company reserves the right to improve product design , functions and reliability without notice. REV:A

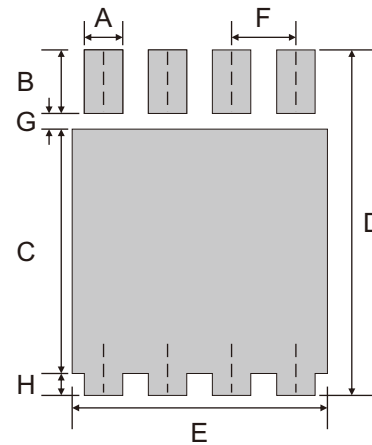
Marking Code

Part Number	Marking Code
CMS35N04V8-HF	40N09 XXXX



Suggested PAD Layout

SIZE	SPR-PAK (PDFN3.3x3.3)	
	(mm)	(inch)
A	0.40	0.016
B	0.60	0.024
C	2.35	0.093
D	3.55	0.140
E	2.80	0.110
F	0.65	0.026
G	0.35	0.014
H	0.25	0.010



Note: 1. The pad layout is for reference purposes only.

Standard Packaging

Case Type	REEL PACK	
	REEL (pcs)	Reel Size (inch)
SPR-PAK (PDFN3.3x3.3)	3000	13