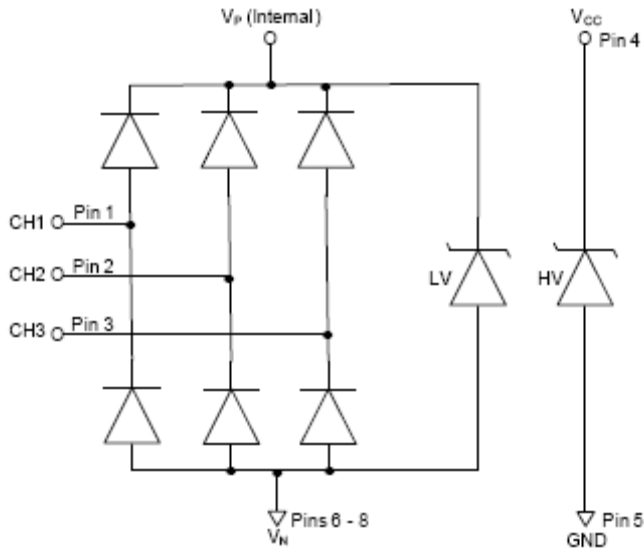


ESD7554

4-Channel Low Capacitance Dual-Voltage ESD Protection Array

Features

- 3 Channels of Low Voltage ESD Protection
- 1 Channel of High Voltage ESD Protection
- Provides ESD Protection to IEC61000-4-2 Level 4:
 - ±8 kV Contact Discharge (Pins 1-3)
 - ±15 kV Contact Discharge (Pin 4)
- Low Channel Input Capacitance
- Minimal Capacitance Change with Temperature and Voltage
- High Voltage Zener Diode Protects Supply Rail
- No Need for External Bypass Capacitors
- Each I/O Pin Can Withstand Over 1000 ESD Strikes*
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



NOTE: Note: Pins 5, and 6 to 8 are connected to a common substrate.

Figure 1. Electrical Schematic

*Standard test condition is IEC61000-4-2 level 4 test circuit with each pin subjected to ±8 kV contact discharge for 1000 pulses. Discharges are timed at 1 second intervals and all 1000 strikes are completed in one continuous test run. The part is then subjected to standard production test to verify that all of the tested parameters are within spec after the 1000 strikes.



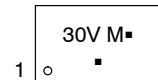
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MARKING DIAGRAM

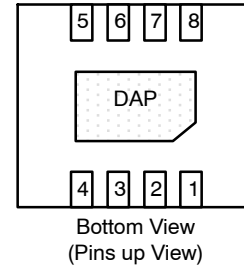


WDFN8
CASE 517BC



30V = Specific Device Code
M = Date Code
■ = Pb-Free Package

PINOUT



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

ESD7554

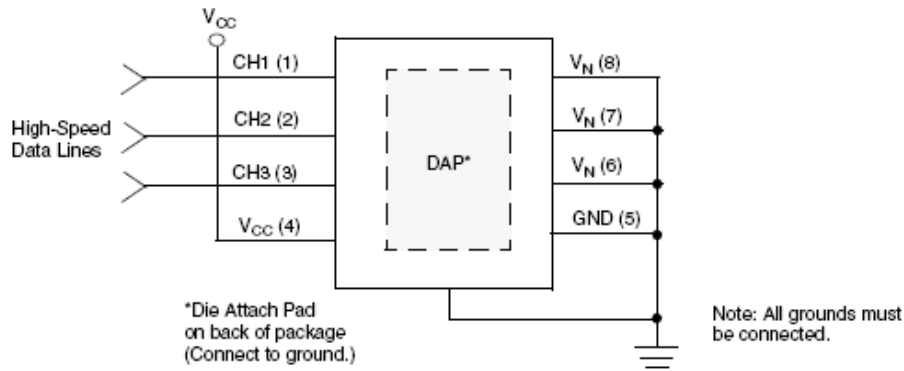


Figure 2. Typical Application

PIN DESCRIPTIONS

| 4-CHANNEL, 8-LEAD, uDFN-8 PACKAGE | | | |
|-----------------------------------|-----------------|--------------------|--------------------------------|
| Pin | Name | Type | Description |
| 1 | CH1 | I/O | LV Low-capacitance ESD Channel |
| 2 | CH2 | I/O | LV Low-capacitance ESD Channel |
| 3 | CH3 | I/O | LV Low-capacitance ESD Channel |
| 4 | V _{CC} | HV V _{DD} | HV ESD Channel |
| 5 | GND | | Ground |
| 6 | V _N | | Negative Voltage Supply Rail |
| 7 | V _N | | Negative Voltage Supply Rail |
| 8 | V _N | | Negative Voltage Supply Rail |
| DAP | GND | | Die Attach Pad (Ground) |

ORDERING INFORMATION

| Device (Note 1) | # of Channels | Leads | Part Marking | Package | Shipping [†] |
|-----------------|---------------|-------|--------------|--------------------------|-----------------------|
| ESD7554MUT2G | 4 | 8 | 30V | uDFN-8, 0.4 mm (Pb-Free) | Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

1. Parts are shipped in Tape and Reel form unless otherwise specified.

ESD7554

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

| Parameter | Rating | Unit |
|---|-------------|------|
| DC Voltage on Low-voltage Pins | 6 | V |
| DC Voltage on High-voltage Pins (V_{CC} pin) | 29 | V |
| Operating Temperature Range | -40 to +85 | °C |
| Storage Temperature Range | -65 to +150 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

STANDARD OPERATING CONDITIONS

| Parameter | Rating | Unit |
|-----------------------------|------------|------|
| Operating Temperature Range | -40 to +85 | °C |

ELECTRICAL OPERATING CHARACTERISTICS (See Note 2)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|--|---|---------------------------------------|-------|------|----------|
| V_F | LV Diode Reverse Voltage (Positive Voltage) | $I_F = 10 \text{ mA}; T_A = 25^\circ\text{C}$ | 6.8 | 8.2 | 9.2 | V |
| | LV Diode Forward Voltage (Negative Voltage) | $I_F = 10 \text{ mA}; T_A = 25^\circ\text{C}$ | -1.05 | -0.9 | -0.6 | V |
| I_{LEAK} | LV Channel Leakage Current (Pins 1 and 2) | $T_A = -30^\circ\text{C to } 65^\circ\text{C}; V_{IN} = 3.3 \text{ V}, V_N = 0 \text{ V}$ | | | 100 | nA |
| | LV Channel Leakage Current (Pin 3 only) | $T_A = -30^\circ\text{C to } 65^\circ\text{C}; V_{IN} = 3.3 \text{ V}, V_N = 0 \text{ V}$ | | | 100 | nA |
| C_{IN} | LV Channel Input Capacitance | At 1 MHz, $V_N = 0 \text{ V}, V_{IN} = 1.65 \text{ V}$ | | 1.2 | 1.5 | pF |
| ΔC_{IN} | LV Channel Input Capacitance Matching | At 1 MHz, $V_N = 0 \text{ V}, V_{IN} = 1.65 \text{ V}$ | | 0.02 | | pF |
| I_{LEAK_HV} | HV Channel Leakage Current | $T_A = 25^\circ\text{C}; V_{CC} = 28 \text{ V}, V_N = 0 \text{ V}$ | | 0.1 | 1.0 | mA |
| C_{IN_HV} | HV Channel Input Capacitance | At 1 MHz, $V_N = 0 \text{ V}, V_{IN} = 2.5 \text{ V}$ | | 30 | | pF |
| V_{F_HV} | HV Diode Breakdown Voltage Positive Voltage | $I_F = 10 \text{ mA}; T_A = 25^\circ\text{C}$ | 30 | | 35 | V |
| V_{ESD} | ESD Protection Peak Discharge Voltage at any channel input, in system Contact discharge per IEC 61000-4-2 standard | $T_A = 25^\circ\text{C}$ | ± 8 (Pin 1-3) ± 15 (Pin 4) | | | kV |
| V_{CL} | LV Channel Clamp Voltage (Pin 1-3) Positive Transients Negative Transients | $T_A = 25^\circ\text{C}, I_{PP} = 1 \text{ A}, t_p = 8/20 \mu\text{S}$ | | +9.64 | | V |
| | | | | -1.75 | | V |
| R_{DYN} | Dynamic Resistance LV Channel Positive Transients LV Channel Negative Transients HV Channel Positive Transients HV Channel Negative Transients | $I_{PP} = 1 \text{ A}, t_p = 8/20 \mu\text{S}$ Any I/O pin to Ground | | 0.72 | | Ω |
| | | | | 0.59 | | |
| | | | | 4.00 | | |
| | | | | 0.20 | | |

2. All parameters specified at $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ unless otherwise noted.

ESD7554

PERFORMANCE INFORMATION

Input channel capacitance performance curves for low voltage pins

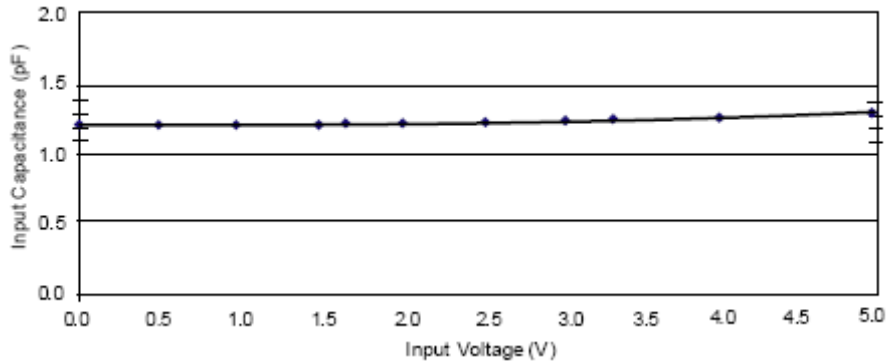


Figure 3. Typical Variation of C_{IN} vs. V_{IN}
(Low Voltage Inputs, $f = 1$ MHz, $V_N = 0$ V)

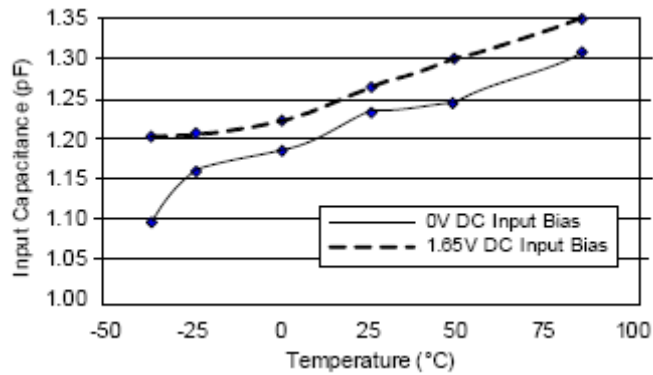


Figure 4. Typical Variation of C_{IN} vs. Temp
(Low Voltage Inputs, $f = 1$ MHz, $V_N = 0$ V)

ESD7554

PERFORMANCE INFORMATION

Typical filter performance for low voltage pins

Nominal conditions unless specified; otherwise, 50 Ω environment

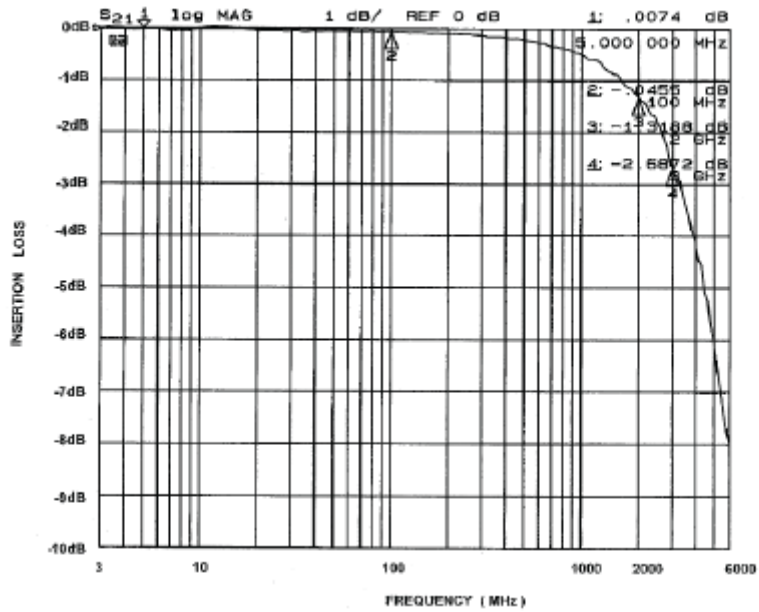


Figure 5. Channel 1 vs. All GND Pins (0 V DC Bias)

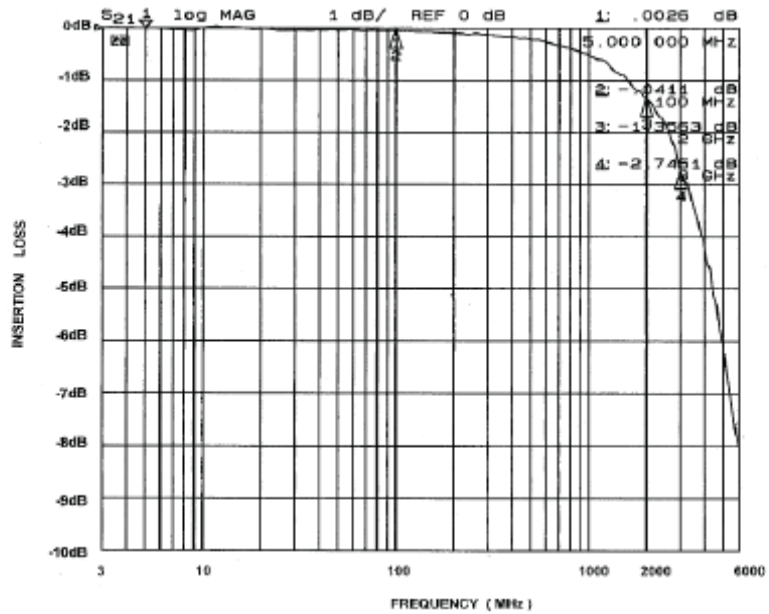


Figure 6. Channel 2 vs. All GND Pins (0 V DC Bias)

ESD7554

PERFORMANCE INFORMATION

Typical filter performance for low voltage pins
Nominal conditions unless specified; otherwise, 50 Ω environment

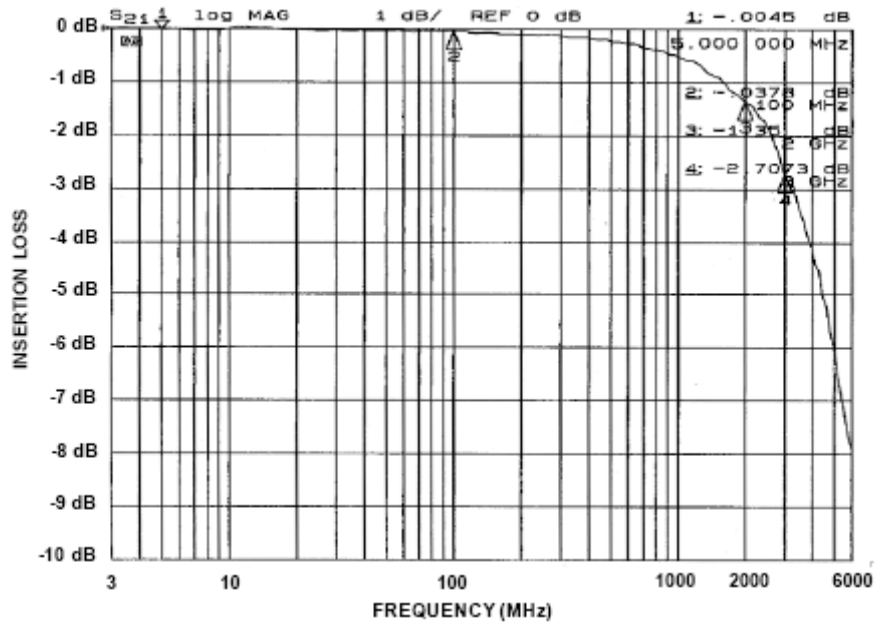


Figure 7. Channel 3 vs. All GND Pins (0 V DC Bias)

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

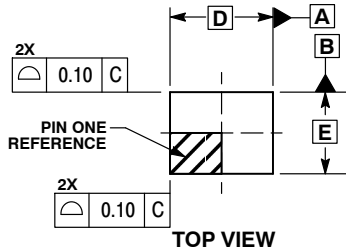
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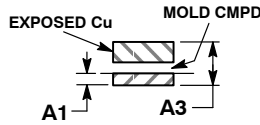
SCALE 4:1

UDFN8, 1.7x1.35, 0.4P
CASE 517BC-01
ISSUE O

DATE 17 NOV 2009



TOP VIEW

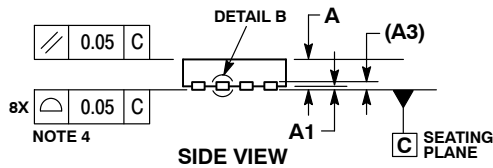


DETAIL B
ALTERNATE
CONSTRUCTIONS

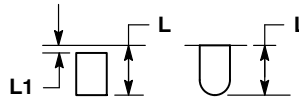
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

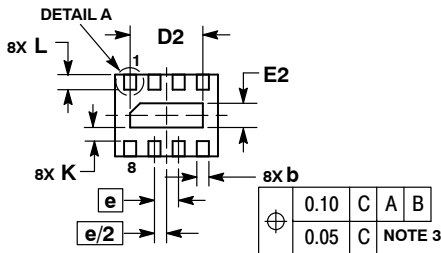
| MILLIMETERS | | |
|-------------|------|------|
| DIM | MIN | MAX |
| A | 0.45 | 0.55 |
| A1 | 0.00 | 0.05 |
| A3 | 0.13 | REF |
| b | 0.15 | 0.25 |
| D | 1.70 | BSC |
| D2 | 1.10 | 1.30 |
| E | 1.35 | BSC |
| E2 | 0.30 | 0.50 |
| e | 0.40 | BSC |
| K | 0.15 | --- |
| L | 0.20 | 0.30 |
| L1 | --- | 0.05 |



SIDE VIEW

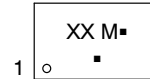


DETAIL A
ALTERNATE TERMINAL
CONSTRUCTIONS



BOTTOM VIEW

GENERIC MARKING DIAGRAM*

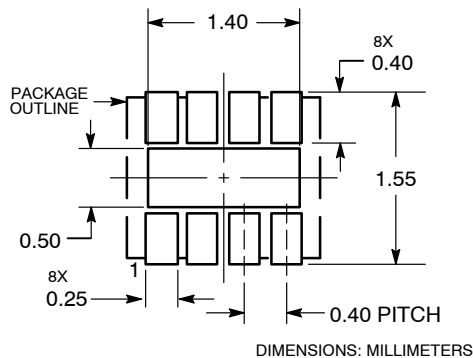


- XX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G", may or not be present.

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
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| DESCRIPTION: | 8 PIN UDFN, 1.7X1.35, 0.4P | PAGE 1 OF 1 |

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