



PUMD4

50 V, 100 mA NPN/PNP resistor-equipped double transistor;
R1 = 10 k Ω , R2 = open

1 October 2022

Product data sheet

1. General description

NPN/PNP double Resistor-Equipped Transistor (RET) in a very small SOT363 (SC-88) Surface-Mounted Device (SMD) plastic package.

NPN/NPN complement: PUMH4

PNP/PNP complement: PUMB4

2. Features and benefits

- Built-in bias resistors
- Simplified circuit design
- Reduction of component count
- Reduced pick and place costs

3. Applications

- Low current peripheral driver
- Replacement for general purpose transistors in digital applications
- Controlling IC inputs

4. Quick reference data

Table 1. Quick reference data

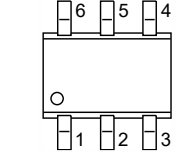
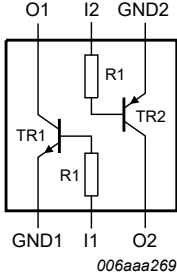
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor; for the PNP transistor with negative polarity						
V _{CEO}	collector-emitter voltage	open base	-	-	50	V
I _O	output current		-	-	100	mA
R1	bias resistor 1 (input)	[1]	7	10	13	k Ω

[1] See section "Test information" for resistor calculation and test conditions.

50 V, 100 mA NPN/PNP resistor-equipped double transistor; R1 = 10 k Ω , R2 = open

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1	 <p>TSSOP6 (SOT363)</p>	 <p>006aaa269</p>
2	I1	input (base) TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2		
5	I2	input (base) TR2		
6	O1	output (collector) TR1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PUMD4	TSSOP6	plastic, surface-mounted package; 6 leads; 0.65 mm pitch; 2.1 mm x 1.25 mm x 0.95 mm body	SOT363

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PUMD4	D%4

[1] % = placeholder for manufacturing site code

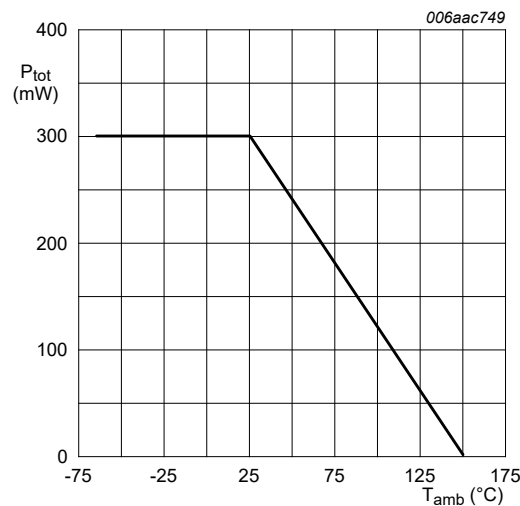
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor; for the PNP transistor with negative polarity						
V_{CBO}	collector-base voltage	open emitter		-	50	V
V_{CEO}	collector-emitter voltage	open base		-	50	V
V_{EBO}	emitter-base voltage	open collector		-	5	V
I_O	output current			-	100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$	[1]	-	200	mW
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-65	150	°C
T_{stg}	storage temperature			-65	150	°C
Per device						
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$	[1]	-	300	mW

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.



FR4 PCB, single-sided, 35 μm copper, tin-plated and standard footprint

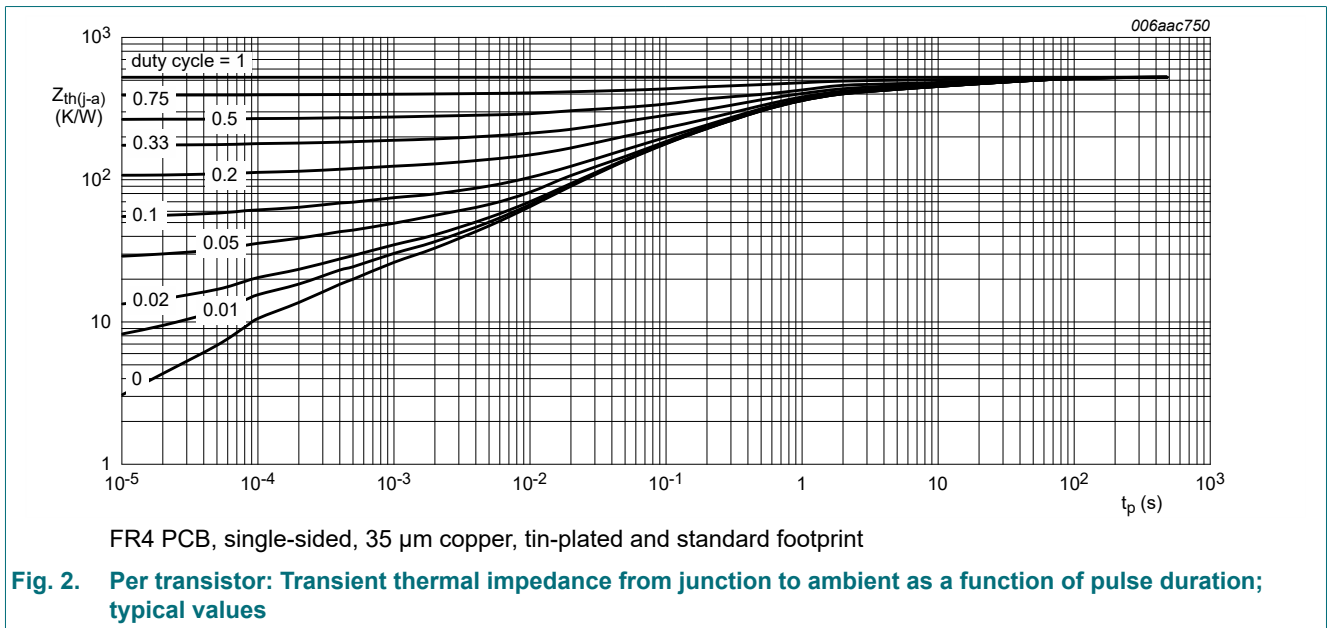
Fig. 1. Per device: Power derating curve

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	625	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	416	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor; for the PNP transistor with negative polarity						
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = 100 \mu\text{A}$; $I_E = 0 \text{ A}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	50	-	-	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	$I_C = 2 \text{ mA}$; $I_B = 0 \text{ A}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	50	-	-	V
I_{CBO}	collector-base cut-off current	$V_{CB} = 50 \text{ V}$; $I_E = 0 \text{ A}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	-	-	100	nA
I_{CEO}	collector-emitter cut-off current	$V_{CE} = 30 \text{ V}$; $I_B = 0 \text{ A}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	-	-	1	μA
		$V_{CE} = 30 \text{ V}$; $I_B = 0 \text{ A}$; $T_j = 150 \text{ }^\circ\text{C}$	-	-	50	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5 \text{ V}$; $I_C = 0 \text{ A}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	-	-	100	nA
h_{FE}	DC current gain	$V_{CE} = 5 \text{ V}$; $I_C = 1 \text{ mA}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	200	-	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 10 \text{ mA}$; $I_B = 0.5 \text{ mA}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	-	-	150	mV
R1	bias resistor 1 (input)		[1]	10	13	kΩ
Transistor TR1 (NPN)						
C_c	collector capacitance	$V_{CB} = 10 \text{ V}$; $I_E = 0 \text{ A}$; $i_e = 0 \text{ A}$; $f = 1 \text{ MHz}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	-	-	2.5	pF
Transistor TR2 (PNP)						
C_c	collector capacitance	$V_{CB} = -10 \text{ V}$; $I_E = 0 \text{ A}$; $i_e = 0 \text{ A}$; $f = 1 \text{ MHz}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	-	-	3	pF

[1] See section "Test information" for resistor calculation and test conditions.

11. Test information

Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R_1 = \frac{V(I_2) - V(I_1)}{I_2 - I_1}$$

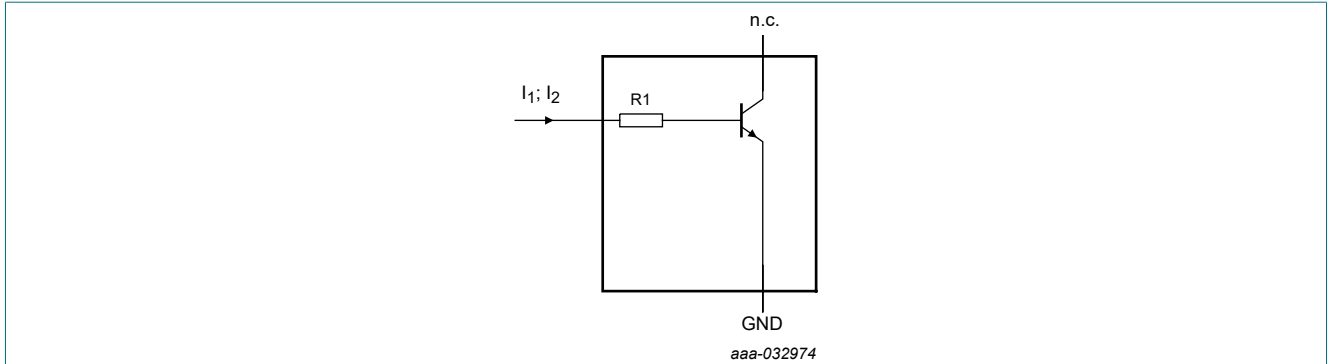


Fig. 3. TR1 (NPN): Resistor test circuit

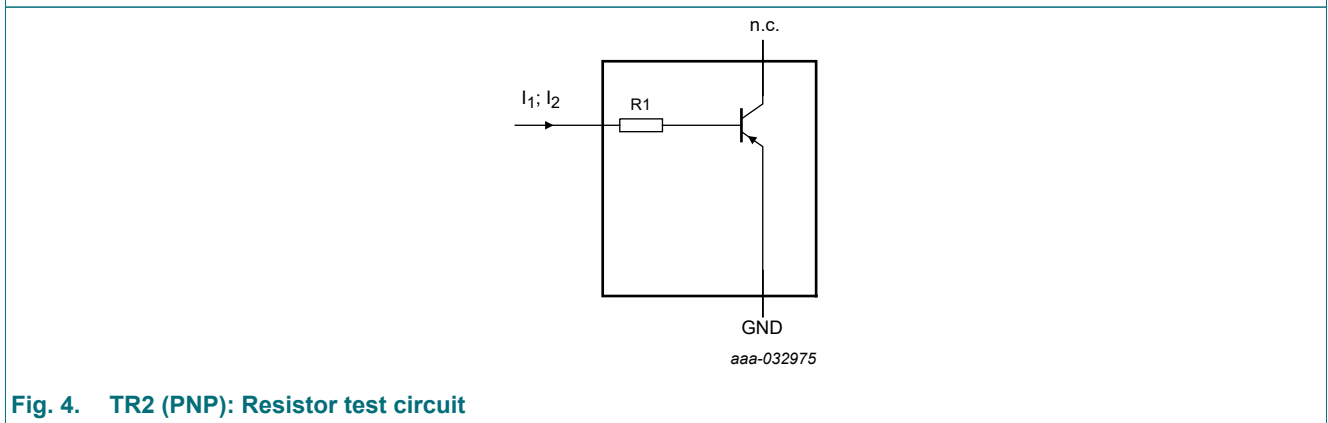


Fig. 4. TR2 (PNP): Resistor test circuit

Resistor test conditions

Table 8. Resistor test conditions

PUMD4	R1 (kΩ)	R2 (open)	Test conditions	
			I ₁	I ₂
TR1 (NPN)	10	-	350 μA	450 μA
TR2 (PNP)	10	-	-350 μA	-450 μA

12. Package outline

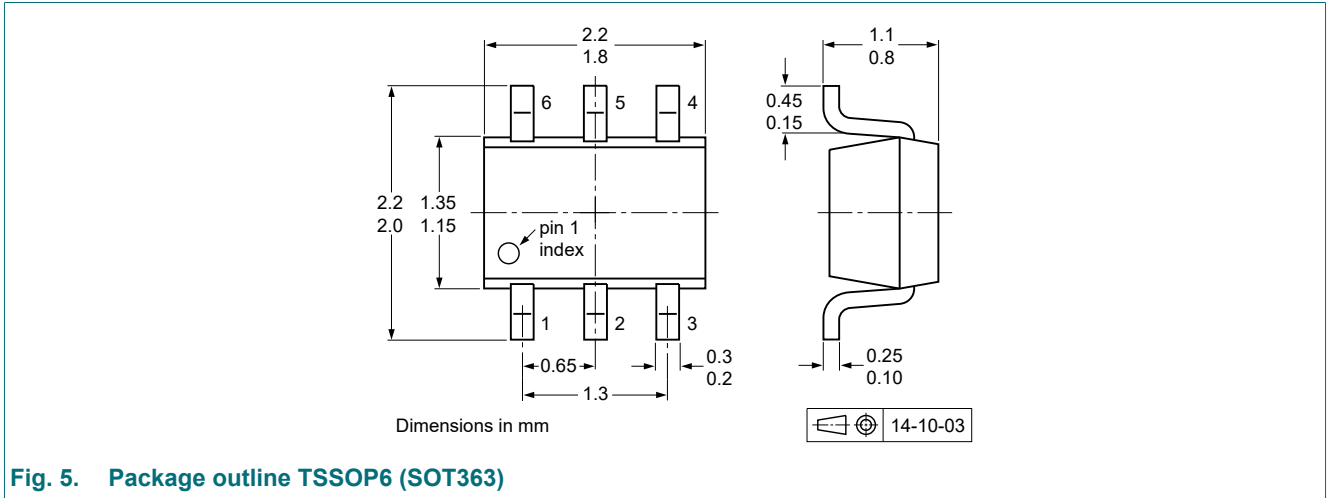


Fig. 5. Package outline TSSOP6 (SOT363)

13. Soldering

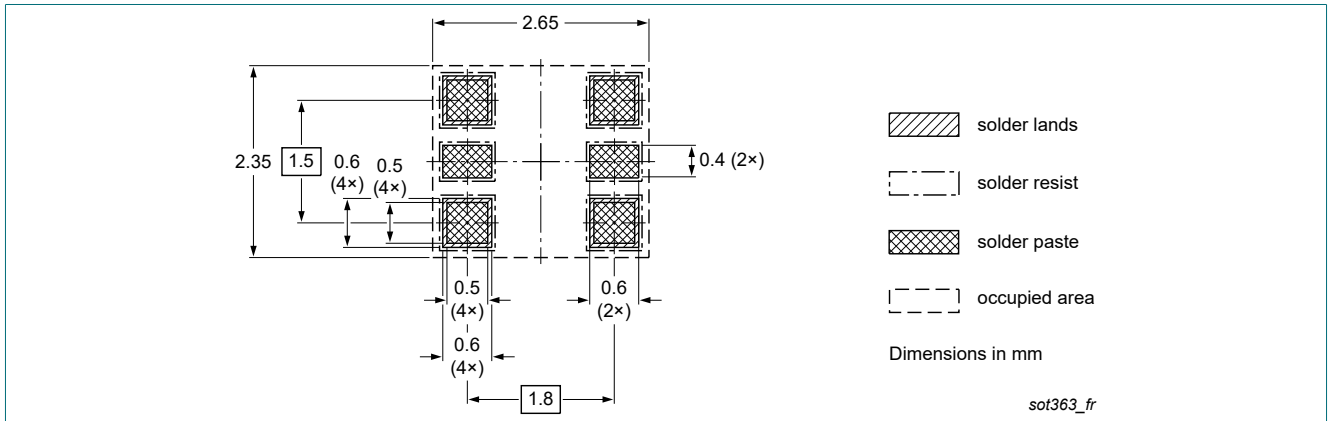


Fig. 6. Reflow soldering footprint for TSSOP6 (SOT363)

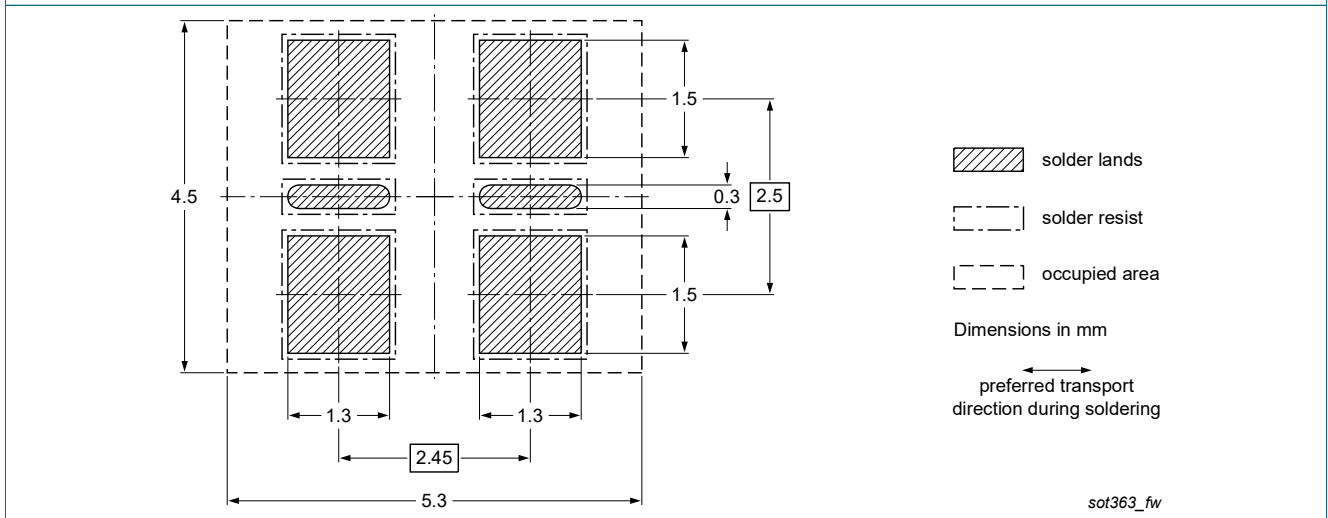


Fig. 7. Wave soldering footprint for TSSOP6 (SOT363)

14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PUMD4 v.3	20221001	Product data sheet	-	PEMD4_PUMD4 v.2
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Family data sheet reduced to single type data sheet. Product changed to non-automotive qualification. Please refer to nexperia.com for automotive (-Q) product alternative(s). 			
PEMD4_PUMD4 v.2	20031010	Product data sheet	-	PEMD4_PUMD4 v.1
PEMD4_PUMD4 v.1	20020114	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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Contents

1. General description.....	1
2. Features and benefits.....	1
3. Applications.....	1
4. Quick reference data.....	1
5. Pinning information.....	2
6. Ordering information.....	2
7. Marking.....	2
8. Limiting values.....	3
9. Thermal characteristics.....	4
10. Characteristics.....	5
11. Test information.....	6
12. Package outline.....	7
13. Soldering.....	8
14. Revision history.....	9
15. Legal information.....	10

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