



# MX555ABD100M000

## Ultra-Low Jitter 100MHz HCSL XO

### ClockWorks® FUSION

### General Description

The MX555ABD100M000 is an ultra-low phase jitter XO with HCSL output optimized for high line rate applications.

### Applications

- PCI Express
- High Speed ADC/DAC
- Storage

### Absolute Maximum Ratings<sup>1</sup>

Supply Voltage (VIN).....	+4.6V
Lead Temperature (soldering, 10s).....	260°C
Case Temperature.....	115°C
Storage Temperature (T <sub>s</sub> ).....	-65°C to +125°C
ESD Machine Model.....	200V
ESD Rating (HBM).....	2kV

### Electrical Characteristics

VDD = 2.5V ±5% or 3.3V ±10%, -40°C to +85°C, outputs terminated with 50 Ohms to VSS.<sup>3</sup>

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
IDD	Supply Current				95	mA
F0	Center Frequency			100		MHz
	Frequency Stability	Note 4			±50	ppm
∅j	Phase Noise	Integration Range (12kHz to 20MHz) Integration Range (1MHz to 20MHz)		135 109	200	fsRMS
Tstart	Start-Up Time				10	ms
TR/TF	Rise/Fall time	20%-80%	150	300	450	ps
	Duty Cycle		48	50	52	%
VOH	Output High Voltage	HCSL output levels	660	700	850	mV
VOL	Output Low Voltage	HCSL output levels	-150	0	27	mV
VOVS	Max Output Including Overshoot				VOH + 0.3	V
VUDS	Min Output Including Undershoot		VOL - 0.3			V
VRB	Ringback Voltage		0.2			V
VOX	Absolute Crossing Point		250	350	550	mV
Vswing	Peak to Peak Output Voltage Swing		640	700	950	mV

#### Notes:

1. Exceeding the absolute maximum ratings may damage the device.
2. The device is not guaranteed to function outside its operating ratings.
3. Guaranteed after thermal equilibrium.
4. Inclusive of initial accuracy, temperature drift, aging, shock, vibration.

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May 27, 2020  
MX555AB1-1510

Revision 1.0  
[tcghelp@microchip.com](mailto:tcghelp@microchip.com)

### Features

- 100MHz HCSL
- PCIe Gen 1/2/3/4/5 Compliant
- Typical phase noise:
  - 109fs (Integration range: 1MHz-20MHz)
- ±50ppm total frequency stability
- -40°C to +85°C temperature range
- Industry standard 6-Pin 5mm x 3.2mm LGA package

### Operating Ratings<sup>2</sup>

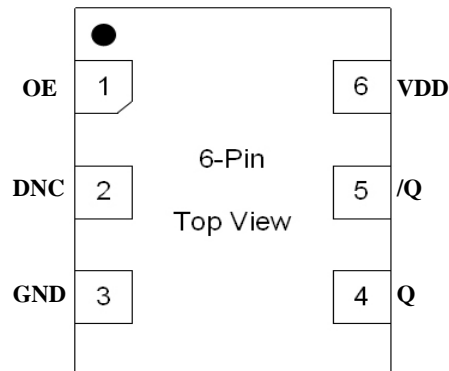
Supply Voltage (VIN).....	+2.375V to +3.63V
Ambient Temperature (TA).....	-40°C to +85°C
Junction Thermal Resistance	
LGA (T <sub>JC</sub> ) Still Air.....	58°C/W

## Ordering Information

Ordering Part Number	Marking Line 1	Marking Line 3	Shipping	Package
MX555ABD100M000	MX555A	BD1000	Tube	6-Pin 5mm x 3.2mm LGA
MX555ABD100M000-TR	MX555A	BD1000	Tape and Reel	6-Pin 5mm x 3.2mm LGA

Devices are Green and RoHS compliant. Sample material may have only a partial top mark.

## Pin Configuration



## Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
1	OE	I, SE	LVC MOS	Output Enable, disables output to tri-state, 0 = Disabled, 1 = Enabled, 50k Ohms Pull-Up (Internal)
2	DNC			Make no connection, leave floating.
3	GND	PWR		Power Supply Ground
4, 5	Q, /Q	O, Diff	HCSL	Clock Output Frequency = 100MHz
6	VDD	PWR		Power Supply

## Environmental Specifications

Thermal Shock	MIL-STD-883, Method 1011, Condition A
Moisture Resistance	MIL-STD-883, Method 1004
Mechanical Shock	MIL-STD-883, Method 2002, Condition C
Mechanical Vibration	MIL-STD-883, Method 2007, Condition A
Resistance to Soldering Heat	J-STD-020C, Table 5-2 Pb-free devices (except 2 cycles max)
Hazardous Substance	Pb-Free / RoHS / Green Compliant
Solderability	JESD22-B102-D Method 2 (Preconditioning E)
Terminal Strength	MIL-STD-883, Method 2004, Test Condition D
Gross Leak	MIL-STD-883, Method 1014, Condition C
Fine Leak	MIL-STD-883, Method 1014, Condition A2, R1=2x10 <sup>-8</sup> atm cc/s
MSL Level	Crystal - MSL-1, Package MSL-3
Solvent Resistance	MIL-STD-202, Method 215

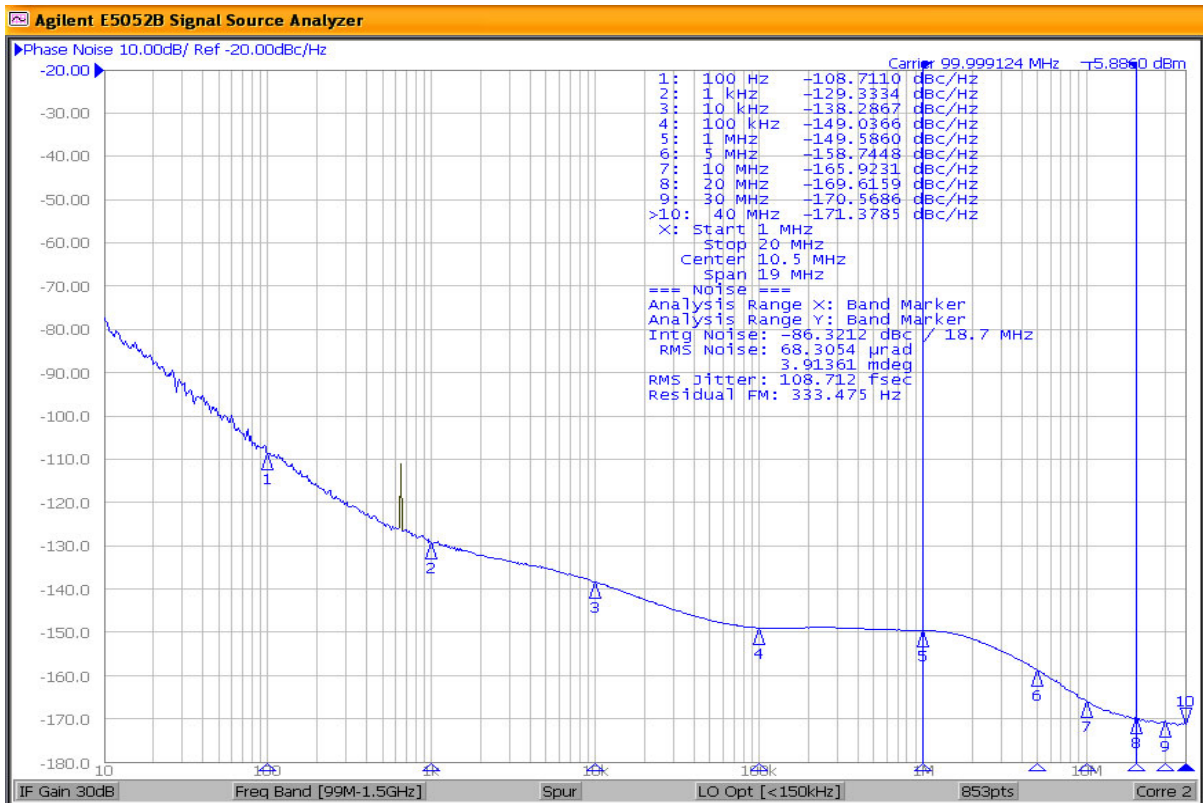


Figure 1. HCSL Output 100MHz 1MHz-20MHz 109fs

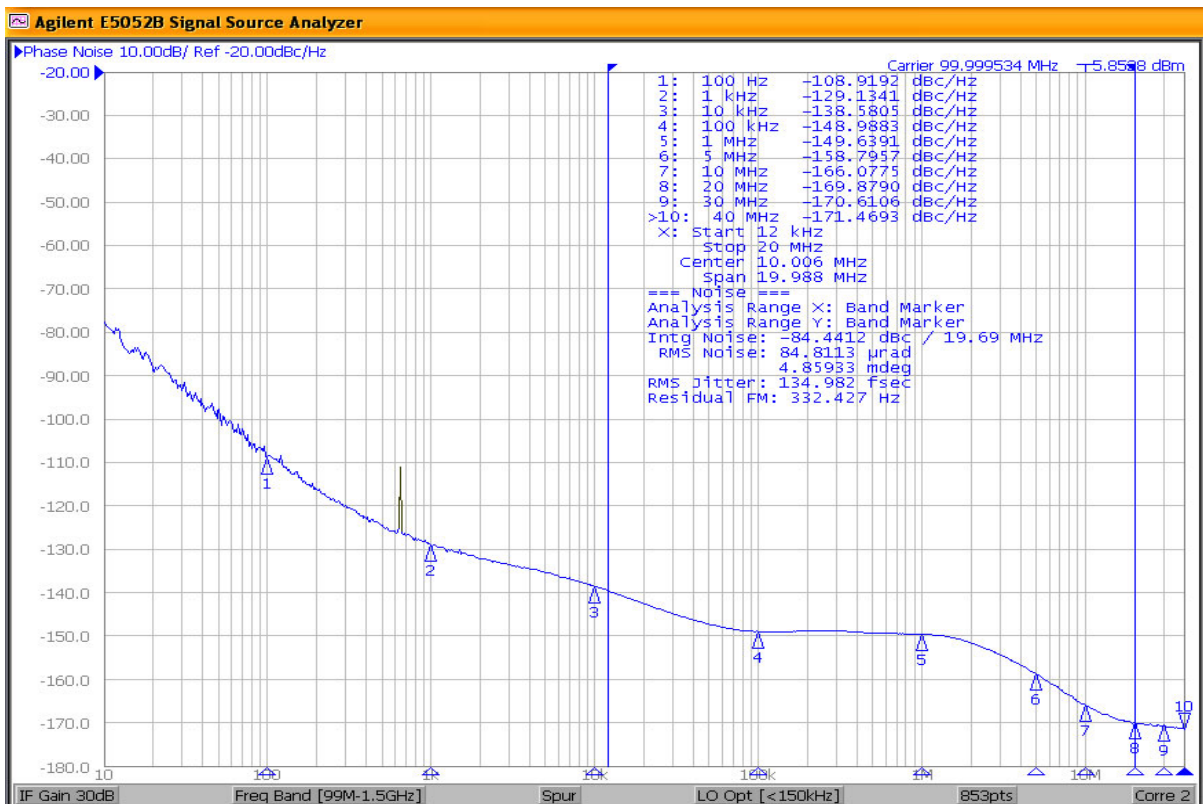


Figure 2. HCSL Output 100MHz 12kHz-20MHz 135fs

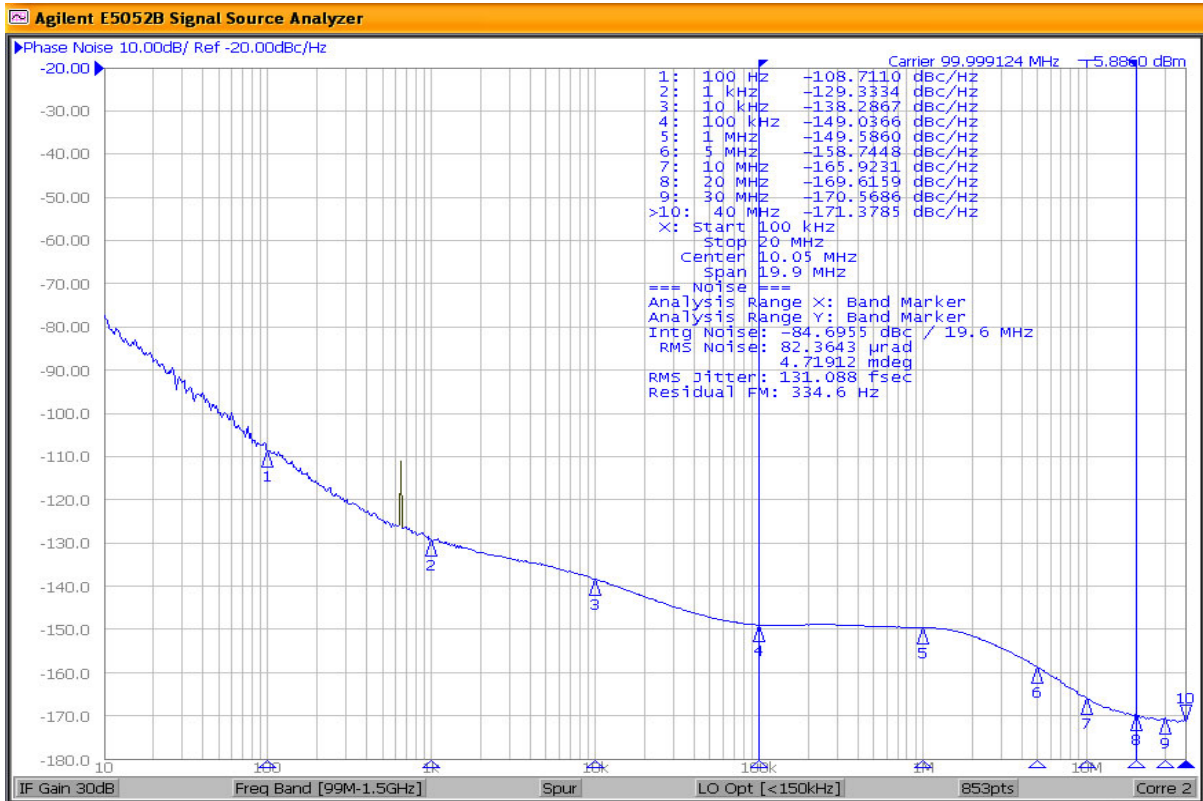
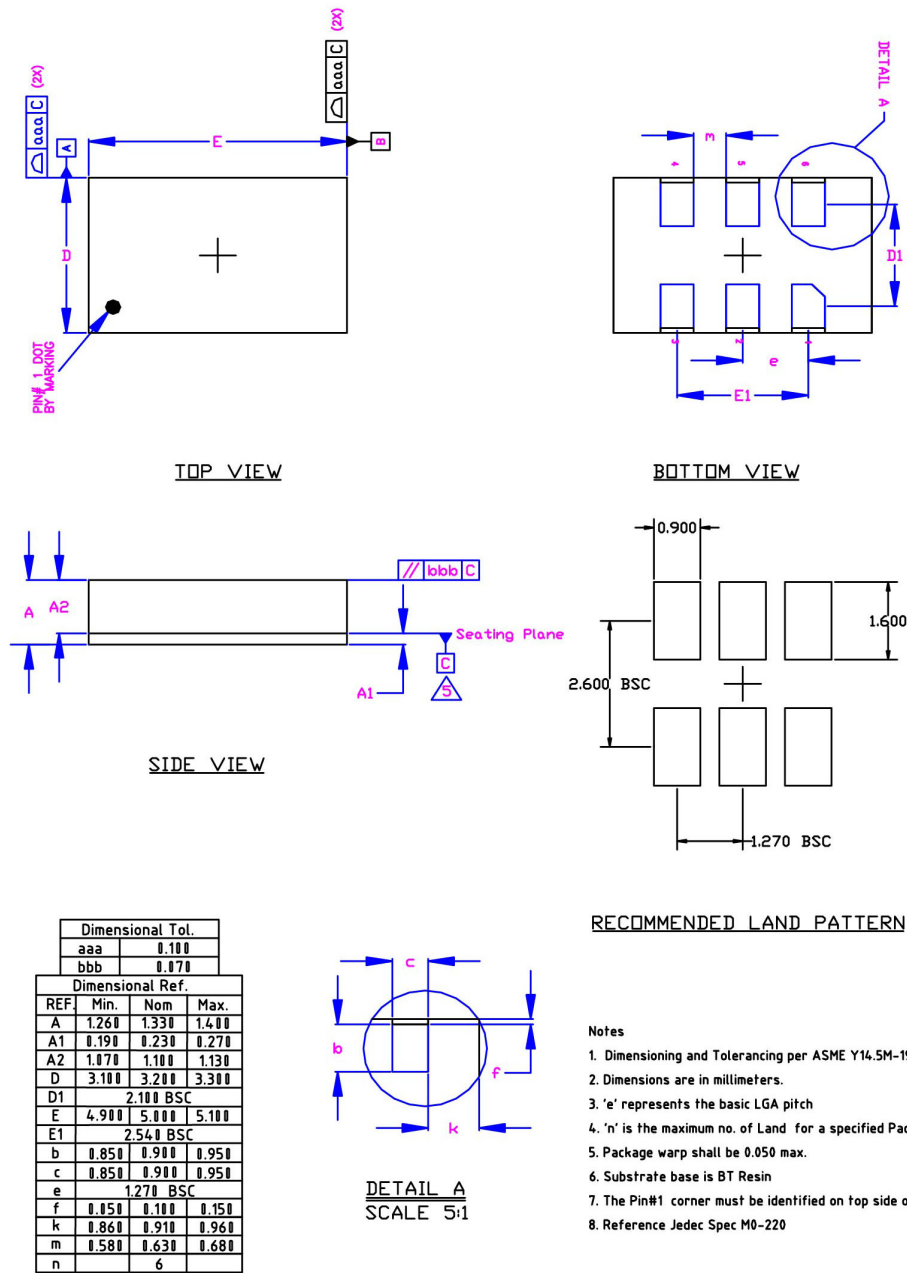


Figure 1. HCSL Output 100MHz 100kHz-20MHz 131fs

### Package Information and Recommended Land Pattern for 6-Pin LGA<sup>3</sup>



**Note:**

3. Package information is correct as of the publication date. For updates and most current information, go to [www.microchip.com](http://www.microchip.com).

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