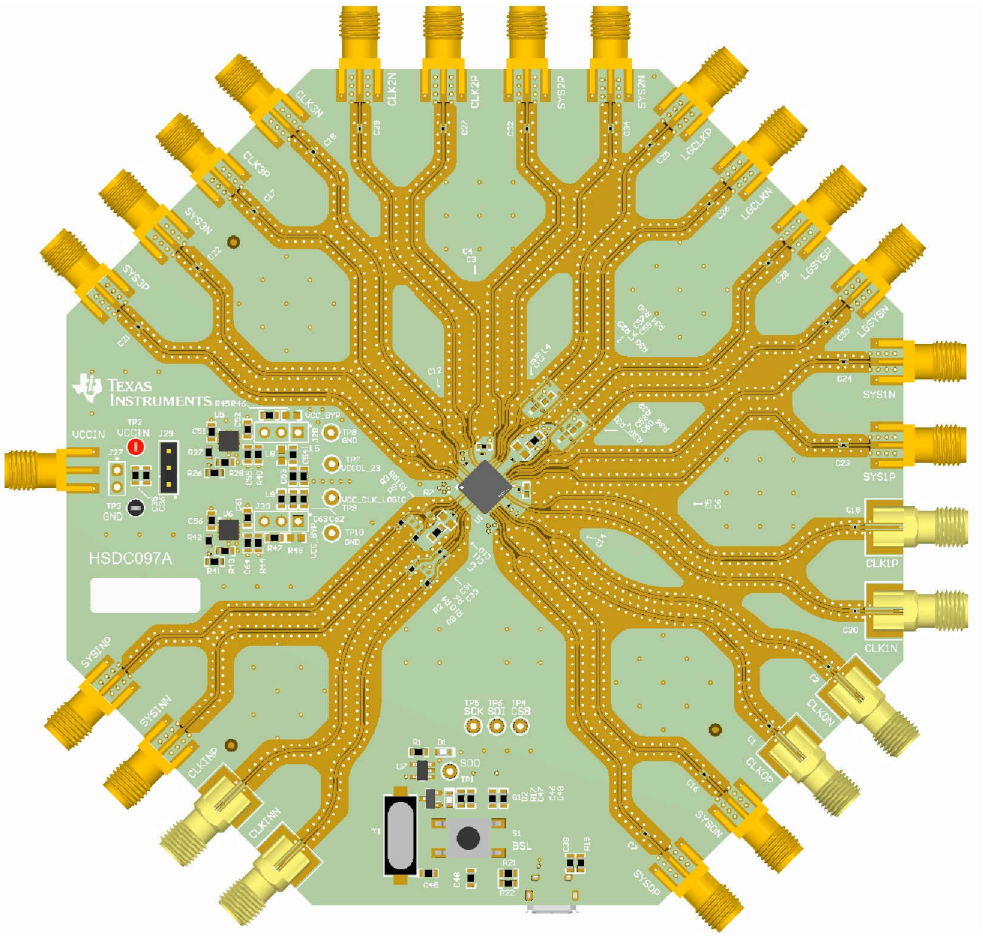
*User's Guide*

# *LMX1204EVM User's Guide*


**ABSTRACT**

The LMX1204EVM is designed to evaluate the performance of LMX1204. This board consists of an LMX1204 device and an integrated USB2ANY programmer.

The LMX1204 is an ultra-low additive-jitter RF buffer, divider, and multiplier, with integrated SYSREF generation capability. The device can buffer RF frequencies up to 12.8 GHz, multiply RF outputs up to 6.4 GHz, and divide outputs by up to 8 GHz. A separate auxiliary clock divider can be used for FPGAs or other logic ICs. Each RF output (and the logic clock) is paired with a complementary SYSREF output with picosecond-precision delay-tuning capability, and can be operated as a generator (with synchronization capability across multiple devices) or as a repeater. The device runs from a single 2.5-V supply, and is programmed by a digital SPI interface from a 1.8-V, 2.5-V, or 3.3-V bus controller.

# Table of Contents

# 1 First-Time Setup

## 1.1 Evaluation Module Contents

Included within each evaluation kit is:

- One LMX1204 EVM board (HSDC097A) with integrated USB2ANY controller
- One USB cable

## 1.2 Evaluation Setup Requirements

At a minimum, evaluation of the buffer mode requires:

- A DC power supply capable of 3.3 V, 2 A
- A high-quality signal source, such as an SMA100B
- A spectrum analyzer or signal analyzer
- A PC with a USB port, running Windows 7 or a more recent version of Windows
- Texas Instruments Clocks and Synthesizers TICS Pro software

Full evaluation requires the following additional hardware:

- A high-speed 4-CH oscilloscope capable of resolving 5-ps step size for SYSREF delay tuning
- A 2-CH arbitrary function generator or other pulse source capable of outputting complementary LVDS pulses and DC levels (1.25 V ± 0.2 V, differential, into 100-Ω DC load) for triggering SYSREF, SYNCing the dividers, and determining SYSREF windowing values
- A phase noise analysis system capable of measuring at up to 12.8 GHz

# 2 EVM Connections

## 2.1 Connection Diagram

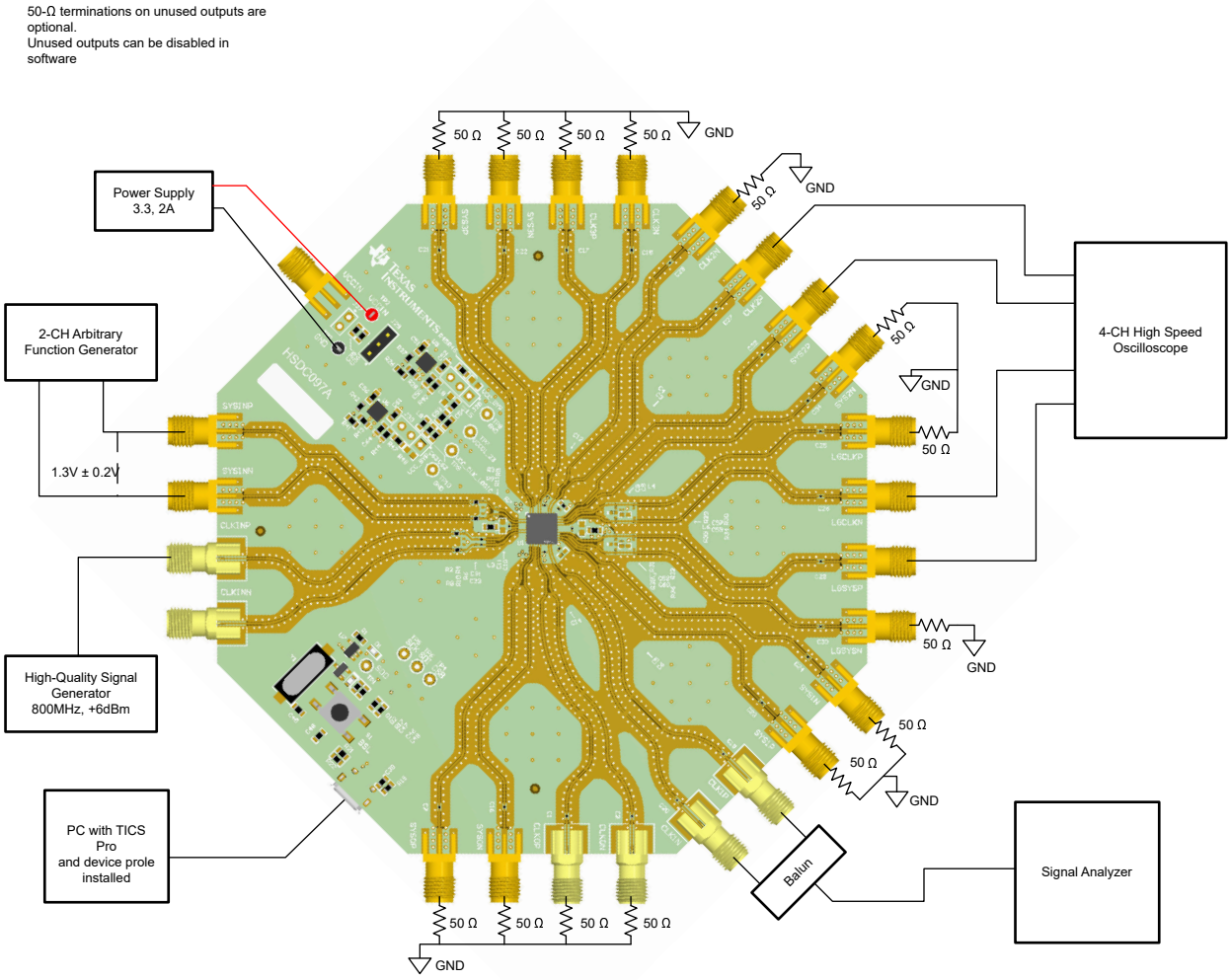



**Figure 2-1. EVM Connection Diagram**

## 2.2 Power Supply

Apply 3.3 V to the J23 header. The acceptable supply voltage range at the board is 3.1 V to 3.5 V, and the device can draw up to 1.3 A during operation, so resistive drop in supply cables can be non-negligible. The on-board LDO has an about 40mA ground current for converting 3.3V to 2.5V supply. Furthermore, enabling or disabling various system functions can change the device current by 50% or more.

## 2.3 Reference Clock

Connect the CLKINP SMA connector to a high-quality signal source such as an SMA100B signal generator. Both CLKIN inputs are terminated internally with 50 Ω to AC-GND (that is, GND connection is formed by an internal capacitor), so no external termination is required or recommended. The other CLKINN SMA connector may be optionally installed beforehand so the input can be driven differentially, provided a suitable balun or differential clock source is available.

The default EVM profile configures the device to evaluate the buffer, multiplier, and divider modes with an 800-MHz CLKIN. This frequency can be modified per the operating range of each functional element if desired. This EVM setup guide and related plots assume 6000-MHz CLKIN for buffer mode and divider mode & 3000-MHz CLKIN for multiplier mode.

If a suitable input source is available, connect the SYSREF input SMAs to a differential output source such as an arbitrary function generator. The EVM connections for the SYSREF input are DC-coupled and provide internal 100-Ω termination with several biasing options. At POR, the EVM automatically applies a weak 1.3-V common mode bias to the SYSREFREQ pins. However, the default EVM profile configures the SYSREF input for DC-coupled input. **In DC-coupled mode, the common mode bias on the SYSREFREQ pins must be between 1 V and 2 V.** The input common mode requirements can be fulfilled with a standard LVDS output buffer.

For evaluating SYNC mode and SYSREF windowing, it is critical to have a SYSREFREQ input source capable of consistently meeting setup and hold requirements for a single cycle of the input clock. This can become very challenging at higher frequencies where setup and hold requirements can be < 50 ps. Another device capable of picosecond-precision timed pulses, such as LMX2820 or LMX2594, could be used as a reference input to both CLKIN and SYSREF for evaluating these features.

## 2.4 Output Connections

Connect any of the CLKOUT SMA connectors to a signal analyzer. All CLKOUT connections are AC-coupled at the LMX1204EVM and can be connected directly to RF instruments with 0VDC requirements; an additional DC block is not required. The unused CLKOUT SMA connector must be terminated with a 50-Ω load, or a differential connection may be used if a balun with a suitable frequency range is available.

If additional hardware such as a high-speed oscilloscope and phase noise analyzer are available, they may also be connected to the output SMA connectors. Recommended oscilloscope connections include one CLKOUT and one SYSREF output from the same channel, as well as the one LOGICLK and one LOGISYS output.

Other unused CLKOUT SMA connectors should be terminated with 50-Ω single-ended or 100-Ω differential load, or alternately should be disabled in software, to minimize unterminated output effects on performance.

## 2.5 Programming Interface

After the 3.3-V power supply has been connected and power has been applied to the EVM, connect the USB cable from the PC to the EVM. The USB interface will provide the necessary power to enable the onboard USB2ANY controller. A firmware update may be required; if prompted, see Appendix B for more details.

Run TICS Pro software and open the device profile:

1. From the top-menu, click *Select Device → Clock Distribution with Divider → LMX1204*

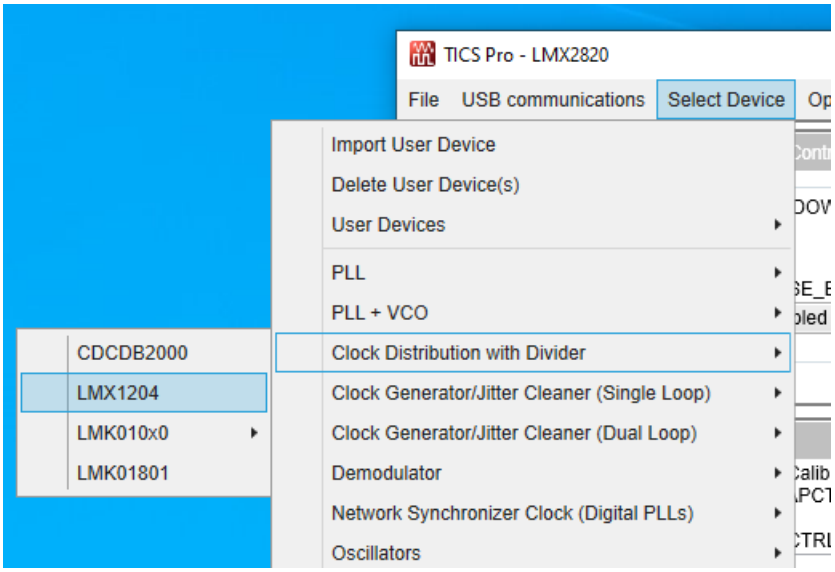



**Figure 2-2. Select Device Menu**

2. The device's *Main Page* will load. The default profile is configured for 800-MHz buffer mode.

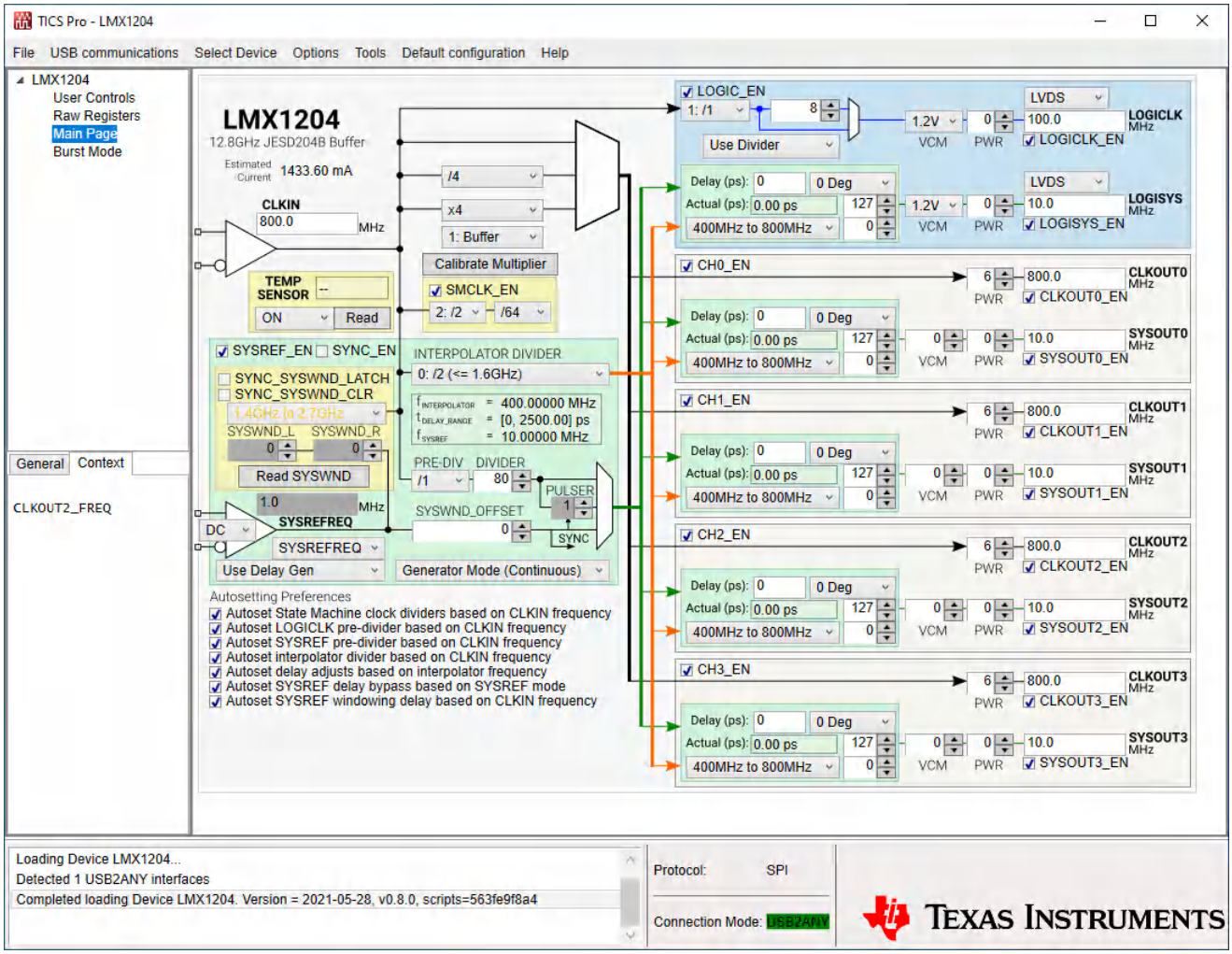



**Figure 2-3. LMX1204 Main Page**

3. From the top-menu, click *USB communications* → *Interface*. Ensure that the selected interface is *USB2ANY* and that the correct controller is selected. To confirm controller selection, click the *Identify* button to blink the onboard green communications LED several times in rapid succession; the LED will return to solid green when complete. After confirming the USB2ANY connection, close the interface window.

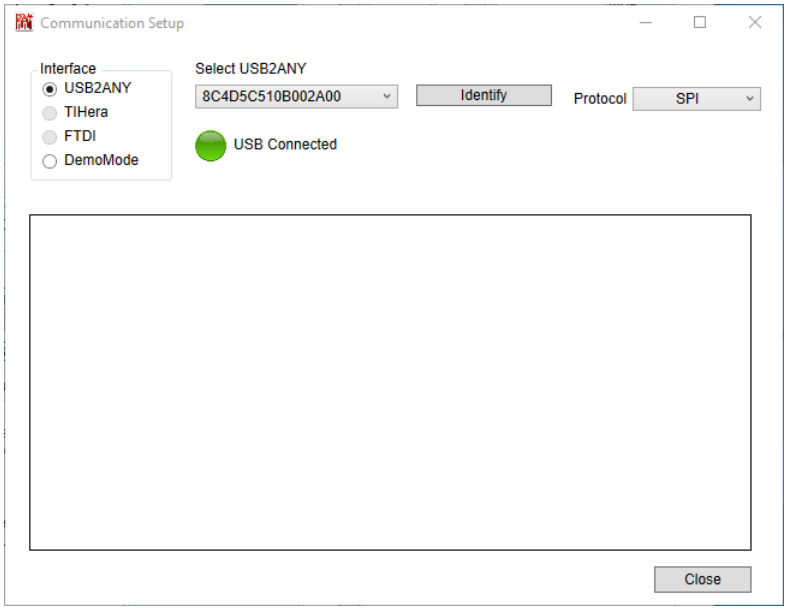



**Figure 2-4. Communication Setup**

4. Ensure that the main window now shows the USB2ANY connection over SPI.

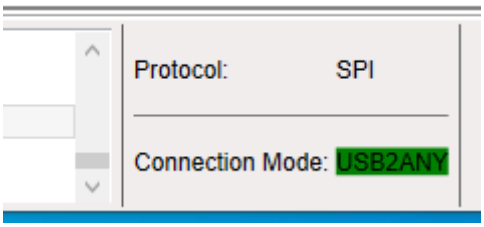



**Figure 2-5. Connection Mode**

# 3 Feature Evaluation

The following sections describe evaluation of the device features, including buffer mode, multiplier mode, and divider mode; SYSREF generation and pulse output; SYSREF delay adjustment; SYSREF windowing; and divider synchronization.

## 3.1 Buffer, Divider, and Multiplier Modes

From the top-menu, click **Default Configuration** → **800MHz Buffer Mode**. This will automatically load the buffer mode profile.

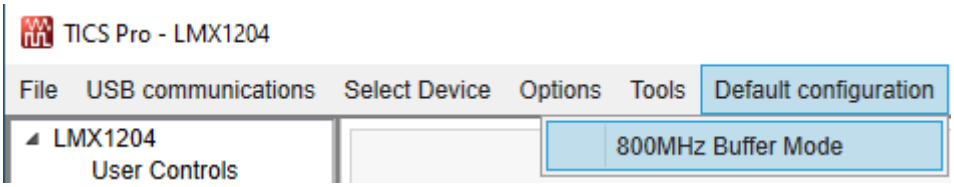



**Figure 3-1. Loading the Default Configuration**

If termination is not applied on all output pins, manually disable the unused outputs using the CHx_EN fields (to completely power down unused channels) or the CLKOUTx_EN, SYSOUTx_EN, and LOGICLK_EN/ LOGISYS_EN fields (to power down output buffers only). Powering down unused channels greatly reduces current consumption, and for the logic clocks in particular can reduce spurious interference.

After the profile is loaded and any changes required have been made, the signal analyzer should see an 6000-MHz signal at around +6-dBm single-ended, or +9-dBm differential.

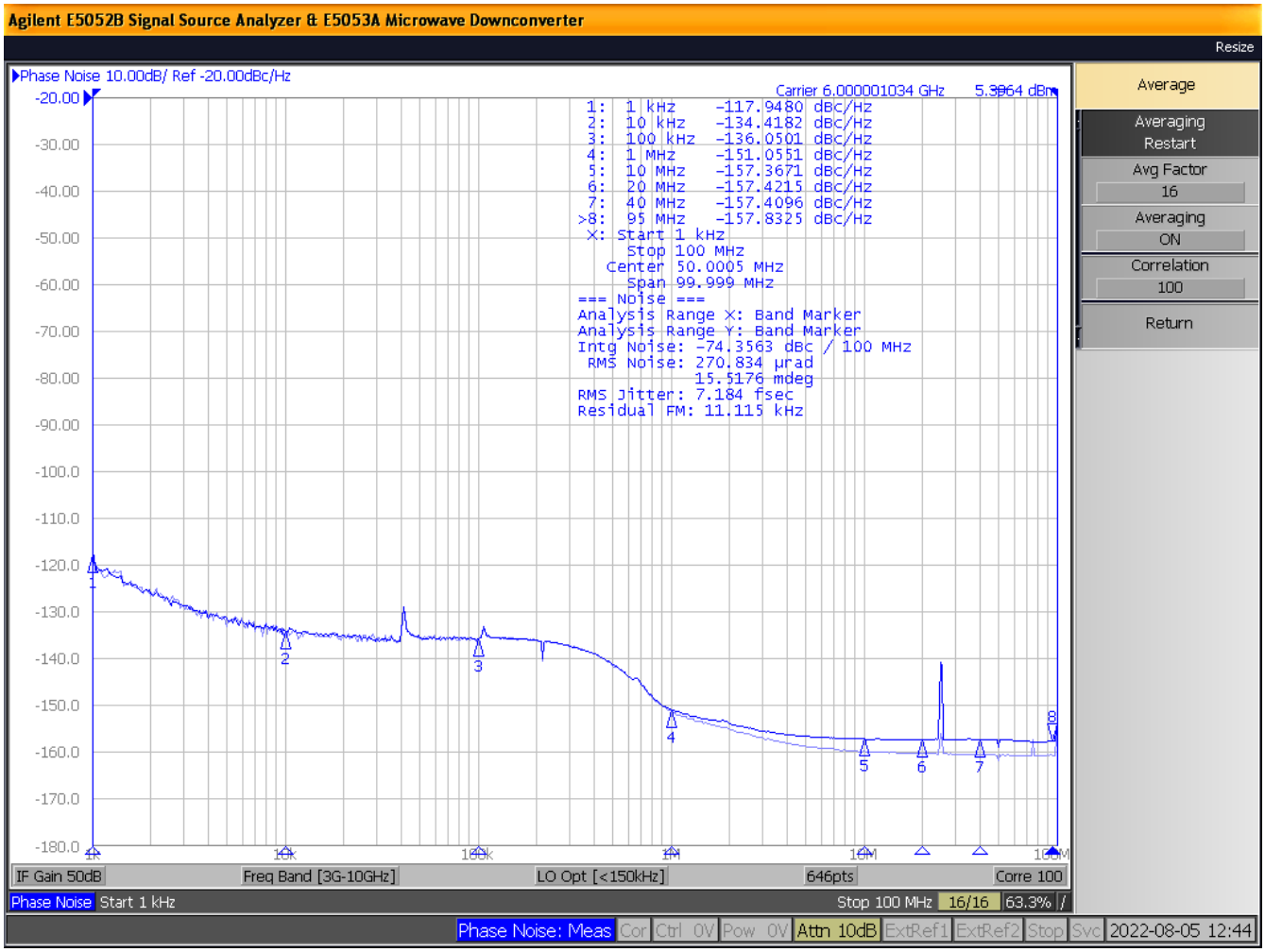



**Figure 3-2. 6000-MHz Buffer Mode Signal Analyzer Plot**

To activate the multiplier or the divider, change the CLK_MUX field to specify divider or multiplier modes, and change the CLK_DIV and CLK_MULT fields to specify the frequency scaling factor. To ensure the device cleanly enters each mode, first the desired configuration should be prepared in the GUI, then from the **User Controls** page the device should be reset by toggling the RESET field, and finally the registers should be reloaded using the **USB Communications** → **Write All Registers** menu option, or by pressing the accelerator keys **CTRL + L**.

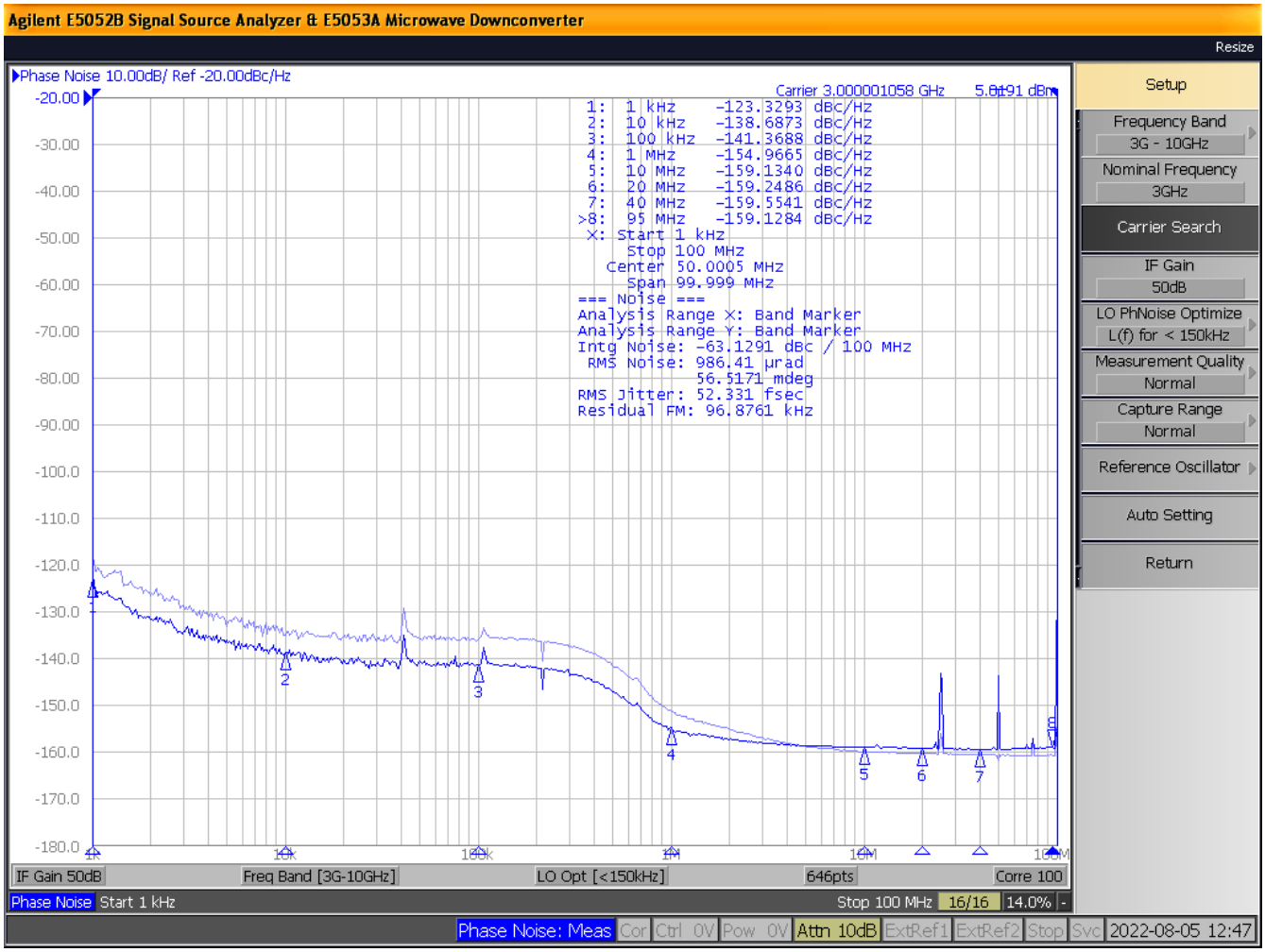



**Figure 3-3. 3000-MHz Divide-by-2 Mode Signal Analyzer Plot**

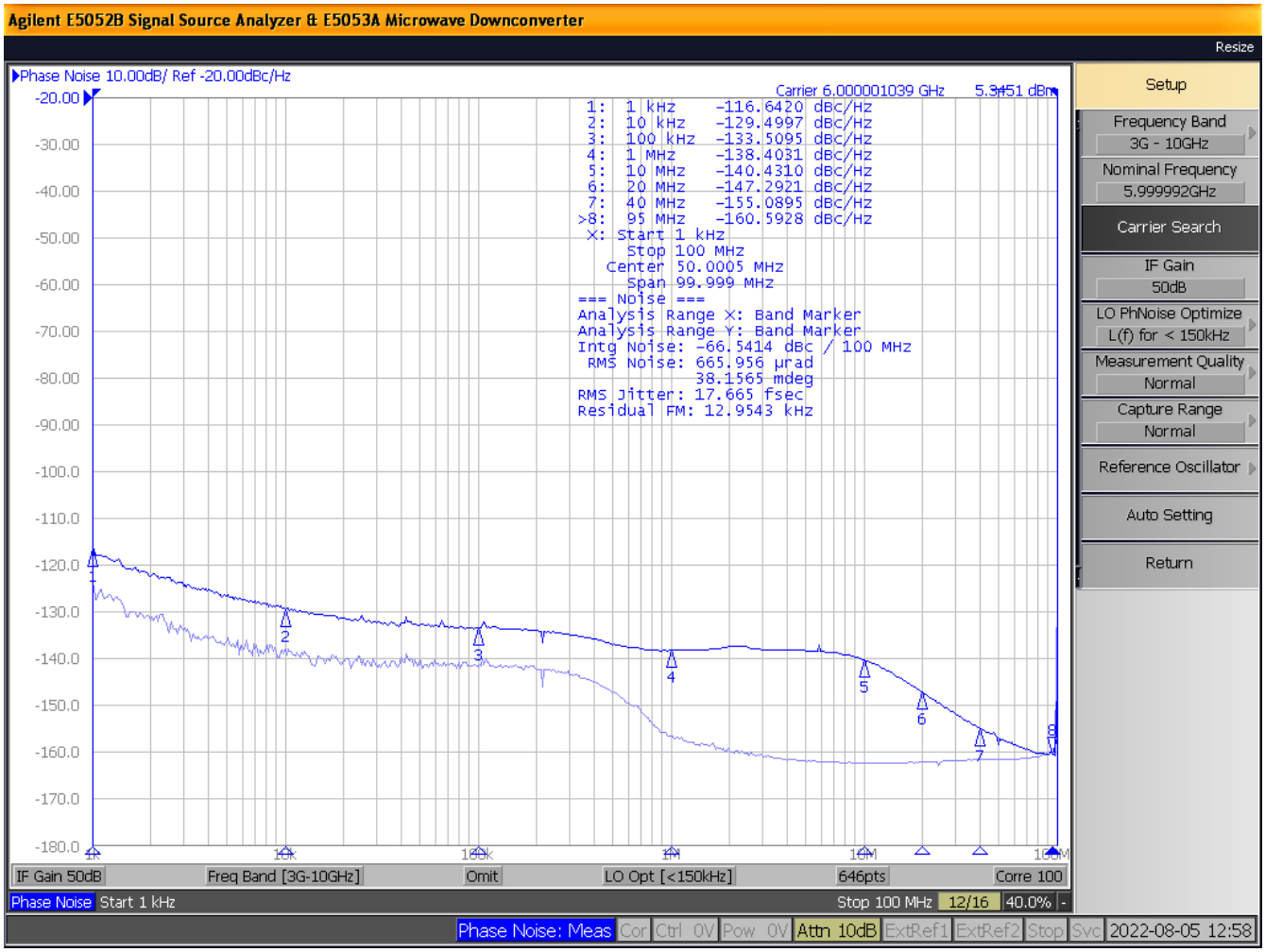



**Figure 3-4. 6000-MHz Multiplier x2 Mode Signal Analyzer Plot**

## 3.2 SYSREF Generation

The SYSREF generation circuit includes a SYSREF pre-divider and post-divider, a pulser with programmable pulse quantity, and a repeater mode bypass. The SYSREF generator modes re-time the SYSREF signal to the output clock, ensuring the SYSREF output is close to the falling edge of the clock output with default delay settings. Repeater mode timing is solely determined by the propagation delay of the device.

To activate the SYSREF generation circuit, the following conditions must be satisfied:

- SRREQ_MODE field must be set to SYSREFREQ mode
- SYSREF_MODE field must be set to the appropriate condition: Continuous, Pulser, or Repeater
- In generator modes (continuous or pulser), $F_{INTERPOLATOR}$ % $F_{SYSREF}$ = 0 must be ensured.
- SYSREF_DLY_BYP field must be configured appropriately for generator or repeater modes (a GUI autoset condition normally ensures this whenever SYSREF_MODE is set)
- SRREQ_VCM field should be set to DC-coupled mode for continuous or pulsed generator output. In repeater mode output, the SYSREF input may be AC- or DC-coupled and SRREQ_VCM should be set accordingly.
- For continuous mode, a HIGH signal must be seen on SYSREFREQ pins continuously. For pulsed generator mode, a LOW→HIGH transition must be seen on SYSREFREQ pins to trigger the pulser. For repeater mode, the output will follow the input state.

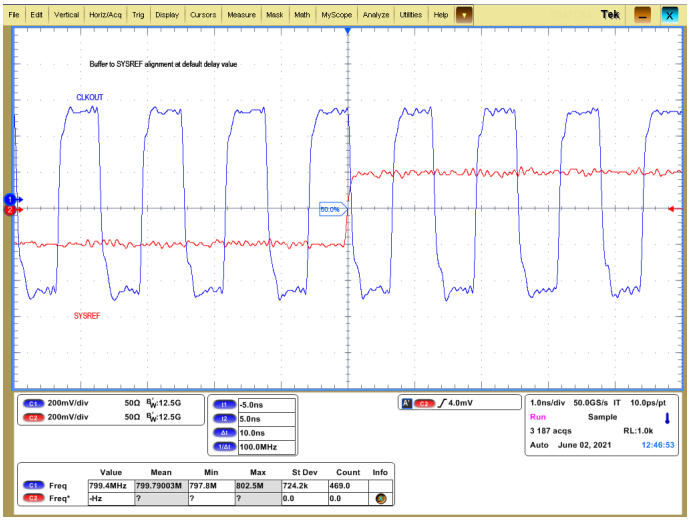



**Figure 3-5. 800-MHz Buffer Mode With SYSREF**

The SYSREF generator frequency is based on the CLKIN frequency, but the re-timing happens at the output frequency; consequently, the SYSREF generator still matches to the falling edge of the clock input even for multiplier and divider modes.

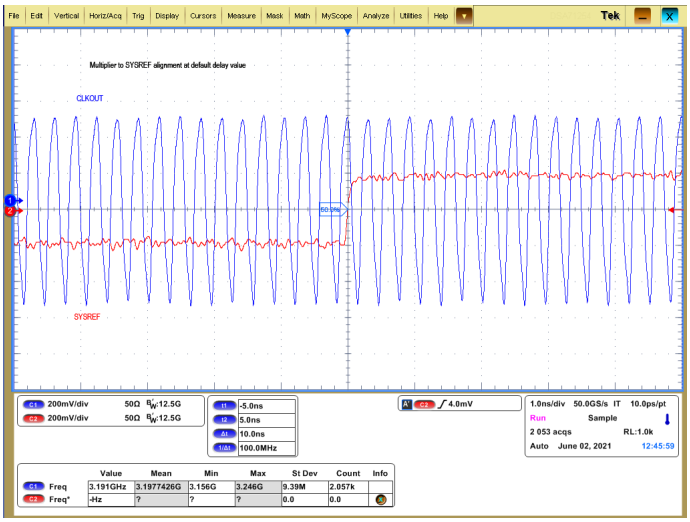



**Figure 3-6. 3200-MHz Multiplier Mode With CLKOUT, LOGICLK, and SYSREF**

## 3.3 SYSREF Delay Generators

In generator modes, the SYSREF can be delayed by picosecond-size steps to more closely meet setup and hold requirements for high-frequency clock outputs. A delay divider, SYSREF_DLY_DIV, generates the interpolator frequency $f_{INTERPOLATOR}$, which is usually in the range of 400 MHz to 800 MHz. This interpolator frequency is further subdivided into 512 delay codes, allowing approximately 2.5-ps to 5-ps delay steps across most of the CLKIN frequency range.

Each channel has its own delay codes which can be entered. The delay code algorithm is documented in the data sheet. To simplify delay calculation, the GUI provides an estimated relative delay: enter the relative delay, and the GUI will calculate the correct step values to achieve the requested delay as closely as possible. Alternately, the register-based delay fields can be stepped through or programmed to achieve the same result.

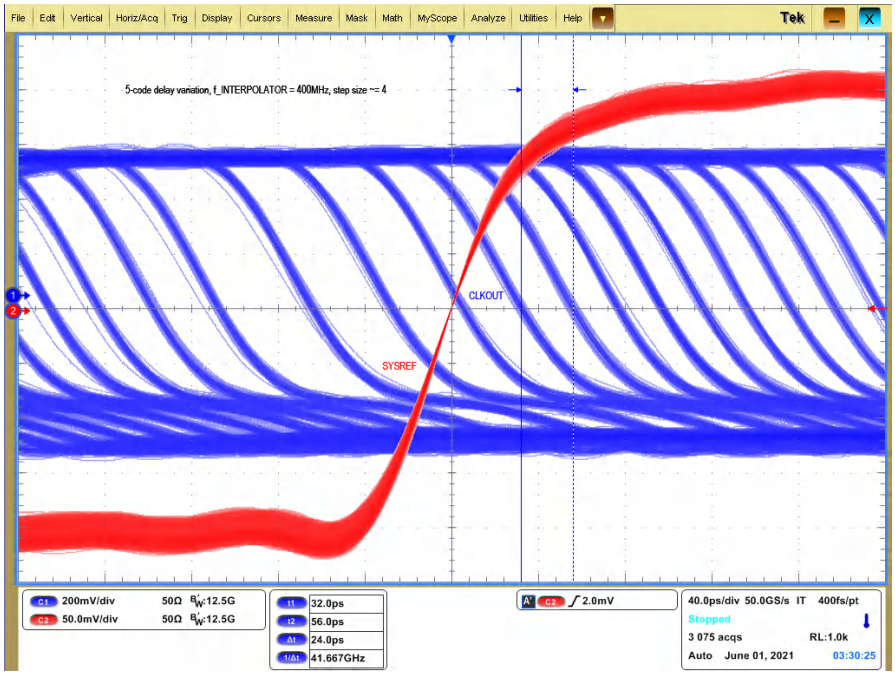



**Figure 3-7. SYSREF Delay, in 5-Code Steps**

# 4 Schematic

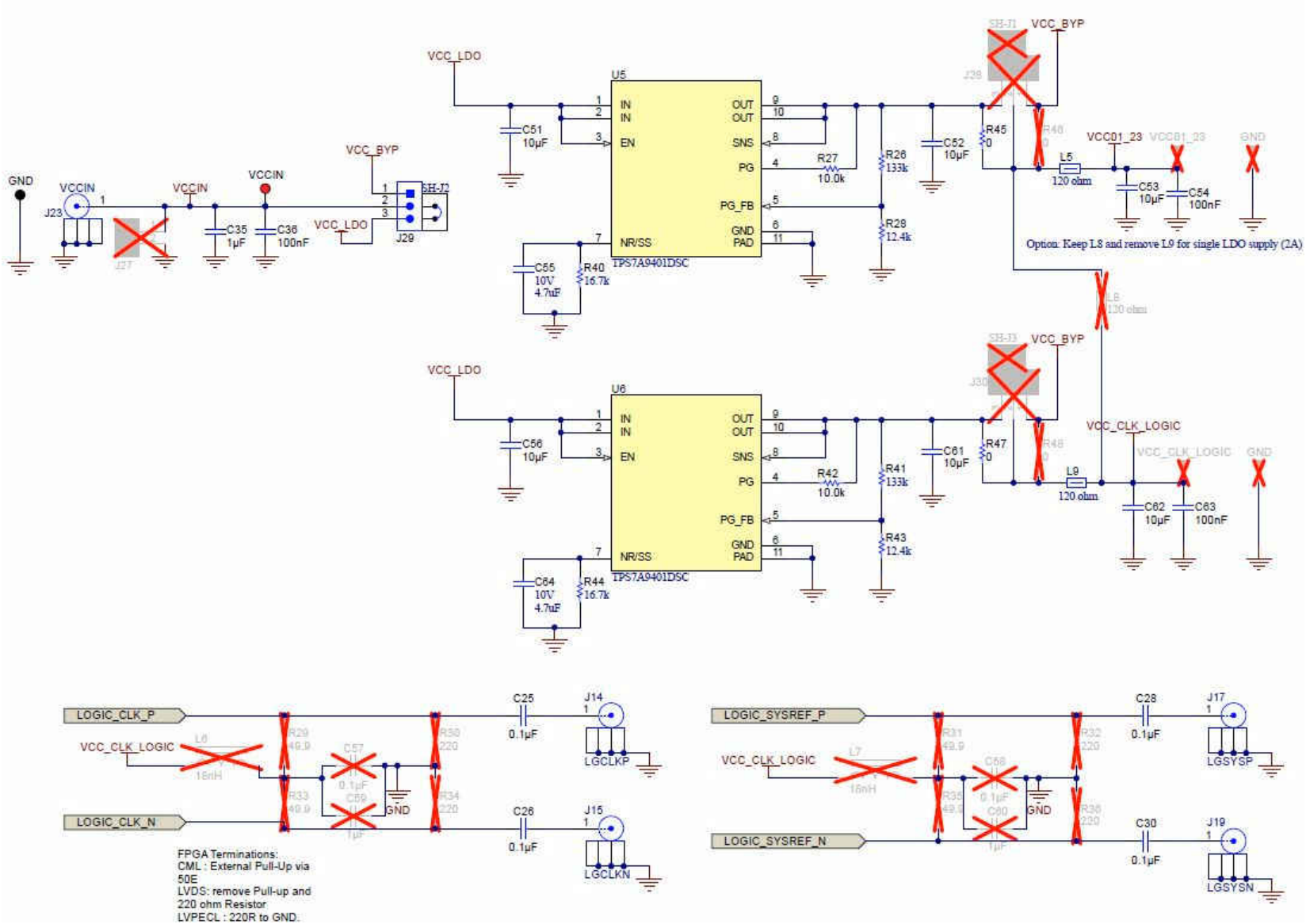



**Figure 4-1. Schematic - Power Supply**

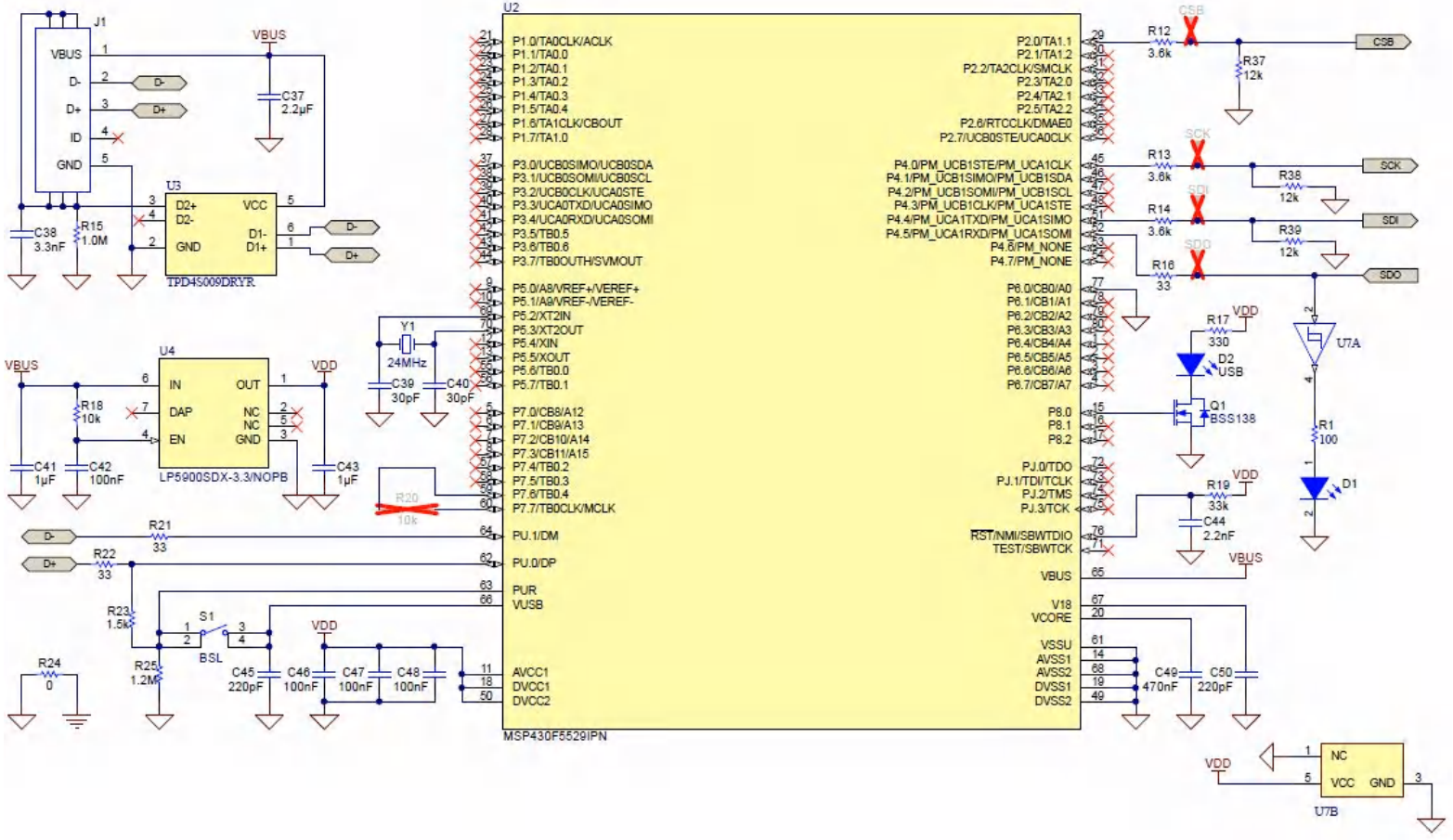



**Figure 4-2. Schematic - LMX1204**

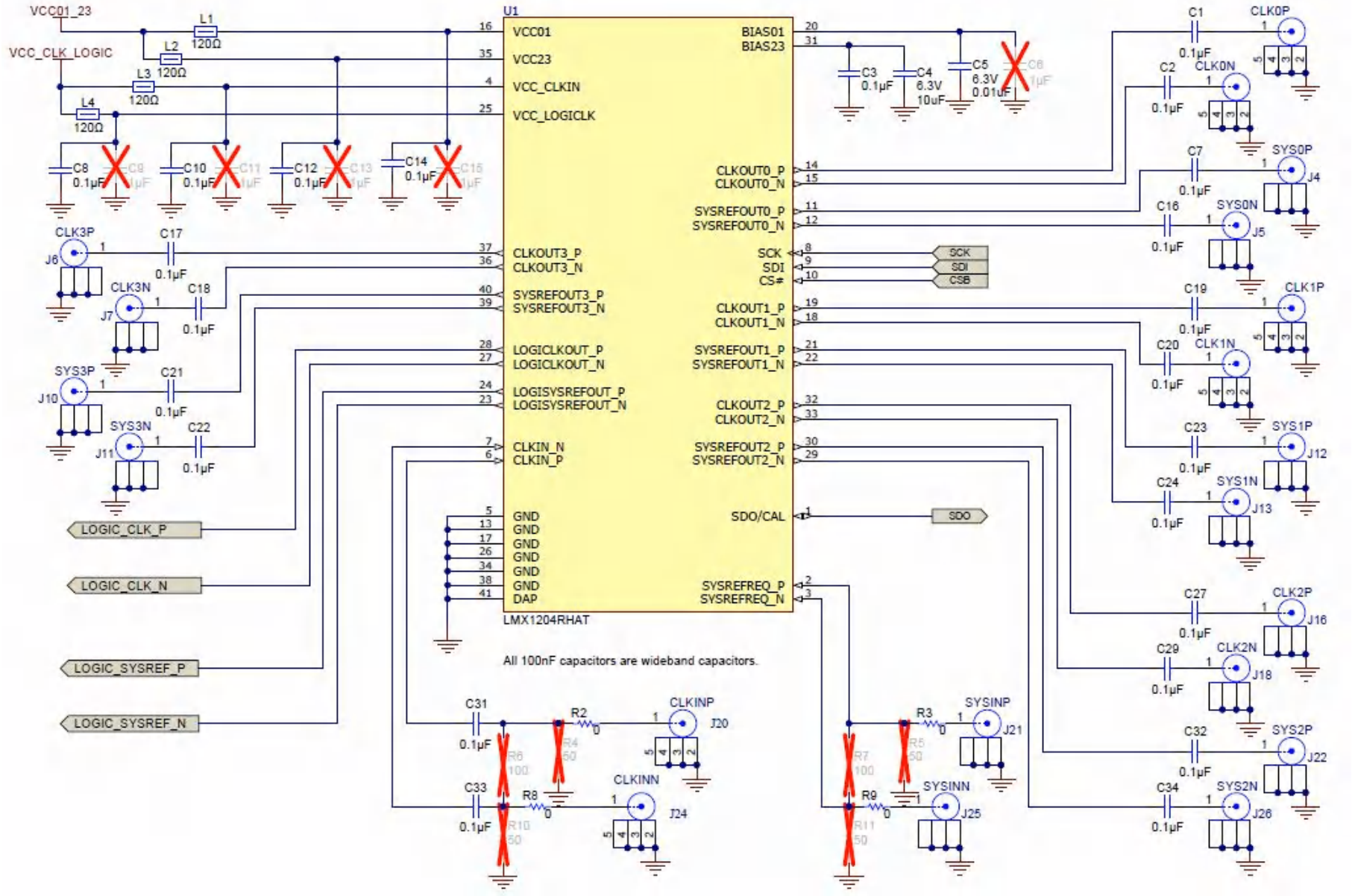



**Figure 4-3. Schematic - USB2ANY**

# 5 PCB Layout and Layer Stack-Up

## 5.1 PCB Layer Stack-Up

The top layer is 1-oz. copper.

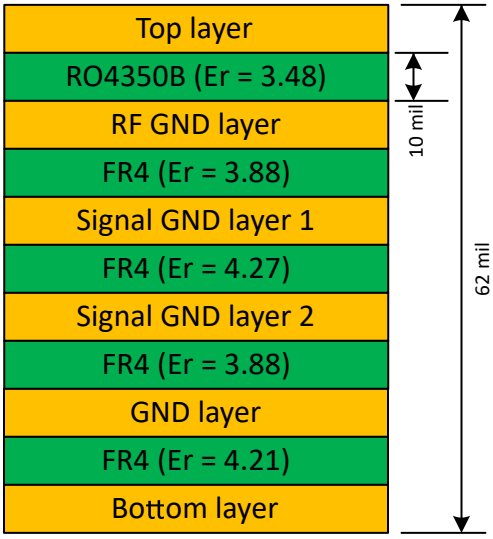



**Figure 5-1. PCB Layer Stack-Up**

## 5.2 PCB Layout

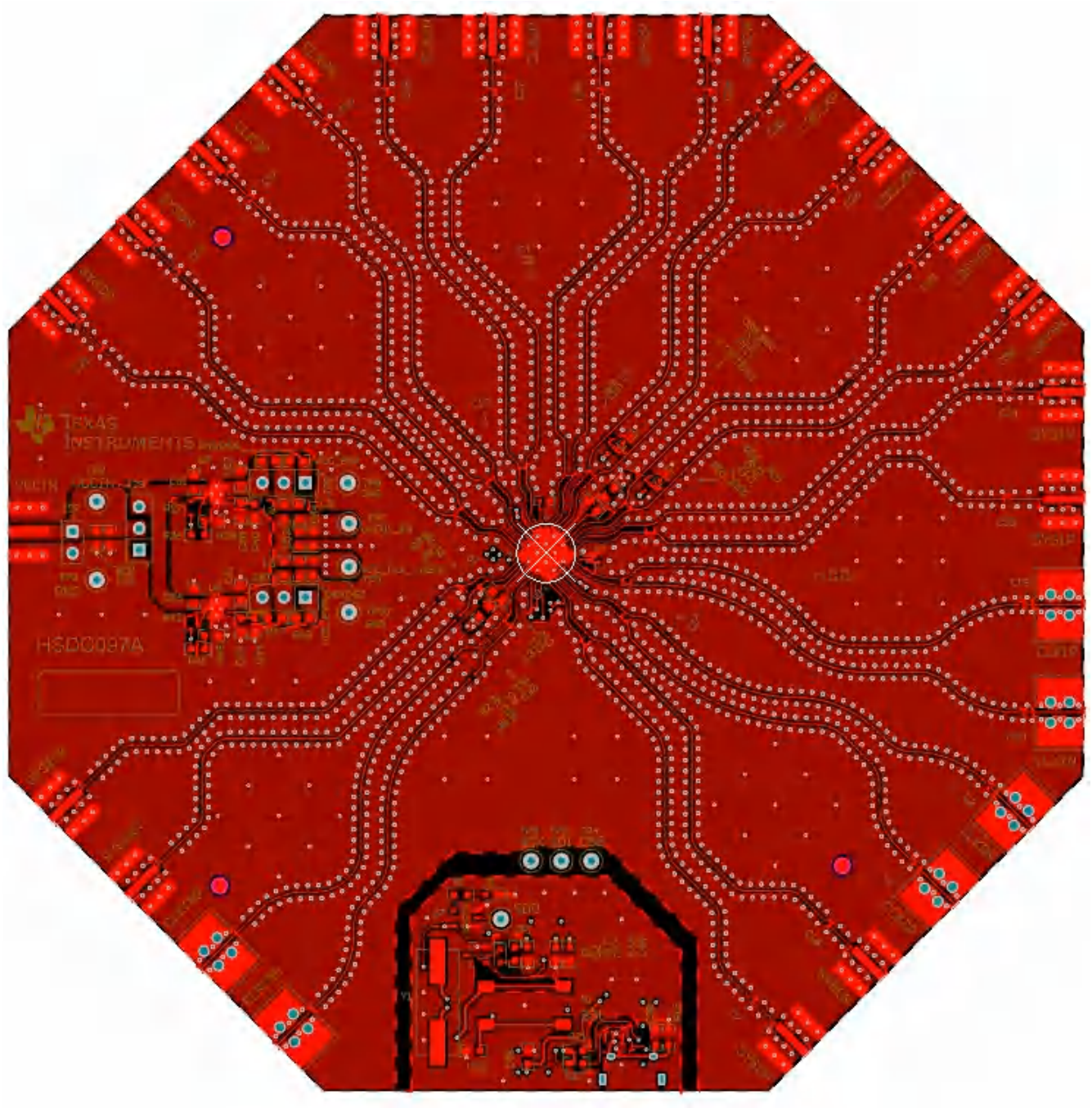



**Figure 5-2. PCB Layer Plot - Top Layer**

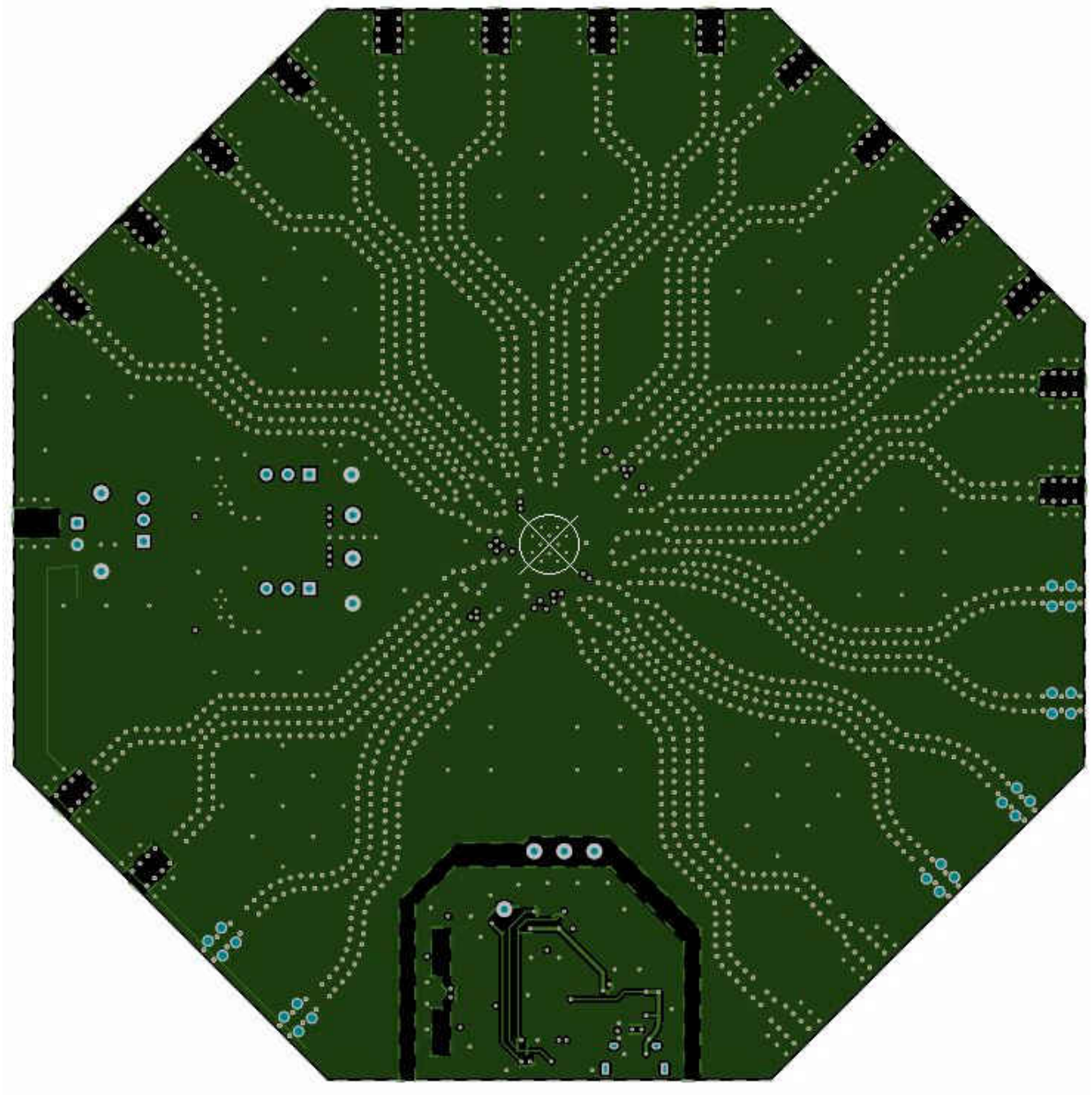


**Figure 5-3. PCB Layer Plot - Layer 2 (RF GND)**

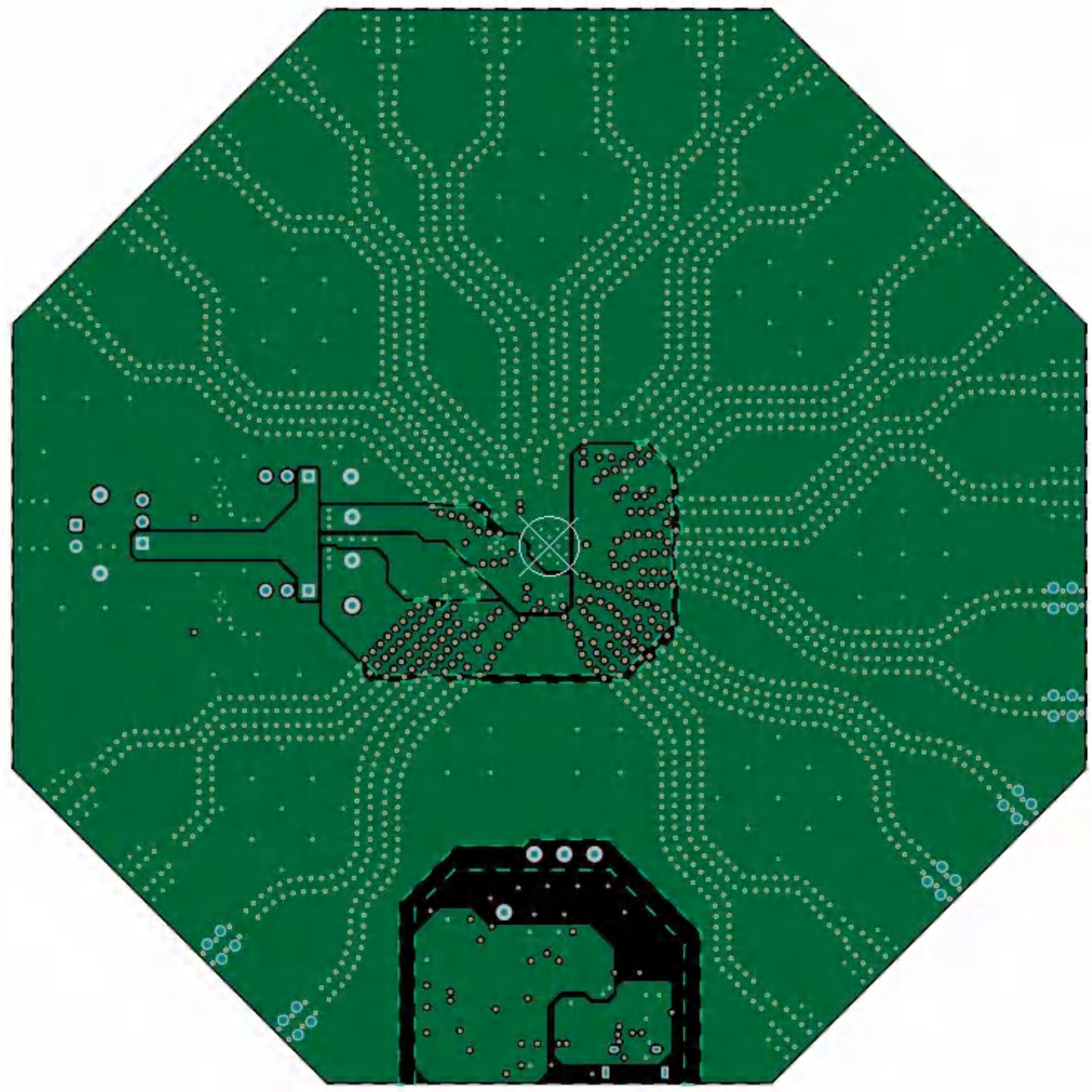


**Figure 5-4. PCB Layer Plot - Layer 3 (Signal GND 1)**

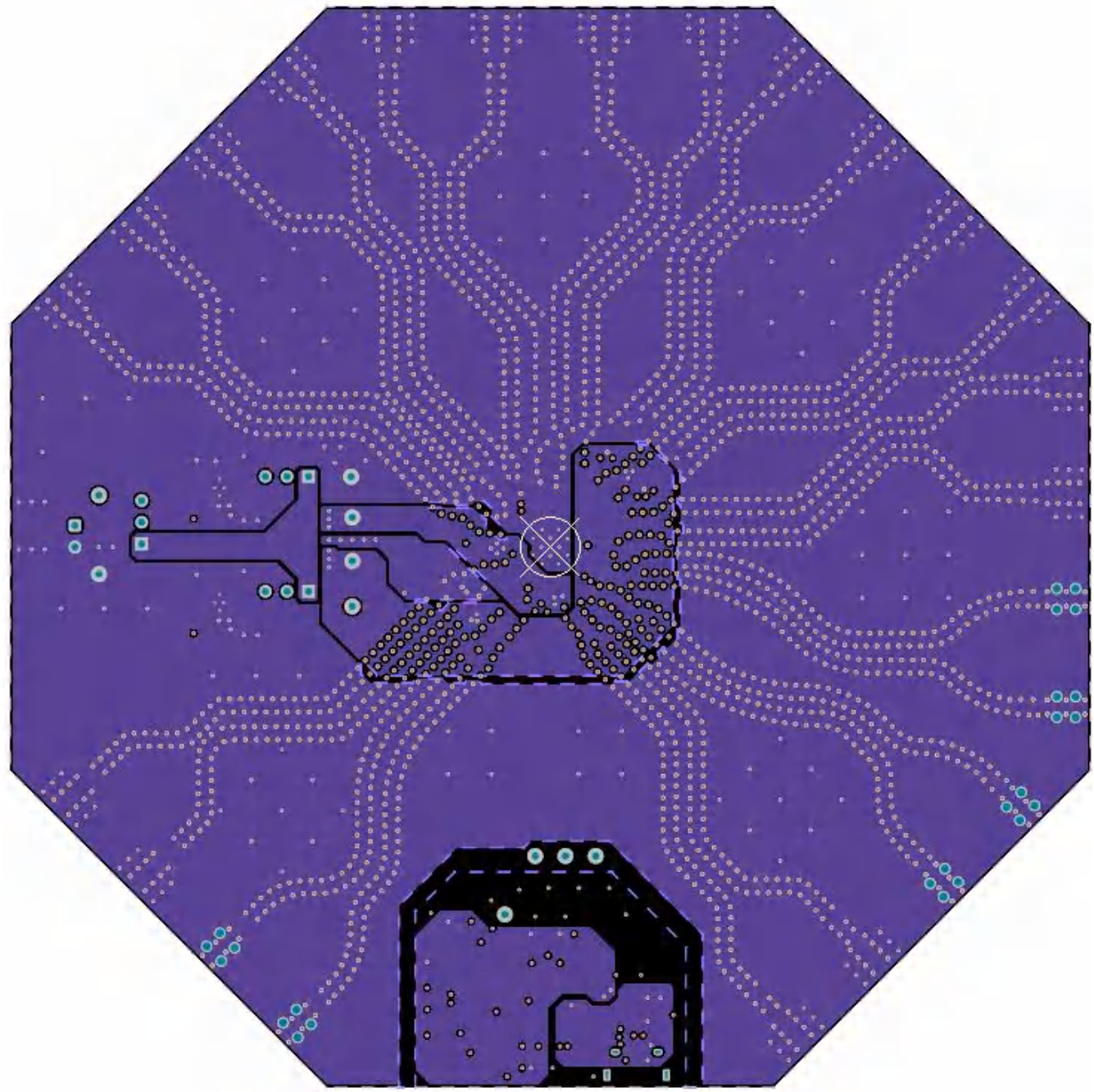


**Figure 5-5. PCB Layer Plot - Layer 4 (Signal GND 2)**

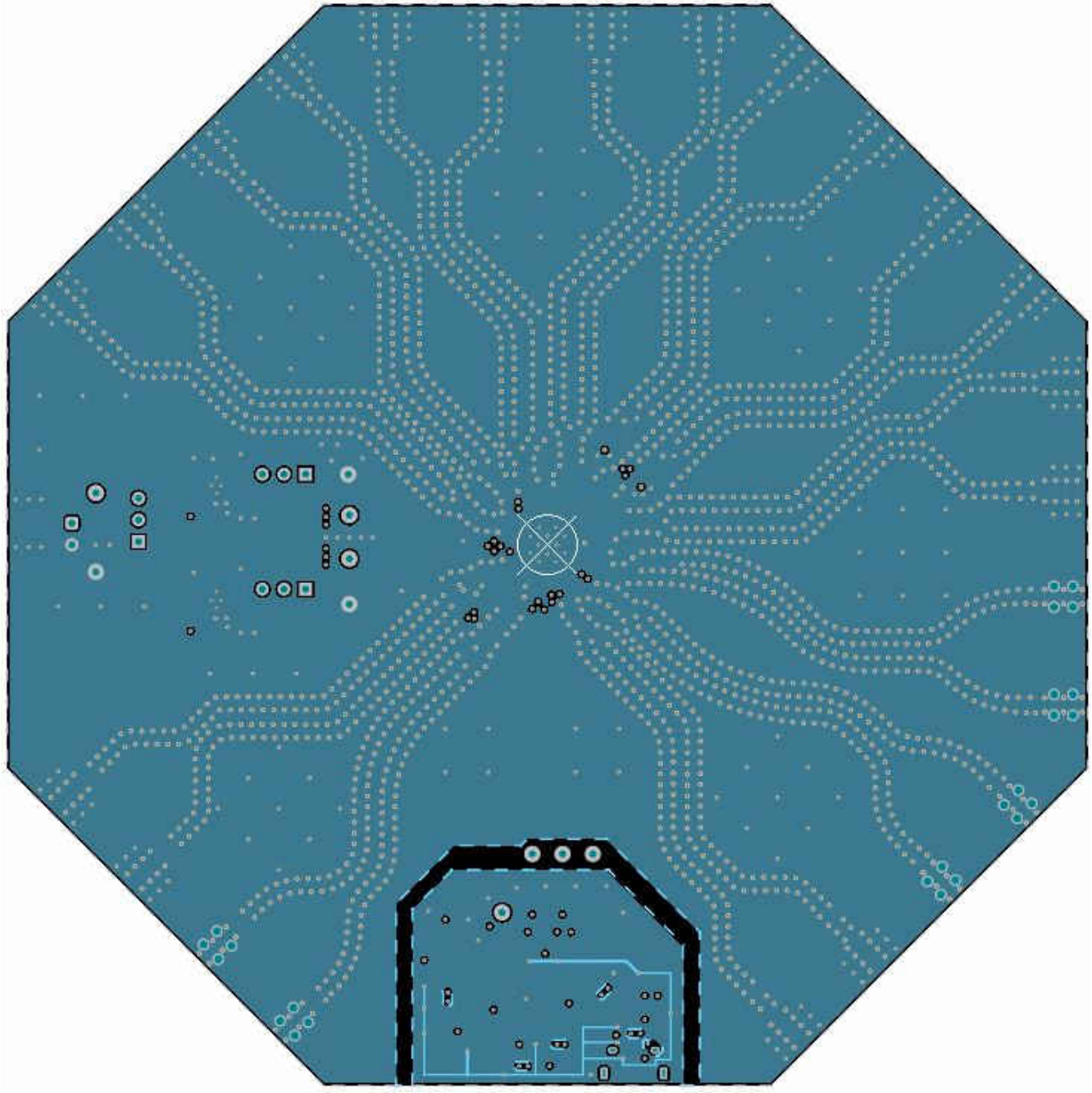


**Figure 5-6. PCB Layer Plot - Layer 5 (GND)**

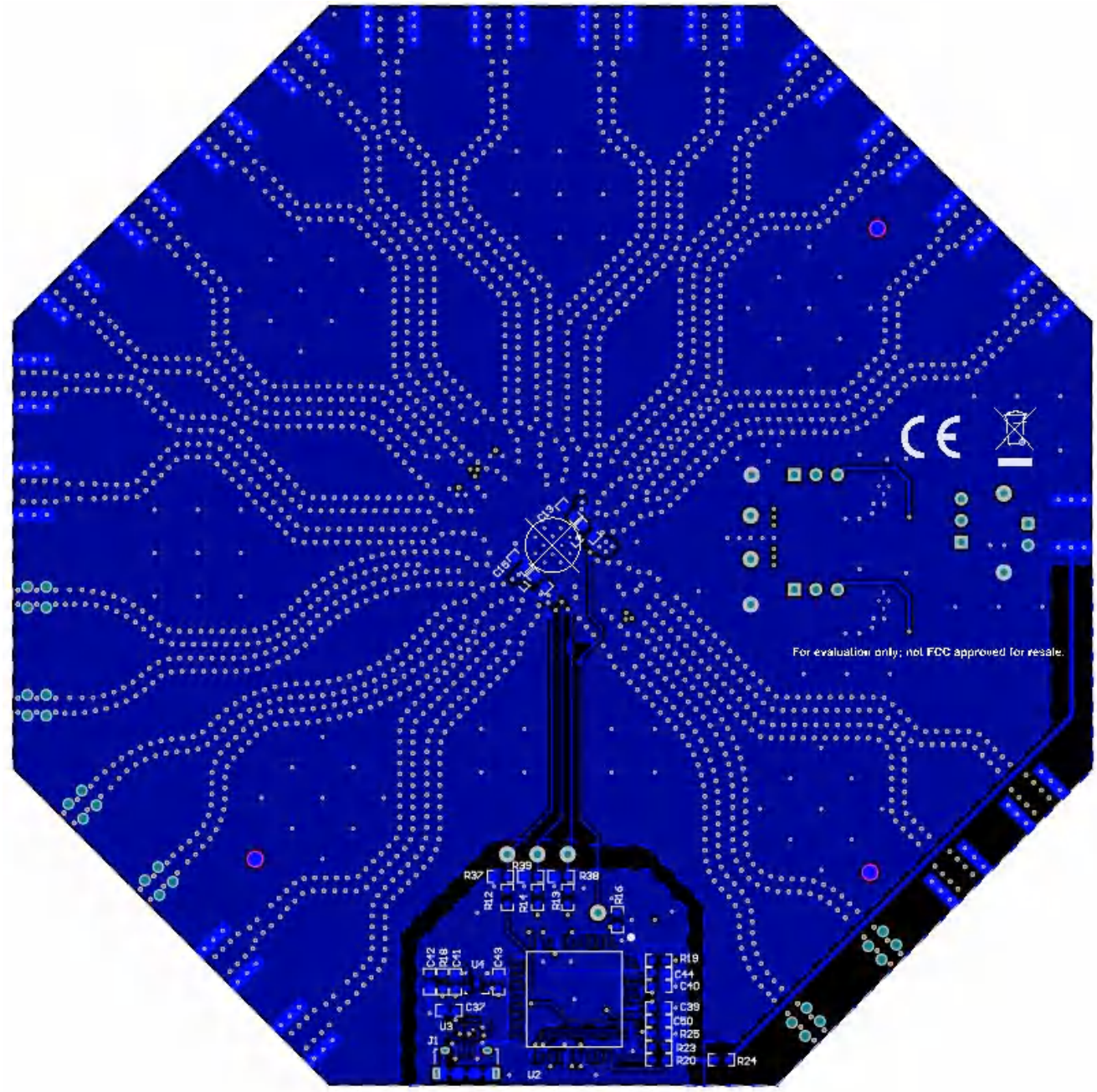



**Figure 5-7. PCB Layer Plot - Bottom Layer**

# 6 Bill of Materials

**Table 6-1. Bill of Materials (BOM)**

| DESIGNATOR | DESCRIPTION | PARTNUMBER | PACKAGEREFERENCE | MANUFACTURER |
|---|---|---|---|---|
| C1, C2, C3, C7, C8, C10, C12, C14, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34 | CAP, CERM, 0.1 µF, 10 V,+/- 10%, X5R, 0201 | 530Z104KT10T | 0201 | American Technical Ceramics |
| C4 | CAP, CERM, 10 uF, 6.3 V, +/- 20%, X5R, 0402 | GRM155R60J106ME15D | 0402 | MuRata |
| C5 | CAP, CERM, 0.01 uF, 6.3 V, +100/-0%, C0G/NP0, 0201 | 550Z103PTT | 0201 | AT Ceramics |
| C35, C41, C43 | CAP, CERM, 1 uF, 16 V, +/- 10%, X7R, 0603 | 885012206052 | 0603 | Wurth Elektronik |
| C36, C42, C46, C47, C48, C54, C63 | CAP, CERM, 0.1 uF, 16 V, +/- 10%, X7R, 0603 | 885012206046 | 0603 | Wurth Elektronik |
| C37 | CAP, CERM, 2.2 uF, 16 V, +/- 20%, X5R, 0603 | 885012106018 | 0603 | Wurth Elektronik |
| C38 | CAP, CERM, 3300 pF, 50 V,+/- 10%, X7R, 0603 | 885012206086 | 0603 | Wurth Elektronik |
| C39, C40 | CAP, CERM, 30 pF, 50 V, +/- 5%, C0G/NP0, 0603 | 06035A300JAT2A | 0603 | AVX |
| C44 | CAP, CERM, 2200 pF, 16 V, +/- 10%, X7R, 0603 | 885012206036 | 0603 | Wurth Elektronik |
| C45, C50 | CAP, CERM, 220 pF, 50 V, +/- 5%, C0G/NP0, 0603 | 06035A221JAT2A | 0603 | AVX |
| C49 | CAP, CERM, 0.47 uF, 16 V, +/- 10%, X7R, 0603 | C0603C474K4RACTU | 0603 | Kemet |
| C51, C52, C53, C56, C61, C62 | CAP, CERM, 10 µF, 10 V,+/- 10%, X5R, 0603 | GRM188R61A106KAALD | 0603 | MuRata |
| C55, C64 | CAP, CERM, 4.7 uF, 10 V, +/- 10%, X5R, 0603 | C0603C475K8PACTU | 0603 | Kemet |
| D1, D2 | LED, Green, SMD | LTST-C190GKT | 1.6x0.8x0.8mm | Lite-On |
| J1 | Receptacle, USB 2.0, Micro-USB Type B, R/A, SMT | 10118194-0001LF | USB-micro B USB 2.0, 0.65mm, 5 Pos, R/A, SMT | FCI |
| J2, J3, J8, J9, J20, J24 | Connector, End launch SMA 50 ohm, TH | 142-0761-881 | Connector, TH, End launch SMA | Cinch Connectivity |
| J4, J5, J6, J7, J10, J11, J12, J13, J14, J15, J16, J17, J18, J19, J21, J22, J23, J25, J26 | CONN SMA JACK STR EDGE MNT | CON-SMA-EDGE-S | CONN_JACK | RF Solutions Ltd. |
| J29 | Header, 100mil, 3x1, Gold, TH | TSW-103-07-G-S | 3x1 Header | Samtec |
| L1, L2, L3, L4 | Ferrite Bead, 120 ohm @ 100 MHz, 3 A, 0603 | BLM18SG121TN1D | 0603 | MuRata |
| L5, L9 | Ferrite Bead, 120 ohm @ 100 MHz, 2 A, 0603 | 742792625 | 0603 | Wurth Elektronik |

**Table 6-1. Bill of Materials (BOM) (continued)**

| DESIGNATOR | DESCRIPTION | PARTNUMBER | PACKAGEREFERENCE | MANUFACTURER |
|---|---|---|---|---|
| LBL1 | Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll | THT-14-423-10 | PCB Label 0.650 x 0.200 inch | Brady |
| Q1 | MOSFET, N-CH, 50 V, 0.22 A, SOT-23 | BSS138 | SOT-23 | Fairchild Semiconductor |
| R1 | RES, 100, 1%, 0.1 W, 0603 | CRCW0603100RFKEA | 0603 | Vishay-Dale |
| R2, R3, R8, R9 | RES, 0, 5%, 0.063 W, 0402 | RC0402JR-070RL | 0402 | Yageo America |
| R12, R13, R14 | RES, 3.6 k, 5%, 0.1 W, 0603 | RC0603JR-073K6L | 0603 | Yageo |
| R15 | RES, 1.0 M, 5%, 0.1 W, AEC-Q200 Grade 0, 0603 | CRCW06031M00JNEA | 0603 | Vishay-Dale |
| R16, R21, R22 | RES, 33, 5%, 0.1 W, AEC-Q200 Grade 0, 0603 | CRCW060333R0JNEA | 0603 | Vishay-Dale |
| R17 | RES, 330, 5%, 0.1 W, AEC-Q200 Grade 0, 0603 | CRCW0603330RJNEA | 0603 | Vishay-Dale |
| R18 | RES, 10 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603 | CRCW060310K0JNEA | 0603 | Vishay-Dale |
| R19 | RES, 33 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603 | CRCW060333K0JNEA | 0603 | Vishay-Dale |
| R23 | RES, 1.5 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603 | CRCW06031K50JNEA | 0603 | Vishay-Dale |
| R24, R45, R47 | RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603 | CRCW06030000Z0EA | 0603 | Vishay-Dale |
| R25 | RES, 1.2 M, 5%, 0.1 W, AEC-Q200 Grade 0, 0603 | CRCW06031M20JNEA | 0603 | Vishay-Dale |
| R26, R41 | RES, 133 k, 1%, 0.1 W, 0603 | RC0603FR-07133KL | 0603 | Yageo |
| R27, R42 | RES, 10.0 k, 1%, 0.1 W, 0603 | ERJ-3EKF1002V | 0603 | Panasonic |
| R28, R43 | RES, 12.4 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603 | ERJ-3EKF1242V | 0603 | Panasonic |
| R37, R38, R39 | RES, 12 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603 | CRCW060312K0JNEA | 0603 | Vishay-Dale |
| R40, R44 | RES, 16.7 k, 0.5%, 0.1 W, 0603 | RT0603DRE0716K7L | 0603 | Yageo America |
| S1 | Switch, Tactile, SPST-NO, 0.05A, 12V, SMT | FSM4JSMA | SW, SPST 6x6 mm | TE Connectivity |
| SH-J2 | Mini Shunt, Closed Top, 650 V AC, -45 to 85 degC, Pitch 1.27 mm, Height 3 mm, RoHS | NPB02SVAN-RC | Mini Shunt, Body 2.5x1.27mm, Height 3mm | Sullins Connector Solutions |
| TP2 | Test Point, Miniature, Red, TH | 5000 | Red Miniature Testpoint | Keystone |
| TP3 | Test Point, Miniature, Black, TH | 5001 | Black Miniature Testpoint | Keystone |
| U1 | High Frequency SYSREF Buffer/Multiplier/Divider | LMX1204RHAT | VQFN40 | Texas Instruments |

**Table 6-1. Bill of Materials (BOM) (continued)**

| DESIGNATOR | DESCRIPTION | PARTNUMBER | PACKAGEREFERENCE | MANUFACTURER |
|---|---|---|---|---|
| U2 | 25 MHz Mixed Signal Microcontroller with 128 KB Flash, 8192 B SRAM and 63 GPIOs, -40 to 85 degC, 80-pin QFP (PN), Green (RoHS & no Sb/Br) | MSP430F5529IPN | PN0080A | Texas Instruments |
| U3 | 4-Channel ESD Solution for High-Speed Differential Interface, DRY0006A (USON-6) | TPD4S009DRYR | DRY0006A | Texas Instruments |
| U4 | Ultra Low Noise, 150mA Linear Regulator for RF/ Analog Circuits Requires No Bypass Capacitor, 6-pin LLP, Pb-Free | LP5900SDX-3.3/NOPB | NGF0006A | Texas Instruments |
| U5, U6 | Ultra-Low Noise, Ultra-High PSRR, RF Voltage Regulator, DSC0010J (WSON-10) | TPS7A9401DSC | DSC0010J | Texas Instruments |
| U7 | Single Schmitt-Trigger Buffer, DBV0005A, LARGE T&R | DBV0005A | DBV0005A | Texas Instruments |
| Y1 | Crystal, 24.000 MHz, 20pF, SMD | ECS-240-20-5PX-TR | Crystal, 11.4x4.3x3.8mm | ECS Inc. |

# A Troubleshooting

### General Guidance

- Do not make modifications to the EVM or change the default settings until AFTER it is verified to be working.
- Register readback requires programming MUXOUT_EN = 1 and MUXOUT_SEL = 1. The GUI will also prompt to configure this register before attempting any readback operation.
- The POR current of the LMX1204EVM is between 400 mA and 500 mA with the CLKIN source disabled, and 620 mA with the CLKIN source enabled and oscillating.
- The power-down current of the EVM is approximately 50 mA, which is considering about 40mA ground current of the LDO.

### If Output Not Seen on CLKOUT

CLKOUT should oscillate after POR when CLKIN is powered and enabled. No EVM programming is required just to get output from CLKOUT.

- Confirm the EVM is connected to 3.3 V, and draws approximately 400 mA to 500 mA before CLKIN is applied.
- Confirm the reference input is connected to CLKIN and the reference source is powered and enabled.
- Confirm reference frequency is at least 300 MHz, and input power is at least 0 dBm.
- Confirm enabling CLKIN increases the EVM current to approximately 620 mA.

### If Device Features Not Active

The POR defaults for LMX1204 disable the LOGICLK, SYSREF, and other features. Only buffer mode is active by default. Register settings must be updated to observe these features.

- Confirm the USB cable is connected to the EVM.
- Confirm the connection mode is SPI and the USB2ANY interface is indicated in green on the bottom bar.
- If multiple USB2ANY boards are connected, confirm the correct USB2ANY is connected from *USB Communications* → *Interface* pop-up using the identify button.
- Ensure all registers have been loaded (Ctrl+L), and that the device current has changed proportional to the number of functional blocks enabled in the device.
- If a communication issue with the device is suspected, try toggling the POWERDOWN bit from the *User Controls* page and observe the EVM current. Note that the first write to R0 after POR will be ignored. If the EVM current does not drop to about 50 mA after POWERDOWN is set, a communication issue may be preventing programming, or the IC may be damaged.

### If Multiplier Frequency Not Accurate

The multiplier requires several registers to be programmed, and a calibration must be triggered by R0 write whenever the frequency changes or when the multiplier is first selected.

- Confirm the frequency input and output range for the device is appropriate. The GUI will indicate if frequencies are out of range by highlighting the input or output box with the range violation.
- Ensure that all registers have been loaded (Ctrl+L). This should also calibrate the multiplier.
- Try toggling the RESET bit on the *User Controls* page before loading all registers again (Ctrl+L).

### If Divider Frequency Not Accurate

The main clock output divider is designed with the expectation that the register settings will be loaded only once after POR. In some cases, the main clock output divider does not always cleanly transition between divide values if the value is changed after POR. To change the divider value, toggle the RESET bit on the *User Controls* page and load all registers again (Ctrl+L).

### If SYSREF Not Observed

There are several settings which must be correct to achieve SYSREF outputs.

- Ensure the following settings:
  - Set SYSREF_MODE to Continuous (for debugging)
  - SRREQ_MODE field set to SYSREFREQ mode
  - SRREQ_VCM set for DC-coupled, with about 1.1 V on SYSREFREQ_N and 1.5 V on SYSREFREQ_P
  - SYSREF_DLY_BYP field set to use delay
  - SYSREF_EN=1
- Ensure the frequencies of the SYSREF_DLY_DIV, SYSREF_DIV_PRE, and SYSREF_DLY_ADJ are correctly configured. The GUI will highlight any frequency violations.
- Ensure that $F_{INTERPOLATOR}$ % $F_{SYSREF}$ = 0. The GUI will highlight the SYSREF divider in case of violations.
- Ensure that the output channel (CHx_EN/LOGIC_EN) and the SYSREF buffer (SYSOUTx_EN/LOGISYS_EN) are enabled.
- Confirm that Windowing mode is not enabled on the *User Controls* page (SYSWND_EN=0).
- Confirm that R15[9]=1. This should be set automatically by the GUI, so this potential root cause should be rare.
- Confirm the 1.1-V and 1.5-V source for SYSREFREQ_N and SYSREFREQ_P respectively are actually resulting in the required voltages at the pins. If power supplies are used for these voltages, it is not uncommon for the supplies to be unable to sink current; the 1.1-V source may not be able to sink current from the 1.5-V supply through the internal 100-Ω impedance. An arbitrary function generator is recommended if possible.

# B USB2ANY Firmware Upgrade

When the onboard USB2ANY programmer is first connected, or if the firmware revision used for the onboard USB2ANY programmer does not match the version used by TICS Pro (2.7.0.0), TICS Pro will request a firmware update. Follow the pop-up instructions to complete the update.

1. When the *USB2ANY Firmware Requirement* pop-up window appears, click *OK* to continue.

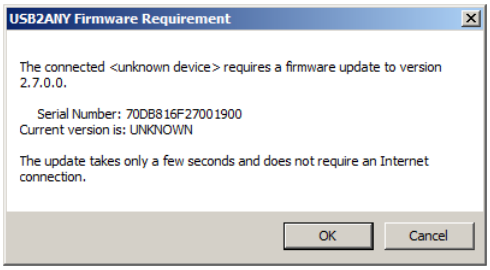



**Figure B-1. Firmware Requirement**

2. The Figure B-2 pop-up window will load. Disconnect the USB cable from the EVM.

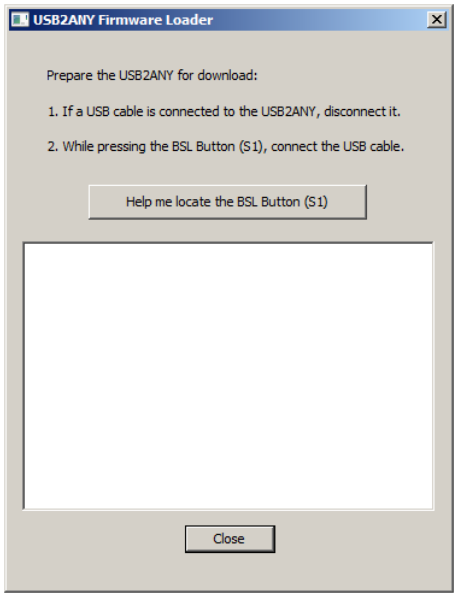



**Figure B-2. Firmware Loader**

3. While pressing the BSL button (shown below), connect the USB2ANY cable.

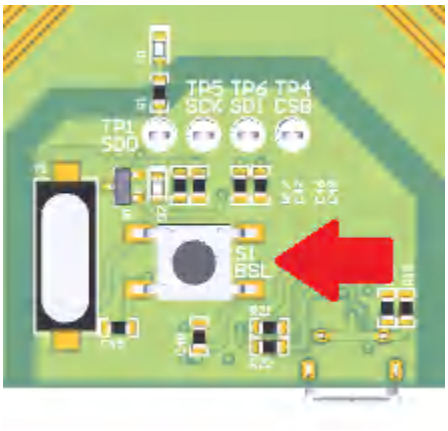



**Figure B-3. BSL Button Location**

4. The firmware loader should recognize the USB2ANY as a target for programming, and an Figure B-4 button should appear.

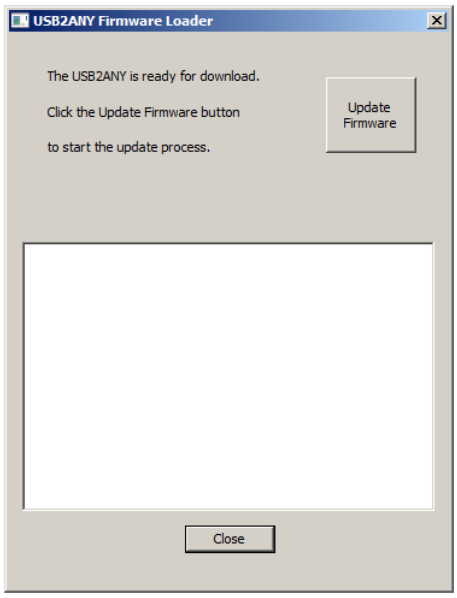



**Figure B-4. Update Firmware**

5. Click *Upgrade Firmware* to start the firmware upgrade. Click *Close* after the upgrade is complete.

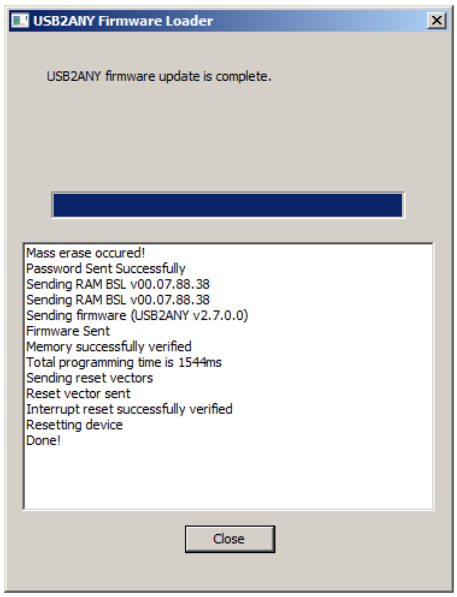



**Figure B-5. Firmware Update Complete**

6. Go to *USB communications* → *Interface* in the TICS Pro software to check the USB connection. Make sure the *USB Connected* button is green.

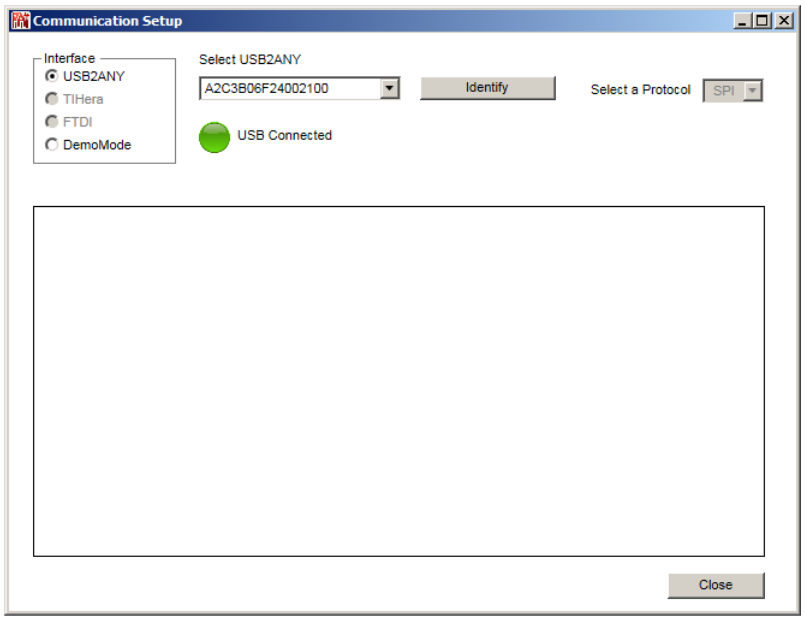



**Figure B-6. USB Communications**

## C Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision * (July 2021) to Revision A (August 2022) | Page |
|---|---|
| • Changed board image | 1 |
| • Changed the supply voltage from 2.5 V to 3.3 V | 3 |
| • Updated the power supply section and operating frequencies | 4 |
| • Updated the connection diagram with latest board image | 4 |
| • Changed phase noise plots for 6000-MHz and 3000-MHz operating frequencies | 7 |
| • Updated schematic | 13 |
| • Updated PCB layer stack up and layout | 16 |
| • Updated PCB layout | 17 |
| • Updated the *Bill of Materials (BOM)* table | 23 |

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NOTE:

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3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

**CAUTION**

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

**FCC Interference Statement for Class A EVM devices**

*NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.*

**FCC Interference Statement for Class B EVM devices**

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

**Concerning EVMs Including Radio Transmitters:**

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

**Concernant les EVMs avec appareils radio:**

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

**Concerning EVMs Including Detachable Antennas:**

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

**Concernant les EVMs avec antennes détachables**

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

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1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

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