RF430CL331H NFC Type 4B Dynamic Dual Interface Transponder

1 Device Overview

1.1 Features

- Pass-Through Operation Sends Data Updates and Requests to Host Controller
- I^2C Interface Allows Writing and Reading of Internal SRAM
- Prefetching, Caching, and Auto ACK Features Increase Data Throughput
- Enables Data Streaming
- All RF Communication up to Layer 4 Handled Automatically
- Supports up to Maximum NDEF Message Size
- Compliant With ISO/IEC 14443B
- Supports up to 848 kbps

1.2 Applications

- Wireless Firmware Updates
- Wi-Fi® and *Bluetooth*® Pairing
- Service Interface
- Wireless Sensor Interfaces

1.3 Description

The TI Dynamic NFC/RFID Interface Transponder RF430CL331H is an NFC Tag Type 4 device that combines a contactless NFC/RFID interface and a wired I^2C interface to connect the device to a host. The NDEF message can be written and read from the integrated I^2C serial communication interface and can also be accessed and updated over a contactless interface using the integrated ISO/IEC 14443 Type B compliant RF interface that supports up to 848 kbps.

The device requests responses to NFC Type 4 commands on demand from the host controller and stores only a portion of the NDEF message in its buffer at any one time. This allows NDEF message size to be limited only by the memory capacity of the host controller and specification limitations.

Support of read caching, prefetching, and write automatic acknowledgment features allows for greater data throughput.

This device enables NFC connection handover for an alternative carrier like *Bluetooth*®, *Bluetooth*® low energy (BLE), or Wi-Fi as an easy and intuitive pairing process or authentication process with only a tap.

As a general NFC interface, the RF430CL331H enables end equipment to communicate with the fast-growing infrastructure of NFC-enabled smart phones, tablets, and notebooks.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (2)
RF430CL331HIPW	TSSOP (14)	5 mm × 4.4 mm
RF430CL331HRGT	VQFN (16)	3 mm × 3 mm

(1) For the most current part, package, and ordering information for all available devices, see the *Package Option Addendum* in Section 8, or see the TI website at www.ti.com.
(2) The sizes shown here are approximations. For the package dimensions with tolerances, see the *Mechanical Data* in Section 8.

1.4 Typical Application

Figure 1-1 shows a typical application.

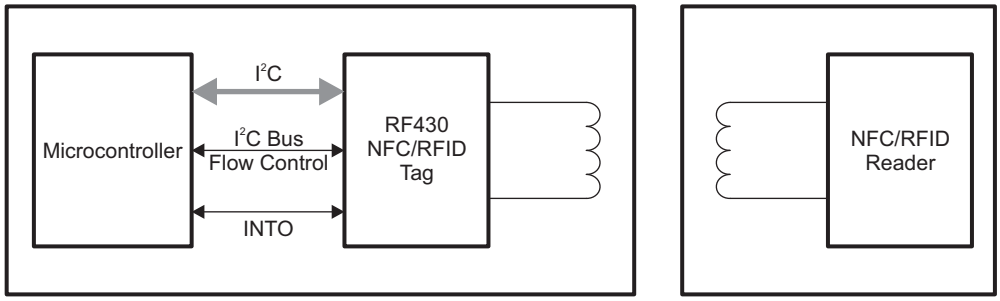


Figure 1-1. Typical Application

Table of Contents

2 Revision History

Changes from September 29, 2015 to November 30, 2015 **Page**

- Deleted "Suggested to be set to 0x3B" from Step 7(a) 34
- Deleted "The recommended setting is maximum possible value, which is 0x3B" in the paragraph that starts "When the internal state machine determines..." 46

3 Terminal Configuration and Functions

3.1 Pin Diagrams

Figure 3-1 shows the pinout for the 14-pin PW package.

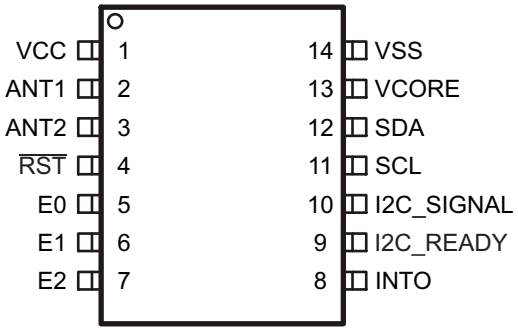


Figure 3-1. 14-Pin PW Package (Top View)

Figure 3-2 shows the pinout for the 16-pin RGT package.

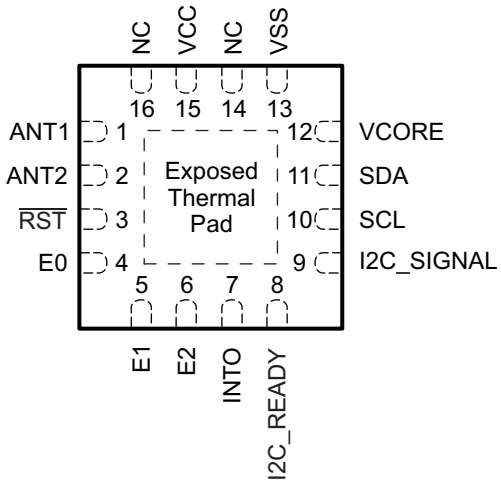


Figure 3-2. 16-Pin RGT Package (Top View)

3.2 Pin Attributes

Table 3-1. Pin Attributes

PIN NUMBER		SIGNAL NAME	SIGNAL TYPE (1)	BUFFER TYPE (2)	POWER SOURCE	RESET STATE (3)
PW	RGT					
1	15	VCC	PWR	Power	VCC	N/A
2	1	ANT1	RF	Analog	–	N/A
3	2	ANT2	RF	Analog	–	N/A
4	3	$\overline{\text{RST}}$	I	LVCMOS	VCC	PU
5	4	E0	I	LVCMOS	VCC	OFF
6	5	E1	I	LVCMOS	VCC	OFF
7	6	E2	I	LVCMOS	VCC	OFF
8	7	INTO	O	LVCMOS	VCC	OFF
9	8	I2C_READY	O	LVCMOS	VCC	DRIVE1
10	9	I2C_SIGNAL	O	LVCMOS	VCC	DRIVE1
11	10	SCL	I/O	LVCMOS	VCC	OFF
12	11	SDA	I/O	LVCMOS	VCC	OFF
13	12	VCORE	PWR	Power	VCC	N/A
14	13	VSS	PWR	Power	VCC	N/A
–	14	NC	–	–	–	–
–	16	NC	–	–	–	–

(1) Signal Types: I = Input, O = Output, I/O = Input or Output, PWR = Power, RF = Radio frequency
(2) Buffer Types: See Table 3-3 for details.
(3) Reset States:
OFF = High-impedance input with pullup or pulldown disabled (if available)
PD = High-impedance input with pulldown enabled
PU = High-impedance input with pullup enabled
DRIVE0 = Drive output low
DRIVE1 = Drive output high
N/A = Not applicable

3.3 Signal Descriptions

Table 3-2 describes the signals.

Table 3-2. Signal Descriptions

FUNCTION	SIGNAL NAME	PIN NUMBER		I/O (1)	DESCRIPTION
		PW	RGT		
Power	VCC	1	15	PWR	3.3-V power supply
	VCORE	13	12	PWR	Regulated core supply voltage
	VSS	14	13	PWR	Ground supply
RF	ANT1	2	1	RF	Antenna input 1
	ANT2	3	2	RF	Antenna input 2
Serial communication	E0	5	4	I	I^2C address select 0
	E1	6	5	I	I^2C address select 1
	E2	7	6	I	I^2C address select 2
	I2C_READY	9	8	O	High indicates that I^2C communication can be started. Low indicates that I^2C communication must not be started.
	I2C_SIGNAL	10	9	O	Low indicates that a wait time extension command is automatically being sent. I^2C communication does not have to be stopped.
	SCL	11	10	I/O	I^2C clock
	SDA	12	11	I/O	I^2C data
System	INTO	8	7	O	Interrupt output
	$\overline{RST}$	4	3	I	Reset input (active low) (2)
No connect	NC	–	14 16	–	Leave open, no connection

(1) I = Input, O = Output, PWR = Power, RF = RF antenna
(2) With integrated pullup

3.4 Pin Multiplexing

None of the pins on this device are multiplexed.

Table 3-3. Buffer Type

BUFFER TYPE (STANDARD)	NOMINAL VOLTAGE	HYSTERESIS	PU OR PD	NOMINAL PU OR PD STRENGTH (µA)	OUTPUT DRIVE STRENGTH (mA)	OTHER CHARACTERISTICS
LVCMOS	3.3 V	Y	N/A	See Section 4.6, *Electrical Characteristics, Digital Inputs*	See Section 4.7, *Electrical Characteristics, Digital Outputs*	
Analog, RF	3.3 V	N	N/A	N/A	N/A	See analog modules in Section 4, *Specifications*, for details
Power	3.3 V	Y with SVS on	N/A	N/A	N/A	

3.5 Connections for Unused Pins

Leave no connect (NC) pins unconnected.

Leave unused outputs unconnected.

Drive or pull unused inputs high or low.

4 Specifications

4.1 Absolute Maximum Ratings (1) (2)

	MIN	MAX	UNIT
Voltage applied at V_{CC} referenced to V_{SS} (V_{AMR})	–0.3	4.1	V
Voltage applied at V_{ANT} referenced to V_{SS} (V_{AMR})	–0.3	4.1	V
Voltage applied to any pin (references to V_{SS})	–0.3	V_{CC} + 0.3	V
Diode current at any device pin		±2	mA
Storage temperature, T_{stg} (3)	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are referenced to VSS.
(3) For soldering during board manufacturing, it is required to follow the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

4.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

Typical values are specified at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	During program execution no RF field present	3.0	3.3	3.6	V
		During program execution with RF field present	2.0	3.3	3.6	
V_{SS}	Supply voltage (GND reference)			0		V
T_A	Operating free-air temperature		–40		85	°C
C_1	Decoupling capacitor on V_{CC} (1)			0.1		µF
C_2	Decoupling capacitor on V_{CC} (1)			1		µF
C_{VCORE}	Capacitor on V_{CORE} (1)		0.1	0.47	1	µF

(1) Low ESR (equivalent series resistance) capacitor

4.4 Recommended Operating Conditions, Resonant Circuit

		MIN	NOM	MAX	UNIT
f_c	Carrier frequency		13.56		MHz
V_{ANT_peak}	Antenna input voltage			3.6	V
Z	Impedance of LC circuit	6.5		15.5	kΩ
L_{RES}	Coil inductance (1)		2.66		µH
C_{RES}	Total resonance capacitance (1), $C_{RES} = C_{IN} + C_{Tune}$		51.8		pF
C_{Tune}	External resonance capacitance		$C_{RES} – C_{IN}$ (2)		pF
QT	Tank quality factor		30		

(1) The coil inductance of the antenna L_{RES} with the external capacitance C_{Tune} plus the device internal capacitance C_{IN} is a resonant circuit. The resonant frequency of this LC circuit must be close to the carrier frequency f_c:
$f_{RES} = 1 / [2\pi(L_{RES}C_{RES})^{1/2}] = 1 / [2\pi(L_{RES}(C_{IN}+C_{Tune}))^{1/2}] \approx f_c$
(2) For C_{IN} refer to Section 4.9.3.

4.5 Supply Currents

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{CC(I2C)}$	I^2C, 400 kHz, Writing into NDEF memory		3.3 V		250		µA
$I_{CC(RF\ enabled)}$	RF enabled, no RF field present		3.3 V		40		µA
$I_{CC(Inactive)}$	Standby enable = 0, RF disabled, no serial communication		3.3 V		15		µA
$I_{CC(Standby)}$	Standby enable = 1, RF disabled, no serial communication		3.3 V		10	45	µA
$\Delta I_{CC(StrongRF)}$	Additional current consumption with strong RF field present		3.0 V to 3.6 V			160	µA
$I_{CC(RF,lowVCC)}$	Current drawn from VCC < 3.0 V with RF field present (passive operation)		2.0 V to 3.0 V			0	µA

4.6 Electrical Characteristics, Digital Inputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage					0.3 × V_{CC}	V
V_{IH}	High-level input voltage			0.7 × V_{CC}			V
V_{HYS}	Input hysteresis			0.1 × V_{CC}			V
I_L	High-impedance leakage current		3.3 V	–50		50	nA
$R_{PU(RST)}$	Integrated $\overline{RST}$ pullup resistor			20	35	50	kΩ

4.7 Electrical Characteristics, Digital Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OL}	Output low voltage	I_{OL} = 3 mA	3 V		0.4	V
			3.3 V		0.4	
			3.6 V		0.4	
V_{OH}	Output high voltage	I_{OH} = –3 mA	3 V	2.6		V
			3.3 V	2.9		
			3.6 V	3.2		

4.8 Thermal Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER			VALUE	UNIT
$R\theta_{JA}$	Junction-to-ambient thermal resistance, still air(1)	TSSOP-14 (PW)	116.0	°C/W
$R\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance(2)		45.1	°C/W
$R\theta_{JB}$	Junction-to-board thermal resistance(3)		57.6	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter		57.0	°C/W
Ψ_{JT}	Junction-to-top thermal characterization parameter		4.6	°C/W
$R\theta_{JA}$	Junction-to-ambient thermal resistance, still air(1)	VQFN-16 (RGT)	48.8	°C/W
$R\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance(2)		60.8	°C/W
$R\theta_{JC(BOT)}$	Junction-to-case (bottom) thermal resistance(4)		7.1	°C/W
$R\theta_{JB}$	Junction-to-board thermal resistance(3)		21.9	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter		21.9	°C/W
Ψ_{JT}	Junction-to-top thermal characterization parameter		1.5	°C/W

(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(4) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

4.9 Timing and Switching Characteristics

4.9.1 Reset Timing

Table 4-1. I²C Power-up Timing

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
t_{Ready}	Time after power up or reset until device is ready to communicate using I²C (1)		20	ms

(1) The device is ready to communicate after t_{Ready}(MAX) at the latest.

4.9.2 Serial Communication Protocol Timing

Table 4-2. I²C Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 4-1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{SCL}	SCL clock frequency (with Master supporting clock stretching according to I²C standard, or when the device is not being addressed)		3.3 V	0	400	kHz
	SCL clock frequency (device being addressed by Master not supporting clock stretching)	Write	3.3 V	0	120	
		Read	3.3 V	0	100	
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} ≤ 100 kHz	3.3 V	4		µs
		f_{SCL} > 100 kHz		0.6		
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} ≤ 100 kHz	3.3 V	4.7		µs
		f_{SCL} > 100 kHz		0.6		
$t_{HD,DAT}$	Data hold time		3.3 V	0		ns
$t_{SU,DAT}$	Data setup time		3.3 V	250		ns
$t_{SU,STO}$	Setup time for STOP		3.3 V	4		µs
t_{SP}	Pulse duration of spikes suppressed by input filter		3.3 V	6.25	75	ns

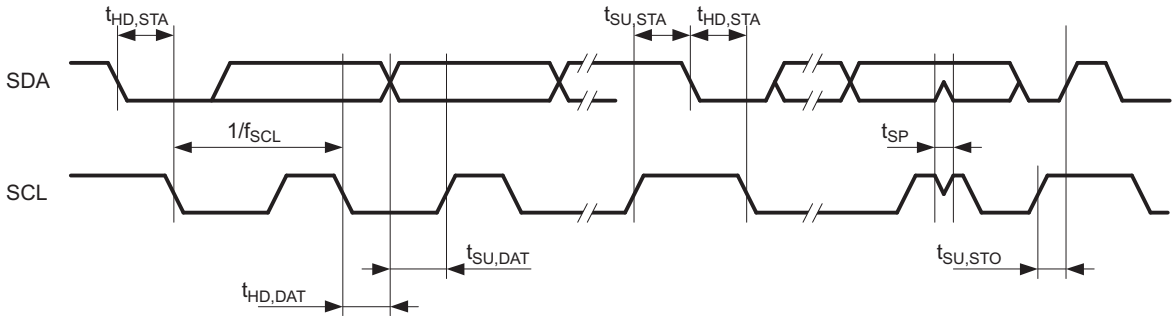


Figure 4-1. I²C Mode Timing

4.9.3 RF143B NFC/RFID Analog Front End

Table 4-3. Recommended Operating Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DDH}	Antenna rectified voltage	Peak voltage limited by antenna limiter	3.0	3.3	3.6	V
I_{DDH}	Antenna load current	RMS, without limiter current			100	µA
C_{IN}	Input capacitance	ANT1 to ANT2, 2 V RMS	31.5	35	38.5	pF

Table 4-4. ISO/IEC 14443B ASK Demodulator

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
DR_{10}	Input signal data rate 10% downlink modulation, 7% to 30% ASK, ISO1443B		106	848	kbps
m10	Modulation depth 10%, tested as defined in ISO/IEC 10373-6	7%		30%	

Table 4-5. ISO/IEC 14443B-Compliant Load Modulator

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
f_{PICC}	Uplink subcarrier modulation frequency	0.2		1	MHz
V_{A_MOD}	Modulated antenna voltage, V_{A_unmod} = 2.3 V	0.5			V
V_{SUB14}	Uplink modulation subcarrier level, ISO/IEC 14443B: H = 1.5 to 7.5 A/m	$22/H^{0.5}$			mV

Table 4-6. Power Supply

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{LIM}	Limiter clamping voltage	I_{LIM} ≤ 70 mA RMS, f = 13.56 MHz	3.0		3.6	V_{pk}
$I_{LIM,MAX}$	Maximum limiter current				70	mA

5 Detailed Description

5.1 Overview

Figure 5-1 shows the functional block diagram.

5.2 Functional Block Diagram

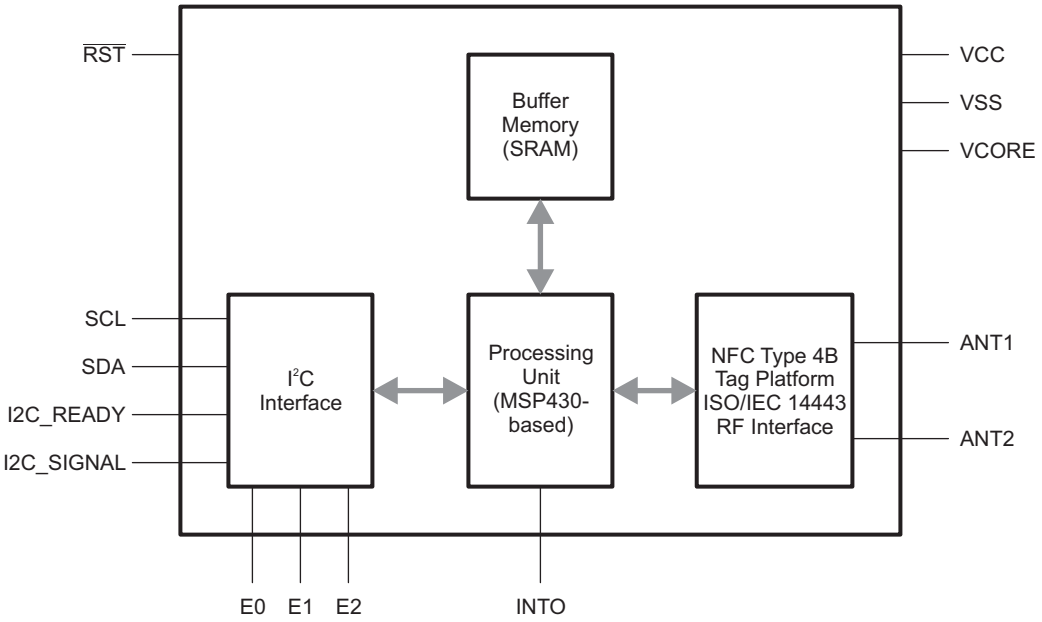


Figure 5-1. Functional Block Diagram

5.3 Terms and Acronyms

Table 5-1 describes the terms and acronyms used in this document.

Table 5-1. Term Definitions

NAME	DESCRIPTION
PCD	Proximity coupling device, such as NFC enabled handset, NFC/RFID reader/writer devices
PICC	Proximity integrated circuit card, dynamic tag, RF430CL331H IC
NFC Type 4 command	See the NFC Forum Type 4 Tag Operation Specification (http://nfc-forum.org/) for details
PICC Buffer	This is a memory range (0 through 2999) that is accessible through the I^2C bus, where buffer data is stored.
Host Controller	This is a MCU or processor connected to the PICC through the I^2C bus. It responds to all the of Type 4 data requests that come from the PICC.
SW	Type 4 command acknowledgments, referred also as SW1 and SW2 (status word). Refer to NFC/RFID and ISO14443-B specifications for details.
SWTX or S(WTX)	Frame wait time extension. When the RF430CL331H cannot respond to a command that PCD sends, it must send a S(WTX) request indicating that it needs more time. The PCD then responds and the RF430CL331H has the negotiated time that it requested.

5.4 Serial Communication Interface

The serial interface of this device is I^2C. The serial interface allows a connected MCU to configure the device and write to and read from the available registers and the RAM buffer on the RF430CL331H.

5.5 Communication Protocol

The tag is programmed and controlled by writing data into and reading data from the address map shown in Table 5-2 through the I^2C serial interface.

Table 5-2. User Address Map

RANGE	ADDRESS	SIZE	DESCRIPTION
Registers	0xFFFE	2 B	Control register
	0xFFFC	2 B	Status register
	0xFFFA	2 B	Interrupt Enable
	0xFFF8	2 B	Interrupt Flags
	0xFFF6	2 B	CRC Result (16-bit CCITT)
	0xFFF4	2 B	CRC Length
	0xFFF2	2 B	CRC Start Address
	0xFFF0	2 B	Communication Watchdog Control register
	0xFFEE	2 B	Version
	0xFFEC	2 B	NDEF File ID register
	0xFFEA	2 B	Host Response register
	0xFFE8	2 B	NDEF Block Length register
	0xFFE6	2 B	NDEF File Offset register
	0xFFE4	2 B	Buffer Start register
	0xFFE2	2 B	Reserved
	0xFFE0	2 B	Reserved
	0xFFDE	2 B	SWTX register
	0xFFDC	2 B	Reserved
	0xFFDA	2 B	Custom SW1 and SW2 Response
Reserved	0x4000 to 0xFFDF		Reserved
	0x0BB8 to 0x3FFF	13KB	Reserved (for example, for future extension of NDEF Memory size)
Buffer	0x0000 to 0x0BB7	3000 B	Buffer Memory

NOTE

Crossing range boundaries causes writes to be ignored and reads to return undefined data.

5.6 I^2C Protocol

A command is always initiated by the master by addressing the device using the specified I^2C device address. The device address is a 7-bit I^2C address. The upper 4 bits are hard-coded, and the lower 3 bits are programmable by the input pins E0, E1, and E2 (see Table 5-3).

Table 5-3. I^2C Device Address

BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	1	1	E2	E1	E0
MSB						LSB

To write data, the device is addressed using the specified I^2C device address with R/$\overline{W}$ = 0, followed by the upper 8 bits of the first address to be written and the lower 8 bits of that address. Next (without a repeated START), the data to be written starting at the specified address is received. With each data byte received, the address is automatically incremented by 1. The write access is terminated by the STOP condition on the I^2C bus.

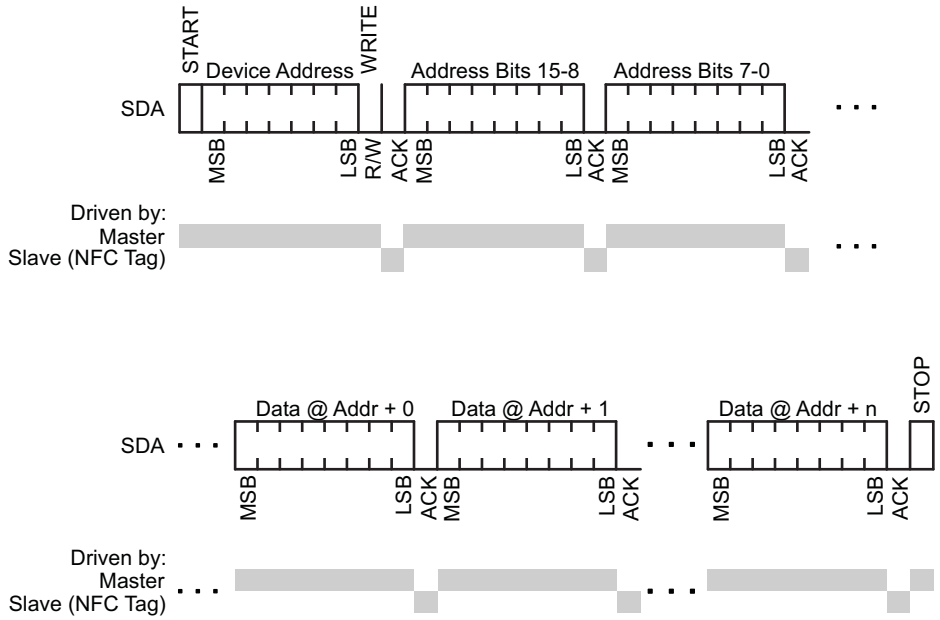


Figure 5-2. I²C Write Access

NOTE

The minimum I²C write transaction is 2 address bytes and 2 data bytes. Writes with only one 1 byte cause the data to be ignored. Avoid a transaction less than 1 data byte, as it results in an error.

To read data, the device is addressed using the specified I²C device address with R/$\overline{W}$ = 0, followed by the upper 8 bits of the first address to be read and then the lower 8 bits of that address. Next, a repeated START condition is expected with the I²C device address and R/$\overline{W}$ = 1. The device then transmit data starting at the specified address until a not acknowledge (NACK) and a STOP condition are received.

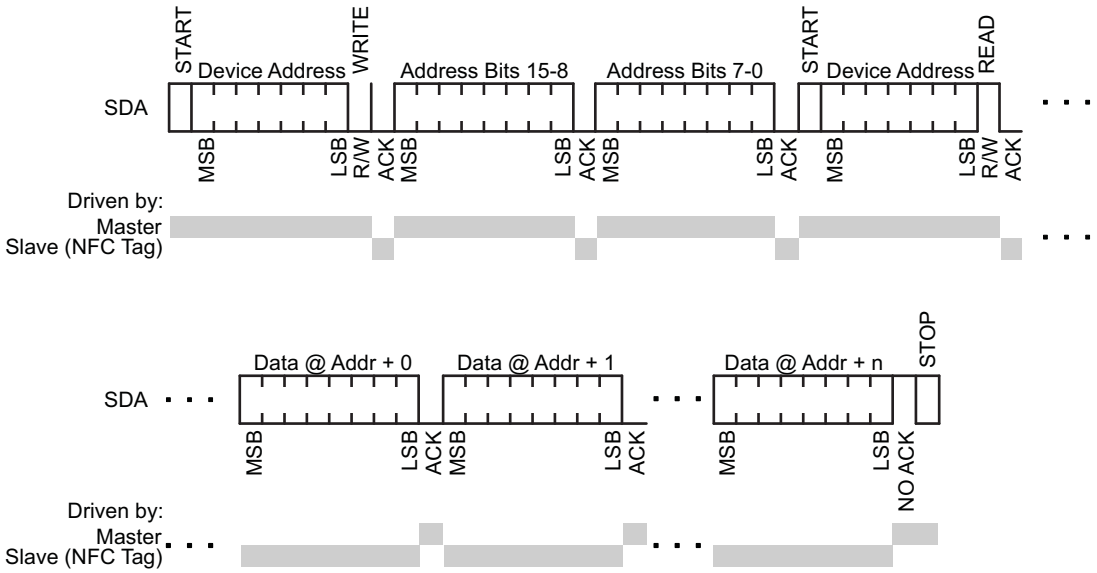


Figure 5-3. I²C Read Access

5.6.1 I²C Examples

Figure 5-4 and Figure 5-5 show examples of I²C accesses to the Control and Status registers, respectively. Comments are provided on the tags in the figures.

5.6.1.1 I²C Write

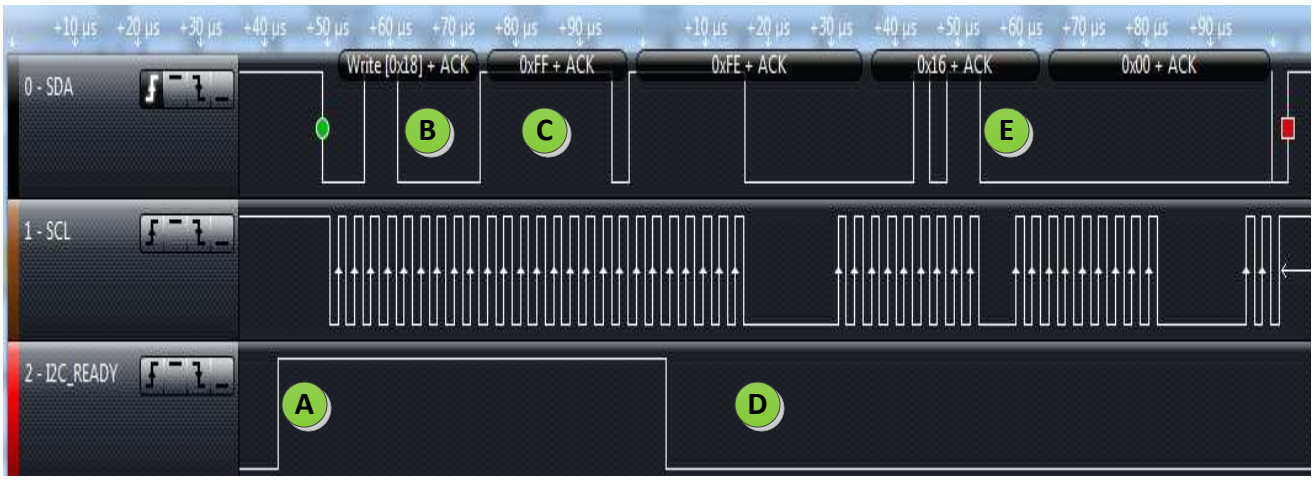


Figure 5-4. I²C Access Example: Write of the Control Register at Address 0xFFFE With 0x00, 0x16 (RF Enable = 1)

A. I2C_READY signal, by being high indicates that I²C communication can be started.

B. The device address (18h because E0 = E1 = E2 = 0) is being transmitted out.

C. Register address is 0xFFFEh (which is the Control register).

D. I2C_READY line is now low, new I²C communication should not be started.

E. The data to write is transmitted (0016h).

5.6.1.2 I²C Read

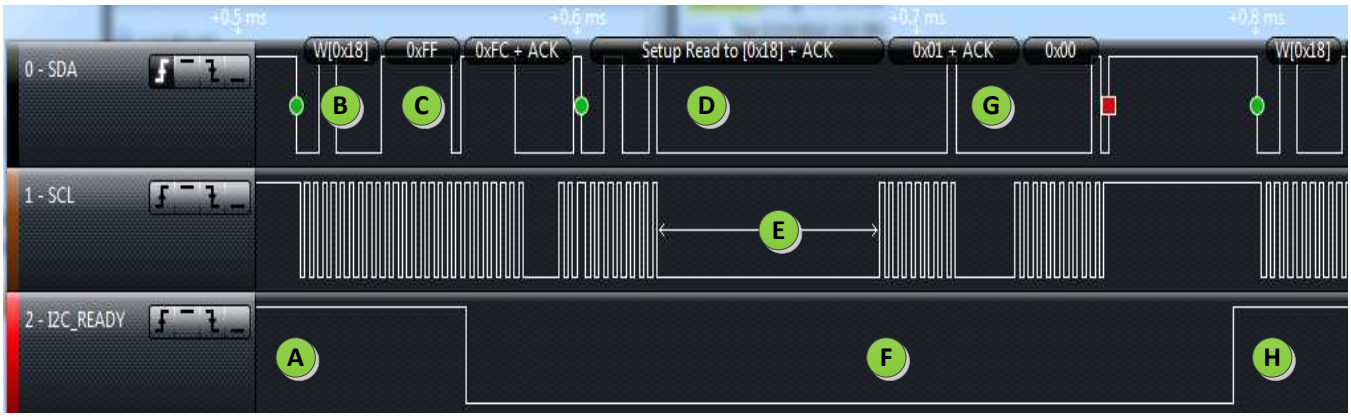


Figure 5-5. I²C Access Example: Read of the Status Register at Address 0xFFFC, Responds With 0x00, 0x01 (Device_Ready = 1)

A. I2C_READY signal, by being high indicates that I²C communication can be started.

B. Packet has started: the device address (18h because E0 = E1 = E2 = 0) is being sent out.

C. Address FFFCh next is transmitted, which is the address of the status register.

D. An I^2C restart was done and device address sent with a read selection.

E. Clock stretching is being used by the RF430CL331H when it needs more time to respond due to unfinished internal processing.

F. I2C_READY line is now low, new I^2C communication should not be started.

G. RF430CL331H drives the SDA line and returns the value of the status register, which is 0001h.

H. I2C_READY signal has returned to high, indicating communication can be started. This occurs after a short period of time after a STOP condition (in square red). This brief time is necessary for the RF430CL331H to finish internal processing.

5.6.2 BIP-8 Communication Mode With I^2C

The BIP-8 communication mode is enabled by setting the BIP-8 bit in the General Control register. All communication after setting this bit uses the following conventions with exactly 2 address bytes (16-bit address) and 2 data bytes (16-bit data) (see Table 5-4 and Table 5-5).

Table 5-4. Write Access

Master	Address Bits 15 to 8	Address Bits 7 to 0	Data at Addr + 0	Data at Addr + 1	BIP-8
Slave	N/A	N/A	N/A	N/A	N/A

The Bit-Interleaved Parity (BIP-8) is calculated using 16-bit address and 16-bit data. If the received BIP-8 does not match with received data, no write is performed. The BIP-8 calculation does not include the I^2C device address.

Table 5-5. Read Access

Master	Address Bits 15 to 8	Address Bits 7 to 0	N/A	N/A	N/A
Slave	N/A	N/A	Data at Addr + 0	Data at Addr + 1	BIP-8

For read access, the Bit-Interleaved Parity (BIP-8) is calculated using the received 16-bit address and the 2 transmitted data bytes, and it is transmitted back to the master. The BIP-8 does not include the device address.

5.7 NFC Type 4B Tag Platform

This device is an NFC Forum Type 4B Tag Platform and ISO/IEC 14443B-compliant transponder that operates according to the NFC Forum Tag Type-4 specification and supports NDEF (NFC Data Exchange Format) data structure. Through the RF interface, the user can read and update the contents in the NDEF memory. The NDEF message in its entirety would only be present on the memory of the host controller. The RF430CL331H only has a portion of the NDEF message at any one time.

NOTE

This device does not have nonvolatile memory; therefore, the information stored in the NDEF memory is lost when power is removed.

This device does not support the peer-to-peer mode or the reader/writer mode. All RF communication between an NFC forum device and this device is in the passive tag mode. The device responds by load modulation and is not considered an intentional radiator.

This device is intended to be used in applications where the primary reader/writer is, for example, an NFC-enabled handset. In this case, the host application can be considered the destination device, and the cell phone or other type of mobile device is treated as the end-point device.

This device supports ISO/IEC 14443-3, ISO/IEC 14443-4, and NFC Forum commands as described in the following sections.

The device supports data rates of 106, 212, 424, and 848 kbps.

Even though all data rates up to 848 kbps are supported, the device by default reports only the capability to support 106 kbps to the PCD. To change this behavior, use the sequence described in Section 5.7.3.

The device always answers ATTRIB commands from the PCD that request higher data rates. The NFC Forum specifies for NFC-B a maximum data rate of 106 kbps. It is assumed that an NFC-compliant PCD would not request higher data rates, thus, no interoperability issues are expected.

The NFC Forum Type 4B Tag Platform and ISO/IEC 14443B command and response structure is detailed in ISO/IEC 14443-3, ISO/IEC 14443-4, and NFC Forum-TS-Digital Protocol. The applicable ISO/IEC 7816-4 commands are detailed in NFC Forum-TS-Type-4-Tag_2.0.

5.7.1 ISO/IEC 14443-3 Commands

These commands use the character, frame format, and timing that are described in ISO/IEC 14443-3, clause 7.1. The following commands are used to manage communication:

REQB and WUPB

The REQB and WUPB commands sent by the PCD are used to probe the field for PICCs of Type B. In addition, WUPB is used to wake up PICCs that are in the HALT state. The number of slots N is included in the command as a parameter to optimize the anticollision algorithm for a given application.

Slot-MARKER

After a REQB or WUPB command, the PCD may send up to (N – 1) Slot-MARKER commands to define the start of each timeslot. Slot-MARKER commands can be sent after the end of an ATQB message received by the PCD to mark the start of the next slot or earlier if no ATQB is received (no need to wait until the end of a slot, if this slot is known to be empty).

ATTRIB

The ATTRIB command sent by the PCD includes information required to select a single PICC. A PICC receiving an ATTRIB command with its identifier becomes selected and assigned to a dedicated channel. After being selected, this PICC only responds to commands defined in ISO/IEC 14443-4 that include its unique CID.

HLTB

The HLTB command is used to set a PICC in HALT state and stop responding to a REQB.

After answering to this command, the PICC ignores any commands except the WUPB.

5.7.2 NFC Tag Type 4 Commands

Select

Selection of applications or files

Read Binary

Read data from file

Update Binary

Update (erase and write) data to file

5.7.3 Data Rate Settings

The device supports data rates of 106, 212, 424, and 848 kbps.

The device always answers ATTRIB commands from the PCD that request higher data rates. The NFC Forum specifies for NFC-B a maximum data rate of 106 kbps. It is assumed that an NFC-compliant PCD would not request higher data rates, thus, no interoperability issues are expected.

Even though all data rates up to 848 kbps are supported, the device by default reports only the capability to support 106 kbps to the PCD.

To change this behavior, follow these steps using the I^2C serial interface:

1. If you do not want to support all data rates up to 848 kbps, change the Data Rate Capability byte according to Table 5-7. Table 5-6 summarizes how to write the data rate, and the Data Rate Capability byte is set by the DATA 0 value in Step 3. Write Access.
2. Do the steps of the selected sequence. It is important to execute this sequence (in Table 5-6) before setting the Control register.

NOTE

The General Control register (see Section 5.11.1) is set to 0 after the sequence is completed in Table 5-6.

Table 5-6. Data Rate Setting Sequence

ACCESS TYPE	ADDRESS BITS 15 TO 8	ADDRESS BITS 7 TO 0	DATA 0	DATA 1
1. Write Access	0xFF	0xE0	0x4E	0x00
2. Write Access	0xFF	0xFE	0x80	0x00
3. Write Access	0x2A	0xBA	0xF7 (1)	0x00
4. Write Access	0x27	0xB8	0x00	0x00
5. Write Access	0xFF	0xE0	0x00	0x00

(1) Data Rate Capability according to Table 5-7. 0xF7: all data rates up to 848 kbps are supported.

Table 5-7. Data Rate Capability

DATA RATA CAPABILITY BYTE								DESCRIPTION
B7	B6	B5	B4	B3	B2	B1	B0	
0	0	0	0	0	0	0	0	PICC supports only 106 kbps in both directions (default).
1	x	x	x	0	x	x	x	Same data rate from PCD to PICC and from PICC to PCD compulsory
x	x	x	1	0	x	x	x	PICC to PCD, data rate supported is 212 kbps
x	x	1	x	0	x	x	x	PICC to PCD, data rate supported is 424 kbps
x	1	x	x	0	x	x	x	PICC to PCD, data rate supported is 848 kbps
x	x	x	x	0	x	x	1	PCD to PICC, data rate supported is 212 kbps
x	x	x	x	0	x	1	x	PCD to PICC, data rate supported is 424 kbps
x	x	x	x	0	1	x	x	PCD to PICC, data rate supported is 848 kbps

5.8 NDEF Structure

The NDEF message in its entirety is not stored at any time on the PICC. The host controller writes to the buffer memory as the NFC Type 4 requests come in.

Table 5-8 shows the mandatory structure. This NDEF message would be present on the memory of the host controller. For more information, refer to the NFC Forum Type 4 Tag Operation Specification (see Section 6.2).

Table 5-8. NDEF Application Data

<table>
<tr><td rowspan="10">NDEF Application
Selectable by Name =
D2760000850101h</td><td rowspan="8">Capability Container
Selectable by
File ID = E103h</td><td colspan="3">2B - CCLen</td><td rowspan="4"></td></tr>
<tr><td colspan="3">1B - Mapping version (1)</td></tr>
<tr><td colspan="3">2B - MLe = 000F9h (2)</td></tr>
<tr><td colspan="3">2B - MLc = 000F6h</td></tr>
<tr><td rowspan="5">NDEF File Ctrl TLV</td><td colspan="2">1B - Tag = 04h</td><td rowspan="5">The NDEF file control TLV is mandatory</td></tr>
<tr><td colspan="2">1B - Len = 06h</td></tr>
<tr><td rowspan="4">6B - Val</td><td>2B - File Identifier</td></tr>
<tr><td>2B - Maximum file size</td></tr>
<tr><td>1B - Read access</td></tr>
<tr><td>1B - Write access</td></tr>
<tr><td rowspan="3">NDEF File
Selectable by
File ID = xxyyh</td><td colspan="3">2B - Len</td><td rowspan="3">Mandatory NDEF file</td></tr>
<tr><td colspan="3">xB - Binary NDEF file content</td></tr>
<tr><td colspan="3">yB - Unused if Len < Maximum file size in File Ctrl TLV</td></tr>
</table>

(1) RF430CL331H only supports mapping version up to 2.0.
(2) RF430CL331H specific

Table 5-9. NDEF Application Data (Includes Proprietary Sections)

NDEF Application Selectable by Name = D2_7600_0085_0101h	Capability Container Selectable by File ID = E103h	2B - CCLen			
		1B - Mapping version (1)			
		2B -MLe = 000F9h (2)			
		2B -MLc = 000F6h (2)			
		NDEF File Ctrl TLV	1B - Tag = 04h		The NDEF file control TLV is mandatory
			1B - Len = 06h		
			6B - Val	2B - File Identifier	
				2B - Maximum file size	
				1B - Read access	
				1B - Write access	
		Proprietary File Ctrl TLV (1)	1B - Tag = 05h		Zero or more proprietary file control TLVs
			1B - Len = 06h		
			6B - Val	2B - File Identifier	
				2B - Maximum file size	
				1B - Read access	
				1B - Write access	
		⋮			
		Proprietary File Ctrl TLV (N)	1B - Tag = 05h		
			1B - Len = 06h		
			6B - Val	2B - File Identifier	
				2B - Maximum file size	
				1B - Read access	
				1B - Write access	
	NDEF File Selectable by File ID = xxyyh	2B - Len			Mandatory NDEF file
		xB - Binary NDEF file content			
		yB - Unused if Len < Maximum file size in File Ctrl TLV			
	Proprietary File (1) Selectable by File ID = xxyyh	2B - Len			Optional proprietary file
		xB - Binary proprietary file content			
		yB - Unused if Len < Maximum file size in File Ctrl TLV			
	⋮				
	Proprietary File (N) Selectable by File ID = xxyyh	2B - Len			Optional proprietary file
		xB - Binary proprietary file content			
		yB - Unused if Len < Maximum file size in File Ctrl TLV			

(1) RF430CL331H only supports mapping version up to 2.0.
(2) RF430CL331H specific

5.9 Typical Operation

Figure 5-6 shows typical operation of this device. Generally, on power up or reset, the host controller initializes this device and then enables the RF. When a PCD approaches the dynamic tag, it starts by performing the ISO14443-B anticollision sequence. This portion is handled automatically by the RF430CL331H.

Eventually the sequence reaches the NFC Type 4 level. When the PCD issues a file select, Read Binary or Update Binary commands, the RF430CL331H interrupts the host controller by asserting the INT0 pin to request the necessary information or act on the information. Each type of interrupt request is detailed in the following sections.

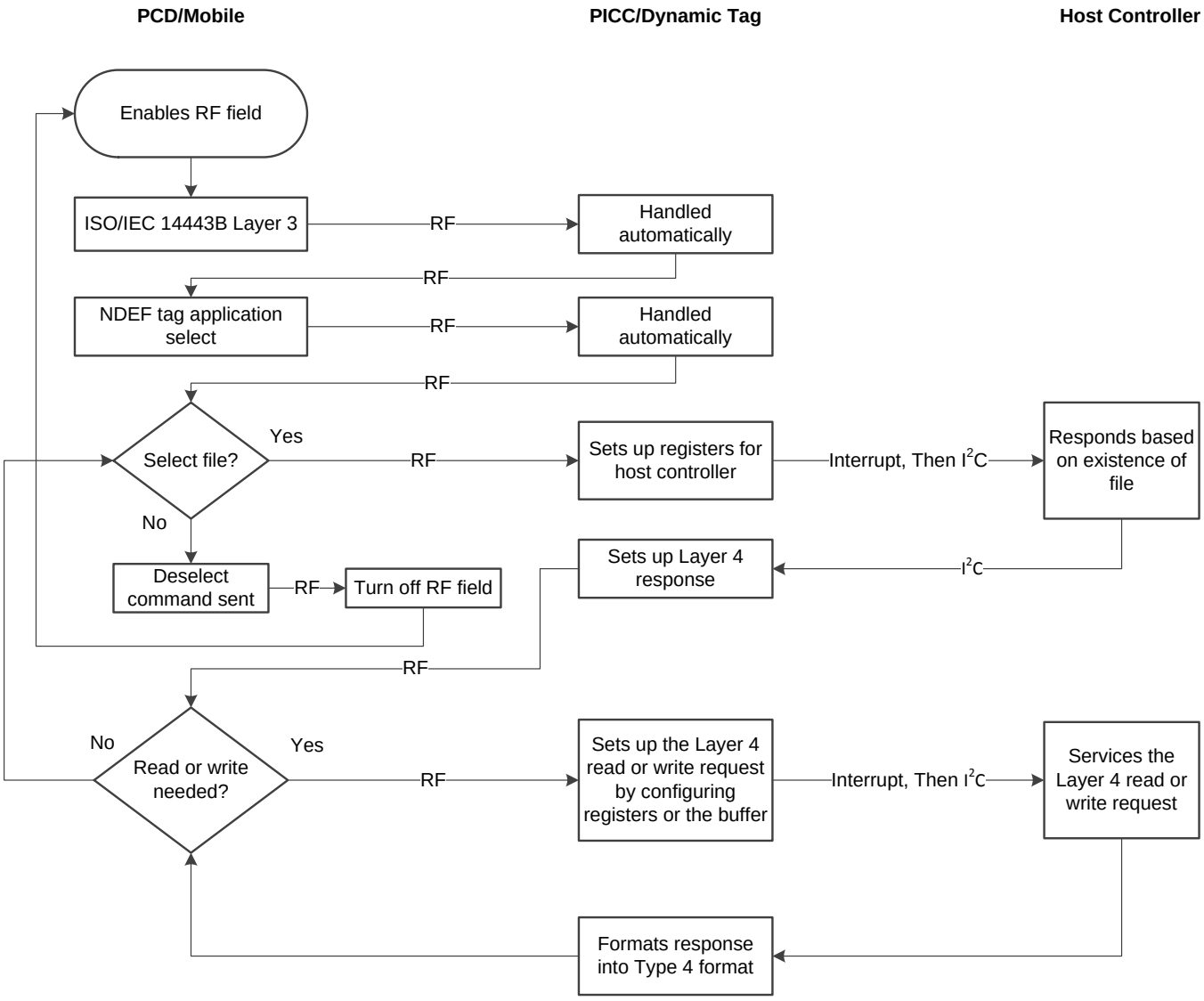


Figure 5-6. High-Level Flow

5.9.1 NDEF or Capability Container Select Procedure

This select procedure does not change between selection of the capability container or an NDEF file. These two types of selects can be differentiated by the file identifier that the RF430CL331H reports in the NDEF File Identifier register (see Section 5.11.7).

For the general flow, see Figure 5-7.

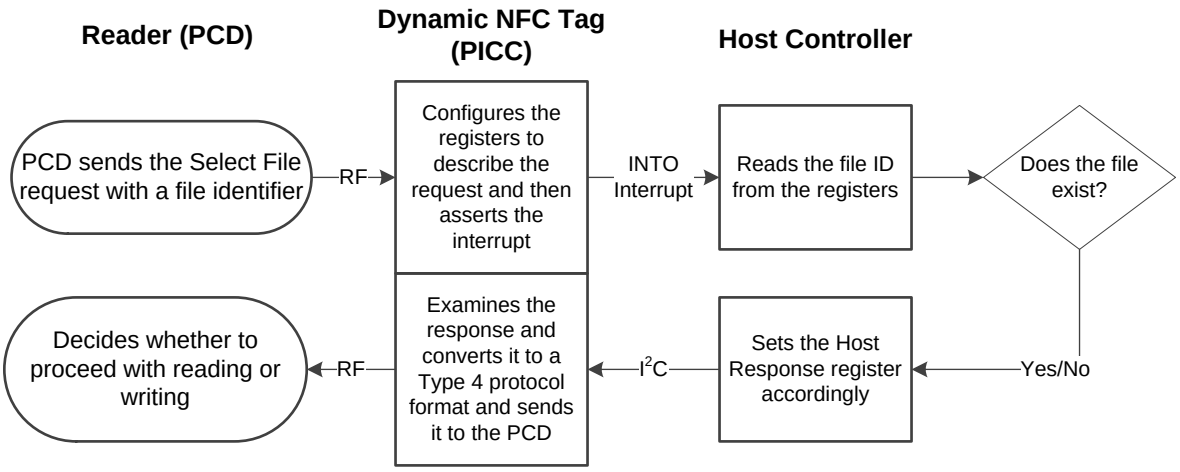


Figure 5-7. Select System Flow

The procedure:

1. PCD procedure:
   (a) Issues a Capability Container or a NDEF File Select command.
2. RF430CL331H procedure:
   (a) Receives the RF packet.
   (b) Sets the NDEF File Identifier register (see Section 5.11.7) using the file identifier that was included in the packet from the PCD.
   (c) Sets up the Status register (see Section 5.11.2) and the interrupt registers (see Section 5.11.3) to describe the file select request.
   (d) Ensure that General Type 4 request interrupt is enabled to generate the required interrupt on the INTO pin.
3. Host controller procedure:
   (a) Interrupt is received.
   (b) Checks the source of the interrupt by reading the interrupt registers (see Section 5.11.3).
   (c) The source of the interrupt is the General Type 4 request.
   (d) When there is a General Type 4 request, the Status register (see Section 5.11.2) must be read and the Type 4 Command field examined to determine what Type 4 command has been received.
   (e) The result is a File Select command.
   (f) The NDEF File Identifier register (see Section 5.11.7) should be read.
   (g) The host controller should, search its available files and determine if the file exists.
   (h) The interrupt must be cleared by writing to the Interrupt Flag register (see Section 5.11.3). This step must be done before setting the Interrupt Serviced field in the Host Response register (see Section 5.11.8).
   (i) If a specific Status Word (SW) response is necessary (generally for communicating specific error conditions) to the Select command:
      (i) Set the Custom Status Word Response register (see Section 5.11.13) with the desired status word.
      (ii) Set the Use Custom SW Response bit in the Host Response register (see Section 5.11.8).
   (j) To complete servicing the Select command interrupt, set the Interrupt Serviced field in the Host

Response register (see Section 5.11.8).

Servicing of the Select command is complete.

4. RF430CL331H procedure:
   (a) If the custom Status Words (SW) feature was not used:
      (i) If the host controller indicated that the file existed, the response to the PCD is SW1 = 90h and SW2 = 00h.
      (ii) If the host controller indicated that the file did not exist, the response to the PCD is SW1 = 6Ah and SW2 = 82h.
   (b) If the custom response feature was used, the response to the PCD is what was set in the Custom Status Word Response register (see Section 5.11.13).

5.9.2 NDEF or Capability Container Read Binary Procedure

This read procedure does not change between when the PCD reads the Capability Container or an NDEF file. These two types of reads can be differentiated by the file identifier that the RF430CL331H reports in the NDEF File Identifier register (see Section 5.11.7).

For the general flow, see Figure 5-8.

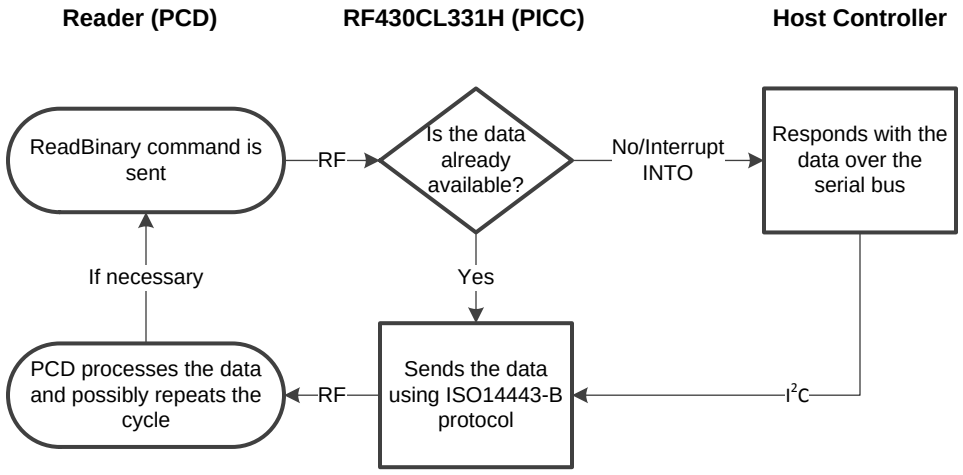


Figure 5-8. Read System Flow

The procedure:

1. PCD procedure:
   (a) Issues a Capability Container or a NDEF Read Binary command.
2. RF430CL331H procedure:
   (a) Receives the RF packet.
   (b) Checks its buffer and determines if all of the requested data in the Read Binary command exists already in the buffer.
   (c) If all the data is available in the buffer then (in the case that extra data was written in a previous read request):
      (i) No interrupt is issued to the host controller.
      (ii) The data is supplied in the response packet to the PCD automatically.
      (iii) The status word response SW1 = 90h and SW2 = 00h is appended to the packet.
      (iv) The flow returns to wait for the next Type 4 request.
   (d) If no data or only partial data is available, then an interrupt is issued to the host controller.
3. Host controller procedure:
   (a) An interrupt is received.
   (b) Checks the source of the interrupt by reading the interrupt registers (see Section 5.11.3).

(c) The source of the interrupt is the General Type 4 request.
(d) When there is a General Type 4 request, the Status register (see Section 5.11.2) must be read and the Type 4 Command field examined to determine what Type 4 command has been received.
(e) The result is a Read Binary command.
(f) The NDEF File Identifier register (see Section 5.11.7) may be read, but it is not necessary as it is always the file that the last Select command selected.
(g) Read the Buffer Start register (see Section 5.11.11) to determine where in the buffer of the RF430CL331H to begin storing the data.
(h) Read the NDEF File Offset register (see Section 5.11.10) to determine at which index in the NDEF or CC file to begin supplying the data to the RF430CL331H.
(i) Read the NDEF Block Length register (see Section 5.11.9) to determine what block length the PCD is requesting.
(j) Check if the request is valid:
  (i) If it is valid, write the data into the buffer of the RF430CL331H starting at Buffer Start index for NDEF Block Length bytes.
  (ii) If it is not valid, assert the Custom Status Word option in the Host Response register (see Section 5.11.8) and write the custom word in the Custom Status Word Response register (see Section 5.11.13). Only the status word response supplied will be sent out.
(k) If caching is desirable, extra sequential data can be written to the RF430CL331H buffer, up to the maximum RF430CL331H buffer length (length is 3000 bytes, highest index is 2999).

NOTE

To improve the Read Binary performance of the RF430CL331H , a caching feature may be used. After writing the requested Read Binary request data into the RF430CL331H buffer, extra sequential data may be written. If on the next Read Binary request, all of the requested data is in the buffer, the RF430CL331H automatically responds and services that request without any intervention of the host controller; that is, no interrupt is issued.

(l) Update the NDEF Block Length register (see Section 5.11.9) with the number of bytes written into the buffer.
(m) The interrupt must be cleared by writing to the Interrupt Flag register. This step must be done before setting the Interrupt Serviced field in the Host Response register.
(n) To complete servicing the Read Binary command interrupt, set the Interrupt Serviced field in the Host Response register.

4. RF430CL331H procedure:
(a) Only the requested data (even if extra was supplied) is included in the response packet to the PCD. The status words are appended to the response packet per NFC Type 4 specification.
(b) If the command was valid, the status words are SW1 = 90h and SW2 = 00h.
(c) If the custom response feature *was* used, the response to the PCD is only what was set in the Custom Status Word Response register.

5.9.2.1 NDEF Read Command Internal Buffer Handling

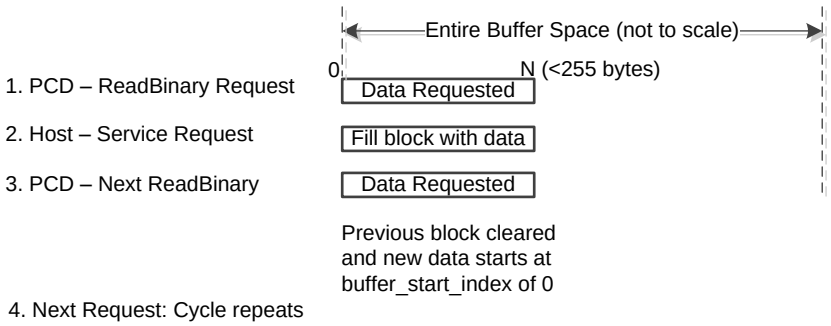


Figure 5-9. Read Buffer Flow (no extra data)

In normal read mode, when Read Prefetch functionality has not been enabled, each Read Binary request that comes in, is passed to the host controller and the internal state machine is in blocking mode until the data is sent back to the RF430CL331H . The RF430CL331H uses the same memory for each request, it is no more than the size of the read request packet length.

5.9.2.2 NDEF Read Command Internal Buffer Handling (With Caching)

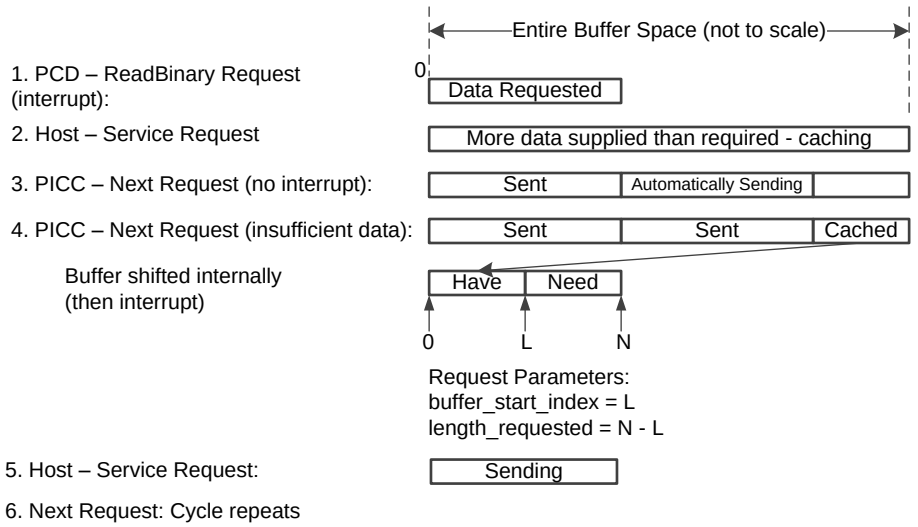


Figure 5-10. Read Buffer Flow (with caching)

1. PCD requests a block of data. PICC received the requests, sets up the internal register and asserts the INTO interrupt.
2. Host controller supplies the request but also adds more data on the file that is continuous with this request.
3. The next PCD request is fulfilled automatically because the data that is requested is already in the buffer. The host controller is not interrupted.
4. The next PCD request has insufficient data, so the data that is available is shifted to the beginning of the buffer and the unavailable data is requested.
5. The full request is transmitted out.
6. The cycle can repeat.

5.9.3 NDEF or Capability Container Read Procedure (Prefetch Feature)

The read prefetch feature includes the standard read procedure. However, after the requested data is written into the RF430CL331H buffer, when the RF430CL331H starts to transmit the requested data over the air, another interrupt is issued to the host controller indicating that extra data can be appended to the RF430CL331H buffer. The host controller can start adding data to the buffer while the RF430CL331H is transmitting over RF, because two tasks are happening at once, this increases the throughput of the system. For optimum operation, the host controller should cease to write extra data before the next interrupt. If the host controller does not cease to write, latency is introduced into the system, which can accumulate until requests start to time out. To determine how much is available to write the prefetch data, the time to send out the packet (that was requested) over RF can be calculated.

To enable read prefetch feature, the Read Prefetch interrupt must be enabled in the Interrupt Enable register (see Section 5.11.3).

For a general flow, see Figure 5-11.

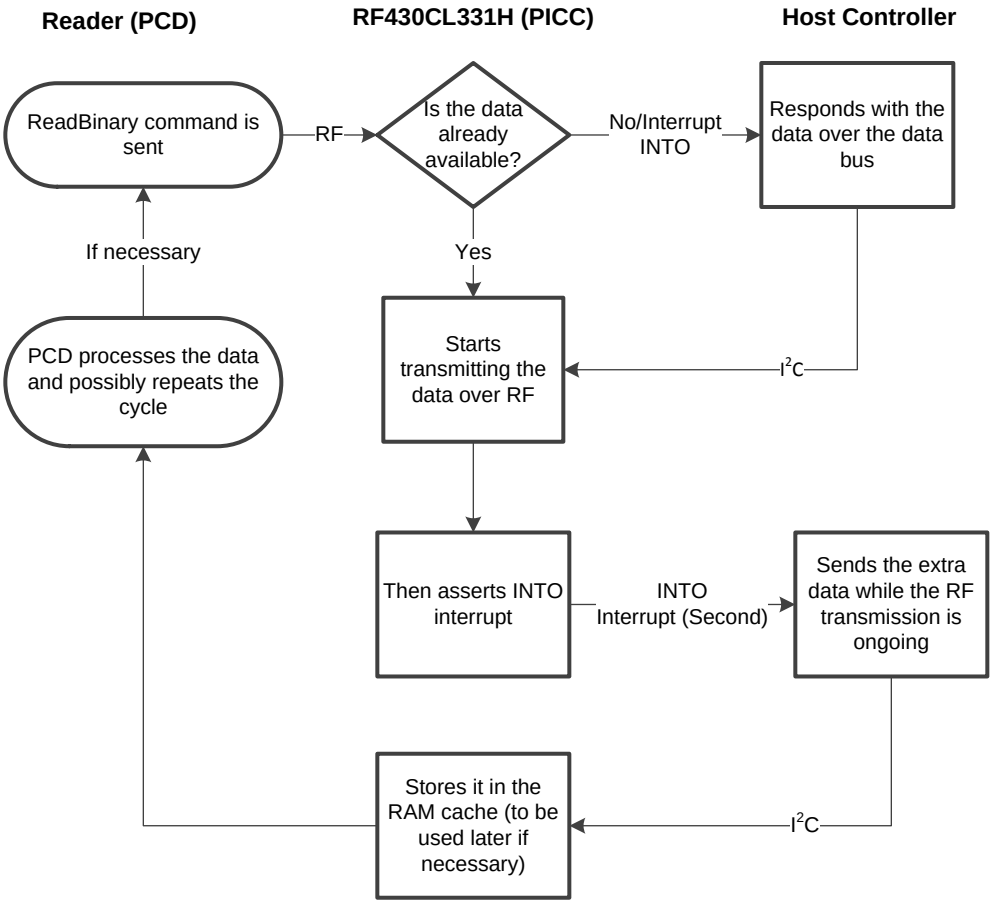


Figure 5-11. Read System Flow (Prefetch Feature)

The procedure:

1. PCD procedure:
   (a) Issues a Capability Container or a NDEF Read Binary command.
2. Dynamic Tag/RF430CL331H procedure:
   (a) Receives the RF packet.
   (b) Checks its buffer and determines if all of the requested data in the Read Binary command exists already in the buffer.
   (c) If all the data is available in the buffer then (in the case that extra data was written in a previous read request)
      (i) No General Type 4 interrupt is issued to the host controller.
      (ii) The data is supplied in the response packet to the PCD automatically.
      (iii) The status word response SW1 = 90h and SW2 = 00h is appended to the packet.
      (iv) The flow now goes to Step 4e.
   (d) If no data or only partial data is available, then a General Type 4 interrupt is issued to the host controller.
3. Host controller procedure:
   (a) Interrupt is received.
   (b) Checks the source of the interrupt by reading the interrupt registers (see Section 5.11.3).
   (c) The source of the interrupt is the General Type 4 request.
   (d) When there is a General Type 4 request, the Status register (see Section 5.11.2) must be read and the Type 4 Command field examined to determine what Type 4 command has been received.
   (e) The result is a Read Binary command.
   (f) The NDEF File Identifier register (see Section 5.11.7) may be read, but it is not necessary as it is always the file that the last Select command selected.
   (g) Read the Buffer Start register (see Section 5.11.11) to determine where in the buffer of the RF430CL331H to begin storing the data.
   (h) Read the NDEF File Offset register (see Section 5.11.10) to determine at which index in the NDEF or CC file to begin supplying the data to the RF430CL331H.
   (i) Read the NDEF Block Length register (see Section 5.11.9) to determine what block length the PCD is requesting.
   (j) Check if the request is valid:
      (i) If it is valid write the data into the buffer of the RF430CL331H starting at Buffer Start index for NDEF Block Length bytes.
      (ii) If it is not valid, assert the Custom Status Word option in the Host Response register (see Section 5.11.8) and write the custom word in the Custom Status Word Response register (see Section 5.11.13). Only the status word response supplied will be sent out.
   (k) Write the requested amount of data to the buffer starting at the Buffer Start register index.

NOTE

Read caching (writing data beyond the request in a General Type 4 request interrupt) should be avoided with the prefetch feature, because caching, at least initially, creates latency because the system is waiting (blocking) for the General Type 4 request interrupt to complete. Instead, in prefetch mode, only the requested data should be supplied in the General Type 4 request interrupt. When the Extra Data interrupt occurs afterwards (in tandem with the RF transmission), only then as much as possible extra data should be written to the buffer.

   (l) Update the NDEF Block Length register with how much bytes were written into the buffer.
   (m) The interrupt must be cleared by writing to the Interrupt Flag register. (This step must be done before setting the Interrupt Serviced field in the Host Response register.)
   (n) To complete servicing the Read Binary command interrupt, set the Interrupt Serviced field in the Host Response register.

4. Dynamic Tag RF430CL331H procedure:
   (a) Only the requested data (even if extra was supplied) is included in the response packet to the PCD. The status words are appended to the response packet per NFC Type 4 specification.
   (b) If the command was valid, the status words are SW1 = 90h and SW2 = 00h.
   (c) If the custom response feature *was* used, the response to the PCD is what was set in the Custom Status Word Response register.
   (d) RF transmission starts, the Extra Data interrupt is always asserted.
5. The host controller must service the Extra Data interrupt by appending to the buffer extra sequential data up until the buffer size (3000 bytes).
   (a) Checks the source of the interrupt by reading the interrupt registers.
   (b) The interrupt is an Extra Data interrupt.
   (c) Read the Buffer Start register to determine where in the buffer of the RF430CL331H to begin storing the data.

NOTE

When the Extra Data interrupt is enabled, the interrupt always occurs when the RF430CL331H is responding to the Read Binary request. However, this does not mean that every interrupt service can add to the RF430CL331H buffer (3000 bytes). If the Buffer Start register read indicates its index is at the end of the buffer, then no more data can be added. In this case the NDEF Block Length register should be set to 0 indicating that no data was added to the buffer. On the next Read Binary request, the valid data in the RF430CL331H buffer is shifted to the beginning to allow more room for extra data to be appended again.

   (d) NDEF File Offset register can be read.
   (e) Write sequential extra data to the buffer starting at the Buffer Start register index.
   (f) The time limit of writing extra data to the buffer is until the next Read Binary command is completed to be transmitted to the RF430CL331H. After that point, latency starts to be introduced into the system as the processing of the new packet is delayed.
   (g) Update the NDEF Block Length register with how many bytes were written into the buffer. If none, set to 0.
   (h) The prefetch interrupt must be cleared by writing to the Interrupt Flag register.
   (i) Set the Extra Data Send In bit in the Host Response register.
   (j) This completes servicing of the Read Prefetch interrupt.

5.9.3.1 NDEF Read Command With Prefetch Internal Buffer Handling

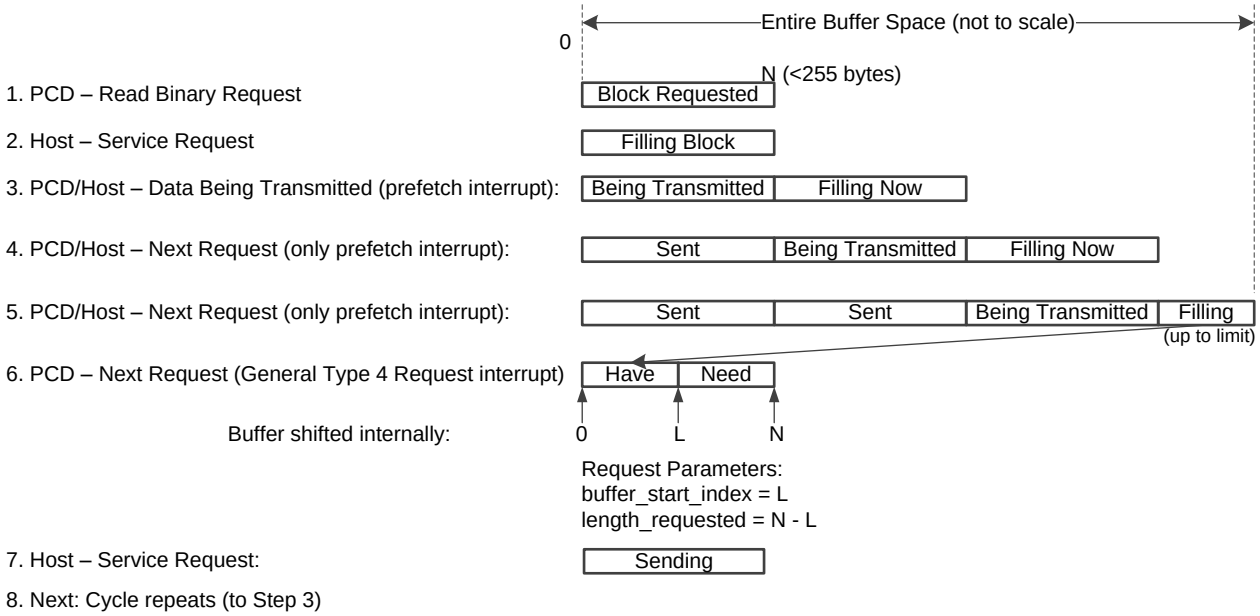


Figure 5-12. Read Buffer Flow (Prefetch Feature)

The key feature with Prefetch is that while the Read Binary is being transmitted, the next packet can be sent out by the host controller and be filling the internal RF430CL331H buffer. Each request is stored in the subsequent buffer memory until the buffer limit is reached. When the buffer limit is reached, the remaining unsent data is shifted to the beginning of the buffer and what data is needed for the next request is requested (see Step 6). This command is requested using the General Type 4 request interrupt (not with a prefetch interrupt) because it does not happen during the time when the RF430CL331H is sending data over RF.

Read buffer flow procedure (see Figure 5-12):

1. PCD requests a block of data.
2. PICC received the requests, sets up the internal register and asserts the INTO interrupt.
3. Host services the interrupt by supplying the data. PICC transmits the data. After starting to transmit the data, PICC issues a Read Prefetch interrupt. The host supplies the extra data while the RF communication is ongoing.
4. When the next Read Binary request comes, because the data is already cached, only the Prefetch interrupt is asserted.
5. This time a Prefetch interrupt is asserted, but only a portion of the data can be written because the buffer space is running out.
6. Because there is not enough data to service the Read Binary requests, a General Type 4 interrupt is asserted. The partial data that has been written previously is shifted to the beginning of the buffer and the only the remaining missing data is requested in the interrupt.
7. The complete data is sent out. The cycle repeats (the Prefetch interrupt is issued again).

If a prefetch interrupt is issued for a file, but there is no more data to send, this interrupt can be canceled by servicing it by setting the data length sent to 0. Also if data was sent by a prefetch but it was not needed by the RF430CL331H (due to a different request by the PCD) that data is discarded and the new request handling initiated.

5.9.4 NDEF or Capability Container Write Procedure (Blocking)

This write procedure does not change between when the PCD writes the Capability Container or an NDEF file. These two types of writes can be differentiated by the file identifier that the RF430CL331H reports in the NDEF File Identifier register (see Section 5.11.7).

For a general flow, see Figure 5-13.

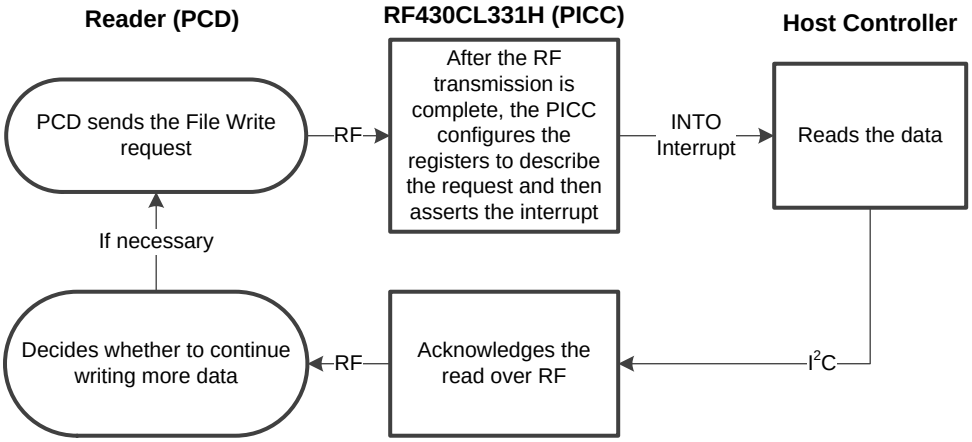


Figure 5-13. Write System Flow (Blocking)

The procedure:

1. PCD procedure:
   (a) Issues a Capability Container or a NDEF File Write (or Update Binary) command.
2. RF430CL331H procedure:
   (a) Receives the RF Update Binary packet.
   (b) Sets up the appropriate registers.
   (c) Issues the General Type 4 request interrupt.
3. Host controller procedure:
   (a) Checks the source of the interrupt by reading the interrupt registers (see Section 5.11.3).
   (b) The source of the interrupt is the General Type 4 request.
   (c) When there is a General Type 4 request, the Status register (see Section 5.11.2) must be read and the Type 4 Command field examined to determine what Type 4 command has been received.
   (d) The result is an Update Binary command.
   (e) The NDEF File Identifier register (see Section 5.11.7) may be read, but it is not necessary as it is always the file that the last Select command selected.
   (f) Read the Buffer Start register (see Section 5.11.11) to determine where in the buffer of the RF430CL331H to begin reading the stored data. Reading this register is unnecessary as it is always 0.
   (g) Read the NDEF File Offset register (see Section 5.11.10) to determine at which index of the NDEF or CC file the current data is starting.
   (h) Read the NDEF Block Length register (see Section 5.11.9) to determine how much data is being sent by the PCD in this packet.
   (i) Read the data from the buffer of the RF430CL331H starting at index of 0 until the block length supplied, updating the main file on the host controller.
   (j) If a specific Status Word (SW) response is necessary to the Update Binary command:
      (i) Set the Custom Status Word Response register (see Section 5.11.13) with the desired status word.
      (ii) Set the Use Custom SW Response bit in the Host Response register.
   (k) The interrupt must be cleared by writing to the Interrupt Flag register. This step must be done before setting the Interrupt Serviced field in the Host Response register.

(l) To complete servicing the Update Binary command interrupt, set the Interrupt Serviced field in the Host Response register.

4. RF430CL331H procedure:
   (a) If the custom SW feature was *not* used, the response is status words SW1 = 90h and SW2 = 00h.
   (b) If the custom response feature *was* used, the response to the PCD is what was set in the Custom Status Word Response register.

5.9.4.1 NDEF Write Command (Blocking) Internal Buffer Handling

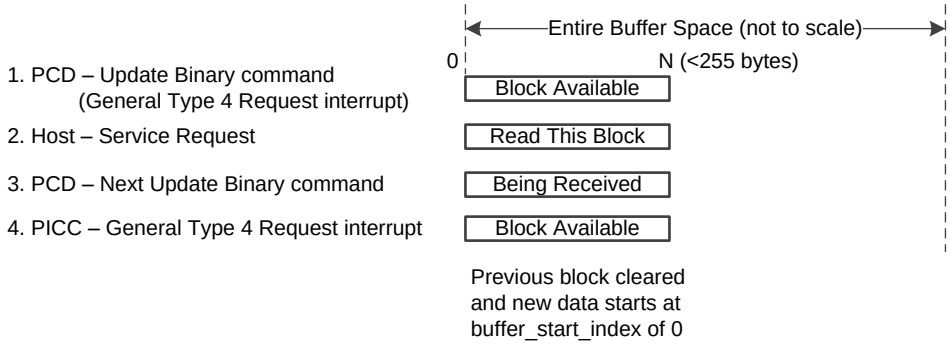


Figure 5-14. Write Buffer Flow (Blocking)

The write with blocking stores the send in data packet until it is read out by the host controller. Once it has been read out, the next write data packet is stored in the same section of memory. The cycle repeats with more Update Binary packets.

5.9.5 NDEF or Capability Container Write Procedure (Nonblocking)

This command is different from the blocking operation in that the RF430CL331H automatically responds to an Update Binary command with a success acknowledgment upon receiving the Update Binary packet.

After the acknowledgment, the PCD starts to send the next Update Binary block. The intent is to increase throughput by downloading the previous Update Binary packet while the new one is being transmitted into a separate buffer on the RF430CL331H.

Care must be taken to read out the entire packet before the new one is completely transmitted to the RF430CL331H. Otherwise, this creates latency that, if not corrected, accumulates to the point where one Update Binary packet request eventually times out.

To enable write nonblocking mode, set the Automatic ACK On Write field in the General Control register.

For a general flow, see Figure 5-15.

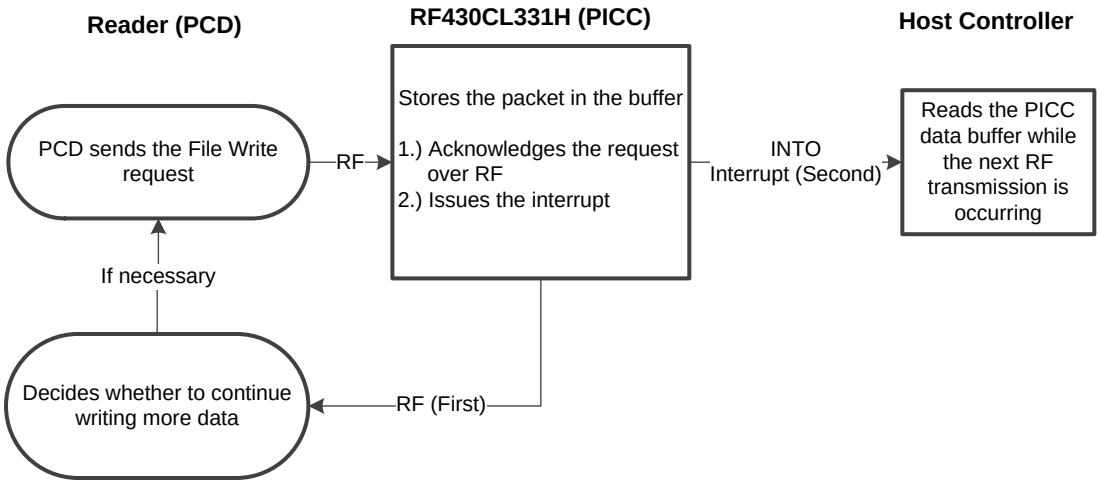


Figure 5-15. Write System Flow (Nonblocking)

1. PCD procedure:
   (a) Issues a Capability Container or a NDEF File Write (or Update Binary) command.
2. RF430CL331H procedure:
   (a) Receives the RF Update Binary packet.
   (b) Automatically responds with a successful acknowledgment: SW1 = 90h and SW2 = 00h.
   (c) Sets up the appropriate registers.
   (d) Issues the General Type 4 request interrupt.
   (e) Waits for a new Update Binary packet to be transmitted to.
3. Host controller procedure:
   (a) Checks the source of the interrupt by reading the interrupt registers (see Section 5.11.3).
   (b) The source of the interrupt is the General Type 4 request.
   (c) When there is a General Type 4 request, the Status register (see Section 5.11.2) must be read and the Type 4 Command field examined to determine what Type 4 command has been received.
   (d) The result is an Update Binary command.
   (e) The NDEF File Identifier register (see Section 5.11.7) may be read, but it is not necessary as it is always the file that the last Select command selected.
   (f) Read the Buffer Start register (see Section 5.11.11) to determine where in the buffer of the RF430CL331H to begin reading the stored data. Reading this register is unnecessary, as it is always 0.
   (g) Read the NDEF File Offset register (see Section 5.11.10) to determine at which index of the NDEF or CC file the current data is starting.
   (h) Read the NDEF Block Length register (see Section 5.11.9) to determine how much data is being sent by the PCD in this packet.
   (i) Read the data from the buffer of the RF430CL331H, starting at the index of 0, until the block length supplied, updating the main file on the host controller.
   (j) The interrupt must be cleared by writing to the Interrupt Flag register. This step must be done before setting the Interrupt Serviced field in the Host Response register.
   (k) To complete servicing the Update Binary command interrupt, set the Interrupt Serviced field in the Host Response register.

5.9.5.1 NDEF Write Procedure (Nonblocking) Internal Buffer Handling

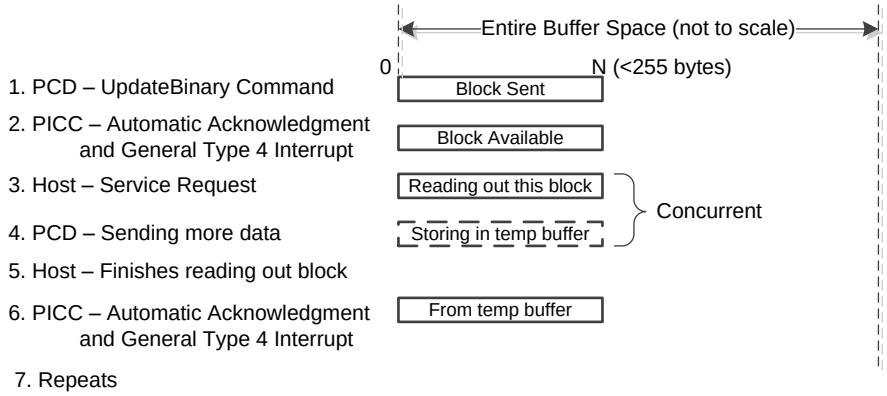


Figure 5-16. Write System Flow (Nonblocking)

The main difference in a nonblocking write operation is that when the data packet has been received from the PCD, the host controller is reading out the packet while the next one is being sent in (see Steps 3 and 4 in Figure 5-16). Data is received into a temporary buffer and when the last packet has been read out, the data in the temporary buffer is copied into the standard buffer so the data can be accessed by the host controller.

5.10 RF Command Response Timing Limits

Meeting specification timing is an important part of designing a stable and reliable system. There are various timing parameters that must be considered in this system, and one of the most important is the RF command response time.

The RF430CL331H negotiates the maximum allowable FWI timing (frame waiting time integer). This negotiated setting is the maximum of 8 (NFC Digital Protocol Section A.2, NFC-B Technology, FWI_{MAX}), giving the time of approximately 77 ms. This is the time that the PCD allows to respond to any command.

The RF430CL331H implements an internal timer monitoring this FWI timing specification. The internal timer defaults to approximately 55 ms instead of 77 ms due to variations in the internal oscillator frequency. The 55 ms allows meeting the 77-ms specification across all devices reliably.

Figure 5-17 gives the command response timings. A detailed description follows.

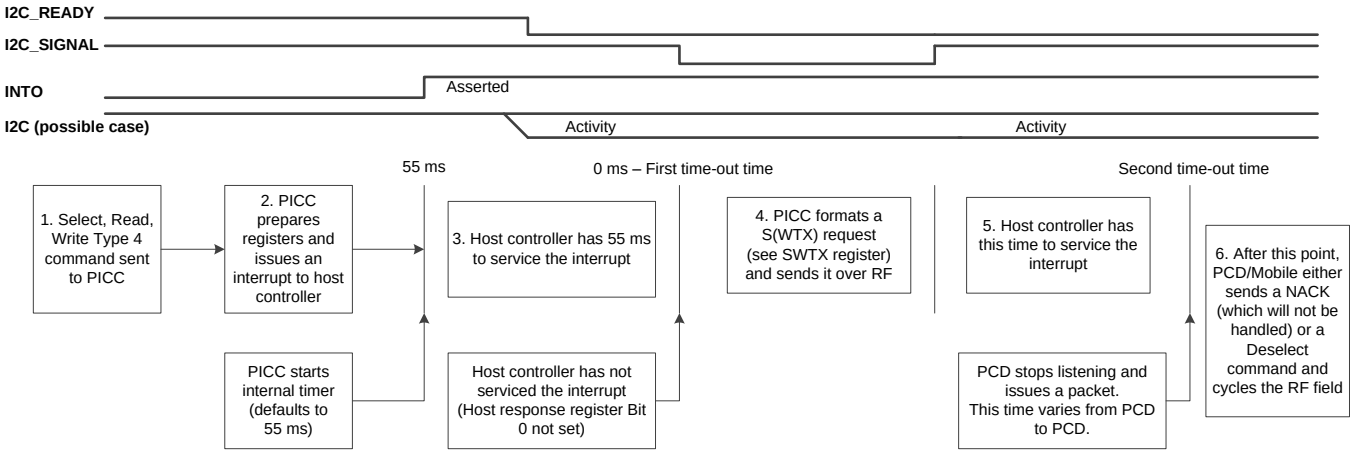


Figure 5-17. Timing Limits

1. The PCD issues a Type 4 command (Select, Read Binary, or Update Binary).
2. If this command needs host controller response, the RF430CL331H sets up the registers and asserts INTO.
3. The RF430CL331H starts the internal initial timer of 55 ms.
4. If the host controller does not respond in 55 ms, (that is, the Host Response register Interrupt Serviced Bit 0 is not set) the RF430CL331H sets the I2C_READY and I2C_SIGNAL pins to low, which. I2C_SIGNAL is a signal that is asserted when there is an active S(WTX) request ongoing. During this time the I^2C communication does not have to be stopped.
5. After the PICC issues the wait time extension there is another period of time in which the host controller has time to respond to the initial interrupt request.
6. At this time, the PCD sends out a packet. This point should be avoided, because this will likely mean the PCD will break off communications..
7. After several milliseconds, the RF430CL331H issues an S(WTX) request to the PCD.
   (a) The WTXM field in the Frame Wait Time Extension (see Section 5.11.12) is set with the value in the SWTX register.
8. Sends the Wait Time Extension request.
9. Sets the I2C_SIGNAL and I2C_READY pins to high indicating that communication can continue.
10. If the host controller does not service the interrupt in a certain period of time (the internal timer expires, but this does not produce an effect), the PCD issues a R(NACK) command. This and any other command are not handled by the RF430CL331H; there is no response, because the RF430CL331H command buffer still has the previous command that it has not serviced. Thus, the command must be serviced after the first S(WTX) request.
11. If the PCD issues a command after the first S(WTX) command, it is likely to not be serviced, and this typically results in a Deselect command with a field reset. The communication must be restarted.

5.11 Registers

NOTE

All 16-bit registers are in little-endian format: the least significant byte with bits 7-0 is at the lowest address (this address is always even). The most significant byte with bits 15-8 is at the highest address (this address is always odd).

5.11.1 General Control Register

Table 5-10. General Control Register

ADDRESS	15	14	13	12	11	10	9	8
0xFFFF	Reserved							Automatic ACK On Write
ADDRESS	7	6	5	4	3	2	1	0
0xFFFE	Reserved	Standby Enable	BIP-8	INTO Drive	INTO High	Enable INT	Enable RF	SW-Reset

Table 5-11. General Control Register Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-9	Reserved	R	0	Reserved for future use. Write with 0.
8	Automatic ACK On Write	R/W	0	Enabling this bit causes an automatic acknowledgment to be sent when an Update Binary command is received. The buffer must be read out immediately (possibly while a new Update Binary command is being received over RF). 0b = Manual acknowledgment of Update Binary command 1b = Automatic acknowledgment of Update Binary command
7	Reserved	R/W	0	
6	Standby Enable	R/W	0	Enables a low-power standby mode. The standby mode is entered if the RF interface is disabled, the communication watchdog is disabled, and no serial communication is ongoing. 0b = Standby mode disabled 1b = Standby mode enabled
5	BIP-8	R/W	0	Enables BIP-8 communication mode (bit interleaved parity). If BIP-8 is enabled, a separate running tally is kept of the parity (that is, the number of ones that occur) for every bit position in the bytes included in the BIP-8 calculation. The corresponding bit position of the BIP-8 byte is set to 1 if the parity is currently odd and is set to 0 if the parity is even – resulting in an overall even parity for each bit position including the BIP-8 byte. All communication when this bit is set must follow the conventions defined in the BIP-8 communication mode sections in Section 5.6.2. 0b = BIP-8 communication mode disabled 1b = BIP-8 communication mode enabled
4	INTO Drive	R/W	0	Configuration of the interrupt output pin INTO 0b = Pin is Hi-Z if there is no pending interrupt. Application provides an external pullup resistor if bit 3 (INTO High) = 0. Application provides an external pull-down resistor if bit 3 (INTO High) = 1. 1b = Pin is actively driven high or low if there is no pending interrupt. It is driven high if bit 3 (INTO High) = 0. It is driven low if bit 3 (INTO High) = 1.
3	INTO High	R/W	0	Configuration of the interrupt output pin INTO 0b = Interrupts are signaled with an active low 1b = Interrupts are signaled with an active high

Table 5-11. General Control Register Description (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
2	Enable INT	R/W	0	Global interrupt output enable 0b = Interrupt output disabled. The INTO pin is Hi-Z. 1b = Interrupt output enabled. The INTO pin signals any enabled interrupt according to the INTO High and INTO Drive bits.
1	Enable RF	R/W	0	Global enable of RF interface. This bit must be set before the PICC can respond to any RF commands. 0b = RF interface disabled 1b = RF interface enabled
0	SW-Reset	W	0	Software reset 0b = Always reads 0. 1b = Resets the device to default settings and clears memory. The serial communication is restored after t_{Ready}, and the register settings and NDEF memory must be restored afterward.

5.11.2 Status Register

Table 5-12. Status Register

ADDRESS	15	14	13	12	11	10	9	8
0xFFFD	Reserved							
ADDRESS	7	6	5	4	3	2	1	0
0xFFFC	Reserved		Type 4 Command MSb	Type 4 Command LSb	Reserved	RF Busy	CRC Active	Device Ready

Table 5-13. Status Register Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-6	Reserved	R	0	Reserved for future use. Write with 0.
5-4	Type 4 Command	R	0	This is set after a NFC Type 4 command is received and only must be serviced if a General Type 4 request interrupt has been asserted. Bit 5 + Bit 4 00b = No Type 4 command has been received 01b = File Select Command has been received and must be serviced 10b = Read Binary command has been received and must be serviced 11b = Update Binary command has been received and must be serviced
3	Reserved	R	0	Reserved for future use. Write with 0.
2	RF Busy	R	0	0b = No RF communication ongoing 1b = RF communication ongoing
1	CRC Active	R	0	0b = No CRC calculation ongoing 1b = CRC calculation ongoing
0	Device Ready	R	0	0b = Device not ready 1b = Device ready for serial communication and control

5.11.3 Interrupt Registers

The interrupt enable register (see Table 5-14 and Table 5-15) determines which interrupt events are signaled on the external output pin INTO. Setting any bit high in this register allows the corresponding event to trigger the interrupt signal. See Table 5-18 for a description of each interrupt.

All enabled interrupt signals are ORed together, and the result is signaled on the output pin INTO.

Table 5-14. Interrupt Enable Register

ADDRESS	15	14	13	12	11	10	9	8
0xFFFB	Reserved							Read Prefetch
ADDRESS	7	6	5	4	3	2	1	0
0xFFFA	Generic Error	RF Field Removed	General Type 4 Request	BIP-8 Error Detected	CRC Calculation Completed	Reserved		

Table 5-15. Interrupt Enable Register Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-9	Reserved	R	0	Reserved for future use. Write with 0.
8	Read Prefetch	R/W	0	Enable for the Read Prefetch IRQ. All enabled interrupt signals are ORed together, and the result is signaled on the output pin INTO. 0b = IRQ disabled 1b = IRQ enabled
7	Generic Error	R/W	0	Enable for the Generic Error IRQ. All enabled interrupt signals are ORed together, and the result is signaled on the output pin INTO. 0b = IRQ disabled 1b = IRQ enabled
6	RF Field Removed	R/W	0	Enable for the RF Field Removed IRQ. All enabled interrupt signals are ORed together, and the result is signaled on the output pin INTO. 0b = IRQ disabled 1b = IRQ enabled
5	General Type 4 Request	R/W	0	Enable for the General Type 4 Request IRQ. All enabled interrupt signals are ORed together, and the result is signaled on the output pin INTO. 0b = IRQ disabled 1b = IRQ enabled
4	BIP-8 Error Detected	R/W	0	Enable for the BIP-8 Error Detected IRQ. All enabled interrupt signals are ORed together, and the result is signaled on the output pin INTO. 0b = IRQ disabled 1b = IRQ enabled
3	CRC Calculation Completed	R/W	0	Enable for the CRC Calculation Completed IRQ. All enabled interrupt signals are ORed together, and the result is signaled on the output pin INTO. 0b = IRQ disabled 1b = IRQ enabled
2-0	Reserved	R	0	Reserved for future use. Write with 0.

The interrupt flag register (see Table 5-16 and Table 5-17) is used to report the status of any interrupts that are pending. Setting any bit high in this register acknowledges and clears the interrupt associated with the respective bit. See Table 5-18 for a description of each interrupt.

Table 5-16. Interrupt Flag Register

ADDRESS	15	14	13	12	11	10	9	8
0xFFF9	Reserved							Read Prefetch
ADDRESS	7	6	5	4	3	2	1	0
0xFFF8	Generic Error	RF Field Removed	General Type 4 Request	BIP-8 Error Detected	CRC Calculation Completed	Reserved		

Table 5-17. Interrupt Flag Register Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-9	Reserved	R	0	Reserved for future use. Write with 0.
8	Read Prefetch	R/W	0	Flag pending Read Prefetch IRQ. Read Access: 0b = No pending IRQ 1b = Pending IRQ Write Access: 0b = No change 1b = Clear pending IRQ flag
7	Generic Error	R/W	0	Flag pending Generic Error IRQ. Read Access: 0b = No pending IRQ 1b = Pending IRQ Write Access: 0b = No change 1b = Clear pending IRQ flag
6	RF Field Removed	R/W	0	Flag pending RF Field Removed IRQ. Read Access: 0b = No pending IRQ 1b = Pending IRQ Write Access: 0b = No change 1b = Clear pending IRQ flag
5	General Type 4 Request	R/W	0	Flag pending General Type 4 Request IRQ. Read Access: 0b = No pending IRQ 1b = Pending IRQ Write Access: 0b = No change 1b = Clear pending IRQ flag

Table 5-17. Interrupt Flag Register Description (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
4	BIP-8 Error Detected	R/W	0	Flag pending BIP-8 Error Detected IRQ. Read Access: 0b = No pending IRQ 1b = Pending IRQ Write Access: 0b = No change 1b = Clear pending IRQ flag
3	CRC Calculation Completed	R/W	0	Flag pending CRC Calculation Completed IRQ. Read Access: 0b = No pending IRQ 1b = Pending IRQ Write Access: 0b = No change 1b = Clear pending IRQ flag
2-0	Reserved	R	0	Reserved for future use. Write with 0.

Table 5-18. Interrupts

INTERRUPT	DESCRIPTION
CRC Calculation Completed	This IRQ occurs when a CRC calculation that is triggered by writing into the CRC registers is completed and the result can be read from the CRC result register (see Section 5.11.4).
BIP-8 Error Detected	This IRQ occurs when a BIP-8 error is detected (only if the BIP-8 communication mode is enabled).
General Type 4 Request	This IRQ occurs if a NFC Type 4 command has been received (Select, Read Binary, Update Binary) and requires the service of the host controller.
RF Field Removed	This IRQ occurs when at least NDEF Tag Application Select command has been received and after that the RF field is removed.
Generic Error	This IRQ occurs for any error that makes the device unreliable or nonoperational.
Read Prefetch	This IRQ occurs immediately after Read Binary request has been serviced (automatically or manually) and the RF transmission has been started. This allows RF transmission and I^2C communication to happen at the same time.

5.11.4 CRC Registers

Writing the CRC address and the CRC length registers initiates a 16-bit CRC calculation of the specified address range. The length is always assumed to be even (16-bit aligned). Writing the length register starts the CRC calculation.

During the CRC calculation, the CRC active bit is set (= 1). When the calculation is complete, the CRC completion interrupt flag is set and the result of the CRC calculation can be read from the CRC result register. TI recommends performing a CRC calculation only when the RF interface is disabled (RF Enable = 0).

Table 5-19. CRC Result Register

ADDRESS	15	14	13	12	11	10	9	8
0xFFF7	CRC CCITT Result (high byte)							
ADDRESS	7	6	5	4	3	2	1	0
0xFFF6	CRC CCITT Result (low byte)							

Table 5-20. CRC Result Register Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-0	CRC-CCITT Result	R	0	CRC-CCITT Result

Table 5-21. CRC Length Register

ADDRESS	15	14	13	12	11	10	9	8
0xFFF5	CRC Length (high byte)							
ADDRESS	7	6	5	4	3	2	1	0
0xFFF4	CRC Length (low byte)							

Table 5-22. CRC Length Register Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-0	CRC Length	RW	0	CRC Length. Always assumed to be even (Bit 0 = 0). Writing into high byte starts CRC calculation.

Table 5-23. CRC Start Address Register

ADDRESS	15	14	13	12	11	10	9	8
0xFFF3	CRC Start Address (high byte)							
ADDRESS	7	6	5	4	3	2	1	0
0xFFF2	CRC Start Address (low byte)							

Table 5-24. CRC Start Address Register Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-0	CRC Start Address	RW	0	CRC Start Address. Defines start address within NDEF memory. This address is always assumed to be even (bit 0 = 0).

The CRC is calculated based on the CCITT polynomial initialized with 0xFFFF.

CCITT polynomial: $x^{16} + x^{12} + x^5 + 1$

5.11.5 Communication Watchdog Register

When the communication watchdog is enabled, it expects a write or read access within a specified period; otherwise, the watchdog resets the device. If the BIP-8 communication mode is enabled, the transfer must be valid to be accepted as a watchdog reset.

Table 5-25. Communication Watchdog Register

ADDRESS	15	14	13	12	11	10	9	8
0xFFF1	Reserved							
ADDRESS	7	6	5	4	3	2	1	0
0xFFF0	Reserved				Time-out Period Selection			Enable

Table 5-26. Communication Watchdog Register Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-4	Reserved	R	0	Reserved for future use. Write with 0.
3-1	Time-out Period Selection	R/W	0	000b = 2 s ±30% (1) 001b = 32 s ±30% (1) 010b = 8.5 min ±30% (1) 011b to 111b = Reserved
0	Enable	R/W	0	0b = Communication Watchdog disabled 1b = Communication Watchdog enabled

(1) This value is based on use of the integrated low-frequency oscillator with a frequency of 256 kHz ±30%.

5.11.6 Version Register

Provides version information about the implemented ROM code.

Table 5-27. Version Register

ADDRESS	15	14	13	12	11	10	9	8
0xFFEF	Major Version							
ADDRESS	7	6	5	4	3	2	1	0
0xFFEE	Minor Version							

Table 5-28. Version Register Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-8	Major Version	R	1	Software version
7-0	Minor Version	R	0	Software version

5.11.7 NDEF File Identifier Register

This register is used by the host controller to determine which file has been selected (or also for Read Binary and Update Binary commands as needed).

Table 5-29. NDEF File Identifier Register

ADDRESS	15	14	13	12	11	10	9	8
0xFFED	File Identifier Second Byte							
ADDRESS	7	6	5	4	3	2	1	0
0xFFEC	File Identifier First Byte							

Table 5-30. NDEF File Identifier Register Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-8	File Identifier Second Byte	R/W	0	This is the file identifier. It is references the second byte of the File ID in the Select command. (For example this byte for the Capability Container would be 03h).
7-0	File Identifier First Byte	R/W	0	This is the file identifier. It is references the first byte of the File ID in the Select command. (For example this byte for the Capability Container would be E1h).

5.11.8 Host Response Register

This register is used, after an interrupt is asserted by the RF430CL331H. It communicates various responses from the host controller. The actual interrupt flag clearing must happen immediately before setting the response in this register.

Table 5-31. Host Response Register

ADDRESS	15	14	13	12	11	10	9	8
0xFFEB	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
ADDRESS	7	6	5	4	3	2	1	0
0xFFEA	Reserved	Reserved	Reserved	Reserved	Extra Data Sent In	Use Custom SW Response	File Exists	Interrupt Serviced

Table 5-32. Host Response Register Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-4	Reserved	R/W	0	Reserved for future use. Write with 0.
3	Extra Data Sent In	R/W	0	This may only be set if the Read Prefetch interrupt has been asserted. This is possible only after a Read Binary command. This indicates to the RF430CL331H that extra data has been written to the buffer during RF data transmission to a previous Read Binary command. To enable this feature, the Extra Data Interrupt Enable must be set. This also called Prefetch on Read. 0b = No extra data has been written. 1b = Extra data has been written. Update buffer size.
2	Use Custom SW Response	R/W	0	This sets whether or not a custom SW (status word) should be responded to a NFC Type 4 command (Select, Read Binary, Update Binary). 0b = Default response to the PCD. 1b = Custom response to the PCD. The actual SW response is taken from the Custom SW Response Register.
1	File Exists	R/W	0	This is the response to the interrupt of General Type 4 Request with status of file select. 0b = File named in the NDEF File Identifier Register does *not* exist. 1b = File named in the NDEF File Identifier Register *does* exist.
0	Interrupt Serviced	R/W	0	Setting this bit high after an interrupt (this applies only to General Type 4 Requests IRQ) has been asserted by the RF430CL331H indicates that the interrupt has been completely serviced. The actual interrupt flag clearing must happen immediately before setting this register. 0b = The interrupt is in the process of being serviced by the host controller 1b = The interrupt has been serviced, RF430CL331H to start processing the response

5.11.9 NDEF Block Length Register

This register indicates the block length of the Read Binary or Update Binary commands to the host controller.

Table 5-33. NDEF Block Length Register

ADDRESS	15	14	13	12	11	10	9	8
0xFFE9	Block Length MSB							
ADDRESS	7	6	5	4	3	2	1	0
0xFFE8	Block Length LSB							

Table 5-34. NDEF Block Length Register Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-8	Block Length MSB	R/W	0	Block length most significant byte.
7-0	Block Length LSB	R/W	0	Block length least significant byte.

5.11.10 NDEF File Offset Register

This register indicates the offset of the Read Binary or Update Binary commands to the host controller.

Table 5-35. NDEF File Offset Register

ADDRESS	15	14	13	12	11	10	9	8
0xFFE7	File Offset MSB							
ADDRESS	7	6	5	4	3	2	1	0
0xFFE6	File Offset LSB							

Table 5-36. NDEF File Offset Register Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-8	File Offset MSB	R/W	0	File offset most significant byte.
7-0	File Offset LSB	R/W	0	File offset least significant byte.

5.11.11 Buffer Start Register

This register is written after a Read Binary command by the host controller indicating the index in buffer memory where the data started to be written. On an Update Binary command, this register indicates where the RF430CL331H has started to write the packet in its buffer memory.

Table 5-37. Buffer Start Register

ADDRESS	15	14	13	12	11	10	9	8
0xFFE5	Buffer Start MSB							
ADDRESS	7	6	5	4	3	2	1	0
0xFFE4	Buffer Start LSB							

Table 5-38. Buffer Start Register Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-8	Buffer Start MSB	R/W	0	Buffer start most significant byte.
7-0	Buffer Start LSB	R/W	0	Buffer start least significant byte.

5.11.12 SWTX Register

When a PCD issues a command, there is a time-out that is negotiated (FWI in the SENSB_RES/ATQB command). The RF430CL331H has this amount of time to respond to the PCD command. If this time-out cannot be met by RF430CL331H, the NFC protocol allows a sending a S(WTX) request (refer to Section 13.2.2 of the NFC Digital Protocol). This allows the time-out to be restarted after the PCD S(WTX) response.

When the internal state machine determines that a wait time extension is necessary, it uses this register value to populate the INF field of the S(WTX) request (refer to Table 84 of the NFC Digital Protocol). This custom setting response allows flexibility in negotiating this wait time extension.

Table 5-39. SWTX Register

ADDRESS	15	14	13	12	11	10	9	8
0xFFDF	Reserved							
ADDRESS	7	6	5	4	3	2	1	0
0xFFDE	SWTX Request							

Table 5-40. SWTX Register Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-8	Reserved	R/W	0	Reserved for future use. Write with 0.
7-0	SWTX Request	R/W	1	S(WTX) request byte.

5.11.13 Custom Status Word Response Register

On a NFC Type 4 command (Select, Read Binary, Update Binary), the response contains a status word (SW). This indicates whether or not the request was successful. By default, the RF430CL331H handles the SW responses automatically with predefined values. However, if custom responses are needed, for custom error status word responses, this feature may be used.

When the Use Custom SW Response is set in the Host Response register, the RF430CL331H firmware uses the SW set here to respond to the command.

Table 5-41. Custom Status Word Response Register

ADDRESS	15	14	13	12	11	10	9	8
0xFFDB	Custom Status Word Response MSB							
ADDRESS	7	6	5	4	3	2	1	0
0xFFDA	Custom Status Word Response LSB							

Table 5-42. Custom Status Word Response Register Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-8	Custom Status Word Response MSB	R/W	0	Custom status word 1 (SW1).
7-0	Custom Status Word Response LSB	R/W	0	Custom status word 2 (SW2).

5.12 Identification

5.12.1 Revision Identification

The device revision information is shown as part of the top-side marking on the device package. The device-specific errata sheet describes these markings (see Section 7.2.1).

5.12.2 Device Identification

The device type can be identified from the top-side marking on the device package. The device-specific errata sheet describes these markings (see Section 7.2.1).

5.12.3 JTAG Identification

This device does not provide JTAG-compliant boundary scan test.

5.12.4 Software Identification

The Version register (see Section 5.11.6) stores the software version number.

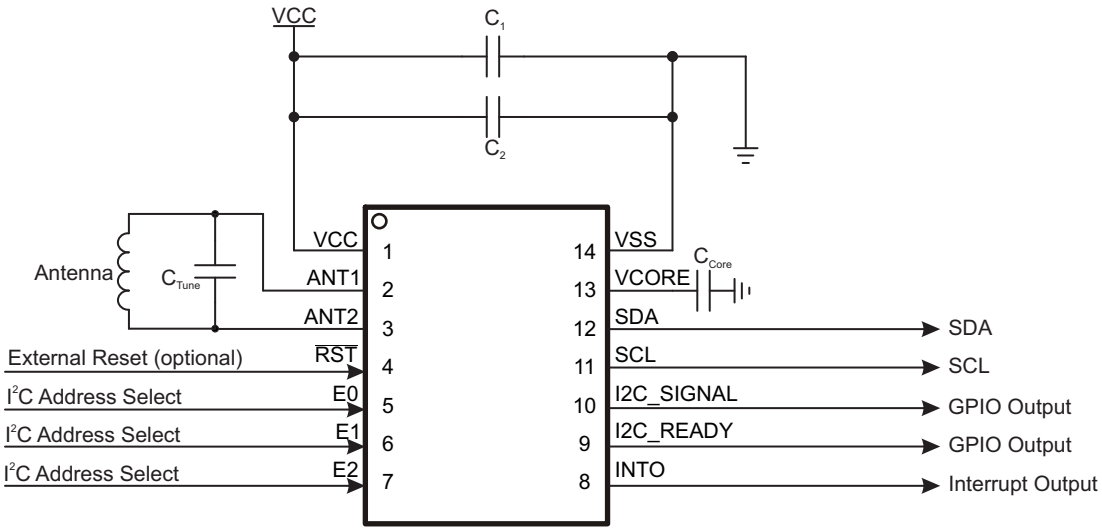
6 Applications, Implementation, and Layout

NOTE

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 Application Diagram

Figure 6-1 shows a sample application diagram.



For recommended capacitance values, see Recommended Operating Conditions.

Figure 6-1. Application Diagram

6.2 References

1. ISO/IEC 14443-2:2010, Part 2: Radio frequency interface power and signal interface (http://www.iso.org)
2. ISO/IEC 14443-3:2011, Part 3: Initialization and anticollision (http://www.iso.org)
3. ISO/IEC 14443-4:2008, Part 4: Transmission protocols (http://www.iso.org)
4. NFC Data Exchange Format (NDEF) Technical Specification (http://nfc-forum.org/)
5. NFC Forum Type 4 Tag Operation Specification (http://nfc-forum.org/)
6. NFC Digital Protocol Technical Specification, Section 13.2.2, Frame Wait Time Extension (http://nfc-forum.org/)

7 Device and Documentation Support

7.1 Device Support

7.1.1 Development Support

7.1.1.1 Getting Started and Next Steps

TI offers an extensive line of development tools, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules. The tool's support documentation is electronically available within the Code Composer Studio™ Integrated Development Environment (IDE).

The following products support development of the RF430CL331H device applications:

Software Development Tools: Code Composer Studio Integrated Development Environment (IDE): including Editor C/C++/Assembly Code Generation, and Debug plus additional development tools.

Hardware Development Tools: For a complete listing of development-support tools for the RF430CL331H platform, visit the TI website at www.ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

7.1.2 Device and Development Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all RF430 MCU devices and support tools. Each commercial family member has one of three prefixes: RF, P, or X (for example, RF430FRL152H). TI recommends two of three possible prefix designators for its support tools: RF and X. These prefixes represent evolutionary stages of product development from engineering prototypes (with X for devices and tools) through fully qualified production devices and tools (with RF for devices tools).

Device development evolutionary flow:

X – Experimental device that is not necessarily representative of the electrical specifications of the final device

P – Silicon die that conforms to the electrical specifications of the final device but has not completed quality and reliability verification

RF – Fully qualified production device

Support tool development evolutionary flow:

X – Development-support product that has not yet completed TI's internal qualification testing.

RF – Fully-qualified development-support product

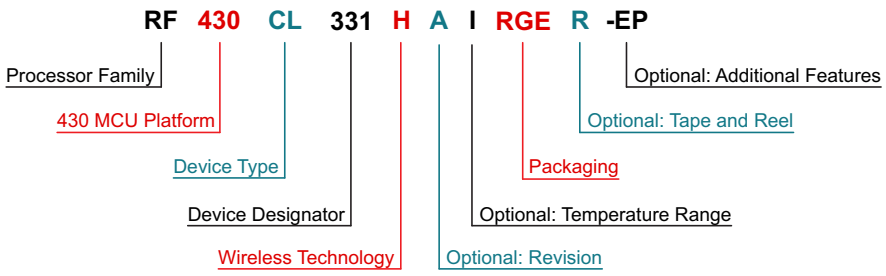
X and P devices and X development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

RF devices and RF development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X and P) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, RGE) and temperature range (for example, T). Figure 7-1 provides a legend for reading the complete device name for any family member.



Processor Family	RF = Embedded RF radio X = Experimental silicon P = Prototype device
430 MCU Platform	TI's low-power microcontroller platform
Device Type	C = Fixed function L = Low-power series
Device Designator	Various levels of integration within a series
Wireless Technology	H = High frequency
Optional: Revision	A = Device revision
Optional: Temperature Range	S = 0°C to 50°C C = 0°C to 70°C I = –40°C to 85°C T = –40°C to 105°C
Packaging	http://www.ti.com/packaging
Optional: Tape and Reel	T = Small reel R = Large reel No markings = Tube or tray
Optional: Additional Features	-EP = Enhanced product (–40°C to 105°C) -HT = Extreme temperature parts (–55°C to 150°C)

Figure 7-1. Device Nomenclature

7.2 Documentation Support

7.2.1 Related Documentation

The following documents describe the RF430CL331H transponder. Copies of these documents are available on the Internet at www.ti.com.

SLAZ672 ***RF430CL331H Device Erratasheet.*** Describes the known exceptions to the functional specifications for all silicon revisions of the device.

7.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Community
TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

TI Embedded Processors Wiki
Texas Instruments Embedded Processors Wiki. Established to help developers get started with embedded processors from TI and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

7.4 Trademarks

Code Composer Studio, E2E are trademarks of Texas Instruments.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.
Wi-Fi is a registered trademark of Wi-Fi Alliance.

7.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.6 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

7.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
RF430CL331HIPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL331H	Samples
RF430CL331HIRGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL331H	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

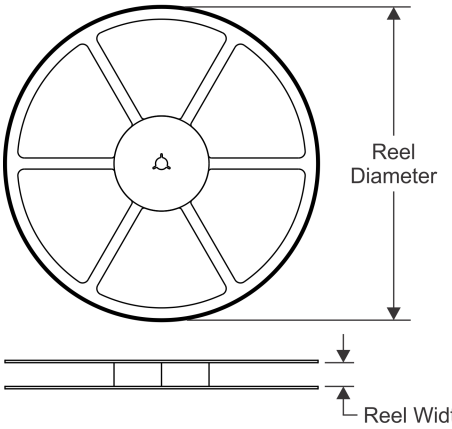
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

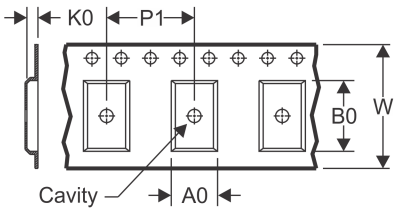
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

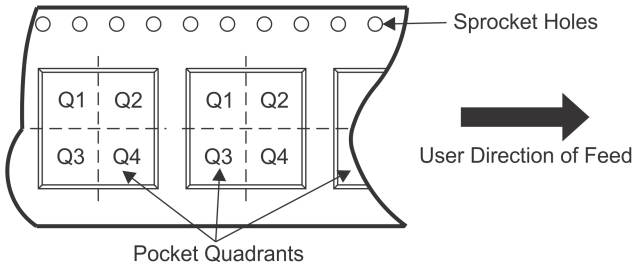


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

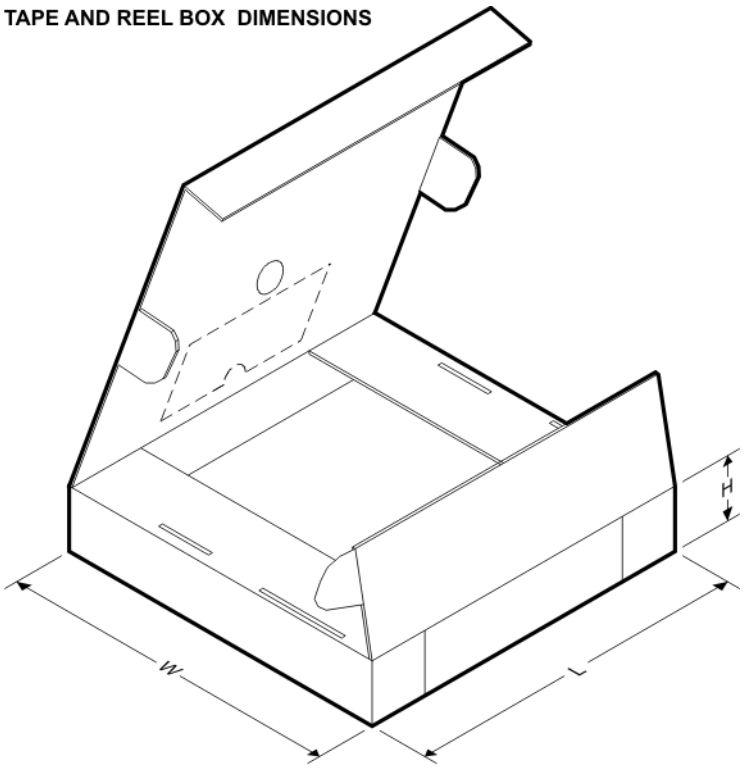
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
RF430CL331HIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
RF430CL331HIRGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

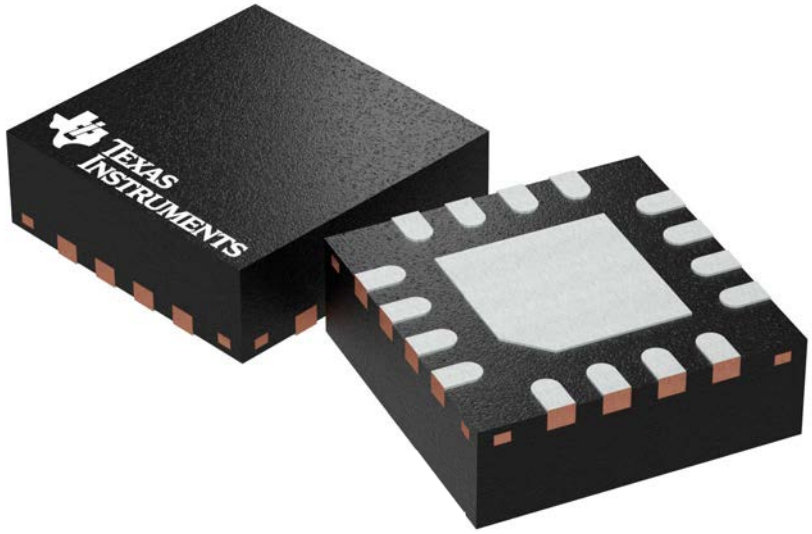


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
RF430CL331HIPWR	TSSOP	PW	14	2000	338.1	338.1	20.6
RF430CL331HIRGTR	VQFN	RGT	16	3000	350.0	350.0	43.0

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



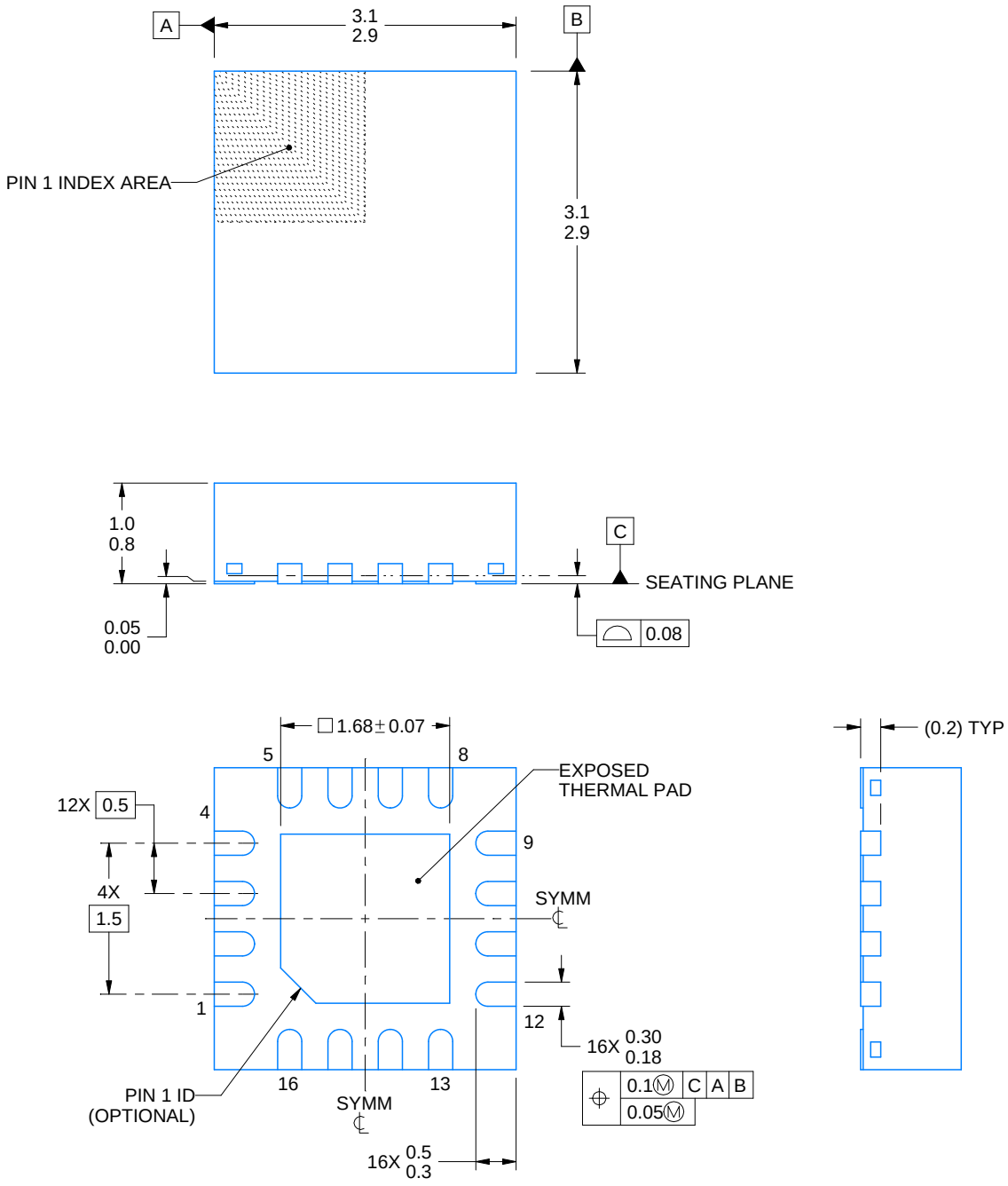
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RGT0016C

PACKAGE OUTLINE

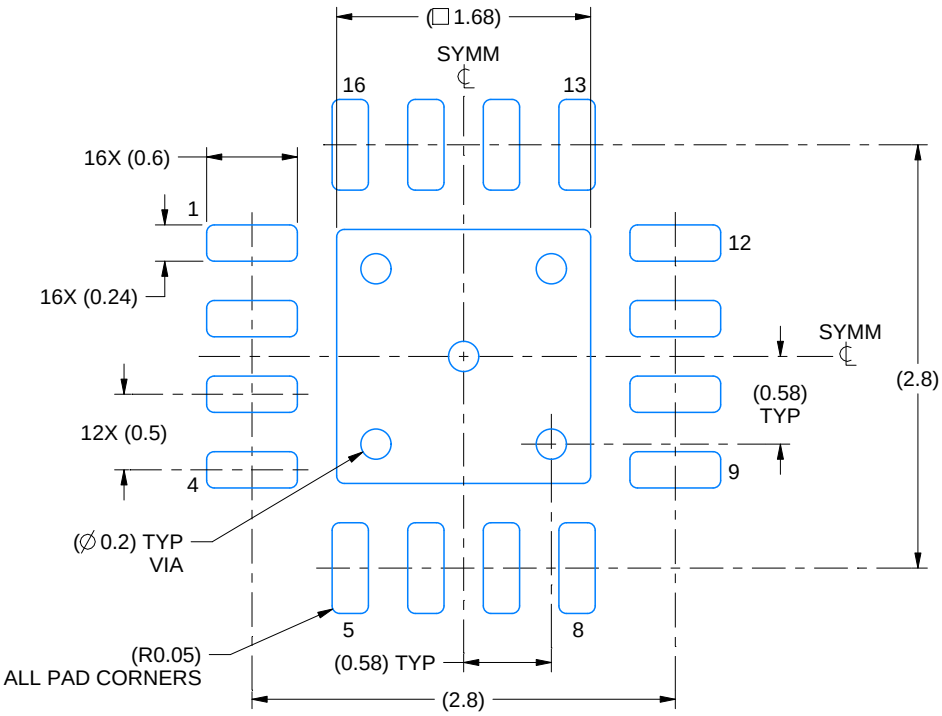
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

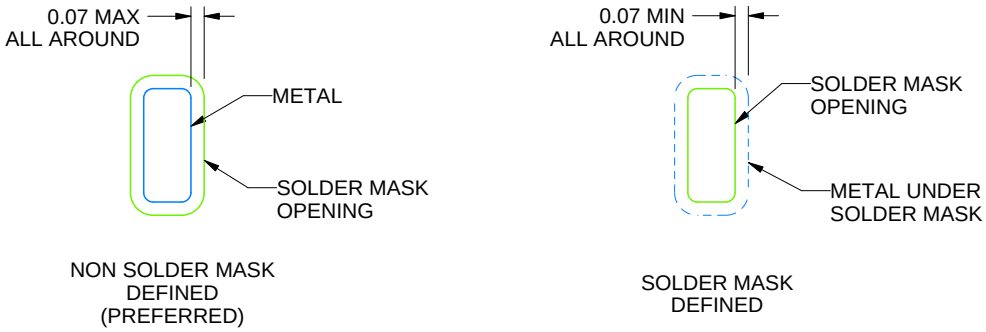


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

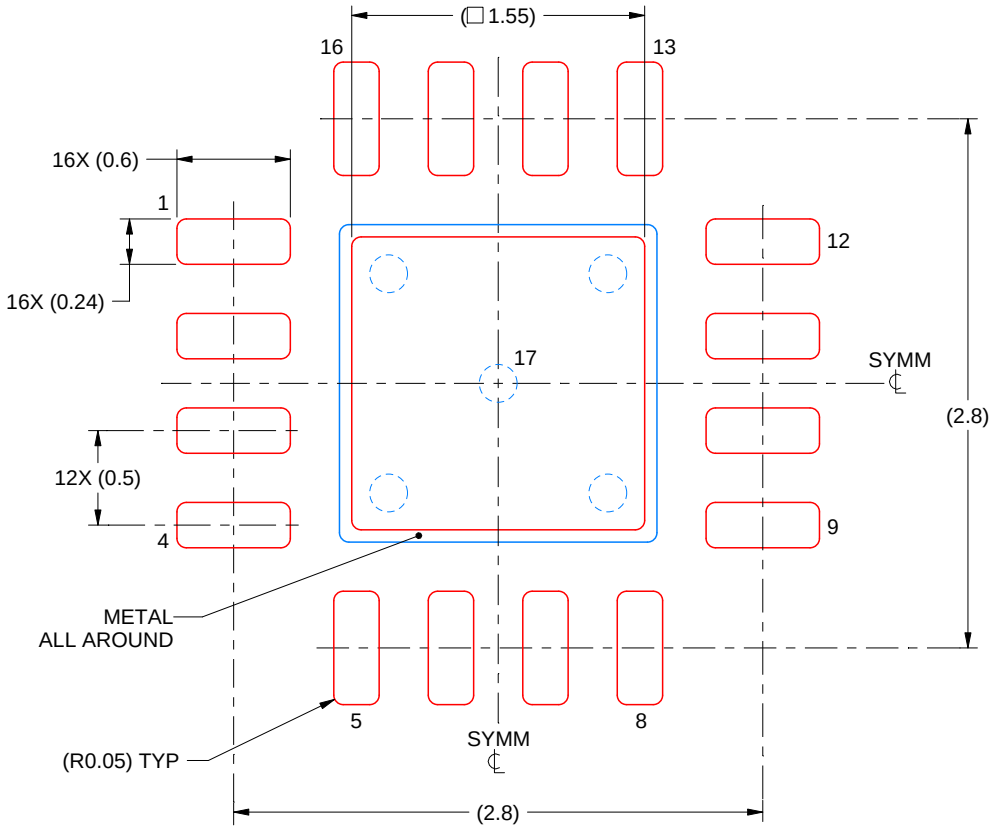


SOLDER MASK DETAILS

4222419/C 04/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

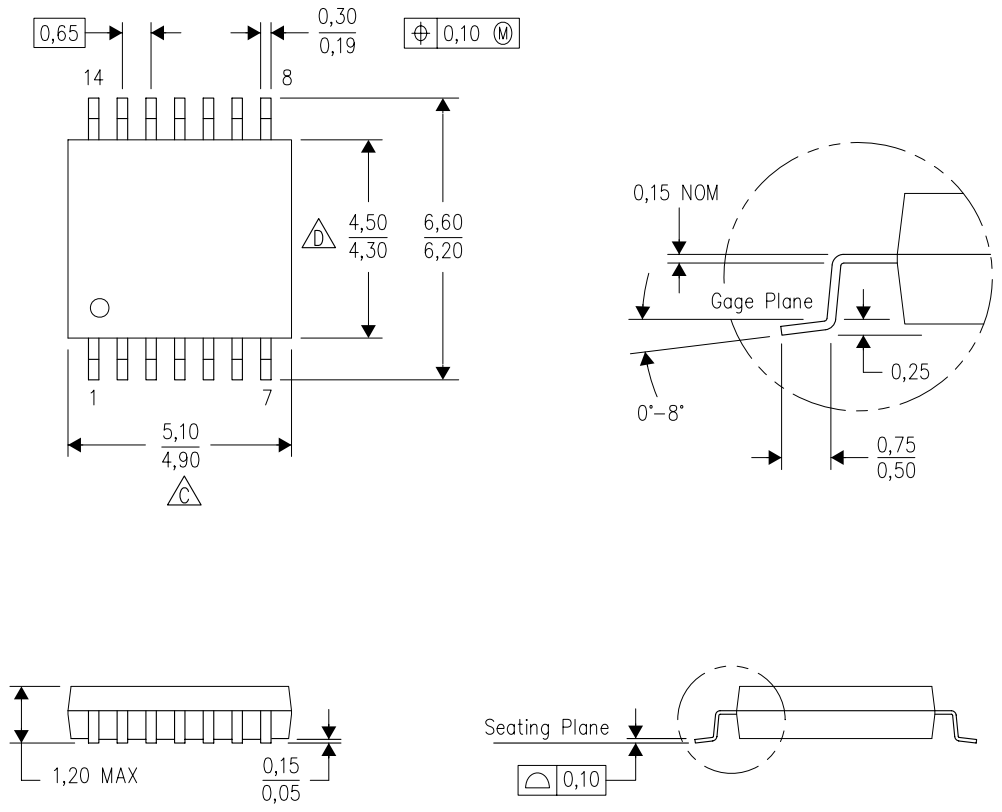
EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222419/C 04/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

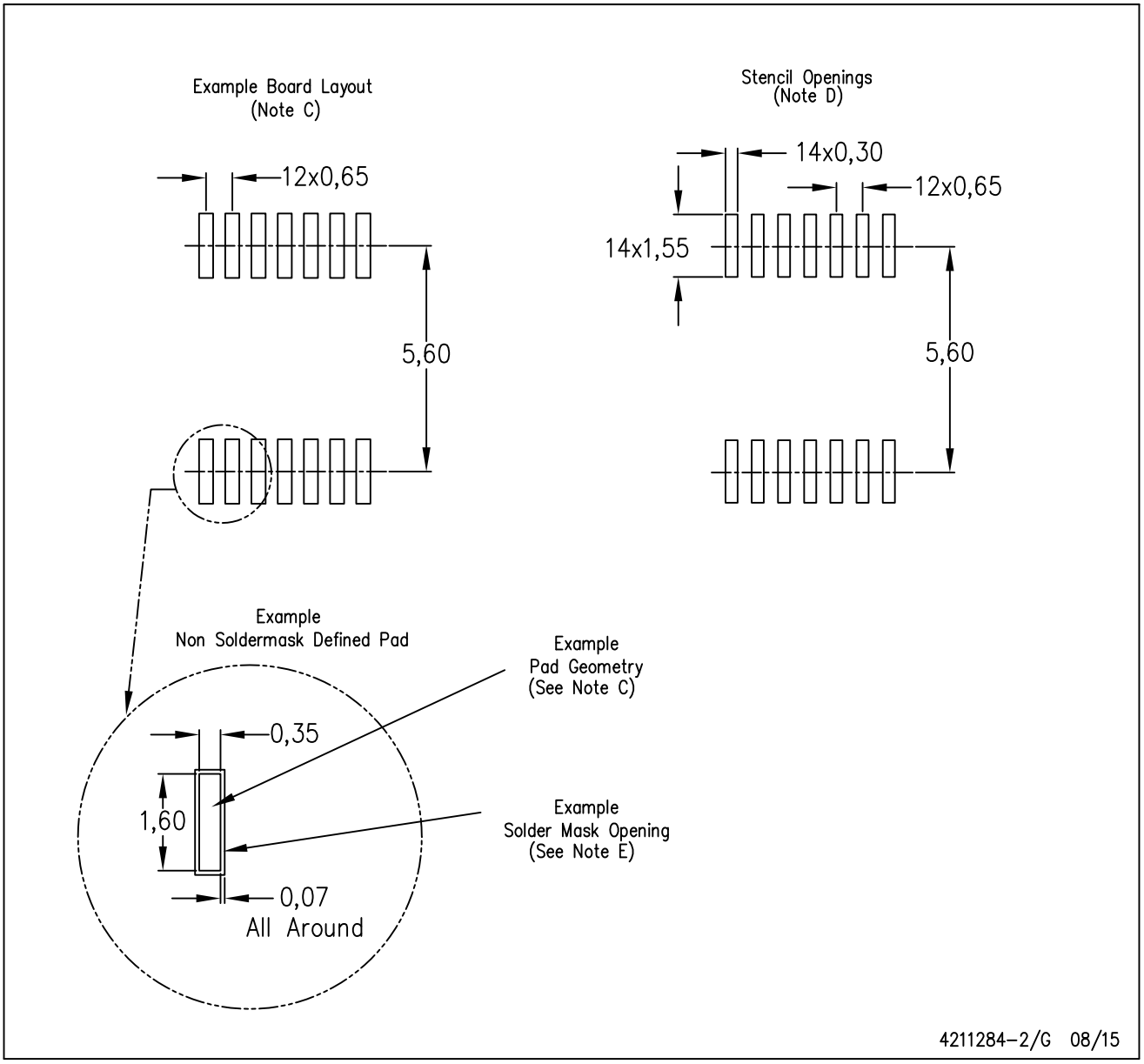
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265