General Description

The packages with solder balls from ESPROS Photonics are Wafer-Level Chip-Scale Packages (WL-CSP) for use in standard SMT assembly lines with standard SMT processes and equipment. Due to the very thin and space saving silicon chip substrate, the assembly process needs specific attention. The chips are quite brittle and need careful handling. However, by following the guidelines described herein, high yield production and high reliability products can be achieved.

Please note that this information was prepared on certain equipment, with certain PCB base material and consumables under certain conditions. It is in the responsibility of the assembler / process owner to develop and qualify his own process and process parameters and materials to achieve the best results.

Industry experience has shown that ESPROS' WL-CSP packages are fully SMT compatible. Assembly and underfill can be achieved by standard tools and processes. Stable processes will return industry standard quality and yield results. If not otherwise stated in this application note, general rules and requirements for SMT assembly need to be observed.

Features

- PCB layout advice
- Substrate material selection
- Equipment considerations
- SMT assembly process recommendations
- Underfill processing
- Cleaning
- Inspection

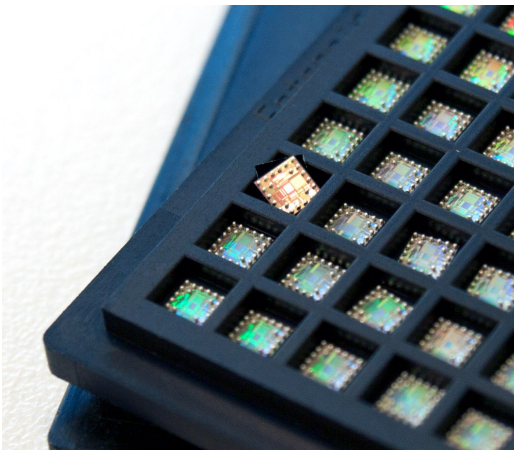

Figure 1: epc611 WL-CSP
Chip size 2.65 x 2.65mm

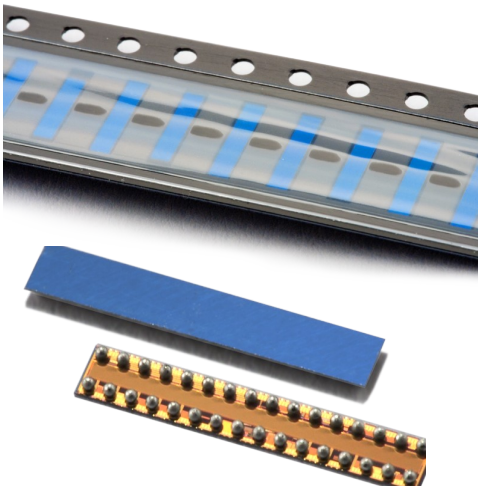

Figure 2: epc901 with CSP32 package
Note the high aspect ratio of 8.0 x 1.3mm

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1. Process flow

The assembly shall follow standard SMT assembly processes like

- Drying of the substrate material
- Printing of solder paste on a PCB
- Component placement using pick-and-place equipment
- Soldering by applying a reflow soldering process
- Cleaning
- Underfill application and curing
- Inspection

2. Recommended PCB design guidelines

Good assembly and reliability results can be achieved only by applying an appropriate PCB layout. The pad and the solder mask designs are especially important. If the given advice is not applied, pad lift-off and other assembly defects can occur. Refer as well to the product datasheets where product-specific layout information is provided.

2.1. SMT footprint design

For the PCB fabrication, the following two types of PCB pads/land patterns referred in 3 are used for surface mount assembly:

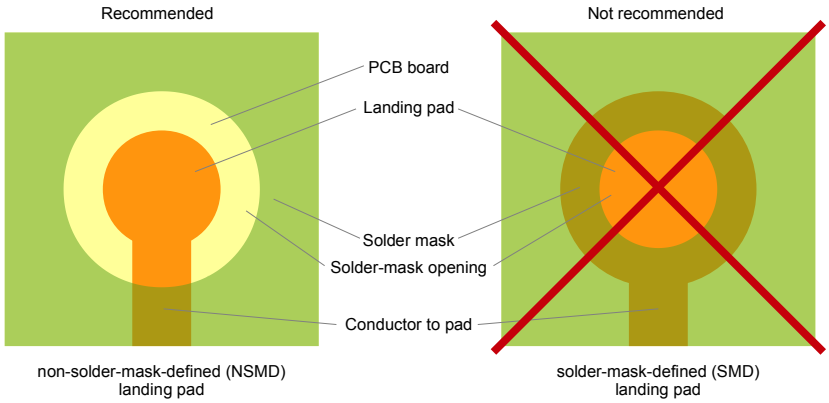


Figure 3: Basic footprint designs

- **Recommended**: Non-solder mask defined
  The metal pad on the PCB is smaller than the solder mask opening (left picture in 3).
  We recommend NSMD pads for CSP, because the copper etching process has a better pattern definition than with the solder masking process and therefore improves the reliability of the solder joints.

- **Not recommended**: Solder mask defined
  The solder mask opening is smaller than the metal pad.
  It is not recommended because lower pitches may not work with this layout due to PCB limitations. A misalignment of the solder mask can cause defects like pad lift-off or openings.

The design of the landing pads has to follow the recommendations for trace, space and solder mask capabilities of the PCB manufacturer. The recommended pad geometry in 1 is for the use of fine-line PCB boards:

Dimension	Ref.	Fine-line PCB
Pad pitch		450µm *
Pad diameter	A	max. 300µm
Line width	B	min. 150µm **
Ratio track to landing pad	B / A	max. 50%
Space track to line		min. 150µm **
Space track to solder mask	C	100µm **

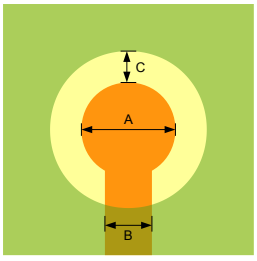


Table 1: Recommended PCB design guidelines e.g. epc300

Notes: * Dimensions defined by chip
** Dimensions defined by PCB design rules

The designer has to take care about the wettable area between the track which is not covered by the solder mask and the landing pad in order to reduce solder drain as much as possible. The trace width at the connection to the landing pad should be as small as possible and must not exceed 50% of the pad diameter. The distance from the solder mask to the landing pad needs to be as small as possible.

The solder mask accuracy and alignment capability of the board manufacturer should be considered first to ensure that the solder mask opening is max. 100 µm larger than the pad on either side.

The fan-out of the tracks should be symmetrical and balanced across both the x and y directions to avoid part rotation and offset forces due to surface tension of the tin during soldering (refer to 4).

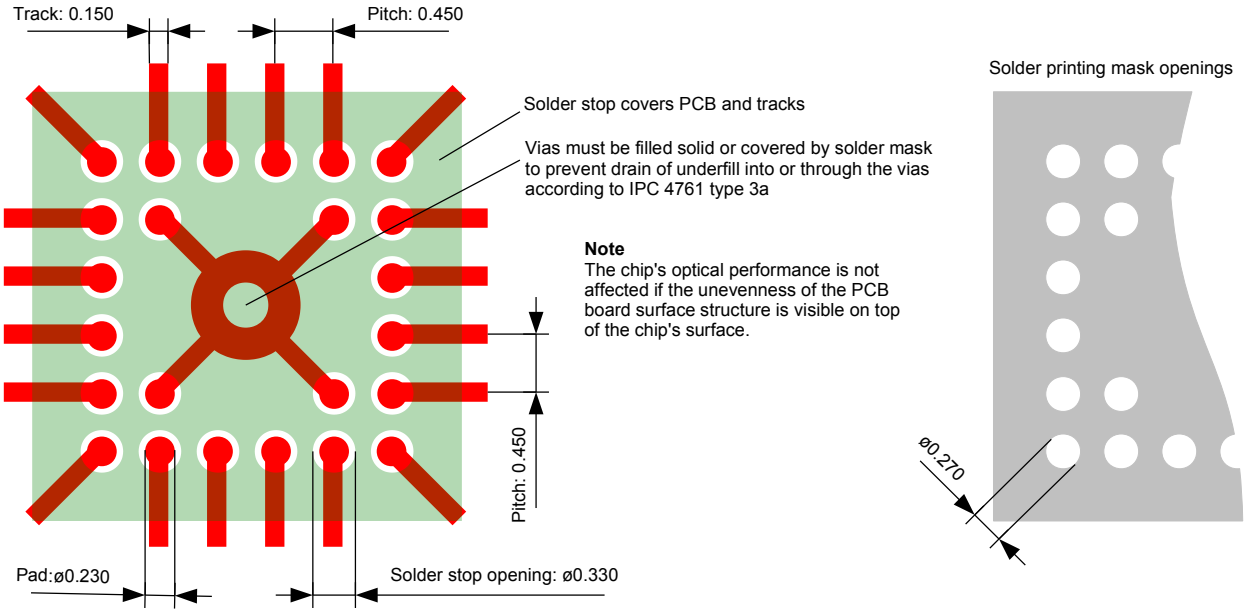


Figure 4: Example 1 of a recommended, balanced fine-line PCB design for epc611 with a “closed” center via of the GND pads (dimensions in mm)

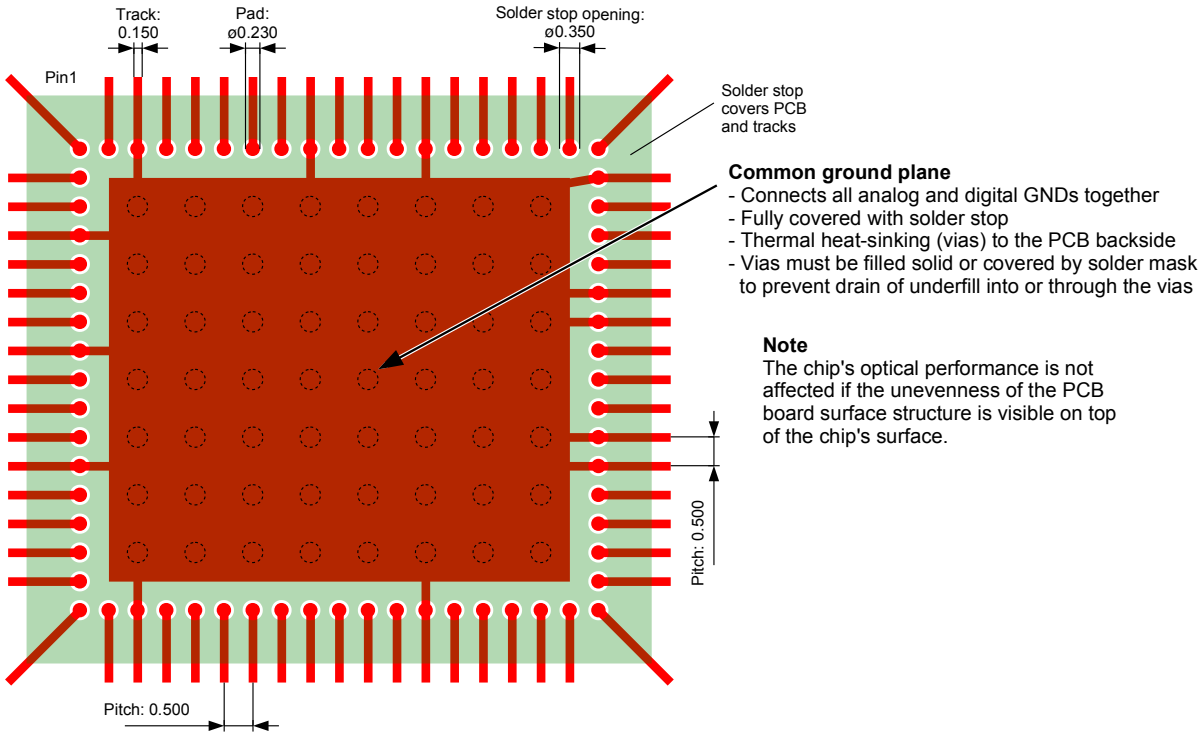


Figure 5: Example 2 of a recommended, balanced fine-line PCB design for epc660 with thermal heat-sink (dimensions in mm)

IMPORTANT:

1. Reference PCB designs
   Reference PCB designs and footprints in the datasheets of the chips are always based on latest practice experience for the individual part and can be more comprehensive than the examples herein. ESPROS suggest to use designs according these proposals.
2. Pull-back of components next to the chip
   Refer to Chapter 6 for free distance between TOF chip and other components next to, assembled on the same PCB side.

All advises in this application note shall help the PCB board designer and assembly responsible having a better understanding of the principle of the way to reliably assemble modules with very thin, 50µm thickness, and brittle wafer level chip scale packages (WL CSP).

2.2. PCB material

ESPROS chips can be assembled on standard epoxy-glass substrates. However, High-Tg FR-4 substrate provides much higher reliability over standard FR-4 material due to a lower thermal expansion coefficient (CTE-z). A copper layer thickness of 35µm (1 oz) or less is necessary to achieve the required patterning definition. A higher copper thickness results in lower pad accuracy.

Via-in-pad is not recommended to prevent voiding of the solder joint due to uneven planarity of the pad.

The final layer on the metal pad has a significant effect on assembly yield and reliability. Organic surface preservative (OSP), immersion tin, or electroless nickel/immersion gold with gold thickness limited to <0.2 µm are the most appropriate finishes. HASL (Hot Air Solder Leveled) board finish is not recommended.

3. Stencil printing

The pad diameter of ESPROS' WL-CSP packages is typically 200 - 300µm. This should not pose any fundamental problems to modern SMD assembly. However, proper application of the solder paste is the baseline for a stable assembly process and both stencil printing equipment as well as the choice of soldering paste are major criteria. The following parameters have demonstrated good results and may therefore be referred to as a guideline.

3.1. Equipment and tools

A fully automatic inline stencil printer shall be used for this process:

Process positioning accuracy:	± 20µm, 6σ
Stencil cleaning:	Vacuum cleaning
Cleaning cycle:	After each print by wet/vacuum/dry
Alignment:	With vision system using 2-3 markers

Print verification by a 2.5D vision system is highly recommended for high yield results. Experience shows that the process can be stabilized without the requirement of a 100% vision inspection.

3.2. Solder paste

Solder paste type is a key factor for stable assembly results. Solder paste Senju M705-RGS800HF has proven good and stable results (www.senju-m.co.jp):

Type:	SAC305 (96.5Sn/3.0Ag,0.5Cu), Type 5
Solder flux class:	No-Clean; ROL0

3.3. Stencil

Thickness:	100µm
Surface:	Electrolytic polishing (nickel, gives enhanced dissolving behavior and longterm stability)
Opening:	Pad diameter 270 .. 300µm, according to ESPROS product datasheet.
	(Stencil aperture circumferentially reduced by 5-10%)

4. Pick-and-place processing

4.1. Moisture sensitivity level (MSL)

There is no need of die preparation, e.g. baking prior to SMD assembly, because ESPROS' bare silicon dies are not moisture sensitive. This is due to the fact that there is no organic material in the packages.

Since there is no organic material in our packages, MSL classification cannot be applied. It’s more like a hermetic package which cannot collect and prevent water vapor inside the package. That’s better than the best MSL class.

However, we recommend the following:

- Store the parts inside the unopened, sealed plastic bag. The bag contains Nitrogen (N) which keeps humidity away. Humidity can lead to corrosion and oxidation of the solder balls.
- If a bag is opened, store the parts in a Nitrogen atmosphere to avoid corrosion or oxidation of the solder balls.
- No baking of the parts is needed.
- Make sure, the PCB is baked out before the assembly process to avoid popcorn effects.

4.2. Machine capability and requirements

The pick-and-place machine should have a repeatability and accuracy capable of placing 0402 components or better. Standard feeders for tape and reel can be used.

Vision alignment should be used to place the components. The alignment can be done on the part edges. It is typically not necessary to make the alignment based on the solder balls.

We strongly recommend to use a vision system which is capable to identify pin 1, according to the data sheet.

Placing by the use of standard fiducials on the panel works well. Local fiducials are not necessarily required. ESPROS' CSP devices with solder bumps self-align when placed, even with a (small) offset, due to the self-centering nature of the tin-alloy solder balls.

Attention should be taken to z-height placement to insure that the solder balls or the chips are not damaged (compressed) during picking and placement. The placement force should be kept to ≤ 0.8N to slightly press the balls into the solder paste.

4.3. Picking and placement parameters

Picking and placement parameters have to be well controlled due to the chip thickness of 50µm. High stress during pick or place, especially in the z-axis, may lead to chipping of the thin dies. The following specifications of the pick-and-place tool was used in the verification of this assembly process, refer to 7:

Placement accuracy x/y:	Min. ± 50µm 4σ (for pad size 0.3mm)	
Theta accuracy:	± 0.05°	
Maximum vertical force F_Z per chip:	Conventional CMOS chip e.g. epc13x:	≤ 1.5N
	50µm thick photosensitive chip e.g. epc611, epc901, … :	≤ 0.8 N preferred
	Preferred is forceless picking and placing with vacuum only.	
Maximum shear force F_{SH_B} per ball:	≤ 25gf in any direction	

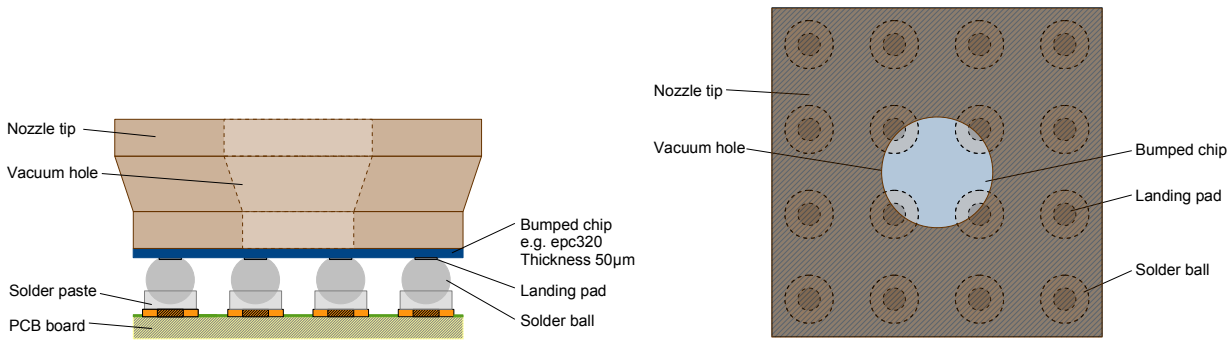
It is very important that the picking process lifts the chip from the tape high enough in the vertical direction in order to avoid any collision between the solder balls underneath the chip and the tape cavity boundaries. A collision may lead to lost solder balls during the assembly process.

Special care should also be taken to achieve a stable and continuous tape feeding process. Jerking during the feeding motion may lead to chip displacement in the tape cavity which may impede proper picking.

It is also highly recommended to use a „kiss-and-goodbye“ concept to place the component. It means that the nozzle should not touch the part to the solder paste but rather blow it away at close distance when it does the placing.

4.4. Nozzle

To minimize mechanical damage possibilities, the pick-up tool must have a compliant tip. Standard nozzles adapted to the chip geometry will easily pick up the part. Recommended is a plastic or ceramic tip with a contact area equal to the chip size, refer to 6.



side view of the tip

top view of chip - minimum contact area of the tip

Figure 6: Pick-and-place tool for epc320

The nozzle

- shall have a flat surface with better than 10µm flatness
- surface roughness shall be better than 100nm (polished)
- pickup area must not touch the pixel-field area
- should not have any flashes.
- must have the same size as the chip, maximal contact area on the chip. Refer to 7.
- Take care using not a too strong vacuum. It can lead to bending effects of the chip or to not correct picking the chip.

The chip can get damaged if the above guidelines are not followed! With tooling designated as “use only for optical devices” you can keep the surfaces clean and prevent any damage to the very sensitive surfaces of photosensitive parts.

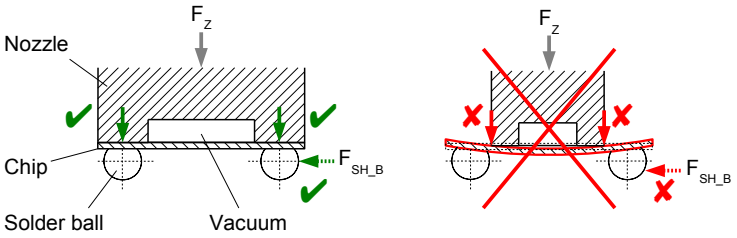


Figure 7: Pick-and-place; left: good nozzle, good picking; right: bad nozzle, bad picking

In order to reduce stress on the chip, it is advised that the nozzle has maximal contact area on the chip. The nozzle has to bring the F_Z force evenly distributed vertically to the center of the solder balls during picking and placing. Refer to 7, left picture. It means that it should be large enough so that it picks the chip not just in the middle of the part but also in the area above the solder balls.

Bending of the chip is not allowed, nor caused by picking or placing forces nor by the vacuum of the nozzle. Refer to 7, right picture.

Keep attention to have no shear forces on the solder balls during picking the chip from the tape pocket and/or placing. Do touch with the chip nor the pocket walls nor anywhere.

5. Soldering

ESPROS' CSP devices are compatible with industry standard reflow process for both lead-free (RoHS) and Sn/Pb eutectic solder compositions to form solder joint interconnections.

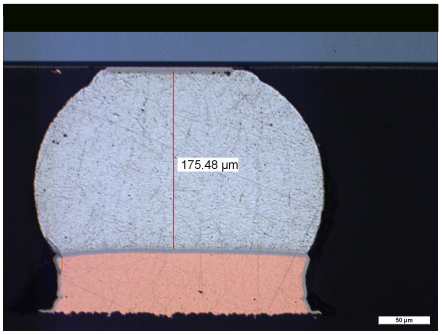


Figure 8: Cross section of a solder ball (epc611 on top of a fine-line PCB)

Once soldered, the chip remains fragile and should be protected against mechanical contact. The chips may get damaged if PCB's are dropped or exposed to high acceleration before the underfill is applied.

Soldering is done by reflow process following the J-STD-020 standard. Optimization parameters by the respective solder paste manufacturer should be observed. The temperature gradient of the reflow process should be kept as low as possible and should not exceed the values stated in 2 to prevent possible bending of the PCB.

Qualified reflow operations is:

Item	Description
Solder ball alloy	typically Sn96.5Ag3.0Cu0.5 (SAC305), refer to the ESPROS datasheet
Soldering profile	follow the recommendations of IPC/JEDEC J-STD020C (revision C and later) for lead-free assembly
Soldering peak temperature	240ºC with 60s time above liquid (T_{AL}). **Important Note:** The chip itself can withhold higher temperature. However the maximum peak temperature for the solder paste we recommend is 255°C. Furthermore the mismatch in thermal expansion of the chip and PCB gets more significant the higher the temperature and can lead to bad chip soldering or at some point even chip breakage.
Temperature gradients	Heating up: max. +2.5 ºC/s; cooling down: max. 6 ºC/s
Soldering in protection air	Nitrogen purge during solder process (recommended)

Table 2: Soldering

6. Underfill

In order to achieve JEDEC temperature cycle requirements, underfill is a must to reduce thermal and mechanical fatigue as well as to increase longterm reliability.

Applying underfill under the CSP components reduces stress to the solder pads caused by e.g. temperature cycling or mechanical bending of the PCB. The thermal and mechanical fatigue will be reduced and the longterm reliability will be increased. Underfill process and product (type) is application specific. It shall follow JEDEC-STD JEP150: Stress-test-driven qualification of and failure mechanisms associated with assembled solid state surface mount components.

In order to avoid mechanical damage, a jet dispenser is preferred for the underfill application. The process was verified with an inline tool that meets a placing accuracy of ± 50um @ 6σ.

A suitable underfill product is to be chosen with respect to the specific customer requirements. Factors like pot/shelf life, curing process ramp and time are to be considered.

The following key specifications may be used as a reference:

Chip model	**Chip size**	**Underfill**	**Manufacturer**	**Viscosity**	**Pot life**	**Process temperature**	**Curing ramp _/‾_**			**Comments**
	[mm]	Type		[cPs]	[h]	[ºC]	ramp-up	dwell	ramp-dow	
epc200 epc3xx epc611 epc660 epc635 epc901	1.8 x 1.8 various 2.8 x 2.8 9.7 x 8.7 6.3 x 4.2 8.0 x 1.4	Loctite Eccobond FP4531	Henkel	10'000	24	60 - 90	80ºC → 120ºC, gradient: 2.5ºC/min	120ºC for 40min	120ºC → t_a, gradient: 0.8ºC/min	Automotive applications (high reliability)
		XSUF 1594-1	Namics	700	24	20 - 60	t_a → 120ºC, gradient: 2.5ºC/min	120ºC for 1h	120ºC → t_a, gradient: 0.8ºC/min	Re-workable underfill
epc200 epc611	1.8 x 1.8 2.8 x 2.8	Epotek 353 ND	Epoxy Technology	3'000 - 5'000	3	80	80ºC → 100ºC, gradient: 10ºC/min	100ºC for 30min	100ºC → t_a, gradient: 0.6ºC/min	
		Epicol 33	APM Technica	300 - 600	6	20 - 24	t_a → 90ºC, gradient: 1ºC/min	90ºC for 60min	90ºC → t_a, gradient: 1ºC/min	

Table 3: Overview underfill application

Important notes:

1) Curing has to take place directly after dispensing the underfill. Keep retention time as short as possible.
2) Process temperature: Component and PCB board shall have this temperature during underfill process. The underfill has ambient temperature and gets fluid during application.
3) Never exceed the maximum rated temperature.
4) Dispensing tools: Follow strictly the recommendations of the underfill manufacturer, e.g. for Namics XSUF 1594-1: Use a dispensing needle with gauge 18 - 23 (ID 0.33 – 0.84 mm).
5) No open vias in the underfill area. Refer to 4 and 5.

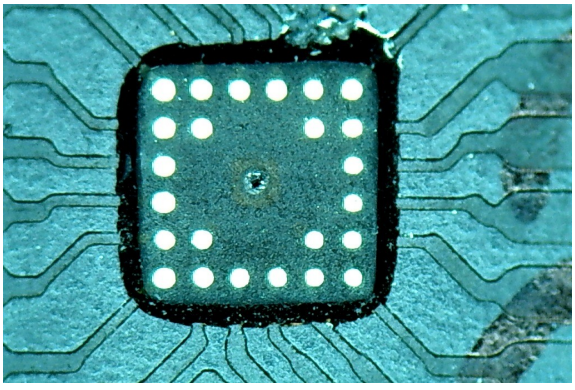


Figure 9: Well done underfilling. Underfill evenly distributed underneath of the chip (view of PCB with chip removed)

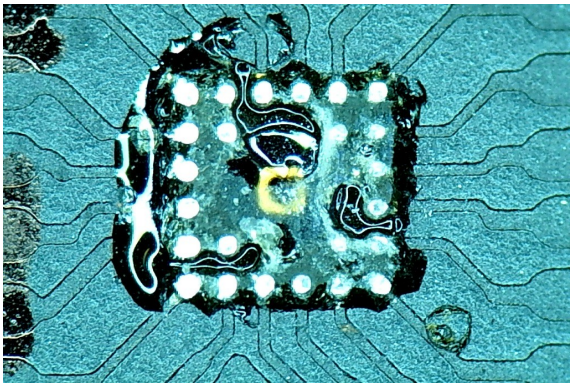


Figure 10: Failed underfilling. Underfill does not cover underneath full chip area (view of PCB with chip removed)

6.1. PCB design for covering assembly and underfill needs

The proposed footprints for chips e.g. in Chapter 2.1 cover mainly the assembly needs for the chips themselves. Rules for surrounding the chip, on the same PCB side, with other components depends strongly from the available assembly processes and machines as well as of the used tooling for the underfill process. The user has to adjust the necessary pull-backs of these components according to the manufacturing line recommendations.

Here a general example which shows a way to treat this:

1. The, by the underfill manufacturer recommended, dispensing needle in this example shall have an exterior diameter of 0.65mm.
2. During the underfill process, the assembler should not go with the needle too close to e.g. the epc660 chip. It is due to the risk of touching, damaging the chip or prevent of flowing of underfill onto chip's top surface.
3. On the other hand, too far is also not good otherwise the underfill does not flow perfectly under the chip.
4. Thereof, a good approach for the design can be:
   - Keep clear a gap of minimum 1.5 mm between chip and components on 1 or 2 sides for I- or L-type underfill dispensing, respectively.
   - All other sides can have a free minimum distance of 1 mm.
   - Around all 4 corners reserve free a radius of 1.5mm.
   - U-type underfill dispensing is not recommended.

7. Testing and de-paneling of modules

Electrical testing and de-paneling of modules (separation, singularization) with WL CSP chips assembled and under-filled follow the same rules as necessary e.g. for large ceramic multilayer capacitors. Under-filled chips are quite robust but still, handle the circuits with the necessary care to prevent of mechanical damaging of the chips e.g. by bending to break solder ball interconnects on chip side.

The forces to probe, mill or cut the modules shall not stress e.g. vibrations or bend the PCB boards. We do not suggest to depanel modules by punching. For very thin PCB carriers, we propose to separate the PCBs before assembly and use during the assembly, soldering and testing process multi-module carrier frames instead of processing them in full panels.

IMPORTANT:
ESPROS dissuades from testing and de-paneling of panels or modules with not under-filled chips due to the risk of yield loss or long-term aging effects caused by applied mechanical stress to the chip.

8. Process and environment cleanliness

The ESPROS WL-CSP products are imagers or photo-electric chips which convert light into electric charge. The photosensitive area is on the top of the chip which is called the optical window. If there is dirt on this surface, the optical properties of the imager can be negatively affected. Therefore, the processes to assemble the chips including the application of underfill and further processing of the assembled PCB's should be done under cleanroom conditions matching the final optical requirements.

9. Cleaning

No cleaning is necessary if solder paste with no-clean flux is used. Otherwise the cleaning step depends on type of flux used. The approved component surface cleaning agent is Isopropanol or the like.

10. Inspection

Regular process quality inspections, e.g. per lot, are suggested. Voids, oxide and solder failures can be detected easily by cross-sections of the bumps.

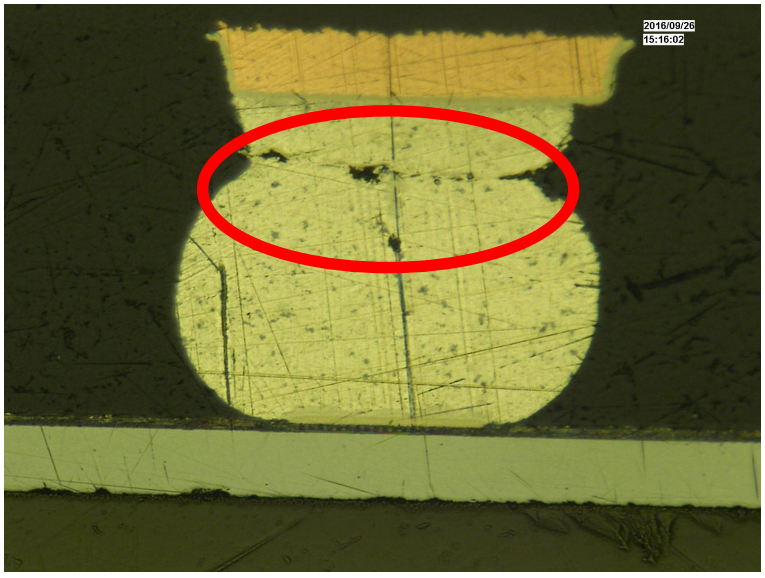


Figure 11: Lost contact due to a head-in-pillow (snowman) defect during soldering (cross section of the solder ball)

11. Rework

Replacement of the component prior to the start of underfilling is possible using appropriate standard rework equipment.

12. Storage of components

The following procedures shall apply for the (long term) storage, unless otherwise specified:

- ESPROS' CSP devices are not moisture sensitive (JEDEC J-STD-020). They do not need baking before mounting. In case of a necessary bake, components in tape on reel may not be baked at any temperature > 40º C. Do not apply more than one bake cycle.
- Preferred storage is on reel in a hermetic sealing which covers the components from mechanical damaging, dust, foreign particles or pollution (JEDEC J-STD-033 and EIA-583).
- Components should be stored (resealed) in dry environment to reduce to a minimum the oxidation of solder or solder balls (10% RH, clean dry air bagging or vacuum bagging as a minimum). See also next item.
- Components should be stored (resealed) in a non-oxidizing atmosphere to reduce to a minimum the oxidation of solder or solder balls. Storage in nitrogen atmosphere is suggested.
- Storage temperature should be in the range of 18 ... 24º C for products not in process or transit.
- The sealing/packaging material should be either conductive or antistatic. The electrostatic discharge sensitive (ESD) protection should be compliant with JESD625 and EIA 541.
- Products should be used based upon the first-in, first-out (FIFO) inventory method.

13. Checklist questions

If significant yield losses occur, the following checks may help to identify the root cause of the problem.

Problem	Root cause	Solution
Are cracks or other mechanical defects visible on the chip?	■ Pick-and-place has inappropriate z movement-forces ■ The PCB mechanically stressed during assembly or operation ■ PCB separation from panel (de-panelization) may induce mechanical stress, typically bending to the PCB	■ Refer to section 4 Pick-and-place processing ■ Use a de-panelization tool with zero-force to the PCB, e.g. laser cutting
Are head-in-pillow defects visible?	■ Pad geometry not appropriate ■ Does the layout correspond to the recommendation? Especially critical is the solder-stop mask. ■ Solder paste printing process not stable, not properly cleaned stencil mask ■ Use appropriate type of solder-paste	■ Refer to section 2.1 SMT footprint design ■ Refer to 3 Stencil printing ■ Refer to 5 Soldering
Reliability qualifications fails with contact opening or mechanical damage of the chip	■ No underfill used ■ Wrong underfill used ■ Shelf time and curing process inappropriate ■ Curing has not taken place immediately after application of the underfill ■ The underfill is not cured ■ Temperature profile for curing the underfill is not appropriate ■ Curing temperature is too high	■ Refer to 6 Underfill

14. Process Support

In order to support our customers in case of assembly and/or reliability issues, the following information shall be provided:

- Cross-sections pictures
- ESPROS lot number
- Delivery date of product

15. Summary

Industry experience has shown that ESPROS' WL-CSP packages are fully SMT compatible. Assembly and underfill can be achieved by standard tools and processes. Stable processes will return industry standard quality and yield results. If not otherwise stated in this application note, general rules and requirements for SMT assembly need to be observed.

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