Description

The DIODES AP43771V is a highly integrated USB Type-C® power delivery controller targeted for USB Type-C adapter and charger application. It is compatible with Qualcomm® QC4/4+/QC5 protocol, which supports USB power delivery specification Rev3.0 V1.2 (including optional PPS support).

The AP43771V can support PPS APDO (Augmented Power Data Object) with 20mV/step voltage resolution and 50mA/step current resolution for power management. Also embedded is cable-loss compensation and SOP command for e-Marker detection.

The AP43771V can provide a robust protection scheme with built-in OVP/OCP/SCP/OTP features.

Supporting emerging multiple Type-C PD applications, the AP43771V (W-QFN4040-24 (Type A1)) can be used for implementing smart power sharing scheme. It monitors status of other I2C interface connected ports and leverages the embedded MCU for command execution through I2C interface to re-allocate desired power profile for each Type-C port.

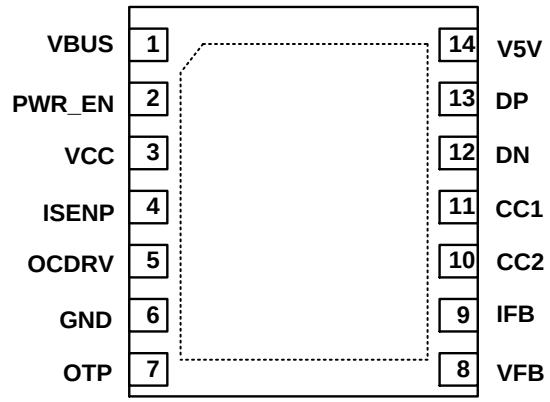
Rich power functions are embedded on the chip to reduce total BOM. A one-time programmable ROM is provided for main firmware, and a multi-time programmable ROM is provided for user configuration data.

Features

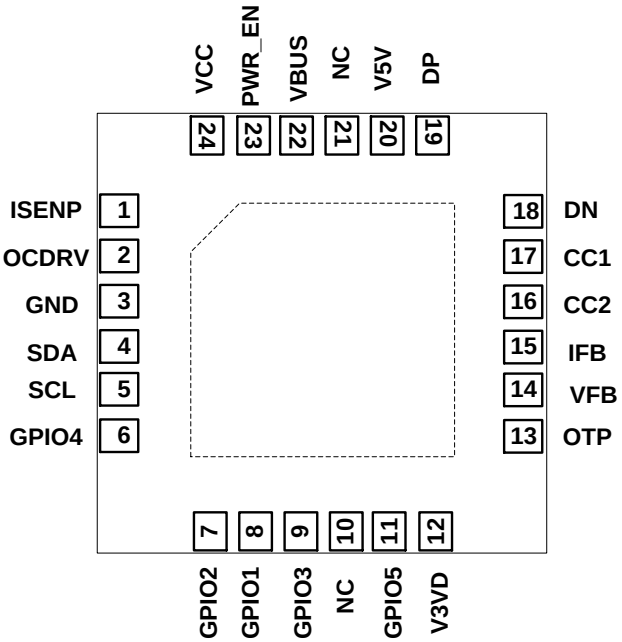
- Compatible with USB PD Rev3.0 V1.2 (TID = 4305)
- Qualcomm QC4/4+/QC5 Protocol Certificated(QC20201127203)
- OTP (One-Time Programmable) for Main Firmware
- MTP (Multi-Time Programmable) for System Configuration
- Built-In Regulator for CV and CC Control
- Support SCP/OTP/OVP/UVP with Auto Restart
- Support Power Saving Mode
- External nMOSFET Control for VBUS Power Delivery
- Support E-Marker Cable Detection
- Support I2C interface (W-QFN4040-24 (Type A1) only)
- Operating Voltage Range: 3.3V to 24V
- Fewest External Component Count
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.**
  https://www.diodes.com/quality/product-definitions/

Pin Assignments

(Top View)



W-DFN3030-14 (Type A1)



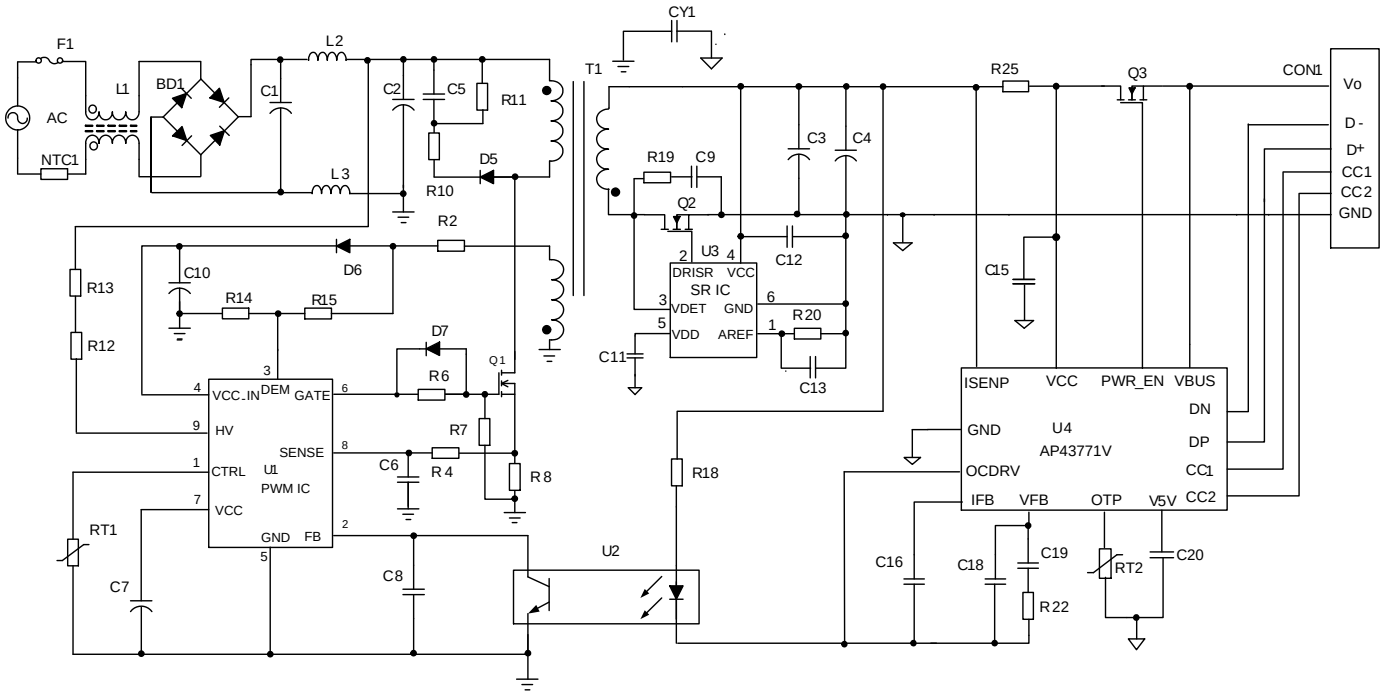
W-QFN4040-24 (Type A1)

Applications

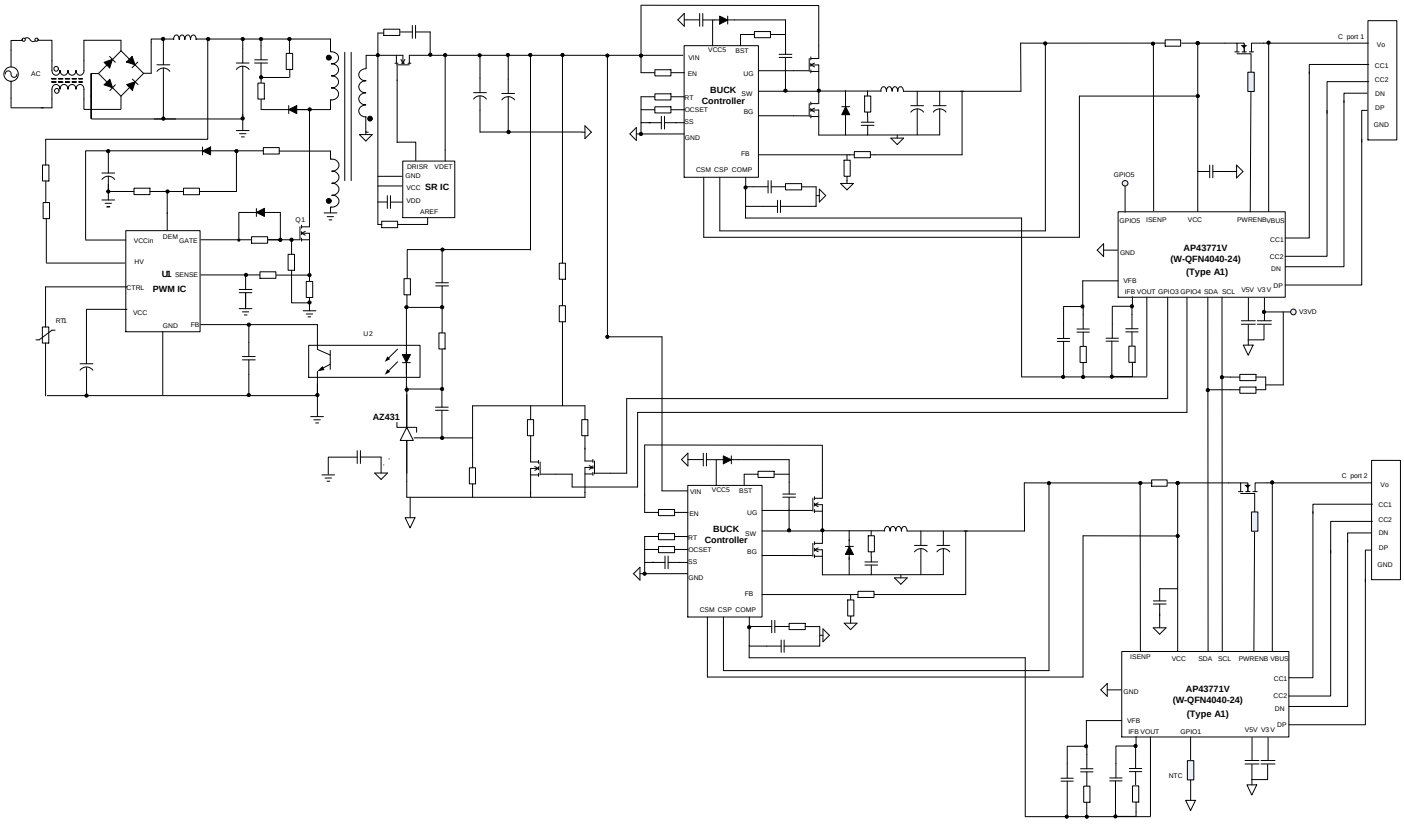
- Type-C USB adapters/chargers
- USB PD converters

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit



Application 1: Traditional Single Type-C Port USB PD Charger Application



Application 2: Dual C-Ports USB PD Charger Application (W-QFN4040-24 (Type A1) Only）

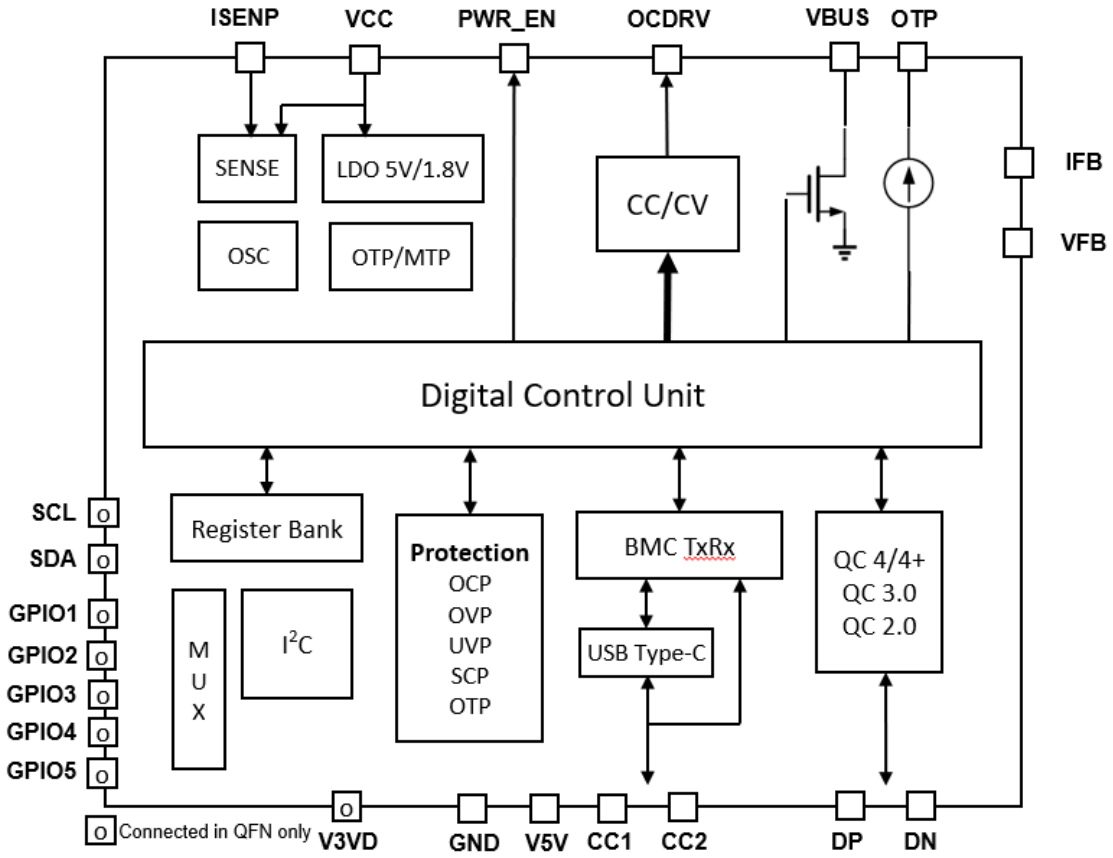
Pin Descriptions (W-DFN3030-14 (Type A1))

Pin Number	Pin Name	Function
1	VBUS	Output Terminal for Discharge Path.
2	PWR_EN	External NMOS Gate Driver. To control external MOS switch, 1: To enable VBUS voltage 0: Disconnect VBUS.
3	VCC	The power supply of the IC, connected to a ceramic capacitor.
4	ISENP	Input Current Sense Positive Node.
5	OCDRV	CC/CV Output. Open Drain Output for Opto-Coupler.
6	GND	Ground
7	OTP	Source current to external NTC sensor for OTP (Overtemperature Protection). Current amplitude is programmable.
8	VFB	CV Input. Negative Node of CV OPAMP for Opto-Coupler.
9	IFB	CC Input. Negative Node of CC OPAMP for Opto-Coupler.
10	CC2	Type-C_CC2
11	CC1	Type-C_CC1
12	DN	Type-C_DN
13	DP	Type-C_DP
14	V5V	LDO-5V Output

Pin Descriptions (W-QFN4040-24 (Type A1))

Pin Number	Pin Name	Function
1	ISENP	Input Current Sense Positive Node.
2	OCDRV	CC/CV Output. Open Drain Output for Opto-Coupler.
3	GND	Ground
4	SDA	GPIO/I2C Data
5	SCL	GPIO/I2C Clock
6	GPIO4	General Purpose Input or Output
7	GPIO2	General Purpose Input or Output
8	GPIO1	General Purpose Input or Output
9	GPIO3	General Purpose Input or Output
10	NC	No Connection
11	GPIO5	General Purpose Input or Output
12	V3VD	LDO-3V Output
13	OTP	Source Current to External NTC Sensor for OTP (Overtemperature Protection). Current amplitude is programmable.
14	VFB	CV Input. Negative Node of CV OPAMP for Opto-Coupler.
15	IFB	CC Input. Negative Node of CC OPAMP for Opto-Coupler.
16	CC2	Type-C_CC2
17	CC1	Type-C_CC1
18	DN	Type-C_DN
19	DP	Type-C_DP
20	V5V	LDO-5V Output
21	NC	No Connection
22	VBUS	Output Terminal for Discharge Path.
23	PWR_EN	External NMOS Gate Driver. To control external MOS switch, 1: To enable VBUS voltage 0: Disconnect VBUS.
24	VCC	The Power Supply of The IC, Connected to A Ceramic Capacitor.

Functional Block Diagram



Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating		Unit
V_{CC}	Input Voltage at VCC Pin	-0.3 to 24		V
V_{FB}, V_{IFB}, V_{OTP}	Input Voltage at VFB, IFB, OTP Pins	-0.3 to 7		V
V_{BUS}, V_{PWR_EN}, V_{ISENP},V_{OCDRV}	Input Voltage at VBUS, PWR_EN, ISENP, OCDRV Pins	-0.3 to 24		V
—	Voltage from PWR_EN to VCC Pin	-16 to 7		V
V_{V5V}	Input Voltage at V5V Pin	-0.3 to 7		V
V_{CC1}, V_{CC2}	Input Voltage at CC1, CC2 Pins	-0.3 to 7		V
V_{DP}, V_{DN}	Input Voltage at DP, DN Pins	-0.3 to 7		V
V_{GPIO1} - V_{GPIO5}, V_{SDA}, V_{SCL}	Input Voltage at GPIO1-5, SDA, SCL Pins (Note 5)	-0.3 to 5		V
T_J	Operating Junction Temperature	-40 to +150		°C
T_{STG}	Storage Temperature	-65 to +150		°C
T_{LEAD}	Lead Temperature (Soldering, 10s)	+300		°C
θ_{JA}	Thermal Resistance (Junction to Ambient) (Note 6)	W-DFN3030-14 (Type A1)	54	°C/W
		W-QFN4040-24 (Type A1)	28	
θ_{JC}	Thermal Resistance (Junction to Case) (Note 6)	W-DFN3030-14 (Type A1)	34	°C/W
		W-QFN4040-24 (Type A1)	16	
—	ESD (Human Body Model) Voltage on DP, DN, Pins	6		kV
—	ESD (Human Body Model) Voltage on VBUS, ISENP, PWR_EN, VCC, OCDRV, OTP, V5V, IFB, VFB, CC1, CC2 Pins	2		kV
—	ESD (Charged Device Model)	750		V

Notes:
4. Stresses greater than those listed under "*Absolute Maximum Ratings*" can cause permanent damage to the device. These are stress ratings only, and Functional operation of the device at these or any other conditions beyond those indicated under "*Recommended Operating Conditions*" is not implied. Exposure to "*Absolute Maximum Ratings*" for extended periods can affect device reliability.
5. When GPIO1-5, SDA, SCL Pins are pulled high to a voltage source, it is strongly recommended to series a resistor with minimum 10k value.
6. Test condition: Device mounted on FR-4 substrate PC board, 2oz copper, with the minimum footprint.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	Power Supply Voltage	3.3	24	V
T_{OP}	Operating Temperature Range	-40	+85	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VCC PIN SECTION						
V_{ST}	Startup Voltage	—	2.5	2.8	3.2	V
V_{UVLO}	Minimum Operating Voltage	—	2.4	2.7	3	V
V_{CC_HYS}	V_{CC} Hysteresis (V_{ST}-V_{UVLO})	—	0.05	—	—	V
$I_{CC\_DEEP\ SLEEP}$	V_{IN} Current in Deep Sleep Mode	CC1/2 Detach after 3s V_{CC} = 5V	—	550	900	μA
I_{CC_OPR}	Operating Supply Current	V_{CC} = 5V	—	3.3	6	mA
VOLTAGE CONTROL LOOP SECTION						
V_{REF_CV5}	Reference Voltage for 5V CV Control	—	4.85	5	5.15	V
V_{REF_CV9}	Reference Voltage for 9V CV Control	—	8.73	9	9.27	V
V_{REF_CV12}	Reference Voltage for 12V CV Control	—	11.64	12	12.36	V
V_{CABLE}	Cable Compensation (Note 7)	—	22	32	42	mV/A
I_{OS}	Maximum OCDRV Pin Sink Current	V_{OUT} = 5V	10	16	30	mA
PROTECTION FUNCTION SECTION						
V_{OVP5V}	OVP_5V Enable Voltage (Note 8)	—	5.6	6	6.8	V
V_{OVP9V}	OVP_9V Enable Voltage (Note 8)	—	9.9	10.8	12.1	V
V_{OVP12V}	OVP_12V Enable Voltage (Note 8)	—	13.2	14.4	16.2	V
$t_{DEBOUNCE\_OVP}$	OVP Debounce Time (Note 10)	—	—	90	—	ms
V_{UVP5V}	UVP_5V Enable Voltage	—	3.3	3.7	4.4	V
V_{UVP9V}	UVP_9V Enable Voltage	—	5.9	6.8	7.7	V
V_{UVP12V}	UVP_12V Enable Voltage	—	7.9	9.1	10	V
I_{OVD}	Overvoltage Discharge Current	V_{CC} = 5V	150	200	250	mA
t_{OCP}	OCP Deglitch Time (Note 9)	—	—	30	—	ms
$t_{RESTART\_INTERVAL\_SCP}$	Restart Interval Time under SCP (Note 9)	—	—	0.8	—	s
T_{OTP}	Internal OTP Temperature (Note 9)	—	—	+140	—	°C
$I_{OTP\_EXTERNAL}$	External OTP Current	—	90	100	110	μA

Notes:
7. Cable compensation voltage can be adjusted by setting from 0 to $V_{CABLE * N}$ (N: 0 to 7).
8. 120% OVP setting & 76% UVP setting.
9. Guaranteed by design.
10. OVP blanking time during V_O transition from high output voltage to low output voltage, such as 9V to 5V, or 12V to 5V.

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.) (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
PROTECTION FUNCTION SECTION						
T_{HYS}	OTP Recovery Hysteresis Temperature (Note 9)	—	—	+25	—	°C
t_{SLEEP}	Enter Sleep Mode Time after Cable Detached (Note 9)	—	—	3	—	s
t_{OV_DELAY}	Delay from OVP Threshold Trip to NMOS Gate Turn-Off (Note 9)	—	—	—	50	μs
t_{UV_DELAY}	Delay from UVP Threshold Trip to NMOS Gate Turn-Off (Note 9)	—	—	30	—	ms
CC1/CC2, DP/DN PIN SECTION						
V_{L_RD3A}	Low Voltage Threshold Used to Distinguish R_D Attached or Detached for 3A Delivery	—	—	1.35	—	V
V_{H_RD3A}	High Voltage Threshold Used to Distinguish R_D Attached or Detached for 3A Delivery	—	—	2.0	—	V
I_{RD3A}	CC1/CC2 Current Source for 3A Advertisement	V_{CC} = 5V	304	330	356	μA
V_{OVP_DN}	DN Line Overvoltage Protection Threshold	—	4.1	4.5	4.8	V
V_{OVP_DP}	DP Line Overvoltage Protection Threshold	—	4.1	4.5	4.8	V

Note: 9. Guaranteed by design.

Performance Characteristics

System Power-On Sequence

Once provided an external power source, the AP43771V will wake up, and the USB PD controller and MCU will initialize. All analog control blocks will be ready and waiting for the PD negotiation process. Meanwhile, the AP43771V monitors the voltage and current conditions to avoid abnormal conditions from happening. Once any unacceptable condition happens, the AP43771V will go into the protection procedure according to the types of abnormal conditions.

Voltage Transition

According to USB PD's protocol, the PD device requests different power profiles, and the AP43771V's power control blocks will change voltage and current values. The AP43771V provides corresponding Overvoltage Protection (OVP), Overcurrent Protection (OCP) scheme, and feedback system stability to guarantee monotonic voltage transition and avoid violating USB PD electrical specification.

The AP43771V provides zero-mismatch voltage methodology that is more flexible for customer system-design requirements. When UFP/DFP makes an acceptable power request deal, the AP43771V will change the VFB pin voltage according to the USB PD command. The voltage regulator control loop regulates the required V_{BUS} voltage according to V_{FB}. In addition, the shunt regulator is built-in to minimize the total external components and cost.

I2C Interface (W-QFN4040-24 (Type A1) Only)

It includes I2C Interface pins (SCL, SDA,) as below table, I2C commands are supported by firmware so that It can monitors and changes status of other I2C devices .

I2C interface pin list

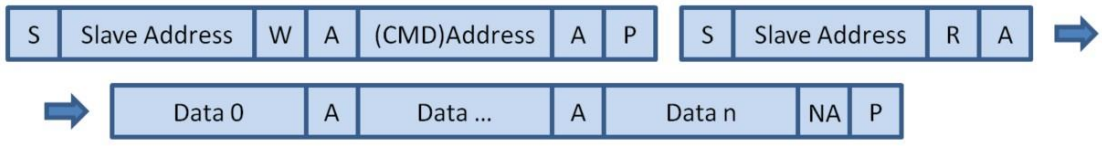
Pin No	Pin Name	Pin Function
4	SDA	I2C Data
5	SCL	I2C Clock

One AP43771V is played as an I2C either master or slave device. The I2C read and write operations are supported as below.

All transactions begin with a START (S) and be terminated by a STOP (P). A START condition is defined whenever a HIGH to LOW transition on the SDA while SCL is HIGH. A STOP condition is defined whenever a LOW to HIGH transition on the SDA while SCL is HIGH. START and STOP conditions are always generated by the master.

I2C Format for Write Data

I2C Format for Read Data



Protection

The AP43771V provides OVP/UVP/OCP/SCP/OTP functions and supports Constant Current (CC) function. All of the protection thresholds depend on the requested power profile, and provide the most reliable protection scheme.

The AP43771V provides OVP feature by turning off the power switch when V_{BUS} is higher than OVP enable voltage. Meanwhile, it provides an internal discharge path to reduce the overvoltage duration, and terminates discharge current as soon as V_{BUS} reaches the target voltage. To avoid the VBUS pin working abnormally, the AP43771V provides UVP function whenever V_{BUS} drops to UVP enable voltage.

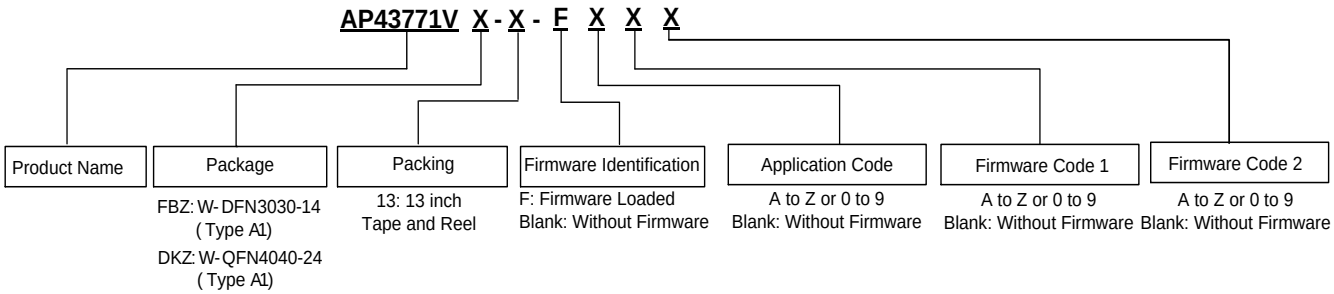
To ensure the safe operation of USB PD, the AP43771V provides programmable OCP function to make sure output current will not be higher than the allowed maximum current. Once OCP conditions happen, the AP43771V will shut down the USB PD system and send "Hard Reset" to the Upstream-Facing Port (UFP) device.

Performance Characteristics (continued)

CV/CC

The AP43771V supports Constant Voltage (CV) and Constant Current (CC) functions to control the output voltage and the output current by the control pin OCDRV. During the CV mode, the AP43771V operates in fixed PDO, and the output voltage will be regulated to the request voltage if the output current is below the allowed maximum current. Once the sink device draws more than I_{OCP}, the overcurrent protection occurs. When the CC mode function is enabled, the output voltage drops, and the source current is limited within 150mA whenever output current exceeds the allowed maximum current. When the output voltage drops below UVP, the constant current limit turns off V_{BUS} and starts error recovery procedure. The AP43771V will reset if the voltage continues dropping to the UVLO threshold.

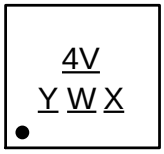
Ordering Information



Part Number	Package	Identification Code	Packing	
			Qty.	Carrier
AP43771VFBZ-13-FXXX	W-DFN3030-14 (Type A1)	4V	3000	13” Tape and Reel
AP43771VDKZ-13-FXXX	W-QFN4040-24 (Type A1)	6B	3000	13” Tape and Reel

Marking Information

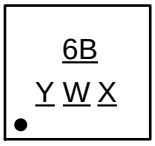
(Top View)



4V : Identification Code
Y : Year : 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents
52 and 53 week
X : Internal Code

W-DFN3030-14 (Type A1)

(Top View)



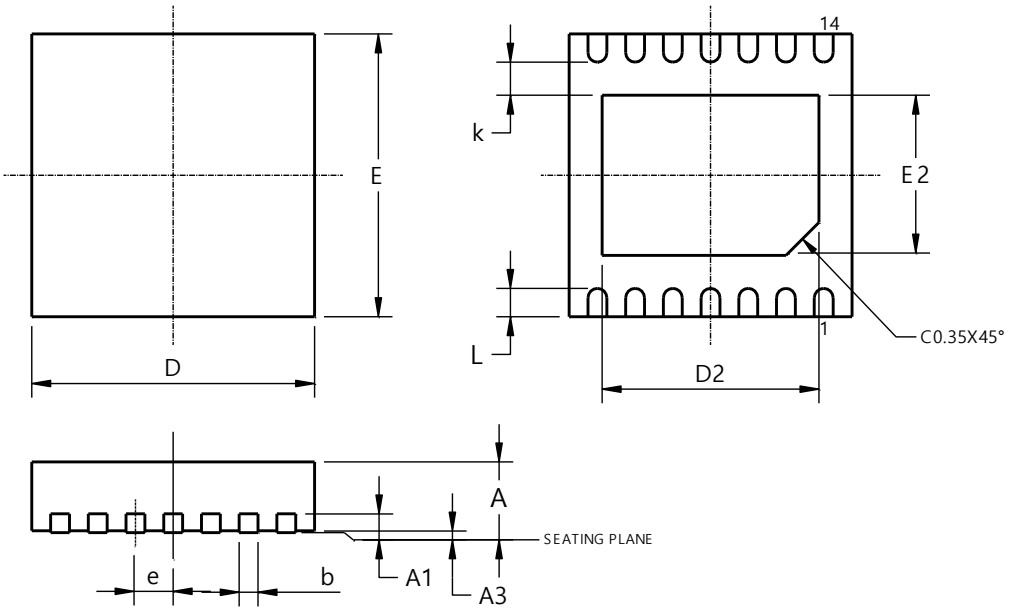
6B : Identification Code
Y : Year : 0 to 9
W : Week : A to Z : 1 to 26 Week;
a to z : 27 to 52 Week; z Represents
52 and 53 Week
X : Internal Code

W-QFN4040-24 (Type A1)

Package Outline Dimensions

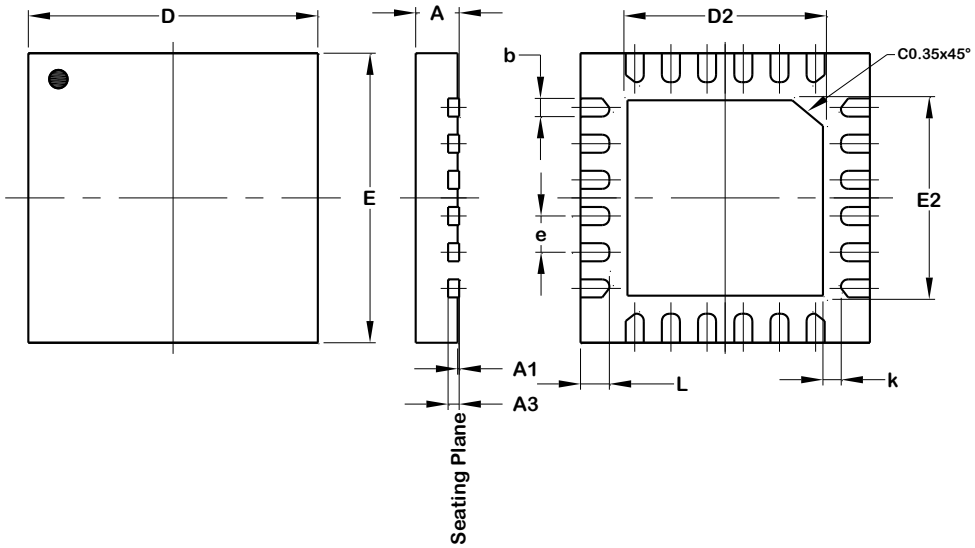
Please see http://www.diodes.com/package-outlines.html for the latest version.

W-DFN3030-14 (Type A1)



W-DFN3030-14 (Type A1)			
Dim	**Min**	**Max**	**Typ**
A	0.70	0.80	0.75
A1	0	0.05	0.02
A3	0.203REF		
b	0.15	0.25	0.20
D	3.00BSC		
D2	2.55	2.65	2.60
e	0.40BSC		
E	3.00BSC		
E2	1.65	1.75	1.70
k	0.20	--	--
L	0.35	0.45	0.40
All Dimensions in mm			

W-QFN4040-24 (Type A1)

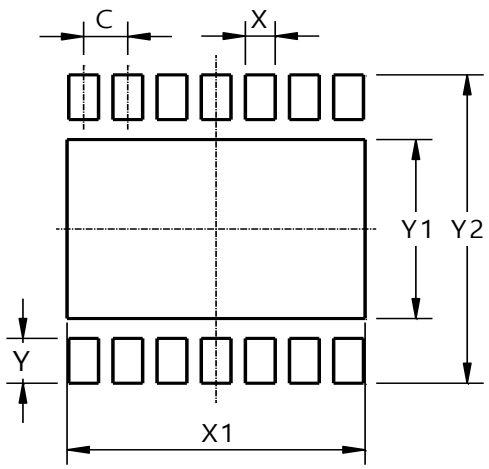


W-QFN4040-24 (Type A1)			
Dim	**Min**	**Max**	**Typ**
A	0.70	0.80	0.75
A1	0.00	0.05	0.02
A3	0.203 REF		
b	0.18	0.30	0.25
D	4.00 BSC		
D2	2.65	2.75	2.70
E	4.00 BSC		
E2	2.65	2.75	2.70
e	0.50 BSC		
k	0.20	--	--
L	0.35	0.45	0.40
All Dimensions in mm			

Suggested Pad Layout

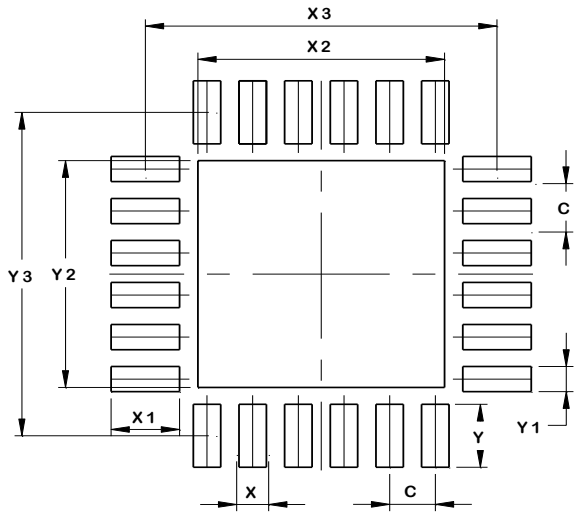
Please see http://www.diodes.com/package-outlines.html for the latest version.

W-DFN3030-14 (Type A1)



Dimensions	Value (in mm)
C	0.40
X	0.27
X1	2.70
Y	0.45
Y1	1.80
Y2	3.10

W-QFN4040-24 (Type A1)



Dimensions	Value (in mm)
C	0.500
X	0.300
X1	0.750
X2	2.700
X3	3.850
Y	0.750
Y1	0.300
Y2	2.700
Y3	3.850

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per J-STD-202 e3
- Weight: W-DFN3030-14 (Type A1), 0.017 grams (Approximate)
  W-QFN4040-24 (Type A1), 0.041 grams (Approximate)

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