

# KSZ9477 EVB/Demo Board with Atmel SAMA5D3 SoC

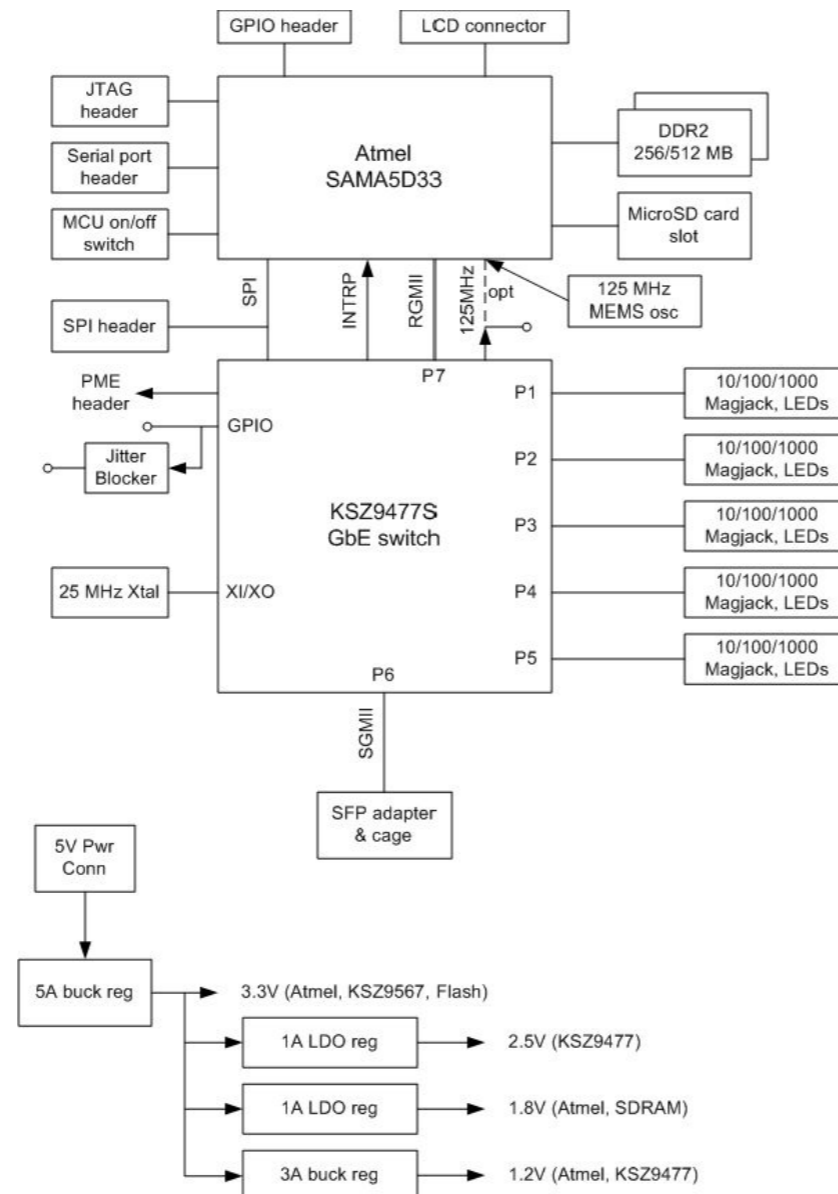
## Table of Contents



Sheet	Description
1	Block Diagram
2	Power Regulation
3	Power Connections - Switch and SoC
4	KSZ9477S Switch and RGMII
5	Ethernet Port Connectors
6	SoC Main - Flash, SD card, USB
7	SDRAM
8	GPIO and LCD Connectors

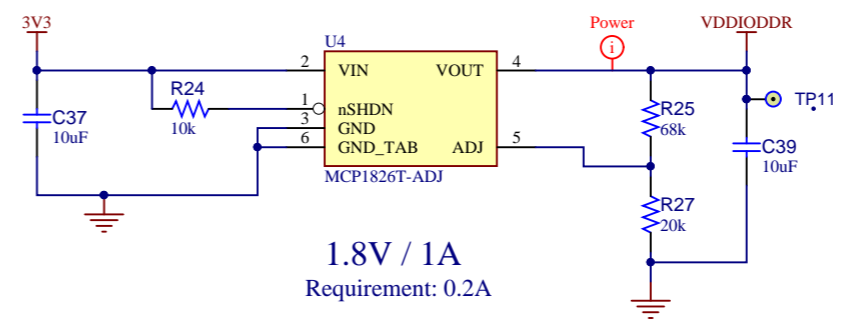
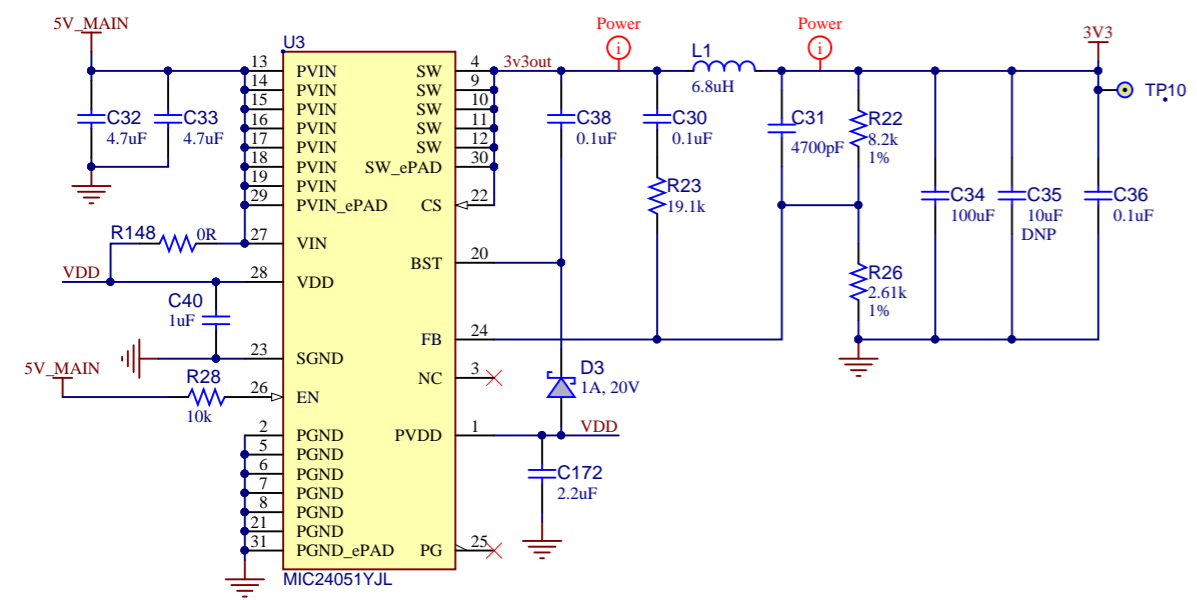
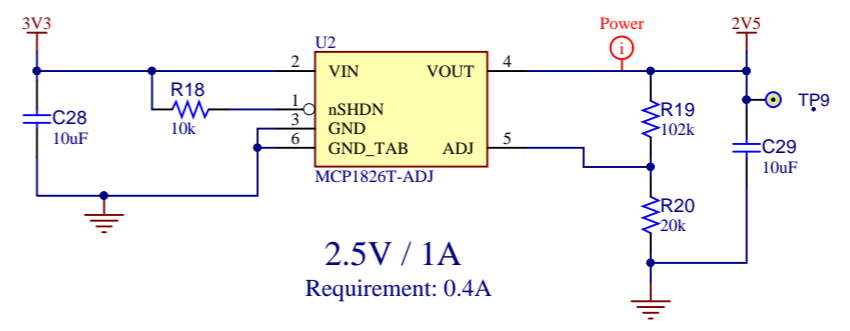
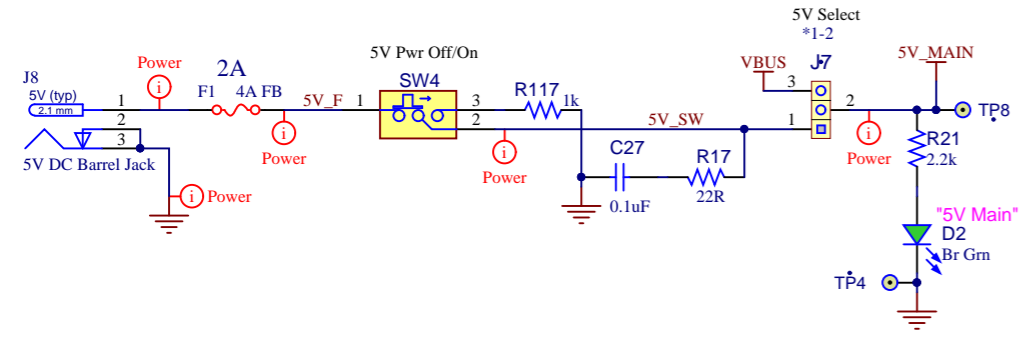
## Revision History

Revision	Date	Revision Summary	Author
A00	6/23/2016	Pre-release	Kelly Maas
B	12/15/2016	Release	Kelly Maas
B1	3/9/2017	Update KSZ9477 SGMII pin names, update notes	Kelly Maas

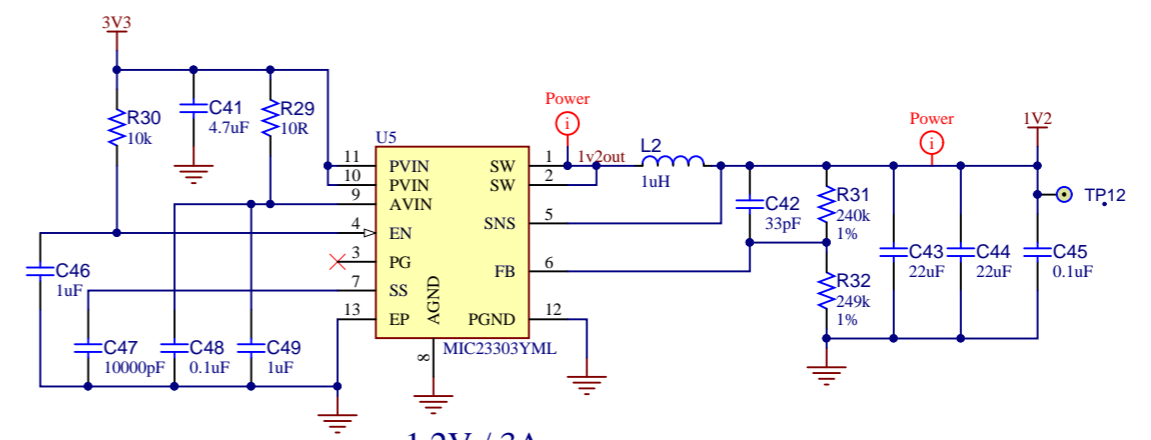
## Block Diagram



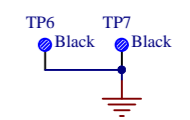
	Microchip Technology, Inc. USB/Network Group - UNG www.Microchip.com	Designed with 		
	Description: <b>KSZ9477 EVB_Demo Board with SAMA5D3 SoC</b> Page Title: <b>Title Page</b> Project Name: <b>KSZ9477 EVB_Demo</b> PN: <b>UNG_8071</b>			
Size: B	Date: 3/30/2017	Designer: Kelly Maas	Sheet 1 of 8	Rev B1

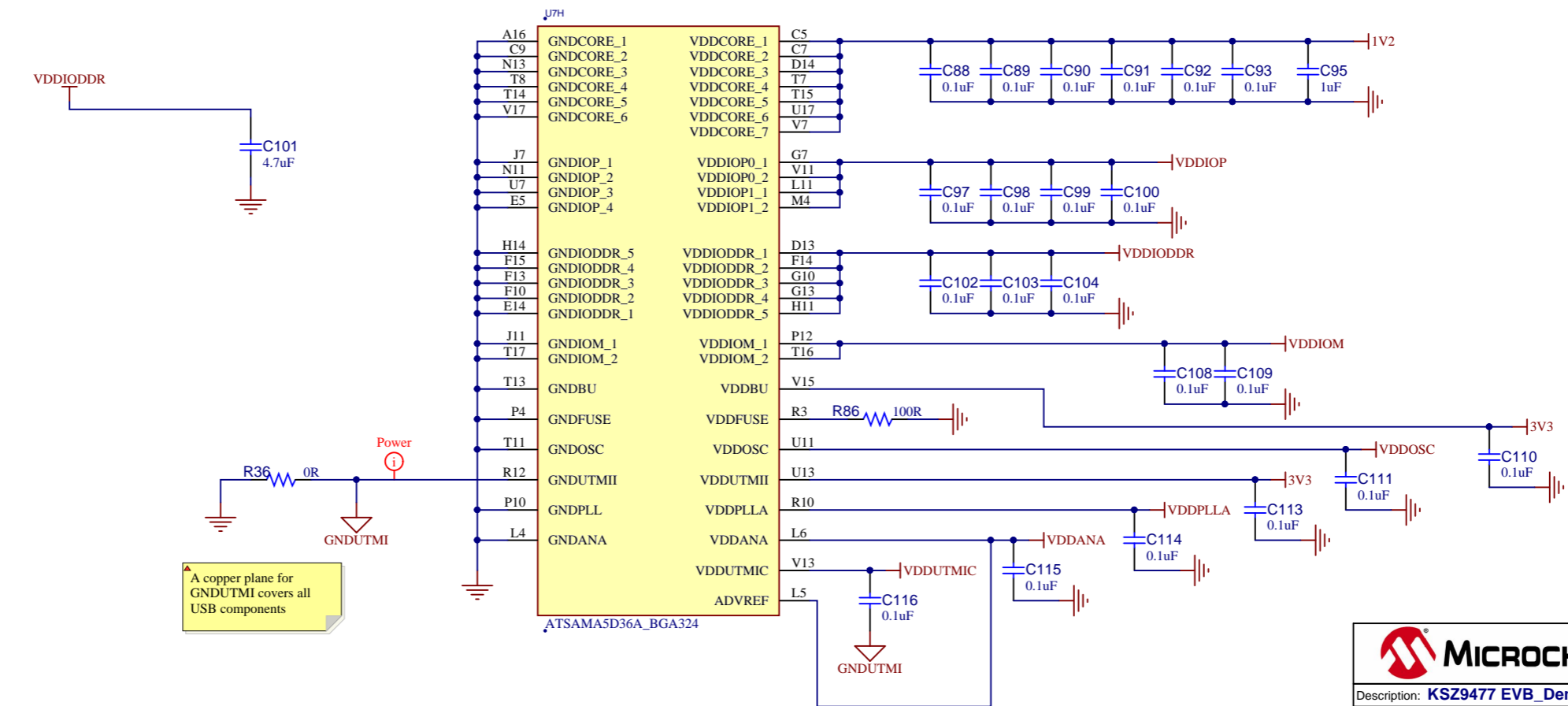
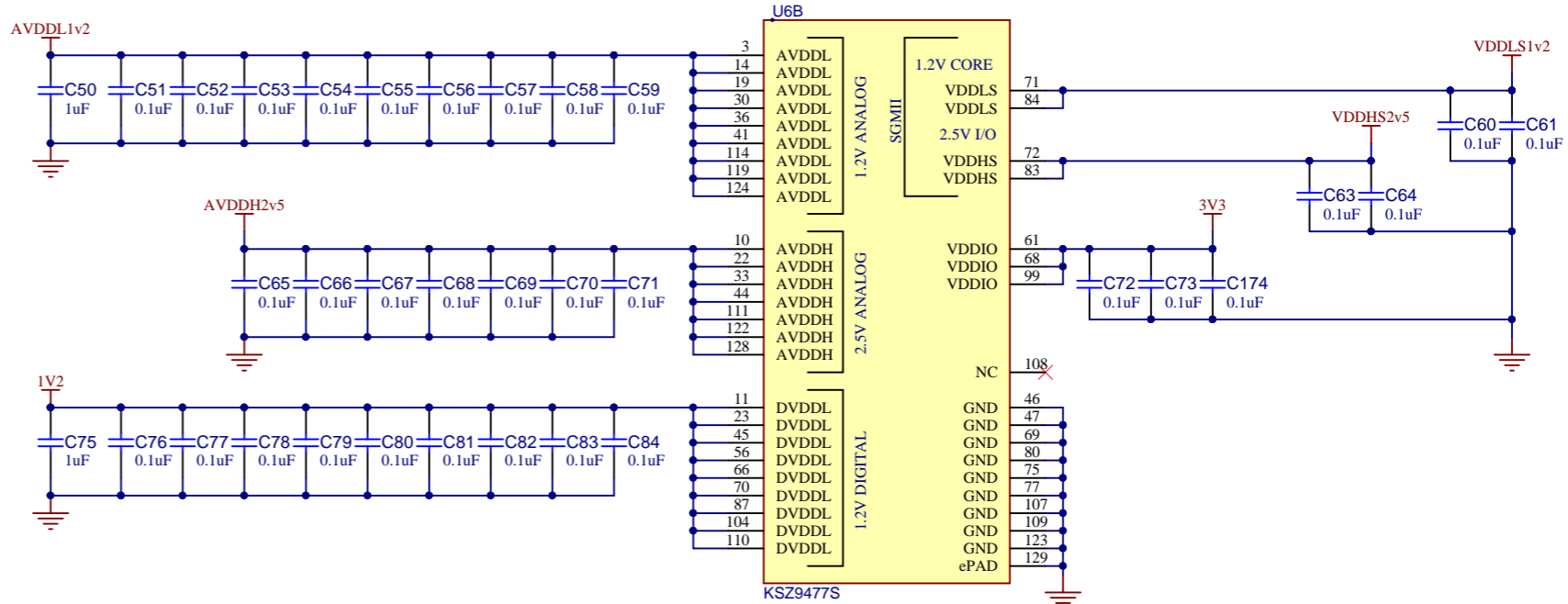
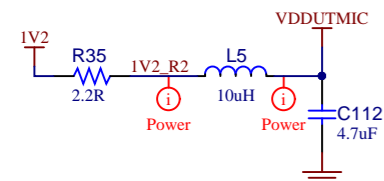
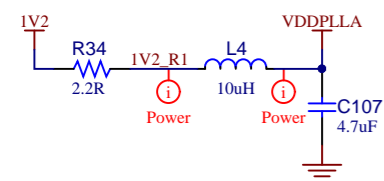
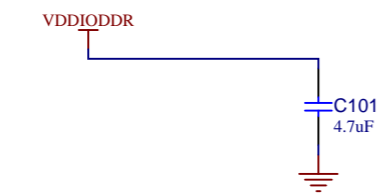
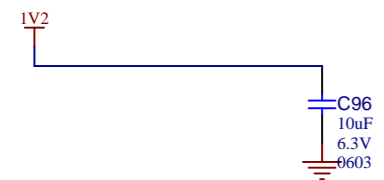
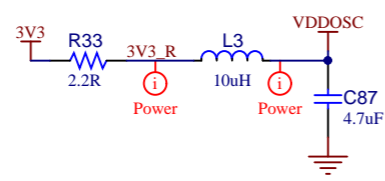
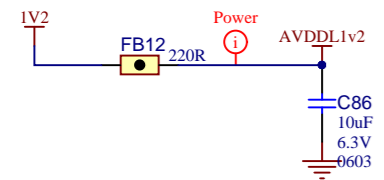
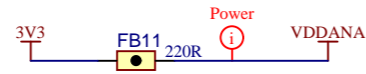
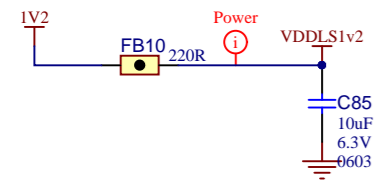
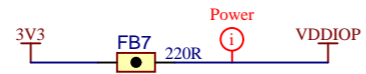
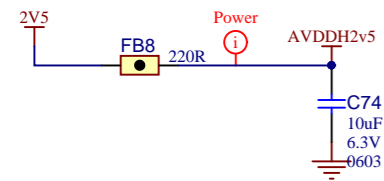
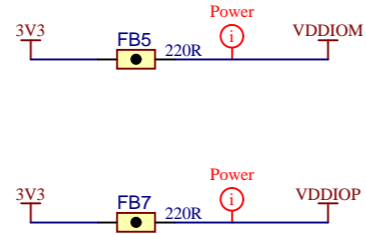
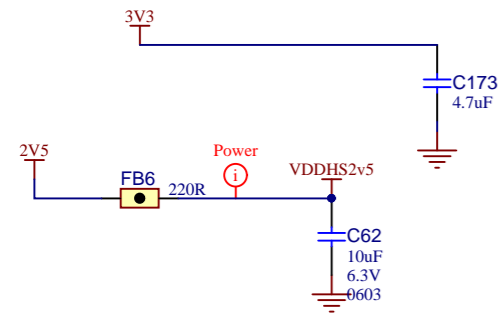


3.3V / 6A  
Requirement: 2A

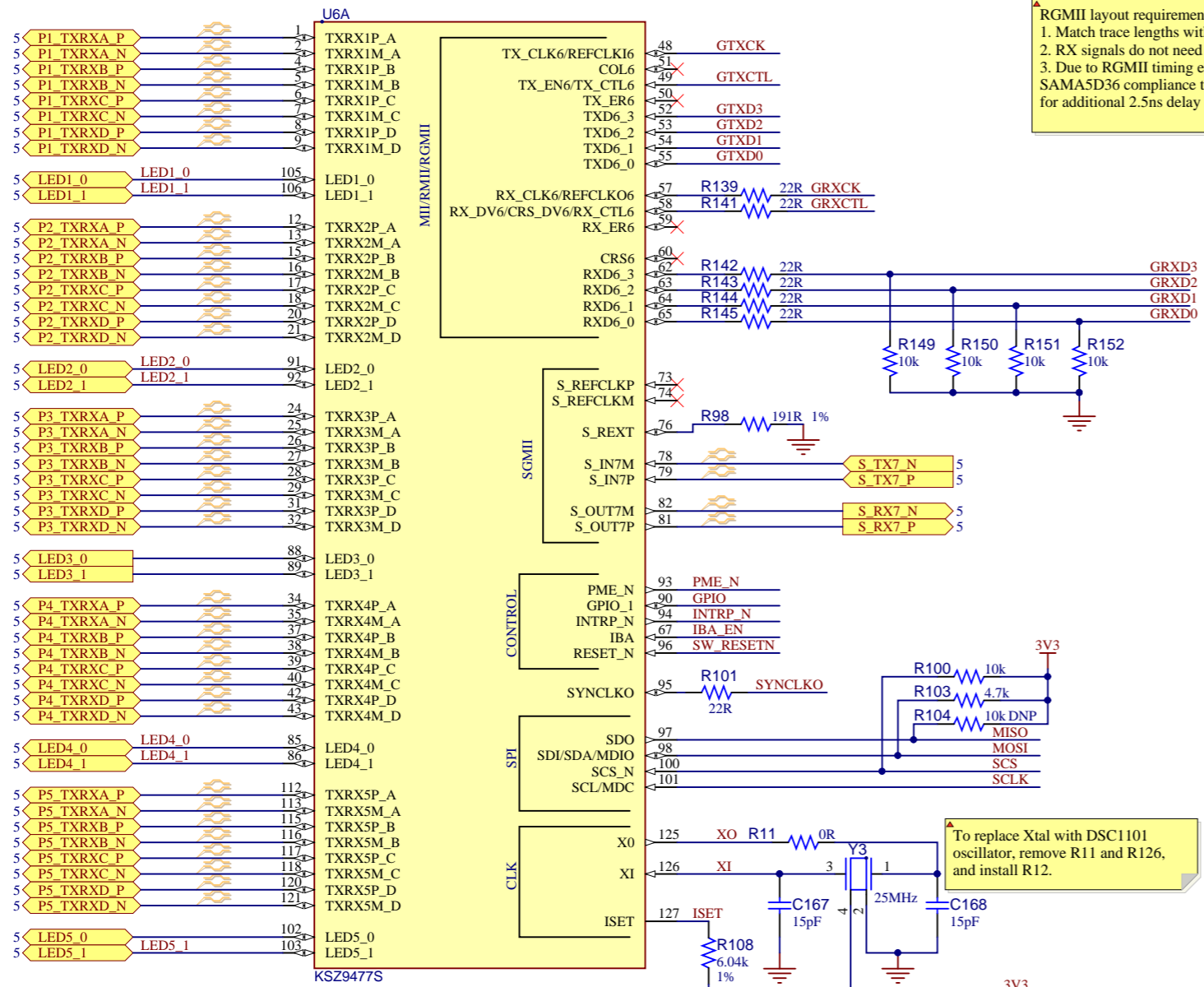


1.2V / 3A  
Requirement: 1.6A



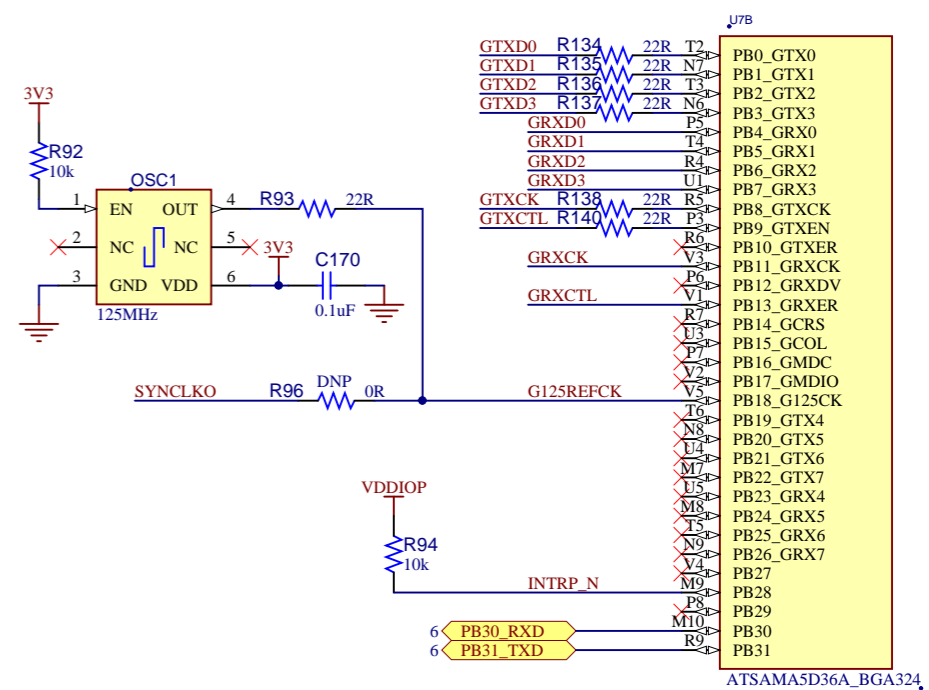


A copper plane for GNDUTMI covers all USB components

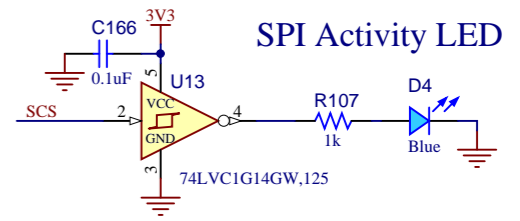
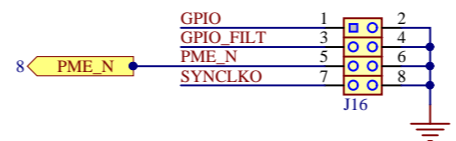


**RGMII layout requirements**

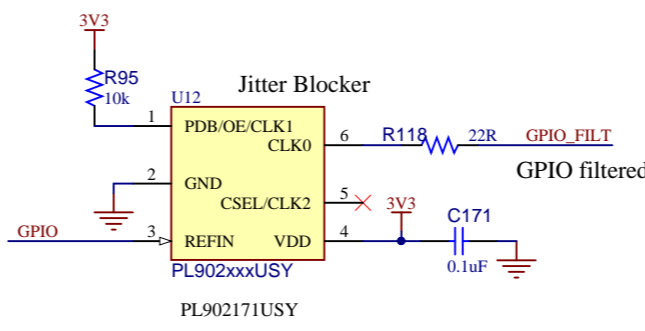
1. Match trace lengths within 10 to 100 mils.
2. RX signals do not need to be length match to TX signals.
3. Due to RGMII timing error in port 6 of KSZ9477, plus SAMASD36 compliance to RGMII v1.3, GTXCK must be routed for additional 2.5ns delay relative to GTXD[3:0] and GTXCTL.



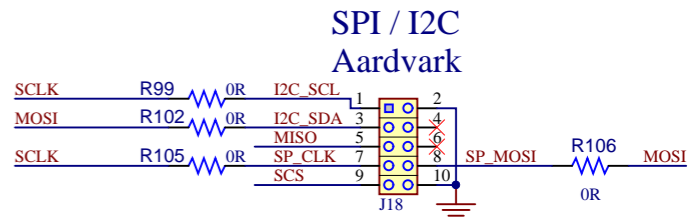
**KSZ9477 Output Header**



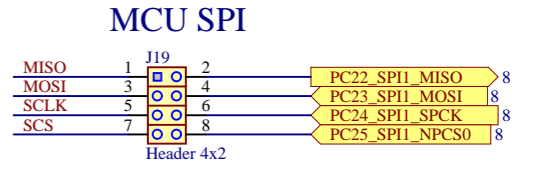
**SPI Activity LED**



**Jitter Blocker**

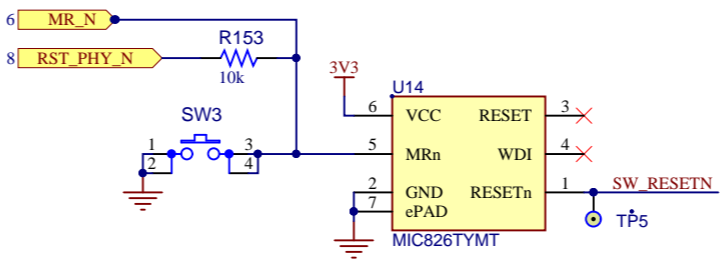


**SPI / I2C Aardvark**



**MCU SPI**

Install all 4 jumpers at J19 for MCU to control KSZ9477 via SPI. Remove all jumpers at J19 when connecting external SPI or I2C controller to header J18.



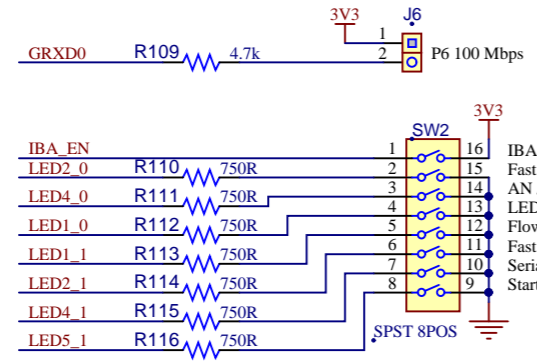
**KSZ9477 Reset 200ms delay**

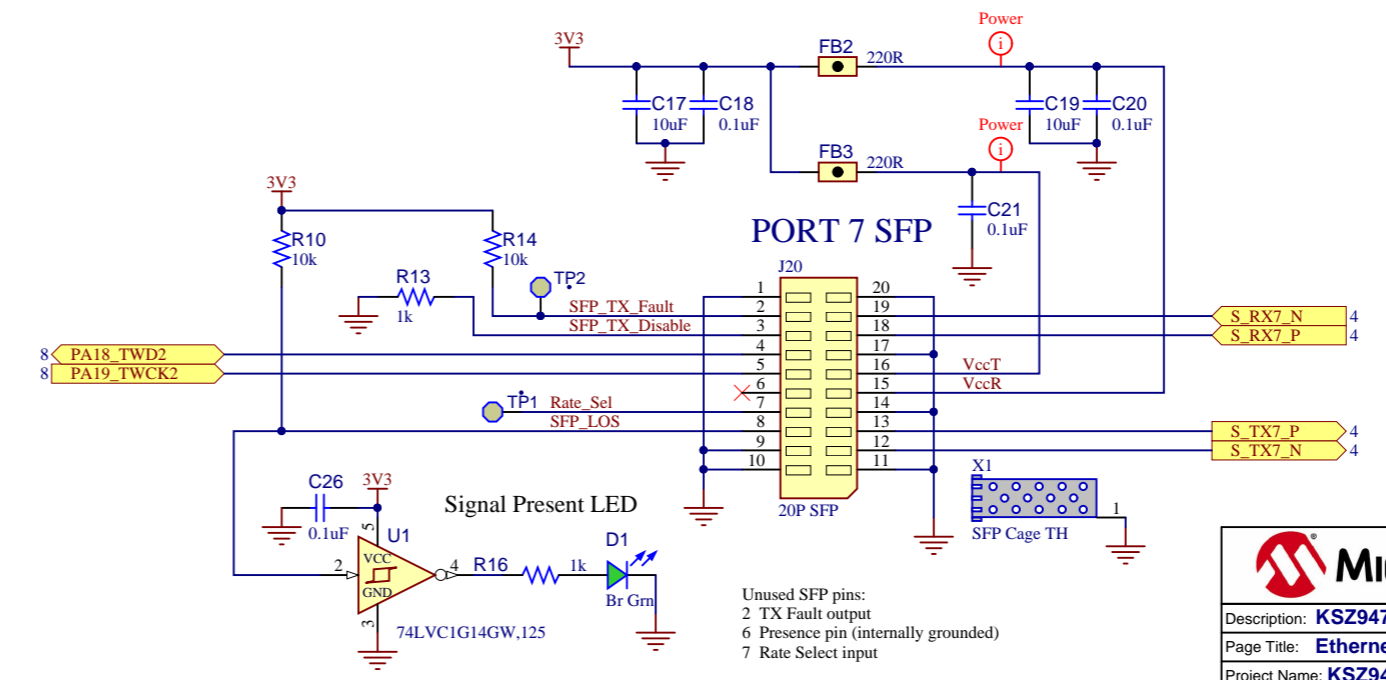
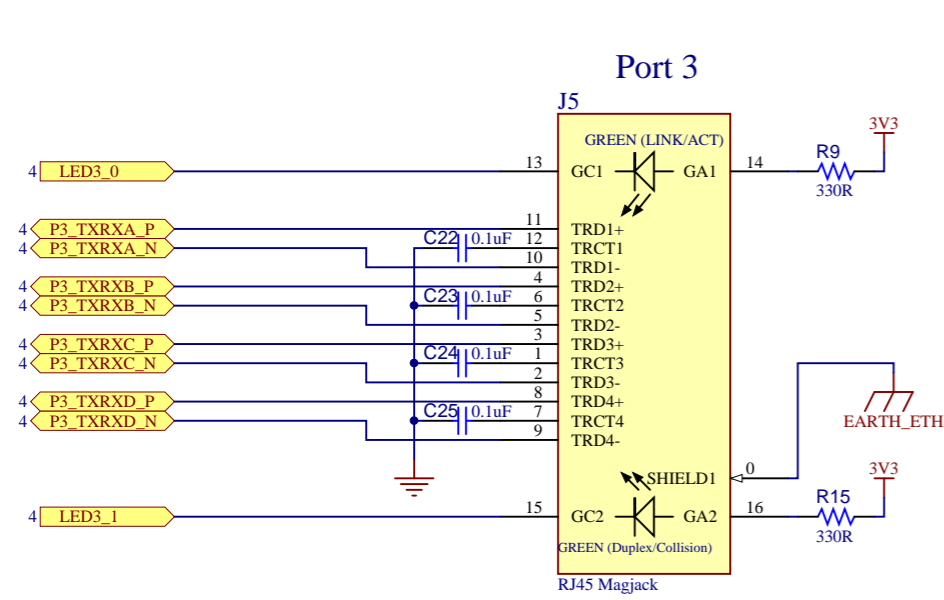
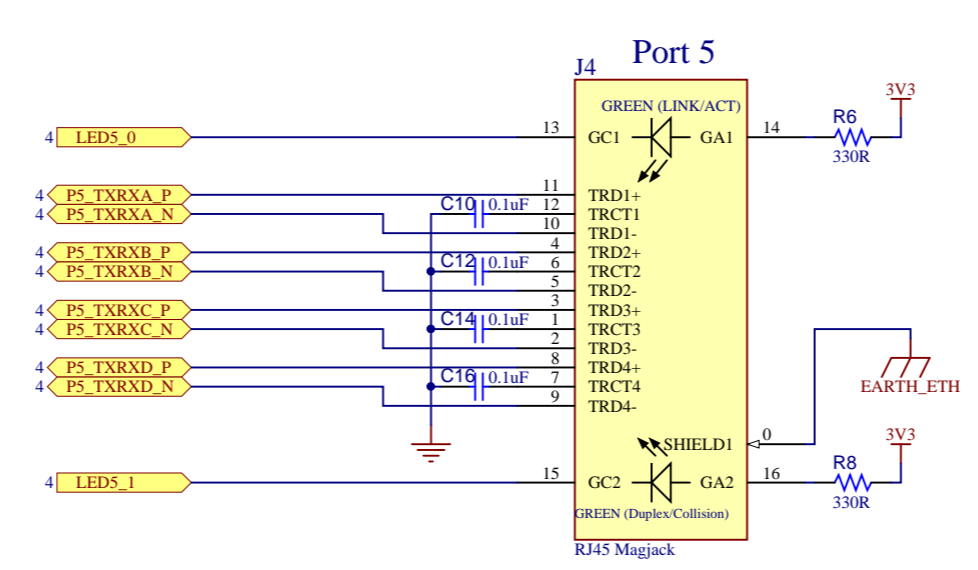
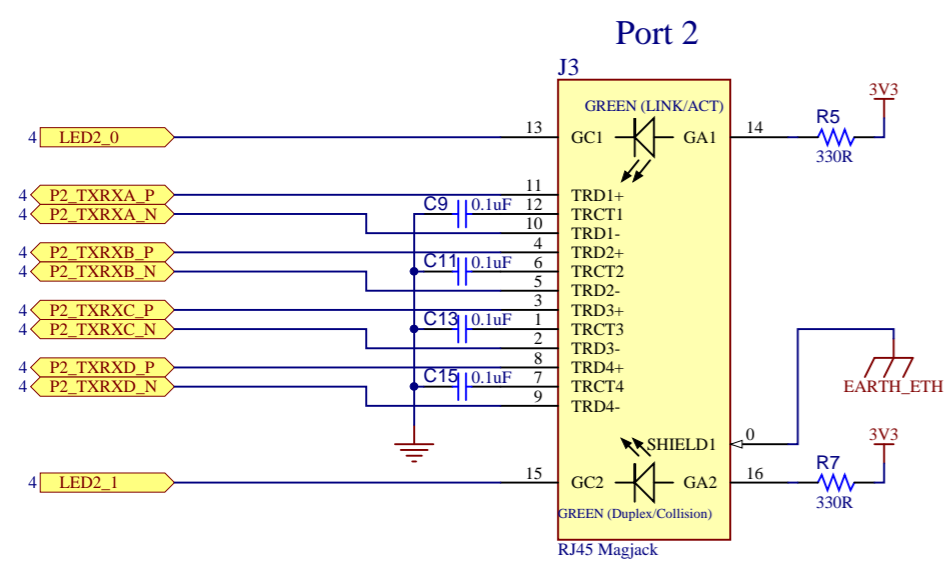
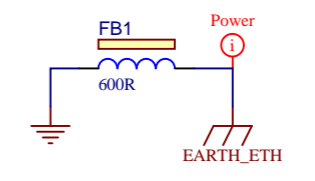
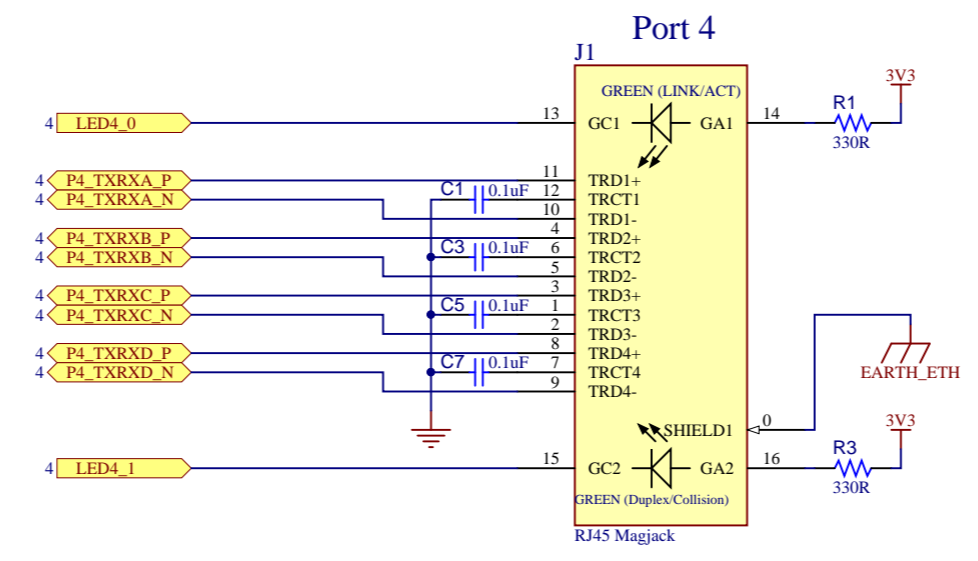
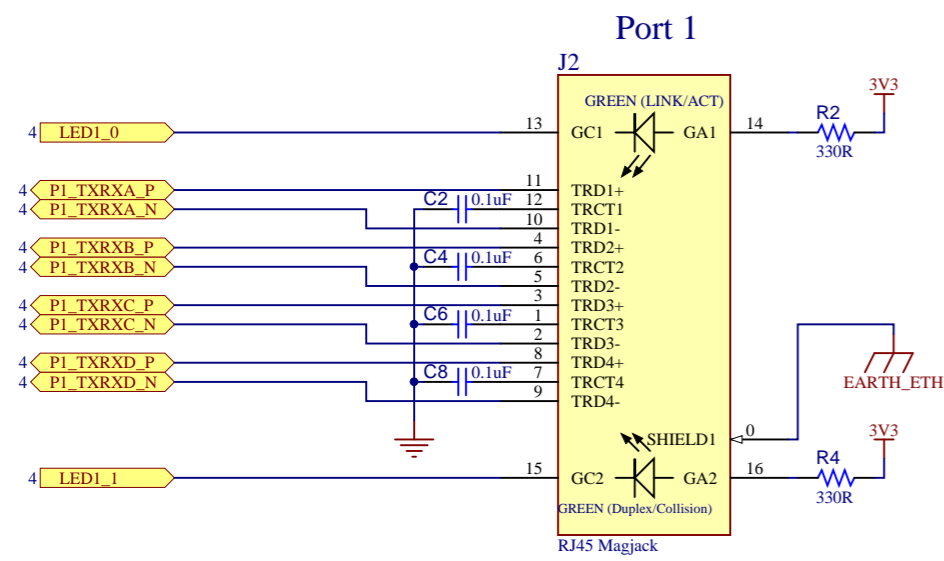
**KSZ9477S Configuration Strap Options**

	Open	Closed
GRXD0	RGMII: 1000 Mb/s	RGMII: 100 Mb/s
LED2_0	1000B-T master or 10/100 MDI	1000B-T slave or 10/100 MDI-X
LED4_0	Enable AN or 100B-TX	Disable AN or 1000B-T
LED1_0	Quiet-WIRE off	Quiet-WIRE on
LED1_1	Flow control on	Flow control off
LED2_1	Normal link up	Fast link up
LED4_1	SPI	I2C
LED5_1	Start switch	Don't start switch
IBA	IBA off	IBA enabled

No option:  
 LED3\_1 No option for MDC/MDIO  
 RXD6\_[3:2] Port 6 fixed as RGMII  
 RXD6\_1 Not relevant when port is RGMII  
 SYNCLKO S\_REFCLKP/M input clock not used

**KSZ9477 Configuration Strap Options**

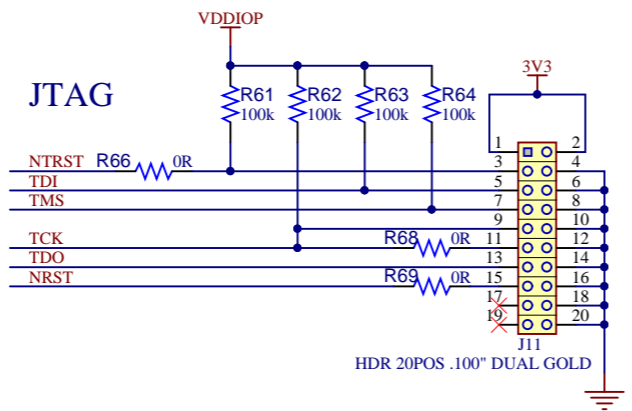




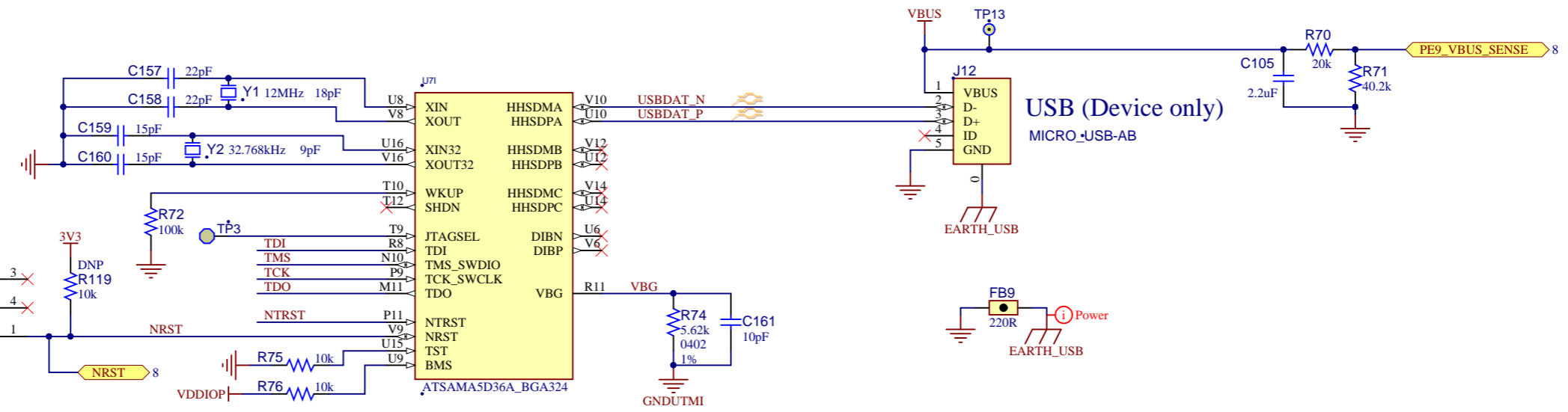
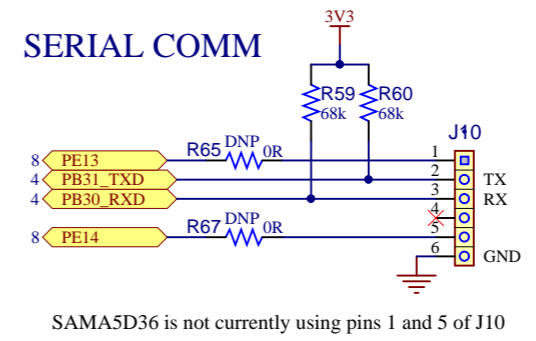
Unused SFP pins:  
 2 TX Fault output  
 6 Presence pin (internally grounded)  
 7 Rate Select input

	Microchip Technology, Inc. USB/Network Group - UNG www.Microchip.com	 Designed with Altium.com
	Description: <b>KSZ9477 EVB_Demo Board with SAMA5D3 SoC</b> Page Title: <b>Ethernet ports and SGMII SFP</b> Project Name: <b>KSZ9477 EVB_Demo</b> PN: <b>UNG_8071</b> Size: B   Date: <b>2/16/2017</b>   Designer: <b>Kelly Maas</b>   Sheet 5 of 8   Rev B1	

### JTAG

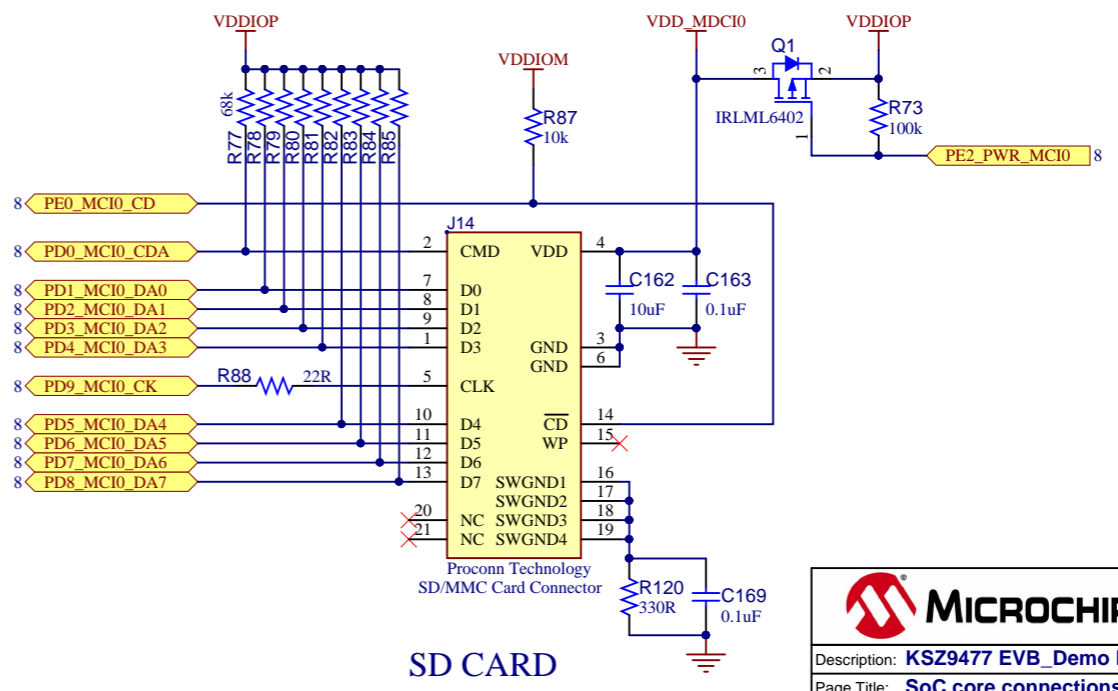
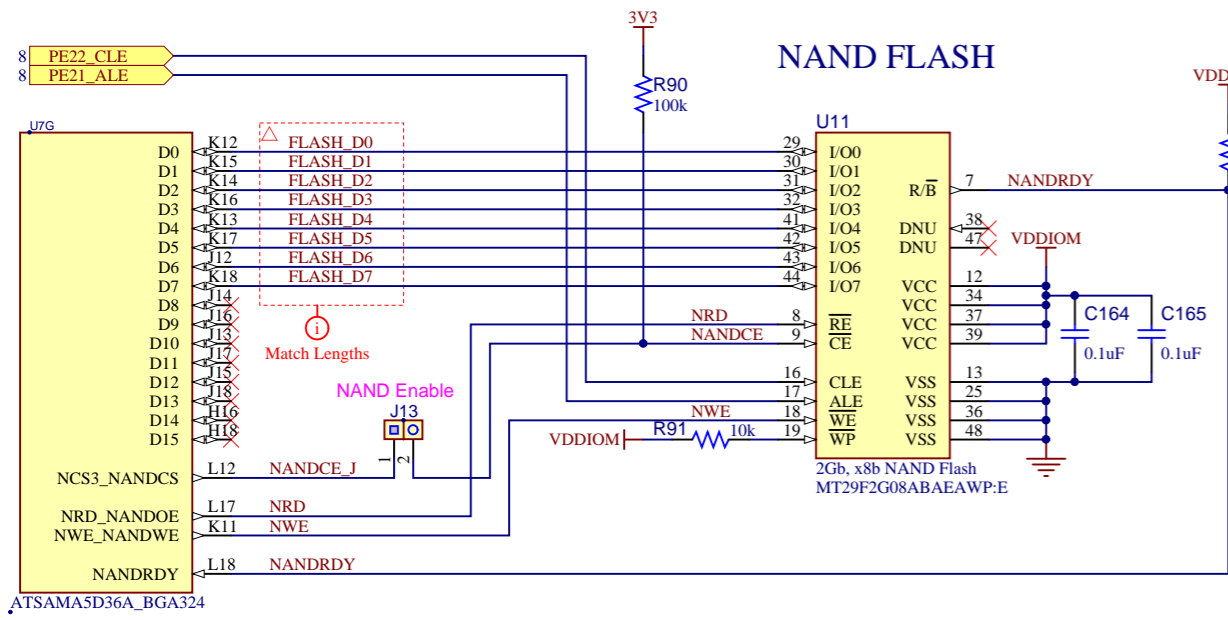


### SERIAL COMM



Reset / 200ms delay

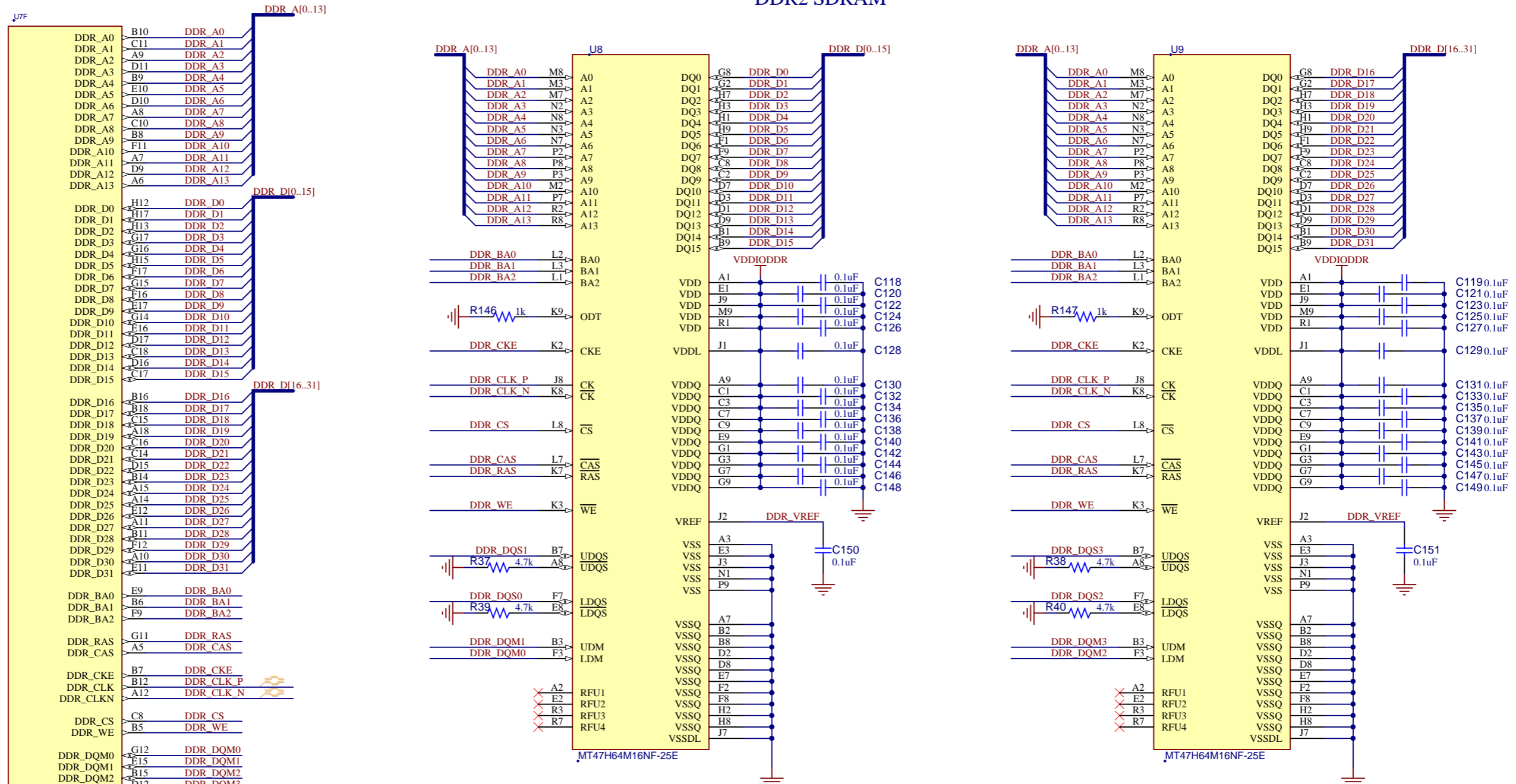
### NAND FLASH



Preferred location is bottom side of board

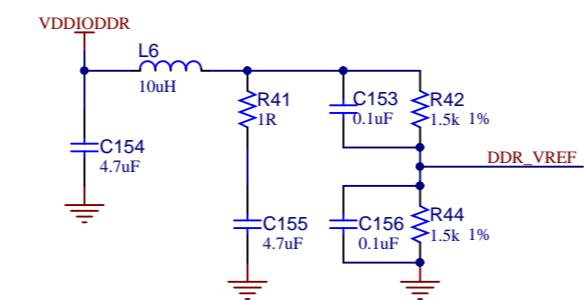
	Microchip Technology, Inc. USB/Network Group - UNG www.Microchip.com	
	Description: <b>KSZ9477 EVB_Demo Board with SAMA5D3 SoC</b> Page Title: <b>SoC core connections, NAND Flash, SD Card</b> Project Name: <b>KSZ9477 EVB_Demo</b> PN: <b>UNG_8071</b> Size: B   Date: <b>3/9/2017</b>   Designer: <b>Kelly Maas</b>   Sheet 6 of 8   Rev B1	

# DDR2 SDRAM

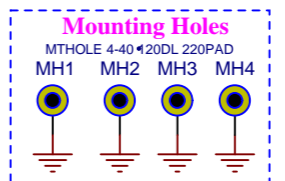
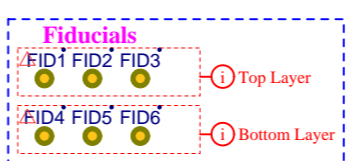
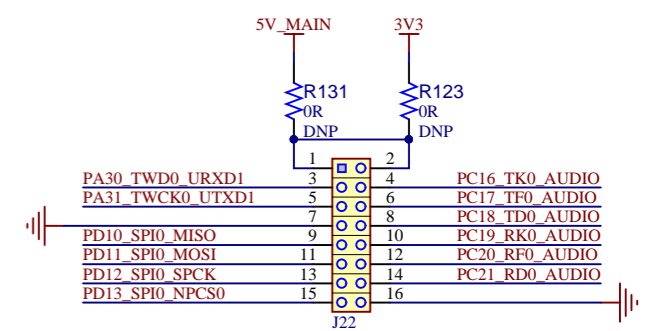
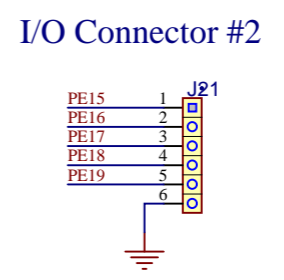
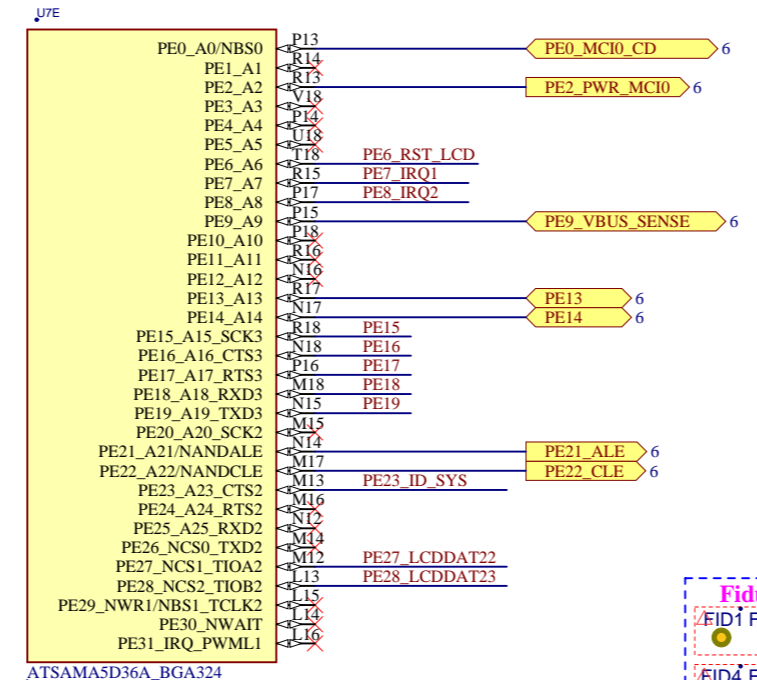
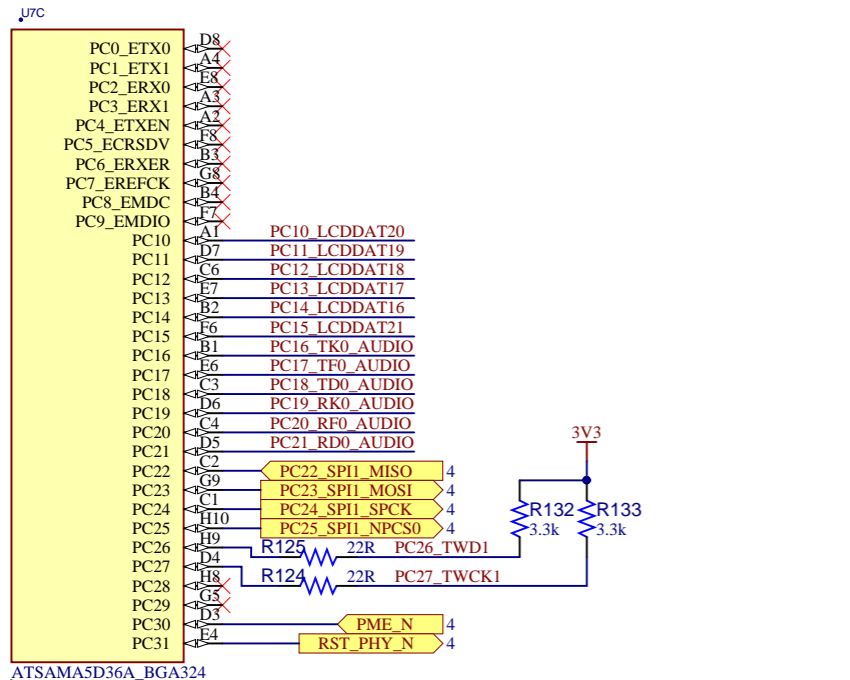
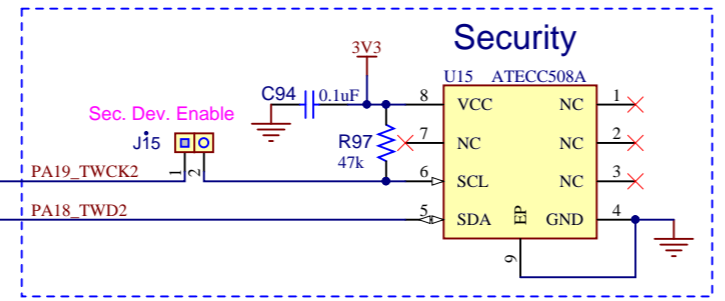
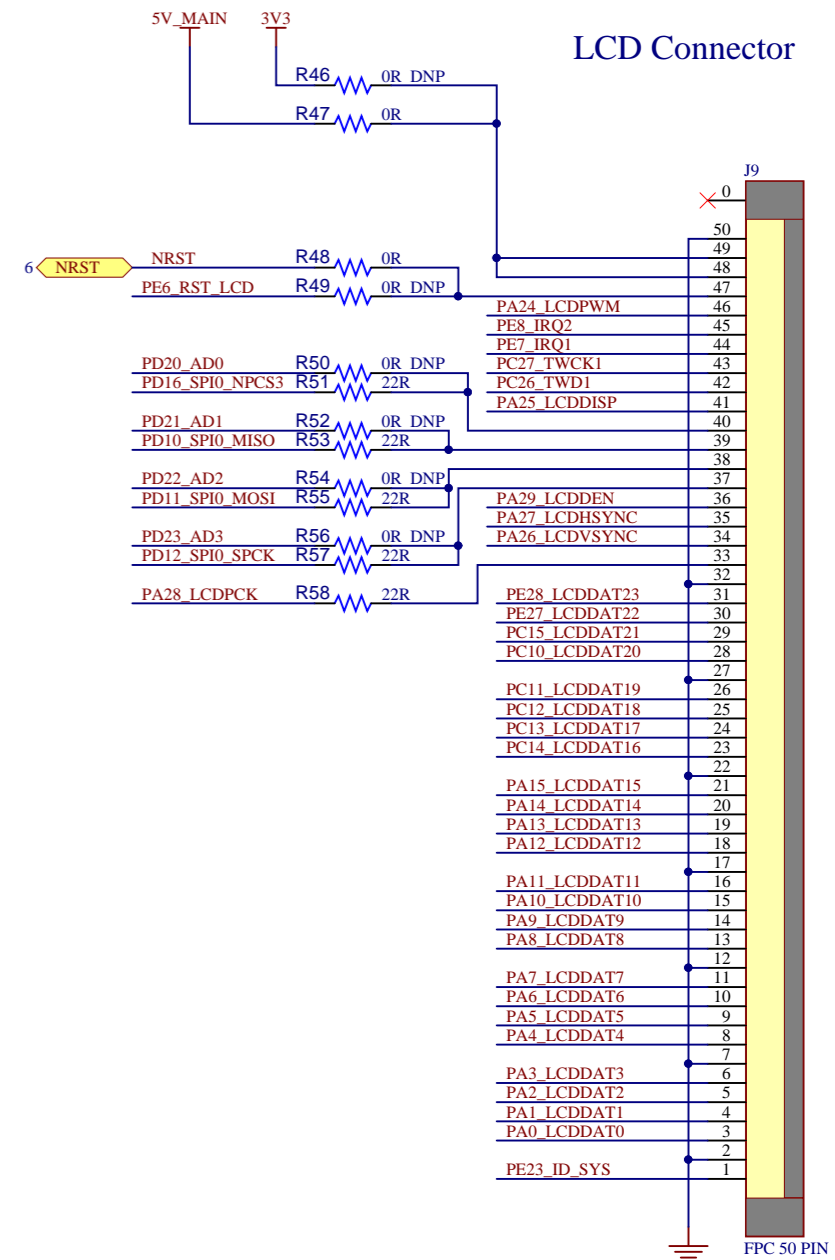
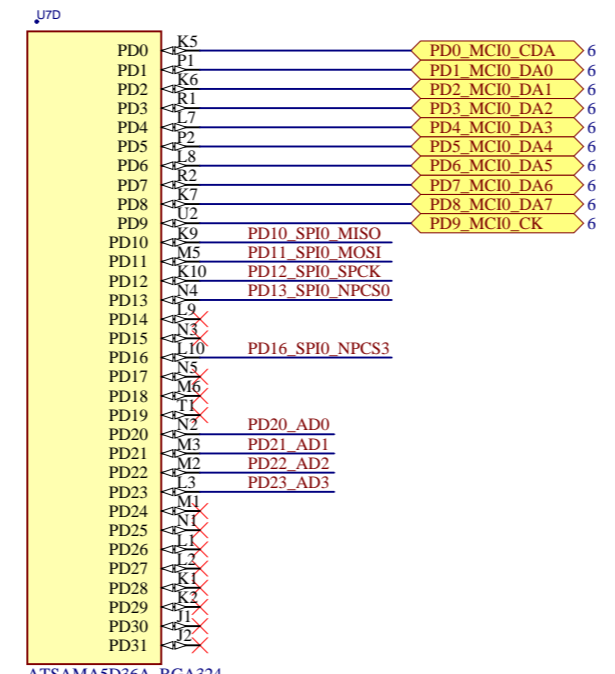
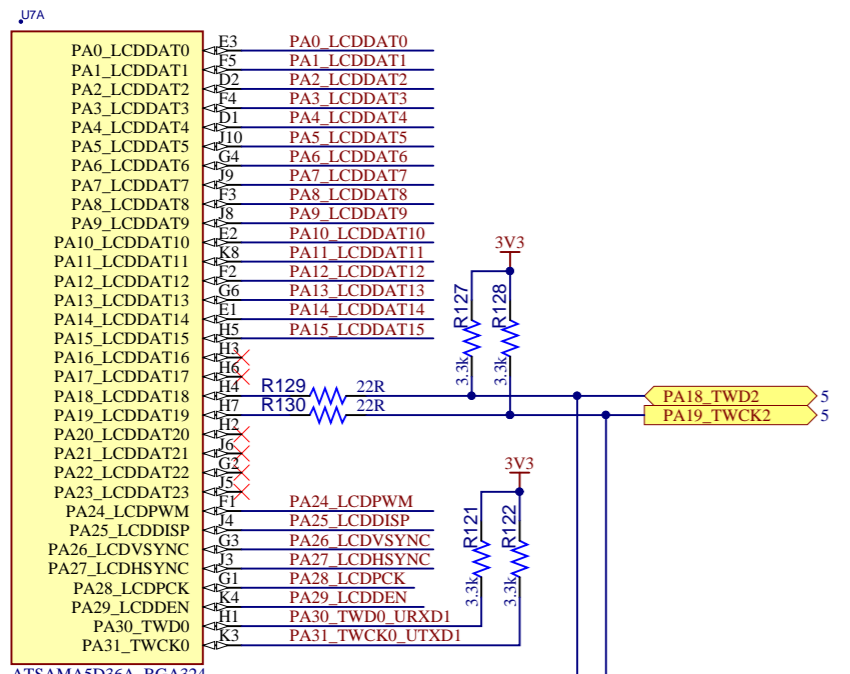


Keep nets as short as possible. Therefore DDR2 devices have to be placed as close as possible to SAM5D3. The layout EBI DDR2 should use controlled impedance traces of Z0= 50ohm.

Address, control and data traces may not exceed 1.3 inches (33mm).  
 Address, control and data traces must be length matched to within 0.1 inch (2.54mm).  
 Address, control and data traces must match the data group trace lengths to within 0.25 inch (6.35mm).



	Microchip Technology, Inc. USB/Network Group - UNG www.Microchip.com	
	Description: <b>KSZ9477 EVB_Demo Board with SAM5D3 SoC</b> Page Title: <b>DDR2 SDRAM</b> Project Name: <b>KSZ9477 EVB_Demo</b> PN: <b>UNG_8071</b> Size: B   Date: <b>12/6/2016</b>   Designer: <b>Kelly Maas</b>   Sheet 7 of 8   Rev B1	



		Microchip Technology, Inc. USB/Network Group - UNG www.Microchip.com		 Designed with Altium.com	
Description: <b>KSZ9477 EVB_Demo Board with SAMA5D3 SoC</b>					
Page Title: <b>SoC GPIO, LCD Connector, misc headers</b>					
Project Name: <b>KSZ9477 EVB_Demo</b>			PN: <b>UNG_8071</b>		
Size: B	Date: 12/9/2016	Designer: Kelly Maas	Sheet 8 of 8	Rev B1	