



PSMN005-30K

N-channel TrenchMOS SiliconMAX logic level FET

Rev. 2 — 22 December 2011

Product data sheet

1. Product profile

1.1 General description

SiliconMAX logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Suitable for high frequency applications due to fast switching characteristics

1.3 Applications

- Computer motherboards
- DC-to-DC converters
- Switched-mode power supplies

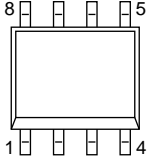
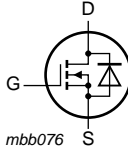
1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$	-	-	30	V
I_D	drain current	$T_{sp} = 80\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 1	-	-	20	A
P_{tot}	total power dissipation	$T_{sp} = 80\text{ °C}$; see Figure 2	-	-	3.5	W
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 15\text{ A}$; $T_j = 25\text{ °C}$; see Figure 9 ; see Figure 10	-	4.4	5.5	m Ω
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 4.5\text{ V}$; $I_D = 20\text{ A}$; $V_{DS} = 15\text{ V}$; $T_j = 25\text{ °C}$; see Figure 11	-	14	-	nC

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>SOT96-1 (SO8)</p>	
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		

3. Ordering information

Table 3. Ordering information

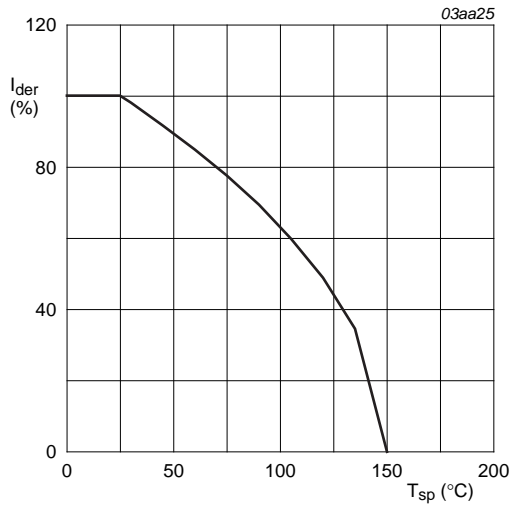
Type number	Package		
	Name	Description	Version
PSMN005-30K	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

4. Limiting values

Table 4. Limiting values

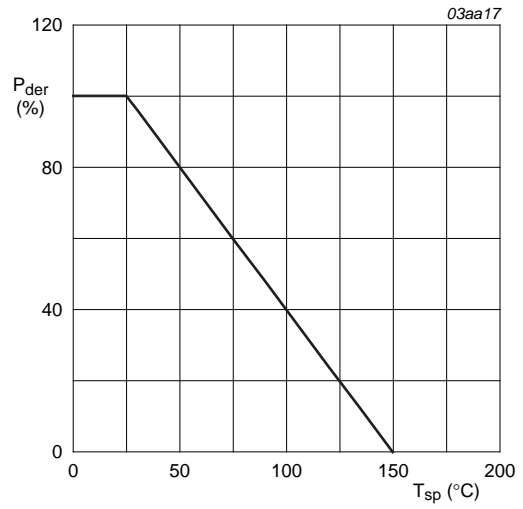
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$	-	30	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$T_{sp} = 80\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 1	-	20	A
I_{DM}	peak drain current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; see Figure 3	-	60	A
P_{tot}	total power dissipation	$T_{sp} = 80\text{ °C}$; see Figure 2	-	3.5	W
T_{stg}	storage temperature		-55	150	°C
T_j	junction temperature		-55	150	°C
Source-drain diode					
I_S	source current	$T_{sp} = 80\text{ °C}$	-	20	A
I_{SM}	peak source current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	60	A



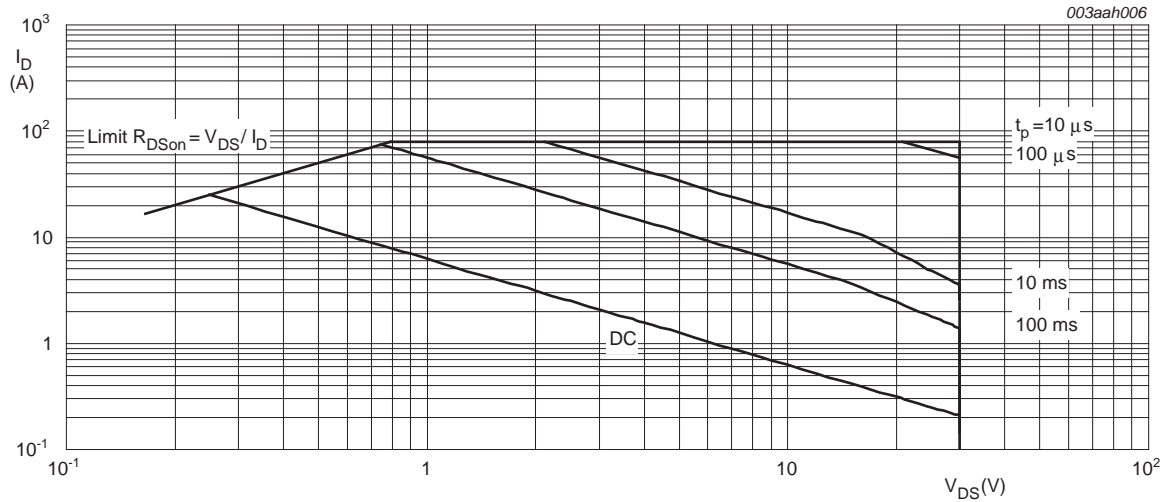
$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$

Fig. 1. Normalized continuous drain current as a function of solder point temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

Fig. 2. Normalized total power dissipation as a function of solder point temperature



$T_{sp} = 25^\circ\text{C}$; I_{DM} is single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	mounted on a metal clad board ; see Figure 4	-	-	20	K/W

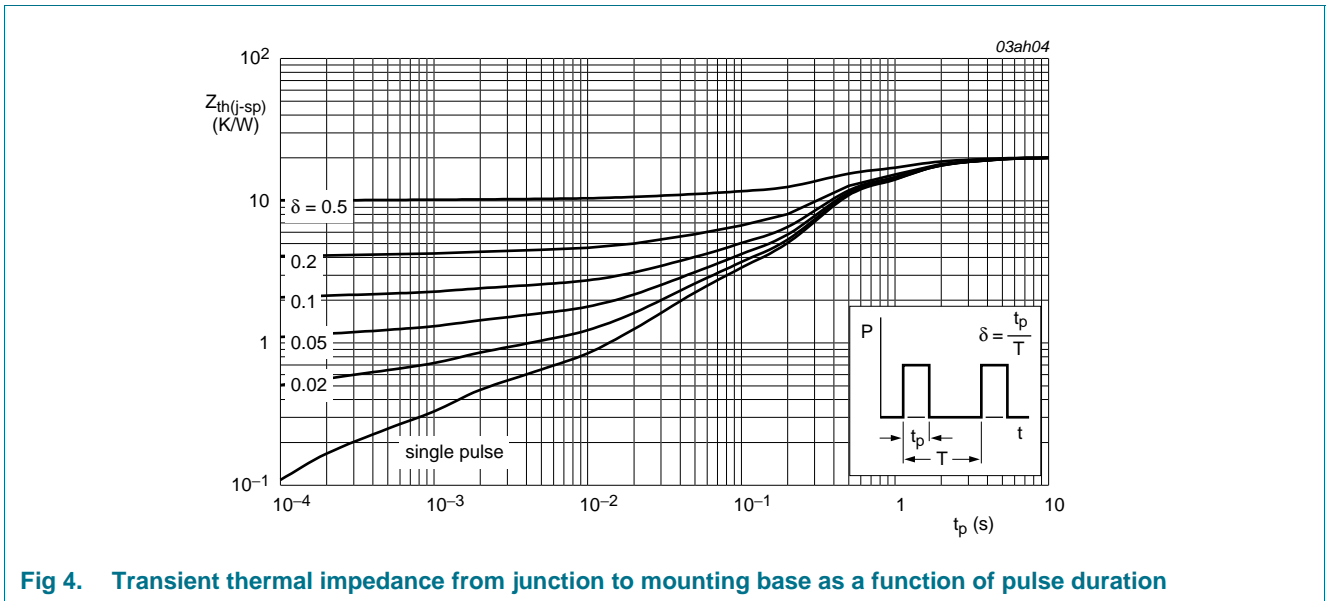
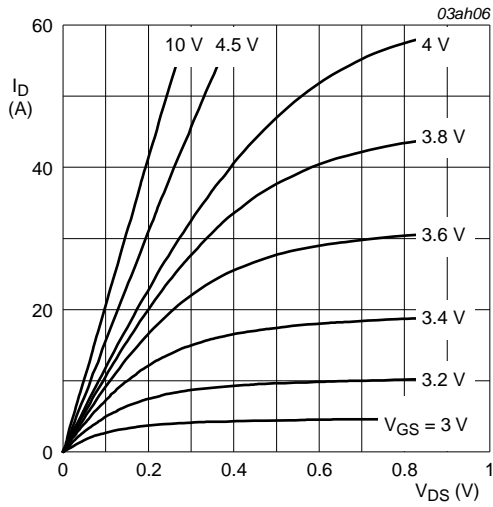


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

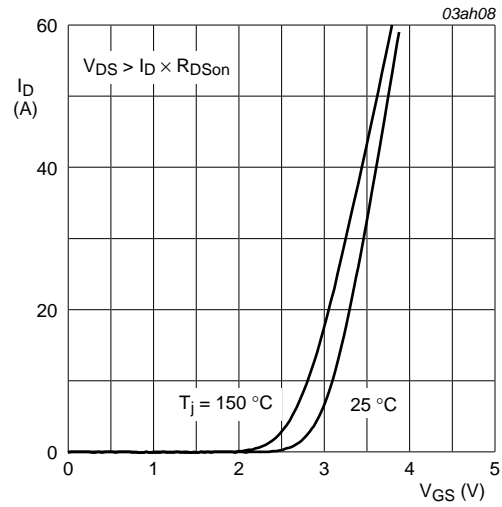
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$	30	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 150 \text{ }^\circ C$; see Figure 8	0.5	-	-	V
		$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$; $T_j = -55 \text{ }^\circ C$; see Figure 8	-	-	3.4	V
		$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 25 \text{ }^\circ C$; see Figure 8	1	-	3	V
I_{DSS}	drain leakage current	$V_{DS} = 30 V$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	1	μA
		$V_{DS} = 30 V$; $V_{GS} = 0 V$; $T_j = 150 \text{ }^\circ C$	-	-	0.5	mA
I_{GSS}	gate leakage current	$V_{GS} = 20 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	100	nA
		$V_{GS} = -20 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5 V$; $I_D = 13 A$; $T_j = 25 \text{ }^\circ C$; see Figure 9 ; see Figure 10	-	6.6	8	m Ω
		$V_{GS} = 10 V$; $I_D = 15 A$; $T_j = 25 \text{ }^\circ C$; see Figure 9 ; see Figure 10	-	4.4	5.5	m Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 20 A$; $V_{DS} = 15 V$; $V_{GS} = 4.5 V$; $T_j = 25 \text{ }^\circ C$; see Figure 11	-	34	-	nC
Q_{GS}	gate-source charge		-	15	-	nC
Q_{GD}	gate-drain charge		-	14	-	nC
C_{iss}	input capacitance	$V_{DS} = 25 V$; $V_{GS} = 0 V$; $f = 1 \text{ MHz}$; $T_j = 25 \text{ }^\circ C$; see Figure 12	-	3100	-	pF
C_{oss}	output capacitance		-	605	-	pF
C_{rss}	reverse transfer capacitance		-	405	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15 V$; $R_L = 15 \text{ } \Omega$; $V_{GS} = 10 V$; $R_{G(ext)} = 6 \text{ } \Omega$; $T_j = 25 \text{ }^\circ C$	-	18	-	ns
t_r	rise time		-	16	-	ns
$t_{d(off)}$	turn-off delay time		-	65	-	ns
t_f	fall time		-	45	-	ns
g_{fs}	transfer conductance	$V_{DS} = 15 V$; $I_D = 20 A$; $T_j = 25 \text{ }^\circ C$	-	60	-	S
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 15 A$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$; see Figure 13	-	0.81	1.3	V
t_{rr}	reverse recovery time	$I_S = 10 A$; $di_S/dt = -100 \text{ A}/\mu s$; $V_{GS} = 0 V$; $V_{DS} = 25 V$; $T_j = 25 \text{ }^\circ C$	-	35	-	ns
Q_r	recovered charge		-	20	-	nC



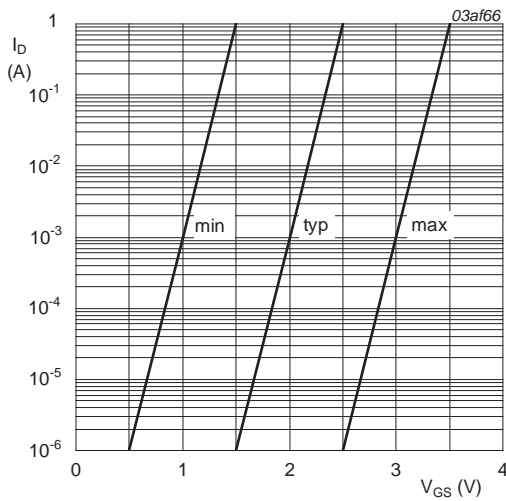
$T_j = 25^\circ C$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



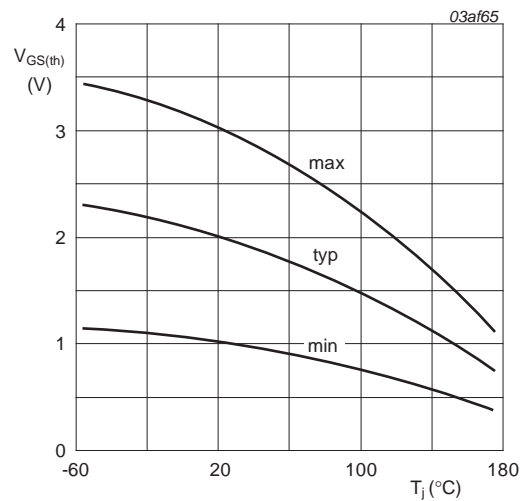
$T_j = 25^\circ C$ and $175^\circ C; V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



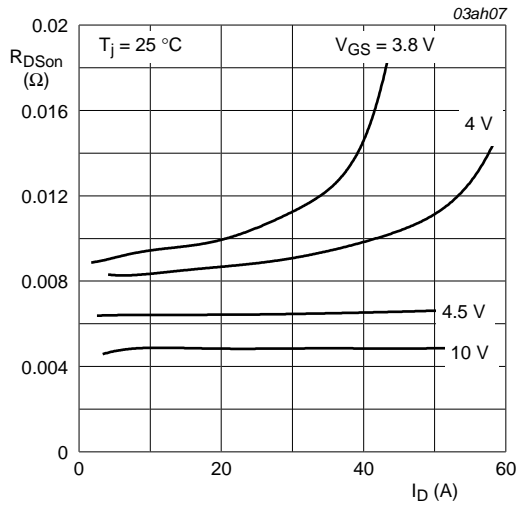
$T_j = 25^\circ C; V_{DS} = 5V$

Fig 7. Sub-threshold drain current as a function of gate-source voltage



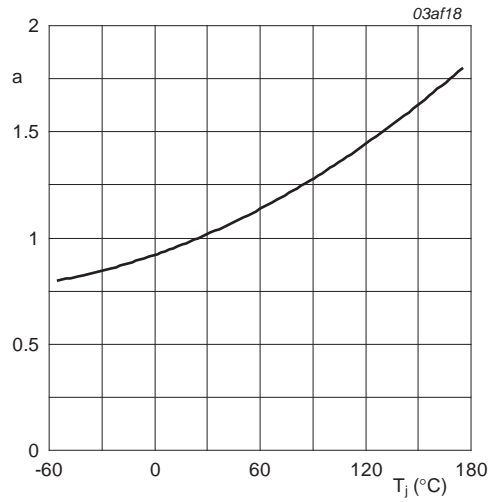
$I_D = 1mA; V_{DS} = V_{GS}$

Fig 8. Gate-source threshold voltage as a function of junction temperature



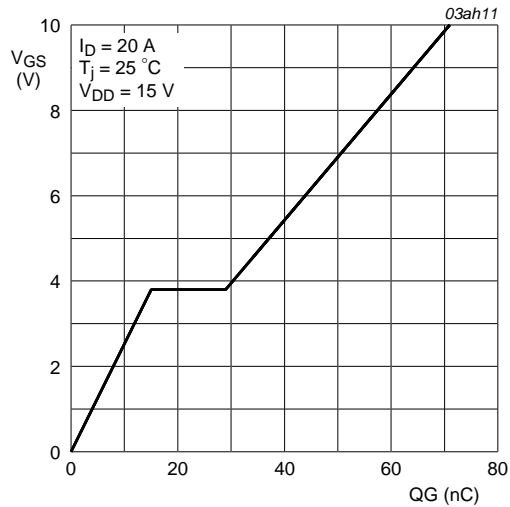
$T_j = 25\text{ }^\circ\text{C}$

Fig 9. Drain-source on-state resistance as a function of drain current; typical values



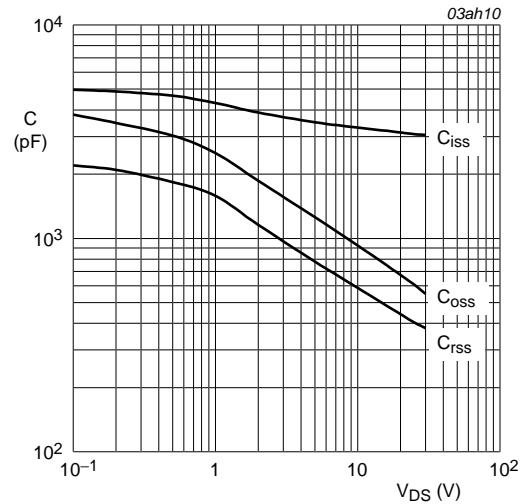
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^\circ\text{C})}}$$

Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature



$I_D = 20\text{ A}; V_{DS} = 15\text{ V}$

Fig 11. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

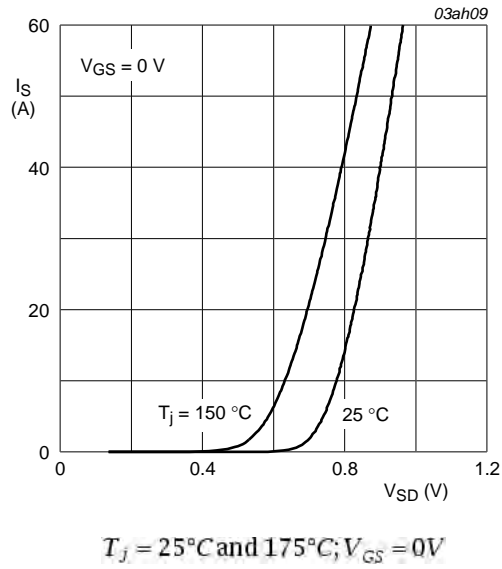


Fig 13. Source current as a function of source-drain voltage; typical values

7. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

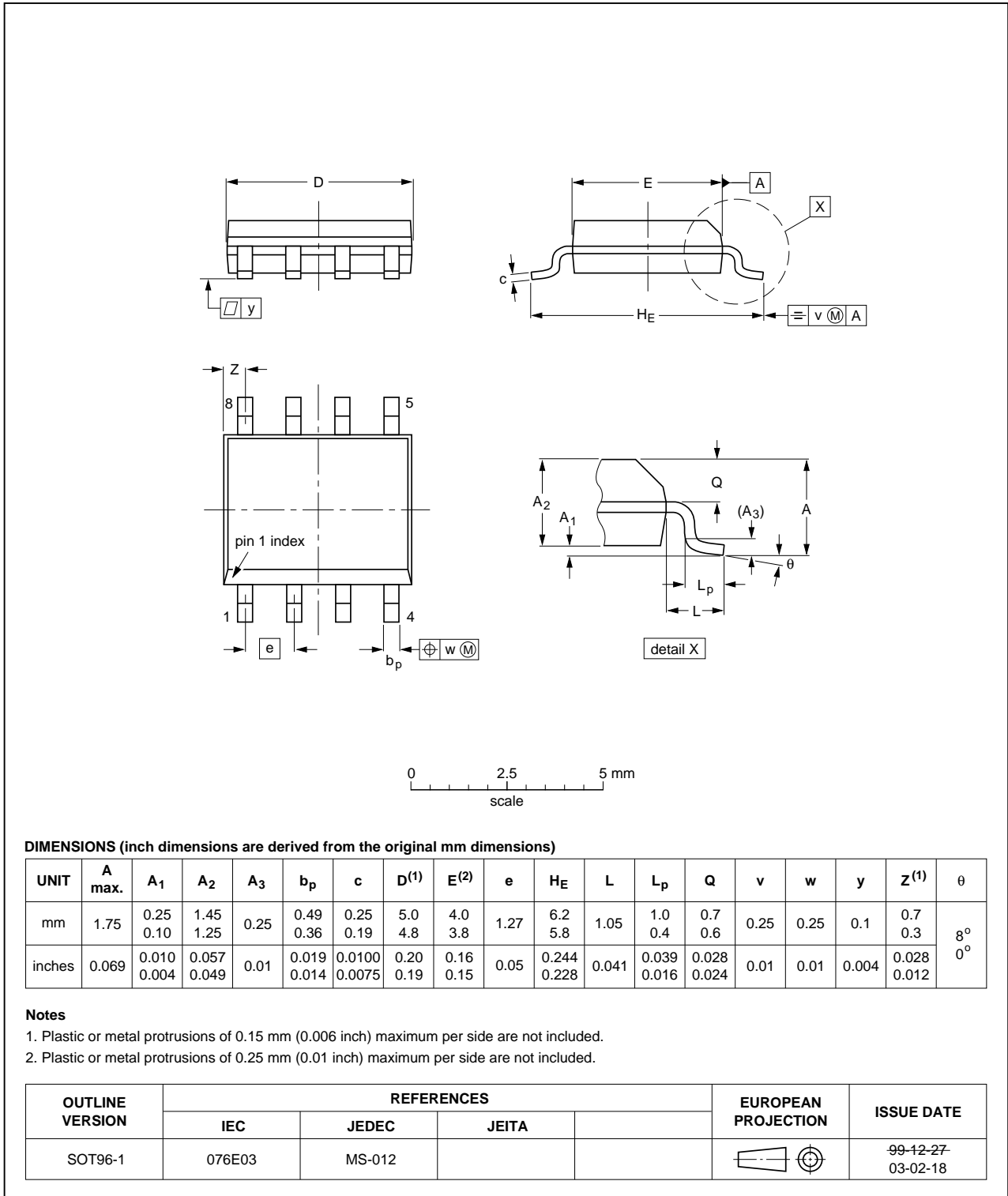


Fig 14. Package outline SOT96-1 (SO8)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN005-30K v.2	20111222	Product data sheet	-	PSMN005-30K_1
Modifications:	• Various changes to content.			
PSMN005-30K_1	20091117	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^[1] ^[2]	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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