ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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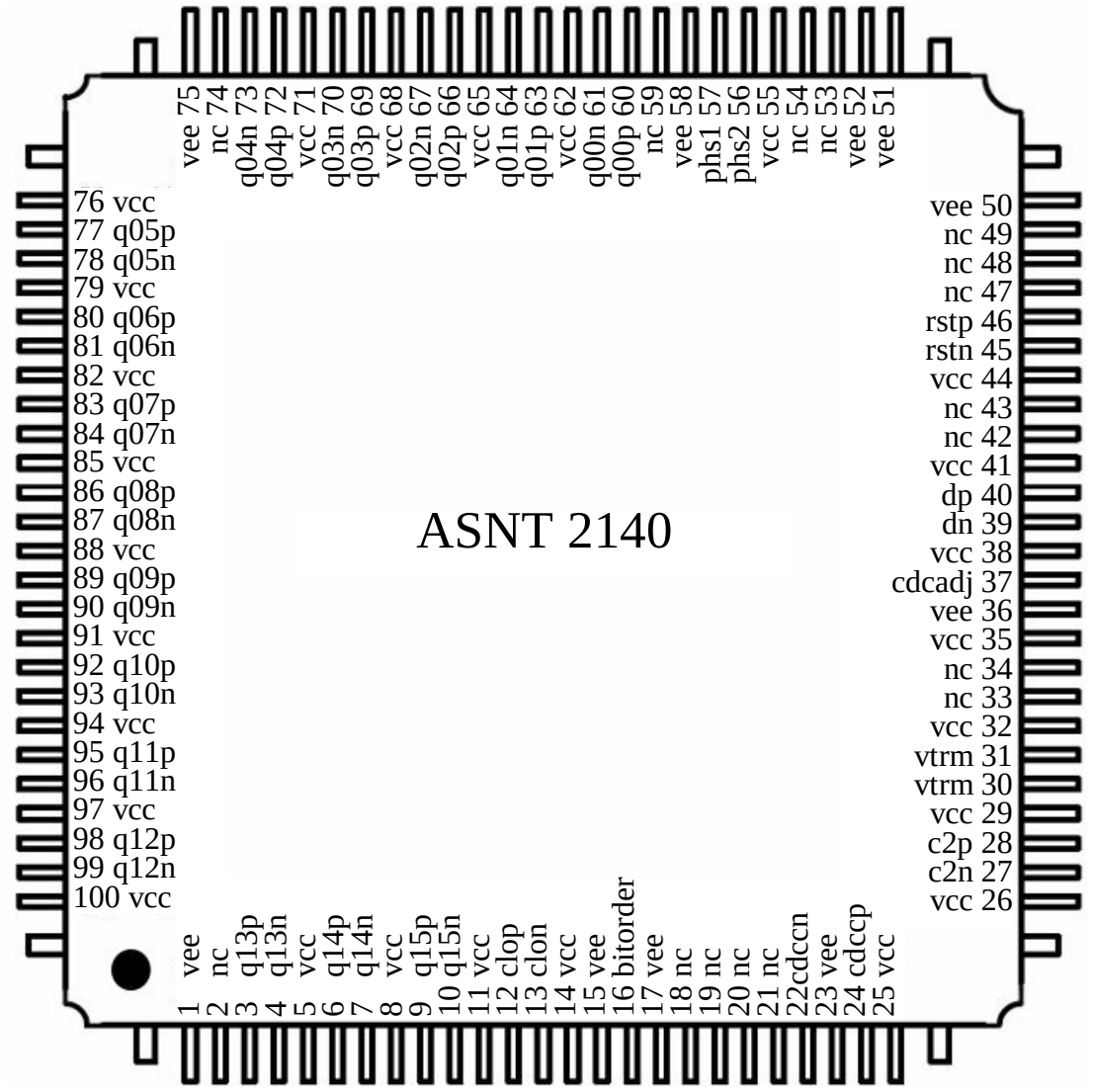
ASNT2140-KMA

DC-to-32*Gbps* Programmable DDR Demultiplexer 1:16 / Deserializer

- Programmable digital deserializer 1-to-16
- Supports data rates from DC to 32*Gb/s* in DDR clocking mode
- CML input data buffer
- CML input sampling clock buffer
- 16-bit parallel LVDS output data interface
- LVDS output forwarded clock-divided-by-16 with a selectable phase
- Divider external reset for synchronization of multiple devices
- Single +3.3*V* power supply
- Industrial temperature range
- Power consumption of 1350*mW* at maximum speed
- Custom 100-pin CQFP package (13*mm* x 13*mm*)



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DESCRIPTION

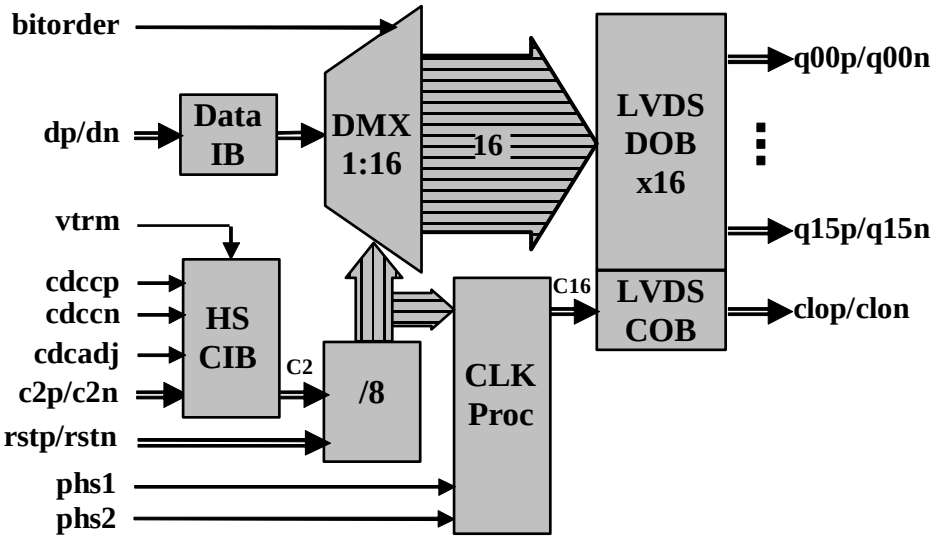

Fig. 1. Functional Block Diagram

ASNT2140-KMA is a high-speed DDR (dual data rate) digital 1-to-16 demultiplexer (DMX) / deserializer. The IC shown in Fig. 1 functions seamlessly over the specified range of data rates (f_{bit}).

The main function of the IC is to demultiplex a high-speed serial bit stream running at f_{bit} into 16 parallel data channels running at a bit rate of $f_{bit}/16$. It accepts a high-speed data transmitted over a controlled impedance media of 50*Ohm*. The transmission media can be a printed circuit board or copper coaxial cables. The functional distance of the data transfer is dependent upon the attenuation characteristics of the transportation media and the degree of noise coupling to the signaling environment.

During normal operation, the deserializer's CML data input buffer (Data IB) accepts a HS serial input data signal dp/dn and delivers it to the demultiplexer's core (DMX1:16) for deserialization. A half-rate CML sampling clock (a full-rate clock divided by 2) must be provided by an external source to the inputs c2p/c2n of the high-speed clock input buffer (HS CIB) where it is routed to the internal divider-by-8 (/8). The high-speed CML data and clock input buffers provide on-chip 50*Ohm* termination and are designed to be driven by devices with 50*Ohm* source impedance. The duty cycle of the internal clock c2 can be adjusted either through a single ended control pin cdcadj or through a dual control port cdccp/cdccn. The clock input buffer uses a separate positive supply vtrm for additional common mode voltage adjustment.

The divider provides signaling for DMX1:16 and produces a divided-by-16 full-rate forwarded clock C16 for the low-speed LVDS-compliant clock output buffer (LVDS COB). The divider can be preset to a certain initial state using external CML signals rstp/rstn. The phase of the low-speed forwarded clock clop/clon can be modified in 90° increments by utilizing pins phs1 and phs2 and the clock processing block (CLK Proc).

The deserialized digital words are delivered to the output parallel interface through 16 LVDS-compliant data output buffers LVDS DOBx16. By utilizing the pin bitorder, the deserializer can designate either q00p/q00n or q15p/q15n as the MSB (most significant bit that is delivered first to the serial interface), thus simplifying the interface between the demultiplexer and a following ASIC.

The chip uses a single +3.3*V* power supply and is characterized for junction temperature from −25°*C* to 125°*C*.

Data IB

The Data Input Buffer (Data IB) can accept high-speed serial data signals at its differential CML input port dp/dn. It can also accept a single-ended signal with a threshold voltage applied to the unused pin. HS DIB can handle a wide range of input signal amplitudes. The buffer utilizes on-chip single-ended 50*Ohm* termination to vcc for each input line.

HS CIB

The High-Speed Clock Input Buffer (HS CIB) can accept high-speed clock signals at its differential CML input port c2p/c2n. It can also accept a single-ended signal with a threshold voltage applied to the unused pin. HS CIB can handle a wide range of input signal amplitudes. The buffer utilizes on-chip single-ended 50*Ohm* termination to vtrm for each input line. This termination voltage can be adjusted within the range from vcc to vcc-0.8*V*.

The buffer provides two options for adjustment of the output signal duty cycle. The duty cycle can be adjusted by changing two control voltages cdccp and cdccn that affect the input signals c2p and c2n respectively.

It can also be adjusted using one control voltage cdcadj following the diagram shown in Fig. 2. Here red lines correspond to the dp input, blue lines correspond to the dn input, solid lines represent typical conditions while dotted and dashed lines represent slow and fast conditions respectively.

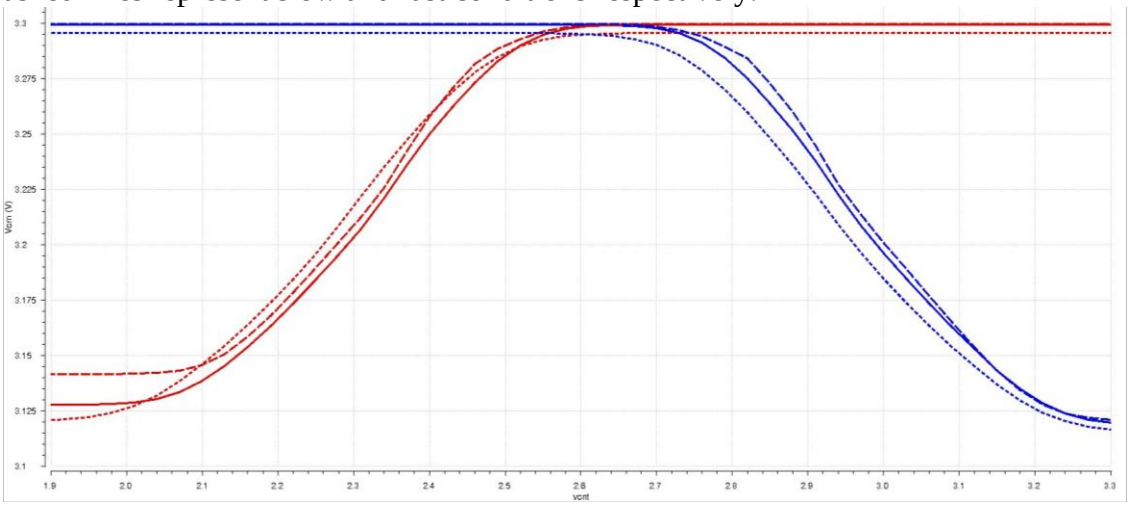

Fig. 2. Duty Cycle Control Diagram

It should be noted that only one control option should be activated at a certain time. Either cdccp/cdccn or cdcadj pins should be left not connected or AC-terminated with 50*Ohm* loads. Otherwise, the two internal control circuits interact and the desired result cannot be achieved.

/8

The Divider-by-8 (/8) includes three divide-by-2 circuits connected in series. The half-speed clock C2 is routed internally to the first divide-by-2 circuit and outside of the block to MUX16:1 as a sampling clock. Other divided down clock signals are formed and routed to MUX16:1 in a similar fashion. C16 is passed on to LVDS COB to become the output low-speed forwarded clock signal clop/clon.

The divider can be preset to a “0” state using external differential CML signals rstp/rstn that have on-chip 50*Ohm* termination to vcc. The reset circuitry can operate at high speed and features internal retiming by the

falling edge of half-rate clock. The desired phase relation between the reset signal and the sampling input clock c2p/c2n is illustrated by Fig. 3.

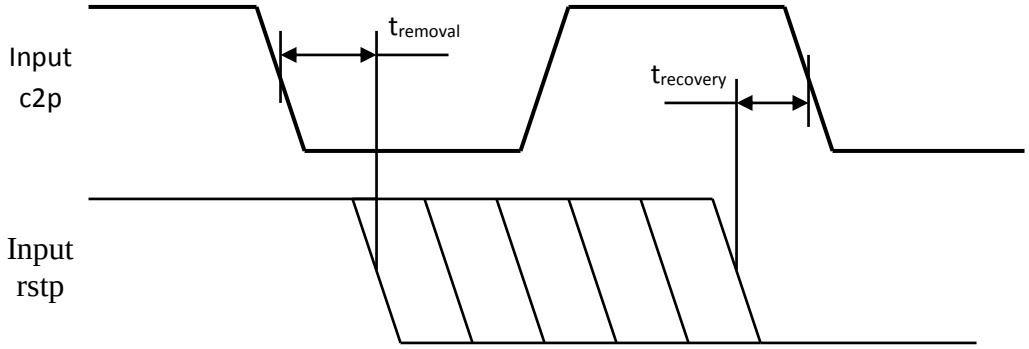

Fig. 3. Reset Timing Diagram

Recovery ($t_{recovery}$) and removal ($t_{removal}$) times depend on the input reset signal slew rate, the process corner, and the die temperature. Maximum required values are $t_{removal}$ = 33*ps* and $t_{recovery}$ = -18*ps*.

DMX1:16

The 1-to-16 demultiplexer (DMX1:16) utilizes the tree-type architecture and latches in the data stream from Data IB on both edges of the half-rate clock signal that is supplied by the divider /8. The high speed data signal is subsequently demultiplexed down and delivered to LVDS data output buffers (LVDS DOBx16) as16-bit wide parallel words.

CLK Proc

By utilizing the 3.3*V* CMOS control pins phs1 and phs2, the phase of the main low-speed forwarded clock output signal clop/clon can be selected in accordance with the table below.

Table 1. Clock Phase Selection

phs1	phs2	C16 phase
vee (default)	vee (default)	270°
vee	vcc	180°
vcc	vee	90°
vcc	vcc	0°

LVDS DOBx16

LVDS data output buffers (LVDS DOBx16) accept 16-bit wide words from DMX1:16 and convert them into sixteen LVDS output signals. Each proprietary low-power LVDS output buffer utilizes a special architecture that ensures operation at bit rates up to 2*Gb/s* with a low power consumption level of 30*mW*. The buffer satisfies all the requirements of the IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995. The block also provides a bit order selection under control of the external 3.3*V* CMOS signal bitorder. The first input serial bit (MSB) is assigned to q15p/q15n at bitorder = "0" (default) or to q00p/q00n at bitorder = "1".

LVDS COB

The LVDS clock output buffer (LVDS COB) utilizes a faster version of the same proprietary output buffer as in DOBx16. It receives the C16 clock signal from the Clk Proc and converts it into the LVDS output forwarded clock signal clop/clon. The phase of clop/clon can be adjusted as described above.

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Input Timing

Reliable latching of the incoming HS data dp/dn requires a certain phase relation between the input data and the half-rate input clock c2p/c2n that is specified in Table 2 and illustrated by Fig. 4.

Table 2. Input High-Speed Data to Input High-Speed Clock Phase Delay

Maximum required setup time, *ps*	Maximum required hold time, *ps*
-10	20

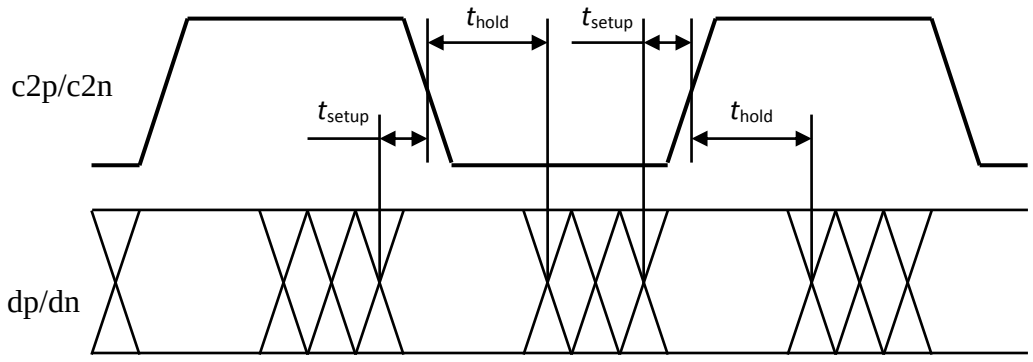

Fig. 4. Input Timing Diagram

Output Timing

The phase relation between the output LVDS data qXXp/qXXn and the divided-by-16 full-rate output forwarded clock clop is illustrated by Fig. 5, when phs1 = "0" and phs2 = "1". Data-to-clock delay (t_{qc}) varies from 48*ps* to 99*ps* depending on the process corner and the die temperature.

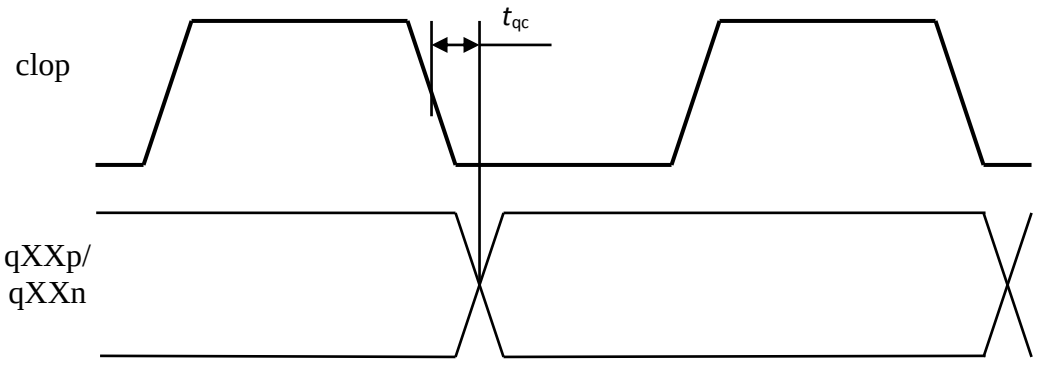

Fig. 5. Output Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 3 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vee).

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Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vcc)		+3.6	*V*
Power Consumption		1.0	*W*
RF Input Voltage Swing (SE)		1.2	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTIONS

Supply and Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Positive power supply (+3.3*V*)	5, 8, 11, 14, 25, 26, 29, 32, 35, 38, 41, 44, 55, 62, 65, 68, 71, 76, 79, 82, 85, 88, 91, 94, 97, 100
vee	Negative power supply (GND or 0*V*)	1, 15, 17, 23, 36, 50, 51, 52, 58, 75
vtrm	Termination voltage for clock inputs (default – vcc, minimum – vcc-0.8*V*)	30, 31
nc	Unconnected pin	2, 18, 19, 20, 21, 33, 34, 42, 43, 47, 48, 49, 53, 54, 59, 74

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-Speed I/Os			
dp	40	Input	CML differential data inputs with internal SE 50*Ohm* termination to vcc
dn	39		
c2p	28	Input	CML differential sampling clock inputs with internal SE 50*Ohm* termination to vtrm
c2n	27		
rstp	46	Input	CML differential internal divider reset inputs with internal SE 50*Ohm* termination to vcc
rstn	45		
Controls			
bitorder	16	CMOS input	Output bit order selection (default: low, the first serial bit (MSB) is q15p/q15n; active: high, MSB is q00p/q00n)
cdcadj	37	Analog input	Internal half-rate clock duty cycle adjustment, SE
cdccp	24	Analog input	Internal half-rate clock duty cycle adjustment, Differential
cdccn	22		
phs1	57	LS In., CMOS	Low-speed output forwarded clock clop/clon phase selection (default: both low)
phs2	56		

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TERMINAL			DESCRIPTION
Name	No.	Type	
Low-Speed I/Os			
q15n	10	Output	LVDS data outputs
q15p	9		
q14n	7		
q14p	6		
q13n	4		
q13p	3		
q12n	99		
q12p	98		
q11n	96		
q11p	95		
q10n	93		
q10p	92		
q09n	90		
q09p	89		
q08n	87		
q08p	86		
q07n	84		
q07p	83		
q06n	81		
q06p	80		
q05n	78		
q05p	77		
q04n	73		
q04p	72		
q03n	70		
q03p	69		
q02n	67		
q02p	66		
q01n	64		
q01p	63		
q00n	61		
q00p	60		
clop	12	Output	LVDS low-speed full-rate forwarded clock outputs. Can transmit four different clock phases as defined in Table 1
clon	13		

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vcc	+3.14	+3.3	+3.47	*V*	±5%
vtrm	vcc		vcc-0.8	*V*	
vee		0.0		*V*	External ground
*I*vcc		409		*mA*	
Power consumption		1350		*mW*	
Junction temperature	-25	50	125	*°C*	
HS Input Data (dp/dn)					
Maximum Data rate	32			*Gbps*	
Minimum Data rate		-		*Gbps*	
Swing (Diff or SE)	0.02		1.0	*V*	Peak-to-peak
CM Voltage Level	vcc-0.8		vcc	*V*	
HS Input Sampling Clock (c2p/c2n)					
Maximum Frequency	16			*GHz*	
Minimum Frequency		-		*GHz*	
Swing (Diff or SE)	0.2		1.0	*V*	Peak-to-peak
CM Voltage Level	vcc -0.8		vcc	*V*	
Duty Cycle	40	50	60	*%*	
LS Output Data (q00p/q00n-q15p/q15n)					
Maximum Data Rate	2			*Gbps*	
Minimum Data Rate		-		*Gbps*	
Interface		LVDS			Meets the IEEE Std. 1596.3-1996
LS Output Forwarded Clocks (clop/clon)					
Maximum Frequency	2			*GHz*	
Minimum Frequency		-		*GHz*	
Interface		LVDS			Meets the IEEE Std. 1596.3-1996
CMOS Control Inputs (bitorder, phs1, phs2)					
Logic “1” level	vcc -0.4			*V*	
Logic “0” level			vee +0.4	*V*	
Analog Control Inputs (cdcadj, cdccp/cdccn)					
Voltage range	vee		vcc	*V*	
cdcadj termination		22 / 5.6		*KOhm*	to vee / vcc
cdccp termination		0.95		*KOhm*	to c2p
cdccn termination		0.95		*KOhm*	to c2n

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PACKAGE INFORMATION

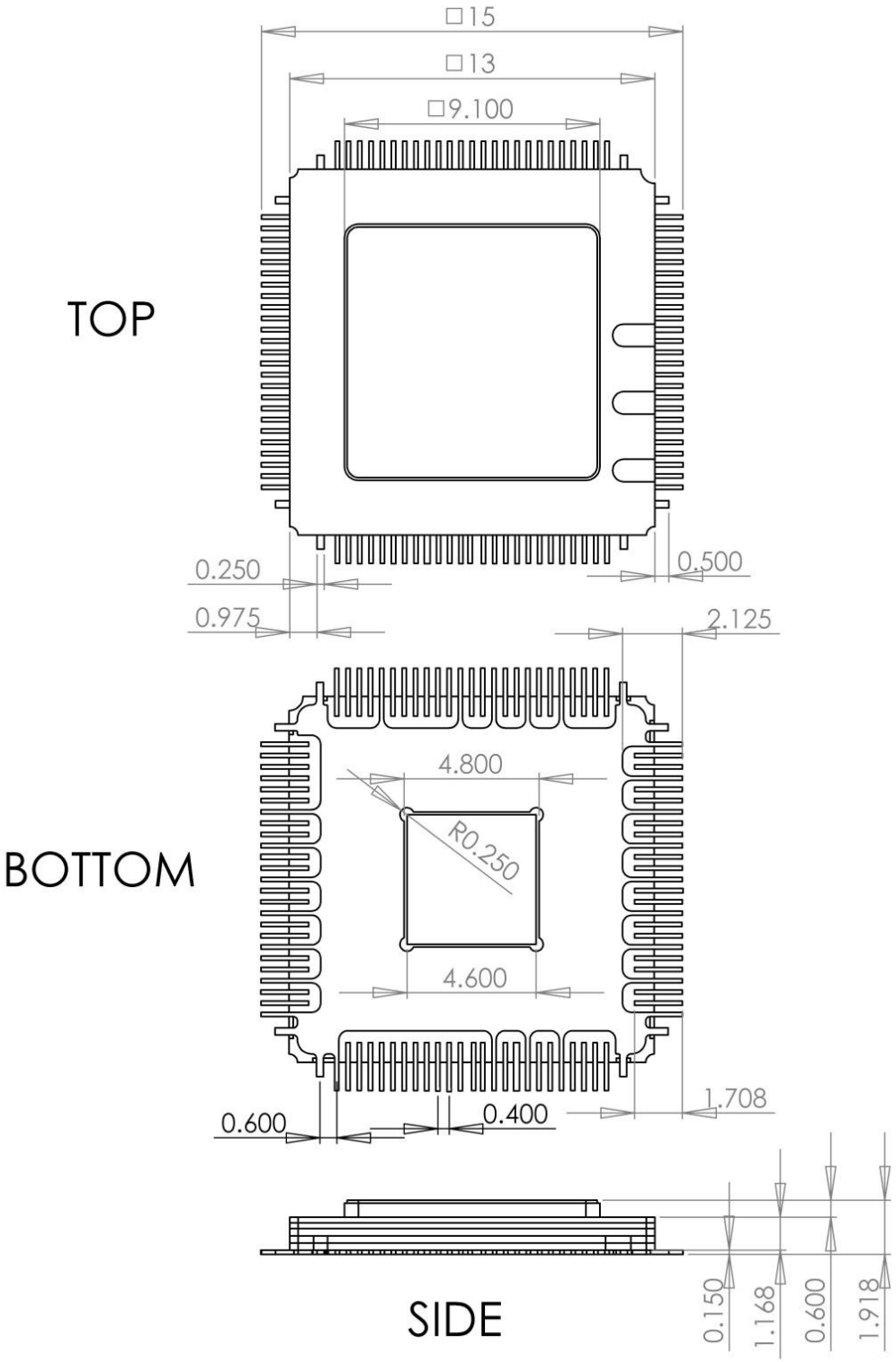

Fig. 6. CQFP 100-Pin Package Drawing (All Dimensions in mm)

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The chip die is housed in a custom 100-pin CQFP package shown in Fig. 6. The package's leads will be trimmed to a length of 1.0mm. After trimming, the package's leads will be further processed as follows:

1. The lead's gold plating will be removed per the following sections of J-STD-001D:
   - 3.9.1 Solderability
   - 3.2.2 Solder Purity Maintenance
   - 3.9.2 Solderability Maintenance
   - 3.9.3 Gold Removal
2. The leads will be tinned with Sn63Pb37 solder

The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the vcc plain, which is power for a positive supply.

The part's identification label is ASNT2140-KMA. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

REVISION HISTORY

Revision	Date	Changes
1.6.2	08-2020	Corrected terminal descriptions for vtrm, dp/dn, c2p/c2n
1.5.2	05-2020	Updated Package Information
1.4.2	07-2019	Updated Letterhead
1.4.1	02-2016	Updated frequency of operation Updated Electrical characteristics table
1.3.1	07-2015	Corrected pinout diagram (pins 52 and 53) Corrected Terminal Functions
1.2.1	07-2015	Updated frequency of operation Updated Electrical characteristics table
1.1.1	05-2015	Updated Description Corrected Terminal Functions table Revised package information section Corrected format
1.0.1	03-2015	Updated pin out diagram Updated Terminal Functions table Included vtrm function description
1.0.0	11-2014	Preliminary release