

MOSFET - Power, Single P-Channel, WDFN8 -100 V, 120 mΩ, -13 A



ON Semiconductor®

www.onsemi.com

NTTFS115P10M5

Features

- Small Footprint (3.3 x 3.3 mm) for Compact Design
- These Devices are non-ESD Protected
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	-100	V
Gate-to-Source Voltage	V _{GS}	±20	V
Continuous Drain Current R _{θJC} (Note 2)	I _D	T _C = 25°C	-13
		T _C = 100°C	-8.0
Power Dissipation R _{θJC} (Note 2)	P _D	T _C = 25°C	41
		T _C = 100°C	16
Continuous Drain Current R _{θJA} (Notes 1, 2)	I _D	T _A = 25°C	-2.0
		T _A = 100°C	-1.1
Power Dissipation R _{θJA} (Notes 1, 2)	P _D	T _A = 25°C	0.9
		T _A = 100°C	0.3
Pulsed Drain Current	T _A = 25°C, t _p = 10 μs	I _{DM}	-137
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +150	°C
Source Current (Body Diode)	I _S	-34	A
Single Pulse Drain-to-Source Avalanche Energy (I _{L(pk)} = -9.1 A)	E _{AS}	41	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)	T _L	260	°C

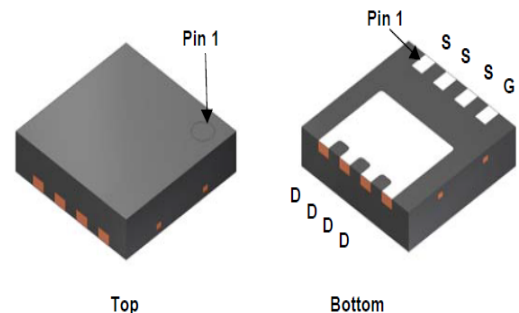
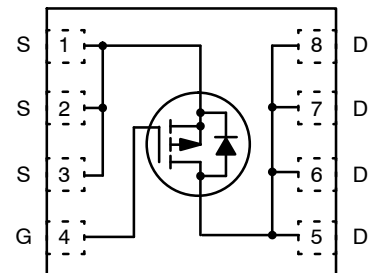
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State (Note 2)	R _{θJC}	3.0	°C/W
Junction-to-Ambient - Steady State (Note 2)	R _{θJA}	134	

1. Surface-mounted on FR4 board using a 1 in² pad size, 1 oz Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

V _{(BR)DSS}	R _{DS(on)} MAX	I _D MAX
-100 V	120 mΩ @ -10 V	-13 A
	254 mΩ @ -6 V	



WDFN8
CASE 511DH

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

NTTFS115P10M5

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	-100			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 250\ \mu\text{A}$, ref to 25°C		-67		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = -80\text{ V}$	$T_J = 25^\circ\text{C}$		-1	μA
			$T_J = 125^\circ\text{C}$		-100	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -45\ \mu\text{A}$	-2.0	-3.0	-4.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	$I_D = 250\ \mu\text{A}$, ref to 25°C		6.2		mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -2.4\text{ A}$		97	120	$\text{m}\Omega$
		$V_{GS} = -6\text{ V}, I_D = -1.6\text{ A}$		127	254	
Forward Transconductance	g_{FS}	$V_{DS} = -10\text{ V}, I_D = -2.1\text{ A}$		5.5		S
Gate-Resistance	R_G	$T_A = 25^\circ\text{C}$		3.5		Ω

CHARGES & CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = -50\text{ V}$		637		pF	
Output Capacitance	C_{OSS}			93.5			
Reverse Transfer Capacitance	C_{RSS}			4.5			
Total Gate Charge	$Q_G(\text{TOT})$	$V_{GS} = -6\text{ V}, V_{DS} = -50\text{ V}, I_D = -2.4\text{ A}$		5.7		nC	
Total Gate Charge	$Q_G(\text{TOT})$		$V_{GS} = -10\text{ V}, V_{DS} = -50\text{ V}, I_D = -2.4\text{ A}$		9.2		
Gate-to-Source Charge	Q_{GS}				3.0		
Gate-to-Drain Charge	Q_{GD}				1.3		
Plateau Voltage	V_{GP}				4.4		

SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -10\text{ V}, V_{DS} = -50\text{ V}, I_D = -2.4\text{ A}, R_G = 2.5\ \Omega$		8.7		ns
Rise Time	t_r			2.1		
Turn-Off Delay Time	$t_{d(OFF)}$			13.4		
Fall Time	t_f			4.1		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = -2.4\text{ A}$	$T_J = 25^\circ\text{C}$		0.84	1.2	V
			$T_J = 125^\circ\text{C}$		0.71		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, \text{d}I_S/\text{d}t = 300\text{ A}/\mu\text{s}, I_S = -1.2\text{ A}$		28.7		ns	
Reverse Recovery Charge	Q_{RR}			87.6		nC	
Charge Time	t_a			18.4		ns	
Discharge Charge	t_b			10.4		ns	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures.

4. Pulse Test: Pulse Width < 300 μs . Duty Cycle < 2%.

5. Maximum current for pulses as long as 1s is higher but is independent on pulse duration or duty cycles.

TYPICAL CHARACTERISTICS

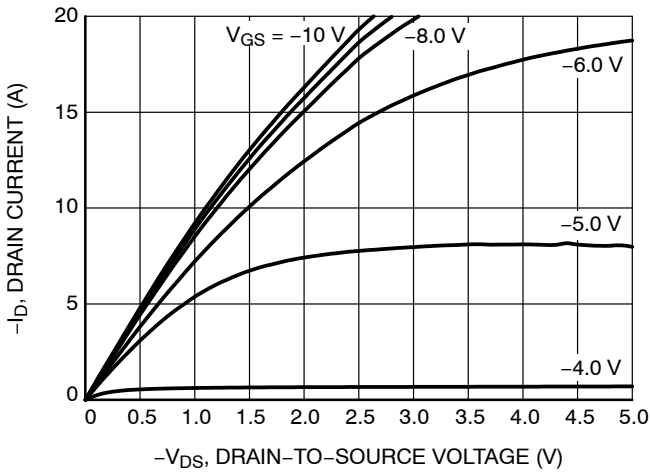


Figure 1. On-Region Characteristics

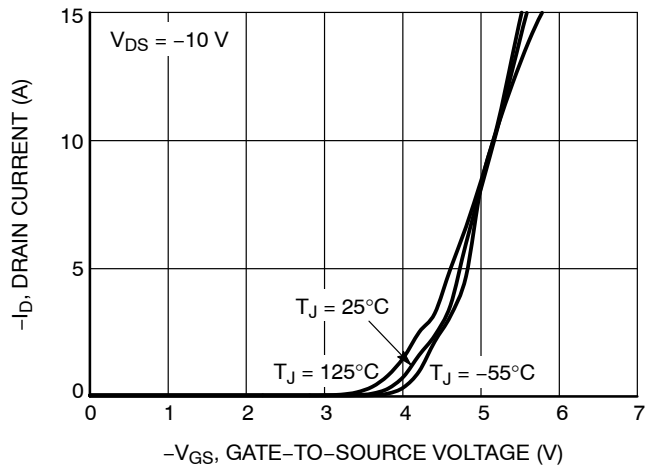


Figure 2. Transfer Characteristics

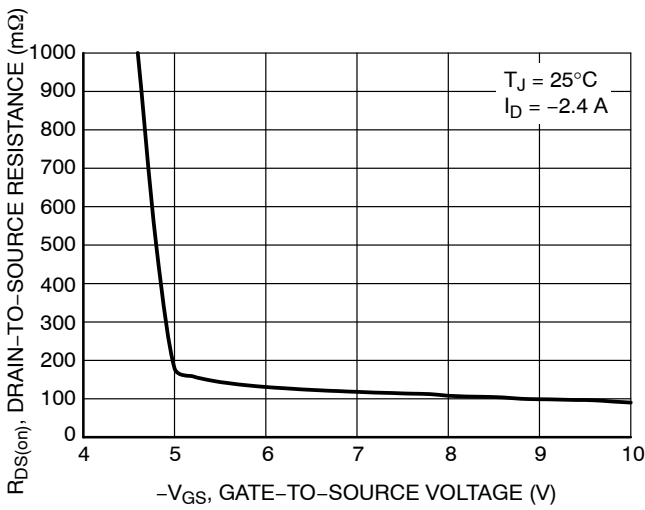


Figure 3. On-Resistance vs. Gate-to-Source Voltage

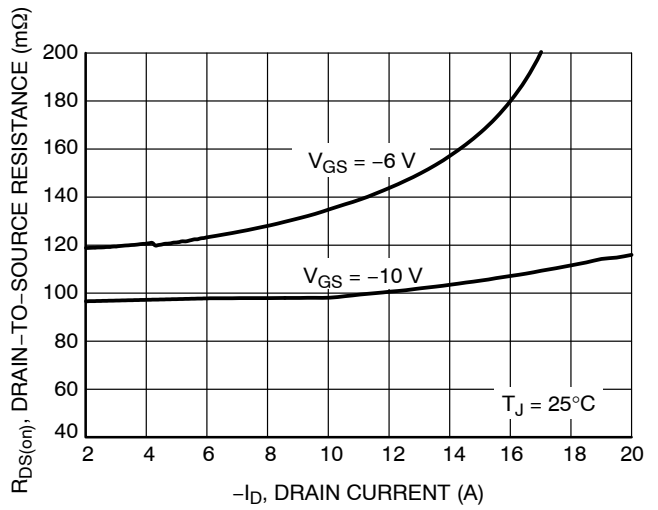


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

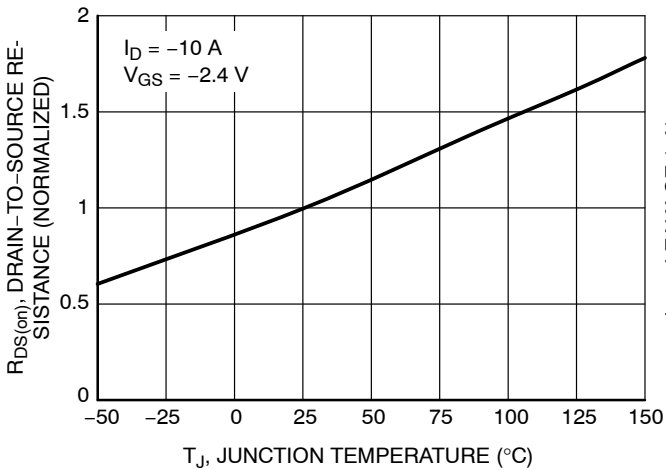


Figure 5. On-Resistance Variation with Temperature

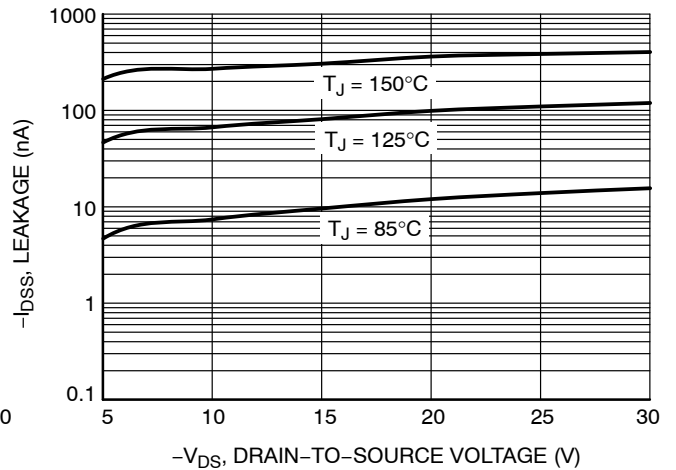


Figure 6. Drain-to-Source Leakage Current vs. Voltage

NTTFS115P10M5

TYPICAL CHARACTERISTICS

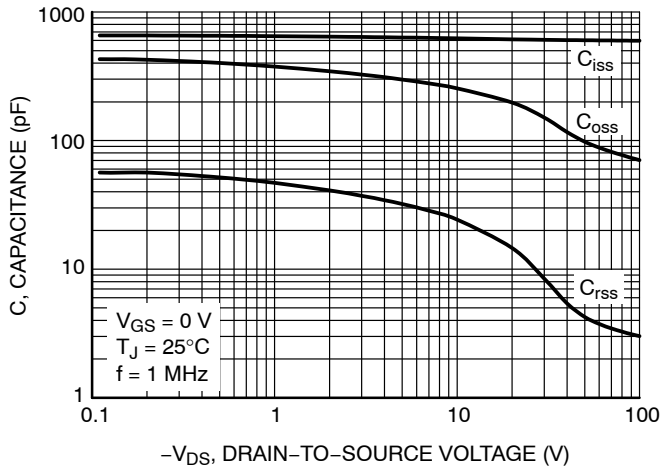


Figure 7. Capacitance Variation

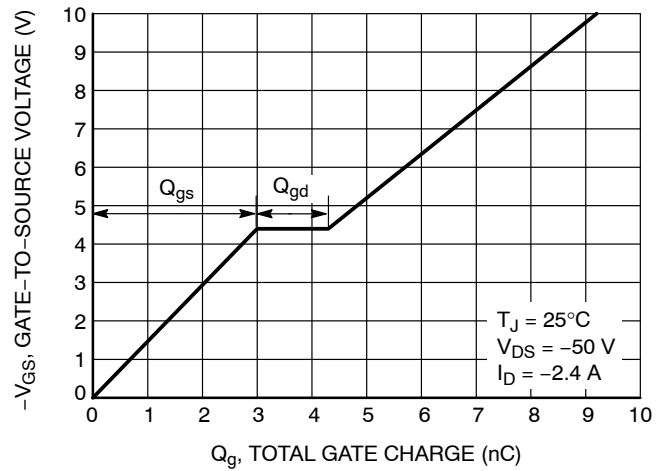


Figure 8. Gate-to-Source vs. Total Charge

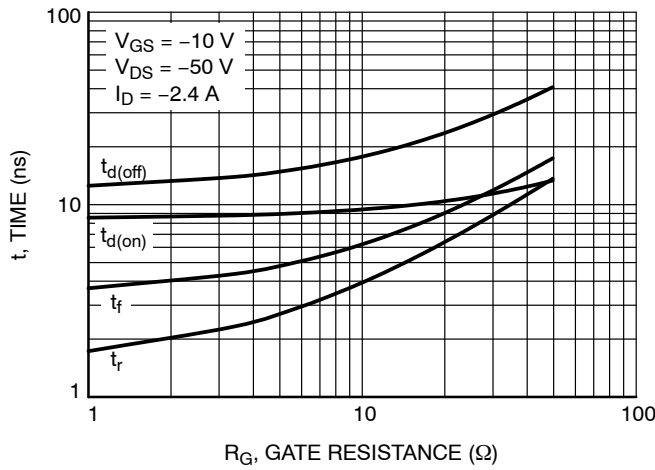


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

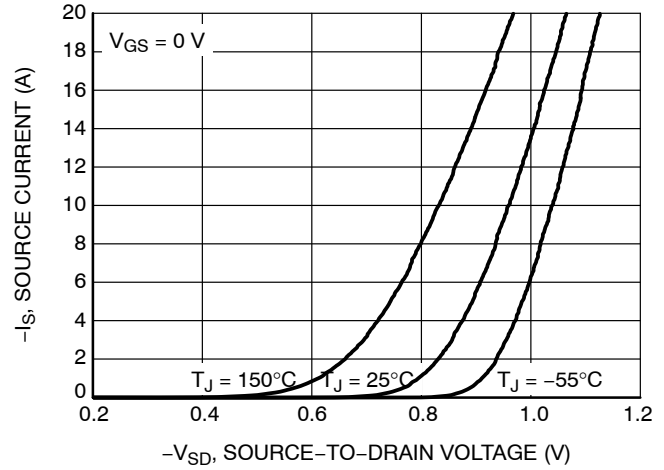


Figure 10. Diode Forward Voltage vs. Current

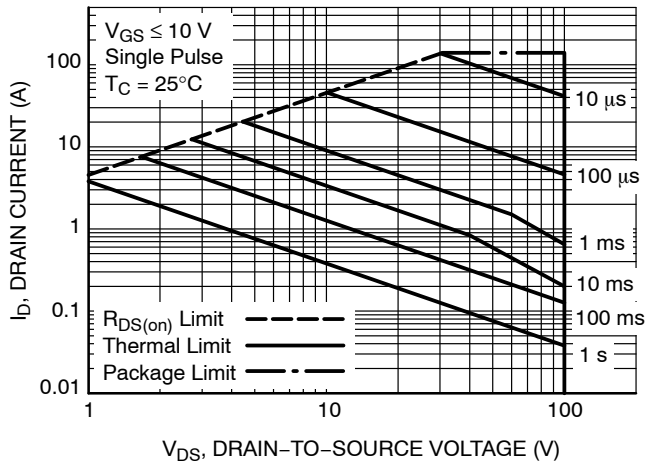


Figure 11. Maximum Rated Forward Biased Safe Operating Area

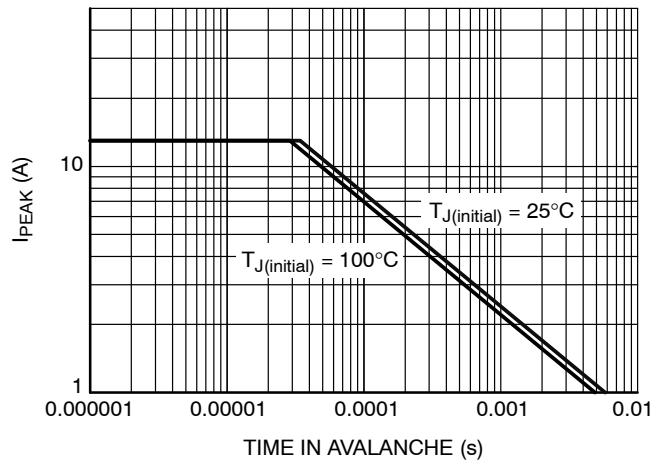


Figure 12. I_{PEAK} vs. Time in Avalanche

NTTFS115P10M5

TYPICAL CHARACTERISTICS

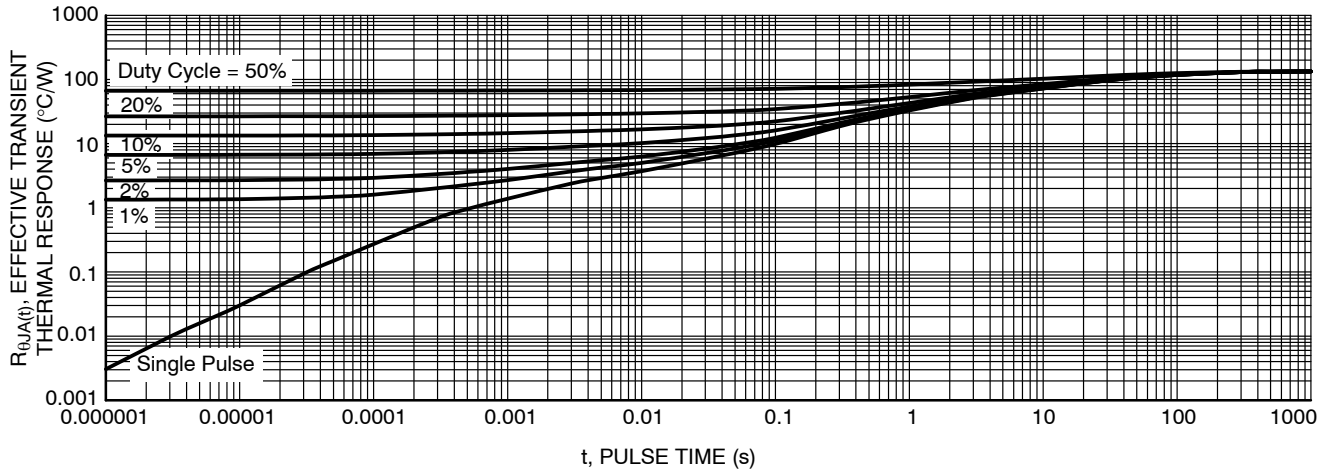


Figure 13. Thermal Response

DEVICE ORDERING AND MARKING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Shipping [†]
NTTFS115P10M5	115P10M5	WDFN8 (Pb-Free)	13"	12 mm	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

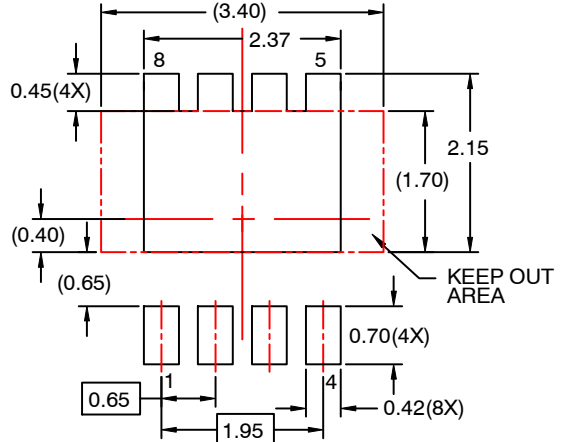
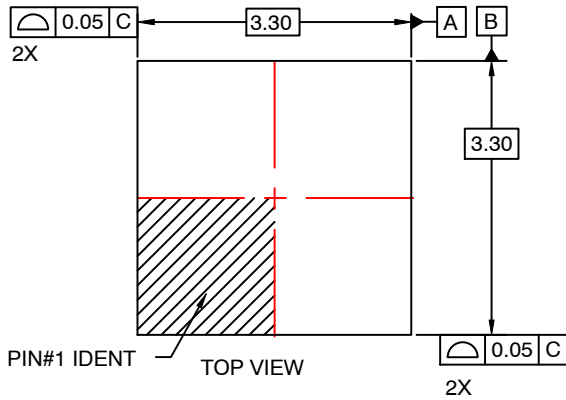
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®



WDFN8 3.3x3.3, 0.65P
CASE 511DH
ISSUE O

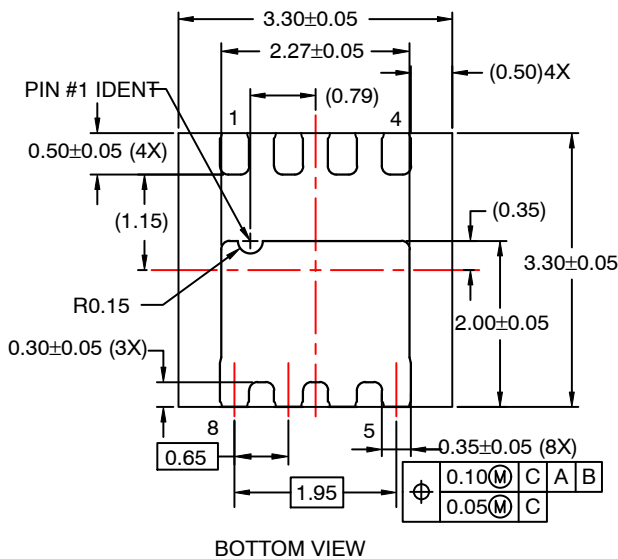
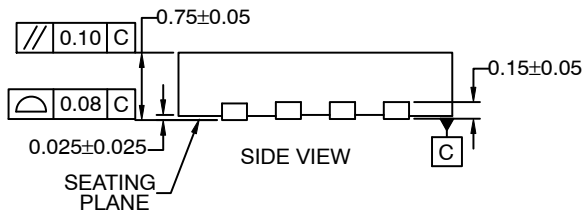
DATE 31 JUL 2016



RECOMMENDED LAND PATTERN

NOTES:

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.



BOTTOM VIEW

DOCUMENT NUMBER:	98AON13625G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	WDFN8 3.3X3.3, 0.65P	PAGE 1 OF 1

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales