

# NTMFS4854NS

## Power MOSFET

25 V, 149 A, Single N-Channel, SO-8 FL

### Features

- Accurate, Lossless Current Sensing
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

- CPU Power Delivery
- DC-DC Converters
- Low Side Switching

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	$V_{DSS}$	25	V	
Gate-to-Source Voltage	$V_{GS}$	$\pm 16$	V	
Continuous Drain Current $R_{\theta JA}$ (Note 1)	$I_D$	$T_A = 25^\circ\text{C}$	24.4	A
		$T_A = 85^\circ\text{C}$	17.6	
Power Dissipation $R_{\theta JA}$ (Note 1)	$P_D$	$T_A = 25^\circ\text{C}$	2.31	W
Continuous Drain Current $R_{\theta JA}$ (Note 2)	$I_D$	$T_A = 25^\circ\text{C}$	15.2	A
		$T_A = 85^\circ\text{C}$	11	
Power Dissipation $R_{\theta JA}$ (Note 2)	$P_D$	$T_A = 25^\circ\text{C}$	0.9	W
Continuous Drain Current $R_{\theta JC}$ (Note 1)	$I_D$	$T_C = 25^\circ\text{C}$	149	A
		$T_C = 85^\circ\text{C}$	107.5	
Power Dissipation $R_{\theta JC}$ (Note 1)	$P_D$	$T_C = 25^\circ\text{C}$	86.2	W
Pulsed Drain Current	$I_{DM}$	298	A	
Operating Junction and Storage Temperature	$T_J, T_{STG}$		-55 to +150	$^\circ\text{C}$
Source Current (Body Diode)	$I_S$	71	A	
Drain to Source DV/DT	dV/dt	6	V/ns	
Single Pulse Drain-to-Source Avalanche Energy ( $T_J = 25^\circ\text{C}$ , $V_{DD} = 30\text{ V}$ , $V_{GS} = 10\text{ V}$ , $I_L = 20\text{ A}_{pk}$ , $L = 1.0\text{ mH}$ , $R_G = 25\ \Omega$ )	EAS	200	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

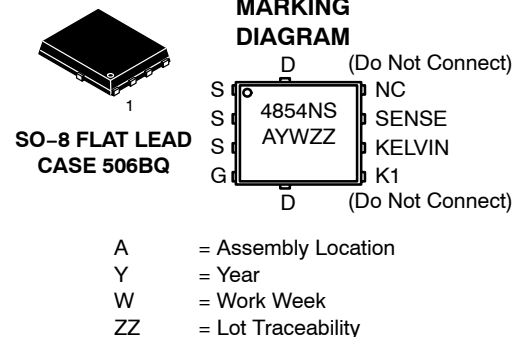
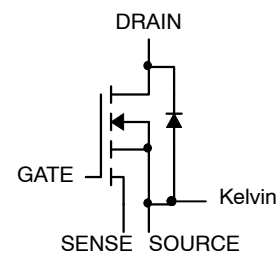
1. Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
2. Surface-mounted on FR4 board using the minimum recommended pad size.



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$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	$I_D$ MAX
25 V	2.5 m $\Omega$ @ 10 V	149 A
	3.9 m $\Omega$ @ 4.5 V	119 A



### ORDERING INFORMATION

Device	Package	Shipping†
NTMFS4854NST1G	SO-8 FL (Pb-Free)	1500 Tape / Reel
NTMFS4854NST3G	SO-8 FL (Pb-Free)	5000 Tape / Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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## THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	1.45	°C/W
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	54	
Junction-to-Ambient – Steady State (Note )	$R_{\theta JA}$	138.7	

3. Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.

4. Surface-mounted on FR4 board using the minimum recommended pad size.

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	25			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			30		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}$	$T_J = 25^\circ\text{C}$		10	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		200	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 16\text{ V}$			$\pm 100$	nA

## ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.0		2.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			6.8		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 15\text{ A}$	$T_J = 25^\circ\text{C}$	1.5	2.5	m $\Omega$
			$T_J = 75^\circ\text{C}$	2.5	3.9	
			$T_J = 125^\circ\text{C}$	6.0	10	
			$T_J = 25^\circ\text{C}$	5.1	8.8	
Forward Transconductance	$g_{FS}$	$V_{DS} = 15\text{ V}, I_D = 15\text{ A}$		28		S

## CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 12\text{ V}$		4830		pF
Output Capacitance	$C_{OSS}$			1130		
Reverse Transfer Capacitance	$C_{RSS}$			550		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}; I_D = 30\text{ A}$		36	66	nC
Threshold Gate Charge	$Q_{G(TH)}$			4.7		
Gate-to-Source Charge	$Q_{GS}$			13		
Gate-to-Drain Charge	$Q_{GD}$			15		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 11.5\text{ V}, V_{DS} = 15\text{ V}; I_D = 30\text{ A}$		85		nC

## SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 15\text{ A}, R_G = 3.0\ \Omega$		20		ns
Rise Time	$t_r$			54		
Turn-Off Delay Time	$t_{d(OFF)}$			38		
Fall Time	$t_f$			45		

5. Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .

6. Switching characteristics are independent of operating junction temperatures.

7. With 0V potential from sense lead to source lead, i.e. using a virtual ground.

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## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>SWITCHING CHARACTERISTICS</b> (Note 6)						
Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 11.5\text{ V}, V_{DS} = 15\text{ V},$ $I_D = 15\text{ A}, R_G = 3.0\ \Omega$		11		ns
Rise Time	$t_r$			32		
Turn-Off Delay Time	$t_{d(OFF)}$			54		
Fall Time	$t_f$			34		

## DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V},$ $I_S = 30\text{ A}$	$T_J = 25^\circ\text{C}$		0.80	1.2	V
			$T_J = 125^\circ\text{C}$		0.65		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s},$ $I_S = 30\text{ A}$			36		ns
Charge Time	$t_a$				17		
Discharge Time	$t_b$				19		
Reverse Recovery Charge	$Q_{RR}$					33	

## PACKAGE PARASITIC VALUES

Source Inductance	$L_S$	$T_A = 25^\circ\text{C}$		0.65		nH
Drain Inductance	$L_D$			0.005		nH
Gate Inductance	$L_G$			1.84		nH
Gate Resistance	$R_G$			1.4		$\Omega$

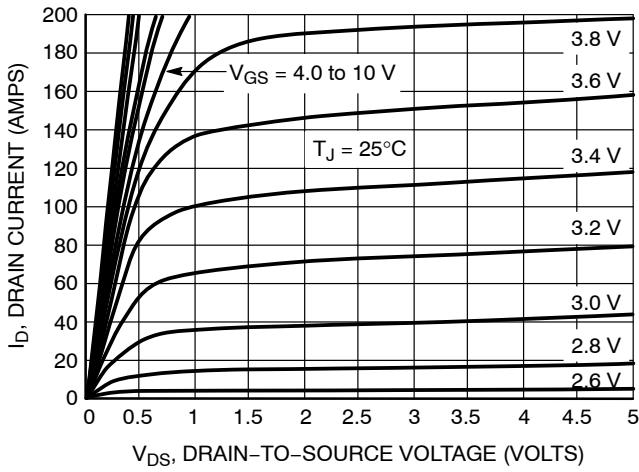
## CURRENT SENSE CHARACTERISTICS

Current Sensing Ratio	$I_{ratio}$	$V_{GS} = 5\text{ V}, 0\text{-}70^\circ\text{C}, 5\text{-}20\text{ A}$	374	399	424	
Current Sensing Ratio	$I_{ratio}$	$V_{GS} = 5\text{ V}, 0\text{-}70^\circ\text{C}, 1\text{-}5\text{ A}$	362	399	436	
Current Sense Temperature Coefficient (Note 7)				0.006		%/ $^\circ\text{C}$

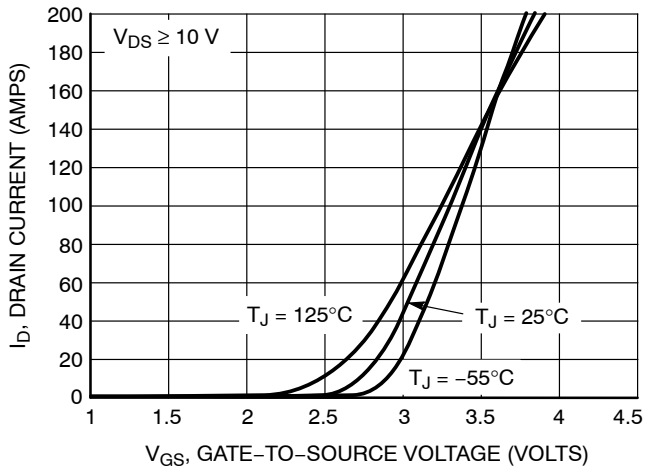
5. Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .
6. Switching characteristics are independent of operating junction temperatures.
7. With 0V potential from sense lead to source lead, i.e. using a virtual ground.

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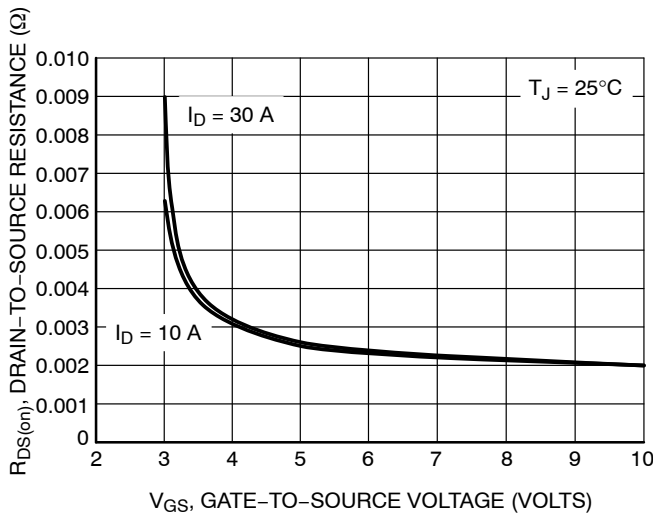
## TYPICAL PERFORMANCE CURVES



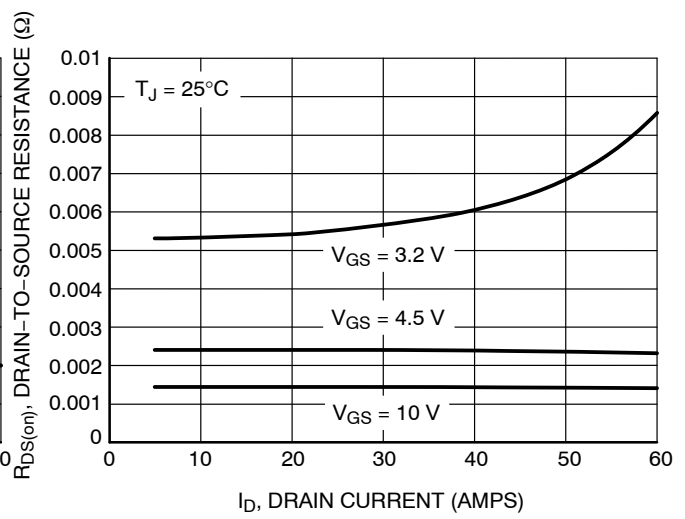
**Figure 1. On-Region Characteristics**



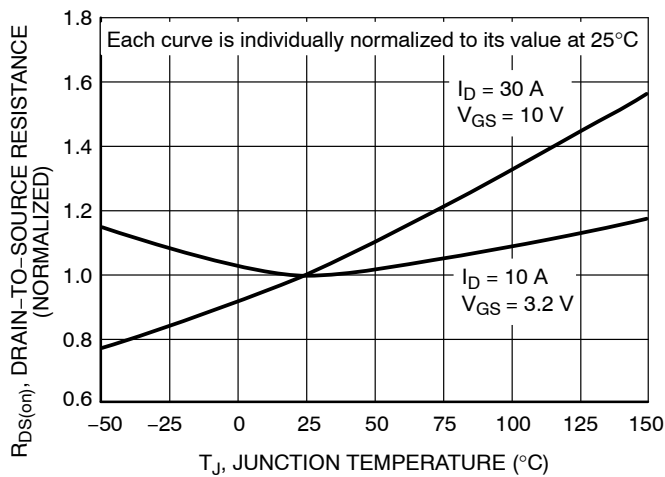
**Figure 2. Transfer Characteristics**



**Figure 3. On-Resistance vs. Gate-to-Source Voltage**



**Figure 4. On-Resistance vs. Drain Current and Gate Voltage**



**Figure 5. On-Resistance Variation with Temperature**

TYPICAL PERFORMANCE CURVES

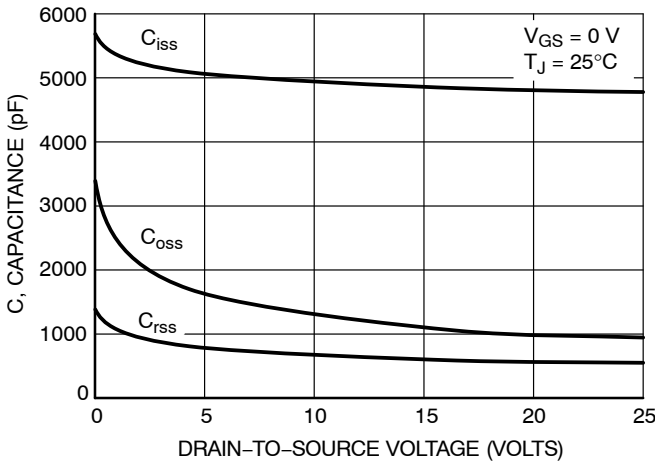


Figure 6. Capacitance Variation

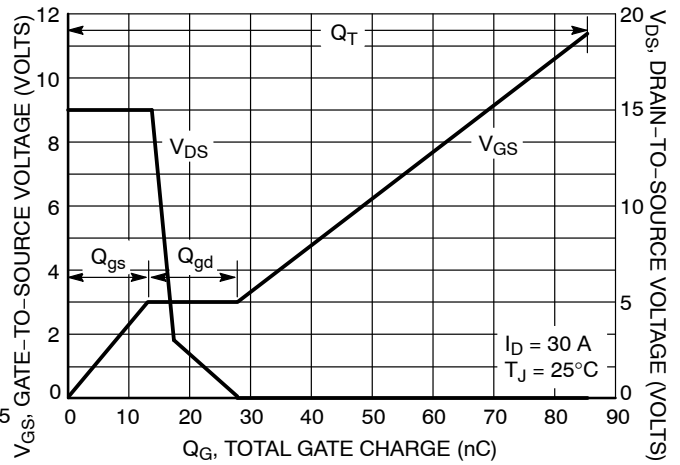


Figure 7. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge

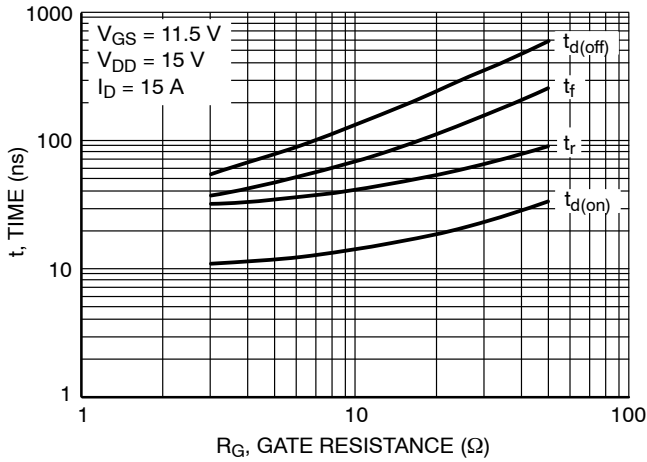


Figure 8. Resistive Switching Time Variation vs. Gate Resistance

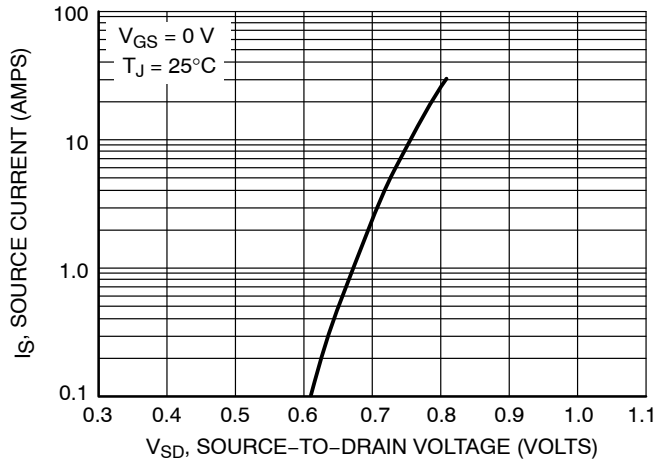


Figure 9. Diode Forward Voltage vs. Current

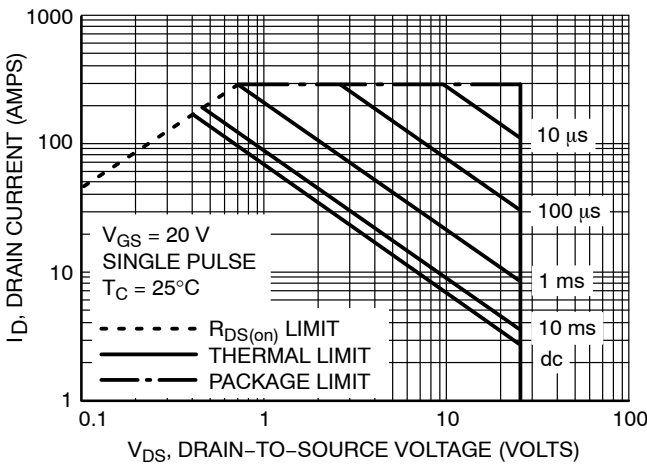


Figure 10. Maximum Rated Forward Biased Safe Operating Area

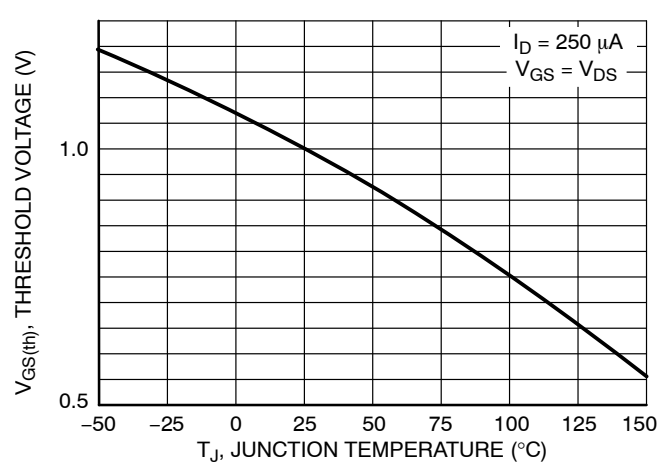


Figure 11. Threshold Voltage

# NTMFS4854NS

## TYPICAL CHARACTERISTICS

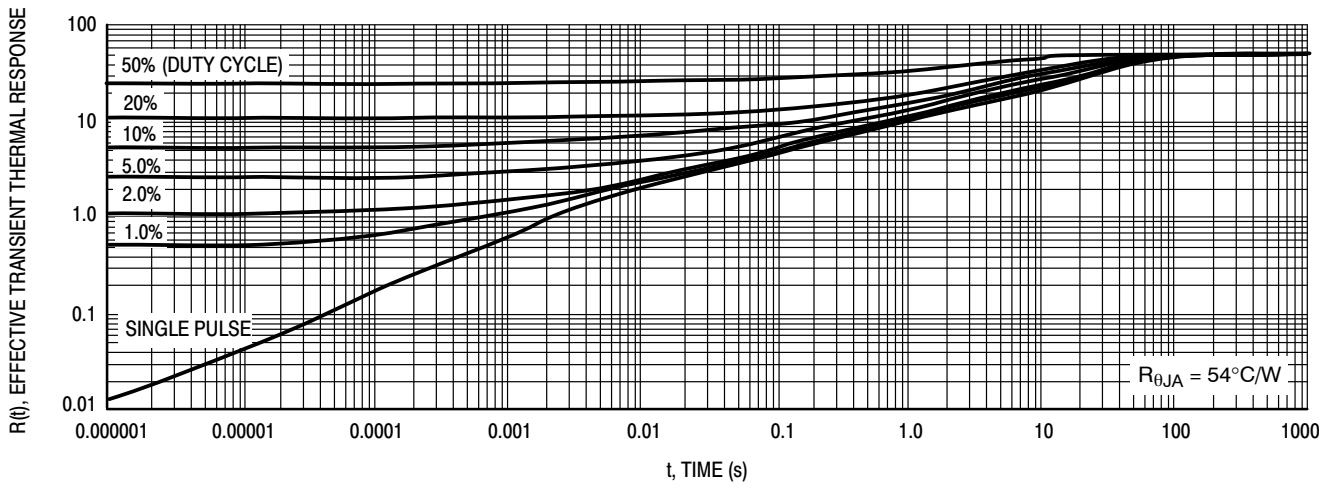
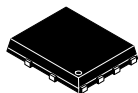


Figure 12. FET Thermal Response

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

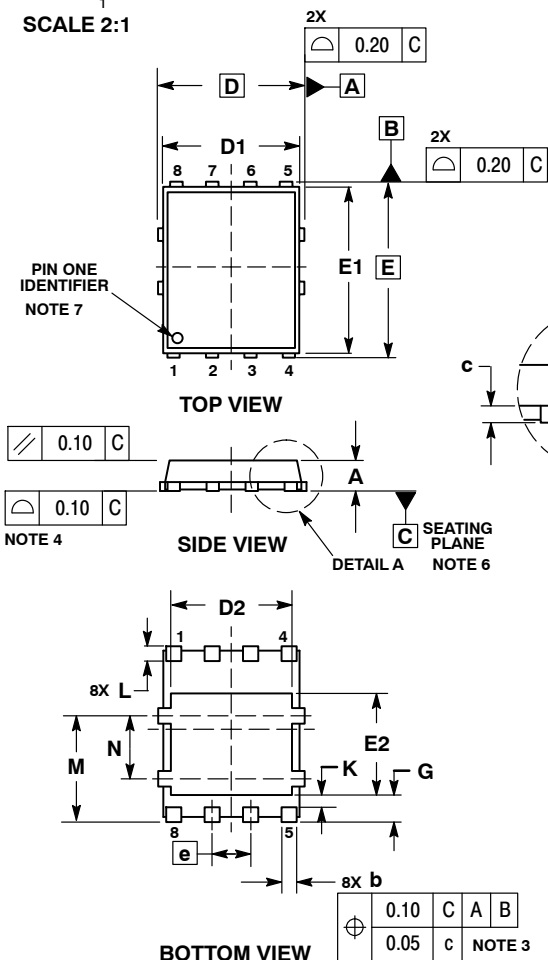
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1  
SCALE 2:1

## DFN8 5x6, 1.27P CASE 506BQ ISSUE C

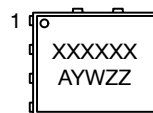
DATE 12 APR 2012



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. PROFILE TOLERANCE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINAL.
5. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
7. A VISUAL INDICATOR FOR PIN 1 MUST BE LOCATED IN THIS AREA.

### GENERIC MARKING DIAGRAM\*

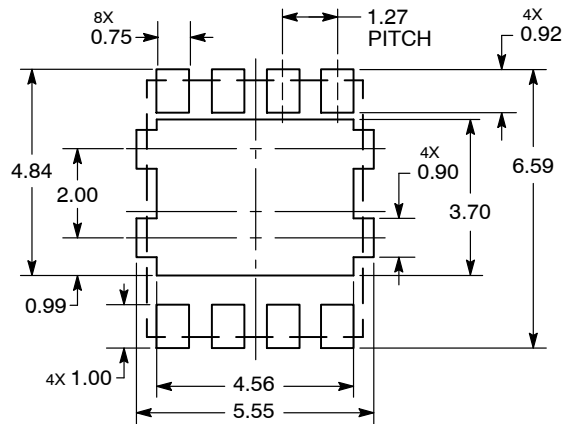


- XXXXXX = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 W = Work Week  
 ZZ = Lot Traceability

DIM	MILLIMETERS	
	MIN	MAX
A	0.90	1.10
A1	---	0.05
b	0.33	0.51
c	0.20	0.33
D	5.15 BSC	
D1	4.50	5.10
D2	3.90	4.30
E	6.15 BSC	
E1	5.50	6.10
E2	3.00	3.50
e	1.27 BSC	
G	0.80	1.20
h	---	12 °
K	0.20	---
L	0.51	0.71
M	3.25	3.75
N	1.80	2.20

\*This information is generic. Please refer to device data sheet for actual part marking.

### SOLDERING FOOTPRINT\*



DIMENSION: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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