Dual Very Low Noise Precision Operational Amplifier

Data Sheet

OP270

FEATURES

- **Very low noise density of 5 nV/√Hz at 1 kHz maximum**
- **Excellent input offset voltage of 75 µV maximum**
- **Low offset voltage drift of 1 µV/°C maximum**
- **Very high gain of 1500 V/mV minimum**
- **Outstanding CMR of 106 dB minimum**
- **Slew rate of 2.4 V/µs typical**
- **Gain bandwidth product of 5 MHz typical**
- **Industry-standard 8-lead dual pinout**

FUNCTIONAL BLOCK DIAGRAMS

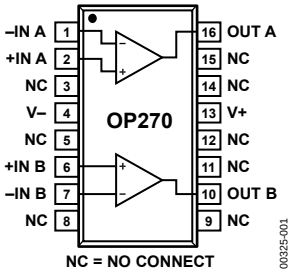

Figure 1. 16-Lead SOIC (S-Suffix)

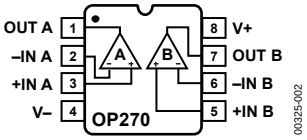

Figure 2. 8-Lead PDIP (P-Suffix)
8-Lead CERDIP
(Z-Suffix)

GENERAL DESCRIPTION

The OP270 is a high performance, monolithic, dual operational amplifier with exceptionally low voltage noise density (5 nV/√Hz maximum at 1 kHz). It offers comparable performance to the industry-standard OP27 from Analog Devices, Inc.

The OP270 features an input offset voltage of less than 75 µV and an offset drift of less than 1 µV/°C, guaranteed over the full military temperature range. Open-loop gain of the OP270 is more than 1,500,000 into a 10 kΩ load, ensuring excellent gain accuracy and linearity, even in high gain applications. The input bias current is less than 20 nA, which reduces errors due to signal source resistance. With a common-mode rejection (CMR) of greater than 106 dB and a power supply rejection ratio (PSRR) of less than 3.2 µV/V, the OP270 significantly reduces errors due to ground noise and power supply fluctuations. The power consumption of the dual OP270 is one-third less than two OP27 devices, a significant advantage for power conscious applications. The OP270 is unity-gain stable with a gain bandwidth product of 5 MHz and a slew rate of 2.4 V/µs.

The OP270 offers excellent amplifier matching, which is important for applications such as multiple gain blocks, low noise instrumentation amplifiers, dual buffers, and low noise active filters.

The OP270 conforms to the industry-standard 8-lead CERDIP and PDIP pinouts.

For higher speed applications, the ADA4004-2 or the AD8676 are recommended. For a quad op amp, see the OP470 data sheet.

Rev. F

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2/10—Rev. D to Rev. E

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2/09—Rev. C to Rev. D

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2/01—Revision 0: Initial Version

SPECIFICATIONS

V_S = ±15 V, T_A = 25°C, unless otherwise noted.

Table 1.

			OP270E			OP270F			OP270G			
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Input Offset Voltage	V_{OS}			10	75		20	150		50	250	µV
Input Offset Current	I_{OS}	V_{CM} = 0 V		1	10		3	15		5	20	nA
Input Bias Current	I_B	V_{CM} = 0 V		5	20		10	40		15	60	nA
Input Noise Voltage[1]	e_n p-p	0.1 Hz to 10 Hz		80	200		80	200		80		nV p-p
Input Noise Voltage Density[2]	e_n	f_O = 10 Hz		3.6	6.5		3.6	6.5		3.6		nV/√Hz
	e_n	f_O = 100 Hz		3.2	5.5		3.2	5.5		3.2		nV/√Hz
	e_n	f_O = 1 kHz		3.2	5.0		3.2	5.0		3.2		nV/√Hz
Input Noise Current Density	i_n	f_O = 10 Hz		1.1			1.1			1.1		pA/√Hz
	i_n	f_O = 100 Hz		0.7			0.7			0.7		pA/√Hz
	i_n	f_O = 1 kHz		0.6			0.6			0.6		pA/√Hz
Large-Signal Voltage Gain	A_{VO}	V_O = ±10 V, R_L = 10 kΩ	1500	2300		1000	1700		750	1500		V/mV
		V_O = ±10 V, R_L = 2 kΩ	750	1200		500	900		350	700		V/mV
Input Voltage Range[3]	IVR		±12	±12.5		±12	±12.5		±12	±12.5		V
Output Voltage Swing	V_O	R_L ≥ 2 kΩ	±12	±13.5		±12	±13.5		±12	±13.5		V
Common-Mode Rejection	CMR	V_{CM} = ±11 V	106	125		100	120		90	110		dB
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V		0.56	3.2		1.0	5.6		1.5	5.6	µV/V
Slew Rate	SR		1.7	2.4		1.7	2.4		1.7	2.4		V/µs
Supply Current (All Amplifiers)	I_{SY}	No load		4	6.5		4	6.5		4	6.5	mA
Gain Bandwidth Product	GBP			5			5			5		MHz
Channel Separation[1]	CS	V_O = ±20 V p-p, f_O = 10 Hz	125	175		125	175			175		dB
Input Capacitance	C_{IN}			3			3			3		pF
Input Resistance												
Differential Mode	R_{IN}			0.4			0.4			0.4		MΩ
Common Mode	R_{INCM}			20			20			20		GΩ
Settling Time	t_S	A_V = +1, 10 V, step to 0.01%		5			5			5		µs

[1] Guaranteed but not 100% tested.
[2] Sample tested.
[3] Guaranteed by CMR test.

ELECTRICAL SPECIFICATIONS

V_S = ±15 V, −40°C ≤ T_A ≤ 85°C, unless otherwise noted.

Table 2.

			OP270E			OP270F			OP270G			
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Input Offset Voltage	V_{OS}			25	150		45	275		100	400	µV
Average Input Offset Voltage Drift	TCV_{OS}			0.2	1		0.4	2		0.7	3	µV/°C
Input Offset Current	I_{OS}	V_{CM} = 0 V		1.5	30		5	40		15	50	nA
Input Bias Voltage	I_B	V_{CM} = 0 V		6	60		15	70		19	80	nA
Large-Signal Voltage Gain	A_{VO}	V_O = ±10 V, R_L = 10 kΩ	1000	1800		600	1400		400	1250		V/mV
	A_{VO}	V_O = ±10 V, R_L = 2 kΩ	500	900		300	700		225	670		V/mV
Input Voltage Range[1]	IVR		±12	±12.5		±12	±12.5		±12	±12.5		V
Output Voltage Swing	V_O	R_L ≥ 2 kΩ	±12	±13.5		±12	±13.5		±12	±13.5		V
Common-Mode Rejection	CMR	V_{CM} = ±11 V	100	120		94	115		90	100		dB
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V		0.7	5.6		1.8	10		2.0	1.5	µV/V
Supply Current (All Amplifiers)	I_{SY}	No load		4.4	7.2		4.4	7.2		4.4	7.2	mA

[1] Guaranteed by CMR test.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	±18 V
Differential Input Voltage[1]	±1.0 V
Differential Input Current[1]	±25 mA
Input Voltage	Supply voltage
Output Short-Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering, 60 sec)	300°C
Junction Temperature (T_J)	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C

[1] The OP270 inputs are protected by back-to-back diodes. To achieve low noise performance, current-limiting resistors are not used. If the differential voltage exceeds +10 V, the input current should be limited to ±25 mA.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

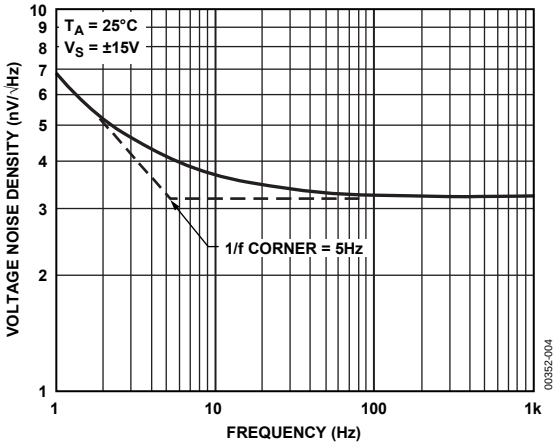


Figure 3. Voltage Noise Density vs. Frequency

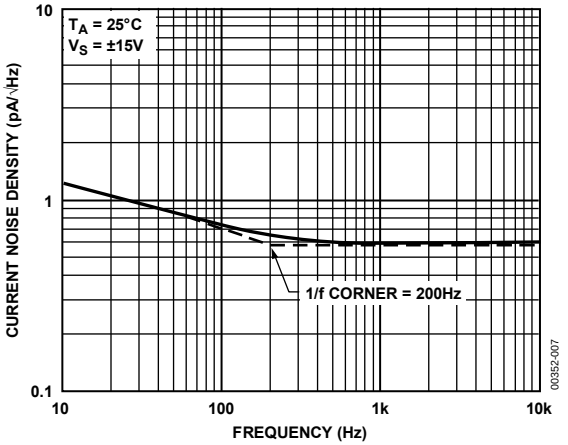


Figure 6. Current Noise Density vs. Frequency

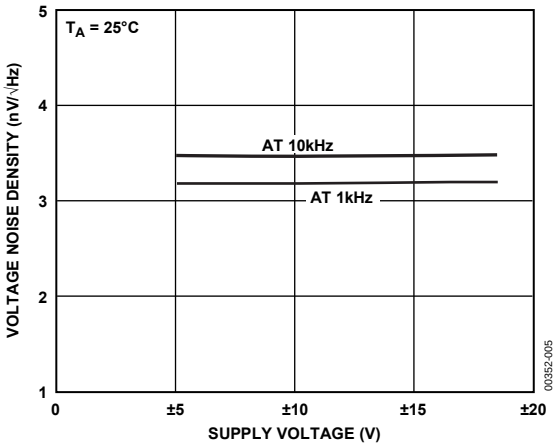


Figure 4. Voltage Noise Density vs. Supply Voltage

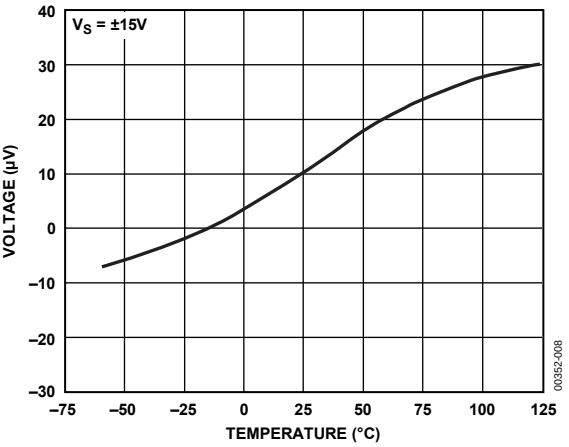


Figure 7. Input Offset Voltage vs. Temperature

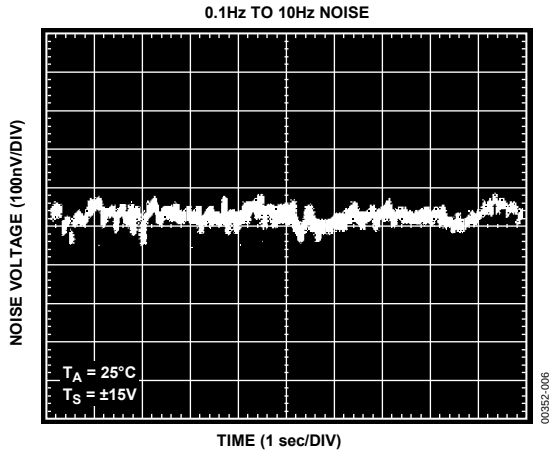


Figure 5. 0.1 Hz to 10 Hz Input Voltage Noise

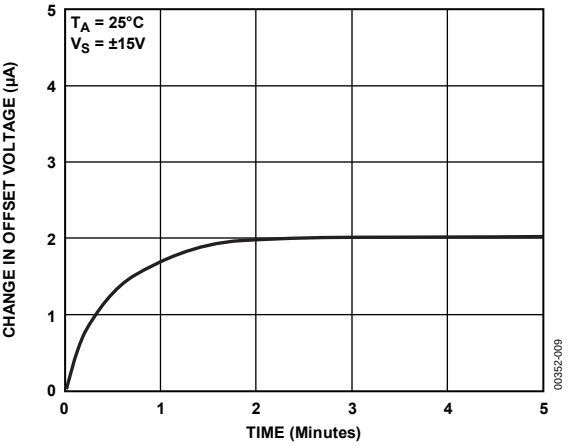


Figure 8. Warm-Up Offset Voltage Drift

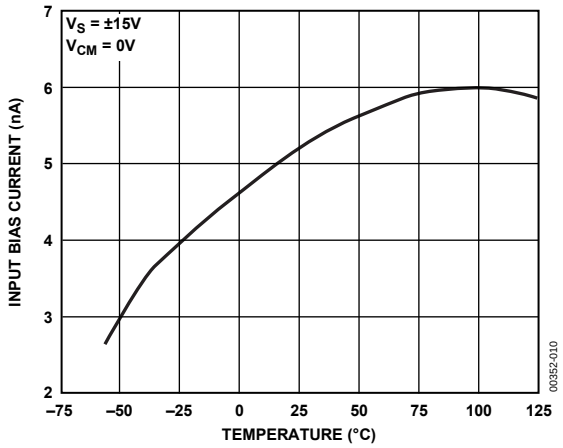


Figure 9. Input Bias Current vs. Temperature

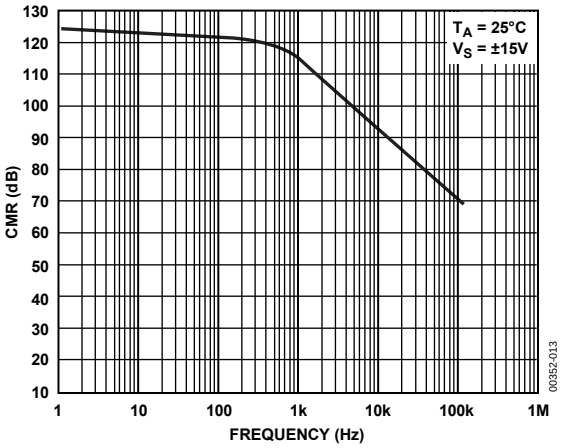


Figure 12. CMR vs. Frequency

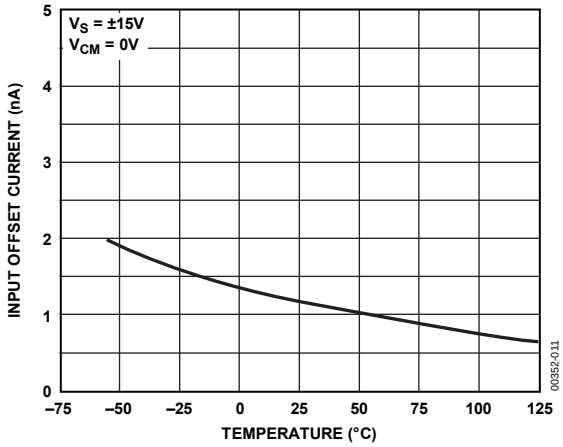


Figure 10. Input Offset Current vs. Temperature

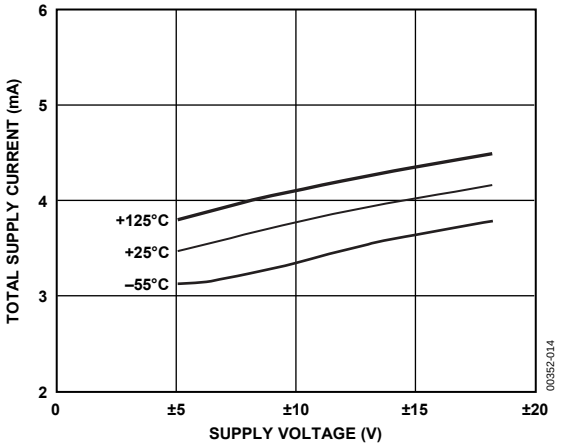


Figure 13. Total Supply Current vs. Supply Voltage

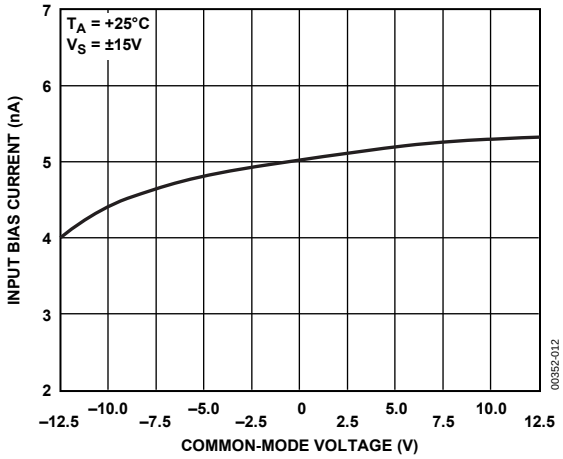


Figure 11. Input Bias Current vs. Common-Mode Voltage

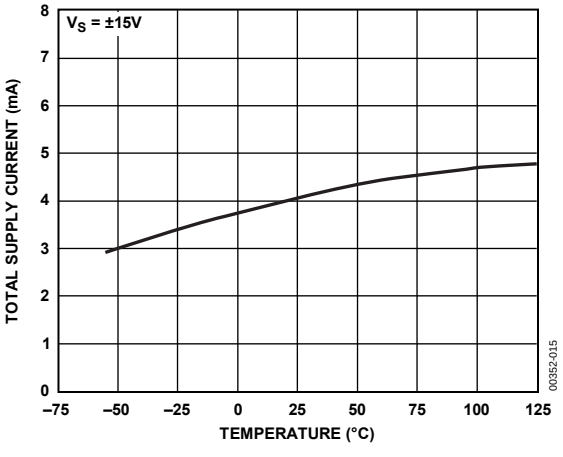


Figure 14. Total Supply Current vs. Temperature

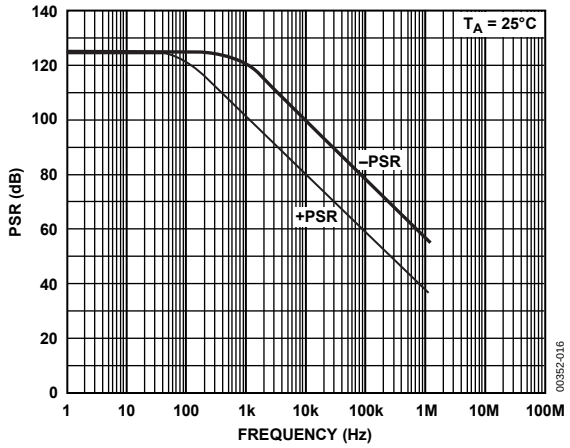


Figure 15. PSR vs. Frequency

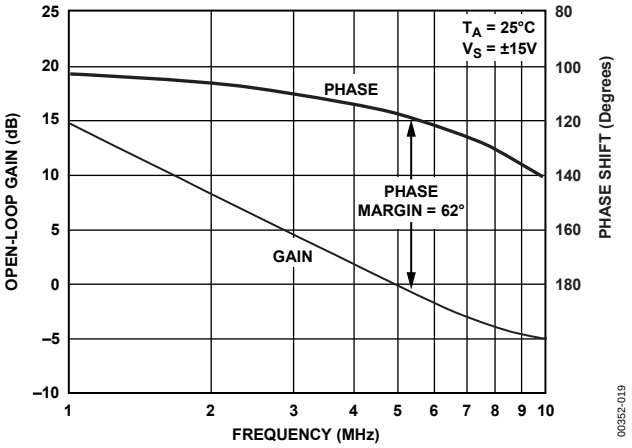


Figure 18. Open-Loop Gain and Phase Shift vs. Frequency

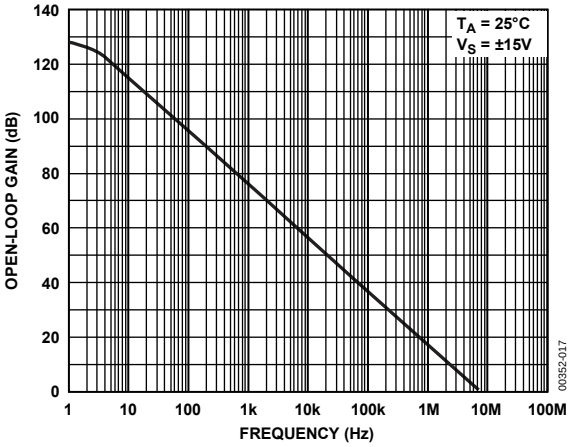


Figure 16. Open-Loop Gain vs. Frequency

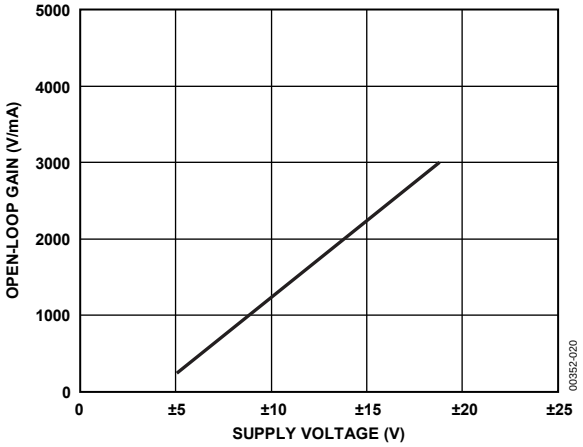


Figure 19. Open-Loop Gain vs. Supply Voltage

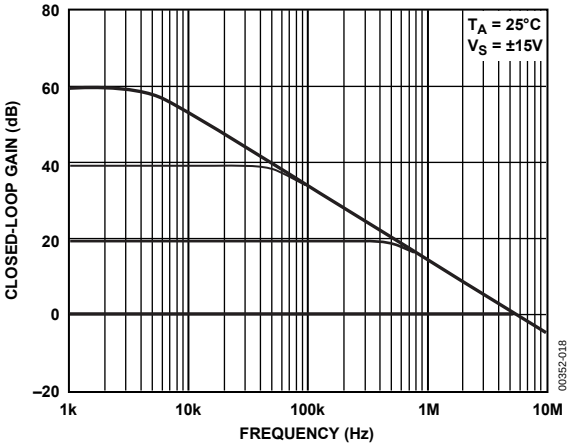


Figure 17. Closed-Loop Gain vs. Frequency

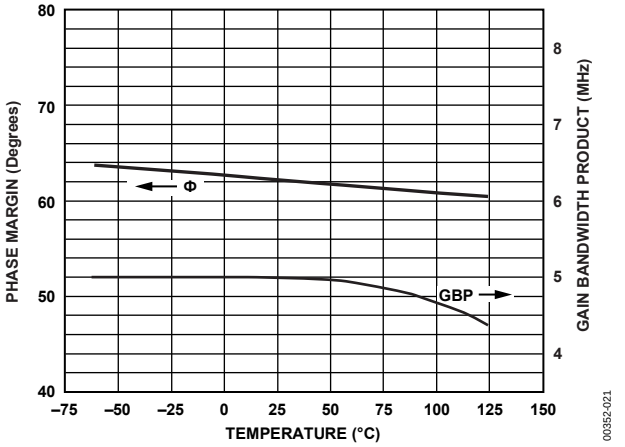


Figure 20. Phase Margin and Gain Bandwidth Product vs. Temperature

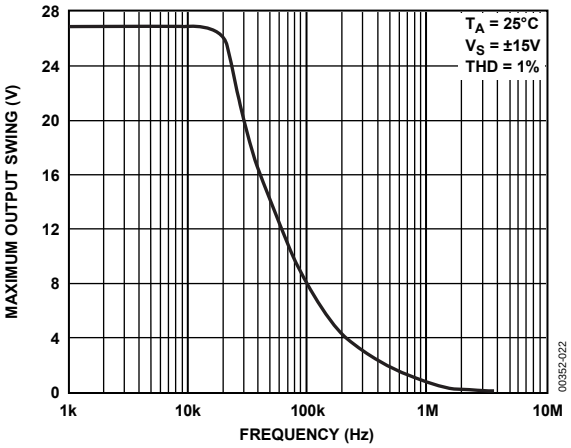


Figure 21. Maximum Output Swing vs. Frequency

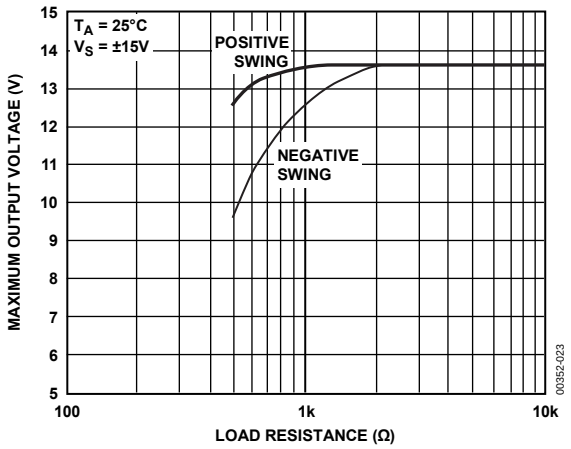


Figure 22. Maximum Output Voltage vs. Load Resistance

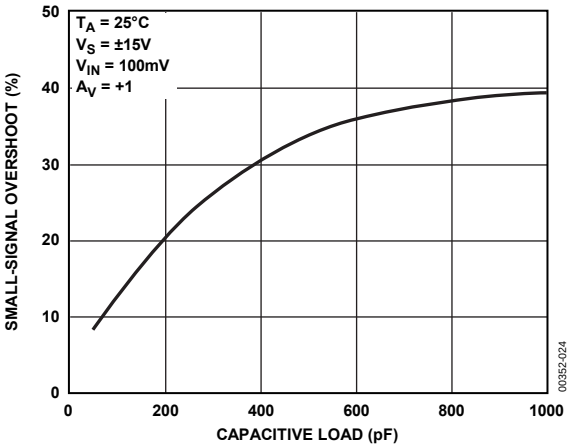


Figure 23. Small-Signal Overshoot vs. Capacitive Load

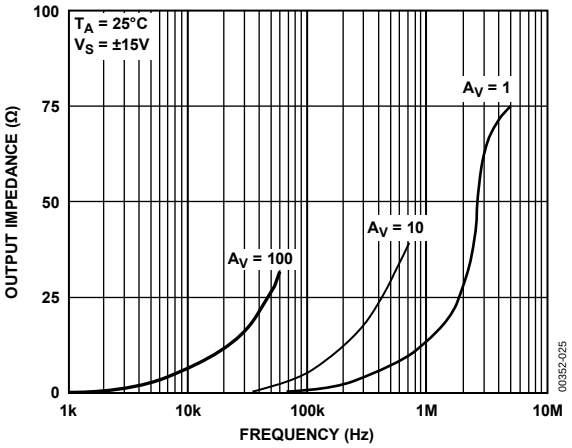


Figure 24. Output Impedance vs. Frequency

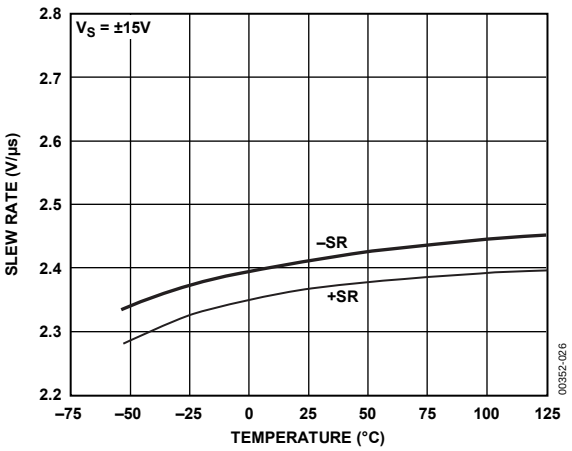


Figure 25. Slew Rate vs. Temperature

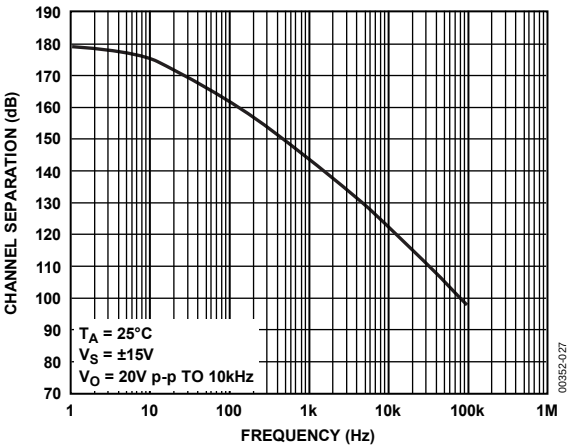


Figure 26. Channel Separation vs. Frequency

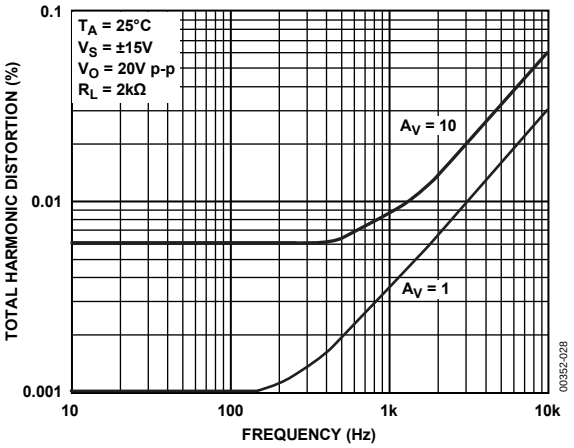


Figure 27. Total Harmonic Distortion vs. Frequency

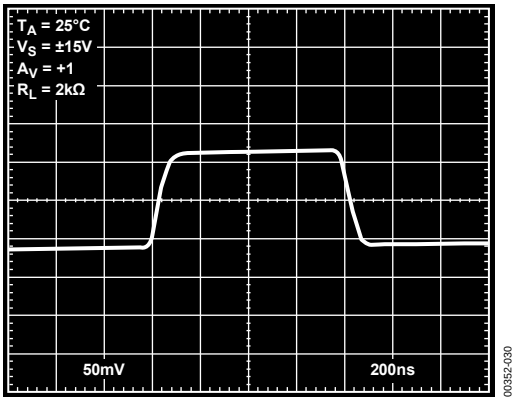


Figure 29. Small-Signal Transient Response

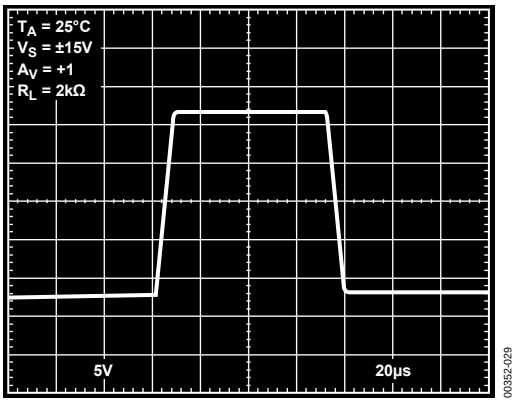


Figure 28. Large-Signal Transient Response

TEST CIRCUITS

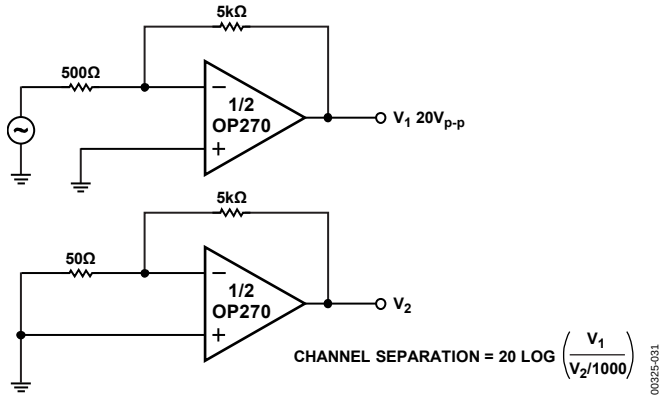


Figure 30. Channel Separation Test Circuit

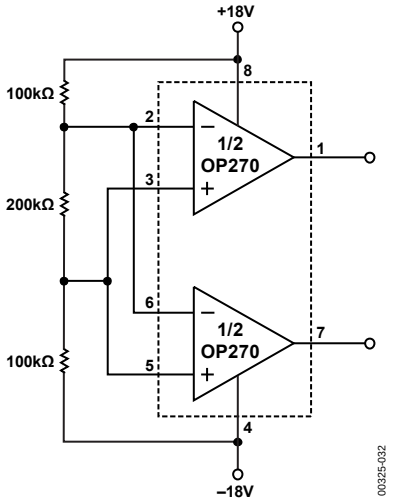


Figure 31. Burn-In Circuit

APPLICATIONS INFORMATION

VOLTAGE AND CURRENT NOISE

The OP270 is a very low noise dual op amp, exhibiting a typical voltage noise density of only 3.2 nV/√Hz at 1 kHz. Because the voltage noise is inversely proportional to the square root of the collector current, the exceptionally low noise characteristic of the OP270 is achieved in part by operating the input transistors at high collector currents. Current noise, however, is directly proportional to the square root of the collector current. As a result, the outstanding voltage noise density performance of the OP270 is gained at the expense of current noise performance, which is normal for low noise amplifiers.

To obtain the best noise performance in a circuit, it is vital to understand the relationships among voltage noise (e_n), current noise (i_n), and resistor noise (e_t).

TOTAL NOISE AND SOURCE RESISTANCE

The total noise of an op amp can be calculated by

$$E_n = \sqrt{(e_n)^2 + (i_n R_s)^2 + (e_t)^2}$$

where:
E_n is the total input-referred noise.
e_n is the op amp voltage noise.
i_n is the op amp current noise.
e_t is the source resistance thermal noise.
R_S is the source resistance.

The total noise is referred to the input and at the output is amplified by the circuit gain.

Figure 32 shows the relationship between total noise at 1 kHz and source resistance. When R_S is less than 1 kΩ, the total noise is dominated by the voltage noise of the OP270. As R_S rises above 1 kΩ, total noise increases and is dominated by resistor noise rather than by the voltage or current noise of the OP270. When R_S exceeds 20 kΩ, the current noise of the OP270 becomes the major contributor to total noise.

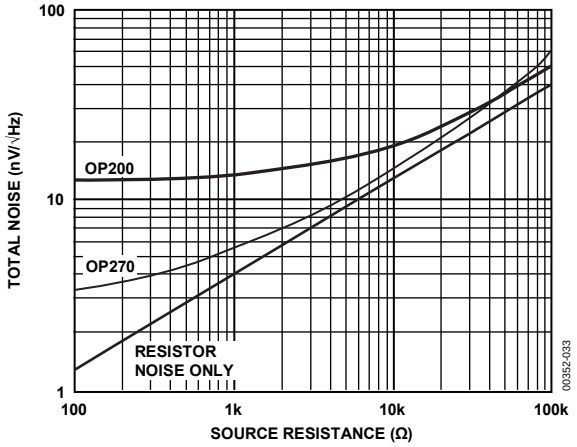


Figure 32. Total Noise vs. Source Resistance (Including Resistor Noise) at 1 kHz

Figure 33 also shows the relationship between total noise and source resistance, but at 10 Hz. Total noise increases more quickly than shown in Figure 32 because current noise is inversely proportional to the square root of frequency. In Figure 33, the current noise of the OP270 dominates the total noise when R_S is greater than 5 kΩ.

Figure 32 and Figure 33 show that to reduce total noise, source resistance must be kept to a minimum. In applications with a high source resistance, the OP200, with lower current noise than the OP270, can provide lower total noise.

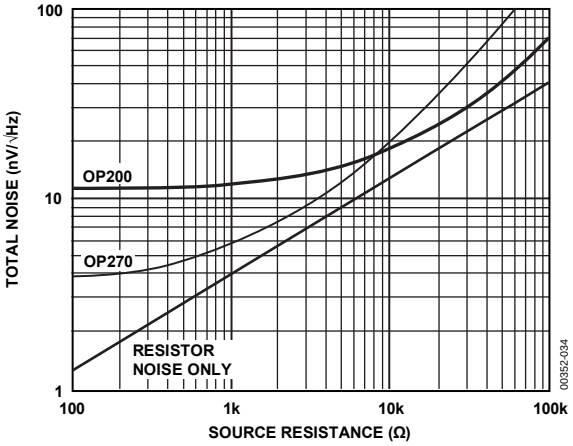


Figure 33. Total Noise vs. Source Resistance (Including Resistor Noise) at 10 Hz

Figure 34 shows peak-to-peak noise vs. source resistance over the 0.1 Hz to 10 Hz range. At low values of R_S, the voltage noise of the OP270 is the major contributor to peak-to-peak noise, with current noise becoming the major contributor as R_S increases. The crossover point between the OP270 and the OP200 for peak-to-peak noise is at a source resistance of 17 kΩ.

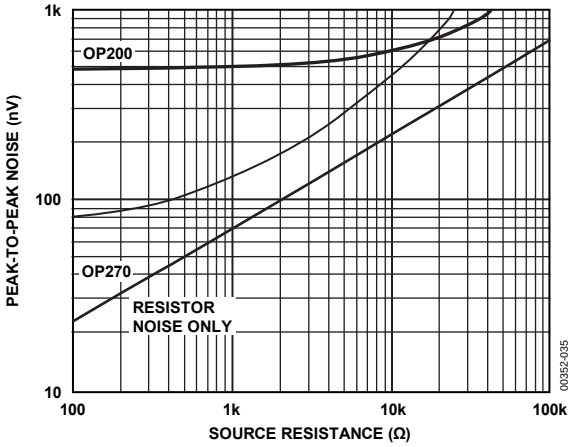


Figure 34. Peak-to-Peak Noise (0.1 Hz to 10 Hz) vs. Source Resistance (Including Resistor Noise)

For reference, typical source resistances of some signal sources are listed in Table 4.

Table 4. Typical Source Resistances

Device	Source Impedance	Comments
Strain Gage	<500 Ω	Typically used in low frequency applications.
Magnetic Tapehead, Microphone	<1500 Ω	Low I_B is very important to reduce self-magnetization problems when direct coupling is used. OP270 I_B can be disregarded.
Magnetic Phonograph Cartridge	<1500 Ω	Low I_B is important to reduce self-magnetization problems in direct-coupled applications. OP270 does not introduce any self-magnetization problems.
Linear Variable Differential Transformer	<1500 Ω	Used in rugged servo-feedback applications. The bandwidth of interest is 400 Hz to 5 kHz.

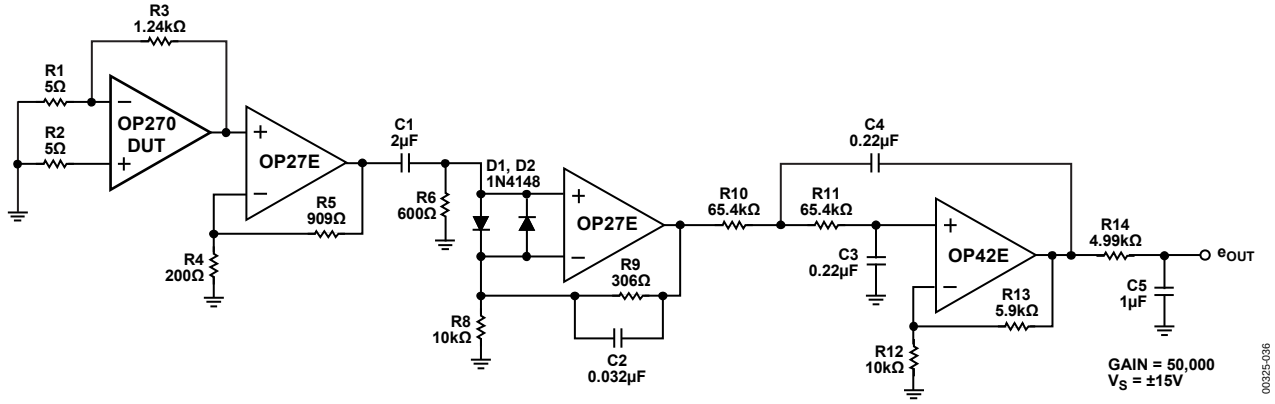


Figure 35. Peak-to-Peak Voltage Noise Test Circuit (0.1 Hz to 10 Hz)

NOISE MEASUREMENTS

Peak-to-Peak Voltage Noise

The circuit of Figure 35 is a test setup for measuring peak-to-peak voltage noise. To measure the 200 nV peak-to-peak noise specification of the OP270 in the 0.1 Hz to 10 Hz range, the following precautions must be observed:

- The device has to be warmed up for at least five minutes. As shown in the warm-up drift curve (see Figure 8), the offset voltage typically changes 2 µV due to increasing chip temperature after power-up. In the 10 sec measurement interval, these temperature-induced effects can exceed tens of nanovolts.
- For similar reasons, the device has to be well shielded from air currents. Shielding also minimizes thermocouple effects.
- Sudden motion in the vicinity of the device can also feed through to increase the observed noise.
- The test time to measure noise of 0.1 Hz to 10 Hz should not exceed 10 sec. As shown in the noise-tester frequency response curve of Figure 36, the 0.1 Hz corner is defined by only one pole. The test time of 10 sec acts as an additional pole to eliminate noise contribution from the frequency band below 0.1 Hz.
- A noise voltage density test is recommended when measuring noise on several units. A 10 Hz noise voltage density measurement correlates well with a 0.1 Hz to 10 Hz peak-to-peak noise reading because both results are determined by the white noise and the location of the 1/f corner frequency.
- Power should be supplied to the test circuit by well bypassed low noise supplies, such as batteries. Such supplies will minimize output noise introduced via the amplifier supply pins.

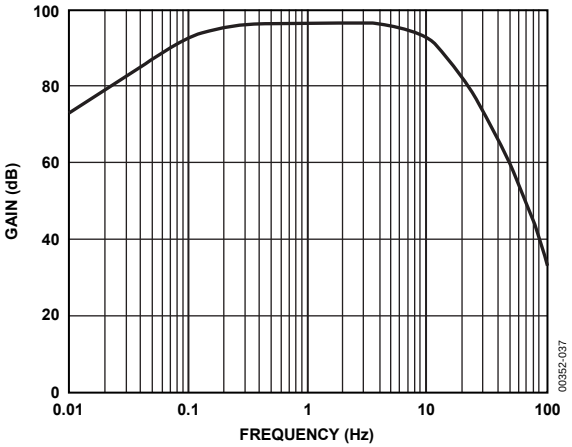


Figure 36. 0.1 Hz to 10 Hz Peak-to-Peak Voltage Noise Test Circuit Frequency Response

Noise Measurement—Noise Voltage Density

The circuit of Figure 37 shows a quick and reliable method for measuring the noise voltage density of dual op amps. The first amplifier is in unity gain, with the final amplifier in a noninverting gain of 101. Because the noise voltages of the amplifiers are uncorrelated, they add in rms to yield

$$e_{OUT} = 101\left(\sqrt{(e_{nA})^2 + (e_{nB})^2}\right)$$

The OP270 is a monolithic device with two identical amplifiers. Therefore, the noise voltage densities of the amplifiers match, giving

$$e_{OUT} = 101\left(\sqrt{2e_n{}^2}\right) = 101\left(\sqrt{2}e_n\right)$$

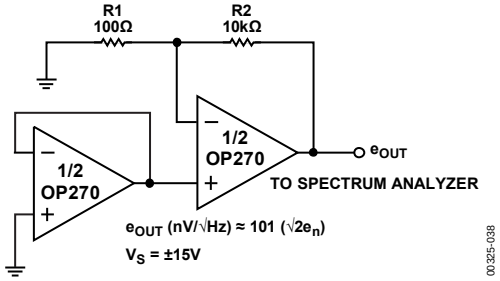


Figure 37. Noise Voltage Density Test Circuit

Noise Measurement—Current Noise Density

The test circuit shown in Figure 38 can be used to measure current noise density. The formula relating the voltage output to the current noise density is

$$i_n = \frac{\sqrt{\left(\frac{e_{nOUT}}{G}\right)^2 - \left(40\,nV/\sqrt{Hz}\right)^2}}{R_S}$$

where:

G is a gain of 10,000.

R_S = 100 kΩ source resistance.

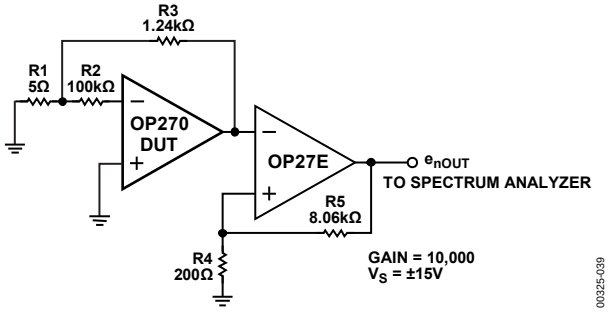


Figure 38. Current Noise Density Test Circuit

CAPACITIVE LOAD DRIVING AND POWER SUPPLY CONSIDERATIONS

The OP270 is unity-gain stable and capable of driving large capacitive loads without oscillating. Nonetheless, good supply bypassing is highly recommended. Proper supply bypassing reduces problems caused by supply line noise and improves the capacitive load driving capability of the OP270.

In the standard feedback amplifier, the output resistance of the op amp combines with the load capacitance to form a low-pass filter that adds phase shift in the feedback network and reduces stability. A simple circuit to eliminate this effect is shown in Figure 39. The components C1 and R3 decouple the amplifier from the load capacitance and provide additional stability. The values of C1 and R3 shown in Figure 39 are for a load capacitance of up to 1000 pF when used with the OP270.

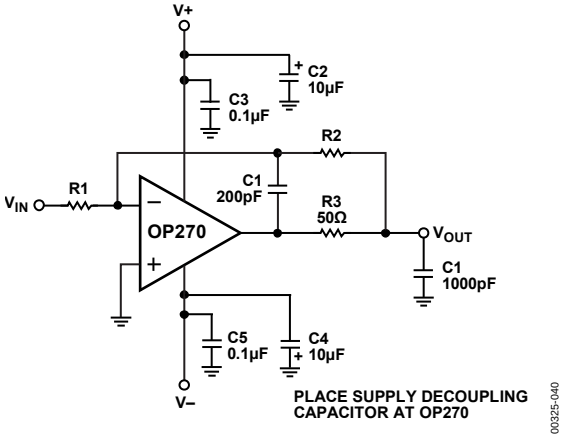


Figure 39. Driving Large Capacitive Loads

UNITY-GAIN BUFFER APPLICATIONS

When $R_f \leq 100\ \Omega$ and the input is driven with a fast, large signal pulse (>1 V), the output waveform looks like the one in Figure 40.

During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input, and a current, limited only by the output short-circuit protection, is drawn by the signal generator. With $R_f \geq 500\ \Omega$, the output is capable of handling the current requirements ($I_L \leq 20$ mA at 10 V); the amplifier stays in its active mode and a smooth transition occurs.

When $R_f > 3\ k\Omega$, a pole created by R_f and the input capacitance (3 pF) of the amplifier creates additional phase shift and reduces phase margin. A small capacitor (20 pF to 50 pF) in parallel with R_f helps eliminate this problem.

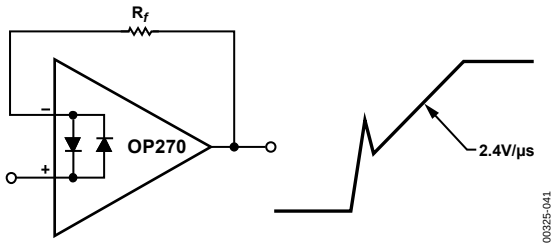


Figure 40. Pulsed Operation

LOW PHASE ERROR AMPLIFIER

The simple amplifier depicted in Figure 41 utilizes a monolithic dual operational amplifier and a few resistors to substantially reduce phase error compared with conventional amplifier designs. At a given gain, the frequency range for a specified phase accuracy is more than a decade greater than that of a standard single op amp amplifier.

The low phase error amplifier performs second-order frequency compensation through the response of Op Amp A2 in the feedback loop of A1. Both op amps must be extremely well matched in frequency response. At low frequencies, the A1 feedback loop forces $V_2/(K1 + 1) = V_{IN}$. The A2 feedback loop forces $V_O/(K1 + 1) = V_2/(K1 + 1)$, yielding an overall transfer function of $V_O/V_{IN} = K1 + 1$. The dc gain is determined by the resistor divider at the output, V_O, and is not directly affected by the resistor divider around A2. Note that, like a conventional single op amp amplifier, the dc gain is set by resistor ratios only. Minimum gain for the low phase error amplifier is 10.

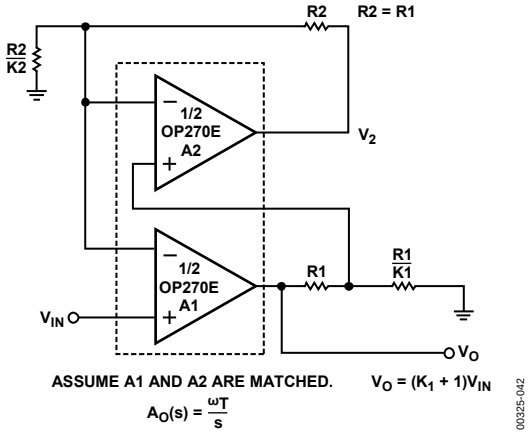


Figure 41. Low Phase Error Amplifier

Figure 42 compares the phase error performance of the low phase error amplifier with a conventional single op amp amplifier and a cascaded two-stage amplifier. The low phase error amplifier shows a much lower phase error, particularly for frequencies where $\omega/\beta\omega_T < 0.1$. For example, a phase error of −0.1° occurs at 0.002 $\omega/\beta\omega_T$ for the single op amp amplifier, but at 0.11 $\omega/\beta\omega_T$ for the low phase error amplifier.

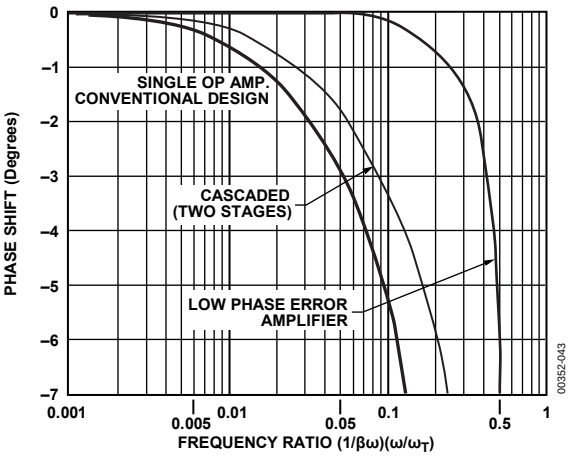


Figure 42. Phase Error Comparison

FIVE-BAND, LOW NOISE, STEREO GRAPHIC EQUALIZER

The graphic equalizer circuit shown in Figure 43 provides 15 dB of boost or cut over a five-band range. Signal-to-noise ratio over a 20 kHz bandwidth is better than 100 dB and referred to a 3 V rms input. Larger inductors can be replaced by active inductors, but consequently reduces the signal-to-noise ratio.

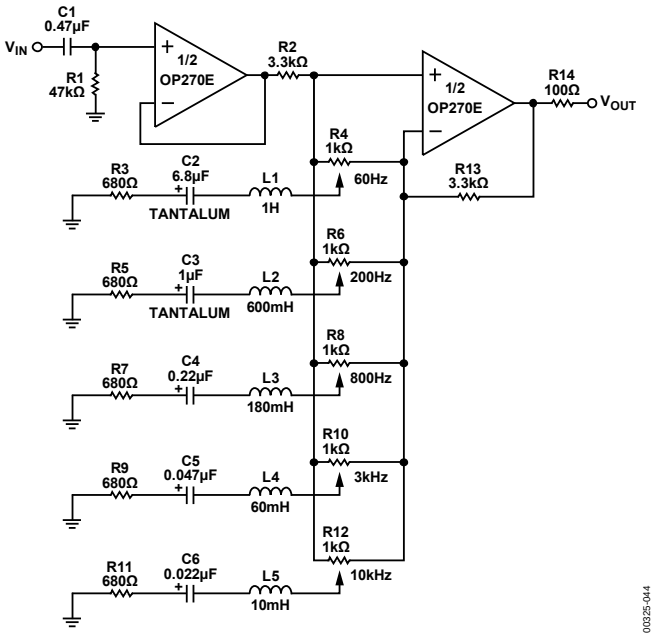


Figure 43. Five-Band, Low Noise Graphic Equalizer

DIGITAL PANNING CONTROL

Figure 44 uses a DAC8221 (a dual 12-bit CMOS DAC) to pan a signal between two channels. One channel is formed by the current output of DAC A driving one-half of an OP270 in a current-to-voltage converter configuration. The other channel is formed by the complementary output current of DAC A, which normally flows to ground through the AGND pin. This complementary current is converted to a voltage by the other half of the OP270, which also holds AGND at virtual ground.

Gain error due to mismatching between the internal DAC ladder resistors and the current-to-voltage feedback resistors is eliminated by using feedback resistors internal to the DAC8221. Only DAC A passes a signal; DAC B provides the second feedback resistor. With $V_{REF}B$ unconnected, the current-to-voltage converter, using R_{FBB}, is accurate and not influenced by digital data reaching DAC B. Distortion of the digital panning control is less than 0.002% over the 20 Hz to 20 kHz audio range. Figure 45 shows the complementary outputs for a 1 kHz input signal and a digital ramp applied to the DAC data input.

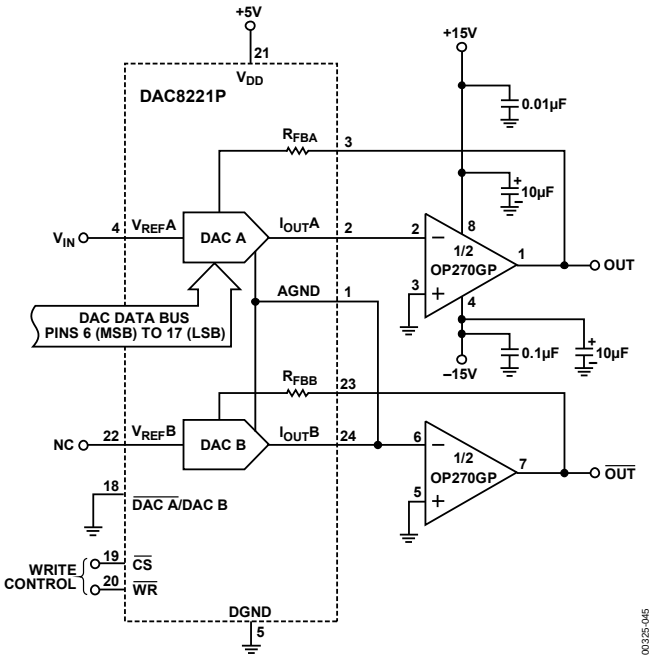


Figure 44. Digital Panning Control

DUAL PROGRAMMABLE GAIN AMPLIFIER

The dual OP270 and the DAC8221 (a dual 12-bit CMOS DAC) can be combined to form a space-saving, dual programmable amplifier. The digital code present at the DAC, which is easily set by a microprocessor, determines the ratio between the internal feedback resistor and the resistance that the DAC ladder presents to the op amp feedback loop. Gain of each amplifier is

$$\frac{V_O}{V_{IN}} = -\frac{4096}{n}$$

where n is the decimal equivalent of the 12-bit digital code present at the DAC.

If the digital code present at the DAC consists of all 0s, the feedback loop opens, causing the op amp output to saturate. A 20 MΩ resistor placed in parallel with the DAC feedback loop eliminates this problem with only a very small reduction in gain accuracy.

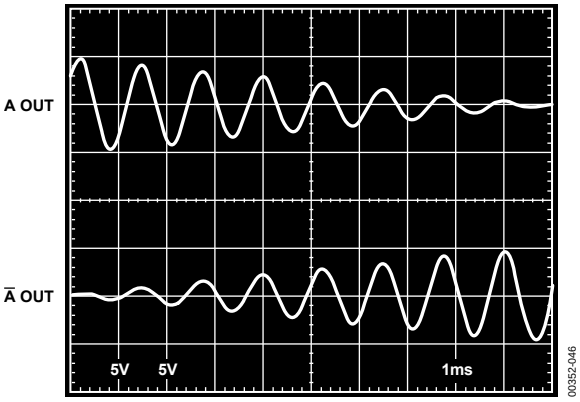


Figure 45. Digital Panning Control Output

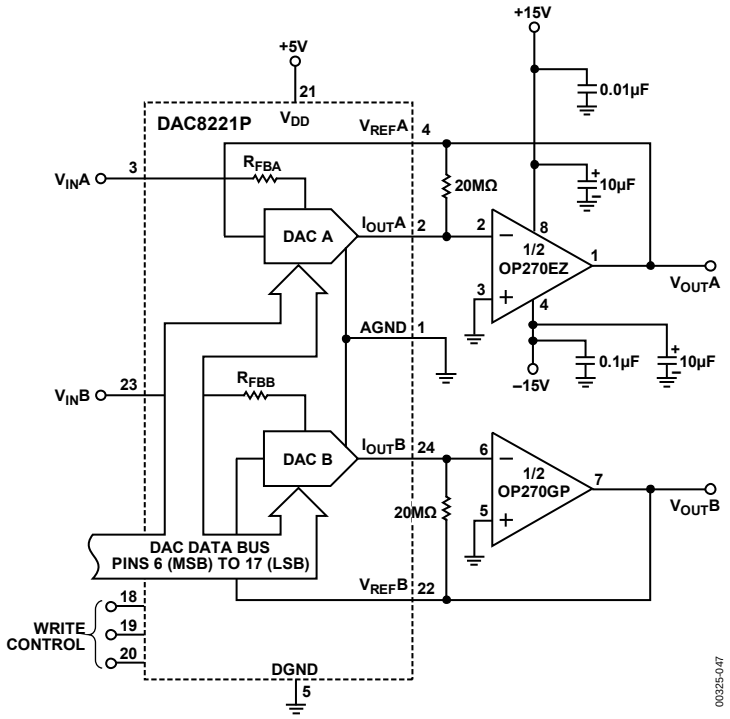


Figure 46. Dual Programmable Gain Amplifier

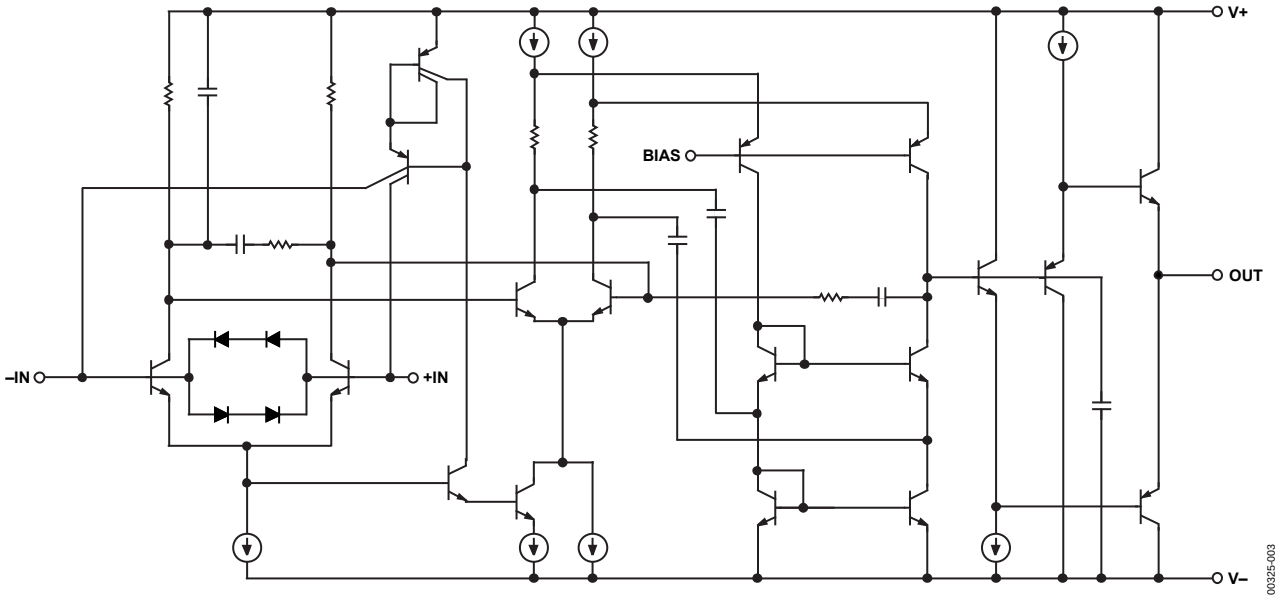
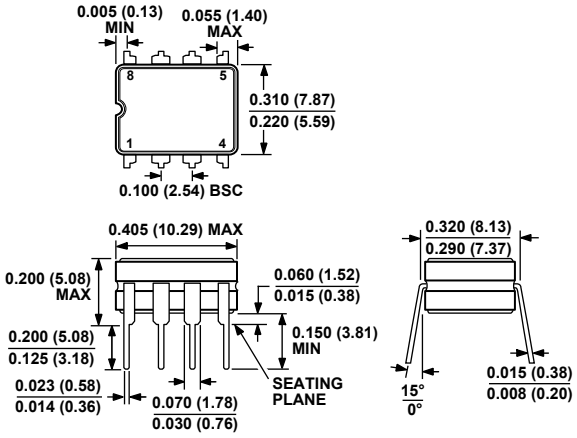


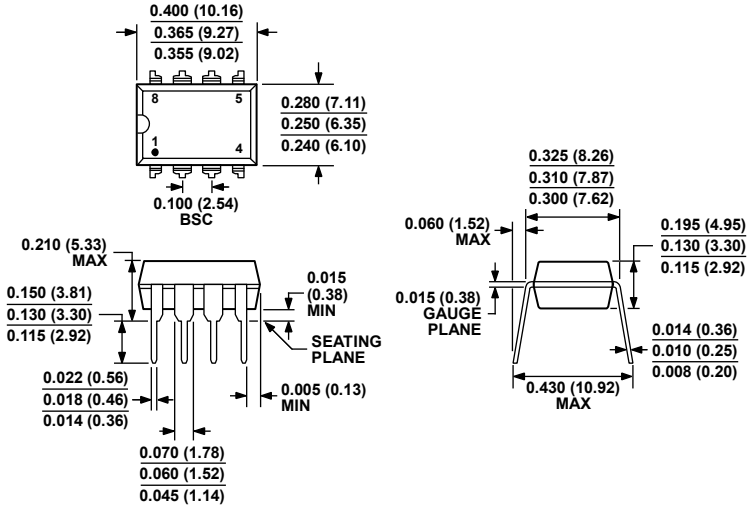
Figure 47. Simplified Schematic
(One of Two Amplifiers Is Shown)

OUTLINE DIMENSIONS



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 48. 8-Lead Ceramic Dual In-Line Package [CERDIP]
Z-Suffix
(Q-8)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-001

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

07 06 06-A

Figure 49. 8-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
P-Suffix
(N-8)
Dimensions shown in inches and (millimeters)

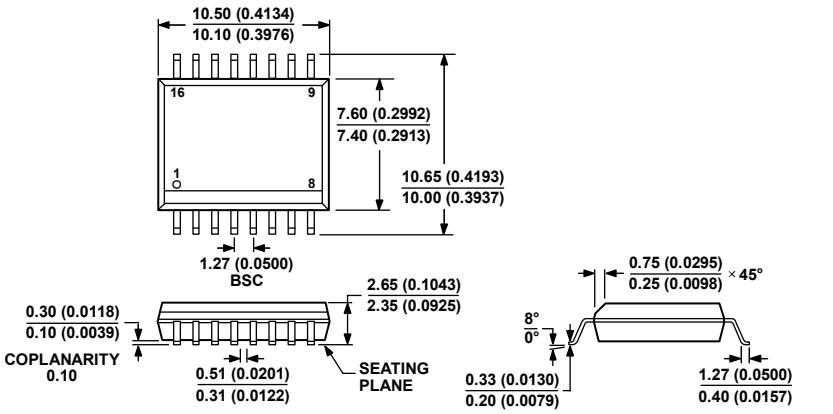


Figure 50. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body
S-Suffix
(RW-16)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	T_A = +25°C V_{OS} Max (µV)	θ_{JC} (°C/W)	θ_{JA}[2] (°C/W)	Temperature Range	Package Description	Package Option
OP270EZ	75	12	134	−40°C to +85°C	8-Lead CERDIP	Q-8 (Z-Suffix)
OP270FZ	150	12	134	−40°C to +85°C	8-Lead CERDIP	Q-8 (Z-Suffix)
OP270GP	250	37	96	−40°C to +85°C	8-Lead PDIP	N-8 (P-Suffix)
OP270GPZ				−40°C to +85°C	8-Lead PDIP	N-8 (P-Suffix)
OP270GS	250	27	92	−40°C to +85°C	16-Lead SOIC_W	RW-16 (S-Suffix)
OP270GS-REEL				−40°C to +85°C	16-Lead SOIC_W	RW-16 (S-Suffix)
OP270GSZ				−40°C to +85°C	16-Lead SOIC_W	RW-16 (S-Suffix)
OP270GSZ-REEL				−40°C to +85°C	16-Lead SOIC_W	RW-16 (S-Suffix)

[1] The OP270GPZ, OP270GSZ, and OP270GSZ-REEL are RoHS compliant parts.
[2] θ_{JA} is specified for worst-case mounting conditions, that is, θ_{JA} is specified for device in socket for CERDIP and PDIP packages; θ_{JA} is specified for device soldered to printed circuit board for SOIC package.