



FXPS7400D4

Digital absolute pressure sensor, 20 kPa to 400 kPa

Rev. 6 — 6 June 2022

Product data sheet

1 General description

The FXPS7400D4 high-performance, high-precision barometric absolute pressure (BAP) sensor consists of a compact capacitive micro-electro-mechanical systems (MEMS) device coupled with a digital integrated circuit (IC) producing a fully calibrated digital output.

The sensor is based on NXP's high-precision capacitive pressure cell technology. The architecture benefits from redundant pressure transducers as an expanded quality measure. This sensor delivers highly accurate pressure and temperature readings through either a serial peripheral interface (SPI) or an inter-integrated circuit (I²C) interface. Furthermore, the sensor employs an on-demand digital self-test for the digital IC and the MEMS transducers.

The sensor operates over a pressure range of 20 kPa to 400 kPa and over a wide temperature range of -40 °C to 130 °C.

The sensor comes in an industry-leading 4 mm x 4 mm x 1.98 mm, restriction of hazardous substances (RoHS) compliant, high power quad flat no lead (HQFN) package^[1] suitable for small PCB integration. Its AEC-Q100^[2] compliance, high accuracy, reliable performance, and high media resistivity make it ideal for use in automotive, industrial, and consumer applications.

2 Features and benefits

- Absolute pressure range: 20 kPa to 400 kPa
- Operating temperature range: -40 °C to 130 °C
- Pressure transducer and digital signal processor (DSP)
 - Digital self-test
- I²C compatible serial interface
 - Client mode operation
 - Standard mode, Fast mode, and Fast-mode Plus support
- 32-bit SPI compatible serial interface
 - Sensor data transmission commands
 - 12-bit data for absolute pressure
 - 8-bit data for temperature
 - 2-bit basic status and 2-bit detailed status fields
 - 3, 4, or 8-bit configurable CRC
- Capacitance to voltage converter with anti-aliasing filter
- Sigma delta ADC plus sinc filter
- 800 Hz or 1000 Hz low-pass filter for absolute pressure
- Lead-free, 16-pin HQFN, 4 mm x 4 mm x 1.98 mm package



3 Applications

3.1 Automotive

- Engine management digital MAP and BAP
- Small engine control

3.2 Industrial

- Compressed air
- Manufacturing line control
- Gas metering
- Weather stations

3.3 Medical/Consumer

- Blood pressure monitor
- Medicine dispensing systems
- White goods

4 Ordering information

Table 1. Ordering information

| Type number | Package | | |
|----------------------------|---------|--|-----------|
| | Name | Description | Version |
| FXPS7400DI4 FXPS7400DS4 | HQFN16 | HQFN16, plastic, thermal enhanced quad flat pack; no leads; 16 terminals; 0.8 mm pitch; 4 mm x 4 mm x 1.98 mm body | SOT1573-1 |

4.1 Ordering options

Table 2. Ordering options

| Device | Range [kPa] | Packing | Interface | Temperature range |
|---------------|-------------------|---------------|------------------|-------------------|
| FXPS7400DI4T1 | 20 kPa to 400 kPa | Tape and reel | I ² C | −40 °C to 130 °C |
| FXPS7400DS4T1 | 20 kPa to 400 kPa | Tape and reel | SPI | −40 °C to 130 °C |

5 Block diagram

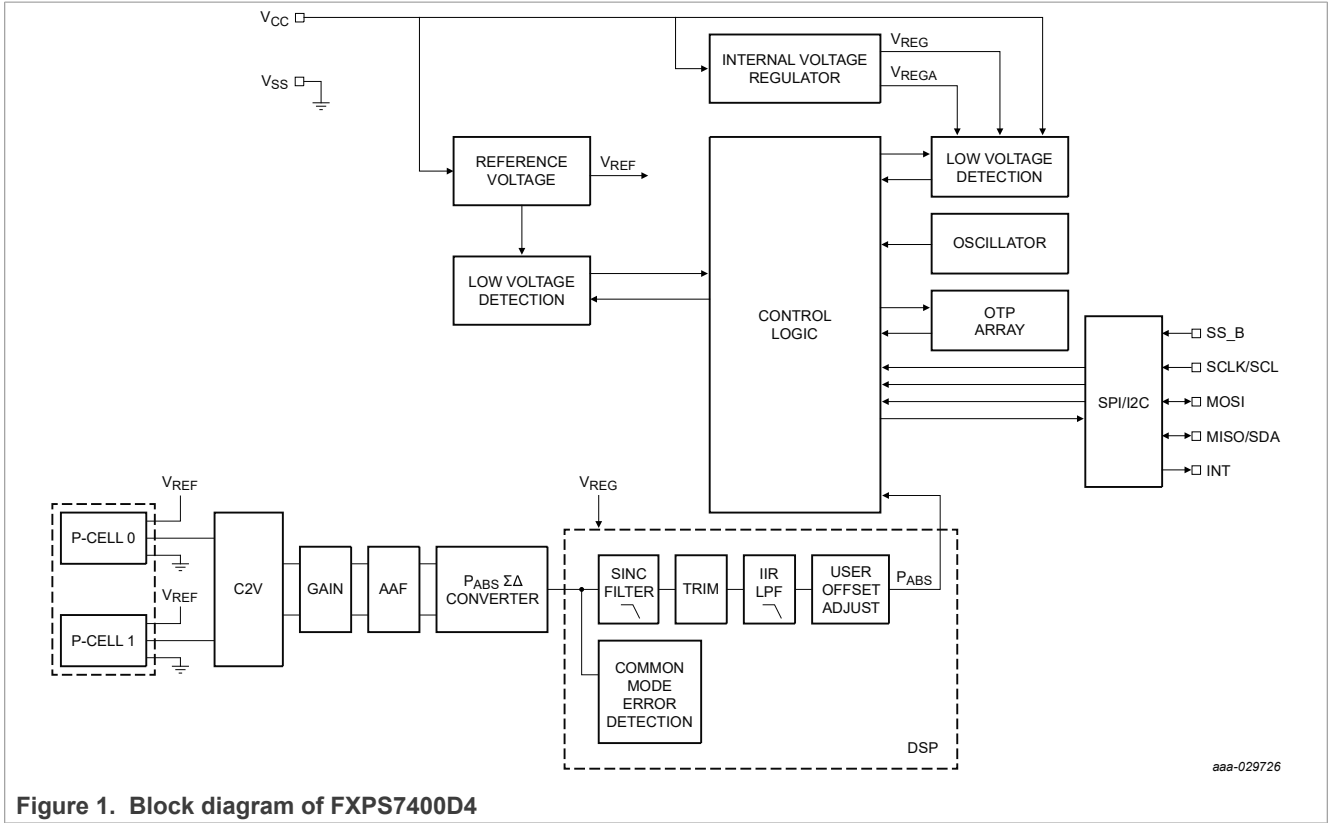


Figure 1. Block diagram of FXPS7400D4

6 Pinning information

6.1 Pinning

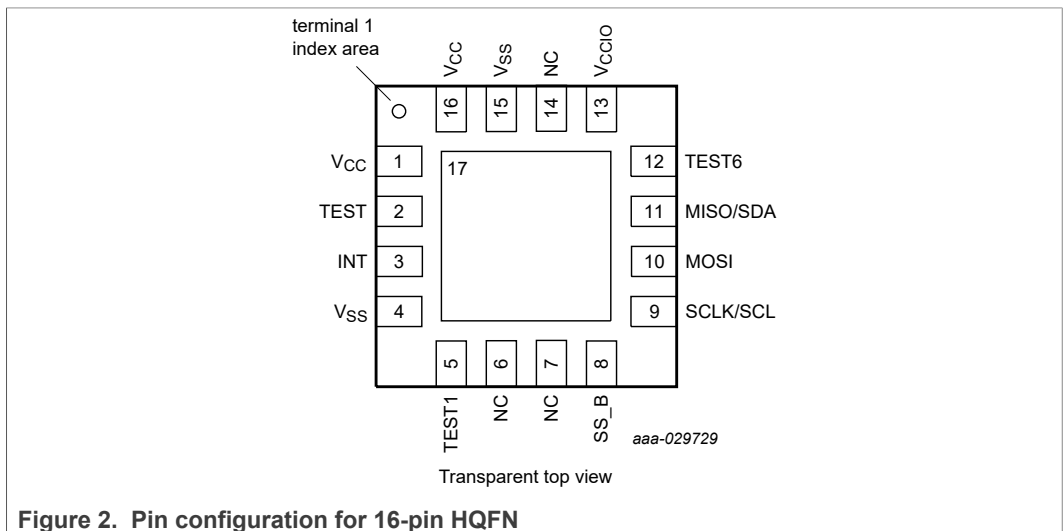


Figure 2. Pin configuration for 16-pin HQFN

6.2 Pin description

Table 3. Pin description

| Pin | Pin name | Description |
|----------|------------|---|
| 3 | INT | Interrupt output The output can be configured to be active low or active high. If unused, NXP recommends pin 3 be unterminated. Optionally, pin 3 can be tied to V_{SS} . |
| 1, 16 | V_{CC} | Power supply |
| 4, 15 | V_{SS} | Supply return (ground) |
| 2, 12 | TESTx | Test pin. NXP recommends pins 2, and 12 be unterminated. Optionally, these pins can be tied to V_{SS} . |
| 5 | TESTx | Test pin. NXP recommends pin 5 be tied to V_{CC} . Optionally, this pin can be tied to V_{SS} . |
| 6, 7, 14 | NC | No connect |
| 8 | SS_B | Client / Device select In I ² C mode, input pin 8 must be connected to V_{CC} with an external pull-up resistor, as shown in the application diagram. In SPI mode, input pin 8 provides the client select for the SPI port. An internal pull-up device is connected to this pin. |
| 9 | SCLK/SCL | In I ² C mode, input pin 9 provides the serial clock. This pin must be connected to V_{CC} with an external pull-up resistor, as shown in the application diagram. In SPI mode, input pin 9 provides the serial clock. An internal pull-down device is connected to this pin. |
| 10 | MOSI | SPI data in In SPI mode, pin 10 functions as the serial data input to the SPI port. An internal pull-down device is connected to this pin. |
| 11 | MISO/SDA | SPI/I ² C data out In I ² C mode, pin 11 functions as the serial data input/output. Pin 11 must be connected to V_{CC} with an external pull-up resistor, as shown in the application diagram. In SPI mode, pin 11 functions as the serial data output. |
| 13 | V_{CCIO} | I/O supply Pin 13 must be connected to V_{CC} , the device supply. |
| 17 | PAD | Die attach pad Pin 17 is the die attach flag, and must be connected to V_{SS} . |

7 Functional description

7.1 Voltage regulators

The device derives its internal supply voltage from the V_{CC} and V_{SS} pins. An external filter capacitor is required for V_{CC} , as shown in [Figure 23](#) and [Figure 24](#).

A reference generator provides a reference voltage for the $\Sigma\Delta$ converter.

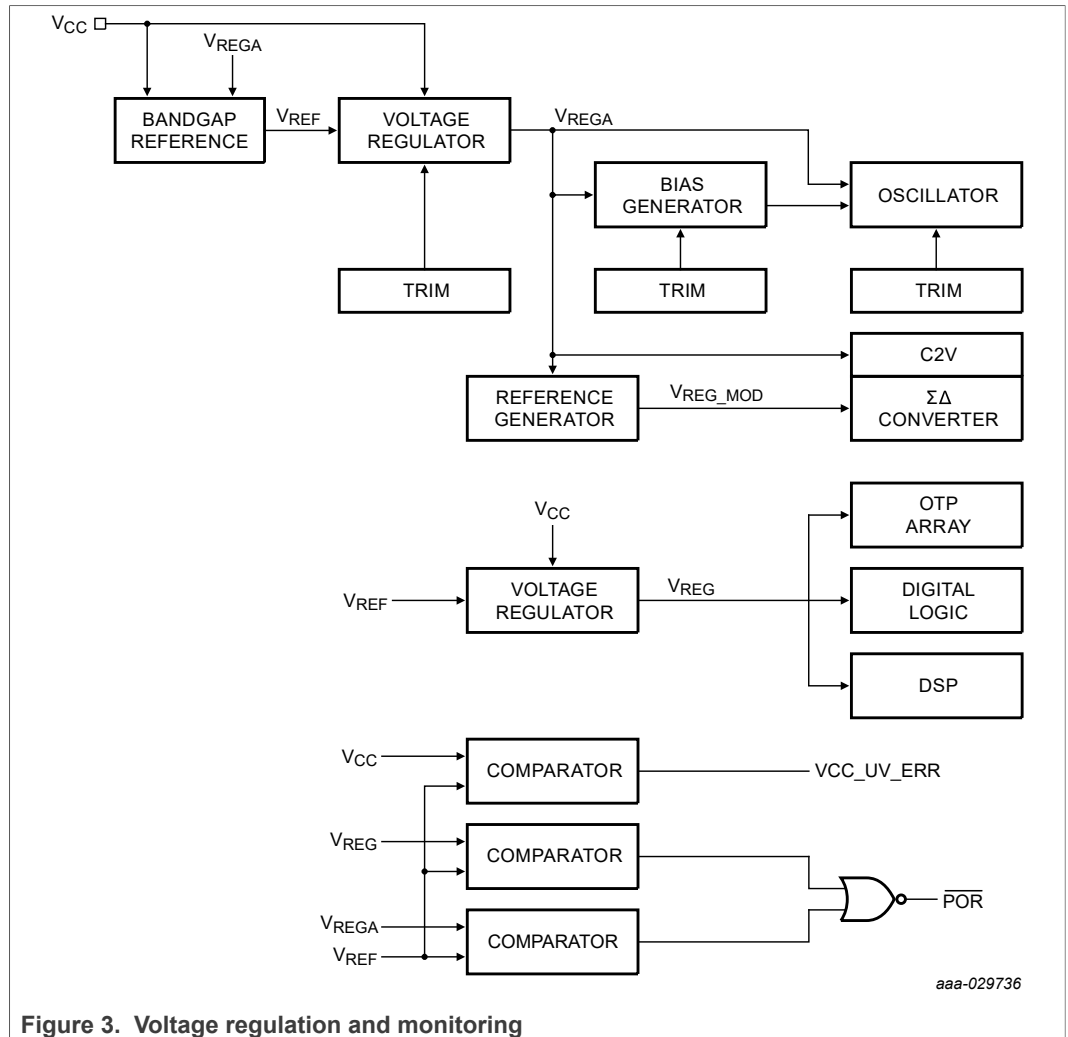


Figure 3. Voltage regulation and monitoring

7.1.1 V_{CC}, V_{REG}, V_{REGA}, undervoltage monitor

A circuit is incorporated to monitor the V_{CC} supply voltage and the internally regulated voltages V_{REG} and V_{REGA}. If any of the voltages fall below the specified undervoltage thresholds in Table 104, SPI and I²C transactions are terminated. Once the supply returns above the threshold, the device resumes responses.

7.2 Internal oscillator

The device includes a factory trimmed oscillator.

7.3 Pressure sensor signal path

7.3.1 Self-test functions

The device includes analog and digital self-test functions to verify the functionality of the transducer and the signal chain. The self-test functions are selected by writing to the ST_CTRL[3:0] bits in the DSP_CFG_U5 register. The ST_CTRL bits select the desired self-test connection.

Once the ENDINIT bit is set, the ST_CTRL bits are forced to '0000'. Future writes to the ST_CTRL bits are disabled until a device reset.

7.3.1.1 P_{ABS} common mode verification

When the P_{ABS} common mode self-test is selected, the ST_ACTIVE bit is set, the ST_ERROR is cleared, and the device begins an internal measurement of the common mode signal of the P-cells and compares the result against a predetermined limit. If the result exceeds the limit, the ST_ERROR bit is set. The P_{ABS} common mode self-test repeats continuously every t_{ST_INIT} when the ST_CTRL bits are set to the specified value. Once the test is disabled, the ST_ERROR bit updates with the final test result within t_{ST_INIT} of disabling the test. The ST_ACTIVE bit remains set until the final test result is reported. Figure 4 is an example of a user-controlled self-test procedure.

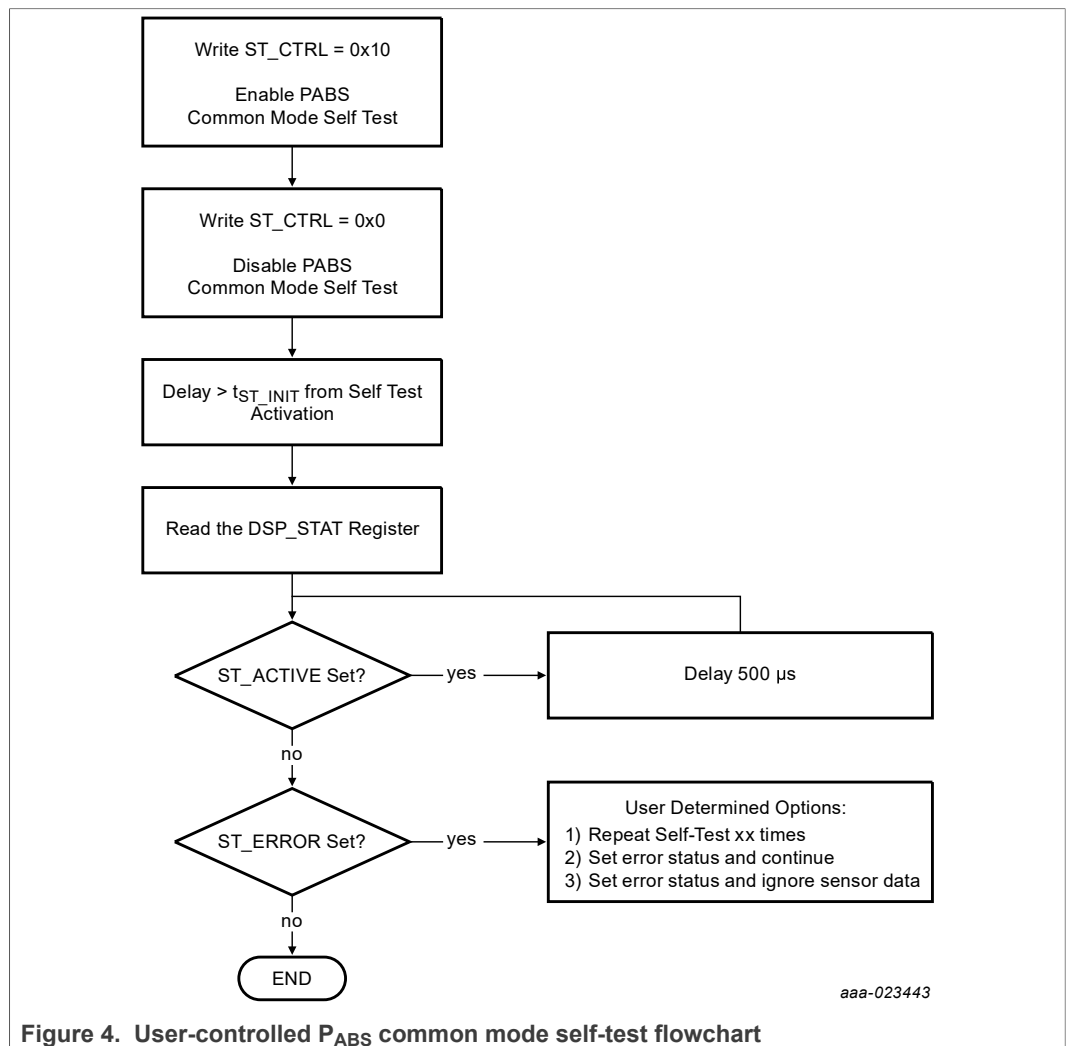


Figure 4. User-controlled P_{ABS} common mode self-test flowchart

7.3.1.2 Startup digital self-test verification

Four unique fixed values can be forced at the output of the sinc filter by writing to the ST_CTRL bits as shown in Table 4. The digital self-test values result in a constant value at the output of the signal chain. After a specified time period, the SNS_DATAx register value can be verified against the specified values in the table below. The values listed below are for the P_{ABS} signal. When any of these self-test functions are selected, the

ST_ACTIVE bit is set. These signals can only be selected when the ENDINIT bit is not set.

Table 4. Self-test control register

| ST_CTRL[3] | ST_CTRL[2] | ST_CTRL[1] | ST_CTRL[0] | Function | SNS_DATAx register contents |
|------------|------------|------------|------------|----------------------|-----------------------------|
| 1 | 1 | 0 | 0 | Digital self-test #1 | 8171h |
| 1 | 1 | 0 | 1 | Digital self-test #2 | 6C95h |
| 1 | 1 | 1 | 0 | Digital self-test #3 | 807Ah |
| 1 | 1 | 1 | 1 | Digital self-test #4 | 78ACh |

7.3.1.3 Startup sense data fixed value verification

Four unique fixed values can be forced to the SNS_DATAx_x registers by writing to the ST_CTRL bits as shown in Table 5. When any of these values are selected, the ST_ACTIVE bit is set. These signals can only be selected when the ENDINIT bit is not set.

Table 5. Self-test control bits for sense data fixed value verification

| ST_CTRL[3] | ST_CTRL[2] | ST_CTRL[1] | ST_CTRL[0] | Function | SNS_DATAx register contents |
|------------|------------|------------|------------|---|-----------------------------|
| 0 | 1 | 0 | 0 | DSP write to SNS_DATAx_X registers inhibited. | 0000h |
| 0 | 1 | 0 | 1 | DSP write to SNS_DATAx_X registers inhibited. | AAAAh |
| 0 | 1 | 1 | 0 | DSP write to SNS_DATAx_X registers inhibited. | 5555h |
| 0 | 1 | 1 | 1 | DSP write to SNS_DATAx_X registers inhibited. | FFFFh |

7.3.2 ΣΔ converter

A second order sigma delta modulator converts the voltage from the analog front end to a data stream that is input to the DSP. A simplified block diagram is shown in Figure 5.

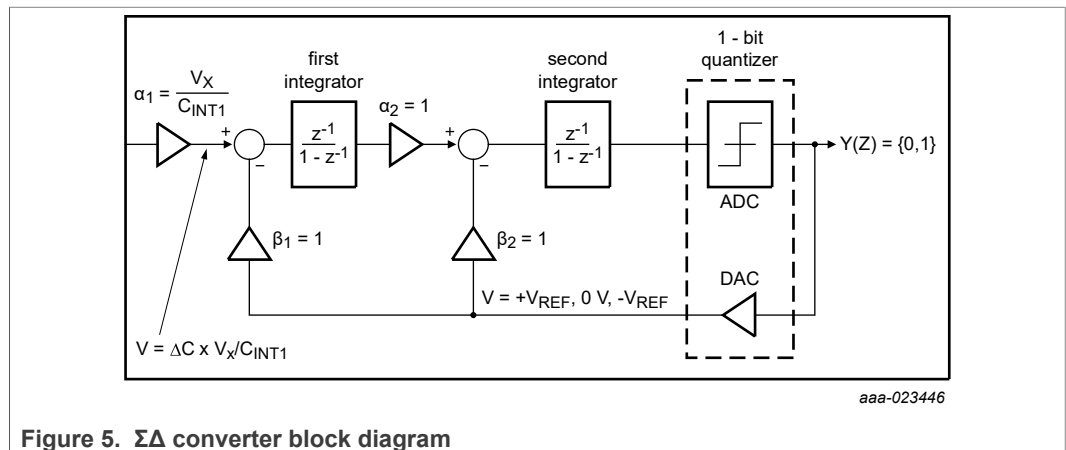


Figure 5. ΣΔ converter block diagram

The sigma delta modulator operates at a frequency of 1 MHz, with the transfer function in Equation 1.

$$H(Z) = \frac{\alpha_1}{Z^2} \tag{1}$$

7.3.3 Digital signal processor (DSP)

A DSP is used to perform signal filtering and compensation. A diagram illustrating the signal processing flow within the DSP is shown in [Figure 6](#).

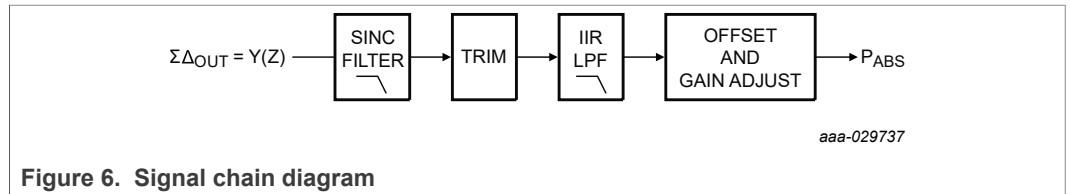


Figure 6. Signal chain diagram

7.3.3.1 Decimation sinc filter

In [Equation 2](#), the output of the $\Sigma\Delta$ modulator is decimated and converted to a parallel value by two third-order sinc filters; the first with a decimation ratio of 24 and the second with a decimation ratio of 4.

$$H(Z) = \left(\frac{1}{24^3}\right) \times \left(\frac{1 - Z^{-24}}{1 - Z^{-1}}\right)^3 \quad H(Z) = \left(\frac{1}{4^3}\right) \times \left(\frac{1 - Z^{-4}}{1 - Z^{-1}}\right)^3 \tag{2}$$

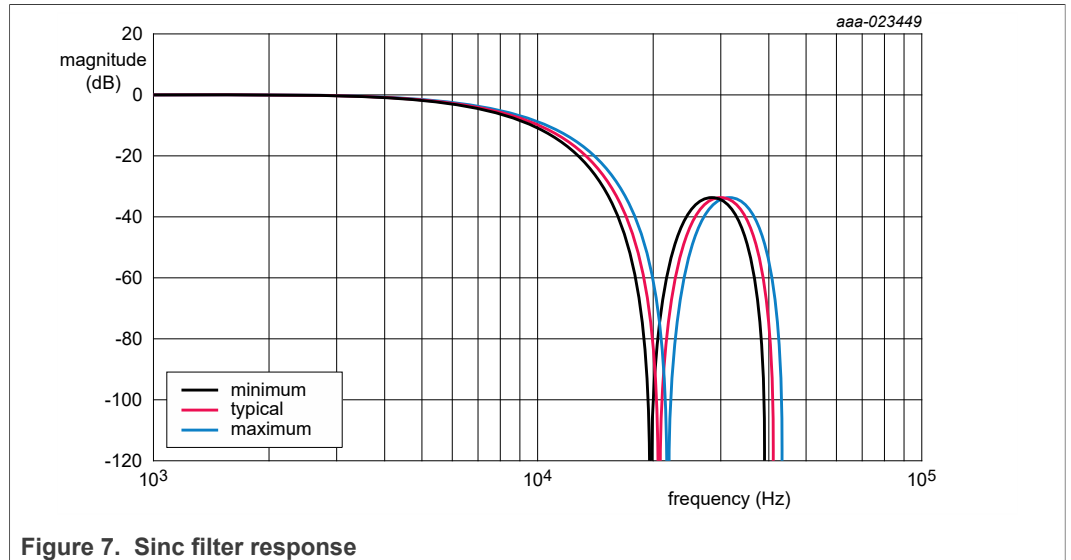


Figure 7. Sinc filter response

7.3.3.2 Signal trim and compensation

The device includes digital trim to compensate for sensor offset, sensitivity, and nonlinearity over temperature.

7.3.3.3 Low-pass filter

Data from the sinc filter is processed by an infinite impulse response (IIR) low-pass filter with the transfer function and coefficients shown in Equation 3.

$$H(Z) = a_0 \times \frac{(n_{11} \times z^0) + (n_{12} \times z^{-1}) + (n_{13} \times z^{-2})}{(d_{11} \times z^0) + (d_{12} \times z^{-1}) + (d_{13} \times z^{-2})} \times \frac{(n_{21} \times z^0) + (n_{22} \times z^{-1}) + (n_{23} \times z^{-2})}{(d_{21} \times z^0) + (d_{22} \times z^{-1}) + (d_{23} \times z^{-2})} \quad (3)$$

Table 6. IIR low pass filter coefficients

| Filter number | Typical -3 dB frequency | Filter order | Filter coefficients (24 bit) | | | | Group delay (µs) | Typical attenuation @ 1000 Hz (dB) |
|---------------|-------------------------|--------------|------------------------------|-------------------|-----------------|--------------------|------------------|------------------------------------|
| | | | | | | | | |
| 1 | 800 Hz | 4 | a ₀ | 0.088642612609670 | — | — | 418 | 4.95 |
| | | | n ₁₁ | 0.029638050039039 | d ₁₁ | 1 | | |
| | | | n ₁₂ | 0.087543281056143 | d ₁₂ | -1.422792640957290 | | |
| | | | n ₁₃ | 0.029695285913601 | d ₁₃ | 0.511435253566960 | | |
| | | | n ₂₁ | 0.250241278804809 | d ₂₁ | 1 | | |
| | | | n ₂₂ | 0.499999767379068 | d ₂₂ | -1.503329908017845 | | |
| | | | n ₂₃ | 0.249758953816089 | d ₂₃ | 0.621996524706640 | | |
| 2 | 1000 Hz | 4 | a ₀ | 0.129604264748411 | — | — | 333 | 2.99 |
| | | | n ₁₁ | 0.043719804402508 | d ₁₁ | 1 | | |
| | | | n ₁₂ | 0.087543281056143 | d ₁₂ | -1.300502656562698 | | |
| | | | n ₁₃ | 0.043823599710731 | d ₁₃ | 0.430106921311110 | | |
| | | | n ₂₁ | 0.250296586927511 | d ₂₁ | 1 | | |
| | | | n ₂₂ | 0.499999648540934 | d ₂₂ | -1.379959571988366 | | |
| | | | n ₂₃ | 0.249703764531484 | d ₂₃ | 0.555046257157745 | | |

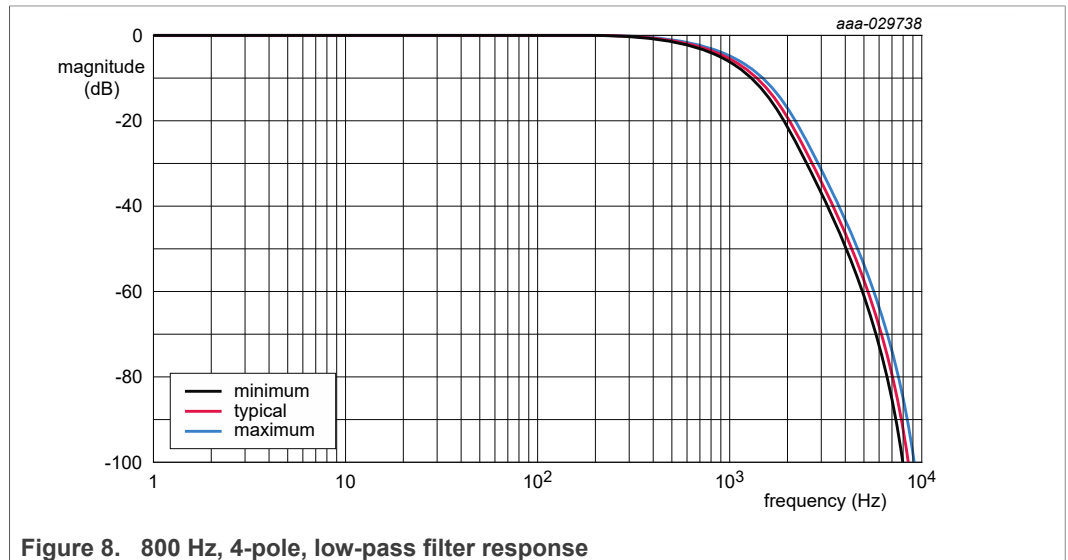


Figure 8. 800 Hz, 4-pole, low-pass filter response

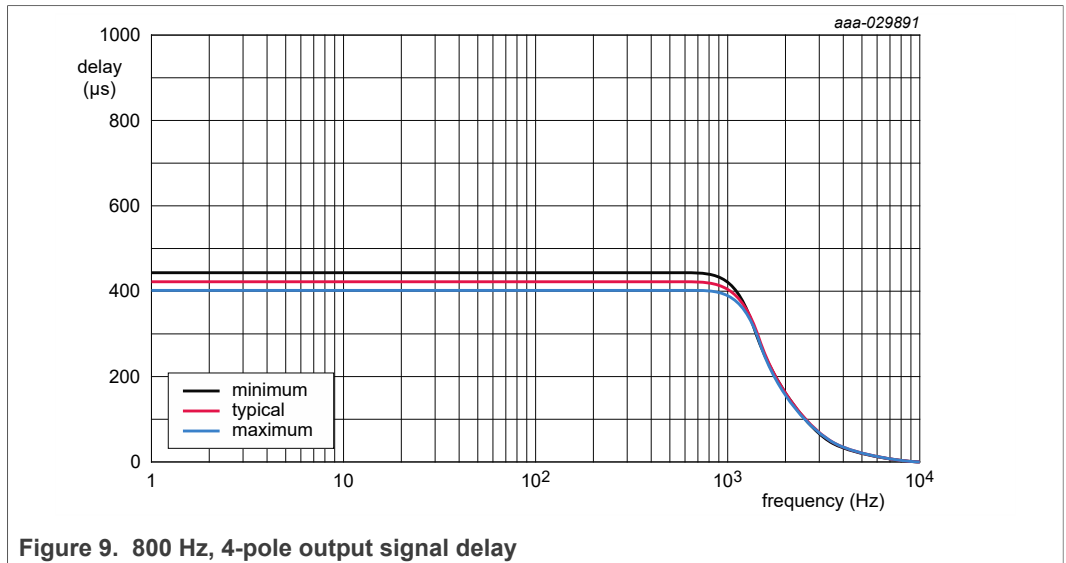


Figure 9. 800 Hz, 4-pole output signal delay

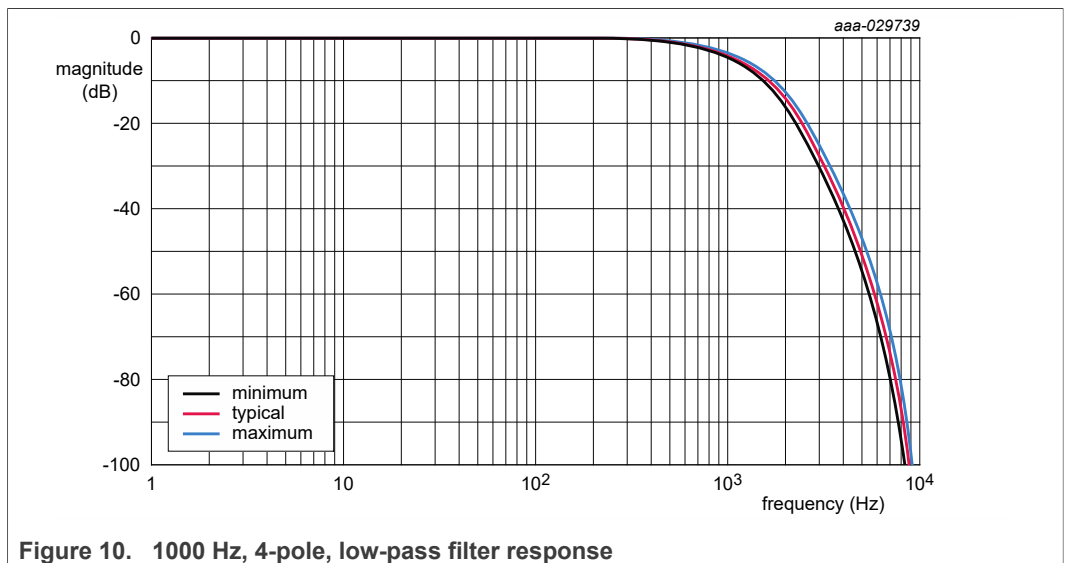
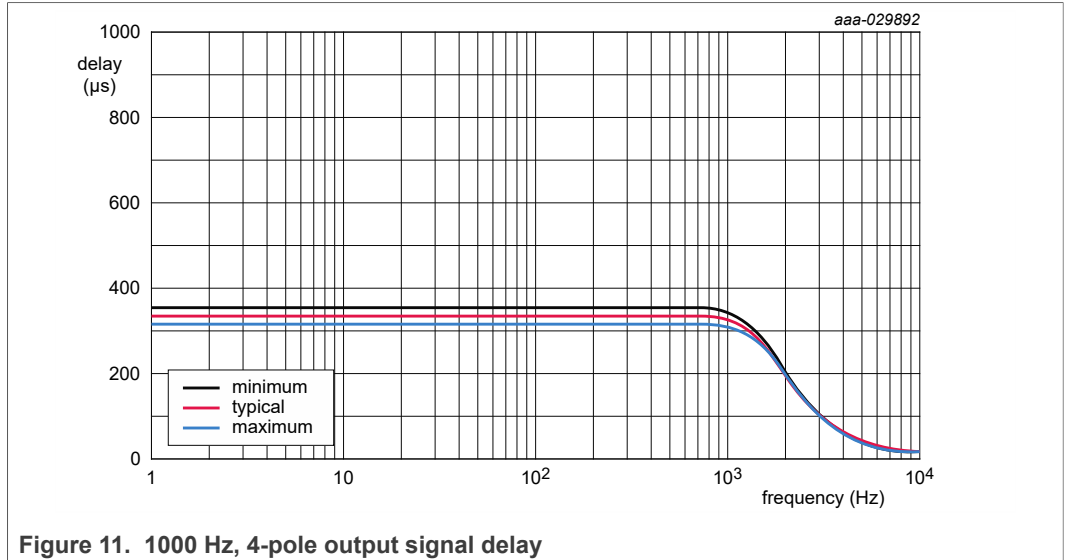


Figure 10. 1000 Hz, 4-pole, low-pass filter response



7.3.3.4 Absolute pressure output data scaling equation

Equation 4 is used to convert absolute pressure readings with the variables as specified in Table 7. Note, the specified values apply only if the P_CAL_ZERO value is set to 0000h.

$$PABS_{kPa} = \frac{PABS_{LSB} - PABSOFF_{LSB}}{PABS_{SENSE}} \tag{4}$$

Where:

- PABS_{kPa} = The absolute pressure output in kPa.
- PABS_{LSB} = The absolute pressure output in LSB.
- PABSOFF_{LSB} = The internal trimmed absolute pressure output value at 0 kPa in LSB.
- PABS_{SENSE} = The trimmed absolute pressure sensitivity in LSB/kPa.

Table 7. Scaling parameters

| Range | Data reading | PABSOFF _{LSB} (LSB) | PABS _{SENSE} (LSB/kPa) |
|------------------|---|------------------------------|---------------------------------|
| 20 kPa - 400 kPa | 12-bit sensor data request ^[1] | 159 | 7 |
| | 16-bit register/data read 62h and 63h | 28990 | 14 |
| | Interrupt threshold registers 46h to 49h | 28990 | 14 |
| | 16-bit sensor data request ^[1] | 2544 | 112 |

[1] SPI mode only. See Section 7.7.8.1 for more details.

7.3.4 Temperature sensor

7.3.4.1 Temperature sensor signal chain

The device includes a temperature sensor for signal compensation and user readability. Figure 12 shows a simplified block diagram. Temperature sensor parameters are specified in Table 104 and Table 105.

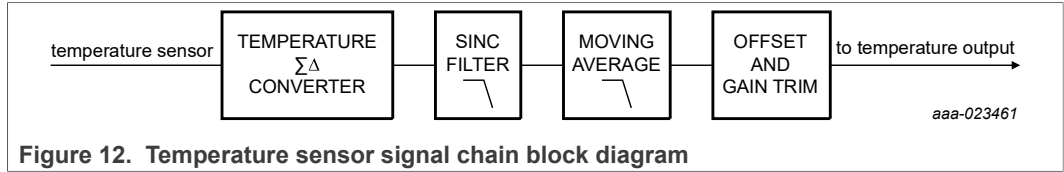


Figure 12. Temperature sensor signal chain block diagram

7.3.4.2 Temperature sensor output scaling equation

Equation 5 is used to convert temperature readings with the variables specified in Table 8.

$$T_{DEGC} = \frac{T_{LSB} - T0_{LSB}}{T_{SENSE}} \tag{5}$$

Where:

T_{DEGC} = The temperature output in degrees C

T_{LSB} = The temperature output in LSB

T_{0LSB} = The expected temperature output in LSB at 0 °C

T_{SENSE} = The expected temperature sensitivity in LSB/°C

Table 8. Temperature conversion variables

| Data reading | T _{0LSB} (LSB) | T _{SENSE} LSB/C) |
|---------------------|-------------------------|---------------------------|
| 8-bit register read | 68 | 1 |

7.3.5 Common mode error detection signal chain

The device includes a continuous pressure transducer common mode error detection. A simplified block diagram is shown in Figure 13. The common mode error signal is compared against the normal absolute pressure signal. If the comparison falls outside pre-determined limits, the CM_ERROR bit in the DSP_STAT register is set. Once the error condition is removed, the CM_ERROR bit is cleared as specified in Section 7.7.15 "DSP_STAT - DSP specific status register (address 60h)".

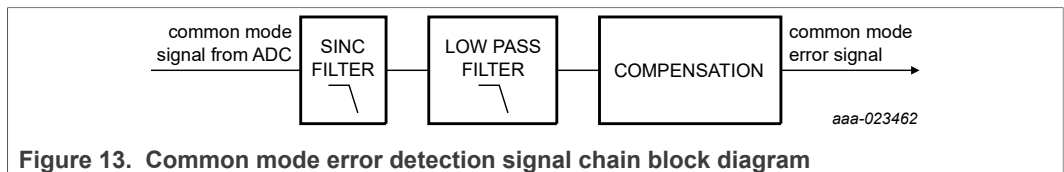


Figure 13. Common mode error detection signal chain block diagram

7.4 Inter-integrated circuit (I²C) interface

The device includes an interface compliant to the NXP I²C-bus specification^[4]. The device operates in client mode and includes support for standard mode, fast mode, and fast mode plus, although the maximum practical operating frequency for I²C in a given system implementation depends on several factors including the pull-up resistor values and the total bus capacitance.

7.4.1 I²C bit transmissions

The state of SDA when SCL is high determines the bit value being transmitted. SDA must be stable when SCL is high and change when SCL is low as shown in [Figure 14](#). After the START signal has been transmitted by the host, the bus is considered busy. Timing for the start condition is specified in [Table 105](#).

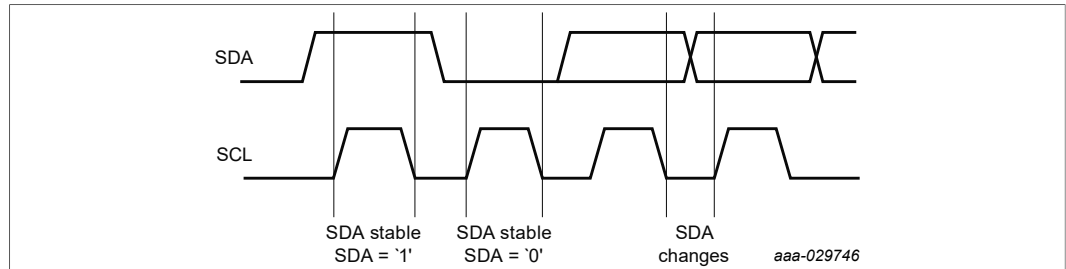


Figure 14. I²C bit transmissions

7.4.2 I²C start condition

A bus operation is always started with a start condition (START) from the host. A START is defined as a high to low transition on SDA while SCL is high as shown in [Figure 15](#). After the START signal has been transmitted by the host, the bus is considered busy. Timing for the start condition is specified in [Table 105](#).

A start condition (START) and a repeat START condition (rSTART) are identical.

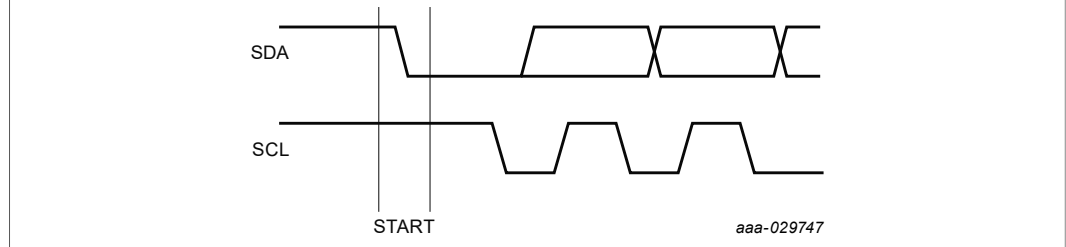


Figure 15. I²C start condition

7.4.3 I²C byte transmission

Data transfers are completed in byte increments. The number of bytes that can be transmitted per transfer is unrestricted. Each byte must be followed by an acknowledge bit ([Section 7.4.4 "I²C acknowledge and not acknowledge transmissions"](#)) from the receiver. Data is transferred with the most significant bit (MSB) first (see [Figure 16](#)). The host generates all clock pulses, including the ninth clock for the acknowledge bit. Timing for the byte transmissions is specified in [Section 7.4.4 "I²C acknowledge and not acknowledge transmissions"](#). All functions for this device are completed within the acknowledge clock pulse. Clock stretching is not used.

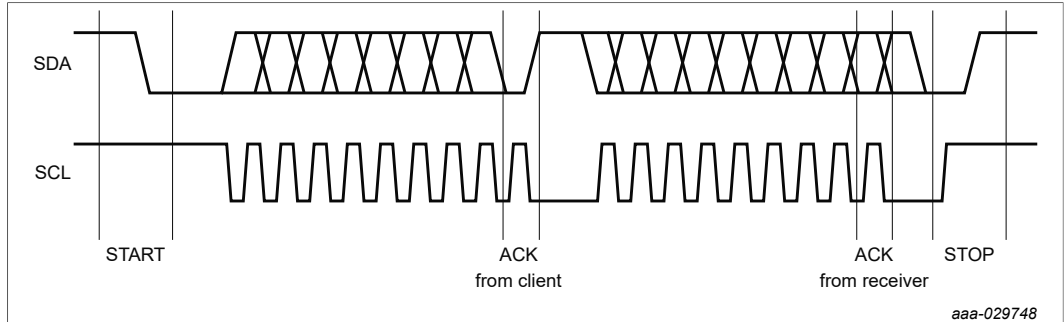


Figure 16. I²C byte transmissions

7.4.4 I²C acknowledge and not acknowledge transmissions

Each byte must be followed by an acknowledge bit (ACK) from the receiver. For an ACK, the transmitter releases SDA during the acknowledge clock pulse and the receiver pulls SDA low during the high portion of the clock pulse. Set up and hold times as specified in [Table 105](#) must also be taken into account.

For a not acknowledge bit (NACK), SDA remains high during the entire acknowledge clock pulse. Five conditions lead to a NACK:

1. No receiver is present on the bus with the transmitted address.
2. The addressed receiver is unable to receive or transmit because it is performing some real-time function and is not ready to start communication with the host.
3. The receiver receives unrecognized data or commands.
4. The receiver cannot receive any more data bytes.
5. The host-receiver signals the end of the transfer to the client transmitter.

Following a NACK, the host can transmit either a STOP to terminate the transfer, or a repeated START to initiate a new transfer.

An example ACK and NACK are shown in [Figure 17](#).

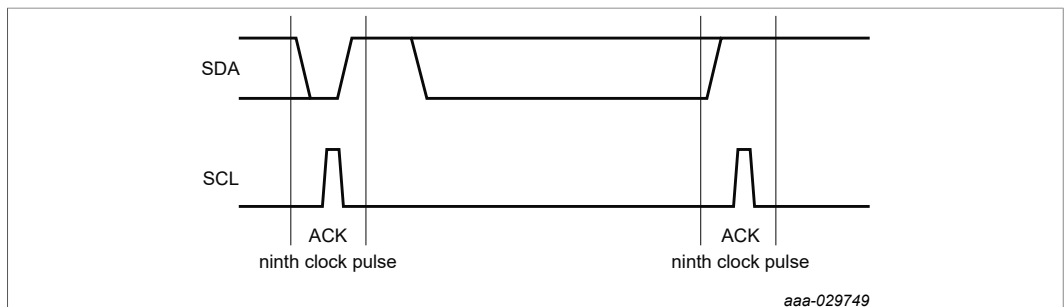


Figure 17. I²C acknowledge and not acknowledge transmission

7.4.5 I²C stop condition

A bus operation is always terminated with a stop condition (STOP) from the host. A STOP is defined as a low to high transition on SDA while SCL is high as shown in [Figure 18](#). After the STOP has been transmitted by the host, the bus is considered free. Timing for the stop condition is specified in [Table 105](#).

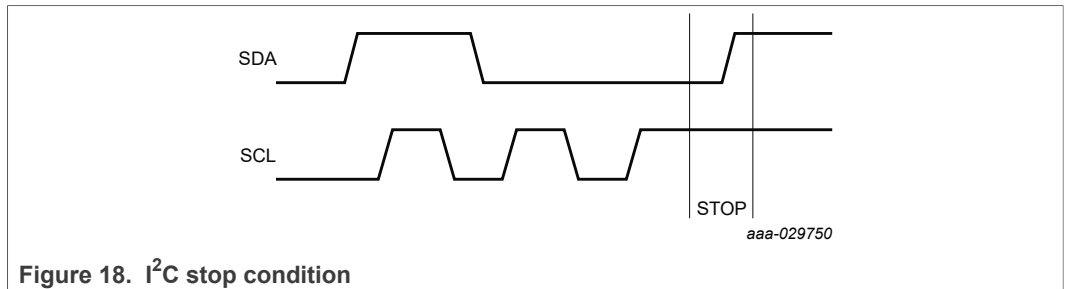


Figure 18. I²C stop condition

7.4.6 I²C register transfers

7.4.6.1 Register write transfers

The device supports I²C register write data transfers. Register write data transfers are constructed as follows:

1. The host transmits a START condition.
2. The host transmits the 7-bit client address.
3. The host transmits a '0' for the read/write bit to indicate a write operation.
4. The client transmits an ACK.
5. The host transmits the register address to be written.
6. The client transmits an ACK.
7. The host transmits the data byte to be written to the register address.
8. The client transmits an ACK.
9. The host transmits a STOP condition.



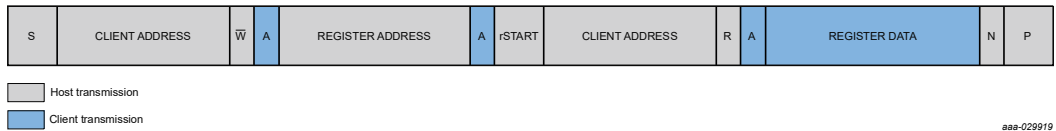
The device automatically increments the register address allowing for multiple register writes to be completed in one transaction. In this case, the register write data transfers are constructed as follows:

1. The host transmits a START condition.
2. The host transmits the 7-bit client address.
3. The host transmits a '0' for the read/write bit to indicate a write operation.
4. The client transmits an ACK.
5. The host transmits the register address to be written.
6. The client transmits an ACK.
7. The host transmits the data byte to be written to the register address.
8. The client transmits an ACK.
9. The host transmits the data byte to be written to the register address +1.
10. The client transmits an ACK.
11. Repeat steps 9 and 10 until all registers are written.
12. The host transmits a STOP condition.

7.4.6.2 Register read transfers

The device supports I²C register read data transfers. Register read data transfers are constructed as follows:

1. The host transmits a START condition.
2. The host transmits the 7-bit client address.
3. The host transmits a '0' for the read/write bit to indicate a write operation.
4. The client transmits an ACK.
5. The host transmits the register address to be read.
6. The client transmits an ACK.
7. The host transmits a repeat START condition.
8. The host transmits the 7-bit client address.
9. The host transmits a '1' for the read/write bit to indicate a read operation.
10. The client transmits an ACK.
11. The client transmits the data from the register addressed.
12. The host transmits a NACK.
13. The host transmits a STOP condition.



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7.4.6.3 Sensor data register read wrap around

The device includes automatic sensor data register read wrap-around features to optimize the number of I²C transactions necessary for continuous reads of sensor data. Depending on the state of the SIDx_EN bits in the SOURCEID_0 and SOURCEID_1 registers, the register address automatically wraps back to the DEVSTAT_COPY register as shown in Table 9.

Table 9. Sensor data register read wrap-around description

| SID1_EN | SID0_EN | Address increment and wrap-around effect | Optimized register-read sequence |
|---------|---------|---|--|
| 0 | 0 | Address wraps around from FFh to 00h | None |
| 0 | 1 | Address wraps from 63h (SNSDATA0_H) to 61h (DEVSTAT_COPY) | DEVSTAT_COPY, SNSDATA0_L, SNSDATA0_H |
| 1 | 0 | Address wraps from 65h (SNSDATA1_H) to 61h (DEVSTAT_COPY) | DEVSTAT_COPY, SNSDATA0_L, SNSDATA0_H, SNSDATA1_L, SNSDATA1_H |
| 1 | 1 | Address wraps from 69h (SNSDATA0_TIME3) to 61h (DEVSTAT_COPY) | DEVSTAT_COPY, SNSDATA0_L, SNSDATA0_H, SNSDATA1_L, SNSDATA1_H, SNSDATA0_TIME0, SNSDATA0_TIME1, SNSDATA0_TIME2, SNSDATA0_TIME3 |

7.4.7 I²C timing diagram

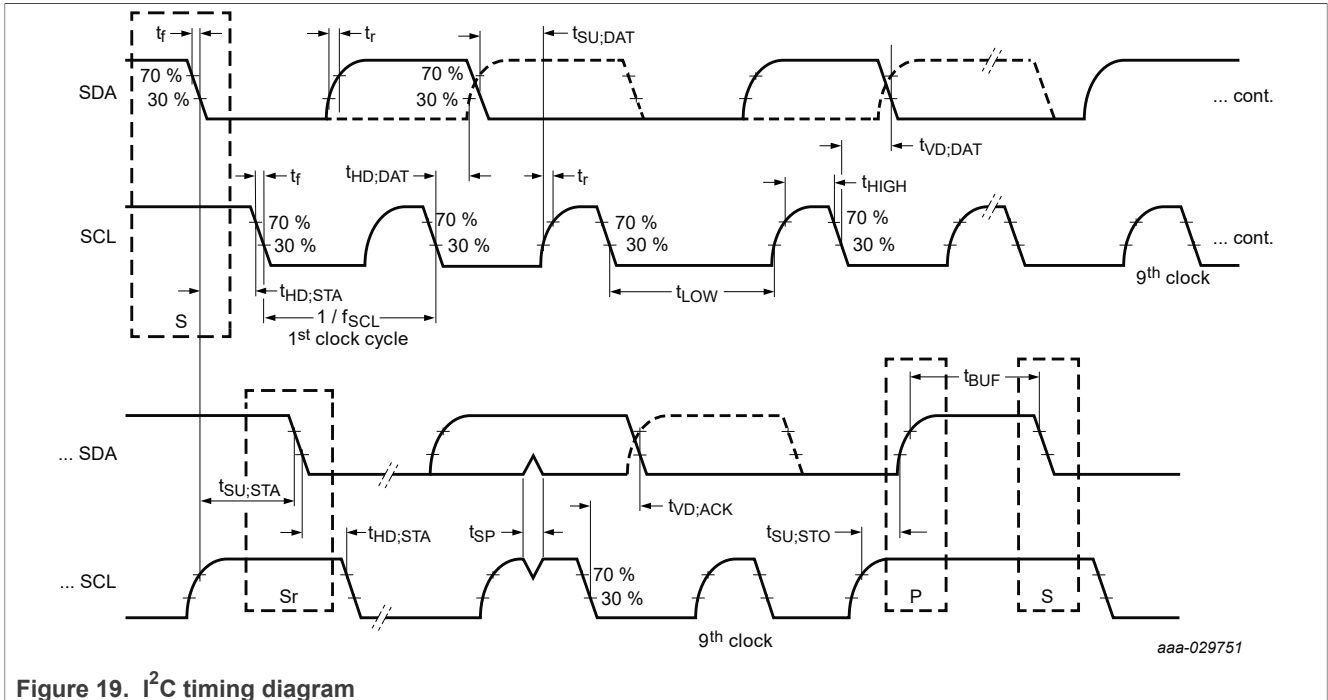


Figure 19. I²C timing diagram

7.5 Standard 32-bit SPI protocol

The device includes a standard SPI protocol requiring 32-bit data packets. The device is a client device and requires a low base clock value (CPOL = 0) with data captured on the rising edge of the clock and data propagated on the falling edge of the clock (CPHA = 0). The most significant bit is transferred first (MSB first). SPI transfers are completed through a sequence of two phases. During the first phase, the command is transmitted from the SPI host to the device. During the second phase, response data is transmitted from the client device. MOSI and SCLK transitions are ignored when SS_B is not asserted.

Table 11. SPI command summary

| C[3:0] | | | | Command type | Data source SOURCEID[2:0] = C[3:1] ^[1] |
|--------|---|---|---|--|---|
| 0 | 0 | 0 | 0 | Unused Command (reserved for error response) | NA |
| 0 | 0 | 0 | 1 | Sensor Data Request | SOURCEID = 0h |
| 0 | 0 | 1 | 0 | reserved Command | NA |
| 0 | 0 | 1 | 1 | Sensor Data Request | SOURCEID = 1h |
| 0 | 1 | 0 | 0 | reserved Command | NA |
| 0 | 1 | 0 | 1 | Sensor Data Request | SOURCEID = 2h |
| 0 | 1 | 1 | 0 | reserved Command | NA |
| 0 | 1 | 1 | 1 | Sensor Data Request | SOURCEID = 3h |
| 1 | 0 | 0 | 0 | Register Write Request ^[2] | NA |
| 1 | 0 | 0 | 1 | Sensor Data Request | SOURCEID = 4h |
| 1 | 0 | 1 | 0 | reserved Command | NA |
| 1 | 0 | 1 | 1 | Sensor Data Request | SOURCEID = 5h |
| 1 | 1 | 0 | 0 | Register Read Request ^[3] | NA |
| 1 | 1 | 0 | 1 | Sensor Data Request | SOURCEID = 6h |
| 1 | 1 | 1 | 0 | Reserved Command | NA |
| 1 | 1 | 1 | 1 | Sensor Data Request | SOURCEID = 7h |

[1] Source identification code matching the value set in the SOURCEID_X field in register 1Ah and 1Bh for the requested sensor data. Also see Section 7.5.3.3.2 "Sensor data request response message format", Table 22 and Table 24.

[2] See Section 7.5.3.2.1.

[3] See Section 7.5.3.1.1.

7.5.2 SPI response format

Table 12. SPI response format

MSB: bit 31; LSB: bit 0

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--|----|---------------------|----|---|----|---|----|----|----|----|----|----|----|--|----|------------------|----|----------|----|----------------------|----|------------------|---|---|---|---|---|---|---|---|---|
| Response to Register Request | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | | Basic Status | | Unused Data 0h | | Register data: contents of RA[7:1] high byte | | | | | | | | Register data: contents of RA[7:1] low byte | | | | | | | | 8-bit CRC | | | | | | | | | |
| C[0], [3:1] | | ST[1:0] | | 0 0 | | RD[15:8] | | | | | | | | RD[7:0] | | | | | | | | CRC[7:0] | | | | | | | | | |
| Response to Sensor Data Request | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | | Basic Status | | Sensor Data | | | | | | | | | | Detail Status | | 8-bit CRC | | | | | | | | | | | | | | | |
| C[0], [3:1] | | ST[1:0] | | SD[11:0] | | | | | | | | | | Optional SD resolution | | SF[1:0] | | CRC[7:0] | | | | | | | | | | | | | |
| Error Response to Register Request | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | | Basic Status | | Unused Data = 0000h | | | | | | | | | | | | | | | | Detail Status | | 8-bit CRC | | | | | | | | | |
| C[0], [3:1] | | 1 1 | | 0 | | | | | | | | | | | | | | | | SF[1:0] | | CRC[7:0] | | | | | | | | | |
| Error Response to Sensor Data Request With Sensor Data | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | | Basic Status | | Sensor Data | | | | | | | | | | Detail Status | | 8-bit CRC | | | | | | | | | | | | | | | |
| C[0], [3:1] | | 1 1 | | SD[11:0] | | | | | | | | | | Optional SD resolution | | SF[1:0] | | CRC[7:0] | | | | | | | | | | | | | |
| Error Response to Sensor Data Request Without Sensor Data | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command | | Basic Status | | Unused Data = 0000h | | | | | | | | | | | | | | | | Detail Status | | 8-bit CRC | | | | | | | | | |
| 0 0 0 0 | | 1 1 | | x 0 | | | | | | | | | | | | | | | | SF[1:0] | | CRC[7:0] | | | | | | | | | |

7.5.3 Command summary

7.5.3.1 Register read command

The device supports a register read command. The register read command uses the upper 7 bits of the addresses defined in [Section 7.6 "User-accessible data array"](#) to address 8-bit registers in the register map.

The response to a register read command is shown in [Section 7.5.3.1.2 "Register read response message format"](#). The response is transmitted on the next SPI message if and only if all of the following conditions are met:

- No SPI error is detected (see [Section 7.5.5.3 "SPI error"](#))
- No MISO error is detected (see [Section 7.5.5.4 "SPI data output verification error"](#))

If these conditions are met, the device responds to the register read request as shown in [Section 7.5.3.1.2 "Register read response message format"](#). Otherwise, the device responds with the error response as defined in [Section 7.5.5.2 "Detailed status field"](#). The register read response includes the register contents at the rising edge of SS_B for the register read command.

7.5.3.1.1 Register read command message format

Table 13. Register read command message format

MSB: bit 31; LSB: bit 0

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------------------|----|----|----|-----------------------|----|----|----|------------------|----|----|----|----|----|----|----|---------------|----|----|----|----|----|---|---|-----------|---|---|---|---|---|---|---|---|---|----------|--|--|--|--|--|--|--|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | | | | | | | | |
| Register access command | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command C[3:0] | | | | Fixed bits: must = 0h | | | | Register address | | | | | | | | Register data | | | | | | | | 8-bit CRC | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | RA[7:1] | | | | | | | | RA[0] | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | CRC[7:0] | | | | | | | |

Table 14. Register read command message bit field descriptions

| Bit field | Definition |
|-----------|---|
| C[3:0] | Register read command = '1100' |
| RA[7:0] | RA[7:1] contains the word address of the register to be read. |
| CRC[7:0] | Read CRC Section |

7.5.3.1.2 Register read response message format

Table 15. Register read response message format

MSB: bit 31; LSB: bit 0

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------------------|----|----|----|--------------|----|----------------|----|--|----|----|----|----|----|----|----|---|----|----|----|----|----|---|---|-----------|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Register access command | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command C[0], [3:1] | | | | Basic Status | | Unused Data 0h | | Register data: contents of RA[7:1] high byte | | | | | | | | Register data: contents of RA[7:1] low byte | | | | | | | | 8-bit CRC | | | | | | | |
| 0 | 1 | 1 | 0 | ST[1:0] | | 0 | 0 | RD[15:8] | | | | | | | | RD[7:0] | | | | | | | | CRC[7:0] | | | | | | | |

Table 16. Register read response message bit field descriptions

| Bit field | Definition |
|-------------|---|
| C[0], [3:1] | Register Read Command = '0110' |
| ST[1:0] | Status |
| RD[15:8] | The contents of the register addressed by RA[7:1] high byte (RA[0] = 1) |
| RD[7:0] | The contents of the register addressed by RA[7:1] low byte (RA[0] = 0) |
| CRC[7:0] | 8-bit CRC |

7.5.3.2 Register write command

The device supports a register write command. The register write command writes the value specified in RD[7:0] to the register addressed by RA[7:0].

The response to a register write command is shown in [Section 7.5.3.2.2 "Register write response message format"](#). The register write is executed and a response is transmitted on the next SPI message if and only if all of the following conditions are met:

- No SPI error is detected (see [Section 7.5.5.3 "SPI error"](#))
- No MISO error is detected (see [Section 7.5.5.4 "SPI data output verification error"](#))
- The ENDINIT bit is cleared.
 - This applies to all registers except for the RESET[1:0] bits in the DEVLOCK_WR register
- No invalid register request is detected as described below.

If these conditions are met, the register write is executed and the device responds to the register write request as shown in [Section 7.5.3.2.2 "Register write response message format"](#). Otherwise, no register is written and the device responds with the error response as defined in [Section 7.5.2 "SPI response format"](#). The register is not written until the transfer during which the register write was requested has been completed.

A register write command to a read-only register is not executable, but results in a valid response.

7.5.3.2.1 Register write command message format

Table 17. Register write command message format

MSB: bit 31; LSB: bit 0

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
|-------------------------|----|----|----|-----------------------|----|----|----|------------------|----|----|----|----|----|----|----|---------------|----|---------|----|----|----|---|---|-----------|---|----------|---|---|---|---|---|--|--|
| Register access command | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command C[3:0] | | | | Fixed bits: must = 0h | | | | Register address | | | | | | | | Register data | | | | | | | | 8-bit CRC | | | | | | | | | |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | RA[7:1] | | | | | | | | RA[0] | | RD[7:0] | | | | | | | | CRC[7:0] | | | | | | | |

Table 18. Register write command message bit field descriptions

| Bit field | Definition |
|-----------|---|
| C[3:0] | Register write command = '1000' |
| RA[7:0] | RA[7:1] contains the byte address of the register to be written |
| RD[7:0] | RD[7:0] contains the data byte to be written to address RA[7:0] |
| CRC[7:0] | 8-bit CRC |

7.5.3.2.2 Register write response message format

Table 19. Register write response message format

MSB: bit 31; LSB: bit 0

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------------|----|----|----|---------------------|----|-----------------------|----|---|----|----|----|----|----|----|----|--|----|----|----|----|----|---|---|------------------|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Register access command | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Command C[0], [3:1] | | | | Basic Status | | Unused Data 0h | | Register data: contents of RA[7:1] high byte | | | | | | | | Register data: contents of RA[7:1] low byte | | | | | | | | 8-bit CRC | | | | | | | |
| 0 | 1 | 0 | 0 | ST[1:0] | | 0 | 0 | RD[15:8] | | | | | | | | RD[7:0] | | | | | | | | CRC[7:0] | | | | | | | |

Table 20. Register write response message bit field descriptions

| Bit field | Definition |
|-------------|---|
| C[0], [3:1] | Register Read Command = '0100' |
| ST[1:0] | Status |
| RD[15:8] | The contents of the register addressed by RA[7:1] high byte (RA[0] = 1) |
| RD[7:0] | The contents of the register addressed by RA[7:1] low byte (RA[0] = 0) |
| CRC[7:0] | 8-bit CRC |

7.5.3.3 Sensor data request commands

The device supports standard sensor data request commands. The sensor data request command format is described in [Section 7.5.3.3.1 "Sensor data request command message format"](#). The response to a sensor data request is shown in [Section 7.5.3.3.2 "Sensor data request response message format"](#). The response is transmitted on the next SPI message subject to the error handling conditions specified in [Section 7.5.5 "Exception handling"](#). The sensor data included in the response is the sensor data at the falling edge of SS_B for the sensor data request response.

7.5.3.3.1 Sensor data request command message format

Table 21. Sensor data request command message format

MSB: bit 31; LSB: bit 0

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|------------------|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Command | | | | Fixed bits: must = 0 0000h | | | | | | | | | | | | | | | | | | | | 8-bit CRC | | | | | | | |
| C[3:0] | | | | 0 | | | | | | | | | | | | | | | | | | | | CRC[7:0] | | | | | | | |

Table 22. Sensor data request command message bit field descriptions

| Bit field | Definition |
|------------------------|--|
| C[0] | Sensor data request command = '1' |
| C[3:1] = SOURCEID[2:0] | Source identification code for the requested sensor data |
| CRC[7:0] | 8-bit CRC |

7.5.3.3.2 Sensor data request response message format

Table 23. Sensor data request response message format – 12 bit data length

MSB: bit 31; LSB: bit 0

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------|----|----|----|--------------|----|-------------|----|----|----|----|----|----|------------------------|----|----|----|---------------|----|-----------|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Command | | | | Basic Status | | Sensor Data | | | | | | | | | | | Detail Status | | 8-bit CRC | | | | | | | | | | | | |
| C[0], [3:1] | | | | ST[1:0] | | SD[11:0] | | | | | | | Optional SD resolution | | | | SF[1:0] | | CRC[7:0] | | | | | | | | | | | | |

Table 24. Sensor data request response message bit field descriptions

| Bit field | Definition |
|------------------------|---|
| C[0] | Sensor data request command = '1' |
| C[3:1] = SOURCEID[2:0] | Source identification code for the requested sensor data |
| ST[1:0] | Basic Status |
| SD[11:0] | Sensor data |
| Optional SD resolution | Optional for 16-bit Sensor data. Refer to Section 7.3.3.4 . |
| SF[1:0] | Detailed status |
| CRC[7:0] | 8-bit CRC |

7.5.3.4 Reserved commands

The device responds to reserved commands on the next SPI message subject to the error handling conditions specified in [Section 7.5.5 "Exception handling"](#).

7.5.3.4.1 Reserved command message format

Table 25. Reserved command message format

MSB: bit 31; LSB: bit 0

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|----------|-----------|---|---|---|---|---|---|--|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Command | | | | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | 8-bit CRC | | | | | | | |
| 0 | 0 | 0 | 0 | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | CRC[7:0] | | | | | | | | |
| 0 | 0 | 1 | 0 | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | CRC[7:0] | | | | | | | | |
| 0 | 1 | 0 | 0 | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | CRC[7:0] | | | | | | | | |
| 0 | 1 | 1 | 0 | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | CRC[7:0] | | | | | | | | |
| 1 | 0 | 1 | 0 | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | CRC[7:0] | | | | | | | | |
| 1 | 1 | 1 | 0 | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | CRC[7:0] | | | | | | | | |

Table 26. Reserved command message bit field descriptions

| Bit field | Definition |
|-----------|------------------|
| C[3:0] | Reserved command |
| CRC[7:0] | 8-bit CRC |

7.5.3.4.2 Reserved command response message format

Table 27. Reserved command response message format

MSB: bit 15; LSB: bit 0

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------------|----|----|----|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----------|---|---|----------|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Command Echo | | | | Data | | | | | | | | | | | | | | | | | | 8-bit CRC | | | | | | | | | |
| x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | CRC[7:0] | | | | | | |

Table 28. Reserved command response message bit field descriptions

| Bit field | Definition |
|--------------|----------------------------------|
| Command echo | Reserved command echo. Undefined |
| Data | Response data. Undefined |
| CRC[7:0] | 8-bit CRC |

7.5.4 Error checking

7.5.4.1 Default 8-bit CRC

7.5.4.1.1 Command error checking

The device calculates an 8-bit CRC on the entire 32 bits of each command. Message data is entered into the CRC calculator MSB first, consistent with the transmission order of the message. If the calculated CRC does not match the transmitted CRC, the command is ignored and the device responds with the SPI error response.

The CRC decoding procedure is as follows:

1. A seed value is preset into the LSB of the shift register.
2. Using a serial CRC calculation method, the receiver rotates the received message and CRC into the LSB of the shift register in the order received (MSB first).
3. When the calculation on the last bit of the CRC is rotated into the shift register, the shift register contains the CRC check result.
4. If the shift register contains all zeros, the CRC is correct.
5. If the shift register contains a value other than zero, the CRC is incorrect.

The CRC polynomial and seed are shown in [Table 29](#).

Table 29. SPI Command Message CRC

| SPICRCSEED[3:0] | Default Polynomial | Default non-direct Seed |
|-----------------|---------------------------------|-------------------------|
| 0000 | $x^8 + x^5 + x^3 + x^2 + x + 1$ | 1111 1111 |
| non-zero | $x^8 + x^5 + x^3 + x^2 + x + 1$ | 1111 SPICRCSEED[3:0] |

7.5.4.1.2 Response error checking

The device calculates a CRC on the entire 32 bits of each response. Message data is entered into the CRC calculator MSB first, consistent with the transmission order of the message.

The CRC encoding procedure is as follows:

1. A seed value is preset into the LSB of the shift register.
2. Using a serial CRC calculation method, the transmitter rotates the transmitted message and CRC into the LSB of the shift register (MSB first).

3. Following the transmitted message, the transmitter feeds 8 zeros into the shift register, to match the length of the CRC.
4. When the last zero is fed into the input adder, the shift register contains the CRC.
5. The CRC is transmitted.

The CRC polynomial and seed are shown in [Table 30](#).

Table 30. SPI Response Message CRC

| SPICRCSEED[3:0] | Default Polynomial | Default non-direct Seed |
|-----------------|---------------------------------|-------------------------|
| 0000 | $x^8 + x^5 + x^3 + x^2 + x + 1$ | 1111 1111 |
| nonzero | $x^8 + x^5 + x^3 + x^2 + x + 1$ | 1111 SPICRCSEED[3:0] |

7.5.5 Exception handling

After POR, there a supply error flag is set. Expected initial responses with first 4 commands are shown in [Table 31](#).

Table 31. Expected initial responses after $t_{POR_DataValid}$ post POR

| Command | Response |
|------------------------------|--|
| Command 1 (DEVSTAT READ) | Ignore response 1 |
| Command 2 (DEVSTAT READ) | Ignore response 2 |
| Command 3 (DEVSTAT READ) | Ignore response 3 |
| Command 4 (ANY USER COMMAND) | Response 4 - 0X6080XXXX ^[1] |

[1] Response 4 is 0x6080XXXX after $t_{POR_DataValid}$ wait time from POR. Otherwise only after t_{POR_I2C/POR_SPI} wait time from POR, response would be 0x6081XXXX due to DEVINIT bit still set to 1.

Before soft reset, write SOURCEID_0 in address 1Ah with a non-zero value. Address 1Ah is read back to check soft reset sanity.

During soft reset, flash contents are reloaded into the mirror registers and during this process the supply error flag can get set based on device variation, temperature, and so forth. After 1 ms delay, the expected initial response from the first 5 commands are shown in [Table 32](#).

Table 32. Expected initial responses after $t_{POR_DataValid}$ post soft reset

| Command | Response |
|------------------------------|--|
| Command 1 (DEVSTAT READ) | Ignore response 1 |
| Command 2 (DEVSTAT READ) | Ignore response 2 |
| Command 3 (DEVSTAT READ) | Ignore response 3 |
| Command 4 (SOURCEID_0 READ) | Response 4 - 0X6080XXXX ^[1] |
| Command 5 (ANY USER COMMAND) | Response 5 - valid response with reset value of SOURCEID_0 |

[1] Response 4 is 0x6080XXXX after $t_{POR_DataValid}$ wait time from soft reset. Otherwise only after t_{POR_I2C/POR_SPI} wait time from soft reset, response 4 would be 0x6081XXXX due to DEVINIT bit still set to 1.

7.5.5.1 Basic status field

All responses include a status field (ST[1:0]) that includes the general status of the device and transmitted data as described below. The contents of the status field is

a representation of the device status at the rising edge of SS_B for the previous SPI command.

Table 33. Basic status field for responses to register commands

| ST[1:0] | | Status | Description | SF[1:0] | | Priority |
|---------|---|--------------------------|---|-----------------------|---|----------|
| 0 | 0 | Device in Initialization | Device in initialization (ENDINIT not set) | 0 | 0 | 3 |
| 0 | 1 | Normal Mode | Normal mode(ENDINIT set) | 0 | 0 | 4 |
| 1 | 0 | Self-test | Self-test(ST_CTRL[3:0] not equal to '0000') | 0 | 0 | 2 |
| 1 | 1 | Internal Error Present | Detailed Status Field | Detailed Status Field | | 1 |

7.5.5.2 Detailed status field

The response to sensor data requests includes a detailed status field (SF[1:0]). The contents of the detailed status field is a representation of the device status at the rising edge of SS_B for the previous SPI command.

Table 34. Detailed status bit field descriptions

| SF[1:0] | | Status Sources | DEVSTAT State |
|---------|---|---|--|
| 0 | 0 | CM_ERROR Temperature error | Bit set in DSP_STAT Bit set in DEVSTAT2 |
| 0 | 1 | User OTP memory error (UF2 or UF1) User R/W memory error (UF2) NXP OTP Memory error | U_OTP_ERR set in DEVSTAT2 U_RW_ERR set in DEVSTAT2 F_OTP_ERR set in DEVSTAT2 |
| 1 | 0 | Test Mode active Supply error Reset error | TESTMODE bit set in DEVSTAT Bit set in DEVSTAT1 DEVRES set |
| 1 | 1 | MISO error SPI error | Bit set in DEVSTAT3 N/A |

7.5.5.3 SPI error

The following external SPI conditions result in a SPI error:

- SCLK is high when SS_B is asserted.
- The number of SCLK rising edges detected while SS_B is asserted is not equal to 16.
- SCLK is high when SS_B is deasserted.
- CRC error is detected (MOSI).
- A register write command to any register other than the DEVLOCK_WR register is received while ENDINIT is set.

If a SPI error is detected, the device responds with the error response as described in [Section 7.5.5.2 "Detailed status field"](#) with the detailed status field set to "SPI Error" as defined in [Section 7.5.5.1 "Basic status field"](#).

7.5.5.4 SPI data output verification error

The device includes a function to verify the integrity of the data output to the MISO pin. The function compares the data transmitted on the MISO pin to the data intended to be transmitted. If any one bit does not match, a SPI MISO mismatch fault is detected and the MISO_ERR flag in the DEVSTAT2 register is set.

If a valid sensor data request message is received during the SPI transfer with the MISO mismatch failure, the request is ignored and the device responds with the error response

as described in [Section 7.5.5.2 "Detailed status field"](#) with the detailed status field set to "SPI Error" as defined in [Section 7.5.5.1 "Basic status field"](#) during the subsequent SPI message.

If a valid register write request message is received during the SPI transfer with the MISO mismatch failure, the register write is completed as requested, but the device responds with the error response as described in [Section 7.5.5.2 "Detailed status field"](#) with the detailed status field set to "SPI Error" as defined in [Section 7.5.5.1 "Basic status field"](#) during the subsequent SPI message.

If a valid register read request message is received during the SPI transfer with the MISO mismatch failure, the register read is ignored and the device responds with the error response as described in [Section 7.5.5.2 "Detailed status field"](#) with the detailed status field set to "SPI Error" as defined in [Section 7.5.5.1 "Basic status field"](#), during the subsequent SPI message.

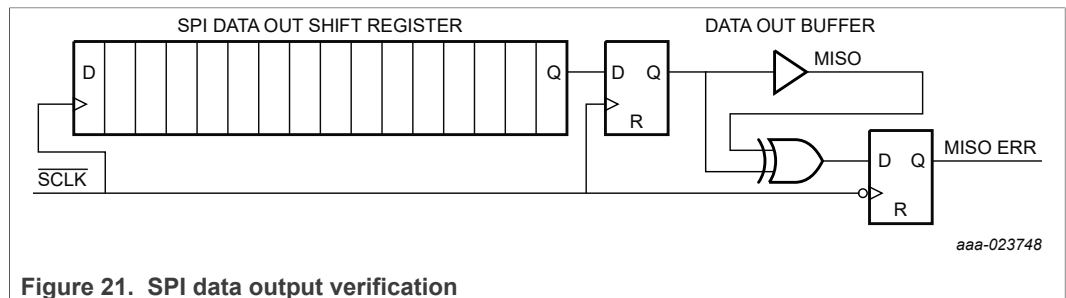


Figure 21. SPI data output verification

7.5.6 SPI timing diagram

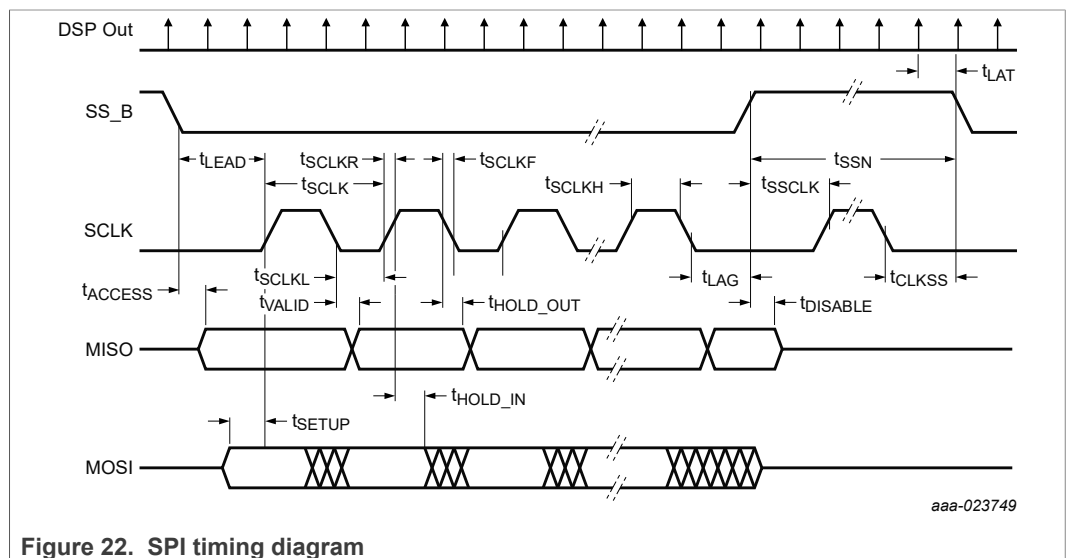


Figure 22. SPI timing diagram

7.6 User-accessible data array

A user-accessible data array allows each device to be customized. The array consists of a one time programmable (OTP) factory-programmable block, an OTP user-programmable block, and read-only registers for data and device status. The OTP blocks incorporate independent data verification. In order to perform the OTP, a custom platform is typically used prior to PCB assembly since the VPP voltage required is much higher than the nominal supply as shown in [Table 103](#). See application note AN12727^[3].

Table 35. User-accessible data — sensor specific information

| Address | Register | Type ^[1] | Bit | | | | | | | |
|------------------------------------|--------------|---------------------|--------------------|----------------|------------------|-------------|-----------------|------------|------------------|----------|
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| General device information | | | | | | | | | | |
| 00h | COUNT | R | COUNT[7:0] | | | | | | | |
| 01h | DEVSTAT | R | DSP_ERR | reserved | COMM_ERR | MEMTEMP_ERR | SUPPLY_ERR | TESTMODE | DEVRES | DEVINIT |
| 02h | DEVSTAT1 | R | VCCUV_ERR | reserved | reserved | reserved | INTREGA_ERR | INTREG_ERR | INTREGF_ERR | CONT_ERR |
| 03h | DEVSTAT2 | R | F_OTP_ERR | U_OTP_ERR | U_RW_ERR | U_W_ACTIVE | reserved | TEMP0_ERR | reserved | reserved |
| 04h | DEVSTAT3 | R | MISO_ERR | reserved | reserved | reserved | reserved | reserved | reserved | reserved |
| 05h to 0Dh | reserved | R | reserved | | | | | | | |
| 0Eh | TEMPERATURE | R | TEMP[7:0] | | | | | | | |
| 0Fh | reserved | R | reserved | | | | | | | |
| Communication information | | | | | | | | | | |
| 10h | DEVLOCK_WR | R/W | ENDINIT | reserved | reserved | reserved | SUP_ERR_DIS | reserved | RESET[1:0] | |
| 11h | WRITE_OTP_EN | R/W | UOTP_WR_INIT | reserved | | | EX_COMMTYPE | EX_PADDR | UOTP_REGION[1:0] | |
| 12h to 13h | reserved | R/W | reserved | | | | | | | |
| 14h | UF_REGION_W | R/W | REGION_LOAD[3:0] | | | | 0 | 0 | 0 | 0 |
| 15h | UF_REGION_R | R | REGION_ACTIVE[3:0] | | | | 0 | 0 | 0 | 0 |
| 16h to 19h | reserved | UF2 | reserved | | | | | | | |
| 1Ah | SOURCEID_0 | UF2 | SID0_EN | reserved | | | SOURCEID_0[3:0] | | | |
| 1Bh | SOURCEID_1 | UF2 | SID1_EN | reserved | | | SOURCEID_1[3:0] | | | |
| 1Ch to 3Ch | reserved | UF2 | reserved | | | | | | | |
| 3Dh | SPI_CFG | UF2 | reserved | DATASIZE | SPI_CRC_LEN[1:0] | | SPICRCSEED[3:0] | | | |
| 3Eh | WHO_AM_I | UF2 | WHO_AM_I[7:0] | | | | | | | |
| 3Fh | I2C_ADDRESS | UF2 | I2C_ADDRESS[7:0] | | | | | | | |
| Sensor specific information | | | | | | | | | | |
| 40h | DSP_CFG_U1 | UF2 | LPF[3:0] | | | | reserved | reserved | reserved | reserved |
| 41h | reserved | UF2 | reserved | | | | | | | |
| 42h | DSP_CFG_U3 | UF2 | reserved | DATATYPE0[1:0] | | reserved | DATATYPE1[1:0] | | reserved | reserved |
| 43h | DSP_CFG_U4 | UF2 | reserved | reserved | reserved | reserved | reserved | INT_OUT | reserved | reserved |
| 44h | DSP_CFG_U5 | UF2 | ST_CTRL[3:0] | | | | reserved | reserved | reserved | reserved |
| 45h | INT_CFG | UF2 | reserved | | INT_PS[1:0] | | INT_POLARITY | reserved | | |
| 46h | P_INT_HI_L | UF2 | P_INT_HI_L[7:0] | | | | | | | |
| 47h | P_INT_HI_H | UF2 | P_INT_HI_H[15:8] | | | | | | | |
| 48h | P_INT_LO_L | UF2 | P_INT_LO_L[7:0] | | | | | | | |
| 49h | P_INT_LO_H | UF2 | P_INT_LO_H[15:8] | | | | | | | |
| 4Ah to 4Bh | reserved | UF2 | reserved | | | | | | | |
| 4Ch | P_CAL_ZERO_L | UF2 | P_CAL_ZERO_L[7:0] | | | | | | | |
| 4Dh | P_CAL_ZERO_H | UF2 | P_CAL_ZERO_H[15:8] | | | | | | | |
| 4Eh to 5Eh | reserved | UF2 | reserved | | | | | | | |

Table 35. User-accessible data — sensor specific information...continued

| Address | Register | Type ^[1] | Bit | | | | | | | |
|---|----------------|---------------------|----------------------|-------------------|----------|-------------|--------------|-----------|----------|----------|
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 5Fh | CRC_UF2 | F | LOCK_UF2 | 0 | 0 | 0 | CRC_UF2[3:0] | | | |
| 60h | DSP_STAT | R | reserved | | | | ST_INCMPLT | ST_ACTIVE | CM_ERROR | ST_ERROR |
| 61h | DEVSTAT_COPY | R | DSP_ERR | reserved | COMM_ERR | MEMTEMP_ERR | SUPPLY_ERR | TESTMODE | DEVRES | DEVINT |
| 62h | SNSDATA0_L | R | SNSDATA0_L[7:0] | | | | | | | |
| 63h | SNSDATA0_H | R | SNSDATA0_H[15:8] | | | | | | | |
| 64h ^[2] | SNSDATA1_L | R | SNSDATA1_L[7:0] | | | | | | | |
| 65h ^[2] | SNSDATA1_H | R | SNSDATA1_H[15:8] | | | | | | | |
| 66h | SNSDATA0_TIME0 | R | SNSDATA0_TIME[7:0] | | | | | | | |
| 67h | SNSDATA0_TIME1 | R | SNSDATA0_TIME[15:8] | | | | | | | |
| 68h | SNSDATA0_TIME2 | R | SNSDATA0_TIME[23:16] | | | | | | | |
| 69h | SNSDATA0_TIME3 | R | SNSDATA0_TIME[31:24] | | | | | | | |
| 6Ah | SNSDATA0_TIME4 | R | SNSDATA0_TIME[39:32] | | | | | | | |
| 6Bh | SNSDATA0_TIME5 | R | SNSDATA0_TIME[47:40] | | | | | | | |
| 6Ch | P_MAX_L | R | P_MAX[7:0] | | | | | | | |
| 6Dh | P_MAX_H | R | P_MAX[15:8] | | | | | | | |
| 6Eh | P_MIN_L | R | P_MIN[7:0] | | | | | | | |
| 6Fh | P_MIN_H | R | P_MIN[15:8] | | | | | | | |
| 70h to 77h | reserved | R | reserved | | | | | | | |
| 78h | FRT0 | R | FRT[7:0] | | | | | | | |
| 79h | FRT1 | R | FRT[15:8] | | | | | | | |
| 7Ah | FRT2 | R | FRT[23:16] | | | | | | | |
| 7Bh | FRT3 | R | FRT[31:24] | | | | | | | |
| 7Ch | FRT4 | R | FRT[39:32] | | | | | | | |
| 7Dh | FRT5 | R | FRT[47:40] | | | | | | | |
| 7Eh to 9Fh | reserved | R | reserved | | | | | | | |
| Sensor specific information - user readable registers with OTP | | | | | | | | | | |
| A0h to AEh | reserved | F | reserved | | | | | | | |
| AFh | CRC_F_A | F | LOCK_F_A | REGA_BLOCKID[2:0] | | | CRC_F_A[3:0] | | | |
| B0h to BEh | reserved | F | reserved | | | | | | | |
| BFh | CRC_F_B | F | LOCK_F_B | REGB_BLOCKID[2:0] | | | CRC_F_B[3:0] | | | |
| Traceability Information | | | | | | | | | | |
| C0h | ICTYPEID | F | ICTYPEID[7:0] | | | | | | | |
| C1h | ICREVID | F | ICREVID[7:0] | | | | | | | |
| C2h | ICMFGID | F | ICMFGID[7:0] | | | | | | | |
| C3h | reserved | F | reserved | | | | | | | |
| C4h | PN0 | F | PN0[7:0] | | | | | | | |
| C5h | PN1 | F | PN1[7:0] | | | | | | | |

Table 35. User-accessible data — sensor specific information...continued

| Address | Register | Type ^[1] | Bit | | | | | | | |
|---------------------|-------------|---------------------|------------------|-------------------|---|---|---|--------------|---|---|
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| C6h | SN0 | F | SN[7:0] | | | | | | | |
| C7h | SN1 | F | SN[15:8] | | | | | | | |
| C8h | SN2 | F | SN[23:16] | | | | | | | |
| C9h | SN3 | F | SN[31:24] | | | | | | | |
| CAh | SN4 | F | SN[39:32] | | | | | | | |
| CBh | ASICWFR# | F | ASICWFR#[7:0] | | | | | | | |
| CCh | ASICWFR_X | F | ASICWFR_X[7:0] | | | | | | | |
| CDh | ASICWFR_Y | F | ASICWFR_Y[7:0] | | | | | | | |
| CEh | reserved | F | reserved | | | | | | | |
| CFh | CRC_F_C | F | LOCK_F_C | REGC_BLOCKID[2:0] | | | | CRC_F_C[3:0] | | |
| D0h | ASICWLOT_L | F | ASICWLOT_L[7:0] | | | | | | | |
| D1h | ASICWLOT_H | F | ASICWLOT_H[7:0] | | | | | | | |
| D2h to DEh | reserved | F | reserved | | | | | | | |
| DFh | CRC_F_D | F | LOCK_F_D | REGD_BLOCKID[2:0] | | | | CRC_F_D[3:0] | | |
| E0h | USERDATA_0 | UF0 | USERDATA_0[7:0] | | | | | | | |
| E1h | USERDATA_1 | UF0 | USERDATA_1[7:0] | | | | | | | |
| E2h | USERDATA_2 | UF0 | USERDATA_2[7:0] | | | | | | | |
| E3h | USERDATA_3 | UF0 | USERDATA_3[7:0] | | | | | | | |
| E4h | USERDATA_4 | UF0 | USERDATA_4[7:0] | | | | | | | |
| E5h | USERDATA_5 | UF0 | USERDATA_5[7:0] | | | | | | | |
| E6h | USERDATA_6 | UF0 | USERDATA_6[7:0] | | | | | | | |
| E7h | USERDATA_7 | UF0 | USERDATA_7[7:0] | | | | | | | |
| E8h | USERDATA_8 | UF0 | USERDATA_8[7:0] | | | | | | | |
| E9h | USERDATA_9 | UF0 | USERDATA_9[7:0] | | | | | | | |
| EAh | USERDATA_A | UF0 | USERDATA_A[7:0] | | | | | | | |
| EBh | USERDATA_B | UF0 | USERDATA_B[7:0] | | | | | | | |
| ECh | USERDATA_C | UF0 | USERDATA_C[7:0] | | | | | | | |
| EDh | USERDATA_D | UF0 | USERDATA_D[7:0] | | | | | | | |
| EEh | USERDATA_E | UF0 | USERDATA_E[7:0] | | | | | | | |
| EFh | CRC_UF0 | F | LOCK_UF0 | REGE_BLOCKID[2:0] | | | | CRC_UF0[3:0] | | |
| F0h | USERDATA_10 | UF1 | USERDATA_10[7:0] | | | | | | | |
| F1h | USERDATA_11 | UF1 | USERDATA_11[7:0] | | | | | | | |
| F2h | USERDATA_12 | UF1 | USERDATA_12[7:0] | | | | | | | |
| F3h | USERDATA_13 | UF1 | USERDATA_13[7:0] | | | | | | | |
| F4h | USERDATA_14 | UF1 | USERDATA_14[7:0] | | | | | | | |
| F5h | USERDATA_15 | UF1 | USERDATA_15[7:0] | | | | | | | |
| F6h | USERDATA_16 | UF1 | USERDATA_16[7:0] | | | | | | | |
| F7h | USERDATA_17 | UF1 | USERDATA_17[7:0] | | | | | | | |
| F8h | USERDATA_18 | UF1 | USERDATA_18[7:0] | | | | | | | |
| F9h | USERDATA_19 | UF1 | USERDATA_19[7:0] | | | | | | | |
| FAh | USERDATA_1A | UF1 | USERDATA_1A[7:0] | | | | | | | |
| FBh | USERDATA_1B | UF1 | USERDATA_1B[7:0] | | | | | | | |
| FCh | USERDATA_1C | UF1 | USERDATA_1C[7:0] | | | | | | | |

Table 35. User-accessible data — sensor specific information...continued

| Address | Register | Type ^[1] | Bit | | | | | | | |
|---------|-------------|---------------------|------------------|-------------------|---|---|--------------|---|---|---|
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FDh | USERDATA_1D | UF1 | USERDATA_1D[7:0] | | | | | | | |
| FEh | USERDATA_1E | UF1 | USERDATA_1E[7:0] | | | | | | | |
| FFh | CRC_UF1 | F | LOCK_UF1 | REGF_BLOCKID[2:0] | | | CRC_UF1[3:0] | | | |

[1] Memory type codes

R — Readable register with no OTP

F — User readable register with OTP

UF2 — One time user programmable OTP location region 2

[2] Useful for I²C read wrap around mode to support temperature data. See [Table 9](#) and [Table 67](#).

7.7 Register information

7.7.1 COUNT - rolling counter register (address 00h)

The count register is a read-only register that provides the current value of a free-running 8-bit counter derived from the primary oscillator. A 10-bit prescaler divides the primary oscillator frequency by 1000. Therefore, the value in the register increases by one count every 100 µs and the counter rolls over every 25.6 ms.

Table 36. COUNT - rolling counter register (address 00h) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|------------|---|---|---|---|---|---|---|
| Symbol | COUNT[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R | R | R | R | R | R | R | R |

7.7.2 Device status registers

The device status registers are read-only registers that contain device status information. These registers are readable in SPI or I²C mode.

7.7.2.1 DEVSTAT - device status register (address 01h)

Table 37. DEVSTAT - device status register (address 01h) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|---------|----------|----------|-------------|------------|-----------|--------|---------|
| Symbol | DSP_ERR | reserved | COMM_ERR | MEMTEMP_ERR | SUPPLY_ERR | TEST MODE | DEVRES | DEVINIT |
| Reset | 1 | reserved | 0 | 0 | x | 0 | 1 | 1 |
| Access | R | R | R | R | R | R | R | R |

Table 38. DEVSTAT - device status register (address 01h) bit description

| Bit | Symbol | Description |
|-----|---------|---|
| 7 | DSP_ERR | The DSP error flag is set if a DSP-specific error is present in the pressure signal DSP: $DSP_ERR = DSP_STAT[ST_INCMPLT] \mid DSP_STAT[CM_ERROR] \mid DSP_STAT[ST_ERROR]$ |

Table 38. DEVSTAT - device status register (address 01h) bit description...continued

| Bit | Symbol | Description |
|------------------|-------------|--|
| 5 | COMM_ERR | The communication error flag is set if any bit in DEVSTAT3 is set: $COMM_ERR = MISO_ERR$ |
| 4 | MEMTEMP_ERR | The memory error flag is set if any bit in DEVSTAT2 is set: $MEMTEMP_ERR = F_OTP_ERR \mid U_OTP_ERR \mid U_RW_ERR \mid U_W_ACTIVE \mid TEMPO_ERR$ |
| 3 ^[1] | SUPPLY_ERR | The supply error flag is set if any bit in DEVSTAT1 is set: $SUPPLY_ERR = VCCUV_ERR \mid INTREG_ERR \mid INTREGA_ERR \mid INTREGF_ERR \mid CONT_ERR$ |
| 2 | TESTMODE | The test mode bit is set if the device is in test mode. The TESTMODE bit can be cleared by a test mode operation or by a power cycle. 0 — Test mode is not active 1 — Test mode is active |
| 1 | DEVRES | The device reset bit is set following a device reset. This error is cleared by a read of the DEVSTAT register through any communication interface or on a data transmission that includes the error in the status field. ^[2] 0 — Normal operation 1 — Device reset occurred |
| 0 | DEVINIT | The device initialization bit is set following a device reset. The bit is cleared once sensor data is valid for read through one of the device communication interfaces ($t_{POR_DataValid}$). 0 — Normal operation 1 — Device initialization in process |

[1] See Section 7.7.4 bit 3, supply error reporting disable bit (SUP_ERR_DIS).

[2] After POR and/or soft reset, see Section 7.5.5 for initialization sequence.

7.7.2.2 DEVSTAT1 - device status register (address 02h)

Table 39. DEVSTAT1 - device status register (address 02h) bit allocation

| Bit ^{[1][2]} | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------------|-----------|----------|----------|----------|-------------|------------|-------------|----------|
| Symbol | VCCUV_ERR | reserved | reserved | reserved | INTREGA_ERR | INTREG_ERR | INTREGF_ERR | CONT_ERR |
| Reset | x | x | x | x | x | x | x | 0 |
| Access | R | R | R | R | R | R | R | R |

[1] During POR and soft reset ignore DEVSTAT1 error flags, refer to Section 7.5.5.

[2] A common timer is used for all error bits in the DEVSTAT1 register. If any supply error is present, the timer is reset to t_{UVOV_RCV} . This bit is cleared based on the state of the SUP_ERR_DIS bit in the DEVLOCK_WR register as shown in Section 7.7.4.

Table 40. DEVSTAT1 - device status register (address 02h) bit description

| Bit ^{[1][2]} | Symbol | Description |
|-----------------------|-----------|---|
| 7 | VCCUV_ERR | The V_{CC} undervoltage error bit is set if the V_{CC} voltage falls below the voltage specified in Table 104. See Section 7.1 for details on the V_{CC} undervoltage monitor. 0 — No error detected 1 — V_{CC} voltage low |

Table 40. DEVSTAT1 - device status register (address 02h) bit description...continued

| Bit ^{[1][2]} | Symbol | Description |
|-----------------------|-------------|---|
| 3 | INTREGA_ERR | The internal analog regulator voltage out-of-range error bit is set if the internal analog regulator voltage falls outside expected limits. 0 — No error detected 1 — Internal analog regulator voltage out of range |
| 2 | INTREG_ERR | The internal digital regulator voltage out-of-range error bit is set if the internal digital regulator voltage falls outside expected limits. 0 — No error detected 1 — Internal digital regulator voltage out of range |
| 1 | INTREGF_ERR | The internal OTP regulator voltage out-of-range error bit is set if the internal OTP regulator voltage falls outside expected limits. 0 — No error detected 1 — Internal OTP regulator voltage out of range |
| 0 | CONT_ERR | The continuity monitor passes a low current through a connection around the perimeter of the device and monitors the continuity of the connection. The error bit is set if a discontinuity is detected in the connection. 0 — No error detected 1 — Error detected in the continuity of the edge seal monitor circuit |

[1] During POR and soft reset ignore DEVSTAT1 error flags, refer to [Section 7.5.5](#).

[2] A common timer is used for all error bits in the DEVSTAT1 register. If any supply error is present, the timer is reset to t_{UVOV_RCV} . This bit is cleared based on the state of the SUP_ERR_DIS bit in the DEVLOCK_WR register as shown in [Section 7.7.4](#).

7.7.2.3 DEVSTAT2 - device status register (address 03h)

Table 41. DEVSTAT2 - device status register (address 03h) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-----------|-----------|----------|------------|----------|-----------|----------|----------|
| Symbol | F_OTP_ERR | U_OTP_ERR | U_RW_ERR | U_W_ACTIVE | reserved | TEMP0_ERR | reserved | reserved |
| Reset | 0 | 0 | 0 | 0 | reserved | 0 | reserved | reserved |
| Access | R | R | R | R | R | R | R | R |

Table 42. DEVSTAT2 - device status register (address 03h) bit description

| Bit | Symbol | Description |
|-----|-----------|---|
| 7 | F_OTP_ERR | The NXP factory OTP array error bit is set if a fault is detected in the factory OTP array. This error is cleared by a read of the DEVSTAT2 register through any communication interface or on a data transmission that includes the error in the status field. 0 — No error detected 1 — Error detected in the NXP factory OTP array |
| 6 | U_OTP_ERR | The user OTP array error bit is set if a fault is detected in the user OTP array. This error is cleared by a read of the DEVSTAT2 register through any communication interface or on a data transmission that includes the error in the status field. 0 — No error detected 1 — Error detected in the user OTP array |

Table 42. DEVSTAT2 - device status register (address 03h) bit description...continued

| Bit | Symbol | Description |
|-----|------------|--|
| 5 | U_RW_ERR | When ENDINIT is set, an error detection is enabled for all user writable registers. The error detection code is continuously calculated on the user writable registers and verified against a previously calculated error detection code. If a mismatch is detected in the error detection, the U_RW_ERR bit is set. This error is cleared by a read of the DEVSTAT2 register through any communication interface or on a data transmission that includes the error in the status field. 0 — No error detected 1 — Error detected in the user read/write array |
| 4 | U_W_ACTIVE | The user OTP write in process status bit is set if a user initiated write to OTP is in process. The U_W_ACTIVE bit is automatically cleared once the write to OTP is complete. 0 — No OTP write in process 1 — OTP write in process |
| 2 | TEMP0_ERR | The temperature error bit is set if an overtemperature or undertemperature condition exists. This error is cleared by a read of the DEVSTAT2 register through any communication interface or on a data transmission that includes the error in the status field. 0 — No error detected 1 — Overtemperature or undertemperature error condition detected |

7.7.2.4 DEVSTAT3 - device status register (address 04h)

Table 43. DEVSTAT3 - device status register (address 04h) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|----------|----------|----------|----------|----------|----------|----------|----------|
| Symbol | MISO_ERR | reserved | reserved | reserved | reserved | reserved | reserved | reserved |
| Reset | 0 | reserved | reserved | reserved | reserved | reserved | reserved | reserved |
| Access | R | R | R | R | R | R | R | R |

Table 44. DEVSTAT3 - device status register (address 04h) bit description

| Bit | Symbol | Description |
|-----|----------|--|
| 7 | MISO_ERR | In SPI mode, the MISO data mismatch flag is set when a MISO Data mismatch fault occurs. The MISO_ERROR bit is cleared by a read of the DEVSTAT3 register through any communication interface, or by a status transmission including the error status through the SPI. 0 — No error detected 1 — MISO data mismatch |

7.7.3 TEMPERATURE - temperature register (address 0Eh)

The temperature register is a read-only register that provides a temperature value for the IC. The temperature value is specified in the temperature sensor signal chain section of [Table 104](#).

Note: The device is only guaranteed to operate within the temperature limits specified in [Section 10 "Static characteristics"](#).

Table 45. TEMPERATURE - temperature register (address 0Eh) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|-----------|---|---|---|---|---|---|---|
| Symbol | TEMP[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R | R | R | R | R | R | R | R |

7.7.4 DEVLOCK_WR - lock register writes register (address 10h)

The lock register writes register is a read/write register that contains the ENDINIT bit and reset control bits.

Table 46. DEVLOCK_WR - lock register writes register (address 10h) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|----------|----------|----------|-------------|----------|------------|-----|
| Symbol | ENDINIT | reserved | reserved | reserved | SUP_ERR_DIS | reserved | RESET[1:0] | |
| Factory default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 47. DEVLOCK_WR - lock register writes register (address 10h) bit description

| Bit | Symbol | Description |
|--------|-------------|---|
| 7 | ENDINIT | <p>The ENDINIT bit is a control bit used to indicate that the user has completed all device and system level initialization tests. Once the ENDINIT bit is set, writes to all writable register bits are inhibited except for the DEVLOCK_WR register. Once set, the ENDINIT bit can only be cleared by a device reset.</p> <p>When ENDINIT is set, the following occurs:</p> <ul style="list-style-type: none"> • An error detection is enabled for all user writable registers. The error detection code is continuously calculated on the user writable registers and verified against a previously calculated error detection code. • Self-test is disabled and inhibited. • Register writes are inhibited except for the RESET[1:0] bits in the DEVLOCK_WR register. |
| 3 | SUP_ERR_DIS | <p>The supply error disable bit allows the user to disable reporting of the supply errors in the SPI status fields.</p> <p>In SPI Mode:</p> <ul style="list-style-type: none"> • 0: No Response until the supply monitor timer expires. The Sensor Data Field Error Code is transmitted for one response after the supply monitor timer expires. All supply errors are cleared by a read of the DEVSTAT1 register through any communication interface or on a data transmission that includes the error in the status field if and only if the timer has reached zero. • 1: No Responses occur if the timer is non-zero. The error is cleared when the timer reaches zero and normal transmissions resume. <p>In I²C Mode (0 or 1):</p> <ul style="list-style-type: none"> • No response until the supply monitor timer expires. • All supply errors are cleared by a read of the DEVSTAT1 register. |
| 1 to 0 | RESET[1:0] | To reset the device, three consecutive register write operations must be performed in the order shown in Table 48 , or the device will not reset. ^[1] |

[1] After POR and/or soft reset, see [Section 7.5.5](#) for initialization sequence.

Table 48. Device reset command sequence

| Register write to DEVLOCK_WR | RESET[0] | RESET[1] | Effect |
|------------------------------|----------|----------|--------------|
| Register write 1 | 0 | 0 | No effect |
| Register write 2 | 1 | 1 | No effect |
| Register write 3 | 0 | 1 | Device RESET |

The response to a register write returns the new register value, including the values written to the RESET[1:0] bits. After the third register write command, the device initiates a reset and therefore does not transmit a response to this command or an acknowledge in I²C mode. The response to a register read returns '00' for RESET[1:0] and terminates the reset sequence. The reset control bits are not included in the read/write array error detection.

7.7.5 WRITE_OTP_EN – write OTP enable register (address 11h)

The write OTP enable register is a user programmed read/write register that allows the user to write the contents of the user programmed OTP array mirror registers to the OTP registers. This register is included in the user read/write array error detection.

This register is readable and writable in SPI and I²C modes.

Table 49. WRITE_OTP_EN – write OTP enable register – (address 11h) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|--------------|----------|----------|----------|-------------|----------|------------------|-----|
| Name | UOTP_WR_INIT | Reserved | Reserved | Reserved | EX_COMMTYPE | EX_PADDR | UOTP_REGION[1:0] | |
| Access | R/W | R/W | R/W | v | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Register writes executed by the user to the user programmed OTP array only update the mirror register contents for the OTP array, not the actual OTP registers. To copy the values to the actual OTP registers, a write must be executed to the WRITE_OTP_EN register with the UOTP_WR_INIT bit set. The state of the UOTP_REGION[1:0], the EX_COMMTYPE, and the EX_PADDR bits in the command determine which region of OTP is written to as shown in [Table 50](#).

Table 50. Writes for OTP registers

| EX_COMMTYPE | EX_PADDR | UOTP_REGION[1] | UOTP_REGION[0] | OTP write operation | Special conditions |
|-------------|----------|----------------|----------------|---|--|
| x | x | 0 | 0 | Write the current contents of the UF0 registers to OTP | — |
| x | x | 0 | 1 | Write the current contents of the UF1 registers to OTP | — |
| 0 | 0 | 1 | 0 | Reserved for future use. | — |
| 0 | 1 | 1 | 0 | Reserved for future use. | — |
| 1 | 0 | 1 | 0 | Reserved for future use. | — |
| 1 | 1 | 1 | 0 | Write the current contents of the UF2 registers to OTP. | Excluding LPF. LPF defaults to 1000 Hz at POR. |
| x | x | 1 | 1 | Reserved for future use | — |

The UF0 and UF1 user OTP regions as well as the NXP programmed F OTP regions share common mirror registers. For this reason, writes to the OTP for each region must be completed independently according to the procedure below.

Once a region is written using the OTP Write sequence, the LOCK_Uxxx bit in the appropriate CRC_xxx register is automatically set, locking the array from future writes. Once a region is locked, an error detection is activated to detect changes to the register values. Register values in the UF2 region can be overwritten using register write commands, but no new values can be written to the OTP.

The procedure for writing to the user OTP array UF0 and UF1 regions is listed below:

1. Read the appropriate CRC_UF_x register and confirm the LOCK_U_{xx} bit is not set.
2. Write the desired values to the user array registers for only the region to be written using the procedures in [Section 7.7.6 "UF_REGION_W, UF_REGION_R - UF region selection registers \(address 14h, 15h\)"](#).
The user must take care to ensure that the proper data is written to each region. If a register write is executed to a new region, the base address changes to the new region. The previous data written to the register block remains in the shared registers and is written to OTP if the Write OTP sequence is completed.
3. Execute a write to the WRITE_OTP_EN register with the appropriate bits set for the desired region to program.
Once the WRITE_OTP_EN register write is completed, a CRC is calculated for the data to be written to the region, the register values are written to OTP and the region is locked from future writes. The UOTP_WR_INIT bit remains set.
4. Delay 10 ms to allow the device to complete the writes to OTP.
5. Verify that the OTP write has successfully completed by reading back all of the OTP registers using register read commands as defined in [Section 7.7.6 "UF_REGION_W, UF_REGION_R - UF region selection registers \(address 14h, 15h\)"](#).
6. Repeat steps 1 through 4 for all regions to be programmed.

The procedure for writing to the user OTP array UF2 region is listed below:

1. Read the CRC_UF2 register and confirm the LOCK_UF2 bit is not set.
2. Write the desired values to the user array registers.
3. Execute a write to the WRITE_OTP_EN register with region 2 selected and the EX_COMMTYPE and EX_PADDR bits set as shown in [Table 50](#).
Once the WRITE_OTP_EN register write is completed, a CRC is calculated for the data to be written to the region, the register values are written to OTP and the region is locked from future writes. The UOTP_WR_INIT bit remains set.
4. Delay 10 ms to allow the device to complete the writes to OTP.
5. Verify that the OTP write successfully completed by reading back all of the OTP registers using register read commands.

7.7.6 UF_REGION_W, UF_REGION_R - UF region selection registers (address 14h, 15h)

The UF region load register is a user read/write register that contains the control bits for the UF0 and UF1 regions to be accessed. This register is included in the user read/write array error detection. The UF region active register is a read-only register that contains the status bits for the UF0 and UF1 regions to be accessed. This register is included in the user read/write array error detection.

The UF_REGION_W register is readable and writable in SPI mode or I²C mode. The UF_REGION_R register is readable in SPI mode or I²C mode.

Table 51. UF_REGION_W - UF region selection register (address 14h) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|------------------|-----|-----|-----|-----|-----|-----|-----|
| Symbol | REGION_LOAD[3:0] | | | | 0 | 0 | 0 | 0 |
| Factory default | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 52. UF_REGION_R - UF region selection register (address 15h) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------------|---|---|---|---|---|---|---|
| Symbol | REGION_ACTIVE[3:0] | | | | 0 | 0 | 0 | 0 |
| Factory default | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| Access | R | R | R | R | R | R | R | R |

The user OTP regions UF0, UF1, and F share a block of 16 registers. Prior to reading the registers via any communication interface, the user must ensure that the desired OTP registers are loaded into the readable registers. Below is the necessary procedure to ensure proper reading of the UF0, UF1, and F registers.

1. Write the desired address range to be read to the REGION_LOAD[3:0] bits in the UF_REGION_W register.

Table 53. REGION_LOAD Bit Definitions

| REGION_LOAD[3:0] | | | | OTP register addresses loaded into the readable registers |
|-------------------|---|---|---|---|
| 0 | 0 | 0 | 0 | not applicable |
| 0 | 0 | 0 | 1 | not applicable |
| 0010 through 1001 | | | | reserved |
| 1 | 0 | 1 | 0 | Address Range A0h through AFh |
| 1 | 0 | 1 | 1 | Address Range B0h through BFh |
| 1 | 1 | 0 | 0 | Address Range C0h through CFh |
| 1 | 1 | 0 | 1 | Address Range D0h through DFh |
| 1 | 1 | 1 | 0 | Address Range E0h through EFh |
| 1 | 1 | 1 | 1 | Address Range F0h through FFh |

2. Add a delay of minimum 50 μs.
3. Optional: Execute a register read of the UF_REGION_R register and confirm the REGION_ACTIVE[3:0] bits match the values written to the REGION_LOAD[3:0] bits in the UF_REGION_W register.

Table 54. REGION_ACTIVE Bit Definitions

| REGION_ACTIVE[3:0] | | | | OTP register addresses loaded into the readable registers |
|--------------------|---|---|---|--|
| 0 | 0 | 0 | 0 | Load of OTP registers is in process |
| 0 | 0 | 0 | 1 | The contents of the shared registers has been over-written by the user |
| 0010 through 1001 | | | | not applicable |
| 1 | 0 | 1 | 0 | Address Range A0h through AFh |
| 1 | 0 | 1 | 1 | Address Range B0h through BFh |
| 1 | 1 | 0 | 0 | Address Range C0h through CFh |
| 1 | 1 | 0 | 1 | Address Range D0h through DFh |
| 1 | 1 | 1 | 0 | Address Range E0h through EFh |
| 1 | 1 | 1 | 1 | Address Range F0h through FFh |

4. Execute a Register Read of the desired registers from the UF0, UF1 or F register section. Complete all desired Register Reads of the selected UF Region.
5. Repeat steps 1 through 4 for the next desired UF region to read.

Notes:

- The user must take care to ensure that the desired registers are addressed. For example, if the REGION_LOAD bits are set to Ah and the user executes a read of address C2h, the contents of registers A2h is transmitted. No error detection is included other than a read of the REGION_ACTIVE bits.
- In SPI and I²C modes, once the ENDINIT bit is set, writes to registers other than the RESET[1:0] bits are inhibited. For this reason, reads of the UF0, UF1, and F registers are only possible for the region selected by the REGION_ACTIVE bits at the time ENDINIT is set.

7.7.7 SOURCEID_x - source identification registers (address 1Ah, 1Bh)

The source identification registers are user programmed read/write registers that contain the source identification information used in SPI Mode. These registers are included in the read/write array error detection.

Table 55. SOURCEID_0 - source identification register (address 1Ah) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|----------|----------|----------|-----------------|-----|-----|-----|
| Symbol | SID0_EN | reserved | reserved | reserved | SOURCEID_0[3:0] | | | |
| Factory default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 56. SOURCEID_1 - source identification register (address 1Bh) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---------|----------|----------|----------|-----------------|-----|-----|-----|
| Symbol | SID1_EN | reserved | reserved | reserved | SOURCEID_1[3:0] | | | |
| Factory default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

7.7.7.1 Data source enable bits (SIDx_EN)

The SIDx_EN are control bits for both I²C and SPI modes. In I²C mode, they configure the automatic register read wrap-around feature to optimize the number of I²C transactions. See [Section 7.4.6.3](#) and [Table 9](#) for details.

In SPI mode, the SIDx_EN bits enable and map the data source (SNSDATA0, SNSDATA1) to the associated source identification as described in [Table 11](#). Additionally, the SPI error response monitoring can be mapped to the SOURCEID_x channels. SPI error responses are detailed in [Section 7.5.4 "Error checking"](#).

Table 57. Source ID enable

| Source ID | Source ID Enable (SIDx_EN) | Transmitted data |
|------------|----------------------------|--------------------|
| SOURCEID_0 | 0 | SPI error response |
| | 1 | SNSDATA0 |
| SOURCEID_1 | 0 | SPI error response |
| | 1 | SNSDATA1 |

In I²C mode, the SOURCEID_x registers are readable and writable but have no effect on the device. See [Table 11](#), for details regarding the effect of the SIDx_EN bits.

7.7.8 SPI Configuration Control Register (SPI_CFG, Address 3Dh)

In SPI mode, the SPI configuration control register is a user programmed read/write register that contains the SPI protocol configuration information. This register is included in the read/write array error detection. This register is readable and writable in SPI mode or I²C mode

Table 58. SPI_CFG Register (address 3Dh) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|----------|------------------|-----|-----------------|-----|-----|-----|
| Symbol | reserved | DATASIZE | SPI_CRC_LEN[1:0] | | SPICRCSEED[3:0] | | | |
| Factory default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

7.7.8.1 SPI Data Field Size (DATASIZE)

The SPI data field size bit controls the size of the SPI data field as shown in [Table 59](#).

Table 59. DATASIZE Bit Definition

| DATASIZE | SPI Data Field Size |
|----------|---------------------|
| 0 | 12-Bits |
| 1 | 16-Bits |

7.7.8.2 SPI CRC Length and Seed Bits

The SPI_CRC_LEN[1:0] bits select the CRC length for SPI Mode as shown in the table below. The SPI CRC seed bits contain the seed used for the SPI Mode. The default SPI CRC is an 8-bit. When the SPI_CRC_LEN[1:0] bits are set to a non-zero value using a Register Write command, the SPI CRC changes as defined in the table. The new polynomial value is enabled for both MISO and MOSI on the next SPI Mode command. The default seed (SPICRCSEED[3:0] = 0h) is FFh for an 8-bit CRC. When the value is changed to a non-zero value using a Register Write command, the SPI CRC seed changes to the value programmed as shown in the table. The new seed value is enabled for both MISO and MOSI on the next SPI Mode command.

Table 60. SPI CRC Definition

| SPI_CRC_LEN[1:0] | | SPICRCSEED | CRC Polynomial | CRC Seed |
|------------------|---|------------|---------------------------------|-----------------------|
| 0 | 0 | 0 | $x^8 + x^5 + x^3 + x^2 + x + 1$ | 1111, 1111 |
| 0 | 0 | non-zero | $x^8 + x^5 + x^3 + x^2 + x + 1$ | 0000, SPICRCSEED[3:0] |
| 0 | 1 | 0 | $x^4 + 1$ | 1010 |
| 0 | 1 | non-zero | $x^4 + 1$ | SPICRCSEED[3:0] |
| 1 | 0 | 0 | $x^3 + x + 1$ | 111 |
| 1 | 0 | non-zero | $x^3 + x + 1$ | SPICRCSEED[2:0] |
| 1 | 1 | 0 | $x^3 + x + 1$ | 111 |
| 1 | 1 | non-zero | $x^3 + x + 1$ | SPICRCSEED[2:0] |

7.7.9 WHO_AM_I - who am I register (address 3Eh)

The WHO_AM_I register is a user programmed read/write register that contains the unique product identifier. This register is included in the read/write array error detection.

Table 61. WHO_AM_I - device identification register (address 3Eh) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------------------------------|---------------|-----|-----|-----|-----|-----|-----|-----|
| Symbol | WHO_AM_I[7:0] | | | | | | | |
| Factory default (stored value) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Factory default (read value) | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

The default register value is 00h. If the register value is 00h, a value of C4h is transmitted in response to a read command. For all other register values, the actual register value is transmitted in response to a read command.

Table 62. WHO_AM_I register values

| WHO_AM_I register value (hex) | Response to a register read command |
|-------------------------------|-------------------------------------|
| 00h | C4h |
| 01h to FFh | Actual register value |

7.7.10 I2C_ADDRESS - I²C client address register (address 3Fh)

The I²C client address register is a user programmed read/write register that contains the unique I²C client address. The register is readable in all modes. This register is included in the read/write array error detection.

Table 63. I2C_ADDRESS - I²C client address register (address 3Fh) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------------------------------|------------------|-----|-----|-----|-----|-----|-----|-----|
| Symbol | I2C_ADDRESS[7:0] | | | | | | | |
| Factory Default (stored value) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Factory Default (read value) | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

The default register value is 00h. If the register value is 00h, the I²C client address is 60h and a value of 60h is transmitted in response to a read command. If the register is written to a value other than 00h, the I²C client address is the lower seven bits of the actual register value and the actual register value is transmitted in response to a read command.

7.7.11 DSP Configuration Registers (DSP_CFG_Ux)

The DSP Configuration registers (DSP_CFG_Ux) are a series of registers that affect the DSP data path.

There are 4 DSP Configuration registers which are DSP_CFG_U1, DSP_CFG_U3, DSP_CFG_U4, and DSP_CFG_U5.

7.7.11.1 DSP_CFG_U1 - DSP user configuration #1 register (address 40h)

The DSP user configuration register #1 is a user programmable read/write register that contains DSP-specific configuration information. This register is included in the read/write array error detection.

Changes to this register reset the DSP data path. The contents of the SNSDATA_x registers are not guaranteed until the DSP has completed initialization as specified in [Table 105](#). Reads of the SNSDATA_x registers and sensor data requests should be prevented during this time.

Table 64. DSP_CFG_U1 - DSP user configuration #1 register (address 40h) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|-----|-----|-----|----------|----------|----------|----------|
| Symbol | LPF[3:0] | | | | reserved | reserved | reserved | reserved |
| Factory default | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 65. Low-pass filter selection bits (LPF[3:0])

| LPF[3] | LPF[2] | LPF[1] | LPF[0] | Low Pass Filter Type |
|--------|--------|--------|--------|-----------------------------------|
| 0 | 0 | 1 | 0 | 800 Hz, 4-Pole |
| 0 | 0 | 1 | 1 | 1000 Hz, 4-Pole ^{[1][2]} |

[1] Default is 1000 Hz.

[2] In case of POR, filter reverts to the default.

Note: Using values other than those listed in [Table 65](#) causes an error in the DEVSTAT.

7.7.11.2 DSP_CFG_U3 - DSP user configuration #3 register (address 42h)

The DSP user configuration register #3 is a user programmable read/write register that contains DSP-specific configuration information. This register is included in the read/write array error detection.

Changes to this register reset the DSP data path. The content of the SNSDATA_x registers are not guaranteed until the DSP has completed initialization. Reads of the SNSDATA_x registers and sensor data requests should be prevented during this time.

This register is readable and writeable in SPI mode, and I²C mode.

Table 66. DSP_CFG_U3 - DSP user configuration #3 register (address 42h) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------|----------------|-----|----------|----------------|-----|----------|----------|
| Symbol | reserved | DATATYPE0[1:0] | | reserved | DATATYPE1[1:0] | | reserved | reserved |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

7.7.11.2.1 DSP data type 0 selection bits (DATATYPE0)

The DSP data type 0 selection bits select the type of data to be included in the SNSDATA0_L and SNSDATA0_H registers.

Table 67. DATATYPE0[1:0]

| DATATYPE0[1] | DATATYPE0[0] | SNSDATA register contents |
|--------------|--------------|---------------------------------------|
| 0 | 1 | Absolute pressure (P _{ABS}) |
| 1 | 1 | Temperature |

7.7.11.2.2 DSP data type 1 selection bits (DATATYPE1)

The DSP data type 1 selection bits select the type of data to be included in the SNSDATA1_L and SNSDATA1_H registers.

Table 68. DATATYPE1[1:0]

| DATATYPE1[1] | DATATYPE1[0] | SNSDATA register contents |
|--------------|--------------|---------------------------------------|
| 0 | 1 | Absolute pressure (P _{ABS}) |

Table 68. DATATYPE1[1:0]...continued

| DATATYPE1[1] | DATATYPE1[0] | SNSDATA register contents |
|--------------|--------------|---------------------------|
| 1 | 1 | Temperature |

7.7.11.3 DSP_CFG_U4 - DSP user configuration #4 register (address 43h)

The DSP user configuration register #4 is a user programmable read/write register that contains DSP-specific configuration information. This register is included in the read/write array error detection.

Table 69. DSP_CFG_U4 - DSP user configuration #4 register (address 43h) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|----------|----------|----------|----------|----------|---------|----------|----------|
| Symbol | reserved | reserved | reserved | reserved | reserved | INT_OUT | reserved | reserved |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 70. DSP_CFG_U4 - DSP user configuration #4 register (address 43h) bit description

| Bit | Symbol | Description |
|-----|---------|--|
| 2 | INT_OUT | The interrupt pin configuration bit selects the mode of operation for the interrupt pin. 0 — Open drain, active high with pull-down current 1 — Open drain, active low with pullup current |

7.7.11.4 DSP_CFG_U5 - DSP user configuration #5 register (address 44h)

The DSP user configuration register #5 is a read/write register that contains DSP-specific configuration information. This register is included in the read/write array error detection.

Table 71. DSP_CFG_U5 - DSP user configuration #5 register (address 44h) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------------|--------------|-----|-----|-----|----------|-----|-----|-----|
| Symbol | ST_CTRL[3:0] | | | | reserved | | | |
| Factory default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 72. DSP_CFG_U5 - DSP user configuration #5 register (address 44h) bit description

| Bit | Symbol | Description |
|--------|--------------|--|
| 7 to 4 | ST_CTRL[3:0] | The self-test control bits select one of the various analog and digital self-test features of the device as shown in Table 73 . The self-test control bits are not included in the read/write array error detection. |
| 3 to 0 | reserved | These bits are reserved. |

Table 73. Self-Test Control Bits (ST_CTRL[3:0])

| ST_CTRL[3] | ST_CTRL[2] | ST_CTRL[1] | ST_CTRL[0] | Function | SNS_DATAx_X Contents (16-bit data) |
|------------|------------|------------|------------|---|------------------------------------|
| 0 | 0 | 0 | 0 | Normal Pressure Signal | 16-bit Absolute Pressure Data |
| 0 | 0 | 0 | 1 | P-Cell Common Mode Verification | 16-bit Absolute Pressure Data |
| 0 | 0 | 1 | 0 | reserved | reserved |
| 0 | 0 | 1 | 1 | reserved | reserved |
| 0 | 1 | 0 | 0 | DSP write to SNS_DATAx_X registers inhibited. | 0000h |
| 0 | 1 | 0 | 1 | DSP write to SNS_DATAx_X registers inhibited. | AAAAh |
| 0 | 1 | 1 | 0 | DSP write to SNS_DATAx_X registers inhibited. | 5555h |
| 0 | 1 | 1 | 1 | DSP write to SNS_DATAx_X registers inhibited. | FFFFh |
| 1 | 0 | 0 | 0 | reserved | reserved |
| 1 | 0 | 0 | 1 | reserved | reserved |
| 1 | 0 | 1 | 0 | reserved | reserved |
| 1 | 0 | 1 | 1 | reserved | reserved |
| 1 | 1 | 0 | 0 | Digital Self-Test 0 | Digital Self-Test Output |
| 1 | 1 | 0 | 1 | Digital Self-Test 1 | Digital Self-Test Output |
| 1 | 1 | 1 | 0 | Digital Self-Test 2 | Digital Self-Test Output |
| 1 | 1 | 1 | 1 | Digital Self-Test 3 | Digital Self-Test Output |

7.7.12 INT_CFG - interrupt configuration register (address 45h)

The interrupt configuration register contains configuration information for the interrupt output. This register can be written during initialization but is locked once the ENDINIT bit is set (see [Section 7.7.4 "DEVLOCK_WR - lock register writes register \(address 10h\)"](#)). The register is included in the read/write array error detection.

Table 74. INT_CFG - interrupt configuration register (address 45h) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------|-----|-------------|-----|--------------|----------|-----|-----|
| Symbol | reserved | | INT_PS[1:0] | | INT_POLARITY | reserved | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 75. INT_CFG - interrupt configuration register (address 45h) bit description

| Bit | Symbol | Description |
|--------|--------------|--|
| 5 to 4 | INT_PS[1:0] | <p>The INT_PS[1:0] bits set the programmable pulse stretch time for the interrupt output. Pulse stretch times are derived from the internal oscillator, so the tolerance on this oscillator applies.</p> <p>00 — 0 ms 01 — 16.000 ms to 16.512 ms 10 — 64.000 ms to 64.512 ms 11 — 256.000 ms to 256.512 ms</p> <p>If the pulse stretch function is programmed to '00', the interrupt pin is asserted if and only if the interrupt condition exists after the most recent evaluated sample. The interrupt pin is deasserted if and only if an interrupt condition does not exist after the most recent evaluated sample.</p> <p>If the pulse stretch function is programmed to a non-zero value, the interrupt pin is controlled only by the value of the pulse stretch timer value. If the pulse stretch timer value is non-zero, the interrupt pin is asserted. If the pulse stretch timer is zero, the interrupt pin is deasserted. The pulse stretch counter continuously decrements until it reaches zero. The pulse stretch counter is reset to the programmed pulse stretch value if and only if an interrupt condition exists after the most recent evaluated sample.</p> |
| 3 | INT_POLARITY | <p>The interrupt polarity bit controls whether the interrupt is activated for values within or outside the window selected by the high and low threshold registers. With this bit and the programmable thresholds, a window comparator can be programmed for activation either within or outside a window.</p> <p>0 — Interrupt activated, if the value is outside the window 1 — Interrupt activated, if the value is inside the window</p> |

7.7.13 P_INT_HI, P_INT_LO - interrupt window comparator threshold registers (address 46h to 49h)

The interrupt threshold registers contain the high and low window comparator thresholds for pressure to be used to activate and deactivate the interrupt output. These registers can be written during initialization but are locked once the ENDINIT bit is set (see [Section 7.7.4 "DEVLOCK_WR - lock register writes register \(address 10h\)"](#)). The register is included in the read/write array error detection.

Table 76. P_INT_HI, P_INT_LO - interrupt window comparator threshold registers (address 46h to 49h) bit allocation

| Location | | Bit | | | | | | | | |
|---------------|--------------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|
| Address | Register | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 46h | PIN_INT_HI_L | PIN_INT_HI[7:0] | | | | | | | | |
| 47h | PIN_INT_HI_H | PIN_INT_HI[15:8] | | | | | | | | |
| 48h | PIN_INT_LO_L | PIN_INT_LO[7:0] | | | | | | | | |
| 49h | PIN_INT_LO_H | PIN_INT_LO[15:8] | | | | | | | | |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

The pressure threshold registers hold independent unsigned 16-bit values for a high and a low threshold. The window comparator threshold alignment is shown in [Section 7.3.3.4 "Absolute pressure output data scaling equation"](#).

If either the high or low threshold is programmed to 0000h, comparisons are disabled for that threshold only. The interrupt comparison still functions for the opposite threshold. If both the high and low thresholds are programmed to 0000h, the interrupt output is disabled.

7.7.14 P_CAL_ZERO - pressure calibration registers (address 4Ch, 4Dh)

The pressure calibration registers contain user programmable values to adjust the offset of the absolute pressure.

These registers can be written during initialization but are locked once the ENDINIT bit is set (see [Section 7.7.4 "DEVLOCK_WR - lock register writes register \(address 10h\)"](#)). These registers are included in the read/write array error detection. Changes to these registers reset the DSP data path. The contents of the SNSDATA_x registers are not guaranteed until the DSP has completed initialization, as specified in [Table 105](#). Reads of the SNSDATA_x registers and sensor data requests should be prevented during this time.

Table 77. P_CAL_ZERO - pressure calibration registers (address 4Ch, 4Dh) bit allocation

| Location | | Bit | | | | | | | |
|---------------|--------------|------------------|-----|-----|-----|-----|-----|-----|-----|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 4Ch | P_CAL_ZERO_L | P_CAL_ZERO[7:0] | | | | | | | |
| 4Dh | P_CAL_ZERO_H | P_CAL_ZERO[15:8] | | | | | | | |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

The P_CAL_ZERO register value is a signed 16-bit value that is directly added to the internally calibrated pressure signal value as shown in [Equation 6](#). The equation applies to the values in the 16-bit SNSDATA registers.

$$PABS_{LSB} = SNSDATA + User \text{ Offset} \tag{6}$$

Note: The pressure calibration registers enable range and resolution options beyond the specified values of the device. The user must take care to ensure that the value stored in this register does not result in a compressed output range or a railed output.

7.7.15 DSP_STAT - DSP specific status register (address 60h)

The DSP status register is a read-only register that contains sensor data-specific status information.

Table 78. DSP_STAT - DSP-specific status register (address 60h) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------------|----------|----------|----------|----------|------------|-----------|----------|----------|
| Symbol | reserved | reserved | reserved | reserved | ST_INCMPLT | ST_ACTIVE | CM_ERROR | ST_ERROR |
| Factory default | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| Access | R | R | R | R | R | R | R | R |

Table 79. DSP_STAT - DSP-specific status register (address 60h) bit description

| Bit | Symbol | Description |
|-----|------------|--|
| 3 | ST_INCMPLT | The self-test incomplete bit is set after a device reset and is only cleared when one of the analog or digital self-test modes is enabled in the ST_CTRL register (ST_CTRL[3] = '1' ST_CTRL[2] = '1' ST_CTRL[1] = '1' ST_CTRL[0] = '1'). 0 — An analog or digital self-test has been activated since the last reset. 1 — No analog or digital self-test has been activated since the last reset. |
| 2 | ST_ACTIVE | The self-test active bit is set if any self-test mode is active. The self-test active bit is cleared when no self-test mode is active. ST_ACTIVE= ST_CTRL[3] ST_CTRL[2] ST_CTRL[1] ST_CTRL[0] |
| 1 | CM_ERROR | The absolute pressure common mode error status bit is set if the common mode value of the analog front end exceeds predetermined limits. The CM_ERROR bit is cleared on a read of the DSP_STAT register through any communication interface or on a data transmission that includes the error in the status field. |
| 0 | ST_ERROR | The self-test error flag is set if an internal self-test fails as described in Section 7.3.1 . This bit can only be cleared by a device reset. |

7.7.16 DEVSTAT_COPY - device status copy register (address 61h)

The device status copy register is a read-only register that contains a copy of the device status information contained in the DEVSTAT register. See [Section 7.7.2.1 "DEVSTAT - device status register \(address 01h\)"](#) for details regarding the DEVSTAT register contents. A read of the DEVSTAT_COPY register has the same effect as a read of the DEVSTAT register.

Table 80. DEVSTAT_COPY - device status copy register (address 61h) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|---------|----------|----------|-------------|------------|----------|--------|---------|
| Symbol | DSP_ERR | reserved | COMM_ERR | MEMTEMP_ERR | SUPPLY_ERR | TESTMODE | DEVRES | DEVINIT |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R | R | R | R | R | R | R | R |

For bit descriptions, see [Table 38](#).

7.7.17 SNSDATA0_L, SNSDATA0_H - sensor data #0 registers (address 62h, 63h)

The sensor data #0 registers are read-only registers that contain the 16-bit sensor data. See [Section 7.3.3.4 "Absolute pressure output data scaling equation"](#) for details regarding the 16-bit sensor data.

The SNSDATA0_H register value is latched on a read of the SNSDATA0_L register value until the SNSDATA0_H register is read. To avoid data mismatch, the user is always required to read the registers in sequence, SNSDATA0_L register first, followed by the SNSDATA0_H register.

Table 81. SNSDATA0_L, SNSDATA0_H - sensor data #0 registers (addresses 62h, 63h) bit allocation

| Location | | Bit | | | | | | | |
|-----------------|------------|------------------|---|---|---|---|---|---|---|
| Address | Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 62h | SNSDATA0_L | SNSDATA0_L[7:0] | | | | | | | |
| 63h | SNSDATA0_H | SNSDATA0_H[15:8] | | | | | | | |
| Factory default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | | R | R | R | R | R | R | R | R |

7.7.18 SNSDATA1_L, SNSDATA1_H - sensor data #1 registers (address 64h, 65h)

The sensor data #1 registers are read-only registers that contain the 16-bit sensor data. See [Section 7.3.3.4 "Absolute pressure output data scaling equation"](#) for details regarding the 16-bit sensor data. The SNSDATA1 registers are beneficial for I²C read wrap around to reduce the number of I²C transactions. In this case, the temperature can be selected to be put into this register. See [Table 9](#) and [Table 67](#).

The SNSDATA1_H register value is latched on a read of the SNSDATA1_L register value until the SNSDATA1_H register is read. To avoid data mismatch, the user is always required to read the registers in sequence, SNSDATA1_L register first, followed by the SNSDATA1_H register.

Table 82. SNSDATA1_L, SNSDATA1_H - sensor data #1 registers (address 64h, 65h) bit allocation

| Location | | Bit | | | | | | | |
|-----------------|------------|------------------|---|---|---|---|---|---|---|
| Address | Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 64h | SNSDATA1_L | SNSDATA1_L[7:0] | | | | | | | |
| 65h | SNSDATA1_H | SNSDATA1_H[15:8] | | | | | | | |
| Factory default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | | R | R | R | R | R | R | R | R |

7.7.19 SNSDATA0_TIME_x - timestamp registers (address 66h to 6Bh)

The sensor data 0 timestamp registers are read-only registers that contain a 48-bit timestamp.

The value of the 48-bit free running timer register is copied to the sensor data 0 timestamp registers each time sensor data 0 data is latched for transmission. The timestamp is updated at the start of the sensor data 0 register value transmission for a register read of the SNSDATA0_L register.

The timestamp register is organized to allow for optimized reading of the timestamp in I²C automatic sensor data register read wrap-around mode as documented in [Table 9](#).

The sensor data 0 timestamp registers are read-only registers that contain a 48-bit timestamp.

The value of the 48-bit free running timer register is copied to the sensor data 0 timestamp registers each time sensor data 0 data is latched for transmission via SPI.

Table 83. SNSDATA0_TIME_x - timestamp register (address 66h to 6Bh) bit allocation

| Location | | Bit | | | | | | | |
|-----------------|----------------|----------------------|---|---|---|---|---|---|---|
| Address | Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 66h | SNSDATA0_TIME0 | SNSDATA0_TIME[7:0] | | | | | | | |
| 67h | SNSDATA0_TIME1 | SNSDATA0_TIME[15:8] | | | | | | | |
| 68h | SNSDATA0_TIME2 | SNSDATA0_TIME[23:16] | | | | | | | |
| 69h | SNSDATA0_TIME3 | SNSDATA0_TIME[31:24] | | | | | | | |
| 6Ah | SNSDATA0_TIME4 | SNSDATA0_TIME[39:32] | | | | | | | |
| 6Bh | SNSDATA0_TIME5 | SNSDATA0_TIME[47:40] | | | | | | | |
| Factory default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | | R | R | R | R | R | R | R | R |

7.7.20 P_MAX, P_MIN - maximum and minimum absolute pressure value registers (address 6Ch to 6Fh)

The minimum and maximum absolute pressure value registers are read-only registers that contain a sample-by-sample continuously updated minimum and maximum 16-bit absolute pressure value. The value is reset to 0000h on a write to a DSP_CFG_U1 register that changes the value of the LPF[2:0] or ST_CTRL[3:0].

The values of P_Max and P_Min obtained during a SPI or I²C register read might not always be the same value as the instantaneous pressure value obtained from the SNSDATA_x registers.

These registers are readable in SPI mode or I²C mode. In I²C mode, the P_xxx_H register value is latched on a read of the P_xxx_L register value until the P_xxx_H

register is read. To avoid data mismatch, the user is always required to read the registers in sequence, P_xxx_L register first, followed by the P_xxx_H register.

Table 84. P_Max and P_Min registers (address 6Ch to 6Fh) bit allocation

| Location | | Bit | | | | | | | |
|------------------------|---------|-------------|---|---|---|---|---|---|---|
| Address | Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 6Ch | P_MAX_L | P_MAX[7:0] | | | | | | | |
| 6Dh | P_MAX_H | P_MAX[15:8] | | | | | | | |
| 6Eh | P_MIN_L | P_MIN[7:0] | | | | | | | |
| 6Fh | P_MIN_H | P_MIN[15:8] | | | | | | | |
| Factory default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | | R | R | R | R | R | R | R | R |

7.7.21 FRT - free running timer registers (addresses 78h to 7Dh)

The free running timer registers are read-only registers that contain a 48-bit free running timer. The free running timer is clocked by the main oscillator frequency and increments every 100 ns.

Table 85. FRT - free running timer registers (addresses 78h to 7Dh) bit allocation

| Location | | Bit | | | | | | | |
|---------------|--------|------------|---|---|---|---|---|---|---|
| Address | Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 78h | FRT0 | FRT[7:0] | | | | | | | |
| 79h | FRT1 | FRT[15:8] | | | | | | | |
| 7Ah | FRT2 | FRT[23:16] | | | | | | | |
| 7Bh | FRT3 | FRT[31:24] | | | | | | | |
| 7Ch | FRT4 | FRT[39:32] | | | | | | | |
| 7Dh | FRT5 | FRT[47:40] | | | | | | | |
| Access | | R | R | R | R | R | R | R | R |

7.7.22 IC type register (Address C0h)

The IC type register is a factory programmable OTP register that contains the IC type as defined below. This register is included in the factory programmed OTP array error detection. This register is readable in SPI mode or I²C mode when ENDINIT is not set.

Table 86. IC TYPE REGISTER (ICTYPEID address C0h) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|---------------|---|---|---|---|---|---|---|
| Symbol | ICTYPEID[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R |

7.7.23 IC manufacturer revision register (Address C1h)

The IC manufacturer revision register is a factory programmable OTP register that contains the IC revision. The upper nibble contains the main IC revision. The lower nibble contains the sub IC revision. This register is included in the factory programmed OTP array error detection. This register is readable in SPI mode or I²C mode when ENDINIT is not set.

Table 87. IC MANUFACTURER REVISION REGISTER (ICREVID address C1h) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|--------------|-----|-----|-----|-----|-----|-----|-----|
| Symbol | ICREVID[7:0] | | | | | | | |
| Reset | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |
| Access | R | R | R | R | R | R | R | R |

7.7.24 IC manufacturer identification register (address C2h)

The IC manufacturer identification register is a factory programmable OTP register that identifies NXP as the IC manufacturer. This register is included in the factory programmed OTP array error detection. This register is readable in SPI mode or I²C mode when ENDINIT is not set.

Table 88. IC MANUFACTURER IDENTIFICATION REGISTER (ICMFGID address C2h) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|--------------|---|---|---|---|---|---|---|
| Symbol | ICMFGID[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R |

7.7.25 Part number register (address C4h, C5h)

The part number registers are factory programmed OTP registers that include the numeric portion of the device part number. These registers are included in the factory programmed OTP array error detection. These registers are readable in SPI mode or I²C mode when ENDINIT is not set.

Table 89. PN0 Register (address C4h) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------|-----|-----|-----|-----|-----|-----|-----|
| Symbol | PN0[7:0] | | | | | | | |
| Reset | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |
| Access | R | R | R | R | R | R | R | R |

Table 90. PN1 Register (address C5h) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------|-----|-----|-----|-----|-----|-----|-----|
| Symbol | PN1[7:0] | | | | | | | |
| Reset | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |
| Access | R | R | R | R | R | R | R | R |

7.7.26 Device serial number registers

The serial number registers are factory programmed OTP registers that include the unique serial number of the device. Serial numbers begin at 1 for all produced devices in each lot and are sequentially assigned. Lot numbers begin at 1 and are sequentially assigned. No lot contains more devices than can be uniquely identified by the 14-bit serial number. Depending on lot size and quantities, all possible lot numbers and serial numbers might not be assigned. These registers are included in the factory programmed OTP array error detection. These registers are readable in SPI mode or I²C mode when ENDINIT is not set.

Table 91. SN0 Register (address C6h) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|---------|-----|-----|-----|-----|-----|-----|-----|
| Symbol | SN[7:0] | | | | | | | |
| Reset | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |
| Access | R | R | R | R | R | R | R | R |

Table 92. SN1 Register (address C7h) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|---------|-----|-----|-----|-----|-----|-----|-----|
| Symbol | SN[7:0] | | | | | | | |
| Reset | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |
| Access | R | R | R | R | R | R | R | R |

Table 93. SN2 Register (address C8h) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|---------|-----|-----|-----|-----|-----|-----|-----|
| Symbol | SN[7:0] | | | | | | | |
| Reset | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |
| Access | R | R | R | R | R | R | R | R |

Table 94. SN3 Register (address C9h) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|---------|-----|-----|-----|-----|-----|-----|-----|
| Symbol | SN[7:0] | | | | | | | |
| Reset | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |
| Access | R | R | R | R | R | R | R | R |

Table 95. SN4 Register (address CAh) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|---------|-----|-----|-----|-----|-----|-----|-----|
| Symbol | SN[7:0] | | | | | | | |
| Reset | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |
| Access | R | R | R | R | R | R | R | R |

7.7.27 ASIC wafer ID registers

The ASIC wafer ID registers are factory programmed OTP registers that include the wafer number, wafer X and Y coordinates and the wafer lot number for the device ASIC. These registers are included in the factory programmed OTP array error detection. These registers are readable in SPI mode or I²C mode when ENDINIT is not set.

Table 96. ASICWFR# Register (address CBh) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|---------------|-----|-----|-----|-----|-----|-----|-----|
| Symbol | ASICWFR#[7:0] | | | | | | | |
| Reset | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |
| Access | R | R | R | R | R | R | R | R |

Table 97. ASICWFR_X Register (address CCh) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------------|-----|-----|-----|-----|-----|-----|-----|
| Symbol | ASICWFR_X[7:0] | | | | | | | |
| Reset | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |
| Access | R | R | R | R | R | R | R | R |

Table 98. ASICWFR_Y Register (address CDh) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------------|-----|-----|-----|-----|-----|-----|-----|
| Symbol | ASICWFR_Y[7:0] | | | | | | | |
| Reset | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |
| Access | R | R | R | R | R | R | R | R |

Table 99. ASICWLOT_L Register (address D0h) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|-----------------|-----|-----|-----|-----|-----|-----|-----|
| Symbol | ASICWLOT_L[7:0] | | | | | | | |
| Reset | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |
| Access | R | R | R | R | R | R | R | R |

Table 100. ASICWLOT_H Register (address D1h) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|-----------------|-----|-----|-----|-----|-----|-----|-----|
| Symbol | ASICWLOT_H[7:0] | | | | | | | |
| Reset | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |
| Access | R | R | R | R | R | R | R | R |

7.7.28 USERDATA_0 to USERDATA_E - user data registers

User data registers are user programmable OTP registers that contain user-specific information. These registers are included in the user programmed OTP array error detection. These registers are readable and writable in SPI mode or I²C mode when ENDINIT is not set.

7.7.29 USERDATA_10 to USERDATA_1E - user data registers

User data registers are user programmable OTP registers that contain user-specific information. These registers are included in the user programmed OTP array error detection. These registers are readable and writable in SPI mode or I²C mode when ENDINIT is not set.

7.7.30 Lock and CRC Registers

The lock and CRC Registers are automatically programmed OTP registers that include the lock bit, the block identifier, and the block OTP array CRC use for error detection. These registers are automatically programmed when the corresponding data array is programmed to OTP using the Write OTP Enable register.

Table 101. Lock and CRC Register bit definitions

| Location | | Bit | | | | | | | |
|-----------------|----------|----------|-------------------|---|---|--------------|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 5Fh | CRC_UF2 | LOCK_UF2 | 0 | 0 | 0 | CRC_UF2[3:0] | | | |
| Factory Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| AFh | CRC_F_A | LOCK_F_A | REGA_BLOCKID[2:0] | | | CRC_F_A[3:0] | | | |
| Factory Default | | 1 | 0 | 0 | 1 | varies | | | |
| BFh | CRC_F_B | LOCK_F_B | REGB_BLOCKID[2:0] | | | CRC_F_B[3:0] | | | |
| Factory Default | | 1 | 0 | 1 | 0 | varies | | | |
| CFh | CRC_F_C | LOCK_F_C | REGC_BLOCKID[2:0] | | | CRC_F_C[3:0] | | | |
| Factory Default | | 1 | 0 | 1 | 1 | varies | | | |
| DFh | CRC_F_D | LOCK_F_D | REGD_BLOCKID[2:0] | | | CRC_F_D[3:0] | | | |
| Factory Default | | 1 | 1 | 0 | 1 | varies | | | |
| EFh | CRC_F_E | LOCK_F_E | REGE_BLOCKID[2:0] | | | CRC_F_E[3:0] | | | |
| Factory Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| FFh | CRC_F_F | LOCK_F_F | REGF_BLOCKID[2:0] | | | CRC_F_F[3:0] | | | |
| Factory Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

7.7.31 Reserved registers

A register read command to a reserved register or a register with reserved bits results in a valid response. The data for reserved bits may be '0' or '1'.

A register write command to a reserved register or a register with reserved bits executes and results in a valid response. The data for the reserved bits may be '0' or '1'. A write to the reserved bits must always be '0' for normal device operation and performance.

7.7.32 Invalid register addresses

A register read command to a register address outside the addresses listed in [Section 7.6 "User-accessible data array"](#) results in a valid response. The data for the registers are '00h'.

A register write command to a register address outside the addresses listed in [Section 7.6 "User-accessible data array"](#) is not executable, but results in a valid response. The data for the registers are '00h'.

A register write command to a read-only register is not executable, but results in a valid response. The data for the registers is the current content of the registers.

7.8 Read/write register array CRC verification

The writable registers (all registers except for the DEVLOCK_WR register) are verified by a continuous 4-bit CRC that is calculated on the entire array once ENDINIT is set. The CRC verification uses a generator polynomial of $g(x) = X^4 + X^3 + 1$, with a seed value = '0000'.

8 Maximum ratings

Absolute maximum ratings are the limits that the device can be exposed to without permanently damaging it. Absolute maximum ratings are stress ratings only; functional


operation at these ratings is not guaranteed. Exposure to absolute maximum ratings conditions for extended periods might affect device reliability.


This device contains circuitry to protect against damage due to high static voltage or electrical fields. NXP advises that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit.

Table 102. Maximum ratings

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--|---|---|--------------|-----------------------|------|
| V _{CCMAX} | Supply Voltage | V _{CC} , V _{CCIO} | [1] — | +6.0 | V |
| V _{IOMAX} | Input/Output Max on pins | INT, TESTx, SS_B, SCLK/SCL, MOSI, MISO/SDA | [1] -0.3 | V _{CC} + 0.3 | V |
| h _{DROP} | Drop shock | To concrete, tile or steel surface, 10 drops, any orientation | [2] — | 1.2 | m |
| T _{stg} | Temperature range | Storage | [2] -40 | +130 | °C |
| T _J | | Junction | [3] -40 | +150 | °C |
| P _{MAX} | Maximum absolute pressure | Continuous | [3] — | 450 | kPa |
| P _{BURST} | | Burst (tested at 100 ms) | [2] — | 1650 | kPa |
| P _{MIN} | Minimum absolute pressure | Continuous | [1] — | 20 | kPa |
| f _{SEAL} | Pressure sealing force | Applied to top face of package | [1] — | 10 | N |
| θ _{JA} | Thermal resistance | | [4] — | 120 | °C/W |
| ESD and latch-up protection characteristics | | | | | |
| V _{ESD} | Electrostatic discharge (per AEC-Q100, Rev H) | Human body model (HBM) | [2] -2000 | 2000 | V |
| V _{ESD} | | Charge device model (CDM) | [2] [5] -500 | 500 | V |

- [1] Parameter verified by parametric and functional validation.
- [2] Parameter verified by qualification testing (Per AEC-Q100 Rev H or per NXP specification).
- [3] Functionality verified by modeling, simulation and/or design verification.
- [4] Thermal resistance provided with device mounted to a two-layer, 1.6 mm FR-4 PCB as documented in AN1902^[1] with one signal layer and one ground layer.
- [5] CDM tested at ±750 V for corner pins and ±500 V for all other pins.

| | |
|---|----------------|
|  | Caution |
| This device is sensitive to mechanical shock. Improper handling can cause permanent damage to the part. | |

| | |
|---|----------------|
|  msc896 | Caution |
| This is an ESD sensitive device. Improper handling can cause permanent damage to the part. | |

9 Operating range

Table 103. Electrical characteristics — supply and I/O

$V_{CC_min} \leq (V_{CC} - V_{SS}) \leq V_{CC_max}$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ °C/min, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Max | Units |
|---------------------|---|--|--------------|---------------|-------|
| V_{CC} | Supply voltage | Measured at V_{CC} ^[1] | 3.10 | 5.25 | V |
| T_A | Operating temperature range | $V_{CC} = 5.0$ V, unless otherwise stated. Production tested operating temperature range ^[1] | T_L -40 | T_H +130 | °C |
| T_A | | Guaranteed operating temperature range ^[1] | -40 | +130 | °C |
| $V_{CC_RAMP_SPI}$ | Supply power on ramp rate | ^[2] | 0.00001 | 10 | V/μs |
| V_{PP} | Programming voltage ($I_{PP} \leq 5$ mA, 15 °C $\leq T_A \leq 40$ °C) Applied to V_{CC} | | 9.0 | 11.0 | V |

[1] Parameter tested at final test.

[2] Parameter verified by parametric and functional validation.

10 Static characteristics

Table 104. Static characteristics

$V_{CC_min} \leq (V_{CC} - V_{SS}) \leq V_{CC_max}$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ °C/min, unless otherwise specified.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|--|--|--|-----------------|------|----------|--------|
| Supply and I/O | | | | | | |
| I_{IH} | Input current high | At V_{IH} ; SCLK/SCL ^[1] | 10 | 20 | 70 | μA |
| I_{IL} | Input current low | At V_{IL} ; SS_B ^[1] | -70 | -20 | -10 | μA |
| I_{MISO_Lkg} | MISO output leakage | ^[1] | -5 | — | 5 | μA |
| I_q | Supply current | $V_{CC} = 5.0$ V ^[1] | — | — | 8.0 | mA |
| $V_{CC_UV_F}$ | Low-voltage detection threshold | V_{CC} falling ^[1] | 2.64 | 2.74 | 2.84 | V |
| V_{I_HYST} | Input voltage hysteresis | SCLK/SCL, SS_B, MOSI ^[2] | 0.125 | — | 0.500 | V |
| V_{IH} | Input high voltage (at $V_{CC} = 3.3$ V) | SCLK/SCL, SS_B, MOSI ^[1] | 2.0 | — | — | V |
| V_{IL} | Input low voltage | SCLK/SCL, SS_B, MOSI ^[1] | — | — | 1.0 | V |
| V_{INT_OH} | Output high voltage | $I_{Load} = -100$ μA ^[1] | $V_{CC} - 0.35$ | — | V_{CC} | V |
| V_{INT_OL} | Output low voltage | $I_{Load} = 100$ μA ^[1] | — | — | 0.1 | V |
| V_{OH} | Output high voltage | MISO/SDA, $I_{Load} = -1$ mA ^[1] | $V_{CC} - 0.2$ | — | — | V |
| Temperature sensor signal chain | | | | | | |
| T_{RANGE} | Temperature measurement range | ^[3] | -50 | — | +160 | °C |
| T_{25} | Temperature output | At 25 °C ^[3] | 83 | 93 | 103 | LSB |
| T_{RANGE} | Range of output (8-bit) | Unsigned temperature ^[3] | 0 | — | 255 | LSB |
| T_{SENSE} | Temperature output sensitivity (8-bit) | ^[4] | — | 1.00 | — | LSB/°C |
| T_{ACC} | Temperature output accuracy (8-bit) | ^[4] | -10 | — | +10 | °C |
| T_{RMS} | Temperature output noise RMS (8-bit) | Standard deviation of 50 readings, $f_{smp} = 8$ kHz ^[4] | — | — | +2 | LSB |
| Absolute pressure sensor signal chain | | | | | | |
| P_{ABS} | Absolute pressure range | ^{[1] [4]} | 20 | — | 400 | kPa |

Table 104. Static characteristics...continued

$V_{CC_min} \leq (V_{CC} - V_{SS}) \leq V_{CC_max}$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25 \text{ }^\circ\text{C/min}$, unless otherwise specified.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|--------------------------------------|---------------------------------------|--|----------|-----|------|-------------|
| P _{SENS} | Absolute pressure output sensitivity | P_CAL_ZERO = 0h V _{CC} = 5.0 V. 12-bit at 0 Hz, tested at P _{ABS} = 200 kPa ± 10 % and 300 kPa ± 10 % | [5] — | 9.2 | — | LSB/ kPa |
| P _{ACC_HIT} | Absolute pressure accuracy | V _{CC} = 5.0 V. 85 °C < T _A ≤ 130 °C | [5] -5.7 | — | +5.7 | kPa |
| P _{ACC_Typ} | Absolute pressure accuracy | V _{CC} = 5.0 V. 0 °C ≤ T _A ≤ 85 °C | [5] -3.8 | — | +3.8 | kPa |
| P _{ACC_LoT} | Absolute pressure accuracy | V _{CC} = 5.0 V. -40 °C ≤ T _A < 0 °C | [5] -5.7 | — | +5.7 | kPa |
| P _{ABS_DErr} | Absolute pressure output range | Digital error response | [2] — | 0 | — | LSB |
| P _{ABS_DRng} | Absolute pressure output range | Digital, 12-bit | [2] 1 | — | 4095 | LSB |
| P _{ABS_DRng} | Absolute pressure output range | Digital error response | [2] — | 0 | — | LSB |
| P _{ABS_DNL} | Absolute pressure nonlinearity | Absolute pressure DNL, 12-bit monotonic with no missing codes | [3] — | — | +1 | LSB |
| P _{ABS_INL} | Absolute pressure nonlinearity | Absolute pressure INL, 12- bit (least squares BFSL) | [3] — | — | +20 | LSB |
| P _{ABS_Peak} | Absolute pressure noise peak (12-bit) | Temperature = -40 °C and 130 °C, V _{CC} = 5.0 V. Maximum deviation from mean, 50 readings, f _{samp} = 1 kHz, LPF = 1000 Hz, 4- pole | [1] -8 | — | +8 | LSB |
| P _{ABS_RMS} | Absolute pressure noise RMS (12-bit) | Temperature = -40 °C and 130 °C, V _{CC} = 5.0 V. Standard deviation of 50 readings, f _{samp} = 8 kHz, LPF = 1000 Hz, 4-pole | [5] — | — | +2 | LSB |
| P _{OFF_D12} | Absolute pressure offset | At minimum rated pressure, P_CAL_ZERO = 0h, Temperature = -40 °C and 130 °C, V _{CC} = 5.0 V, 12-bit | [5] — | 299 | — | LSB |
| PSC ₃ PSC _{SP13} | Digital power supply coupling | C _{VCC} = 0.1 μf, 12-bit data 1 kHz ≤ f _n ≤ 100 MHz, V _{CC} = 3.3 V ± 0.1 V | [3] — | — | 2 | LSB |
| PSC ₅ PSC _{SP15} | Digital power supply coupling | C _{VCC} = 0.1 μf, 12-bit data 1 kHz ≤ f _n ≤ 100 MHz, V _{CC} = 5.0 V ± 0.1 V | [3] — | — | 2 | LSB |

- [1] Parameter verified by pass/fail testing at final test.
- [2] Functionality verified by modeling, simulation and/or design verification.
- [3] Parameter verified by functional validation.
- [4] Parameter verified by characterization.
- [5] Parameter tested at final test.

11 Dynamic characteristics

Table 105. Dynamic characteristics

$V_{CC_{min}} \leq (V_{CC} - V_{SS}) \leq V_{CC_{max}}$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ °C/min, unless otherwise specified.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|------------------------------|--|---|-------|------|------|-------|
| I ² C | | | | | | |
| t _{SCL_100} | Clock (SCL) period (30 % of V _{CC} to 30 % of V _{CC}) | 100 kHz mode | [1] — | 9.50 | — | µs |
| t _{SCLK_400} | | 400 kHz mode | [1] — | 2.37 | — | µs |
| t _{SCLK_1000} | | 1000 kHz mode | [1] — | 1.00 | — | µs |
| t _{SCLH_100} | Clock (SCL) high time (70 % of V _{CC} to 70 % of V _{CC}) | 100 kHz mode | [1] — | 4.00 | — | µs |
| t _{SCLH_400} | | 400 kHz mode | [1] — | 0.60 | — | µs |
| t _{SCLH_1000} | | 1000 kHz mode (not compliant with UM10204, rev.6) | [1] — | 0.50 | — | µs |
| t _{SCLL_100} | Clock (SCL) low time (30 % of V _{CC} to 30 % of V _{CC}) | 100 kHz mode | [1] — | 4.70 | — | µs |
| t _{SCLL_400} | | 400 kHz mode | [1] — | 1.30 | — | µs |
| t _{SCLL_1000} | | 1000 kHz mode | [1] — | 0.50 | — | µs |
| t _{SRISE_100} | Clock (SCL) and data (SDA) risetime (30 % of V _{CC} to 70 % of V _{CC}) | 100 kHz mode | [1] — | — | 1000 | ns |
| t _{SRISE_400} | | 400 kHz mode | [1] — | — | 300 | ns |
| t _{SRISE_1000} | | 1000 kHz mode | [1] — | — | 120 | ns |
| t _{SFALL_100} | Clock (SCL) and data (SDA) fall time (70 % of V _{CC} to 30 % of V _{CC}) | 100 kHz mode | [1] — | — | 300 | ns |
| t _{SFALL_400} | | 400 kHz mode | [1] — | — | 300 | ns |
| t _{SFALL_1000} | | 1000 kHz mode | [1] — | — | 120 | ns |
| t _{SETUP_100} | Data input setup time (SDA = 30/70 % of V _{CC} to SCL = 30 % of V _{CC}) | 100 kHz mode | [1] — | 250 | — | ns |
| t _{SETUP_400} | | 400 kHz mode | [1] — | 100 | — | ns |
| t _{SETUP_1000} | | 1000 kHz mode | [1] — | 50 | — | ns |
| t _{HOLD_100} | Data input hold time (SCL = 70 % of V _{CC} to SDA = 30/70 % of V _{CC}) | 100 kHz mode | [1] — | 0 | 900 | ns |
| t _{HOLD_400} | | 400 kHz mode | [1] — | 0 | 900 | ns |
| t _{HOLD_1000} | | 1000 kHz mode | [1] — | 0 | 300 | ns |
| t _{STARTSETUP_100} | Start condition setup time (SDA = 30/70 % of V _{CC} to SCL = 30 % of V _{CC}) | 100 kHz mode | [1] — | 4.70 | — | µs |
| t _{STARTSETUP_400} | | 400 kHz mode | [1] — | 0.60 | — | µs |
| t _{STARTSETUP_1000} | | 1000 kHz mode | [1] — | 0.26 | — | µs |
| t _{STARTHOLD_100} | Start condition hold time (SCL = 70 % of V _{CC} to SDA = 30/70 % of V _{CC}) | 100 kHz mode | [1] — | 4.00 | — | µs |
| t _{STARTHOLD_400} | | 400 kHz mode | [1] — | 0.60 | — | µs |
| t _{STARTHOLD_1000} | | 1000 kHz mode | [1] — | 0.26 | — | µs |
| t _{STOPSETUP_100} | Stop condition setup time (SDA = 30/70 % of V _{CC} to SCL = 30 % of V _{CC}) | 100 kHz mode | [1] — | 4.00 | — | µs |
| t _{STOPSETUP_400} | | 400 kHz mode | [1] — | 0.60 | — | µs |
| t _{STOPSETUP_1000} | | 1000 kHz mode | [1] — | 0.26 | — | µs |
| t _{VALID_100} | SCLK low to data valid (SCL = 30 % of V _{CC} to SDA = 30/70 % of V _{CC}) | 100 kHz mode | [1] — | — | 3.45 | µs |
| t _{VALID_400} | | 400 kHz mode | [1] — | — | 0.90 | µs |
| t _{VALID_1000} | | 1000 kHz mode | [1] — | — | 0.45 | µs |
| t _{FREE_100} | Bus free time (SDA = 70 % of V _{CC} to SDA = 70 % of V _{CC}) | 100 kHz mode | [1] — | 4.00 | — | µs |
| t _{FREE_400} | | 400 kHz mode | [1] — | 1.30 | — | µs |
| t _{FREE_1000} | | 1000 kHz mode | [1] — | 0.50 | — | µs |
| C _{BUS} | Bus capacitive load | | [2] — | — | 400 | pF |
| SPI | | | | | | |
| t _{SCLK} | Serial interface timing ^[3] | Clock (SCLK) period (10 % of V _{CC} to 10 % of V _{CC}) | [1] — | 90 | — | ns |
| t _{SCLKH} | Serial interface timing ^[3] | Clock (SCLK) period (90 % of V _{CC} to 90 % of V _{CC}) | [1] — | 30 | — | ns |
| t _{SCLKL} | | Clock (SCLK) period (10 % of V _{CC} to 10 % of V _{CC}) | [1] — | 30 | — | ns |
| t _{SCLKR} | Serial interface timing ^[3] | Clock (SCLK) period (10 % of V _{CC} to 90 % of V _{CC}) | [1] — | 10 | 25 | ns |
| t _{SCLKF} | | Clock (SCLK) period (90 % of V _{CC} to 10 % of V _{CC}) | [1] — | 10 | 25 | ns |

Table 105. Dynamic characteristics...continued

$V_{CC_min} \leq (V_{CC} - V_{SS}) \leq V_{CC_max}$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ °C/min, unless otherwise specified.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|-----------------------------|--|--|-----|------|-------|-------|
| t _{LEAD} | Serial interface timing ^[3] | SS_B asserted to SCLK high (SS_B = 10 % of V _{CC} to SCLK = 10 % of V _{CC}) ^[1] | — | 50 | — | ns |
| t _{ACCESS} | Serial interface timing ^[3] | SS_B asserted to SCLK high (SS_B = 10 % of V _{CC} to MISO = 10/90 % of V _{CC}) ^[1] | — | — | 50 | ns |
| t _{SETUP} | Serial interface timing ^[3] | SS_B asserted to SCLK high (MOSI = 10/90 % of V _{CC} to SCLK = 10 % of V _{CC}) ^[1] | — | 20 | — | ns |
| t _{HOLD_IN} | Serial interface timing ^[3] | MOSI data hold time (SCLK = 90 % of V _{CC} to MOSI = 10/90 % of V _{CC}) ^[1] | — | 10 | — | ns |
| t _{HOLD_OUT} | | MOSI data hold time (SCLK = 90 % of V _{CC} to MISO = 10/90 % of V _{CC}) ^[1] | 0 | — | — | ns |
| t _{VALID} | Serial interface timing ^[3] | SCLK low to data valid (SCLK = 10 % of V _{CC} to MISO = 10/90 % of V _{CC}) ^[1] | — | — | 30 | ns |
| t _{LAG} | Serial interface timing ^[3] | SCLK low to SS_B high (SCLK = 10 % of V _{CC} to SS_B = 90 % of V _{CC}) ^[1] | — | 60 | — | ns |
| t _{DISABLE} | Serial interface timing ^[3] | SS_B high to MISO disable (SS_B = 90 % of V _{CC} to MISO = Hi Z) ^[1] | — | — | 60 | ns |
| t _{SSN} | Serial interface timing ^[3] | SS_B high to SS_B low (SS_B = 90 % of V _{CC} to SS_B = 90 % of V _{CC}) ^[1] | — | 500 | — | ns |
| t _{SLKSS} | Serial interface timing ^[3] | SCLK low to SS_B low (SCLK = 10 % of V _{CC} to SS_B = 90 % of V _{CC}) ^[1] | — | 50 | — | ns |
| t _{SSCLK} | Serial interface timing ^[3] | SS_B high to SCLK high (SS_B = 90 % of V _{CC} to SCLK = 90 % of V _{CC}) ^[1] | — | 50 | — | ns |
| t _{LAT_SPI} | Data latency | | — | — | 1 | ns |
| Signal chain | | | | | | |
| t _{SigChain} | P _{ABS} low-pass filter | Signal chain sample time ^[4] | — | 48 | — | µs |
| f _{c0} | | Cutoff frequency, filter option #0, 4-pole ^{[2] [4]} | — | 800 | — | Hz |
| f _{c1} | | Cutoff frequency, filter option #1, 4-pole ^{[2] [4]} | — | 1000 | — | Hz |
| t _{SigDelay} | Signal delay (sinc filter to output delay, excluding the P _{ABS} LPF) ^[4] | | — | — | 128 | µs |
| T _{r_800Hz_LPF} | Response time | 10 % to 90 % of the final output value to input pressure step pulse. ^[4] | — | — | 0.53 | ms |
| T _{r_1kHz_LPF} | | | — | — | 0.42 | ms |
| T _{TD_800Hz_LPF} | Total delay time | Total delay (settling time) of the final output value to input pressure step pulse. ^[4] | — | — | 1.2 | ms |
| T _{TD_1kHz_LPF} | | | — | — | 1.0 | ms |
| t _{ST_INIT} | P _{ABS} startup common mode verification test time ^[4] | | — | — | 24 | ms |
| t _{ST_CMCONT} | P _{ABS} continuous common mode verification response time P _{ABS} error equivalent to 50 kPa ^[4] | | — | — | 4 | s |
| t _{ST_Resp_1000_4} | Self-test response time: self-test activation/deactivation to final value ^[4] | LPF = 1000 Hz, 4-pole | — | — | 2.016 | ms |

Table 105. Dynamic characteristics...continued
 $V_{CC_min} \leq (V_{CC} - V_{SS}) \leq V_{CC_max}$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ °C/min, unless otherwise specified.

| Symbol | Parameter | Condition | Min | Typ | Max | Units | |
|------------------------------|---|---|-------|--------|--------|-------|----|
| t _{ST_FP_Resp} | Fixed pattern response time: self-test activation/deactivation | [4] | — | — | 100 | µs | |
| f _{Package} | Package resonance frequency | [4] | 27.1 | — | — | kHz | |
| Supply and support circuitry | | | | | | | |
| t _{VCC_POR} | Reset recovery (all modes, excluding V _{CC} voltage ramp time) | V _{CC} = V _{CCMIN} to POR release | [2] | — | — | 1 | ms |
| t _{POR_I2C/POR_SPI} | | POR to first I ² C/SPI command | [4] | 0.800 | — | 1 | ms |
| t _{POR_DataValid} | | POR to sensor data valid | [4] | — | — | 7 | ms |
| t _{RANGE_DataValid} | | DSP setting change to sensor data valid | [2] | — | — | 7 | ms |
| t _{SOFT_RESET_I2C} | Soft reset activation time, command complete to reset (no ACK follows) | [4] | — | — | 700 | ns | |
| t _{SOFT_RESET_SPI} | Soft reset activation time, SS_B high to reset | [4] | — | — | 700 | ns | |
| t _{CC_POR} | V _{CC} undervoltage detection delay | [4] | — | — | 5 | µs | |
| t _{UVOV_RCV} | Undervoltage/overvoltage recovery delay | [4] | — | 100 | — | µs | |
| f _{OSC} | Internal oscillator period | [2] [4] | 9.500 | 10.000 | 10.500 | MHz | |

[1] Parameter verified by characterization.

[2] Parameter verified by functional evaluation.

[3] See [Section 7.5.6](#), C_{MISO} ≤ 80 pF, R_{MISO} ≥ 10 kΩ

[4] Functionality verified by modeling, simulation and/or design verification.

12 Media compatibility—pressure sensors only

For more information regarding media compatibility information, contact your local sales representative.

13 Application information

The FXPS7400D4 sensor can operate in two modes: I²C and SPI. The application diagrams in [Figure 23](#) and [Figure 24](#) show the modes and their respective biasing and bypass components.

The sensor can be configured to operate in SPI mode to read the user registers, self-test and diagnostics information. The application diagram in [Figure 24](#) shows the SPI and the respective biasing and bypass components.

Note: A gel is used to provide media protection against corrosive elements which may otherwise damage metal bond wires and/or IC surfaces. Highly pressurized gas molecules may permeate through the gel and then occupy boundaries between material surfaces within the sensor package. When decompression occurs, the gas molecules may collect, form bubbles and possibly result in delamination of the gel from the material it protects. If a bubble is located on the pressure transducer surface or on the bond wires, the sensor measurement may shift from its calibrated transfer function. In some cases, these temporary shifts could be outside the tolerances listed in the data sheet. In rare cases, the bubble may bend the bond wires and result in a permanent shift.

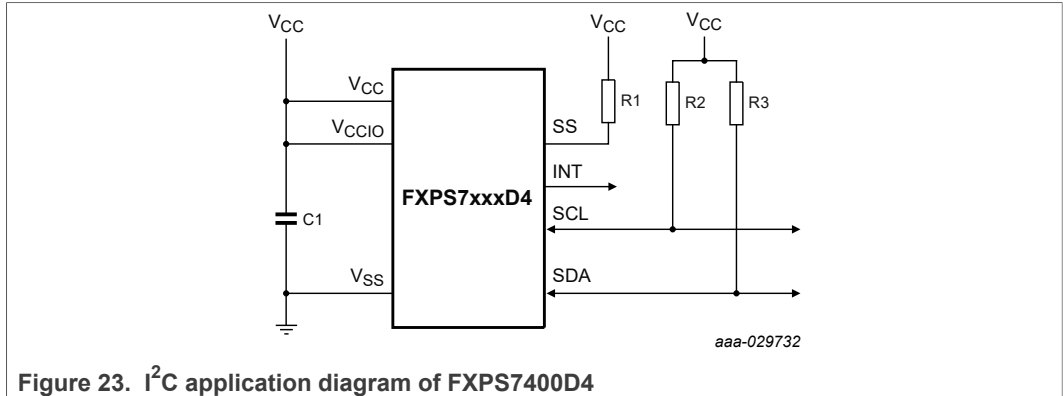


Figure 23. I²C application diagram of FXPS7400D4

Table 106. External component recommendations for I²C

| Name | Type | Description | Purpose |
|------|-----------------|---------------------------------|---|
| C1 | Ceramic | 0.1 μF, 10 %, 10 V minimum, X7R | V _{CC} power supply decoupling |
| R1 | General purpose | 1000 Ω, 5 %, 200 PPM | I ² C selection pin pull-up resistor |
| R2 | General purpose | 1000 Ω, 5 %, 200 PPM | Serial clock pull-up resistor |
| R3 | General purpose | 1000 Ω, 5 %, 200 PPM | Serial data pull-up resistor |

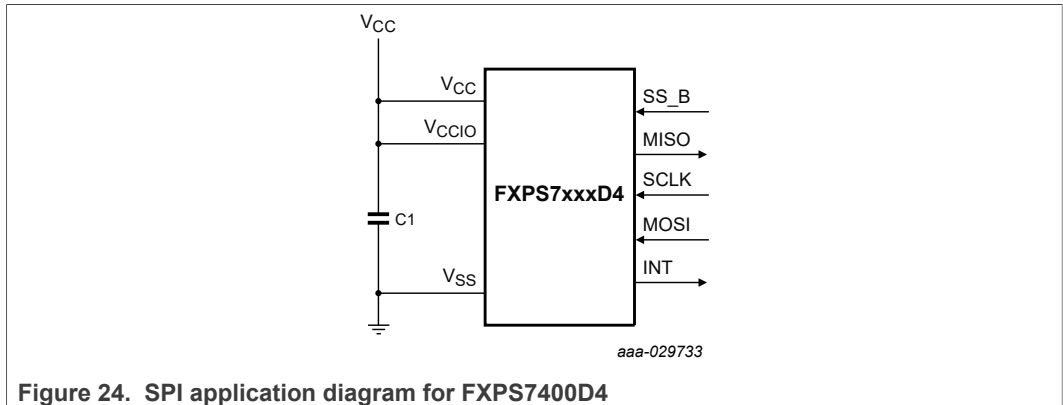


Figure 24. SPI application diagram for FXPS7400D4

Table 107. External component recommendations for SPI

| Name | Type | Description | Purpose |
|------|---------|---------------------------------|---|
| C1 | Ceramic | 0.1 μF, 10 %, 10 V minimum, X7R | V _{CC} power supply decoupling |

14 Package outline

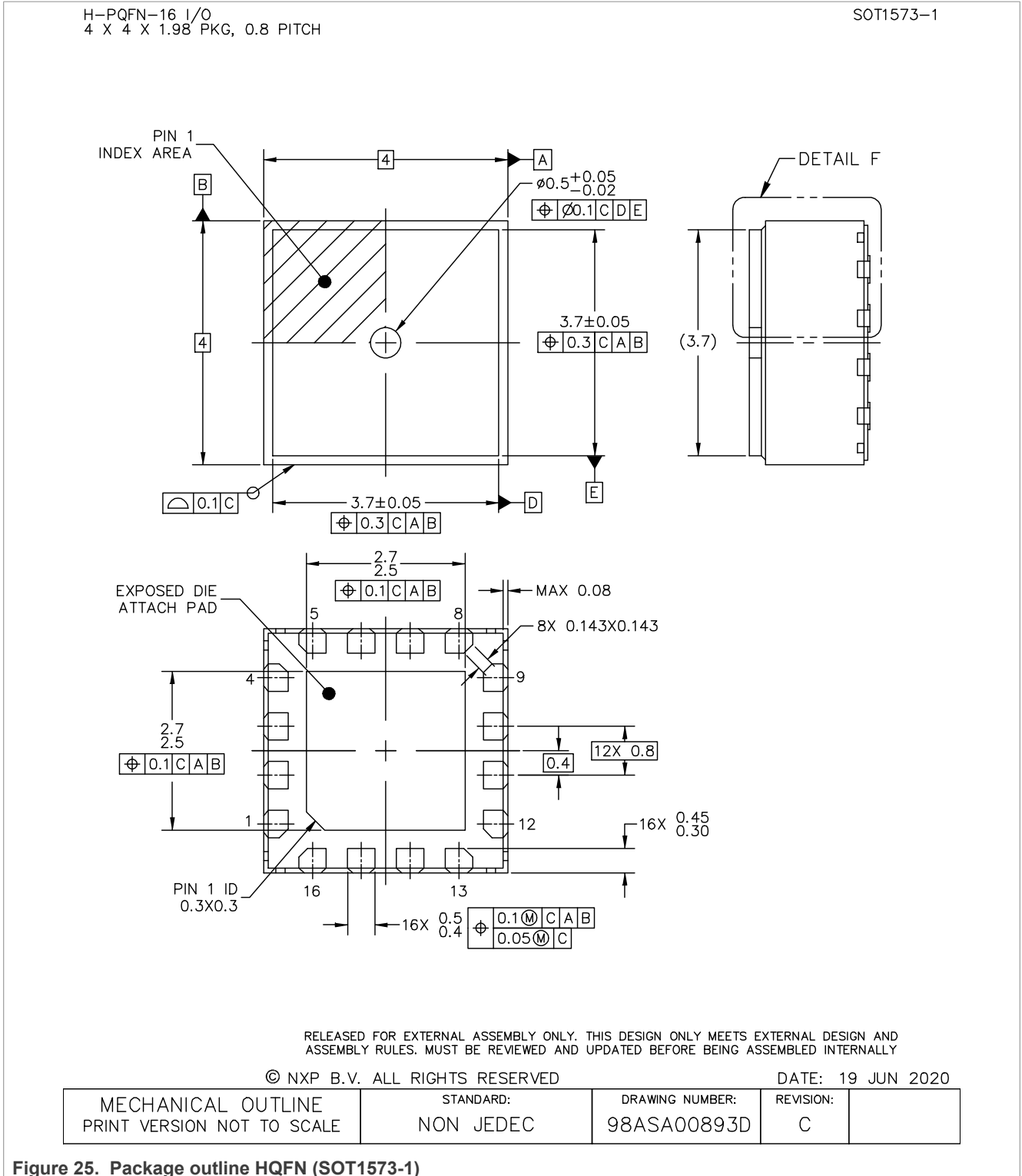
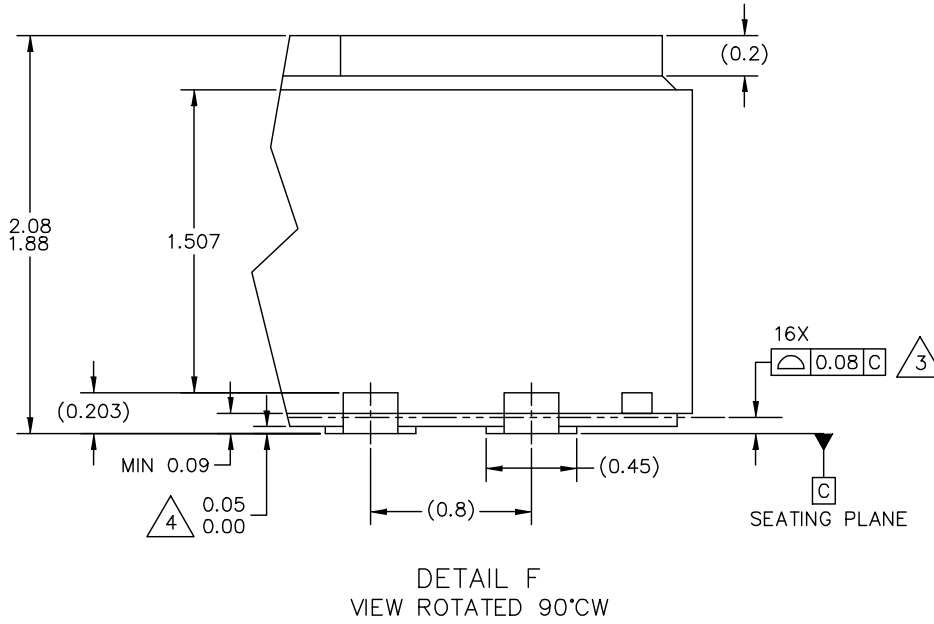


Figure 25. Package outline HQFN (SOT1573-1)

H-PQFN-16 I/O
4 X 4 X 1.98 PKG, 0.8 PITCH

SOT1573-1



RELEASED FOR EXTERNAL ASSEMBLY ONLY. THIS DESIGN ONLY MEETS EXTERNAL DESIGN AND ASSEMBLY RULES. MUST BE REVIEWED AND UPDATED BEFORE BEING ASSEMBLED INTERNALLY

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DATE: 19 JUN 2020

| | | | | |
|--|------------------------|--------------------------------|----------------|--|
| MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE | STANDARD: NON JEDEC | DRAWING NUMBER: 98ASA00893D | REVISION: C | |
|--|------------------------|--------------------------------|----------------|--|

Figure 26. Package outline detail HQFN (SOT1573-1)

H-PQFN-16 I/O
4 X 4 X 1.98 PKG, 0.8 PITCH

SOT1573-1

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. COPLANARITY APPLIES TO LEADS AND DIE ATTACH PAD.
4. DIMENSION APPLIES ONLY FOR TERMINALS.
5. MIN METAL GAP SHOULD BE 0.2 MM.

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DATE: 19 JUN 2020

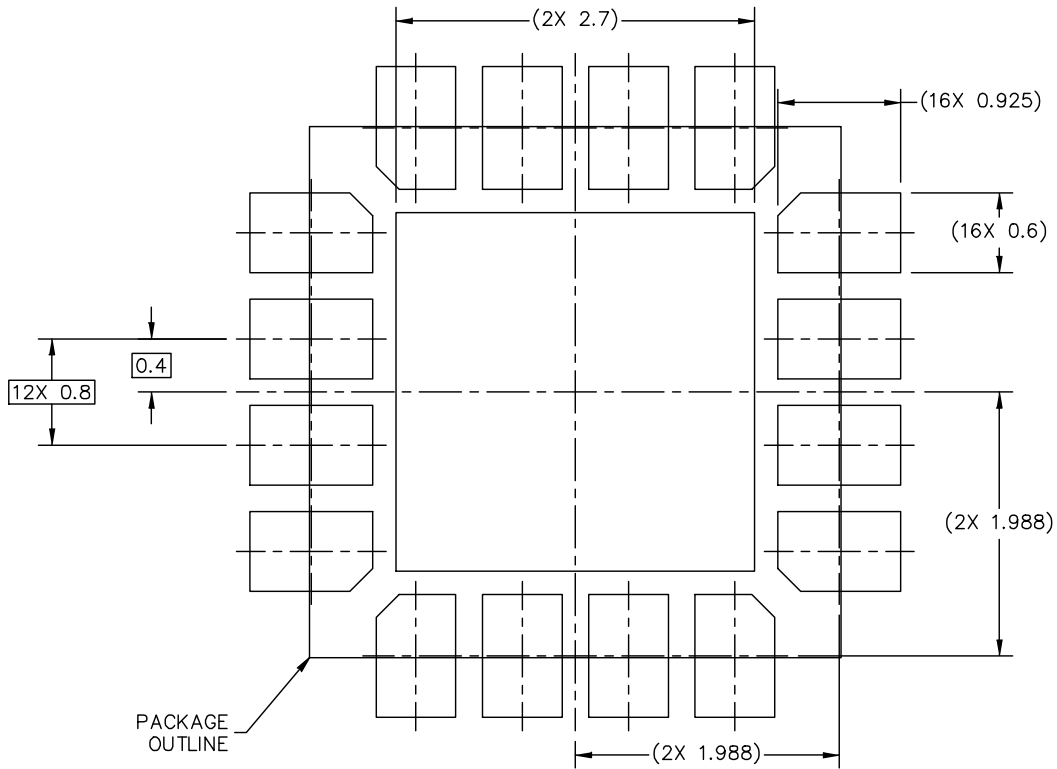
| | | | | |
|--|------------------------|--------------------------------|----------------|--|
| MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE | STANDARD: NON JEDEC | DRAWING NUMBER: 98ASA00893D | REVISION: C | |
|--|------------------------|--------------------------------|----------------|--|

Figure 27. Package outline note HQFN (SOT1573-1)

15 Soldering

H-PQFN-16 I/O
4 X 4 X 1.98 PKG, 0.8 PITCH

SOT1573-1



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

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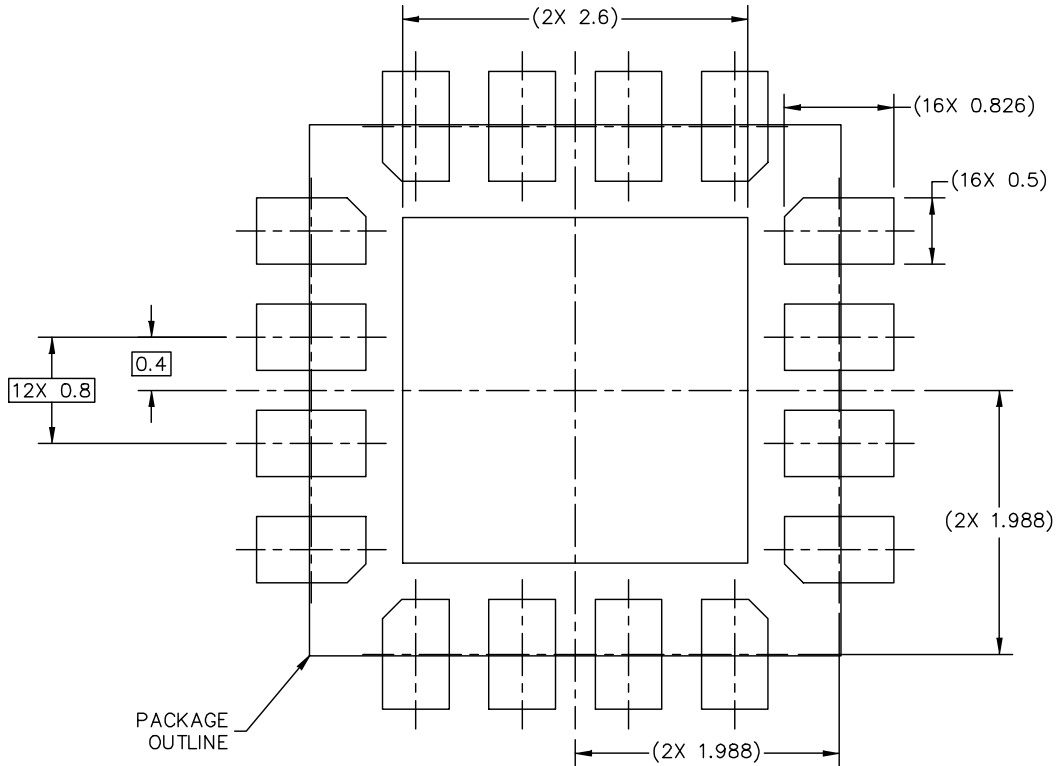
DATE: 19 JUN 2020

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|--|------------------------|--------------------------------|----------------|--|
| MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE | STANDARD: NON JEDEC | DRAWING NUMBER: 98ASA00893D | REVISION: C | |
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Figure 28. SOT1573-1 PCB design guidelines - Solder mask opening pattern

H-PQFN-16 I/O
4 X 4 X 1.98 PKG, 0.8 PITCH

SOT1573-1



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

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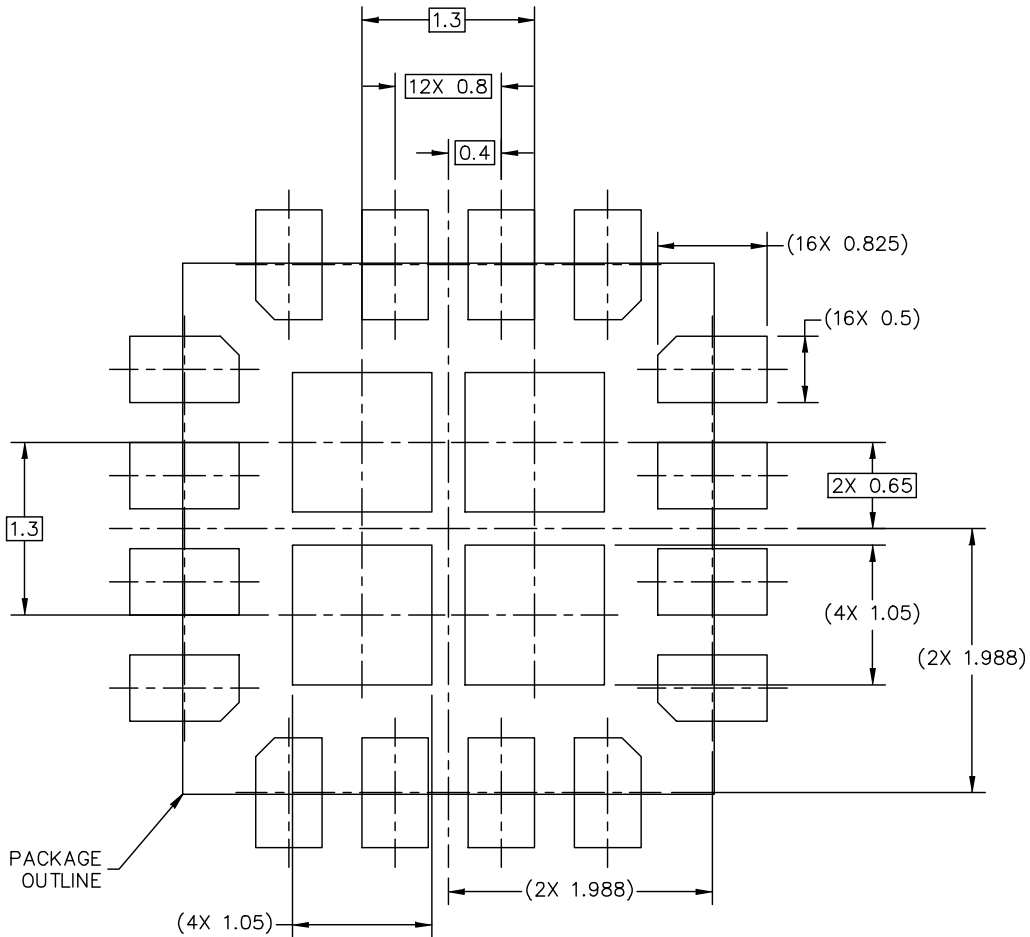
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Figure 29. SOT1573-1 PCB design guidelines - I/O pads and solderable area

H-PQFN-16 I/O
4 X 4 X 1.98 PKG, 0.8 PITCH

SOT1573-1



RECOMMENDED STENCIL THICKNESS 0.125 OR 0.15

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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Figure 30. SOT1573-1 PCB design guidelines - Solder paste stencil

16 Mounting recommendations

The package should be mounted with the pressure port pointing away from sources of debris which might otherwise plug the sensor.

A plugged port exhibits no change in pressure and can be cross checked in the user software.

Refer to NXP application note AN1902^[1] for proper printed circuit board attributes and recommendations.

17 References

- [1] **AN1902 - Assembly guidelines for QFN (quad flat no-lead) and SON (small outline no-lead) packages**
<https://www.nxp.com/docs/en/application-note/AN1902.pdf>
- [2] **AEC documents on Automotive Electronics Council Component Technical Committee's site:**
<http://www.aecouncil.com/AECDocuments.html>
- [3] **AN12727 - FXPS7xxxDI4 User method to flash UF2**
<https://www.nxp.com/webapp/Download?colCode=AN12727&location=null>
- [4] **I²C-Bus specification and user manual** — NXP User Manual (UM) 10204, Rev. 6 - 4 April 2014, 64 pages,
<https://www.nxp.com/docs/en/user-guide/UM10204.pdf>

18 Revision history

Table 108. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------|--|--------------------|---------------|----------------|
| FXPS7400D4 v.6 | 20220606 | Product data sheet | — | FXPS7400D4 v.5 |
| Modifications: | <ul style="list-style-type: none"> • Global: Performed the following global changes: <ul style="list-style-type: none"> – Performed minor grammatical and typographic changes throughout. – Revised all register value formats from the format "\$xx" to the format "xxh" throughout to conform to NXP standards. – Revised "Master" and "Slave" to "Host" and "Client" to conform to the NXP inclusive language. – Updated the image on the first page. • Section 1, removed "The FXPS7400D4 uses either a 3.3 V or 5.0 V power supply." from the second paragraph. • Section 3, revised "Engine management digital BAP" to "Engine management digital MAP and BAP." • Section 6.1, Figure 2, revised the pin 11 label in the image from "MISO" to "MISO/SDA" and revised the label for pin 9 from "SCLK" to "SCLK/SCL". • Section 6.2, Table 3, revised "2, 5, 12" to "2, 12" and inserted new row for pin 5. • Section 7.2, revised "... trimmed oscillator as specified in Table 101" to "...trimmed oscillator". • Section 7.3: Removed the first subsection titled "Transducer". • Section 7.3.1, revised "DSP_CFG_U1" to "DSP_CFG_U5" in the first paragraph. • Section 7.3.1.1, Figure 4, revised the image. • Section 7.3.2, Figure 5, revised the image. • Section 7.3.3, Figure 6, revised the image. • Section 7.3.3.4, Table 7, added new table title and revised the entire table. • Section 7.4.3, Figure 16, revised the image changing "slave" to "client". • Section 7.4.6.1 and Section 7.4.6.2, revised images changing "Master" to "Host" and "Slave" to "Client". | | | |

Table 108. Revision history...continued

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------|--|------------------------|---------------|----------------|
| | FXPS7400D4 v.6 Modifications (Continued) <ul style="list-style-type: none"> • Section 7.7.7.1, inserted new section including Table 57. • Removed section titled "TIMING_CF - communication timing register (address 22h)". • Section 7.7.11, revised the content of the second paragraph. • Section 7.7.11.1, revised as follows: <ul style="list-style-type: none"> – Table 64: revised bits 1 and 0 from "User_Range[1]" and "User_Range[0]" to "reserved". – Table 65: revised the entire table and added table notes. – Added note below Table 65. • Section 7.7.11.2, Section 7.7.11.2.1, and Section 7.7.11.2.2 added new sections. • Section 7.7.11.3, Table 70, removed rows "7 to 4" and "1 to 0" from the table. • Section 7.7.14, updated Equation 6 and removed the "Where" content after the equation. • Section 7.7.15, Table 78, revised bits 6 and 5 from "PABS_HIGH" and "PABS_LOW" to "reserved" and removed the rows for bits 6 and 5 from Table 79. • Section 7.7.16, inserted new paragraph after Table 80. • Section 7.7.18, inserted additional content in the first paragraph. • Section 7.7.20, removed the sentence "The error will always be within 2 kPa of each other." from the end of the second paragraph. • Removed the section titled "DSP_CFG_F Register" including the table titled "Range Indication Bits (RANGE[3:0])" following Section 7.7.21 "FRT - free running timer registers (addresses 78h to 7Dh)". • Section 9, Table 103, inserted row for V_{PP}, and revised the table footnote "Parameter tested 100 % at final test." to "Parameter tested at final test." • Section 10, Table 104, revised as follows: <ul style="list-style-type: none"> – I_q: Removed "Quiescent" from the parameter description of I_q. – PABS_{Peak} and PABS_{RMS}: revised the conditions. – Revised table footnote from "Parameter verified by parametric and functional validation" to "Parameter verified by functional validation". – Revised table footnote from "Parameter tested 100 % at final test." to "Parameter tested at final test." • Section 11, Table 105, revised as follows: <ul style="list-style-type: none"> – Added four rows in the Signal Chain section, "T_{r_800Hz_LPF}", "T_{r_1kHz_LPF}", "T_{TD_800Hz_LPF}", and "T_{TD_1kHz_LPF}". – T_{ST_INIT}: revised the Max value "20" to "24". – t_{POR_I2C/POR_SPI}: revised the condition and the Min value from "0.400" to "0.800" and the max value from "0.700" to "1". – t_{POR_DataValid} and t_{RANGE_DataValid}: revised the Max value from "6" to "7". – f_{OSC}: inserted new row. • Section 15 "Soldering", inserted new section. • Section 16 "Mounting recommendations", inserted new section. • Section 17, updated the reference section content. | | | |
| FXPS7400D4 v.5 | 20190715 | Product data sheet | — | FXPS7400D4 v.4 |
| FXPS7400D4 v.4 | 20190507 | Product data sheet | — | FXPS7400D4 v.3 |
| FXPS7400D4 v.3 | 20190506 | Preliminary data sheet | — | FXPS7400D4 v.2 |
| FXPS7400D4 v.2 | 20190408 | Preliminary data sheet | — | FXPS7400D4 v.1 |
| FXPS7400D4 v.1 | 20190327 | Preliminary data sheet | — | — |

19 Legal information

19.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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