ISL91108

High Efficiency Buck-Boost Regulator with 4.2A Switches

FN8448
Rev 1.00
November 12, 2014

The ISL91108 is a highly-integrated buck-boost switching regulator that accepts input voltages either above or below the regulated output voltage. Unlike other buck-boost regulators, this regulator automatically transitions between operating modes without significant output disturbance.

This device is capable of delivering up to 2.7A of burst current (PVIN = 3V, V_{OUT} = 3.3V), and provides excellent efficiency due to its fully synchronous 4-switch architecture. No load quiescent current of only 27.5µA also optimizes efficiency under light-load conditions. Forced PWM and/or synchronization to an external clock may also be selected for noise sensitive applications.

The ISL91108 is designed for standalone applications and supports a 3.3V fixed output voltage or variable output voltages with an external resistor divider. Output voltages as low as 1V or as high as 5.2V are supported using an external resistor divider.

The ISL91108 requires only a single inductor and very few external components. Power supply solution size is minimized by a 2.34mmx1.72mm WLCSP and a 2.6MHz switching frequency, which further reduces the size of external components.

Related Literature

- AN1903 "ISL91108IIA-EVZ/ISL91108IIN-EVZ Evaluation Board User Guide"

Features

- Accepts input voltages above or below regulated output voltage
- Automatic and seamless transitions between buck and boost modes
- Input voltage range: 1.8V to 5.5V
- Output current: up to 1.6A DC (PVIN = 2.8V, V_{OUT} = 3.3V)
- Burst current: up to 2.7A (PVIN = 3V, V_{OUT} = 3.3V, t_{ON} <600µs, t = 4.6ms)
- High efficiency: up to 95%
- 27.5µA quiescent current maximizes light load efficiency
- 2.6MHz switching frequency minimizes external component size
- Selectable forced PWM mode and external synchronization
- Fully protected for short-circuit, over-temperature, and undervoltage
- Small 2.34mm x 1.72mm WLCSP

Applications

- Smartphones and tablets
- Wireless communication devices
- 2G/3G/4G power amplifiers

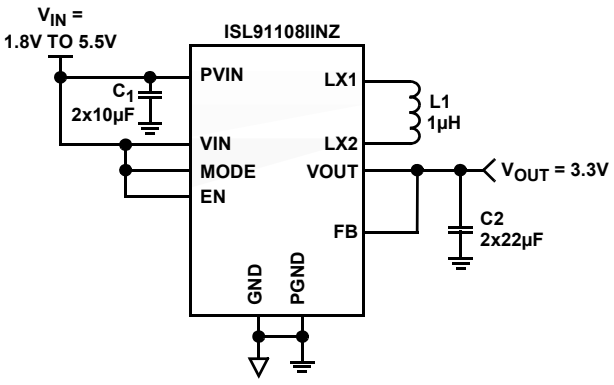


FIGURE 1. TYPICAL FIXED OUTPUT APPLICATION

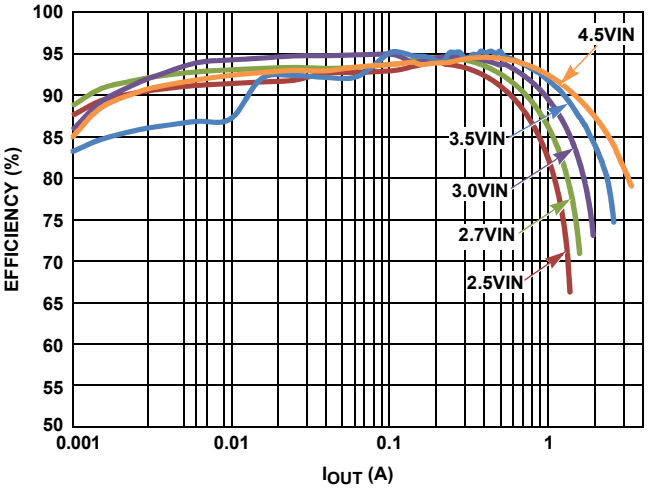
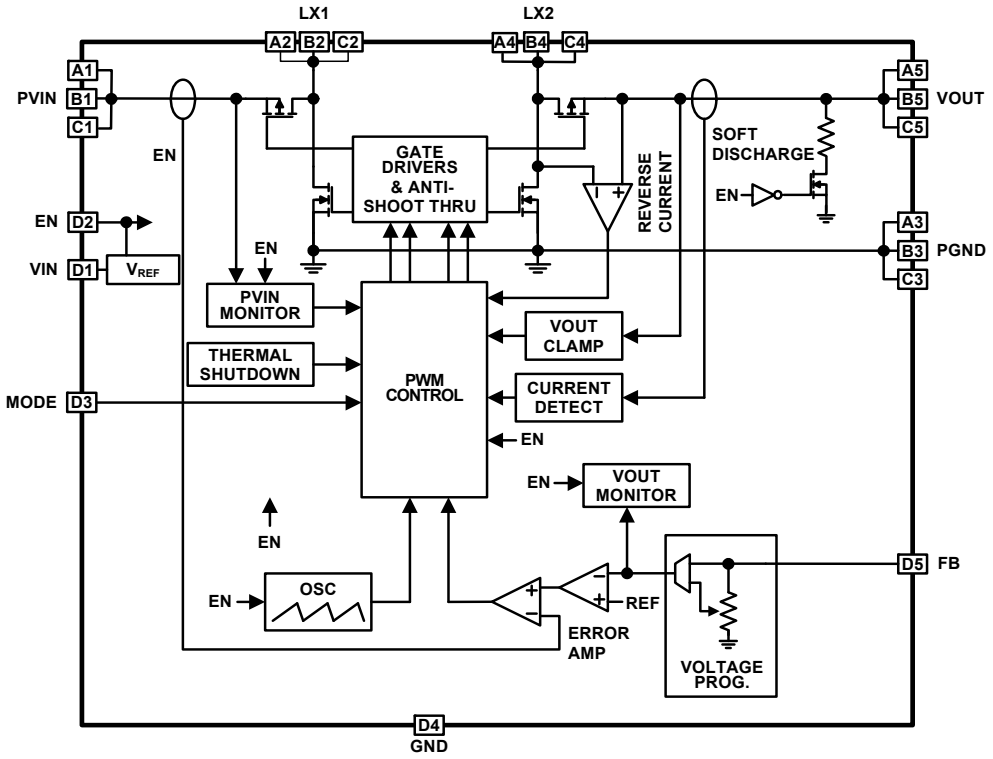


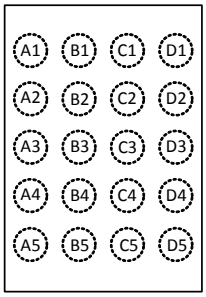
FIGURE 2. ISL91108IINZ EFFICIENCY vs OUTPUT CURRENT

Block Diagram



Pin Configuration

ISL91108
(20 BUMP WLCSP)
TOP VIEW



Pin Descriptions

PIN #	PIN NAMES	DESCRIPTION
A5, B5, C5	VOUT	Buck-boost output. Connect 2x22µF capacitor to PGND.
A4, B4, C4	LX2	Inductor connection, output side.
A3, B3, C3	PGND	Power ground for high switching current.
A2, B2, C2	LX1	Inductor connection, input side.
A1, B1, C1	PVIN	Power input. Range: 1.8V to 5.5V. Connect 2x 10µF capacitor to PGND.
D1	VIN	Supply input. Range: 1.8V to 5.5V.
D2	EN	Logic input, drive HIGH to enable device.
D3	MODE/ SYNC	Logic input, HIGH for auto PFM mode. LOW for forced PWM operation. Also, this pin can be used with an external clock sync input. Range: 2.75MHz to 3.25MHz.
D4	GND	Analog ground pin.
D5	FB	Voltage feedback pin.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	VOUT (V)	TEMP RANGE (°C)	PACKAGE Tape and Reel (Pb-free)	PKG. DWG. #
ISL91108IINZ-T	GAZA	3.3	-40 to +85	20 Bump WLCSP	W4x5.20F
ISL91108IINZ-T7A	GAZA	3.3	-40 to +85	20 Bump WLCSP	W4x5.20F
ISL91108IIAZ-T	GAXA	ADJ.	-40 to +85	20 Bump WLCSP	W4x5.20F
ISL91108IIAZ-T7A	GAXA	ADJ.	-40 to +85	20 Bump WLCSP	W4x5.20F
ISL91108IIN-EVZ	Evaluation Board for ISL91108IINZ				
ISL91108IIA-EVZ	Evaluation Board for ISL91108IIAZ				

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL91108. For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings

PVIN, VIN . . . . . -0.3V to 6.5V
LX1, LX2 (Note 6) . . . . . -0.3V to 6.5V
FB (ISL91108IIAZ) . . . . . -0.3V to 2.7V
FB (ISL91108IINZ) . . . . . -0.3V to 6.5V
GND, PGND . . . . . -0.3V to 0.3V
All Other Pins . . . . . -0.3V to 6.5V
ESD Rating
Human Body Model (Tested per JESD22-A114E) 2.5kV
Machine Model (Tested per JESD22-A115-A) 200V
Charged Device Model 2kV
Latch Up (Tested per JESD-78B; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
2.34x1.72 WLCSP (Notes 4, 5)	66	1.0

Maximum Junction Temperature . . . . . +125°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Temperature Range . . . . . -40°C to +85°C
Supply Voltage (V_{IN}) Range . . . . . 1.8V to 5.5V
Load Current (I_{OUT}) Range (DC) . . . . . 0A to 1.6A
Maximum Burst Current (t_{ON} <600µs, t = 4.6ms) 2.7A

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
6. LX1 and LX2 pins can withstand switching transients of -1.5V for 100ns, and 7V for 20ms.

Analog Specifications

V_{IN} = PVIN = EN = 3.6V, V_{OUT} = 3.3V, L_1 = 1µH, C_1 = 2x 10µF, C_2 = 2x 22µF, T_A = +25°C. **Boldface limits apply across the recommended operating temperature range, -40°C to +85°C and input voltage ranges.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
POWER SUPPLY						
VIN	Input Voltage Range		**1.8**		**5.5**	V
V_{UVLO}	V_{IN} Undervoltage Lockout Threshold	Rising		1.725	**1.775**	V
		Falling	**1.550**	1.650		V
I_{VIN}	V_{IN} Supply Current	PFM mode, no external load on V_{OUT} (Note 8)		27.5	**60**	µA
I_{SD}	V_{IN} Supply Current, Shutdown	EN = GND		0.4	**1.0**	µA
OUTPUT VOLTAGE REGULATION						
VOUT	Output Voltage Range	ISL91108IIAZ, I_{OUT} = 100mA	**1.00**		**5.20**	V
	Output Voltage Accuracy	I_{OUT} = 0mA, PWM mode	**-2**		**+2**	%
		I_{OUT} = 1mA, PFM mode	**-3**		**+4**	%
V_{FB}	FB Pin Voltage Regulation	For adjustable output version (ISL91108IIAZ)	**0.788**	0.80	**0.812**	V
I_{FB}	FB Pin Bias Current	For adjustable output version (ISL91108IIAZ)			**0.2**	µA
ΔVOUT / ΔVIN	Line Regulation, PWM Mode	I_{OUT} = 500mA, MODE = GND, V_{IN} step from 2.3V to 5.5V		±0.005		mV/mV
ΔVOUT / ΔI_{OUT}	Load Regulation, PWM Mode	V_{IN} = 3.7V, MODE = GND, I_{OUT} step from 0mA to 500mA		±0.005		mV/mA
ΔVOUT/ ΔVIN	Line Regulation, PFM Mode	I_{OUT} = 100mA, MODE = V_{IN}, V_{IN} step from 2.3V to 5.5V		±12.5		mV/V
ΔVOUT/ ΔI_{OUT}	Load Regulation, PFM Mode	V_{IN} = 3.7V, MODE = V_{IN}, I_{OUT} step from 0mA to 100mA		±0.4		mV/mA
V_{CLAMP}	Output Voltage Clamp	Rising	**5.25**		**5.95**	V
	Output Voltage Clamp Hysteresis			400		mV
DC/DC SWITCHING SPECIFICATIONS						
f_{SW}	Oscillator Frequency	V_{IN} = 3.6V	**2.4**	2.6	**2.9**	MHz
t_{ONMIN}	Minimum On Time			80		ns
$I_{PFETLEAK}$	LX1 Pin Leakage Current		**-0.5**		**+0.5**	µA
$I_{NFETLEAK}$	LX2 Pin Leakage Current		**-0.5**		**+0.5**	µA

Analog Specifications V_{IN} = PVIN = EN = 3.6V, V_{OUT} = 3.3V, L_1 = 1µH, C_1 = 2x 10µF, C_2 = 2x 22µF, T_A = +25°C. **Boldface limits apply across the recommended operating temperature range, -40°C to +85°C and input voltage ranges. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
SOFT-START and SOFT DISCHARGE						
t_{SS}	Soft-start Time	Time from when EN signal asserts to when output voltage ramp starts.		1		ms
		Time from when output voltage ramp starts to when output voltage reaches 95% of its nominal value with device operating in buck mode. V_{IN} = 4V, I_{OUT} = 200mA		1		ms
		Time from when output voltage ramp starts to when output voltage reaches 95% of its nominal value with device operating in boost mode. V_{IN} = 2V, I_{OUT} = 200mA		2		ms
R_{DISCHG}	VOUT Soft-Discharge ON-Resistance	EN < V_{IL}		110		Ω
POWER MOSFET						
R_{DSON_P}	P-Channel MOSFET ON-Resistance	I_{OUT} = 200mA		90		mΩ
R_{DSON_N}	N-Channel MOSFET ON-Resistance	I_{OUT} = 200mA		75		mΩ
I_{PK_LMT}	P-Channel MOSFET Peak Current Limit		**3.7**	4.2	**4.7**	A
PFM/PWM TRANSITION						
	Load Current Threshold, PFM to PWM			200		mA
	Load Current Threshold, PWM to PFM			75		mA
	External Synchronization Frequency Range	±2%	**2.75**		**3.25**	MHz
	Thermal Shutdown			150		°C
	Thermal Shutdown Hysteresis			35		°C
LOGIC INPUTS						
I_{LEAK}	Input Leakage			0.03	**0.5**	µA
V_{IH}	Input HIGH Voltage		**1.4**			V
V_{IL}	Input LOW Voltage				**0.4**	V

NOTES:

7. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
8. Quiescent current measurements are taken when the output is not switching.

Functional Description

Functional Overview

Refer to the "Block Diagram" on page 2. The ISL91108 implements a complete buck-boost switching regulator, with PWM controller, internal switches, references, protection circuitry, and control inputs.

The PWM controller automatically switches between buck and boost modes as necessary to maintain a steady output voltage with changing input voltages and dynamic external loads.

Internal Supply and References

Referring to the "Block Diagram" on page 2, the ISL91108 provides two power input pins. The PVIN pin supplies input power to the DC/DC converter, while the VIN pin provides operating voltage source required for stable V_{REF} generation. Separate ground pins (GND and PGND) are provided to avoid problems caused by ground shift due to the high switching currents.

Enable Input

A master enable pin EN allows the device to be enabled. Driving EN LOW invokes a power-down mode, where most internal device functions, including input and output power-good detection, are disabled.

Soft Discharge

When the device is disabled by driving EN LOW, an internal resistor between VOUT and GND is activated. This internal resistor has a typical resistance of 110Ω.

POR Sequence and Soft-start

Bringing the EN pin HIGH allows the device to power-up. A number of events occur during the start-up sequence. The internal voltage reference powers up and stabilizes. The device then starts operating. There is a 1ms (typical) delay between assertion of the EN pin and the start of switching regulator soft-start ramp.

The soft-start feature minimizes output voltage overshoot and input inrush currents. During soft-start, the reference voltage is ramped to provide a ramping VOUT voltage. While output voltage is lower than approximately 20% of the target output voltage, switching frequency is reduced to a fraction of the normal switching frequency to aid in producing low duty cycles necessary to avoid input in-rush current spikes. Once the output voltage exceeds 20% of the target voltage, switching frequency is increased to its nominal value.

When the target output voltage is higher than the input voltage, there will be a transition from buck mode to boost mode during the soft-start sequence. At the time of this transition, the ramp rate of the reference voltage is decreased, such that the output voltage slew rate is decreased. This provides a slower output voltage slew rate.

The VOUT ramp time is not constant for all operating conditions. Soft-start into boost mode will take longer than soft-start into buck mode. The total soft-start time into buck operating mode is typically 2ms, whereas the typical soft-start time into boost mode operating mode is typically 3ms. Increasing the load current will increase these typical soft-start times.

Short Circuit Protection

The ISL91108 provides short-circuit protection by monitoring the FB voltage. When FB voltage is sensed to be lower than a certain threshold, the PWM oscillator frequency is reduced in order to protect the device from damage. The P-Channel MOSFET peak current limit remains active during this state.

Undervoltage Lockout

The undervoltage lockout (UVLO) feature prevents abnormal operation in the event that the supply voltage is too low to guarantee proper operation. When the VIN voltage falls below the UVLO threshold, the regulator is disabled.

Thermal Shutdown

A built-in thermal protection feature protects the ISL91108, if the die temperature reaches +150°C (typical). At this die temperature, the regulator is completely shut down. The die temperature continues to be monitored in this thermal shutdown mode. When the die temperature falls to +115°C (typical), the device will resume normal operation.

When exiting thermal shutdown, the ISL91108 will execute its soft-start sequence.

External Synchronization

An external sync feature is provided. Applying a clock signal with a frequency between 2.75MHz and 3.25MHz at the MODE input forces the ISL91108 to synchronize to this external clock. The MODE input supports standard logic levels.

Buck-Boost Conversion Topology

The ISL91108 operates in either buck or boost mode. When operating in conditions where VIN is close to VOUT, the ISL91108 alternates between buck and boost mode as necessary to provide a regulated output voltage.

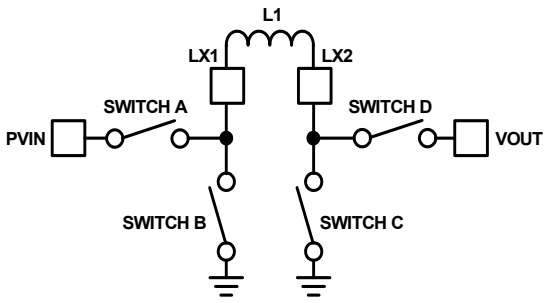


FIGURE 3. BUCK-BOOST TOPOLOGY

Figure 3 shows a simplified diagram of the internal switches and external inductor.

PWM Operation

In buck PWM mode, Switch D is continuously closed and Switch C is continuously open. Switches A and B operate as a synchronous buck converter when in this mode.

In boost PWM mode, Switch A remains closed and Switch B remains open. Switches C and D operate as a synchronous boost converter when in this mode.

PFM Operation

During PFM operation in buck mode, Switch D is continuously closed and Switch C is continuously open. Switches A and B operate in discontinuous mode during PFM operation. During PFM operation in boost mode, the ISL91108 closes Switch A and Switch C to ramp up the current in the inductor. When inductor current reaches a certain threshold, the device turns OFF Switches A and 10 C, then turns ON Switches B and D. With Switches B and D closed, output voltage increases as the inductor current ramps down.

In most operating conditions, there will be multiple PFM pulses to charge up the output capacitor. These pulses continue until V_{OUT} has achieved the upper threshold of the PFM hysteretic controller. Switching then stops, and remains stopped until V_{OUT} decays to the lower threshold of the hysteretic PFM controller.

Operation With V_{IN} Close to V_{OUT}

When the output voltage is close to the input voltage, the ISL91108 will rapidly and smoothly switch from boost to buck mode as needed to maintain the regulated output voltage. This behavior provides excellent efficiency and very low output voltage ripple.

Output Voltage Programming

The ISL91108 is available in fixed and adjustable output voltage versions. To use the fixed output version (ISL91108IINZ), the VOUT pin must be connected directly to FB.

In the adjustable output voltage version (ISL91108IIAZ), an external resistor divider is required to program the output voltage. The FB pin has very low input leakage current, so it is possible to use large value resistors (e.g., R_1 = 187kΩ and R_2 = 60kΩ) in the resistor divider connected to the FB input.

Applications Information

Component Selection

The fixed-output version of the ISL91108 requires only three external power components to implement the buck boost converter: an inductor, an input capacitor, and an output capacitor.

The adjustable ISL91108 versions require three additional components to program the output voltage. Two external resistors program the output voltage, and a small capacitor is added to improve stability and response.

An optional input supply filtering capacitor (“C_4” in Figure 4) can be used to reduce the supply noise on the VIN pin, which provides power to the internal reference. In most applications, this capacitor is not needed.

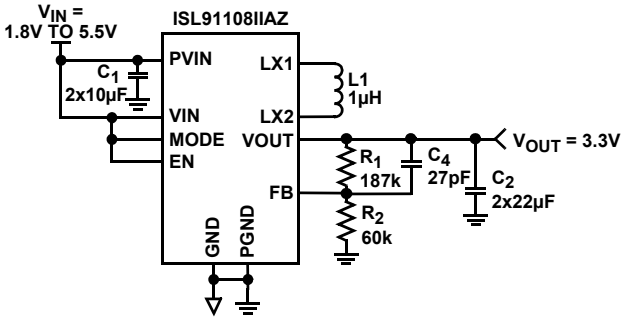


FIGURE 4. TYPICAL ISL91108IIAZ APPLICATION

Output Voltage Programming, Adjustable Version

Setting and controlling the output voltage of the ISL91108IIAZ (adjustable output version) can be accomplished by selecting the external resistor values.

Equation 1 can be used to derive the R_1 and R_2 resistor values:

$$VOUT = 0.8V \bullet \left(1 + \frac{R_1}{R_2}\right) \quad \text{(EQ. 1)}$$

When designing a PCB, include a GND guard band around the FB resistor network to reduce noise and improve accuracy and stability. Resistors R_1 and R_2 should be positioned close to the FB pin.

Feed-Forward Capacitor Selection

A small capacitor (C_4 in Figure 4) in parallel with resistor R_1 is required to provide the specified load and line regulation. The suggested value of this capacitor is 27pF for R_1 = 187kΩ. An NPO type capacitor is recommended.

Nonadjustable Version FB Pin Connection

The fixed output versions of the ISL91108 does not require external resistors or a capacitor on the FB pin. Simply connect VOUT to FB, as shown in Figure 5.

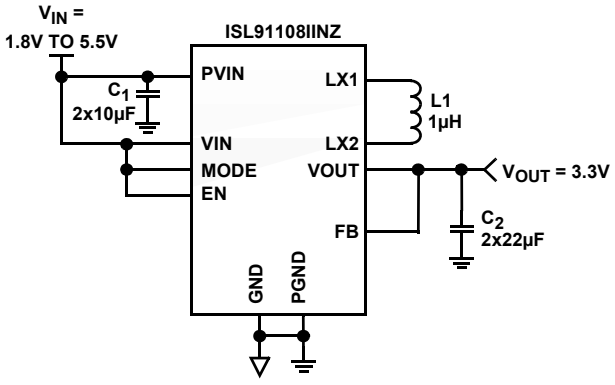


FIGURE 5. TYPICAL ISL91108IINZ APPLICATION

Inductor Selection

An inductor with high frequency core material (e.g., ferrite core) should be used to minimize core losses and provide good efficiency. The inductor must be able to handle the peak switching currents without saturating.

A 1µH inductor with ≥4.0A saturation current rating is recommended. Select an inductor with low DCR to provide good efficiency. In applications where radiated noise must be minimized, a toroidal or shielded inductor can be used.

TABLE 1. INDUCTOR VENDOR INFORMATION

MANUFACTURER	SERIES	DIMENSION (mm)	WEBSITE
Toko	1277AS-H-1R0M	3.2x2.5x1.2	www.toko.com
	FDSD0312-H-1R0M	3.2x3.0x1.2	
Coilcraft	XFL4020-102ME	4.0x4.0x2.1	www.coilcraft.com

PVIN and V_{OUT} Capacitor Selection

The input and output capacitors should be ceramic X5R type with low ESL and ESR. The recommended input capacitor value is 2x 10µF. The recommended V_{OUT} capacitor value is 2x22µF.

TABLE 2. CAPACITOR VENDOR INFORMATION

MANUFACTURER	SERIES	WEBSITE
AVX	X5R	www.avx.com
Murata	X5R	www.murata.com
Taiyo Yuden	X5R	www.t-yuden.com
TDK	X5R	www.tdk.com

Recommended PCB Layout

Correct PCB layout is critical for proper operation of the ISL91108. The input and output capacitors should be positioned as closely to the IC as possible. The ground connections of the input and output capacitors should be kept as short as possible and should be on the component layer to avoid problems that are caused by high switching currents flowing through PCB vias.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
November 12, 2014	FN8448.1	-2nd paragraph: Changed From "This device is capable of delivering up to 2.7A output current (PVIN = 3V, VOUT = 3.3V)...," to “This device is capable of delivering up to 2.7A burst current (PVIN = 3V, VOUT = 3.3V) ... -Features section (bullet point #4) : changed from Output current: up to 1.5A (PVIN = 3V, VOUT = 3.3V) to “Output current: Up to 1.6A DC (PVIN = 2.8V, VOUT = 3.3V)” -Updated Load Current (I_{OUT}) Range (DC) spec under “Recommended Operating Conditions” on page 4 from “0A to 1.5A” to “0A to 1.6A”. -Figures 1, 4 and 5: Removed the text "UP TO 2.7A" that appears next to the VOUT pin
November 6, 2013	FN8448.0	Initial Release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

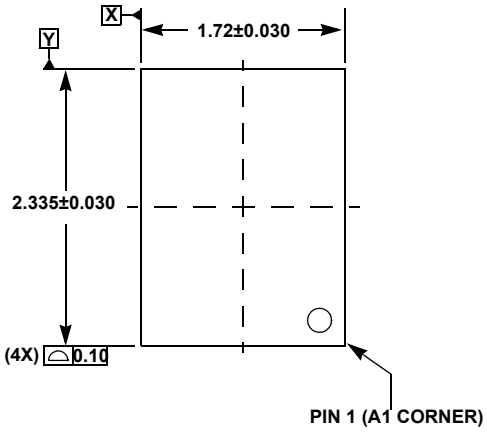
Reliability reports are also available from our website at www.intersil.com/support

Package Outline Drawing

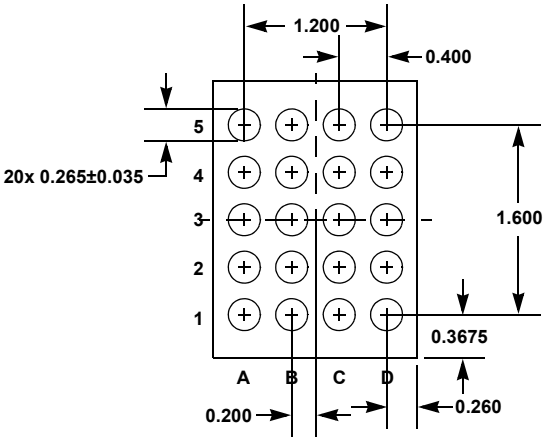
W4x5.20F

20 BALL WAFER LEVEL CHIP SCALE PACKAGE (WLCSP 0.4mm PITCH)

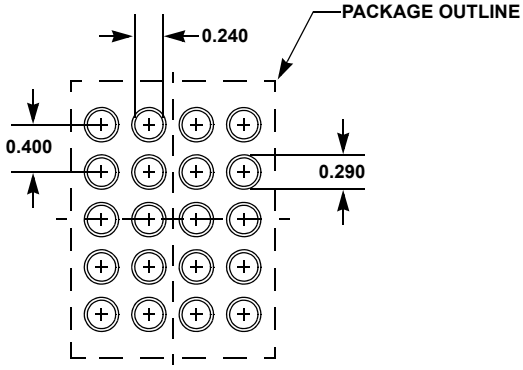
Rev 0, 5/13



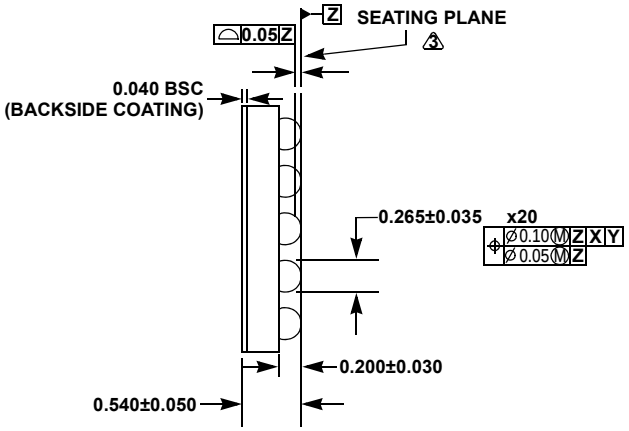
TOP VIEW



BOTTOM VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW

NOTES:

1. Dimensions and tolerance per ASME Y 14.5M - 1994.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z .
3. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
4. Bump position designation per JESD 95-1, SPP-010.
5. There shall be a minimum clearance of 0.10mm between the edge of the bump and the body edge.