10.3125 Gb/s Retiming Dual-Channel Transceiver

ISL37231

The ISL37231 is an advanced dual-channel, dual-simplex retimer for active copper cable applications. Endowed with sophisticated functions, such as media optimized (PCB or Cable) and adaptive equalization, de-emphasis, and signal retiming, this IC fortifies sensitive links that break with lesser retiming solutions. The device contains high performance mixed signal processing technology to provide a maximally robust signal integrity solution for datacenter and consumer applications. Such processing includes up to 25dB of media-optimized equalization and versatile retiming capabilities to reset link jitter budgets.

The ISL37231 provides this high level of performance while significantly reducing power consumption relative to other active cable solutions. At well below 500mW, the operating power is the lowest in class, and a sleep mode function can be invoked to reduce the power to a miniscule 3mW.

To facilitate ease of system integration, the ISL37231 provides advanced diagnostic capabilities in the form of loopback and high-resolution on-chip eye monitor functions, both accessed via a UART interface.

The ISL37231 is optimized to work in conjunction with the ISL80083 power management IC, however, it will also operate with appropriate discrete components (voltage regulators and a 33Mhz crystal oscillator).

Features

- Industry's lowest power and highest performance 10.3125Gbps active cable solution for STP and twin-axial cables
- Supports 64b/66b encoding
- Fully retimed low jitter outputs
- Up to 16.5dB of adjustable (or adaptive) receiver-side equalization
- 9dB output de-emphasis
- Supports independent SSC on each channel
- On-chip microcontroller and eye monitor
- Multiple loopback modes
- Low power (<420mW) operation with 3mW sleep mode
- Ultra-small 5mmx5mm aQFN package

Applications

- Thunderbolt™ active cables
- Proprietary high-speed active cable assemblies

Benefits

- Thinner gauge cable
- Extends cable reach
- Improved BER

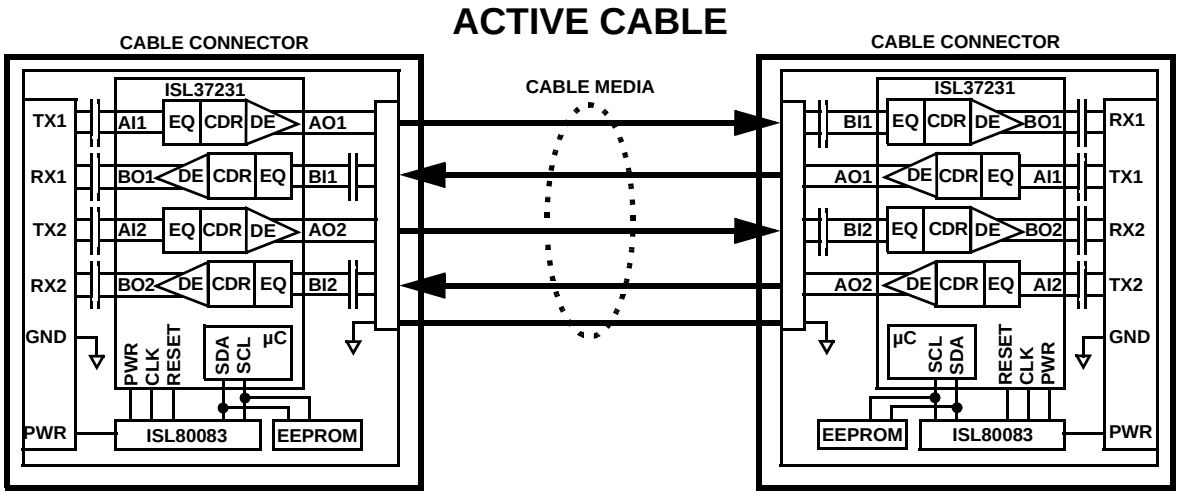


FIGURE 1. TYPICAL APPLICATION

Ordering Information

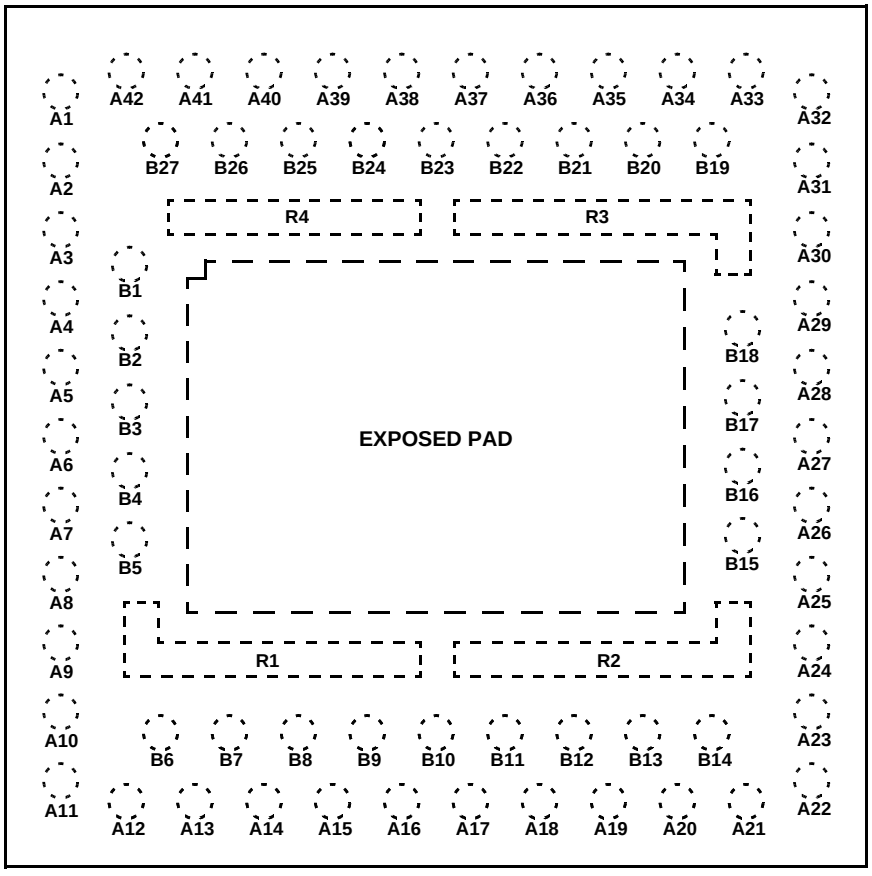
PART NUMBER (Notes 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL37231DRAZ-TS (Note 1)	ISL372 31DRAZ	0 to +85	69 Ld High Density Array (aQFN) package (7” 100 pcs.)	C69.5x5B
ISL37231DRAZ-T7 (Note 1)	ISL372 31DRAZ	0 to +85	69 Ld High Density Array (aQFN) package (7” 1k pcs.)	C69.5x5B
ISL37231DRAZ	ISL372 31DRAZ	0 to +85	69 Ld High Density Array (aQFN) package	C69.5x5B

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL37231. For more information on MSL please see techbrief TB363.

Pin Configuration

ISL37231
(69 LD aQFN)
TOP VIEW



Pin Functions and Definitions

PIN NAME	PIN NUMBER	DIRECTION	DESCRIPTION
AIN1[P,N]	A1, A42	Input	High-speed differential input for on-ramp (device to cable) Channel 1, CML. The use of series 220nF, low ESL/ESR, MLCC capacitors with at least 8GHz frequency response is recommended.
GND	A2, A10, A13, A16, A17, A20, A23, A30, A31, A34, A37, A38, A41, B4, B6, B7, B16, B19, B20, B26, B27, Exposed Pad		Ground. For proper electrical and thermal performance, each of these pads must be connected to the PCB ground plane. For the exposed pad, 3x5 or 4x5 via pattern is recommended, assuming 0.004" diameter vias.
XTAL[P,N]	A3, B1	Input	External 33MHz crystal oscillator input/output. An external 33MHz clock source (1V CMOS logic level) can optionally be connected XTALP, in which case XTALN must be left floating. A differential 33MHz clock source (1V CMOS logic levels) can be input on XTALP and XTALN if OSCMODE (pin A29) is pulled high to 1.8V.
AUTX1	A4	Output	Auxiliary UART output 1. AUTX1 can be configured via the on-chip microcontroller as either a UART output or a GPIO pin, with either 1.8V push-pull or 3.3V tolerant open drain voltage levels.
AURX1	A5	Input	Auxiliary UART data input 1, 1.8V powered CMOS logic tolerant to 3.3V.
EEWE	A6	Output	EEPROM write enable open drain output. Externally pulled high to 3.3V via a ≥5kΩ resistor. Pulled low when the ISL37231 writes to an external EEPROM device via the I^2C serial interface.
CFIG2	A7	Output	Thunderbolt CONFIG2 indicator output. 1.8V powered CMOS logic. Pulled high after the ISL37231 is powered up and stable to indicate to a Thunderbolt controller that a Thunderbolt cable has been plugged in.
OSCEN	A8		Oscillator enable. CMOS logic, 1.8V. Used as a deep-sleep state indicator. During normal operation, OSCEN is pulled high. When entering deep-sleep mode, OSCEN is pulled low. Output is not pulled high again until transitions are detected on the URX input pin (A27).
AUTX2	A9	Output	Auxiliary UART output 2. AUTX2 can be configured via the on-chip microcontroller as either a UART output or a GPIO pin, with either 1.8V push-pull or 3.3V tolerant open drain voltage levels.
BIN1[P,N]	A11, A12	Input	High-speed differential input for off-ramp (cable to device) Channel 1, CML. The use of series 220nF, low ESL/ESR, MLCC capacitors with at least 8GHz frequency response is recommended. (Note 4)
BOUT1[N,P]	A14, A15	Output	High-speed differential output for off-ramp (cable to device) Channel 1, CML. The use of series 220nF, low ESL/ESR, MLCC capacitors with at least 8GHz frequency response is recommended.
BOUT2[P,N]	A18, A19	Output	High-speed differential output for off-ramp (cable to device) Channel 2, CML. The use of series 220nF, low ESL/ESR, MLCC capacitors with at least 8GHz frequency response is recommended.
BIN2[N,P]	A21, A22	Input	High-speed differential input for off-ramp (cable to device) Channel 2, CML. The use of series 220nF, low ESL/ESR, MLCC capacitors with at least 8GHz frequency response is recommended. (Note 4)
LSEN	A24	Output	Level shift enable output. 1.8V powered CMOS logic. Pulled high to indicate an operational UART interface to the ISL37231. When pulled low, UTX (pin A28) is set to a high impedance state.
SCL	A25		Serial interface clock. Open drain output, externally pulled high to 3.3V via a ≥5kΩ resistor. I^2C clock, recommended clock speed is 400kHz.
SDA	A26		Serial interface data. Open drain output, externally pulled high to 3.3V via a ≥5kΩ resistor. Bi-directional data from/to I^2C bus.
URX	A27	Input	UART data input. 1.8V powered CMOS logic, but URX is 3.3V tolerant. When the ISL37231 is in “Sleep” mode, a H to L transition on URX causes the ISL37231 to drive OSCEN high.
UTX	A28	Output	UART data tri-statable output. 1.8V powered CMOS logic. UTX is set to a high impedance state when the UART interface is not in use and LSEN is pulled low. If UTX interfaces to a 3.3V powered UART, then a level translator IC may be needed.
OSCMODE	A29	Input	Oscillator mode. CMOS logic, 1.8V, internally pulled low. When OSCMODE is low, the XTALP and XTALN input pins (A3 and B1) are configured for operation with an external crystal or with an external single-ended clock on XTALP (XTALN must be left floating in this latter case). When OSCMODE is pulled high, the XTALP and XTALN input pins are configured for operation with an external differential clock.

Pin Functions and Definitions (Continued)

PIN NAME	PIN NUMBER	DIRECTION	DESCRIPTION
AIN2[P,N]	A32, A33	Input	High-speed differential input for on-ramp (PCB to cable) Channel 2, CML. The use of series 220nF, low ESL/ESR, MLCC capacitors with at least 8GHz frequency response is recommended.
AOUT2[N,P]	A35, A36	Output	High-speed differential output for on-ramp (PCB to cable) Channel 2, CML. (Note 4)
AOUT1[P,N]	A39, A40	Output	High-speed differential output for on-ramp (PCB to cable) Channel 1, CML. (Note 4)
AVDD1	B2, R1, R2, R3, R4 (Note 5)		1.0V analog supply voltage. The use of parallel 100pF and 10nF decoupling capacitors to ground is recommended for each of these pins/rails for broad high-frequency noise suppression.
AVDD18	B3		1.8V analog supply voltage. The use of parallel 100pF and 10nF decoupling capacitors to ground is recommended for this pin for broad high-frequency noise suppression.
NC	B4, B6, B7, B13, B14, B19, B20, B26, B27		No connection. Do not connect to these pins.
DVDD	B5, B15		1.0V digital supply voltage. The use of parallel 100pF and 10nF decoupling capacitors to ground is recommended for these pins for broad high-frequency noise suppression.
VDDPLLB1	B8		1.8V analog supply voltage for off-ramp Channel 1.
REFRETB1	B9		VDDPLL reference return path for off-ramp Channel 1.
REXT2	B10		External reference resistor connection. Recommended value of 1.18kΩ.
REFRETB2	B11		VDDPLL reference return path for off-ramp Channel 2.
VDDPLLB2	B12		1.8V analog supply voltage for off-ramp Channel 2.
AURX2	B16	Input	Auxiliary UART input 2. CMOS logic, 1.8V (tolerant to 3.3V).
VDDPST	B17		1.8V digital supply voltage. The use of parallel 100pF and 10nF decoupling capacitors to ground is recommended for each of these pins for broad high-frequency noise suppression.
$\overline{\text{RESET}}$	B18	Input	CMOS logic input. 1.8V powered. Resets all internal registers and memory when pulled low.
VDDPLLA2	B21		1.8V analog supply voltage for on-ramp Channel 2.
REFRETA2	B22		VDDPLL reference return path for on-ramp Channel 2.
REXT1	B23		External reference resistor connection. Recommended value of 1.18kΩ.
REFRETA1	B24		VDDPLL reference return path for on-ramp Channel 1.
VDDPLLA1	B25		1.8V analog supply voltage for on-ramp Channel 1.

NOTES:

4. Series coupling capacitors are required at one end of the cable. For best results, place the capacitors at the receiver end of the cable. The use of 220nF low ESL/ESR MLCC capacitors with at least 8GHz frequency response is recommended.
5. Each power bar is independent, so they must all connect to the same 1V supply for proper circuit operation.

Absolute Maximum Ratings

Supply Voltage (V_{DD} to GND, 1.0V Rails) 1.1V
Supply Voltage (V_{DD} to GND, 1.8V Rails) 1.98V
1V Pin Input Voltage (AIN, BIN, XTALP) 1.1V
1.8V Pin Input Voltage (all non 3.3V tolerant logic inputs) . . . . V_{DD} + 0.2V
3.3V Tolerant I/O Pin Voltage (EEWE, SCLK, SDA, URX, AUTX, AURX, $\overline{RESET}$) 3.6V
ESD Ratings
Human Body Model (All Pins) 1.25kV
Charged Device Model (All Pins) 1.0kV
Machine Model (All Pins) 200V
Latch-up (per JEDEC JESD78, Level 2, Class A) . . . . . +85°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
69 Ld aQFN Package (Notes 6, 7)	31.8	2.5

Operating Ambient Temperature Range . . . . . 0°C to +85°C
Storage Ambient Temperature Range . . . . . -55°C to +150°C
Maximum Junction Temperature . . . . . +125°C
Pb-Free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

6. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
7. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Operating Conditions

Boldface limits apply across the operating temperature range, 0°C to +85°C.

PARAMETER	SYMBOL	CONDITION	MIN (Note 12)	TYP	MAX (Note 12)	UNITS
1.0V Supply Voltage	AVDD1, DVDD		**0.95**	1.0	**1.05**	V
1.8V Supply Voltage	AVDD18, VDDPLL, VDDPST		**1.71**	1.8	**1.89**	V
Operating Ambient Temperature	T_A		**0**	25	**85**	°C
Baud Rate		NRZ data applied to any channel	**9.95**	10.3125	**10.4**	Gbps

Logic I/O Specifications

Boldface limits apply across the operating temperature range, 0°C to +85°C.

PARAMETER	SYMBOL	CONDITION	MIN (Note 12)	TYP	MAX (Note 12)	UNITS
Input Leakage Current	I_{LEAK}	Pins URX, AURX1, AURX2, $\overline{RESET}$	**-1**	0.1	**1**	µA
Pull-down Resistor Current	$I_{PULLDOWN}$	OSCMODE. $V_{IN} = V_{DD18}$		103		µA
Input HIGH Voltage	V_{IH}	Pins URX, AURX1, AURX2, $\overline{RESET}$, OSCMODE	**2**		**3.4**	V
Input LOW Voltage	V_{IL}	Pins URX, AURX1, AURX2, $\overline{RESET}$, OSCMODE	**0**		**0.7**	V
Output LOW Voltage	V_{OL}	I_{OL} = 2mA	**0**		**0.4**	V
Output High Voltage	V_{OH}	I_{OH} = 2mA	**1.4**		**V_{DD18}**	V

Electrical Characteristics T_A = +25°C, V_{DD1} = 1.0V, V_{DD18} = 1.8V, unless otherwise noted

PARAMETERS	SYMBOL	CONDITION	MIN (Note 12)	TYP	MAX (Note 12)	UNITS	NOTES
1.0V Supply Current (Combination of all 1V Supplies)	I_{DD1}	Both lanes active, after equalizer has trained and is static, no eye monitors enabled		430	510	mA	
		No lanes active, but microcontroller awake		85	150	mA	
		Sleep Mode		4		mA	8
1.8V Supply Current (Combination of all 1.8V Supplies)	I_{DD18}	Both lanes active, after equalizer has trained and is static, no eye monitors enabled		25	55	mA	
		No lanes active, but microcontroller awake		9	20	mA	
		Sleep Mode		330		µA	8
Return Loss Limit (Differential)	$S_{DD}11$ $S_{DD}22$	0.05GHz to 2GHz		-10		dB	9
		2GHz to 5.2GHz		-6		dB	9
		5.2GHz to 7GHz		-5		dB	9
Return Loss Limit (Common Mode)	$S_{CC}11$ $S_{CC}22$	10MHz to 5GHz		-5		dB	9
Return Loss Limit (Diff. to Com. Conversion)	$S_{CD}11$ $S_{CD}22$	10MHz to 5GHz		-20		dB	9
Input Equalization Range		EQ gain at 5GHz compared to DC. Set to minimum gain		6		dB	10
		EQ gain at 5GHz compared to DC. Set to maximum gain		16.5		dB	10
Input Equalization Increment		10 steps covering the Equalization range		1.5		dB	
Output De-Emphasis Level Range		Off-ramp channels optimized for PCB dielectric loss. On-ramp channels optimized for cable skin loss. Minimum setting		0		dB	
		Off-ramp channels optimized for PCB dielectric loss. On-ramp channels optimized for cable skin loss. Maximum setting		9		dB	
De-Emphasis Increment				1		dB	
Number of De-Emphasis Taps				3			11
Output Differential Amplitude Range	V_{OUT}	Minimum drive setting		200		mV_{P-P}	
		Maximum drive setting		950		mV_{P-P}	
Output Differential Amplitude Increment		15 Uniform Steps		50		mV_{P-P}	
Output Transition Time	t_r, t_f	20% to 80%		45		ps	
Jitter Transfer Function Bandwidth				5		MHz	
Total Output Jitter		1E-13 BER; PRBS-31; no low frequency input periodic jitter		0.3		UI_{P-P}	
SSC Down Spreading Amplitude Tolerance				0.5		%	
SSC Modulation Rate Tolerance				33-37		kHz	

NOTES:

8. The specified Sleep Mode currents can only be achieved when the ISL37231 is used in conjunction with the ISL80083 power management IC.
9. Measured with a Vector Network Analyzer with 100Ω -diff impedance and the ISL37231 input/output impedance at setting 0x07 (i.e. 100Ω-diff).
10. The equalization response includes all effects starting from the IC input pins up to the output of the equalization stage.
11. Three de-emphasis taps composed of: 1 pre-cursor + main + 1 post-cursor.
12. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Operation

The ISL37231 is a robust signal conditioner that ensures maximum performance across a variety of time-varying and unpredictable environments. Endowed with functions, such as transmit and receive equalization, signal retiming, and programmable impedance termination, this IC fortifies sensitive links that break with other retiming-based solutions. To facilitate systems analysis, the ISL37231 additionally provides visibility of link conditions by way of loopback modes, PRBS generators with error counters, and an on-chip eye-monitor.

Equalization

The ISL37231 equalizes each received signal with a highly adjustable equalizer.

Each received signal is equalized with a five stage continuous-time linear filter that can be optimized for either copper cable skin loss or dielectric loss. The amount of equalization is selectable between 0dB and 16.5dB of compensation in increments of 1.5dB. Because the filter is phase/jitter-optimized, the maximum 16.5dB compensation level yields very low jitter for its targeted 2m (~20dB) 34AWG cable length.

In addition to supporting a wide variety of programmable settings, all channel equalizers can be trained upon power up to minimize jitter. The training of all channels is completed within 2.5ms of receiving valid data on the input ports after power up.

Retiming

To provide maximum system robustness, the ISL37231 retimes each of the four data paths in the device prior to output. With independent PLLs for each channel, the device can operate each channel with asynchronous baud rates thereby permitting a high degree of system flexibility. Examples where such flexibility is crucial include independent or staggered SSC rates across different channels and asymmetric transmission where up and down-stream channels operate at different baud rates.

Each retimer has high input jitter tolerance and can output less than 0.3UI of total jitter (provided the inherent RJ of the test equipment is de-embedded and no input low-frequency periodic jitter is present).

Output De-Emphasis

The drive level output of any channel is adjustable from 200 to 950mVppd rail-to-rail (170 to 807.5mVppd eye height) in 16 equal increments.

Each driver supports output equalization with one tap of pre-cursor and one tap of post-cursor de-emphasis. The gains on the pre and post-cursor taps are adjustable between 0 and -1 relative to the main tap in increments of 1/128. The output amplitude and de-emphasis for each channel can be independently programmed to accommodate routing variation between lanes.

Loopback

To facilitate system diagnostics, a loopback mode is available for each signal direction. In particular, for each lane, two loopback paths are provided:

- Near-End/PCB Loopback: The received on-ramp signal is directed back into the off-ramp output driver. This includes PCB equalization, limiting, retiming, and PCB de-emphasis.
- Far-End/Cable Loopback: The received off-ramp signal is directed back into the on-ramp output driver. This includes cable equalization, limiting, retiming, and cable de-emphasis.

Eye Monitor

For accurate and detailed analysis of signal integrity, each channel in the ISL37231 can provide an on-chip eye-diagram of its respective equalizing filter output. This eye diagram can be used to evaluate jitter and eye height at the input of the retime circuit's slicer.

The eye monitor (in conjunction with the on-chip microcontroller) generates up to a 50 pixel x 50 pixel resolution eye-diagram (i.e. down to 0.02 UI resolution in the time domain and 12mV resolution in the voltage domain) that can be read over the UART interface. The output eye diagram represents an estimated probability density function for the equalized signal under investigation.

Besides providing a full eye-diagram, the Eye-Monitor can also be directed to output only the temporal and/or voltage eye-opening for a more concise signal fidelity assessment (i.e., jitter and eye height, respectively).

Polarity Inversion

To accommodate uncertainty in signal polarity (as may be associated with differential cable receive pairs), each channel can be independently programmed to invert its polarity.

On-Chip Microcontroller

An internal microcontroller is used to manage the operation of the ISL37231.

The microcontroller communicates with the system host over a UART interface. Because the ISL37231 UART interface operates at 1.8V, an interfacing IC (such as the ISL80083) is required for applications needing 3.3V levels and tri-state (push/pull/no-load) operation.

The microcontroller also includes an I^2C interface where the ISL37231 serves as the master. This I^2C bus is used to:

- Instruct a power-regulator providing the 1.0V supply that the system is entering sleep mode and power can be removed from non-critical 1.0V rails for maximum power savings during sleep state.
- Load firmware from an external EEPROM.

About Q:ACTIVE® Technology

Intersil has long realized that to enable the complex server clusters of next generation data centers, it is critical to manage the signal integrity issues of electrical interconnects. To address this, Intersil has developed its groundbreaking Q:ACTIVE® product line. By integrating its analog ICs inside cabling interconnects, Intersil is able to achieve unsurpassed improvements in reach, power consumption, latency, and cable gauge size as well as increased airflow in tomorrow's data centers. This new technology transforms passive cabling into intelligent "roadways" that yield lower operating expenses and capital expenditures for the expanding datacenter.

Intersil Lane Extenders allow greater reach over existing cabling while reducing the need for thicker cables. This significantly reduces cable weight and clutter, increases airflow, and improves power consumption.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
January 17, 2013	FN8266.1	Changed TYP values for "I_{DD1}" on page 6.
December 19, 2012	FN8266.0	Initial release

About Intersil

Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the fastest growing markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil or to find out how to become a member of our winning team, visit our website and career page at www.intersil.com.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective product information page. Also, please check the product information page to ensure that you have the most updated datasheet: ISL37231

To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

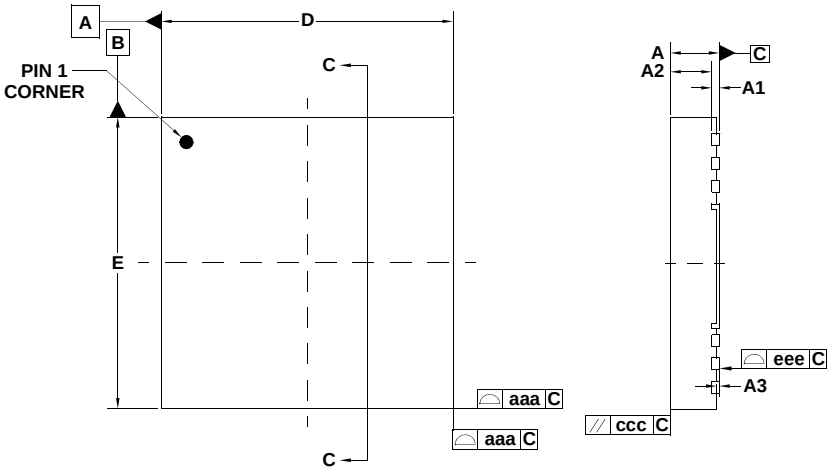
Reliability reports are available from our website at: http://rel.intersil.com/reports/search.php

Package Outline Drawing

C69.5x5B

69 LEAD aQFN 5X5 PACKAGE WITH 0.40 PITCH

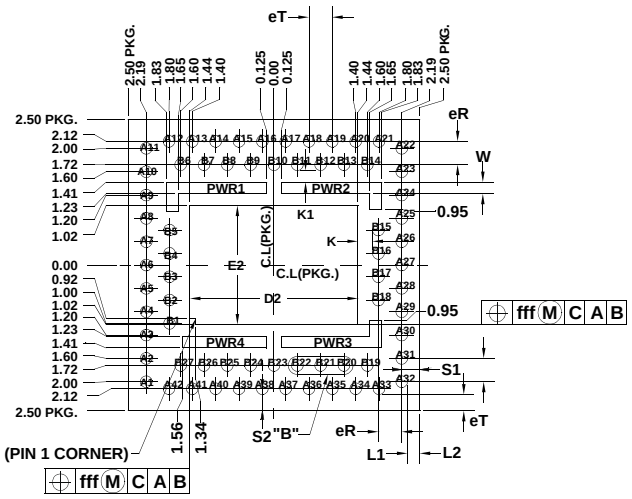
Rev 1, 12/12



TOP VIEW

SECTION C-C

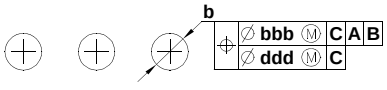
SYMBOL	MILLIMETER			INCH		
	MIN	NOM.	MAX	MIN	NOM.	MAX
A	-	-	0.85	-	-	0.033
A3	0.020	0.050	0.080	0.001	0.002	0.003
A2	0.640	0.675	0.710	0.025	0.027	0.028
A1	0.120	0.130	0.140	0.005	0.005	0.006
b	0.170	0.200	0.230	0.007	0.008	0.009
D	4.900	5.000	5.100	0.193	0.197	0.201
D2	2.780	2.880	2.980	0.109	0.113	0.117
E	4.900	5.000	5.100	0.193	0.197	0.201
E2	1.940	2.040	2.140	0.076	0.080	0.084
eT		0.400			0.016	
eR		0.400			0.016	
K	0.200	0.250	0.300	0.008	0.010	0.012
K1	0.160	0.210	0.260	0.006	0.008	0.010
L1	0.160	0.210	0.260	0.006	0.008	0.010
L2	0.230	0.280	0.330	0.009	0.011	0.013
S1	0.260	0.310	0.360	0.010	0.012	0.014
S2	0.330	0.380	0.430	0.013	0.015	0.017
W	0.150	0.180	0.210	0.006	0.007	0.008
TOLERANCES OF FORM AND POSITION						
aaa		0.100			0.004	
bbb		0.100			0.004	
ddd		0.050			0.002	
ccc		0.100			0.004	
eee		0.100			0.004	
fff		0.100			0.004	



BOTTOM VIEW

NOTE:

1. Controlling dimension: mm



DETAIL "B" (3:1)(69X)