Evaluating the ADA4255 Zero Drift, High Voltage, Programmable Gain Instrumentation Amplifier with Charge Pump

FEATURES

- Enables quick breadboarding and prototyping
- Edge-mounted SMA connector provisions
- Easy connection to test equipment and other circuits

EVALUATION BOARD CONTENTS

- ADA4255CP-EBZ evaluation board

EQUIPMENT NEEDED

- SDP-S board
- Cables (SMA input to evaluation board)
- Standard USB A that connects to a mini-B USB cable
- PC running the Windows 7 and up operating system

DOCUMENTS NEEDED

- ADA4255 data sheet

SOFTWARE NEEDED

- Analog Devices Analysis | Control | Evaluation (ACE) Software

GENERAL DESCRIPTION

The ADA4255CP-EBZ evaluation board is designed to help users evaluate the ADA4255 in its 28-lead lead frame chip scale package (LFCSP). Figure 1 and Figure 2 show the front side and back side of the ADP4255CP-EBZ evaluation board with the 28-lead LFCSP.

The ADA4255CP-EBZ is a 4-layer printed circuit board (PCB). This evaluation board accepts Subminiature Version A (SMA) edge-mounted connectors on the inputs and outputs to efficiently connect to test equipment and/or other circuitry.

The ADA4255CP-EBZ requires the following three supply domains:

- A charge pump voltage, VDDCP, of typically 5 V that generates the high voltage supply domain, which includes VDDH and VSSH, and that are typically +22.3 V and −21.7 V, respectively.
- An analog supply domain, AVDD, of typically 5 V.
- A digital supply domain, DVDD, of typically 3.3 V.

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REVISION HISTORY

7/2021—Revision 0: Initial Version

EVALUATION BOARD PHOTOGRAPHS

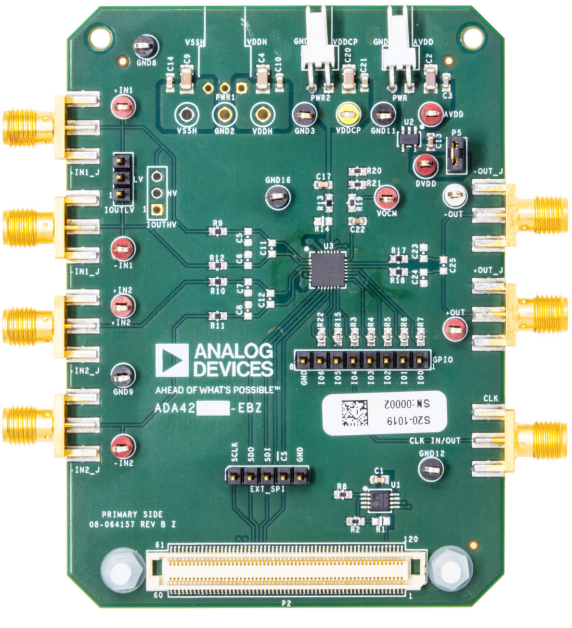

Figure 1. ADA4255CP-EBZ Front

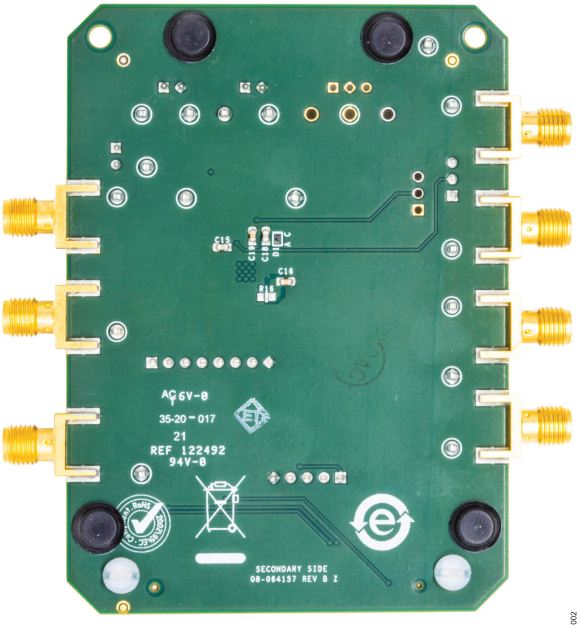

Figure 2. ADA4255CP-EBZ Bottom

EVALUATION BOARD HARDWARE

DEVICE DESCRIPTION

The ADA4255 is a precision programmable gain instrumentation amplifier (PGIA) with integrated bipolar charge pumps. With its integrated charge pumps, the ADA4255 internally produces the high voltage bipolar supplies needed to achieve a wide input voltage range (38 V typical with VDDCP = 5 V) without lowering input impedance. The charge pump topology of the ADA4255 allows channels to be isolated with only low voltage components, reducing complexity, size, and implementation time in industrial and process control systems.

The zero drift PGIA topology of the ADA4255 self calibrates dc errors and lower frequency 1/f noise, achieving excellent dc precision over the entire specified temperature range. The combination of 36 precision gains ranging from 1/16 V/V to 176 V/V within the ADA4255 and high voltage, high impedance inputs allow a wide range of inputs to be scaled to the range of the analog-to-digital converter (ADC).

POWER SUPPLIES

The ADA4255CP-EBZ requires the following three supplies (see Figure 3):

- The AVDD and AVSS supply for the output amplifier. This supply must be provided externally.
- The VDDCP supply for creating the internal VDDH and VSSH supplies. This supply must be provided externally.
- The DVDD supply for the digital supply. This supply is generated on the ADA4255CP-EBZ by using the ADP150 as a 3.3 V voltage regulator.

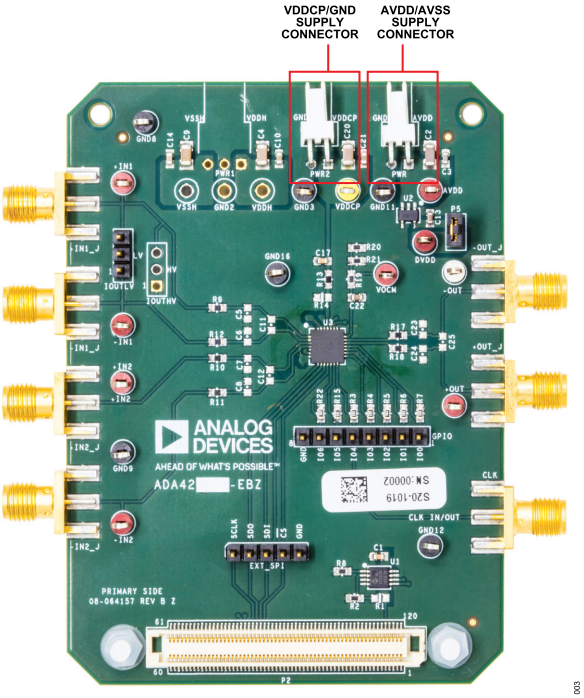

Figure 3. Power Supply Connections

ANALOG INPUTS AND OUTPUTS

The ADA4255CP-EBZ has four inputs that correspond to the four inputs of the ADA4255 input multiplexer (see Figure 4). The ADA4255CP-EBZ also has two outputs corresponding to the fully differential output of the ADA4255.

The output common-mode voltage (VOCM) is set to ½ of the output amplifier supply through a voltage divider. However, the user can control VOCM by connecting an external voltage to the VOCM test point (see Figure 4).

The ADA4255CP-EBZ allows the user to connect the excitation current source output of the ADA4255 to either the +IN1 or −IN1 input through the pin header connector. See Figure 4 for the connection details.

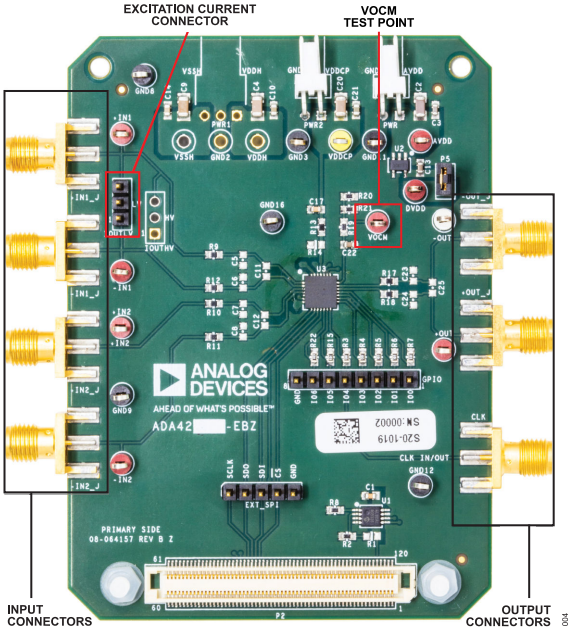

Figure 4. Input and Output SMA Connectors

EVALUATION BOARD HARDWARE

GENERAL-PURPOSE INPUTS AND OUTPUTS (GPIOS)

The ADA4255CP-EBZ allows the user to interact with the various GPIO functions of the ADA4255. The user can set the GPIOx pins as outputs and toggle these pins between high and low. The ADA4255CP-EBZ also allows the user to connect to the GPIO pins through a pin header (see Figure 5).

GPIO4 can be used to either input an external clock or to output the ADA4255 internal clock through the SMA connector. See the ADA4255 data sheet for more information.

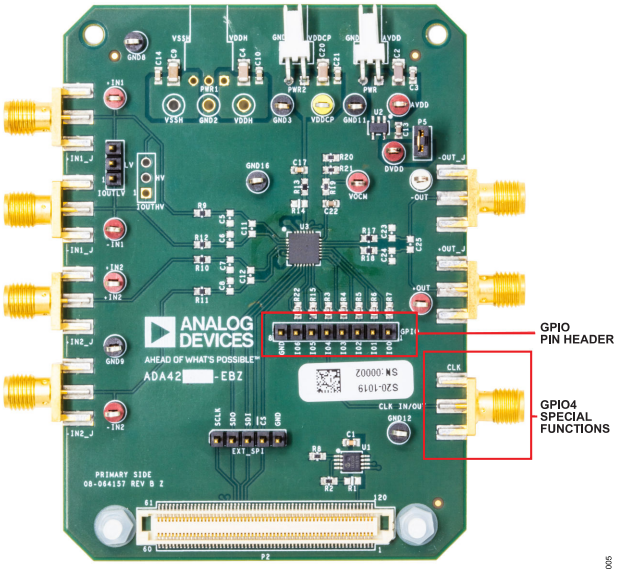

Figure 5. GPIO Connections

EVALUATION BOARD CONTROL

The ADA4255CP-EBZ uses the SDP-S board to communicate with the ACE software. Connect the SDP-S or SDP-B board to the ADA4255CP-EBZ 120-pin connector (see Figure 6). The ADA4255CP-EBZ also allows the user to use serial peripheral interface (SPI) controls through the pin header (SPI).

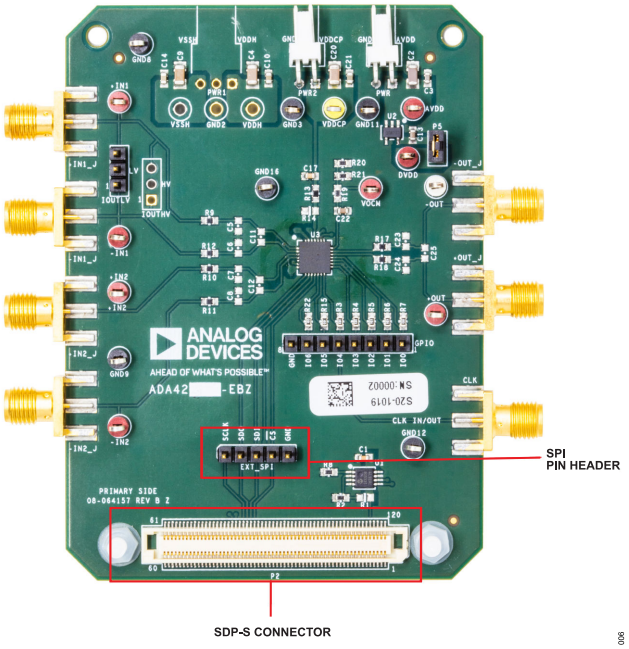

Figure 6. SDP-S Connector and SPI Pin Header Connector

EVALUATION BOARD SOFTWARE

INSTALLATION

The ADA4255CP-EBZ uses the Analog Devices Analysis| Control | Evaluation (ACE) software. ACE is a desktop application that allows user to control and analyze multiple evaluation systems.

The ACE installer loads the necessary system demonstration platform (SDP) drivers and .NET Framework 4 by default. Install the ACE software before connecting the SDP-S board to the USB port of the PC to ensure that the SDP-S board is recognized when the board connects to the PC. To download the ACE software and access the full instructions on how to install and use this software, go to https://www.analog.com/ace.

INITIAL SETUP

To set up the ADA4255CP-EBZ, take the following steps:

1. Connect the ADA4255CP-EBZ to the SDP-S board using the 120-pin header of the SDP board.
2. Connect the SDP-S board to the PC via a USB cable.
3. Power the ADA4255CP-EBZ with 5 V at PWR (AVDD), PWR 1 (VDDCP), and the ground (AVSS) pins.
4. Run the ACE application. The ADA4255CP-EBZ plug-ins appear in the hardware section within the **Start** tab of the ACE software.
5. Double-click on the ADA4255CP-EBZ plug-in to open the board view shown in Figure 7. Ensure that the ADA4255CP-EBZ is connected, which is indicated by the green light next to the **ADA4255 Board** tab.
6. Double-click the ADA4255 chip to access the chip block diagram. This view provides a basic representation of the functionality of the ADA4255CP-EBZ. The main functions are labeled in Figure 8, which is referred to as the block diagram view or the chip view.

QUICK START

When initial setup is complete, take the following three steps to generate an output waveform.

1. Change the **Input Amplifier Gain** to 1.
2. Provide an input sine wave of 1 V p-p at 1 kHz at +IN1 and ground the −IN1 input.
3. Connect the output pins, +OUT and −OUT, to an oscilloscope to check the waveforms. Note that the waveform is superimposed on VOCM, which by default is 2.5 V.

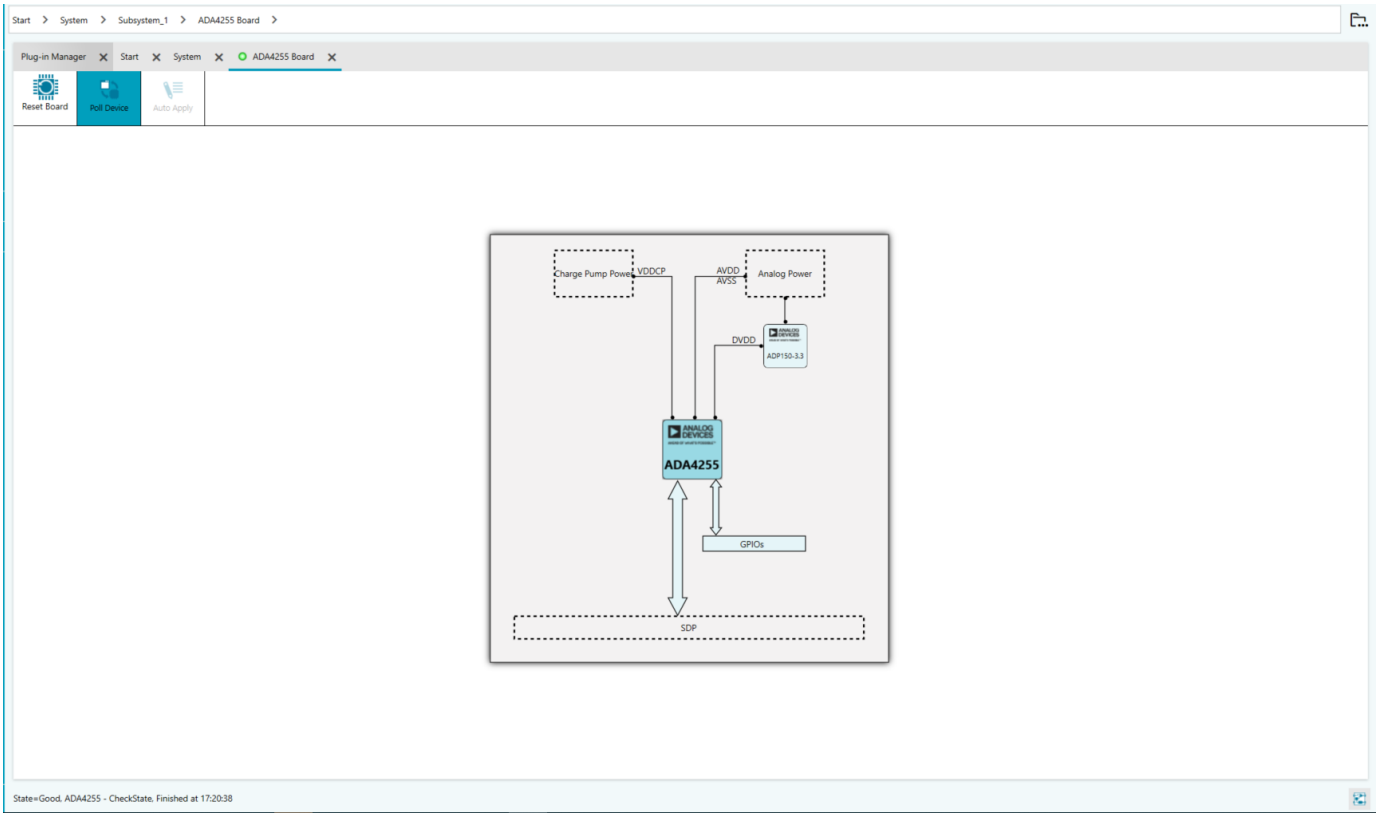

Figure 7. Board View

EVALUATION BOARD SOFTWARE

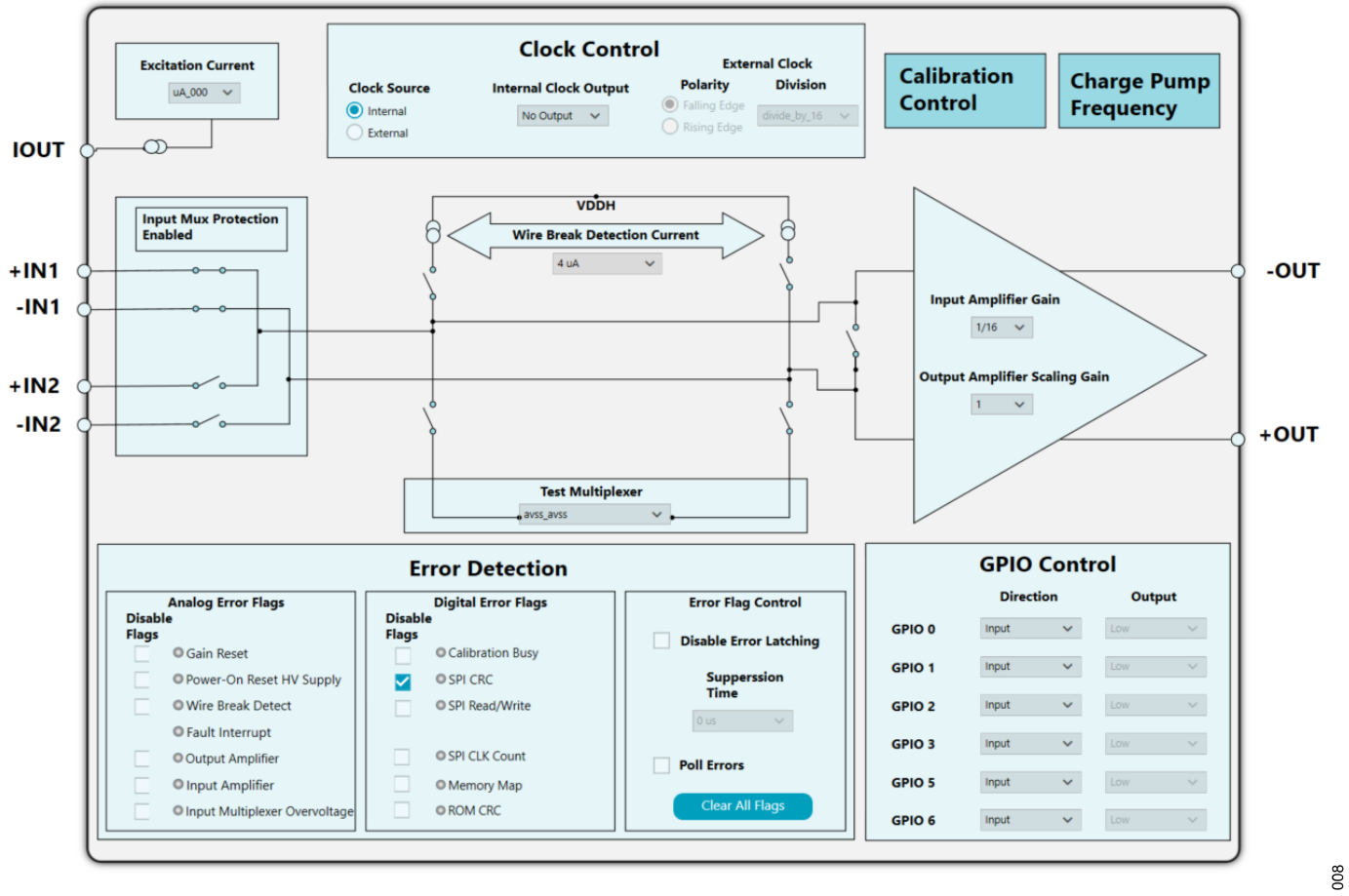

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Figure 8. Chip View

BLOCK DIAGRAM AND DESCRIPTION

The ACE plug-in of the ADA4255 is organized so that the plug-in appears similar to the functional block diagram shown in the data sheet. A full description of each block, register, and its settings is given in the ADA4255 data sheet.

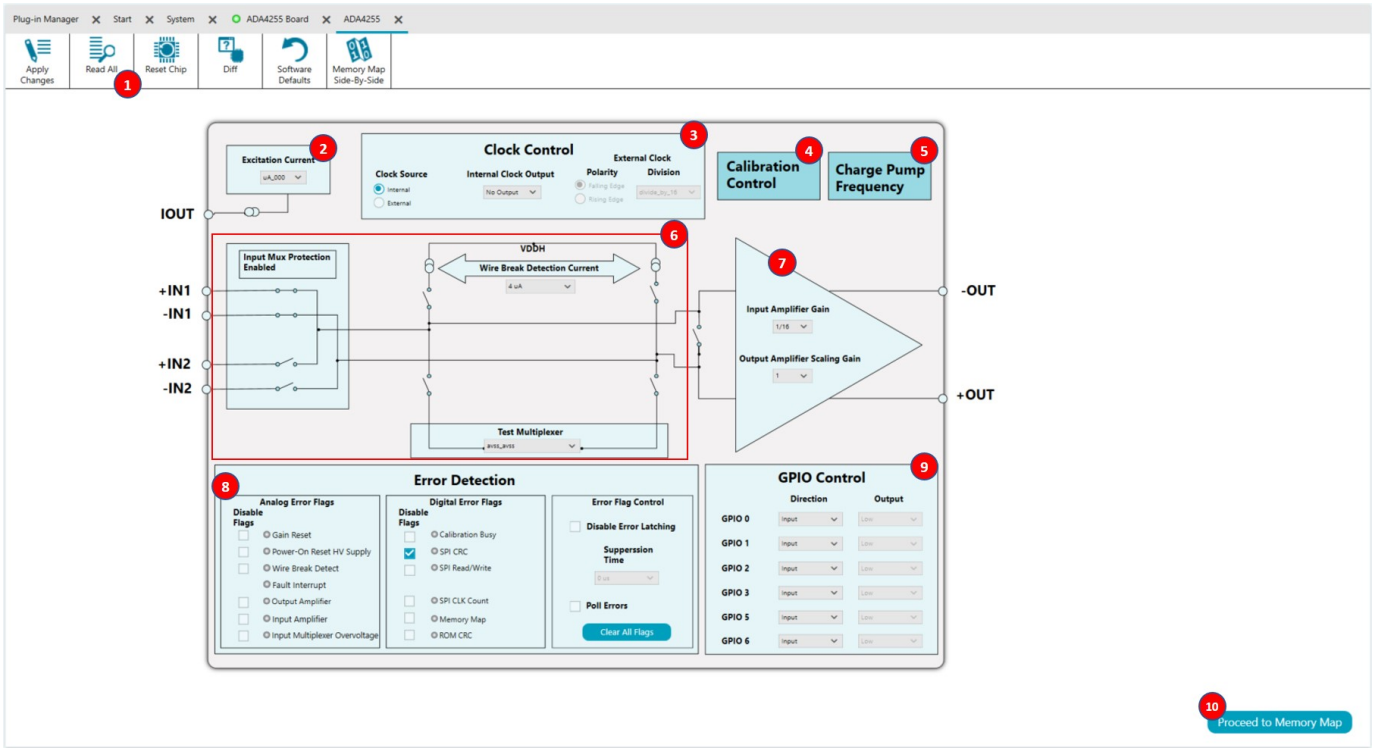

Figure 9. ADA4255 Evaluation Software Main Display

BLOCK DIAGRAM AND DESCRIPTION

Note that the full screen block diagram shown in Figure 9 showcases the full functionality of ADA4255. However, the following describes some of the blocks and their functions as the blocks and functions pertain to the ADA4255CP-EBZ:

1. **Read All** (which is located in the top left of Figure 9) reads all the register values of the ADA4255 and reflects these values in the **Chip View** display and the **Memory Map**. Click **Apply Changes** (which is located in the top left of Figure 9) to ensure that any changes are updated before reading the registers. Clicking **Reset Chip** (Label 1 in Figure 9) writes 0x01 to the software reset register of the ADA4255, which sets the ADA4255 back to the default configuration.
2. The **Excitation Current** (Label 2 in Figure 9) opens a drop-down menu. In this menu, users set the excitation current value for the ADA4255. After a change is made to the **Excitation Current** box, click **Apply Changes** to write the changes to the ADA4255.
3. The **Clock Control** panel (Label 3 in Figure 9) allows the user to either bring out the ADA4255 clock on the GPIO4 or to provide an external clock on the GPIO4. The GPIO4 has an SMA connector for ease of use with the external clock for synchronization purposes. The user can set up the division factor depending on the external clock speed as well as the edge on which the clock synchronizes. After a change is made in the **Clock Control** panel, click **Apply Changes** to write the change to the ADA4255.
4. The **Calibration Control** button (Label 4 in Figure 9) opens the window shown in Figure 10. This window allows the user to configure the calibration of the ADA4255. Set the first bit of the trig_cal register to 1 located in the memory map to trigger a calibration (see Figure 11), and then click **Apply Changes** to write the changes to the ADA4255.
5. The **Charge Pump Frequency** button (Label 5 in Figure 9) opens a window that allows the user to select the frequency of the charge pump. The user can choose from 8 MHz or 16 MHz. After a choice of frequency is made, click **Apply Changes** to write the changes to the ADA4255.

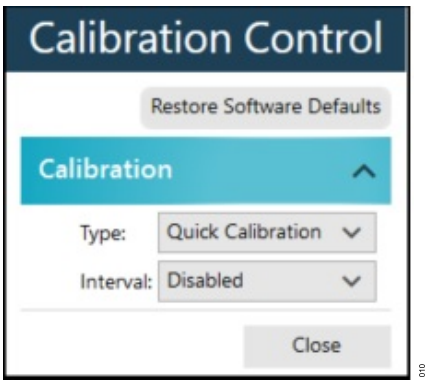

Figure 10. Calibration Settings Window

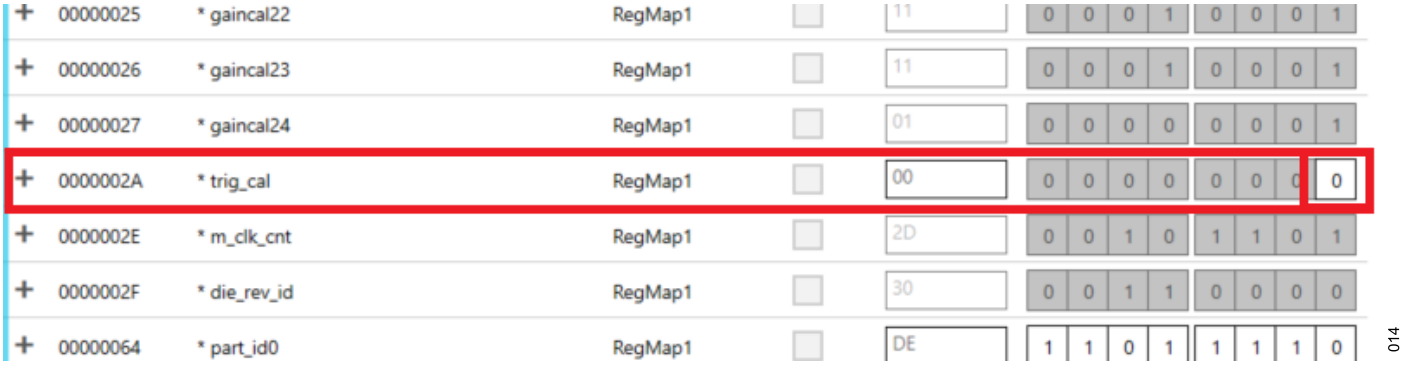

Figure 11. Trig_cal Memory Map

BLOCK DIAGRAM AND DESCRIPTION

DESCRIPTION OF THE SOFTWARE PANEL

The components of the ADA4255 evaluation software user panel shown in Figure 9 include the following:

1. The multiplexer control section (Label 6 in Figure 9) allows users to control all of the switches available in the ADA4255 input multiplexer. This section also sets the wire break detection currents, the wire break switches, and the test multiplexer. After a change is made within the multiplexer control section, click **Apply Changes** to write the changes to the ADA4255.
2. The gain control area (Label 7 in Figure 9) allows users to select the gain of the ADA4255 as well as the scaling gains, 1 V/V, 1.25 V/V, or 1.375 V/V gains. After a change is made in the gain control area of Figure 9, click **Apply Changes** to write the changes to the ADA4255.
3. The **Error Detection** section (Label 8 in Figure 9) has three sections, the first two show the **Analog Error Flags** and the **Digital Error Flags** on the ADA4255. Each ADA4255 error flag is mapped to an indicator that turns on when the corresponding error bit is on. Both the digital and analog error register values are updated in the **Analog Error Flags** and **Digital Error Flags** fields. There is a check box next to each error flag that indicates whether the corresponding error flag is disabled or not. To disable the error flag, click the corresponding check box to update the registers. The last section within the Error Detection section is the **Error Flag Control** section. This section allows users to enable or disable the Error Latching feature of ACE. In disabled mode, users can select the suppression cycles. Click **Clear All Flags** to clear the error registers. This section also allows the user to **Poll Errors** from the ADA4255. Uncheck the corresponding check box to disable error updates from polling. Note that errors still update whenever **Apply Changes** or **Read All** is clicked.
4. The **GPIO Control** section (Label 9 in Figure 9) allows users to configure each GPIO direction by selecting the direction within the corresponding **Direction** dropdown menus. The **Input** and the **Output** directions can also be selected from the **Direction** dropdown menus. If in output mode, the user can set the GPIOx pin to either high or low through the use of the dropdown menus under the **Output** column. If in input mode, the **Output** column dropdown menus automatically update to high or low depending on the corresponding GPIOx pin status.
5. Click **Proceed to Memory Map** (Label 10 in Figure 9) to read from and write to any of the registers. Use hex format in all fields. A detailed view of the memory map is shown in Figure 12. For more information on the Memory Map view, go to https://wiki.analog.com/resources/tools-software/ace/understandingtheui/memorymapview.txt.

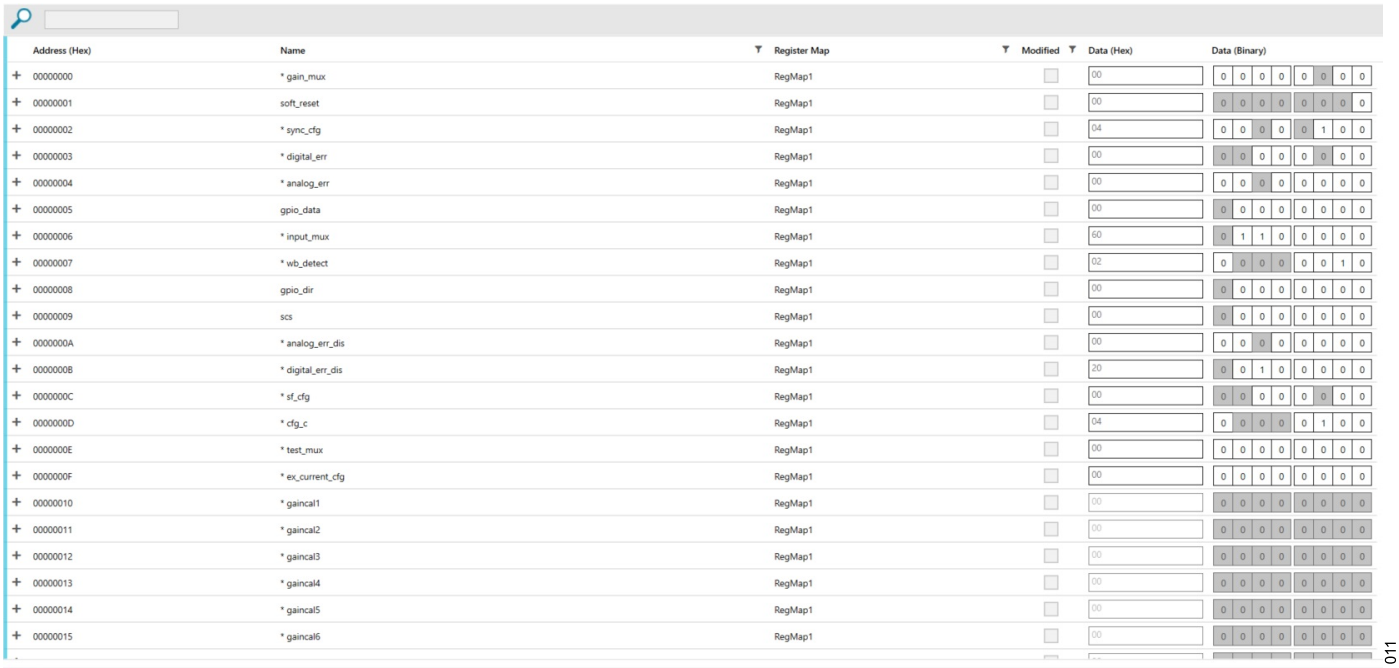

Figure 12. Memory Map of the ADA4255

EVALUATION BOARD SCHEMATICS

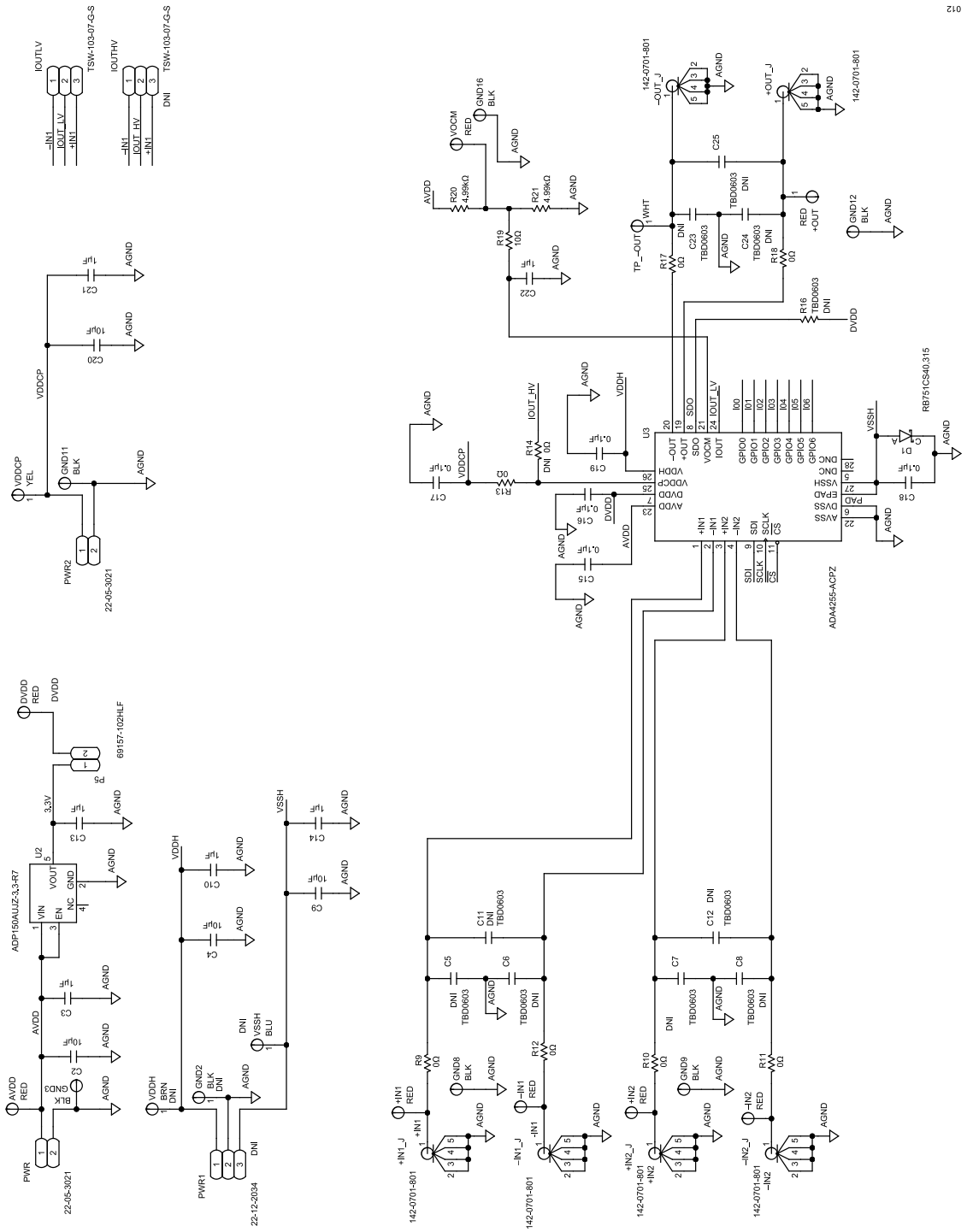

Figure 13. ADA4255CP-EBZ Evaluation Board Schematic, Page 1

EVALUATION BOARD SCHEMATICS

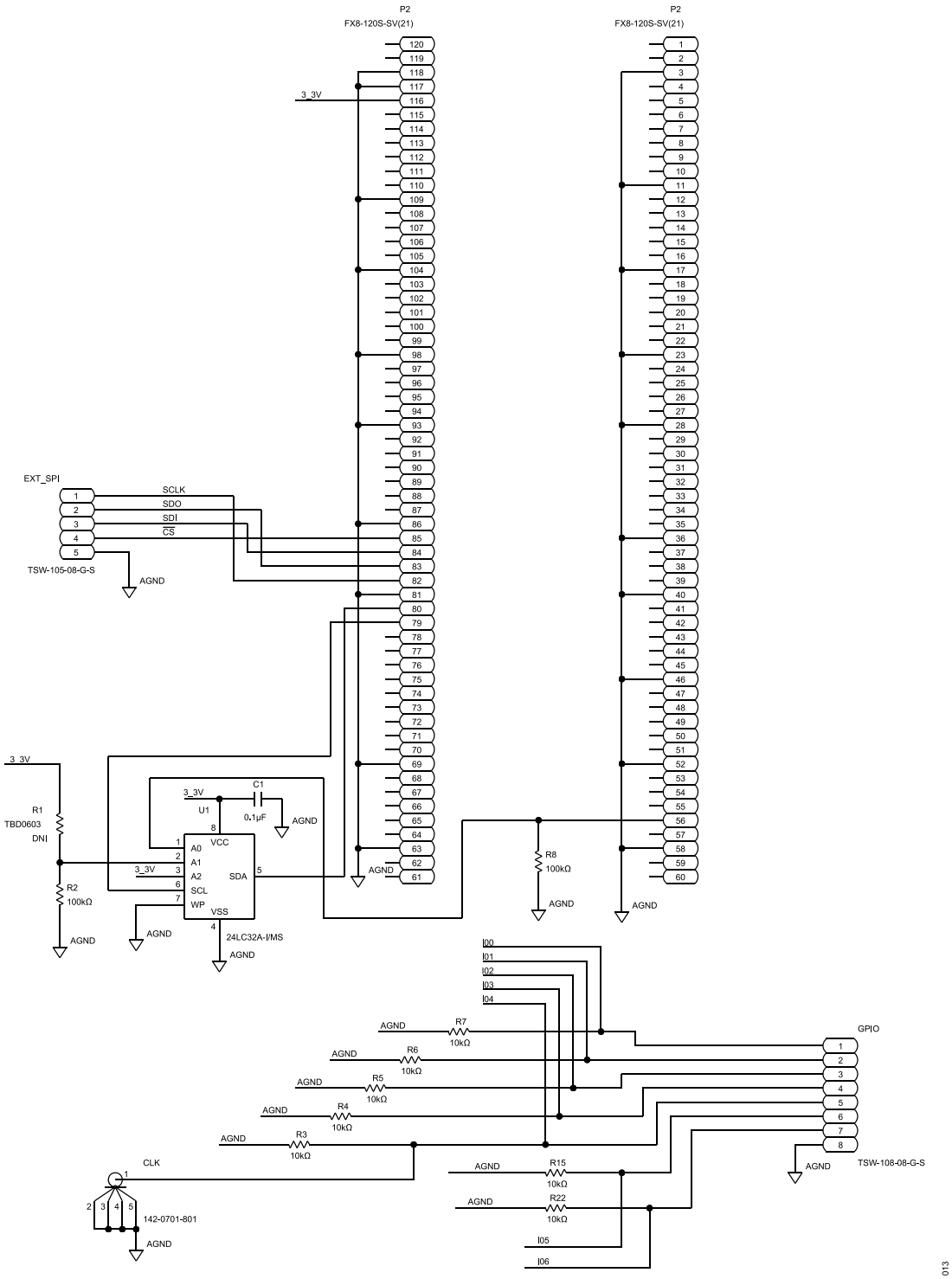

Figure 14. ADA4255CP-EBZ Evaluation Board Schematic, Page 2

ORDERING INFORMATION

BILL OF MATERIALS

Table 1.

Quantity	Reference Designator	Description	Manufacturer	Part Number
8	+IN1, +IN2, +OUT, −IN1, −IN2, AVDD, DVDD, VOCM	CONN-PCB, test points, red	Keystone Electronics	5005
7	+IN1_J, +IN2_J, +OUT_J, −IN1_J, −IN2_J, −OUT_J, CLK	CONN-PCB, coax, SMA end launch	Cinch Connectivity Solutions	142-0701-801
4	C1, C16, C17, C19	0.1 µF ceramic capacitors, 16 V, 10%, X7R, 0603	Kemet	C0603C104K4RAC
3	C10, C14, C21	1 µF ceramic capacitors, 50 V, 10%, X7R, 0603	Taiyo Yuden	UMK107AB7105KA-T
3	C3, C13, C22	1 µF ceramic capacitors, 10 V, 10%, X7R, 0603	Kemet	C0603C105K8RACTU
2	C15, C18	0.1 µF ceramic capacitors, 50 V, 10%, X7R, 0603	AVX	06035C104KAT2A
1	C2	10 µF ceramic capacitors, 16 V, 20%, X7R, 1206	TDK	C3216X7R1C106M160AC
3	C4, C9, C20	10 µF ceramic capacitors, 50 V, 10%, X7R, 1206	Samsung	CL31B106KBHNNNE
1	D1	Schottky diode, single barrier	NXP Semiconductors	RB751CS40,315
1	EXT_SPI	Connector header, vertical, 5 position, 2.54 mm, male header	Samtec	TSW-105-08-G-S
6	GND3, GND8, GND9, GND11, GND12, GND16	CONN-PCB, test points, black	Keystone Electronics	5006
1	GPIO	CONN-PCB, 8 position header, 0.100 single, gold	Samtec	TSW-108-08-G-S
1	IOUTLV	CONN-PCB, 3 position male header, unshrouded, 0.635 mm sq. post, single row, 5.84 mm mating post, 2.54 mm solder tail, 2.54 mm pitch	Samtec	TSW-103-07-G-S
1	P2	CONN-PCB, board to board connector, 0.60 mm pitch	Hirose Electric	FX8-120S-SV(21)
1	P5	Connector header, vertical, 2 position, male header	Amphenol FCI	69157-102HLF
2	PWR, PWR2	CONN-PCB, headers, with right angle friction lock	Molex	22-05-3021
7	R9, R10, R11, R12, R13, R17, R18	0 Ω resistors, surface-mounted device (SMD), 1/10 W, 0603, AEC-Q200 precision power	Vishay	CRCW06030000Z0EA
7	R3, R4, R5, R6, R7, R15, R22	10 kΩ resistors,SMD, 0.05%, 1/10 W, 0603, AEC-Q200 sulfur resistant	Susumu Co, LTD	RG1608N-103-W-T5
1	R19	10 Ω resistors, SMD, 1%, 1/10 W, 0603, AEC-Q200	Panasonic	ERJ-3EKF10R0V
2	R2, R8	100 kΩ resistors, SMD, 1%, 1/10 W, 0603, AEC-Q200	Panasonic	ERJ-3EKF1003V
2	R20, R21	4.99 kΩ resistors, SMD, 1%, 1/10 W, 0603, AEC-Q200	Panasonic	ERJ-3EKF4991V
1	TP_−OUT	CONN-PCB, test point, white	Keystone Electronics	5007
1	U1	IC, 32KBIT SERIAL EEPROM	Microchip Technology	24LC32A-I/MS
1	U2	Ultralow noise, 150 mA CMOS linear regulator	Analog Devices, Inc.	ADP150AUJZ-3.3-R7

ORDERING INFORMATION

Table 1.

Quantity	Reference Designator	Description	Manufacturer	Part Number
1	U3	Zero drift, high voltage, programmable gain instrumentation amplifier with charge pump	Analog Devices	ADA4255-ACPZ
1	VDDCP	CONN-PCB, test point, yellow	Components Corporation	TP-104-01-04

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.