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Power Line Communication with ModelGauge Fuel Gauge and Charger

MAX20357

General Description

The MAX20357 is a Power Line Communication (PLC) slave with ModelGauge m5 EZ fuel gauge and charger. The MAX20357 and MAX20355 provide a complete system solution for charging and data transfer between a charging case and battery powered device over a single contact.

The PLC interface is capable of 100kpbs throughput while simultaneously providing 200mA of charging/system current per channel. A 4Mbaud half-duplex data only UART mode provides an easy and fast method for firmware updates, debugging interface, and factory modes.

The charger on slave device MAX20357 controls the output of the 3.3W buck-boost converter in the MAX20355 with dynamic voltage scaling (DVS).

The MAX20357 integrates an ultra-low power fuel-gauge which implements the Maxim ModelGauge™ m5 algorithm. The IC monitors a single-cell battery pack and supports internal current sensing.

Additional features include comprehensive master device insertion and removal notifications, moisture detection, overcurrent protection, and 8kV contact rated ESD protection on the PLC output.

Applications

- True Wireless Stereo Headphones
- Augmented Reality Glasses
- Wearable Devices

Benefits and Features

- Power Line Communication (PLC) Interface
  - 100kpbs System Throughput
  - 167.7kpbs Bit Rate
  - 200mA Dual-Slave and 400mA Mono-Slave Output Charging Current
  - Automatic Earbud Insertion/Removal Detection
  - 4Mbaud, Half-Duplex, Data Only UART Mode
  - PLC Controllable GPIOs, Reset and Shipping Mode
- High-Efficiency Autonomous Charging System
  - 90% End-to-End Charging Efficiency from Master to Slave Battery
  - 400mA Integrated Linear Charger
  - Optimized Charging Efficiency by Automatic DVS Negotiation between Master and Slave
- Robust PLC Output Protection Features
  - Highly Flexible Moisture Detection Block
  - Input Current Limiting
  - 8kV Contact ESD Protection
- Small Solution Size
  - Low External Component Count
  - 2.69mm x 2.69mm 36-bump, 0.4mm pitch WLP Package

***Ordering information* appears at end of data sheet.**

Simplified Application Circuit

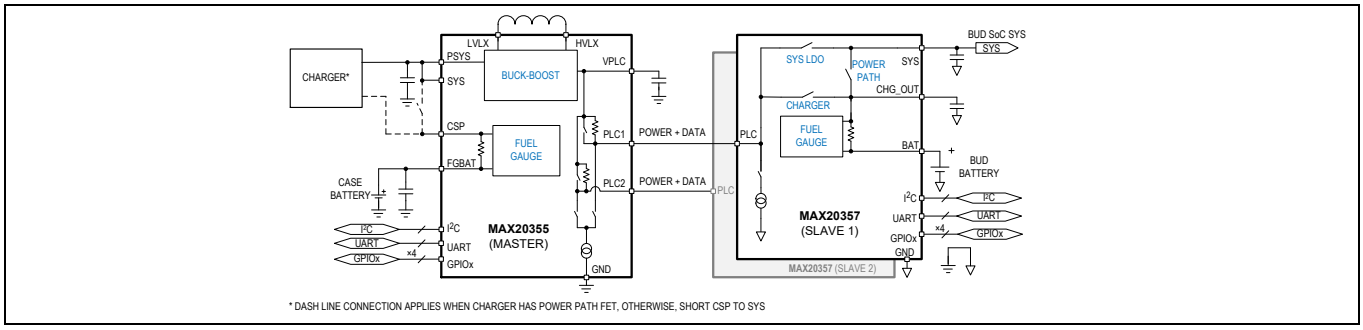

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TABLE OF CONTENTS

General Description 1
Applications 1
Benefits and Features 1
Simplified Application Circuit 1
Package Information 7
Typical Operating Characteristics 20
Pin Configuration 22
Pin Descriptions 23
Functional Diagram 24
Detailed Description 24
  Power Line Communication (PLC) 25
    PLC PING 25
  LISTEN Command and Continuously Updated Information 26
  Master Commands 26
  Slave Commands 27
    Mailbox Data Transfer (DOUT_REQ) 28
    Bulk Data Transfer (FIFO) 29
    Half-Duplex UART Passthrough Interface 32
  Autonomous Optimized Battery Charging 34
    Charger Battery Voltage Tracking Loop 34
    Ultra-Low Dropout Battery Charger 36
    Charger-Off State 38
    Charger IDLE state 38
    Charger IDLE state 39
    Precharge State 39
    Fast-Charge Constant Current (CC2) State 40
    Constant Current Tracking State CC Track 40
    Reduced Charge Current 42
    JEITA Compliance 42
    Thermal Regulation 46
    SYS LDO and Power Path 47
    Reverse Protection 48
  Mono-slave and Dual-slave Mode 48
    Battery Presence Detection 48
  PLC Operation Modes 49

SYSULVO Mode 52
SEAL Mode 53
OFF Mode 53
OFF Mode 53
PLC Detection Mode 53
Moisture Detection 56
PLC IDLE Mode 57
Master/Slave Resets and UBOOT Mode 60
General-Purpose Input Output (GPIO) 60
Watchdog 60
High ESD Protected ESD Outputs 60
ModelGauge M5 EZ Fuel Gauge with Integrated Sense Resistor 61
ModelGauge m5 EZ Performance 61
Application Notes 62
Standard Register Formats 62
ModelGauge m5 Algorithm 63
Analog Measurements 64
Voltage Measurement 64
MaxMinVolt Register (0x1B) 64
Current Measurement 64
Temperature Measurement 65
Temp Register (0x08) 65
MaxMinTemp Register (0x1A) 65
Power Measurement 65
Alert Function 65
Serial Number Feature 66
ModelGauge m5 Memory Space 66
I2C Serial Communication 67
General Description 67
Features 67
I2C Simplified Block Diagram 67
I2C System Configuration 67
I2C Interface Power 68
I2C Data Transfer 68
I2C Start and Stop Conditions 68
I2C Acknowledge Bit 68

I2C Slave Address 69
I2C Clock Stretching 69
I2C General Call Address 69
I2C Device ID 69
I2C Communication Speed 70
I2C Communication Protocols 70
Reading from a Single Register 73
Reading from Sequential Registers 73
Applications Information 74
PLC Current Sink and Detection Threshold 74
Typical Application Circuit 75
PCB Layout Guidelines 75
Register Map 76
Ordering Information 125

LIST OF FIGURES

Figure 1. Simplified Scheme of Power Line Communication (PLC) 25
Figure 2. Periodic PING 26
Figure 3. Sending Commands from the Slave 27
Figure 4. Master to Slave Mailbox Data Transfer 28
Figure 5. Slave to Master Mailbox Data Transfer 29
Figure 6. Bulk Data Transfer Implementation 30
Figure 7. Master to Slave Bulk Data Transfer 31
Figure 8. Slave to Master Bulk Data Transfer 32
Figure 9. UART Interface 33
Figure 10. UART Automatic Exit Through UART Timeout 34
Figure 11. Polling Structure of Automatic Charging Algorithm 35
Figure 12. Slave Voltage Control Algorithm 36
Figure 13. Step Charging Profile 37
Figure 14. Battery Charger FSM Diagram 38
Figure 15. Temperature Monitoring Disabled 43
Figure 16. Charging Enabled in Cool and Room Regions 44
Figure 17. Charging Enabled in Room and Warm Regions 45
Figure 18. Charging Enabled in Cool Room and Warm Regions 46
Figure 19. Input Limiter, Power Path, and Charger Block Diagram 47
Figure 20. MAX20357 Device Operating Modes 50
Figure 21. MAX20357 Device Operating Modes 52
Figure 22. PLC and Moisture Detection Block Diagrams 53
Figure 23. Active Master and Active Slave Connection 54
Figure 24. Active Master and Dead Slave Connection 55
Figure 25. Dead Master and Active Slave Connection 56
Figure 26. Enter PLC IDLE Mode After Slave Battery is Fully Charged. 58
Figure 27. Master and Slave Disconnection While in PLC IDLE Mode 59
Figure 28. ModelGauge m5 EZ Configuration Performance 62
Figure 29. ModelGauge m5 Algorithm 63
Figure 30. I2C Simplified Block Diagram 67
Figure 31. I2C System Configuration 68
Figure 32. I2C Start and Stop Conditions 68
Figure 33. Acknowledge Bit 69
Figure 34. Slave Address Example 69
Figure 35. Writing to a Single 8-bit Register with the Write Byte Protocol 71
Figure 36. Writing to Sequential Registers X to N 72
Figure 37. Example I2C Write 16-bit Data Communication Sequence 73
Figure 38. Reading from a Single Register with the Read Byte Protocol 73
Figure 39. Reading Continuously from Sequential Registers X to N 74
Figure 40. PLC Current Sink and Detection Threshold 75
Figure 41. Typical Application Circuit 75
Figure 42. Layout Guideline 76

LIST OF TABLES

Table 1. Master Commands 27
Table 2. Slave Commands 28
Table 3. UART Switch Settings in Master PLC Command Argument 33
Table 4. UART Switch Settings in Slave PLC Command Argument 33
Table 5. Functional Block Status in Low Power Modes 49
Table 6. Functional Block Status in Low Power Modes 50
Table 7. Moisture Interrupt 57
Table 8. Reset Types and Description 60
Table 9. ModelGauge m5 EZ Performance 61
Table 10. ModelGauge m5 Register Standard Resolutions 62
Table 11. Serial Number Format 66
Table 12. ModelGauge m5 Register Memory Map 66
Table 13. PLC Detection Pair (MAX20355 Data Packet) 74
Table 14. PLC Detection Pair (MAX20357 Data Packet) 74

Absolute Maximum Ratings

VDIG to GND.....-0.3V to +2V

PLC, CHG_OUT, SYS, BAT, THM, UART_TX, UART_RX to GND .....-0.3V to +6V

SDA, SCL, $\overline{INT}$, EN, GPIO1, GPIO2, GPIO3, GPIO4 to GND -0.3V to +6V

$\overline{ALRT}$ to GND .....-0.3V to +17V

CTB to GND .....-0.3V to +6V

CTB to BAT ..... +0.3V

GDIG to GND .....-0.3V to +0.3V

PLC (Continuous Current) 550mA

CHG_OUT (Continuous Current)..... 450mA

BAT to CHG_OUT (SYS power path) sense resistor current limit (100%, Continuous utilization)..... 250mA

BAT to CHG_OUT (SYS power path) sense resistor current limit (10% utilization) 350mA

BAT to CHG_OUT (SYS power path) sense resistor current limit (Peak pulsed current, 250ms maximum pulse width, 10% maximum duty cycle, 1% utilization) 450mA

Any other pin (Continuous Current).....20mA

Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, derate 21.87mW/°C above +70°C.).....1.75W

Operating Temperature Range .....-40°C to +85°C

Junction Temperature .....+150°C

Storage Temperature Range .....-40°C to +150°C

Soldering Temperature (Reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

WLP

Package Code	W362J2+1
Outline Number	*21-100525*
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	45.72°C/W

Electrical Characteristics

(T_A = -40°C to +85°C, V_{BAT} = 3.7V, C_{DIG} = 1µF, C_{SYS} = 1µF, C_{BAT} = 1µF. All capacitance listed are effective values.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GLOBAL POWER SUPPLIES (PLC, BAT)						
PLC Supply Current	I_{PLC}	Master found, Charger and SYS LDO enabled, I_{CHG} = I_{SYS} = 0mA, fuel gauge disabled, PLC communication not active		380	650	µA
PLC Valid Supply Voltage	V_{PLC_DET}			3		V
PLC Detection Debounce Time	t_{PLC_DEB}			19		ms
BAT Input Start-Up Voltage	V_{BAT_STUP}		2.9			V
BAT Input Voltage Range	V_{BAT_RNG}		2.8		5.5	V
BAT Supply Current	I_{BAT1}	Master detection state, V_{BAT} = 3.7V, Fuel Gauge disabled		2.8	30	µA
	I_{BAT2}	Master found, V_{BAT} = 4.2V, device in PLC IDLE State, averaged, Fuel Gauge disabled		11	40	

(T_A = -40°C to +85°C, V_{BAT} = 3.7V, C_{DIG} = 1µF, C_{SYS} = 1µF, C_{BAT} = 1µF. All capacitance listed are effective values.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
	I_{BAT3}	EN = 0, V_{BAT} = 3.7V, device disabled	(OFF state)		0.6	2	
	I_{BAT4}	EN = 0, V_{BAT} = 3.7V, device disabled	SEAL mode (SYSUVLO or SEAL mode)		165		nA
INTERNAL SUPPLIES, UVLO							
Internal V_{DIG} Regulator	V_{DIG}			1.71	1.80	1.89	V
V_{DIG} UVLO Threshold	V_{DIG_UVLOR}	V_{DIG} rising		1.61		1.715	V
	V_{DIG_UVLOF}	V_{DIG} falling		1.51		1.61	
	$V_{DIG_UVLO_H}$				100		mV
Internal V_{CCINT} LDO	V_{CCINT_LDO}	V_{PLC} present			2.8		V
V_{CCINT} UVLO (POR) Threshold	V_{CCINT_UVLOR}	Supply rising		2.25	2.47	2.72	V
	V_{CCINT_UVLOF}	Supply falling		2.2	2.42	2.67	
	V_{CCINT_UVLOH}				50		mV
V_{OTP_OK} UVLO Threshold	$V_{OTP_OK_UVLOF}$	Supply falling		2.6	2.75	2.9	V
	$V_{OTP_OK_UVLOH}$				50		mV
V_{CCINT} FG UVLO Threshold	V_{CCINT_FGUVLR}	Supply rising		2.47	2.55	2.63	V
	V_{CCINT_FGUVLF}	Supply falling		2.42	2.50	2.58	
	V_{CCINT_FGUVLH}				50		mV
Battery Presence, FG BATUVLO Threshold	$V_{BP_FG_UVLOR}$	PLC valid present		2.48	2.55	2.6	V
	$V_{BP_FG_UVLOF}$	PLC valid present		2.45	2.5	2.55	
	$V_{BP_FG_UVLO_H}$	PLC valid present			50		mV
BAT Pulldown Resistance	RPD_{BAT}	BattPullDown = 0b1			3		kΩ
SYS UVLO Threshold	V_{SYS_UVLO1F}	SYSUVLOThSel = 0b00	V_{SYS} falling	2.60	2.70	2.80	V
	V_{SYS_UVLO2F}	SYSUVLOThSel = 0b01	V_{SYS} falling	2.80	2.90	3.00	
	V_{SYS_UVLO3F}	SYSUVLOThSel = 0b10	V_{SYS} falling	2.90	3.00	3.10	
	V_{SYS_UVLO4F}	SYSUVLOThSel = 0b11	V_{SYS} falling	3.10	3.20	3.30	
	$V_{SYS_UVLO_HYS}$				50		mV
POWER LINE COMMUNICATION (PLC)							
Data Throughput	TP_{DAT}	Maximum output current			>100		kbps

(T_A = -40°C to +85°C, V_{BAT} = 3.7V, C_{DIG} = 1µF, C_{SYS} = 1µF, C_{BAT} = 1µF. All capacitance listed are effective values.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
UART SWITCH							
Analog Signal Range	V_{UART_RNG}			0		V_{BAT}	V
On-Resistance	R_{ONUART}				9	15	Ω
On-Resistance Flatness	$R_{FLATUART}$				0.1	0.3	Ω
Off-Leakage Current	$I_{LUART(OFF)}$					1	µA
On-Leakage Current	$I_{LUART(ON)}$	V_{UART} = 0V, V_{BAT} = 3.7V				1	µA
		V_{UART} = 5.5V, V_{BAT} = 5.5V				10	
UART TIMING							
Enter UART Delay Time	t_{UART_DELAY}	From V_{PLC} < 2.9V to UART Done			20.2		ms
Exit UART Idle Time	t_{UART_IDLE}	From UART idle to UART switch open			0.5		s
Exit UART Switch Open Time	t_{SW_OPN}	From UART switch open to UART exit			0.6		s
WATCHDOG TIMING							
Watchdog Timeout	t_{WD_TO}	wd__eoc_sel = 0b00			4		s
		wd__eoc_sel = 0b01			8		
		wd__eoc_sel = 0b10			16		
		wd__eoc_sel = 0b11			32		
BATTERY CHARGER (PLC TO BAT)							
PLC to BAT Charge Current Reduction Threshold	$V_{PLC_BAT_LIM}$	Measured as V_{PLC} - V_{BAT}, V_{BAT} = 4.0V	PLC_DROP = 0b000		50		mV
			PLC_DROP = 0b001		75		
			PLC_DROP = 0b010		100		
			PLC_DROP = 0b011		125		
			PLC_DROP = 0b100		150		
			PLC_DROP = 0b101		175		
			PLC_DROP = 0b110		200		
		Measured as V_{PLC} - V_{BAT}, V_{BAT} = 4.0V	PLC_DROP = 0b111		225		
Precharge Current	I_{PCHG}	IPChg = 0b00			0.047 × I_{FCHG2}		mA
		IPChg = 0b01		0.070 × I_{FCHG2}	0.094 × I_{FCHG2}	0.12 × I_{FCHG2}	
		IPChg = 0b10			0.20 × I_{FCHG2}		
		IPChg = 0b11			0.30 × I_{FCHG2}		
Precharge Threshold	V_{BAT_PCHG}	V_{BAT} rising	VPChg = 0b000		2.7		V
			VPChg = 0b001		2.8		

(T_A = -40°C to +85°C, V_{BAT} = 3.7V, C_{DIG} = 1µF, C_{SYS} = 1µF, C_{BAT} = 1µF. All capacitance listed are effective values.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
			VPChg = 0b010		2.9		
			VPChg = 0b011		3.0		
			VPChg = 0b100		3.1		
			VPChg = 0b101		3.2		
			VPChg = 0b110		3.3		
			VPChg = 0b111		3.4		
Precharge Threshold Hysteresis	$V_{BAT_PCHG_H}$				120		mV
Step Charge Threshold	V_{BAT_STPCHG}	V_{BAT} rising	ChgStepRise = 0b0000		3.80		V
			ChgStepRise = 0b0001		3.85		
			ChgStepRise = 0b0010		3.90		
			ChgStepRise = 0b0011		3.95		
			ChgStepRise = 0b0100		4.00		
			ChgStepRise = 0b0101		4.05		
			ChgStepRise = 0b0110		4.10		
			ChgStepRise = 0b0111		4.15		
			ChgStepRise = 0b1000		4.20		
			ChgStepRise = 0b1001		4.25		
			ChgStepRise = 0b1010		4.30		
			ChgStepRise = 0b1011		4.35		
			ChgStepRise = 0b1100		4.40		
			ChgStepRise = 0b1101		4.45		
			ChgStepRise = 0b1110		4.50		
			ChgStepRise = 0b1111		4.55		
Step Charge Threshold Hysteresis	$V_{BAT_STPCHG_H}$	ChgStepHyst = 0b000			100		mV
		ChgStepHyst = 0b001			200		
		ChgStepHyst = 0b010			300		
		ChgStepHyst = 0b011			400		
		ChgStepHyst = 0b100			500		
		ChgStepHyst = 0b101			600		
		ChgStepHyst = 0b110			600		

(T_A = -40°C to +85°C, V_{BAT} = 3.7V, C_{DIG} = 1µF, C_{SYS} = 1µF, C_{BAT} = 1µF. All capacitance listed are effective values.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		ChgStepHyst = 0b111			600		
Fast-Charge Current Zone 1	I_{FCHG1}	CC1IFChg = 0b0000000 to 0b0111100			5 to 65 step 1		mA
		CC1IFChg = 0b0111101 to 0b1001111			70 to 160 step 5		
		CC1IFChg = 0b1010000 to 0b1010011			170 to 200 step 10		
		CC1IFChg = 0b1010100 to 0b1111111			200		
Fast-Charge Current Zone 2	I_{FCHG2}	CC2IFChg = 0b0000000 to 0b0111100			5 to 65 step 1		mA
Fast-Charge Current Zone 2	I_{FCHG2}	CC2IFChg = 0b0111101 to 0b1001111			70 to 160 step 5		mA
		CC2IFChg = 0b1010000 to 0b1010011			170 to 200 step 10		
		CC2IFChg = 0b1010100 to 0b1111111			200		
Battery-Regulation Voltage	V_{BATREG}	BatReg = 0b001111 to 0b110111			4.05 to 4.6 step 10m		V
		BatReg = 0b111000 to 0b111111			4.6		
Battery-Regulation Voltage	V_{BATREG}	BatReg = 0b001111, T_A = 25°C		4.1958	4.200	4.2042	V
		BatReg = 0b001111		4.179	4.200	4.221	
Battery Recharge Threshold	V_{BAT_RECHG}	Charger recharge threshold to BatReg	BatReChg = 0b00		-50		mV
			BatReChg = 0b01		-100		
			BatReChg = 0b10		-150		
			BatReChg = 0b11		-200		
Precharge Timer	t_{PCHG}	PChgTmr = 0b00			30		min
		PChgTmr = 0b01			60		
		PChgTmr = 0b10			120		
		PChgTmr = 0b11			240		
Fast Charge CC1 Timer	t_{FCHG1}	CC1FChgTmr = 0b00			30		min
		CC1FChgTmr = 0b01			60		
		CC1FChgTmr = 0b10			120		
		CC1FChgTmr = 0b11			240		
Charger Safety Timer	t_{CHG}	ChgTmr = 0b00			75		min
Charger Safety Timer	t_{CHG}	ChgTmr = 0b01			150		min
		ChgTmr = 0b10			300		
		ChgTmr = 0b11			600		
Charge Done Qualification	I_{CHG_DONE}	IChgDone = 0b00			0.023 × I_{FCHG2}		mA

(T_A = -40°C to +85°C, V_{BAT} = 3.7V, C_{DIG} = 1µF, C_{SYS} = 1µF, C_{BAT} = 1µF. All capacitance listed are effective values.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		IChgDone = 0b01			0.051 × I_{FCHG2}		
		IChgDone = 0b10		0.091 x I_{FCHG2}	0.10 x I_{FCHG2}	0.11 x I_{FCHG2}	
		IChgDone = 0b11			0.20 × I_{FCHG2}		
Maximum Maintain Charge Time	t_{MTCHG}	MtChgTmr = 0b00			0		min
		MtChgTmr = 0b01			15		
		MtChgTmr = 0b10			30		
		MtChgTmr = 0b11			60		
Timer Accuracy	t_{CHG_ACC}			-10		+10	%
Fast-Charge Timer Extend Current Threshold	I_{FCHG_TEXT}	See *Figure 14*			50		% $I_{FCHG1,2}$
Fast-Charge Timer Suspend Current Threshold	I_{FCHG_TSUS}	See *Figure 14*			20		% $I_{FCHG1,2}$
Battery Regulation Voltage Reduction Due to Temperature	$V_{BAT_REG_JTA}$	ChgCool/Room/WarmBatReg = 0b00			V_{BAT_REG}-0.15		V
		ChgCool/Room/WarmBatReg = 0b01			V_{BAT_REG} - 0.1		
		ChgCool/Room/WarmBatReg = 0b10			V_{BAT_REG} - 0.05		
		ChgCool/Room/WarmBatReg = 0b11			V_{BAT_REG}		
Fast-Charge Current Reduction Due to Temperature	I_{FCHG_JTA}	CCxIFChg = CC1IFChg or CC2IFChg based on Step Charge comparator status	ChgCool/Room/WarmCCxIFChg = 0b000		20		% $I_{FCHG1,2}$
		CCxIFChg = CC1IFChg or CC2IFChg based on Step Charge comparator status	ChgCool/Room/WarmCCxIFChg = 0b001		30		
			ChgCool/Room/WarmCCxIFChg = 0b010		40		
			ChgCool/Room/WarmCCxIFChg= 0b011		50		
			ChgCool/Room/WarmCCxIFChg = 0b100		60		
			ChgCool/Room/WarmCCxIFChg = 0b101		70		
			ChgCool/Room/WarmCCxIFChg = 0b110		80		

(T_A = -40°C to +85°C, V_{BAT} = 3.7V, C_{DIG} = 1µF, C_{SYS} = 1µF, C_{BAT} = 1µF. All capacitance listed are effective values.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
			ChgCool/Room/WarmCCxIFChg = 0b111		100		
Reverse Protection Threshold	$V_{CHG_REV_TH}$	V_{BAT} raising over V_{PLC}	V_{BAT} - V_{PLC}		25		mV
	$V_{CHG_REV_HYS}$	V_{BAT} raising over V_{PLC}	V_{BAT} - V_{PLC}		50		
LDO (PLC TO SYS)							
PLC to SYS Current Reduction Threshold	$V_{PLC_SYS_LIM}$	Measured as V_{PLC} – V_{SYS}	PLC_DROP = 0b000 SysMin = 0b0000		50		mV
		Measured as V_{PLC} – V_{SYS}	PLC_DROP = 0b001 SysMin = 0b0000		75		
			PLC_DROP = 0b010 SysMin = 0b0000		100		
			PLC_DROP = 0b011 SysMin = 0b0000		125		
			PLC_DROP = 0b100 SysMin = 0b0000		150		
			PLC_DROP = 0b101 SysMin = 0b0000		175		
			PLC_DROP = 0b110 SysMin = 0b0000		200		
			PLC_DROP = 0b111 SysMin = 0b0000		225		
LDO Output Current Limit	I_{LDO_LIM}				3.125 to 200, step 3.125		mA
Minimum SYS Voltage	V_{SYS_MIN}	V_{BAT} = 2.8V	SysMin = 0b0000	2.97	3.0	3.03	V
			SysMin = 0b0001		3.1		
			SysMin = 0b0010		3.2		
			SysMin = 0b0011		3.3		
			SysMin = 0b0100	3.366	3.4	3.434	
			SysMin = 0101		3.5		
			SysMin = 0b0110		3.6		
			SysMin = 0b0111		3.7		
			SysMin = 0b1000		3.8		
			SysMin = 0b1001		3.9		
			SysMin = 0b1010		4.0		
			SysMin = 0b1011		4.1		

(T_A = -40°C to +85°C, V_{BAT} = 3.7V, C_{DIG} = 1µF, C_{SYS} = 1µF, C_{BAT} = 1µF. All capacitance listed are effective values.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
			SysMin = 0b1100		4.2		
			SysMin = 0b1101		4.3		
			SysMin = 0b1110		4.4		
			SysMin = 0b1111		4.5		
SYS Regulation Voltage	V_{SYS_REG}	V_{BAT} = 3V	SysMin = 0b0000		V_{BAT}		V
Reverse Protection Threshold	$V_{LDO_REV_TH}$	V_{SYS} raising over V_{PLC}	V_{SYS} - V_{PLC}		25		mV
Reverse Protection Threshold Hysteresis	$V_{LDO_REV_HYS}$	V_{SYS} - V_{PLC}			50		mV
POWER PATH (BAT TO SYS)							
BAT to SYS On Resistance	R_{PP}	V_{BAT} = 4.35V, I_{SYS}= 200mA, SYS LDO disabled			200	290	mΩ
BAT to SYS On Threshold	$V_{BAT_SYS_ON}$	LDO enabled, V_{BAT} = 4.35V, V_{PLC} = 3.5V, I_{SYS} = 10mA, measured as V_{BAT} - V_{SYS}	PP_drp = 0b000	14	25	36	mV
			PP_drp = 0b001	25	37.5	50	
		LDO enabled, V_{BAT} = 4.35V, V_{PLC} = 3.5V, I_{SYS}=10mA, measured as V_{BAT} - V_{SYS}	PP_drp = 0b010	37.5	50	62.5	
		LDO enabled, V_{BAT} = 4.35V, V_{PLC} = 3.5V, I_{SYS} = 10mA, measured as V_{BAT} - V_{SYS}	PP_drp = 0b011	50	62.5	75	
			PP_drp = 0b100	62	75	88	
			PP_drp = 0b101	74.5	87.5	100.5	
			PP_drp = 0b110	86.5	100	113.5	
			PP_drp = 0b111	98.5	112.5	126.5	
PLC INPUT CURRENT LIMITER							
Total PLC Current Limit	I_{PLC_LIM}	Ichg_x2 = 0			3.333 to 203.3 step 3.125		mA
		Ichg_x2 = 1			6.666 to 406.6 step 6.25		
THERMISTOR MONITOR							
THM Hot Threshold	V_{THM_HOT1}	V_{THM} falling (70°C)		16.36	18.36	20.36	%V_{VDIG}
	V_{THM_HOT2}	V_{THM} falling (65°C)		18.70	20.70	22.70	
	V_{THM_HOT3}	V_{THM} falling (60°C)		21.44	23.44	25.44	
	V_{THM_HOT4}	V_{THM} falling (55°C)		24.17	26.17	28.17	
	V_{THM_HOT5}	V_{THM} falling (50°C)		27.30	29.30	31.30	
	V_{THM_HOT6}	V_{THM} falling (45°C)		30.81	32.81	34.81	
	V_{THM_HOT7}	V_{THM} falling (40°C)		34.72	36.72	38.72	

(T_A = -40°C to +85°C, V_{BAT} = 3.7V, C_{DIG} = 1µF, C_{SYS} = 1µF, C_{BAT} = 1µF. All capacitance listed are effective values.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
	V_{THM_HOT8}	V_{THM} falling (35°C)		39.02	41.02	43.02	
THM Warm Threshold	V_{THM_WARM1}	V_{THM} falling (55°C)		24.17	26.17	28.17	$\%V_{VDIG}$
	V_{THM_WARM2}	V_{THM} falling (50°C)		27.30	29.30	31.30	
	V_{THM_WARM3}	V_{THM} falling (45°C)		30.81	32.81	34.81	
	V_{THM_WARM4}	V_{THM} falling (40°C)		34.72	36.72	38.72	
	V_{THM_WARM5}	V_{THM} falling (35°C)		39.02	41.02	43.02	
	V_{THM_WARM6}	V_{THM} falling (30°C)		43.31	45.31	47.31	
	V_{THM_WARM7}	V_{THM} falling (25°C)		48.00	50.00	52.00	
	V_{THM_WARM8}	V_{THM} falling (20°C)		52.69	54.69	56.69	
THM Cool Threshold	V_{THM_COOL1}	V_{THM} rising (25°C)		48.00	50.00	52.00	$\%V_{VDIG}$
	V_{THM_COOL2}	V_{THM} rising (20°C)		52.69	54.69	56.69	
	V_{THM_COOL3}	V_{THM} rising (15°C)		57.77	59.77	61.77	
	V_{THM_COOL4}	V_{THM} rising (10°C)		62.45	64.45	66.45	
	V_{THM_COOL5}	V_{THM} rising (25°C)		67.14	69.14	71.14	
	V_{THM_COOL6}	V_{THM} rising (20°C)		71.83	73.83	75.83	
	V_{THM_COOL7}	V_{THM} rising (15°C)		76.13	78.13	80.13	
	V_{THM_COOL8}	V_{THM} rising (10°C)		80.03	82.03	84.03	
THM Cold Threshold	V_{THM_COLD1}	V_{THM} rising (15°C)		57.77	59.77	61.77	$\%V_{VDIG}$
	V_{THM_COLD2}	V_{THM} rising (10°C)		62.45	64.45	66.45	
	V_{THM_COLD3}	V_{THM} rising (5°C)		67.14	69.14	71.14	
	V_{THM_COLD4}	V_{THM} rising (0°C)		71.83	73.83	75.83	
	V_{THM_COLD5}	V_{THM} rising (-5ºC)		76.13	78.13	80.13	
	V_{THM_COLD6}	V_{THM} rising (-10°C)		80.03	82.03	84.03	
	V_{THM_COLD7}	V_{THM} rising (-15°C)		83.16	85.16	87.16	
	V_{THM_COLD8}	V_{THM} rising (-20°C)		86.28	88.28	90.28	
THM Disable Threshold	V_{THM_DIS}	V_{THM} rising		91.75	93.75	95.75	$\%V_{VDIG}$
THM Threshold Hysteresis	V_{THM_H}				60		mV
THM Input Leakage	I_{THM_LK}	V_{THM} = 0V to 5.5V	TPU switch open	-1		+1	µA
MOISTURE DETECTION							
Impedance Measurement Range	R_{MOIST_RANGE}			6		1400	kΩ
Current Source Accuracy	I_{ID_ACC}	PLC = 1.5V	I_{ID} = 1µA	-29.5		+5.5	%
			I_{ID} = 4µA	-10.5		+4.5	
			I_{ID} = 16µA	-6.4		+4.9	
			I_{ID} = 64µA	-5.4		+5.0	
Current Source	I_{ID}				1		µA
					4		
					16		
					64		

(T_A = -40°C to +85°C, V_{BAT} = 3.7V, C_{DIG} = 1µF, C_{SYS} = 1µF, C_{BAT} = 1µF. All capacitance listed are effective values.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ADC Resolution	ADC_{RES}				8		bit
ADC Voltage Step	ADC_{STEP}				5.9		mV
ADC Full-Scale Error	ADC_{ERR}			-2		+2	%
ADC Noise Filtering	ADC_{NOISE}				45		µs
ADC Full Scale	ADC_{SCALE}				1.5		V
PLC COMMUNICATION DETECTION THRESHOLDS							
PLC Detection Threshold	V_{TH_PLC}	PLCThrSel = 0b00			75		mV
		PLCThrSel = 0b01			90		
		PLCThrSel = 0b10			105		
		PLCThrSel = 0b11			120		
PLC COMMUNICATION TIME UNIT							
PLC Communication Time Unit	TU_{PLC}				6		us
PLC COMMUNICATION CURRENT SINK							
Current Sink Accuracy	I_{SINK_ACC}			-10		+10	%
Current Sink	I_{SINK}	PLC = 4V	PLCSnkSel = 0b00, Ichg_x2 = 0b0		50		mA
			PLCSnkSel = 0b01, Ichg_x2 = 0b0		70		
			PLCSnkSel = 0b10, Ichg_x2 = 0b0		90		
			PLCSnkSel = 0b11, Ichg_x2 = 0b0		110		
			PLCSnkSel = 0b00, Ichg_x2 = 0b1		100		
			PLCSnkSel = 0b01, Ichg_x2 = 0b1		140		
			PLCSnkSel = 0b10, Ichg_x2 = 0b1		180		
			PLCSnkSel = 0b11, Ichg_x2 = 0b1		220		
FUEL GAUGE POWER SUPPLY							
Shutdown Supply Current	I_{DD0}				0.5		µA
Hibernate Supply Current	I_{DD1}	Average current			5.1		µA
Active Supply Current	I_{DD2}	Average current not including thermistor measurement current			15		µA
FUEL GAUGE ANALOG-TO-DIGITAL CONVERSION							
BATT Measurement Error	V_{GERR}	T_A = +25°C		-7.5		7.5	mV
		-40°C ≤ T_A ≤ +85°C		-20		20	
BATT Measurement Resolution	V_{LSB}				78.125		µV
BATT Measurement Range	V_{FS}			2.8		4.9	V

(T_A = -40°C to +85°C, V_{BAT} = 3.7V, C_{DIG} = 1µF, C_{SYS} = 1µF, C_{BAT} = 1µF. All capacitance listed are effective values.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FUEL GAUGE LEAKAGE	R_{SNS}	T_A = +25°C		30		mΩ
Current Measurement Offset Error	I_{OERR}	Long term average without load current		±1		mA
Current Measurement Resolution	I_{LSB}			39.0625		µA
Current Measurement Gain Error	I_{GERR}	(Note 1)		±2.5		% of Reading
Current Measurement Error	I_{ERR}	T_A ≤ +50°C, 0.125A and 0.25A (Note 1)	-3		+3	% of Reading
Internal Temperature Measurement Error	T_{IGERR}	-40°C ≤ T_A ≤ +85°C		±1		°C
Internal Temperature Measurement Resolution	T_{ILSB}			0.00391		°C
FUEL GAUGE INPUT/OUTPUT						
THM Pullup Resistance (Internal)	R_{TH10}	Config.R100 = 0	9.6	16	22.4	kΩ
	R_{TH100}	Config.R100 = 1	96	160	224	
Output Drive Low, ALRT, SDA	V_{OL}	I_{OL} = 4mA, V_{BAT} = 2.3V			0.4	V
Input Logic-High, ALRT, SCL, SDA	V_{IH}		1.5			V
Input Logic-Low, ALRT, SCL, SDA	V_{IL}				0.5	V
Battery-Detach Detection Threshold	V_{DET}	Measured as a fraction of V_{BAT} on TH rising	91.0	96.2	99.0	%
Battery-Detach Detection Threshold Hysteresis	$V_{DET-HYS}$	Measured as a fraction of V_{BAT} on TH falling		1		%
Battery-Detach Comparator Delay	t_{TOFF}	TH step from 70% to 100% of V_{BAT} (ALRTP = 0, EnAIN = 1, FTHRM = 1)			100	µs
FUEL GAUGE LEAKAGE						
Leakage Current, ALRT	I_{LEAK}	VALRT < 15V	-1		+1	µA
Leakage Current, THM	I_{LEAK_TH}		-1		+1	µA
FUEL GAUGE TIMING						
Time-Base Accuracy	t_{ERR}	T_A = +25°C	-1		1	%
		-40°C ≤ T_A ≤ +85°C	-5		5	%
THM Precharge Time	t_{PRE}		8.48			ms
DIGITAL SIGNALS (SDA, SCL, nINT, EN, GPIO1, GPIO2, GPIO3, GPIO4, ALRT)						
Input Logic-High	V_{IO_IH}		1.4			V
Input Logic-Low	V_{IO_IL}				0.4	V
Input Logic-High GPIO CMOS	$V_{IO_IH_CMOS}$	(Note 2)		0.7 x V_{CCINT}		V
Input Logic-Low GPIO CMOS	$V_{IO_IL_CMOS}$	(Note 2)		0.3 x V_{CCINT}		V

(T_A = -40°C to +85°C, V_{BAT} = 3.7V, C_{DIG} = 1µF, C_{SYS} = 1µF, C_{BAT} = 1µF. All capacitance listed are effective values.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GPIO Input Pullup/Pulldown Resistor	R_{in_GPIO}	Input resistor presence I²C controlled, as Pullup, it is tied to V_{CCINT}			175		kΩ
Input Leakage Current	I_{LK_I}	SCL and EN		-1		+1	µA
Output Logic-High Leakage Current (Open Drain Only)	I_{LK_O}	SDA, nINT, GPIO1, GPIO2, GPIO3, GPIO4, ALRT				1	µA
Output Logic-Low	V_{IO_OL}	I_{SINK} = 20mA				0.4	V
I²C TIMING (SDA, SCL)							
SCL Clock Frequency	f_{SCL}	(Note 3)		0		400	kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}			1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$	(Note 4)		0.6			µs
Low Period of SCL Clock	t_{LOW}			1.3			µs
High Period of SCL Clock	t_{HIGH}			0.6			µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$			0.6			µs
Data Hold Time	$t_{HD:DAT}$	(Note 5, Note 6)		0		0.9	µs
Data Setup Time	$t_{SU:DAT}$	(Note 5)		100			ns
Setup Time for STOP Condition	$t_{SU:STO}$			0.6			µs
Spike Pulse Width Suppressed by Input Filter	t_{SP}	(Note 7)				50	ns
ESD PROTECTION (PLC, ALL OTHER PINS)							
ESD Protection Rating		PLC	Contact discharge		8		kV
		All other pins	HBM		2		
THERMAL PROTECTION & THERMAL CURRENT LIMITATION							
Overtemperature Threshold	T_{SHDN_PLC}	Valid PLC present	ChgThrmLim = 0b0000		40		°C
		Valid PLC present	ChgThrmLim = 0b0001		45		
			ChgThrmLim = 0b0010		50		
		Valid PLC present	ChgThrmLim = 0b0011		55		
		Valid PLC present	ChgThrmLim = 0b0100		60		
			ChgThrmLim = 0b0101		65		
		Valid PLC present	ChgThrmLim = 0b0110		70		

(T_A = -40°C to +85°C, V_{BAT} = 3.7V, C_{DIG} = 1µF, C_{SYS} = 1µF, C_{BAT} = 1µF. All capacitance listed are effective values.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		Valid PLC present	ChgThrmLim = 0b0111		75		
			ChgThrmLim = 0b1000		80		
		Valid PLC present	ChgThrmLim = 0b1001		85		
		Valid PLC present	ChgThrmLim = 0b1010		90		
			ChgThrmLim = 0b1011		95		
		Valid PLC present	ChgThrmLim = 0b1100		100		
		Valid PLC present	ChgThrmLim = 0b1101		105		
			ChgThrmLim = 0b1110		110		
		Valid PLC present	ChgThrmLim = 0b1111		115		
Overtemperature Threshold Hysteresis	T_{SHDN_PLCH}	Valid PLC present			3		°C
Current Thermal Limitation	T_{LIM}	Valid PLC present			T_{SHDN_PLC} -3		°C
Overtemperature Threshold	T_{SHDN}				130		°C
Overtemperature Threshold Hysteresis	T_{SHDN}				18		°C

Note 1: GBD and not production tested.

Note 2: V_{CCINT} is an internal supply generated from either BAT or PLC. Its voltage is determined by the following: If $V_{PLC} > V_{PLC_DET}$ (3V typ), V_{CCINT} = MAX (V_{BAT}, V_{PLC}). Under all other conditions, $V_{CCINT} = V_{BAT}$.

Note 3: Timing must be fast enough to prevent the IC from entering shutdown mode due to bus low for a period greater than the shutdown timer setting.

Note 4: f_{SCL} must meet the minimum clock low time plus the rise/fall times.

Note 5: The maximum t_{HD_DAT} has only to be met if the device does not stretch the low period (t_{LOW}) of the SCL signal.

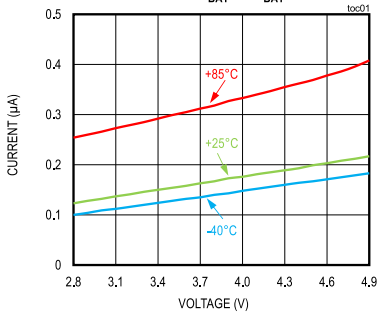
Note 6: This device internally provides a hold time of at least 100ns for the SDA signal (refer to the minimum V_{IH} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 7: Filters on SDA and SCL suppress noise spikes at the input buffers and delay the sampling instant.

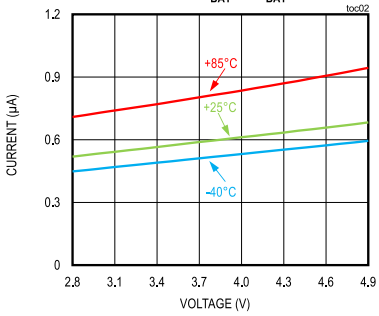
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

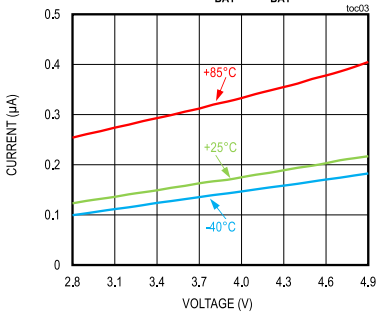
SYSUVLO I_{BAT} vs. V_{BAT}



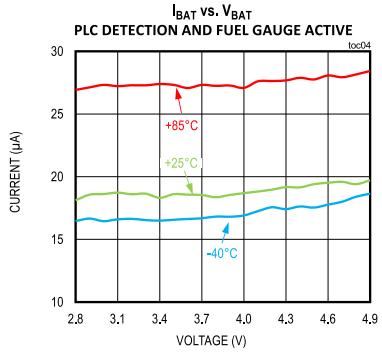
OFF MODE I_{BAT} vs. V_{BAT}



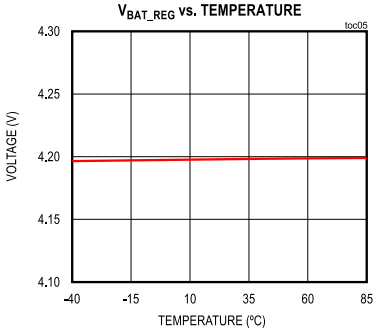
SEAL MODE I_{BAT} vs. V_{BAT}



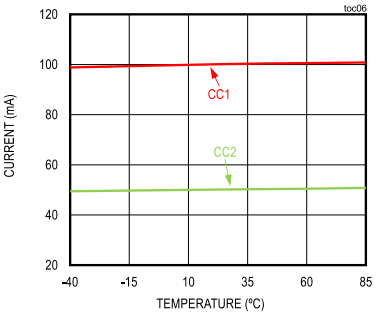
I_{BAT} vs. V_{BAT}
PLC DETECTION AND FUEL GAUGE ACTIVE



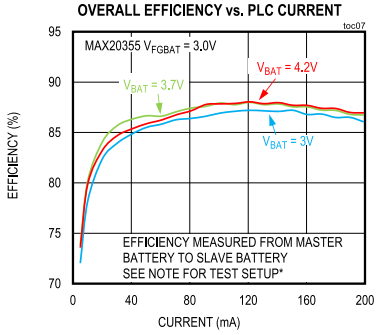
V_{BAT_REG} vs. TEMPERATURE



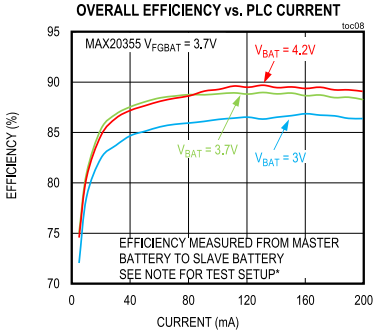
CHARGE CURRENTS vs. TEMPERATURE



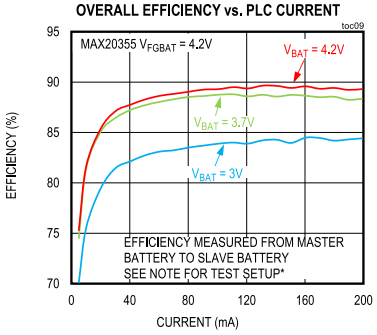
OVERALL EFFICIENCY vs. PLC CURRENT



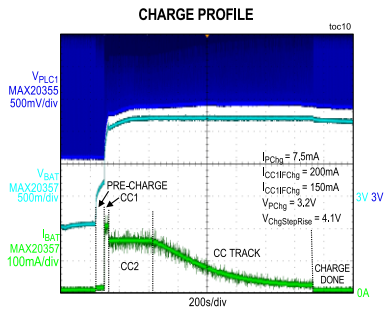
OVERALL EFFICIENCY vs. PLC CURRENT



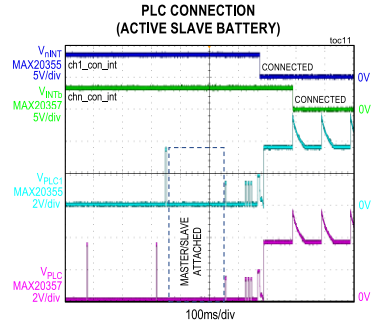
OVERALL EFFICIENCY vs. PLC CURRENT



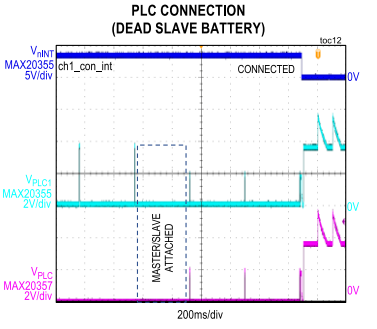
CHARGE PROFILE

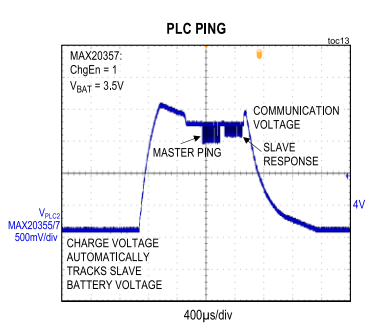


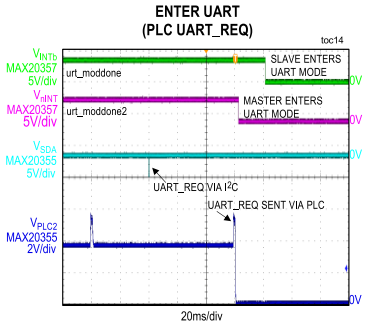
PLC CONNECTION
(ACTIVE SLAVE BATTERY)

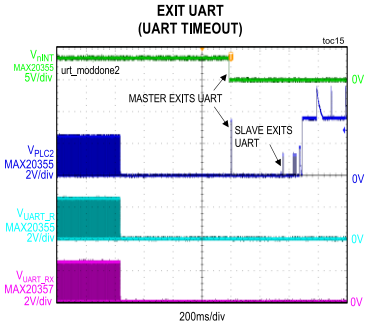


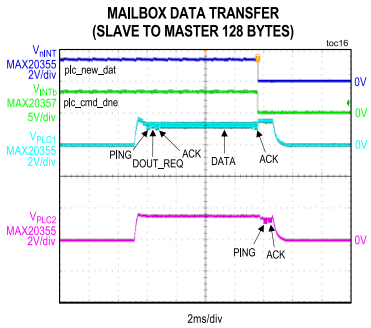
PLC CONNECTION
(DEAD SLAVE BATTERY)

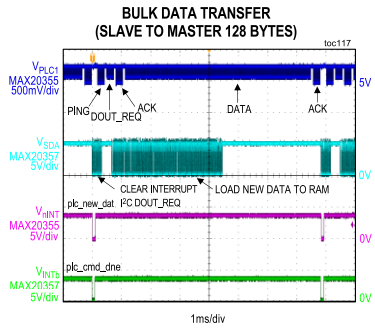


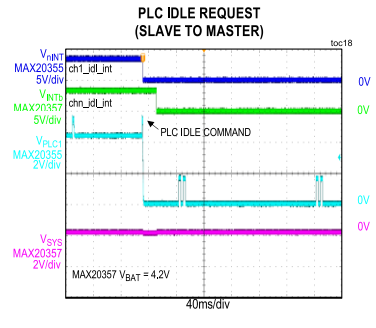


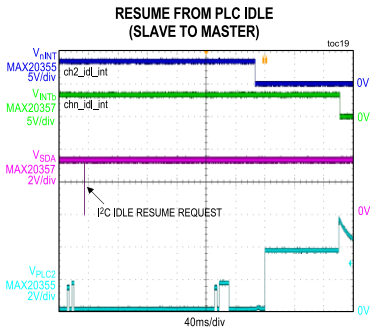


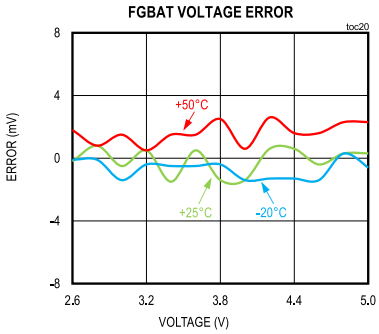


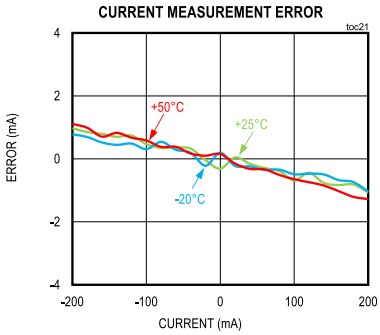










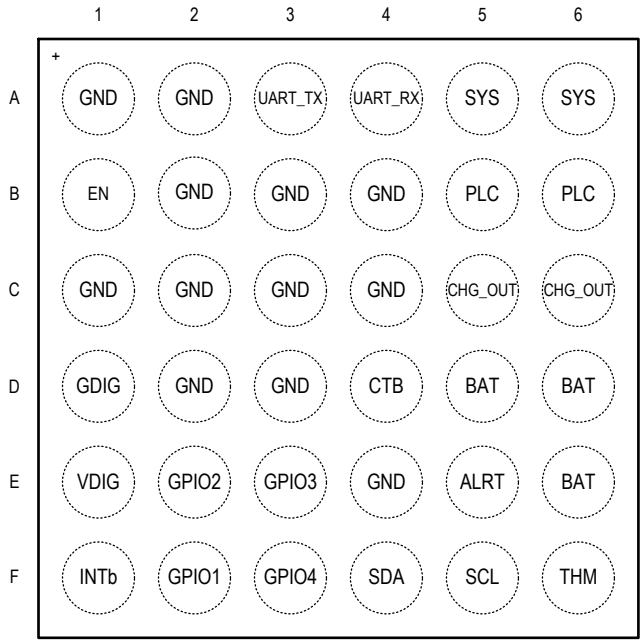


* Efficiency test setup: Test on PLC1
MAX20355: pl2_chn_ena = 0 disable PLC2
MAX20357: PLC_DROP = 100mV, PLC_HREF = 125mV, PLC_HLD = 62.5mV, VPChg = 2.7V, BatReg = 4.5V

Pin Configuration

TOP VIEW
(BUMP SIDE DOWN)

MAX20357

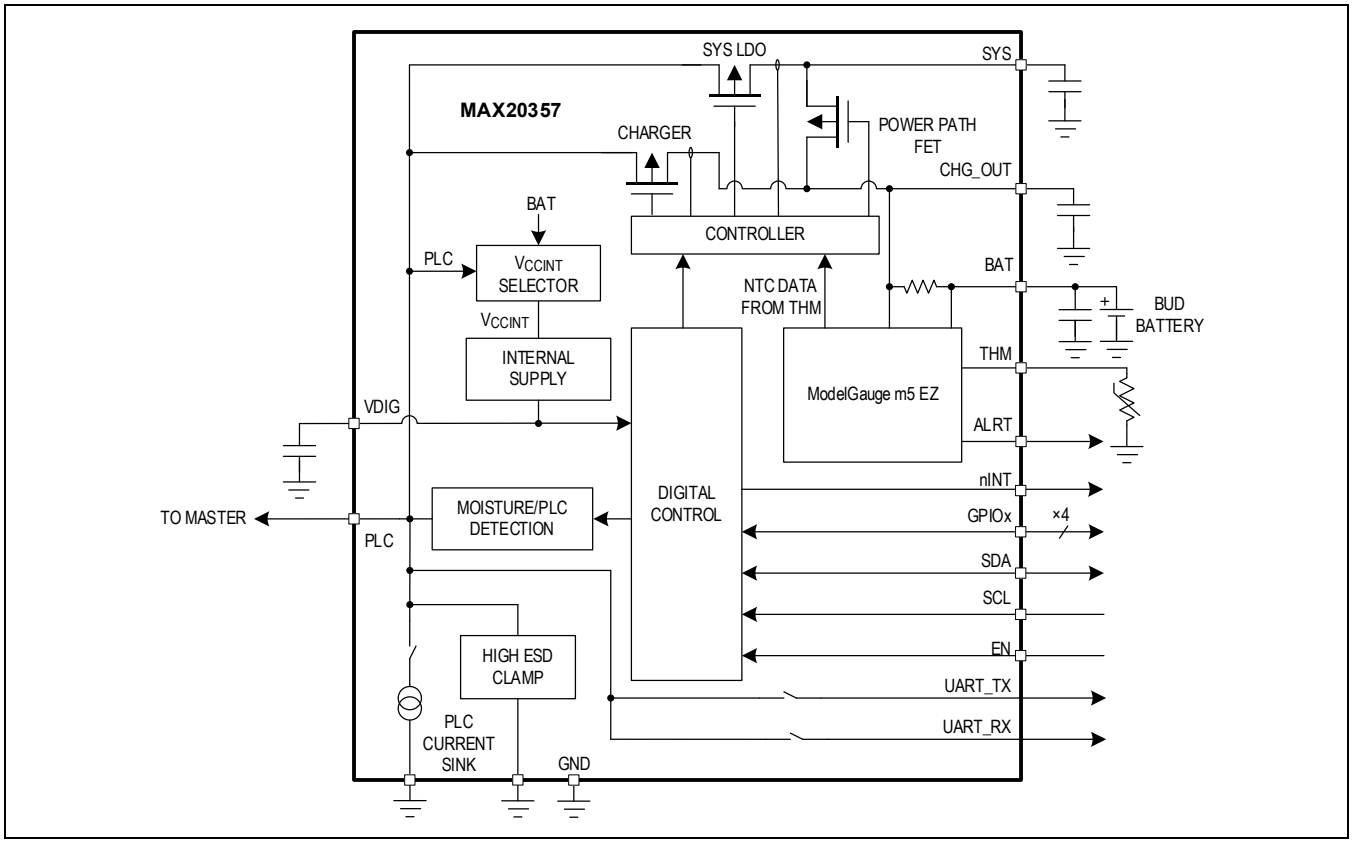


(36-BUMP WLP, 0.4mm PITCH)

Pin Descriptions

PIN	NAME	FUNCTION
A1, A2, B2, B3, B4, C1, C2, C3, C4, D2, D3, E4	GND	Ground
A3	UART_TX	Half-Duplex UART_TX
A4	UART_RX	Half-Duplex UART_RX
A5, A6	SYS	System Power Connection Monitored by the Fuel Gauge. Bypass to ground with 1µF capacitor.
B1	EN	Active High Enable Input. Drive EN low to place the device in low power shutdown mode. EN pin functionality can be disabled through I^2C.
B5, B6	PLC	Power Line Communication Slave Connection. Power input. Data input or output. Connect to master PLC1/2.
C5, C6	CHG_OUT	Charger Output. Direct path input. Internally shorted to FG_BAT through fuel gauge sense resistor. Bypass to ground with 1µF capacitor.
D1	GDIG	Digital Ground. Short to GND.
D4	CTB	Connect to BAT
D5, D6, E6	BAT	Fuel Gauge Connection to Battery. Connect to positive terminal of Li-ion battery.
E1	VDIG	Internal 1.8V Supply. Bypass with 1µF capacitor to GND.
E2	GPIO2	Programmable GPIO2. May be configured as a digital input or open drain output.
E3	GPIO3	Programmable GPIO3. May be configured as a digital input or open drain output.
E5	ALRT	Alert Output. The ALRT pin is open-drain active-low output which indicates fuel gauge alerts. Connect it to GND if not used.
F1	INTb	Open-Drain Active-Low Interrupt Output
F2	GPIO1	Programmable GPIO1. May be configured as a digital input or open drain output.
F3	GPIO4	Programmable GPIO4. May be configured as a digital input or open drain output.
F4	SDA	I^2C Serial Data
F5	SCL	I^2C Serial Clock
F6	THM	Thermistor Input. Connect thermistor between THM and GND.

Functional Diagram



Detailed Description

The MAX20355, together with the MAX20357, form an integrated Power Line Communication (PLC) and automated charging system. These devices provide a complete system solution for efficient charging and data transfer between a charging case and wireless earbuds over a single contact.

The MAX20355 and MAX20357 feature data transfers while simultaneously delivering 200mA of charge/system current per output. Both devices support a 166.7kbps bit rate while charging. With a 166.7kbps bit rate, the PLC protocol can achieve up to 130kpbs of throughput using the bulk data transfer feature. Additionally, a 4Mbaud half-duplex data-only UART mode provides an easy and fast method for firmware updates, debug interface, and factory modes. Finally, dedicated hardware PLC commands allow both devices to control GPIOs and enter various power modes, such as ultra-low current ship mode, through the PLC link.

The MAX20355 integrates a completely autonomous charging system that utilizes a 3.3W buck-boost with dynamic voltage scaling (DVS) to provide an optimized charge voltage to the earbuds. An integrated digital state machine automatically manages the dynamic voltage adjustment based on the earbud battery voltage to minimize earbud power dissipation and maximize charging efficiency.

Additional features include comprehensive earbud insertion and removal notifications, even in dead case or bud battery scenarios, and moisture detection on the PLC outputs to prevent contact corrosion. The PLC pins are protected from overcurrent events by an integrated current limiting circuit and ESD events by integrated 8kV contact-rated ESD protection structures.

Power Line Communication (PLC)

The MAX20355/MAX20357 PLC interface offers a means by which charging, and exchange of data can occur simultaneously on a single wire connection. The interface can accommodate 100kbps of throughput and can do so while delivering up to 200mA of current per channel in dual slave mode and up to 400mA in mono slave mode. The MAX20355 has an integrated current sink and resistor R_{TX} as shown in *Figure 1*. During communication, the MAX20355 utilizes the pulses generated by the PLC current sink over resistor R_{TX} to create PLC pulses on the PLC line. The MAX20355 uses PLC pulses to transfer information to the MAX20357. At the same time, the charging function is not affected. The MAX20357 uses a similar approach to create PLC pulses and transfer information over the PLC line. When there is no ongoing PLC communication, R_{TX} is shorted by a bypass switch to achieve higher overall power transfer efficiency.

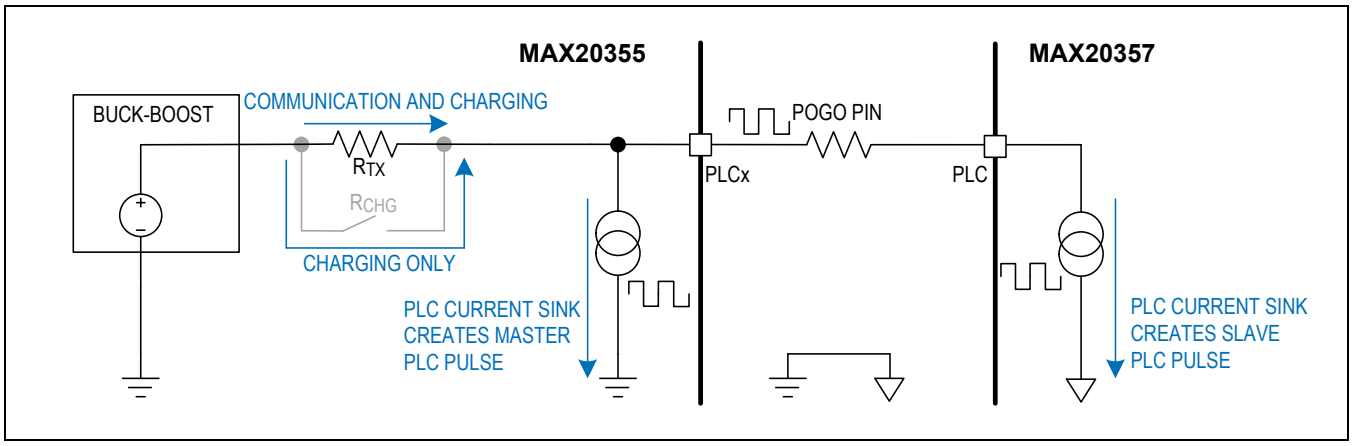


Figure 1. Simplified Scheme of Power Line Communication (PLC)

The PLC interface balances between robustness and throughput. Synchronization mechanisms and checksums offer robust data transfer, but this is also balanced against protocol overhead. With a 166.67kbps bit rate, this careful balance allows a low error rate while achieving throughput up to 130kbps in bulk data transfer mode. To overcome limitations on throughput due to the I^2C interface, the MAX20355/MAX20357 integrates two 128-byte FIFOs. This allows the system to keep I^2C overhead low utilizing bulk writes. The MAX20355 also features a 4Mbaud, data-only, half-duplex UART passthrough mode. This mode uses a simple switch that connects UART ports from master to slave for firmware updates, factory mode, and debug mode over a single PLC line.

The following sections describe the PLC PING (PLC command/mailbox data transfer), FIFO (bulk data transfer), and UART interface in detail.

PLC PING

The PLC interface between master and slave follows a master-initiated scheme. There are two data transfer types—PING and bulk data transfer. PINGs begin with a transfer from master to slave to send data across the interface, request data from the slave, offer the slave a chance to make requests, and sometimes issue commands to the slave. *Figure 2* shows the basic structure of the master to slave PING packet. Master initiates the transmission with a preamble which synchronizes the link and then transmits data. The slave responds in the same manner within a response timeout period. PLC PINGs are automatically generated and transmitted through the PLC line every telemetry period.

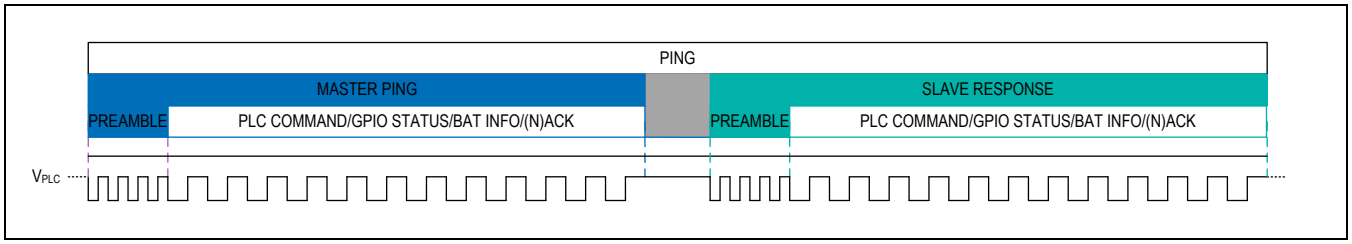


Figure 2. Periodic PING

LISTEN Command and Continuously Updated Information

Each PLC PING contains one PLC command. Most PLC commands are initiated by an I²C write from the system. However, the MAX20355 features automatic LISTEN command, which is sent periodically independent of input from the I²C interface. When there is no customer PLC command issued through I²C, LISTEN command is automatically sent through the PING, the slave has the option to send its command back to the master using its command field. In response to the master's PING, the slave sends the appropriate data based on the contents of the master PING. The contents of the command and data fields are filled according to the requirements of the command sent from the master. The periodic PING offers the following features:

1. Send master PLC command from master to slave (*Table 1*).
2. Give slave an opportunity to send slave PLC commands to master (*Table 2*).
3. Transmit GPIO status between master and slave.
4. Exchange master/slave battery information: master battery voltage, slave battery voltage, slave SoC, and slave charging status.
5. Automatic PLC voltage adjustment to track slave battery voltage and minimize power consumption. Details are described in the *Charger Battery Voltage Tracking Loop* section.
6. Automatic disconnection detection. Master detects slave is disconnected if there is no proper slave response for master PING.

The exchanged GPIO status and battery information between master and slave are ready to read from the master and slave local registers.

Master Commands

In addition to the LISTEN command, which is handled automatically, the master can execute other commands manually as well. Master's command field determines what type of transaction occurs on the PLC interface. Commands over the PLC interface are requested by I²C. *Table 1* describes the various commands master can send and what data and statuses are exchanged. Note that many commands can be sent from master to slave or from slave to master. However, it is only in response to a LISTEN command where the slave may send its commands. Master commands are initiated by writing to the plc_command1/2 and triggered by plc_run_trg1/2 through master I²C. In the command argument register plc_cmd_arg1/2, details on how the command is processed are available for the user to specify.

Table 1. Master Commands

MASTER COMMANDS	plc_command1/2	plc_cmd_arg1/2	
LISTEN	N/A	N/A	
SET_GPIO	0x3	New slave GPIO setting	
DOUT_REQ	0x5	Number of bytes (up to 128 bytes)	
UART_REQ	0x6	slave_uart_sw[1:0]	
SYST_REQ	0x0	0x00	SEAL request. Puts slave in SEAL mode.
		0x01	Soft reset request. Resets slave's registers.
		0x02	Hard reset request. Cycle the power on the slave's SYS node.
		0x03	Fuel gauge reset request. Resets fuel gauge block.
		0x04	FIFO request. Puts system into bulk data transfer mode.
		0x05	Free request. Stop bulk data transfer and free the data line.
		0x06	IDLE mode request. Sends system into PLC IDLE mode.
		0x07	Hard + Soft reset request. Reset all registers, FSM and cycle the power at SYS.
		{0x3F, slave_uart_tx, slave_uart_rx}	UBOOT request. Hard resets slave and puts slave in UART mode.

Slave Commands

The slave can also issue commands to the master. The slave similarly issues the commands based on I2C input, but it must wait for a master LISTEN command before the command can be sent back to the master. Once the LISTEN command is received, the slave then sends its command using the COMMAND field. *Figure 3* shows the method by which the slave can send a command. Slave commands are initiated with a write to plc_command and triggered by plc_run_trg through master I2C. In the command argument register plc_cmd_arg, details on how to process the PLC commands are available for the user to specify.

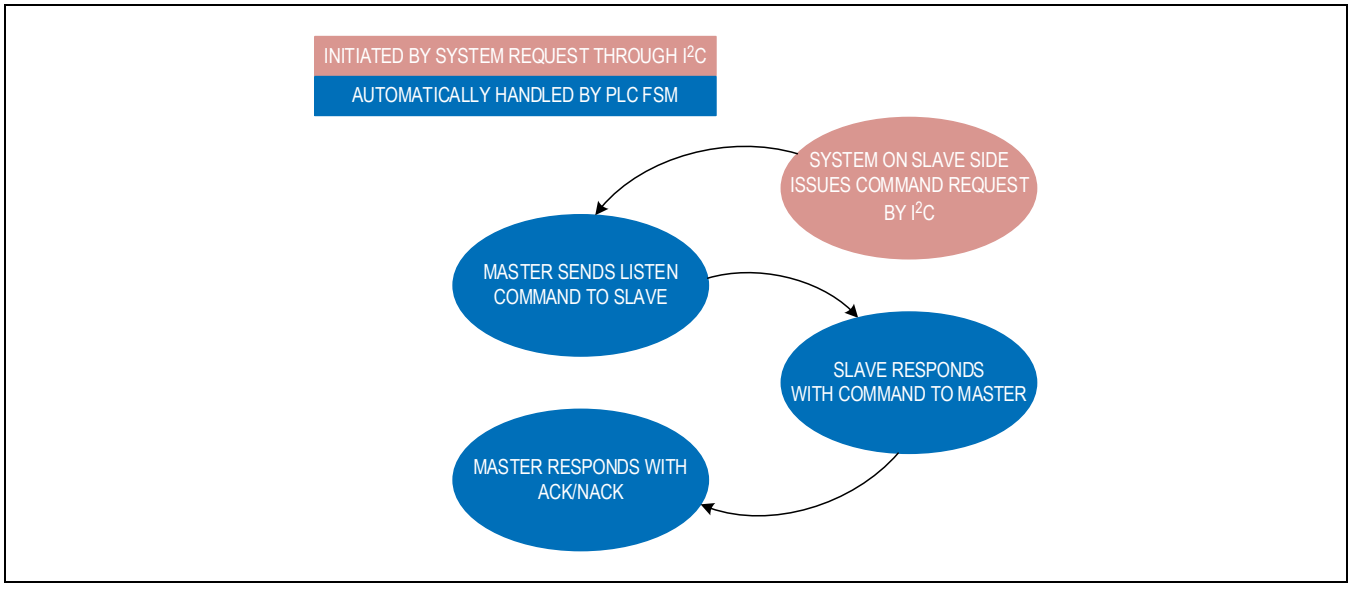


Figure 3. Sending Commands from the Slave

Table 2. Slave Commands

SLAVE COMMAND*	plc_command	plc_cmd_arg (DATA)	
SET_GPIO	0x3	New master GPIO setting	
DOUT_REQ	0x5	Number of bytes (up to 128 bytes)	
UART_REQ	0x6	master_uart_sw[3:0]	
SYST_REQ	0x0	0x01	Soft reset request. Resets master's registers.
		0x03	Fuel gauge reset request. Resets master's fuel gauge block.
		0x04	FIFO request. Puts master and slave into bulk data transfer mode.
		0x05	Free request. Stop bulk data transfer and free the data line.
		0x06	Idle mode request. Sends master into idle mode.

**Always sent in response to the "LISTEN" command from the master shown in Table 1.*

Mailbox Data Transfer (DOUT_REQ)

From Master to Slave

Mailbox data transfers are used to exchange one data packet, up to 128 bytes, from master to slave. A mailbox data transfer begins with a data out request (DOUT_REQ) master command. Fill the data packet into the master RAM, write the number of bytes to be transferred in the command argument field plc_cmd_arg1/2, then trigger the DOUT_REQ command. If slave responds ACK to DOUT_REQ command, data in RAM is transferred to slave automatically. After slave successfully receives data, plc_new_dat interrupt is asserted and RAM_is_full is set to 1. Once RAM_is_full is set to 1, slave RAM is protected from PLC and it sends NACK to master's DOUT_REQ command until RAM_is_full is write cleared. Make sure to read data in RAM before clearing RAM_is_full to avoid data loss. Note that although both PLC devices have two integrated 128-byte RAMs, only one RAM is used in mailbox data transfer. *Figure 4* shows the flow of data during a master to slave write.

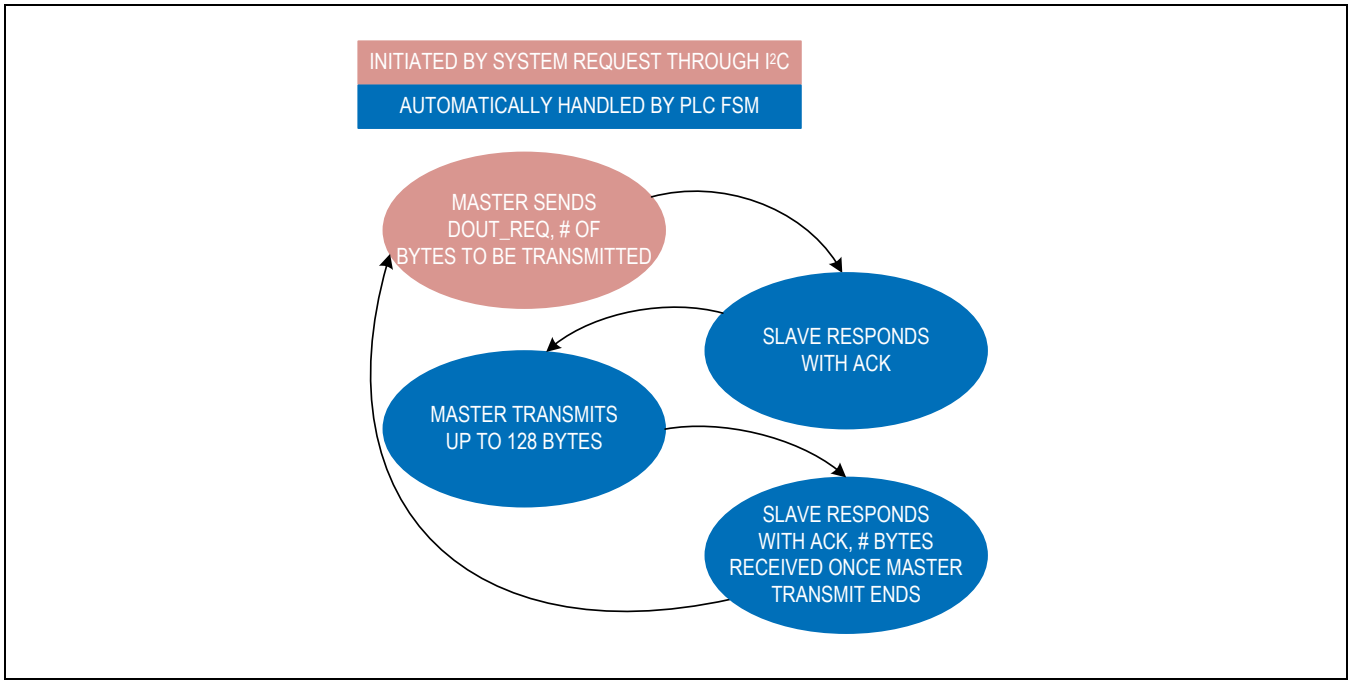


Figure 4. Master to Slave Mailbox Data Transfer

From Slave to Master

A similar scheme is used to send a packet of data, up to 128 bytes, from slave to master. A mailbox data transfer begins with a data out request (DOUT_REQ) slave command. Write the number of bytes to be transferred in the command argument field plc_cmd_arg. Fill the data packet into the slave RAM, write the number of bytes to be transferred in the command argument field plc_cmd_arg, then trigger the DOUT_REQ command. Since the system follows master initiated scheme, the slave triggers the DOUT_REQ command when it receives the master Listen command. After the master receives DOUT_REQ and responds to ACK, data in RAM is transferred to the slave automatically. After master successfully receives data, plc_new_dat interrupt is asserted and RAM_is_full is set to 1. Once RAM_is_full is set to 1, master RAM is protected from PLC, and it sends NACK to slave's DOUT_REQ command until RAM_is_full is write cleared. Make sure to read data in RAM before clearing RAM_is_full to avoid data loss. Note that although both PLC devices have two integrated 128-byte RAMs, only one RAM is used in mailbox data transfer. *Figure 5* shows the flow of data during a slave to master write.

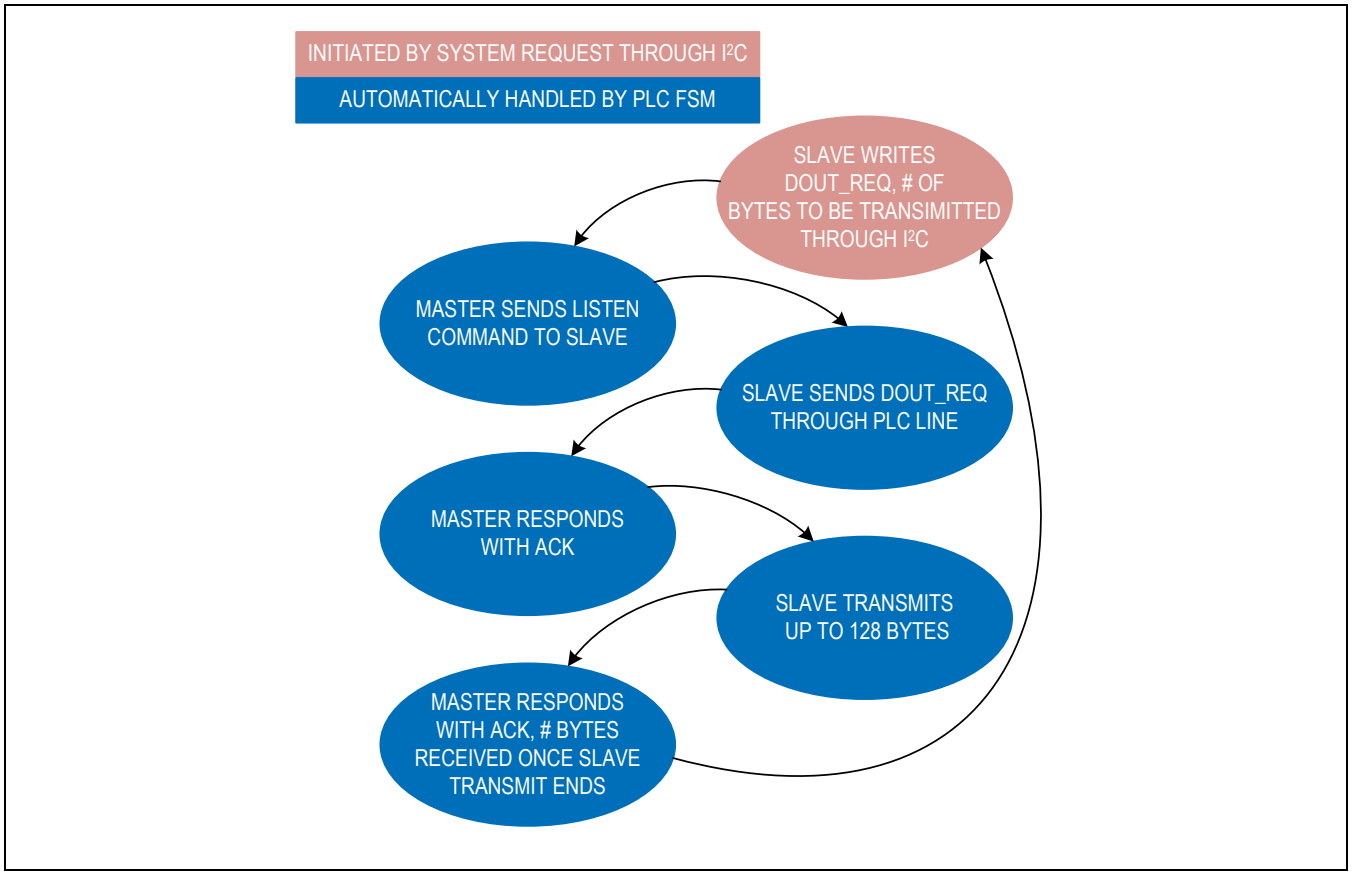


Figure 5. Slave to Master Mailbox Data Transfer

Bulk Data Transfer (FIFO)

To minimize the impact of I²C protocol overhead on the achievable throughput, the MAX20355 and MAX20357 integrate two 128-byte RAMs for bulk data transfer. The bulk data transfer scheme is shown in *Figure 6*. The I²C bus connects first to the RAM_1 to load data with I²C bulk writes at data rates up to 400kbps. Once the DOUT_REQ command is triggered, the I²C bus and PLC line are swapped, I²C bus from RAM_1 to RAM_2 and PLC from RAM_2 to RAM_1. While RAM_1 is being emptied by the PLC engine, the next set of data can be loaded by I²C bulk write again into the RAM_2. An interrupt is sent to the system after RAM_1 is completely emptied. Repeat the same process to swap the I²C bus and PLC back and forth to load and transmit data simultaneously. Similar implementation on receiving side swaps I²C bus and PLC back and forth to receive and read data to receiver's microcontroller. Dual-RAM architecture reduces I²C protocol overhead and enhances achievable throughput. Packets of any size up to 128 bytes can be sent by this method.

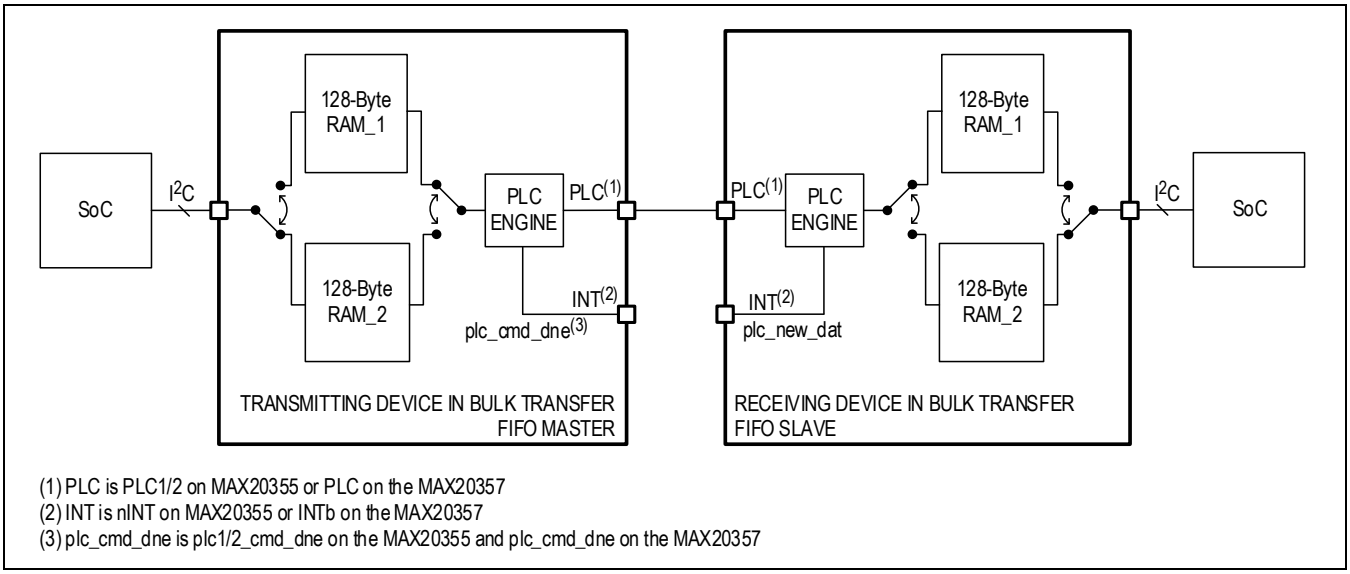


Figure 6. Bulk Data Transfer Implementation

From Master to Slave

Bulk data transfers from master to slave begin with a system request (SYST_REQ) master command. In the command argument of SYST_REQ, the master needs to send a FIFO request. Once receiving an ACK from the slave, PLC voltage is pulled up to communication voltage and the PLC line is locked for bulk data transfer. Before triggering the data transfer, the data packet needs to be filled into the master RAM through I2C. Similar to mailbox data transfer, write the number of bytes to be transferred to plc_cmd_trg1/2, then trigger the DOUT_REQ command and wait for plc1/2_cmd_dne interrupt. Repeat DOUT_REQ and wait for plc1/2_cmd_dne to interrupt multiple times as needed. After all data packets are transferred, issue a FREE request from the master side to unlock the line and return to normal PLC mode. Note that master bulk data transfer is designed to transfer data only from master to slave. *Figure 7* shows the flow of data during a master to slave write.

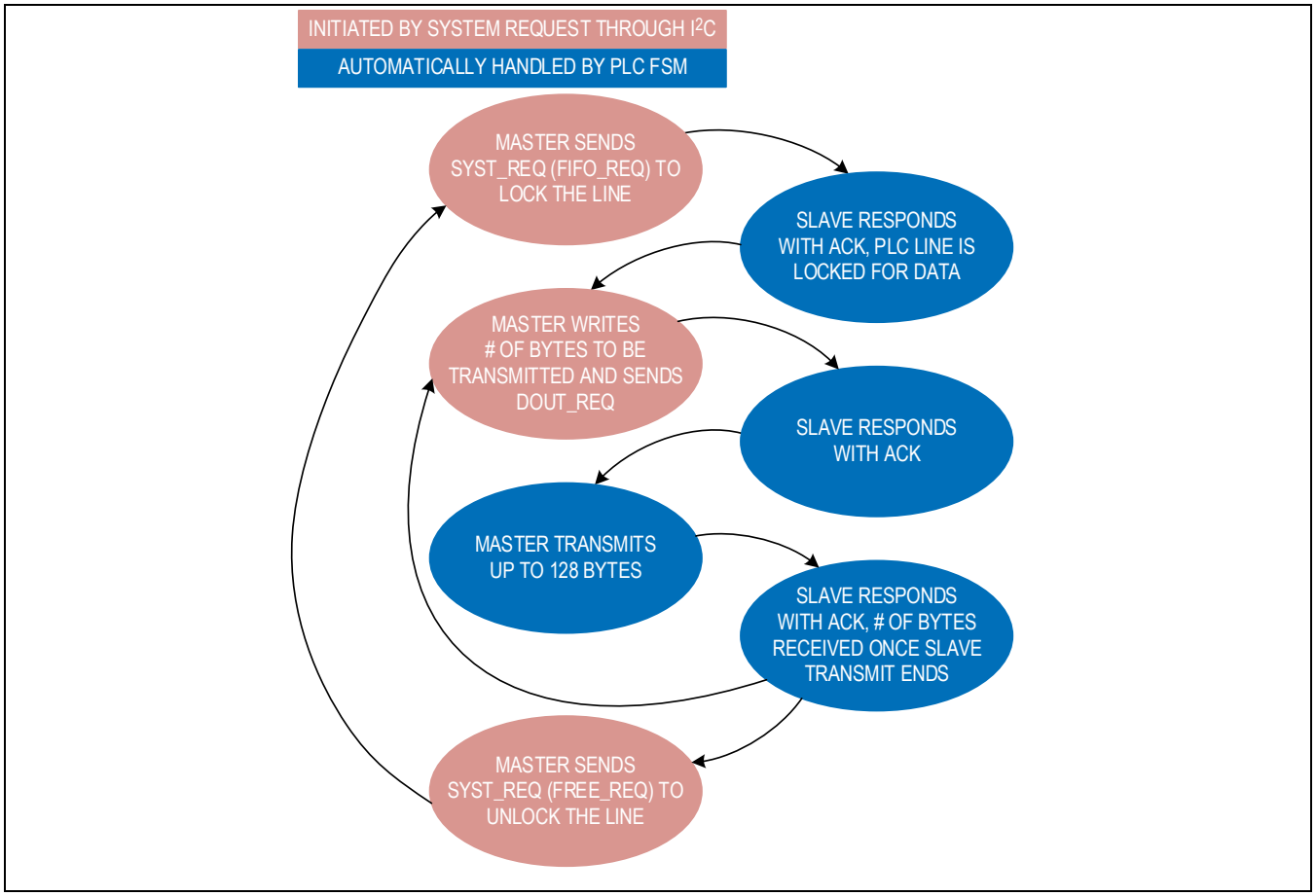


Figure 7. Master to Slave Bulk Data Transfer

From Slave to Master

Bulk data transfers from slave to master begin with a system request (SYST_REQ) slave command. In the command argument of SYST_REQ, the slave needs to write a FIFO request. The slave waits until the master's LISTEN command to send out a FIFO request through the PLC line. Once receiving an ACK from the master, the master locks the PLC line and enters bulk data transfer mode. Before triggering the data transfer, the data packet needs to be filled into the slave RAM. Similar to mailbox data transfer, write the number of bytes to be transferred to plc_cmd_arg, then trigger the DOUT_REQ command and wait for plc_cmd_dne interrupt. Repeat DOUT_REQ and wait for plc_cmd_dne to interrupt multiple times as needed. After all data packets are transferred, issue a FREE request from the slave side to unlock the line and return to normal PLC mode. Note that slave bulk data transfer is designed to transfer data only from slave to master. *Figure 8* shows the flow of data during a slave to master write.

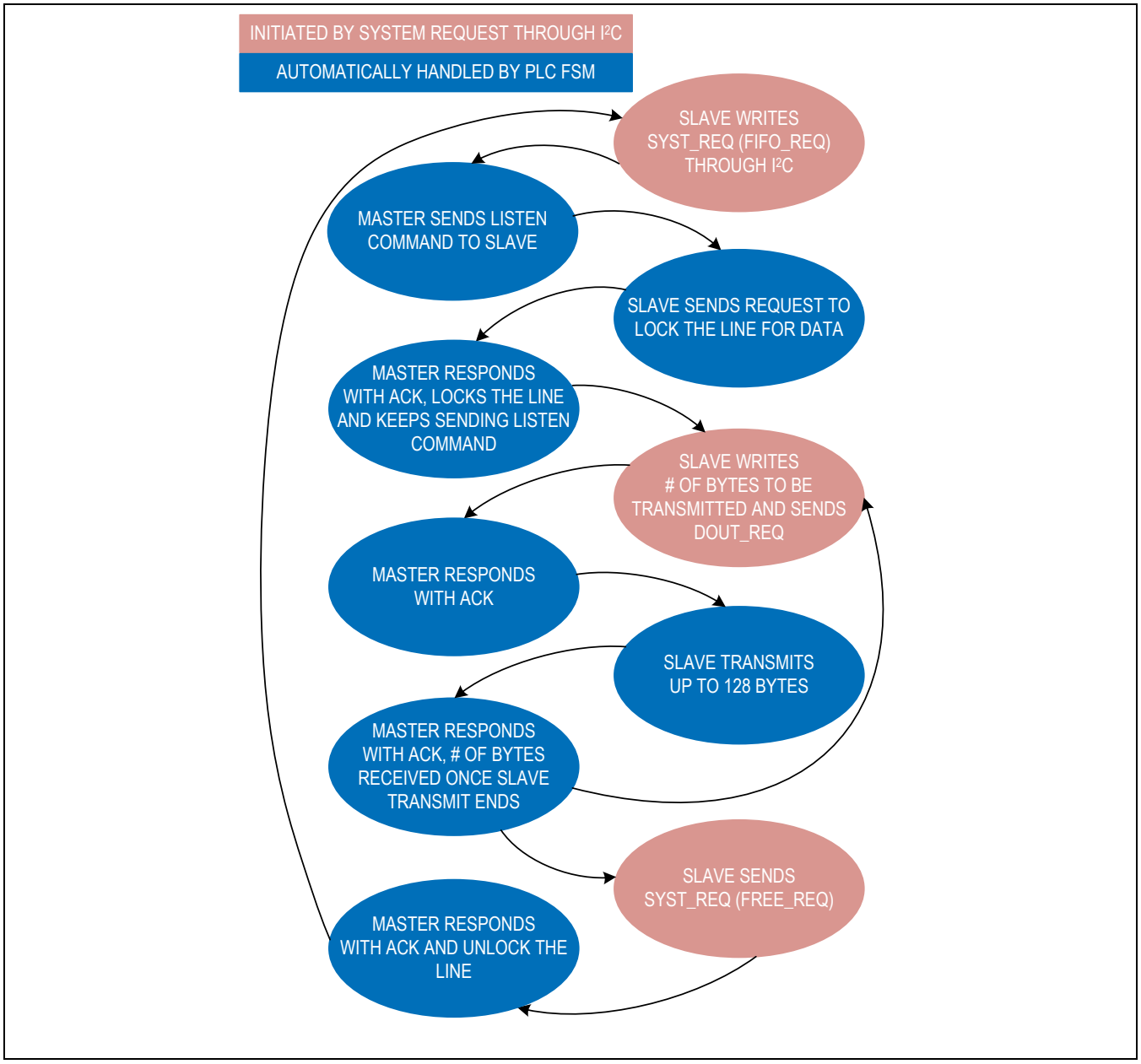


Figure 8. Slave to Master Bulk Data Transfer

Half-Duplex UART Passthrough Interface

The MAX20355 and MAX20357 feature a 4Mbaud, data-only, half-duplex UART passthrough mode. This mode is a simple switch that connects either the TX or RX for firmware updates, factory mode, and debug mode over the single PLC line. A UART command can be sent through the PLC interface to send either device into UART mode in a particular configuration. Internal switches allow the user to separate UART TX and UART RX. The configuration can be seen in *Figure 9*. The user can use the I2C command to switch roles from TX to RX or vice versa on master and slave. The slave provides one additional feature to detect incoming data automatically through its UART_RX pin. In this mode, once the slave enters UART mode, it closes its UART_TX switch by default. Once it detects a rising/falling edge on its UART_RX pin from the slave microcontroller, it toggles the switch from UART_TX to UART_RX automatically. After the data transfer is completed in receiving direction, switch toggles back from UART_RX to UART_TX automatically after a programmable blanking time. This feature allows the user to send and receive data through UART when the slave I2C is not available.

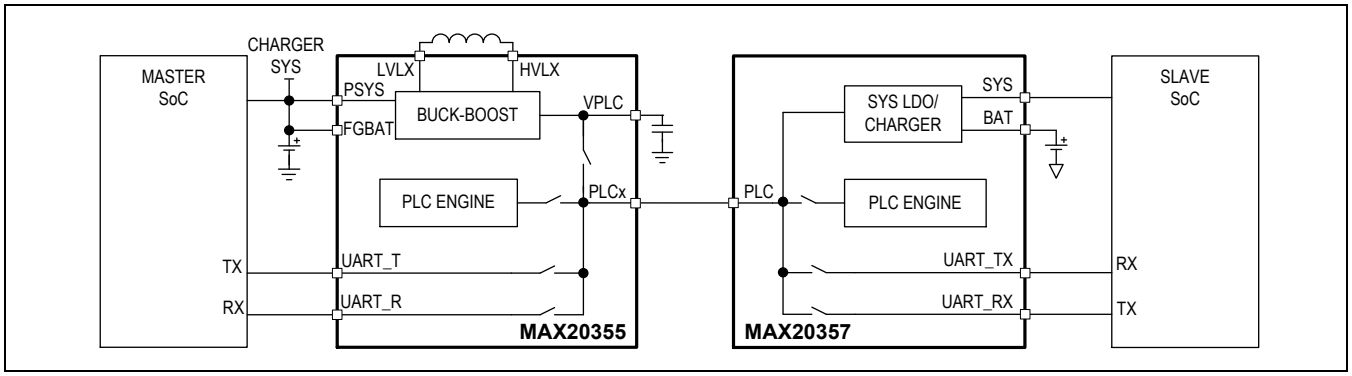


Figure 9. UART Interface

From Master to Slave

The master can put the slave into UART mode by using the UART_REQ master command. The direction of UART communication is set in the command argument. Corresponding master and slave switches are closed once the UART command is successfully triggered. The switch settings are shown in *Table 3*. If the user wants to control UART switches manually in UART mode, all the master/slave UART switch settings can be changed through I2C.

Table 3. UART Switch Settings in Master PLC Command Argument

slave_uart_sw[1:0]	MASTER UART_T	MASTER UART_R	SLAVE UART_TX	SLAVE UART_RX
0b00	x	x	x	x
0b01	x	√	x	√
0b10	√	x	√	x
0b11	√	√	√	√

"√" represents the switch is ON and "x" represents the switch is OFF

From Slave to Master

The slave can put the master into UART mode by using the UART_REQ slave command. Corresponding master switches are closed once the UART command is successfully triggered. The switch settings are shown in *Table 4*. No slave switch is closed after UART_REQ. The slave UART_TX and UART_RX switches need to be closed through the slave I2C write. If the user wants to control UART switches manually in UART mode, all the master/slave UART switch settings can be changed through the master/slave I2C.

Table 4. UART Switch Settings in Slave PLC Command Argument

master_uart_sw[3:0]	MASTER PLC2 UART_T	MASTER PLC2 UART_R	MASTER PLC1 UART_T	MASTER PLC1 UART_R
0b0000	x	x	x	x
0b0001	x	x	x	√
0b0010	x	x	√	x
0b0011	x	x	√	√
0b0100	x	√	x	x
0b1000	√	x	x	x
0b1100	√	√	x	x

"√" represents the switch is ON and "x" represents the switch is OFF

Exit UART Mode

There are two ways to quit UART mode: 1. Master/slave can quit UART mode by disabling UART mode and disconnecting the UART switch through the master/slave I2C; 2. Use master and slave UART timeout counter and wait for UART timeout interrupt. Enable timeout counter through tmo_tmr_ena1/2 on master and tmo_tmr_ena on slave before entering UART mode. Once the TX/RX line is idle for 0.5s, the slave turns off its UART switch, disconnect UART_TX or UART_RX from the PLC line and start a counter to count for 0.6s. After a 0.6s delay, the slave exits UART mode, connects the PLC line to the PLC engine, and returns to the PLC detection mode. Meanwhile, once the line is idle for 0.75s, the master turns off

its UART switch, disconnects UART_T or UART_R from the PLC line, connects to the PLC engine, and returns to the PLC detection mode. Note that once the slave disconnects its UART switch at time point 0.5s, it enters an automatic UART exit process and this process is irreversible. It is not allowed to send data from master through UART after time point 0.5s. If data resumes from the master between time point 0.5s and 0.75s, the master UART timeout counter is cleared, and it holds the master in UART mode for another 0.75s. This causes an issue because the slave exits UART mode at time point 1.1s and starts to send PLC detection pulse immediately. If master is still in UART mode after slave exits UART mode, slave's PLC detection pulse may hold master in UART mode.

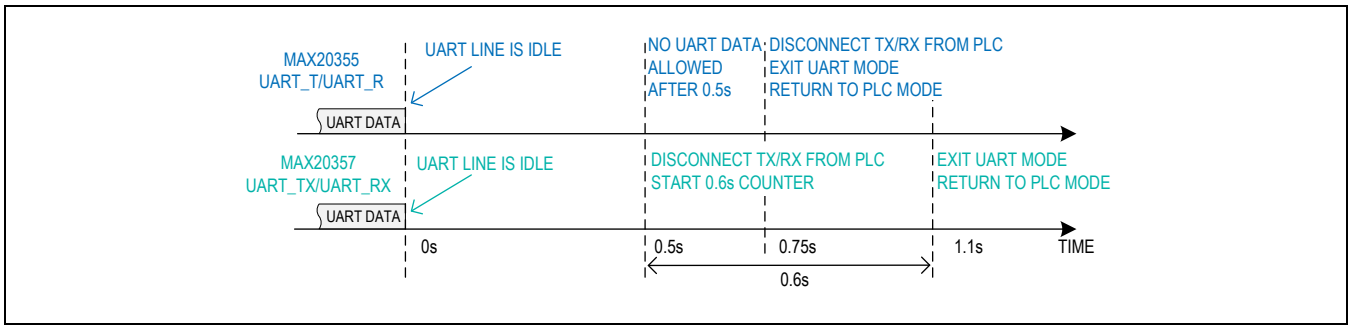


Figure 10. UART Automatic Exit Through UART Timeout

Autonomous Optimized Battery Charging

The MAX20355 interacts with MAX20357 to create an autonomous, closed-loop battery voltage tracking charging system. This system utilizes a dynamic voltage scaling (DVS) buck-boost on the MAX20355 in conjunction with an ultra-low dropout charger (ULDO) on the MAX20357. The PLC interface closes the loop allowing the buck-boost to adjust its output voltage to accommodate the minimum required headroom on the charger. This method allows for excellent 90% efficient energy transfer from the case battery to the earbud battery without the need to place bulky inductors on the tiny form factor ear buds. The excellent efficiency and extremely low heat generation of this charging system offer an increase in the number of charging cycles that can be supported by the case battery as well as the option to increase the rate of charge and deliver faster recharge times to the end customer.

Charger Battery Voltage Tracking Loop

Figure 11 shows the structure of the automatic charger battery voltage tracking algorithm. The charger battery voltage tracking algorithm is accomplished with data exchanges initiated by the master and responded to by the slave(s). Once the connection is built between master and slave(s), the master connects the buck-boost regulator to the PLC line and holds PLC voltage to bb_vlt__def (3.5V by default) for 100ms. Then pull PLC line to communication voltage (5.5V by default) and starts to PING. The communication voltage is programmable through bb_vlt_tran. Slave responds with ACK packet after master sends the first LISTEN command during PING. Slave's ACK packet contains information including slave GPIO status, battery information, charging status, and PLC voltage up/down request. Master adjusts buck-boost output based on the PLC voltage up/down request received from slave(s).

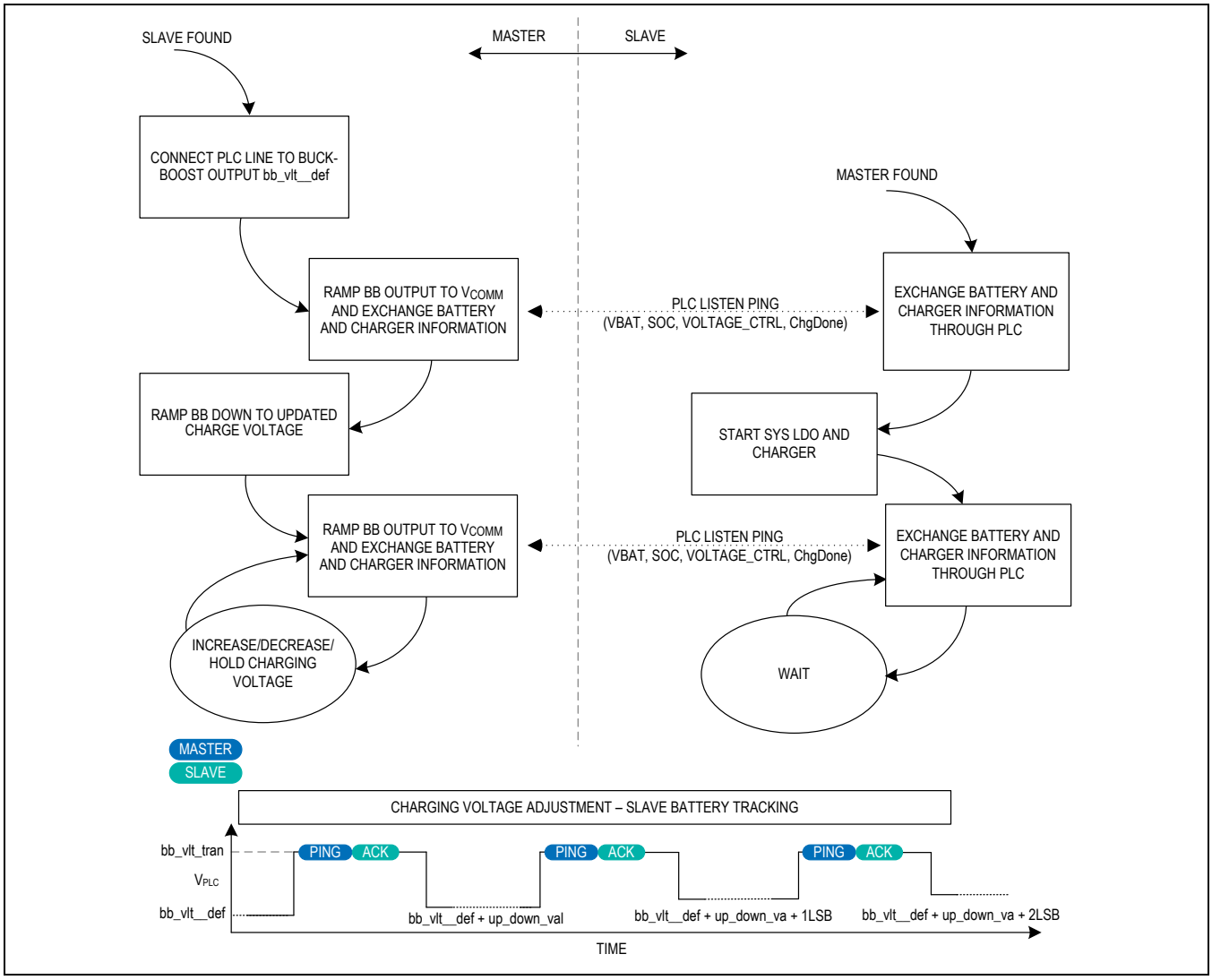


Figure 11. Polling Structure of Automatic Charging Algorithm

Slave compares battery voltage with PLC line voltage. If the PLC input voltage is above the programmed upper threshold (PLC voltage is in decrease zone), the slave sends a “decrease” signal during PING. Similarly, if PLC voltage is below the lower limit (increase zone) or within the limit (hold zone), it sends an “increase” or “hold” signal accordingly. The voltage thresholds are fully programmable through the parameters shown in *Figure 12*. The minimum step of voltage adjustment is programmable through I^2C register bits up_down_val.

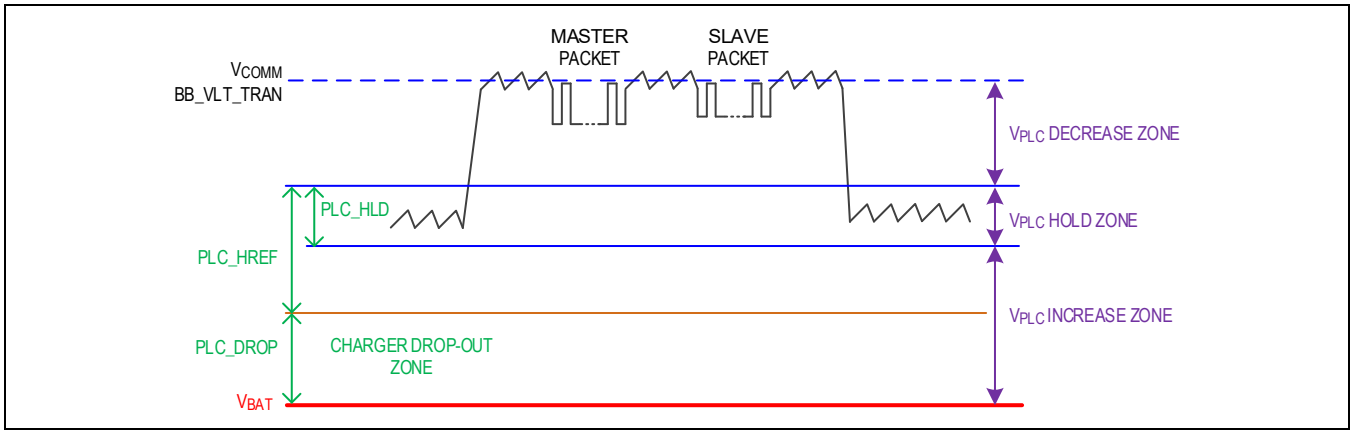


Figure 12. Slave Voltage Control Algorithm

Ultra-Low Dropout Battery Charger

The battery charger on MAX20357 is a fully featured lithium-ion charger offering I²C programmable voltage thresholds through charging phases: precharge voltage VPChg, step charging voltage ChgStepRise, charge termination voltage BatReg, and top off current IChgDone. The MAX20357 also features safety timers, JEITA charging profile with thermistor and overtemperature protection with die temperature sensor. It starts charging from the precharge stage if battery voltage is lower than precharge voltage VPChg. Step charging feature allows higher charge rate at the beginning of the charge cycle during CC1. Once the battery voltage rises to step charge threshold ChgStepRise, the charger transitions to CC2 at a lower charge rate. If the battery voltage is charged up close to BatReg, there are two options to charge in final stage: CC track mode and CV mode. In CC track mode, charger current is regulated and reduced by fixed step as battery charges up. In CV mode, BAT pin voltage is regulated at BatReg and charging current naturally reduces as battery charges up. As shown in *Figure 13*, in CC track mode, charger current is evaluated roughly every 1.3ms, if charge current hits natural charge current controlled by CV mode (dash line in *Figure 13*), the MAX20357 reduces charge current by 1/64 of CC2IFChg. Charger controls current directly in CC track mode, which prevents potential abrupt current change that is common in CV mode. The PLC line is protected from fluctuation of charger current which could lead to communication failure. CC track feature is enabled by default. It is highly recommended to keep the default setting to maintain a clean PLC line for reliable PLC communication.

The charging current options for precharge, CC1 and CC2 can be found in IPChg, CC1IFChg, and CC2IFChg. The voltage threshold from precharge to CC1, from CC1 to CC2, and charge termination voltage can be found in VPChg, ChgStepRise, and BatReg. The top-off current threshold can be found in IChgDone. The step charging profile is shown in *Figure 13*.

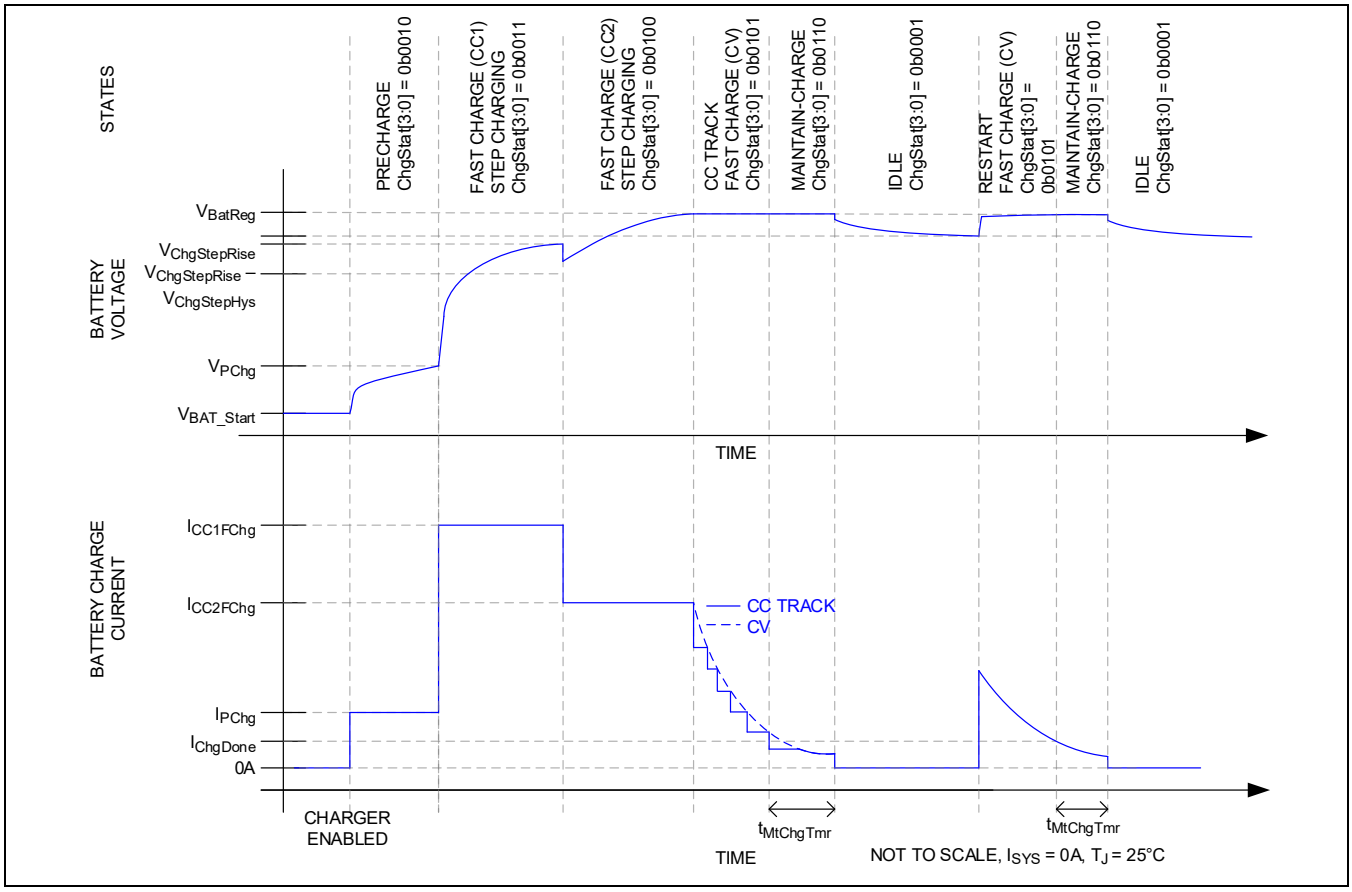


Figure 13. Step Charging Profile

There are also independently programmable temperature thresholds, which allow the user to select in which temperature ranges precharge, CC1, CC2 and battery regulation voltage may operate. Different JEITA compliant temperature operation strategy is I^2C programmable. Timeout function for precharge, CC1 and full charge cycle is also designed to prevent overcharge of the battery. Detailed charger operation is shown in *Figure 14*.

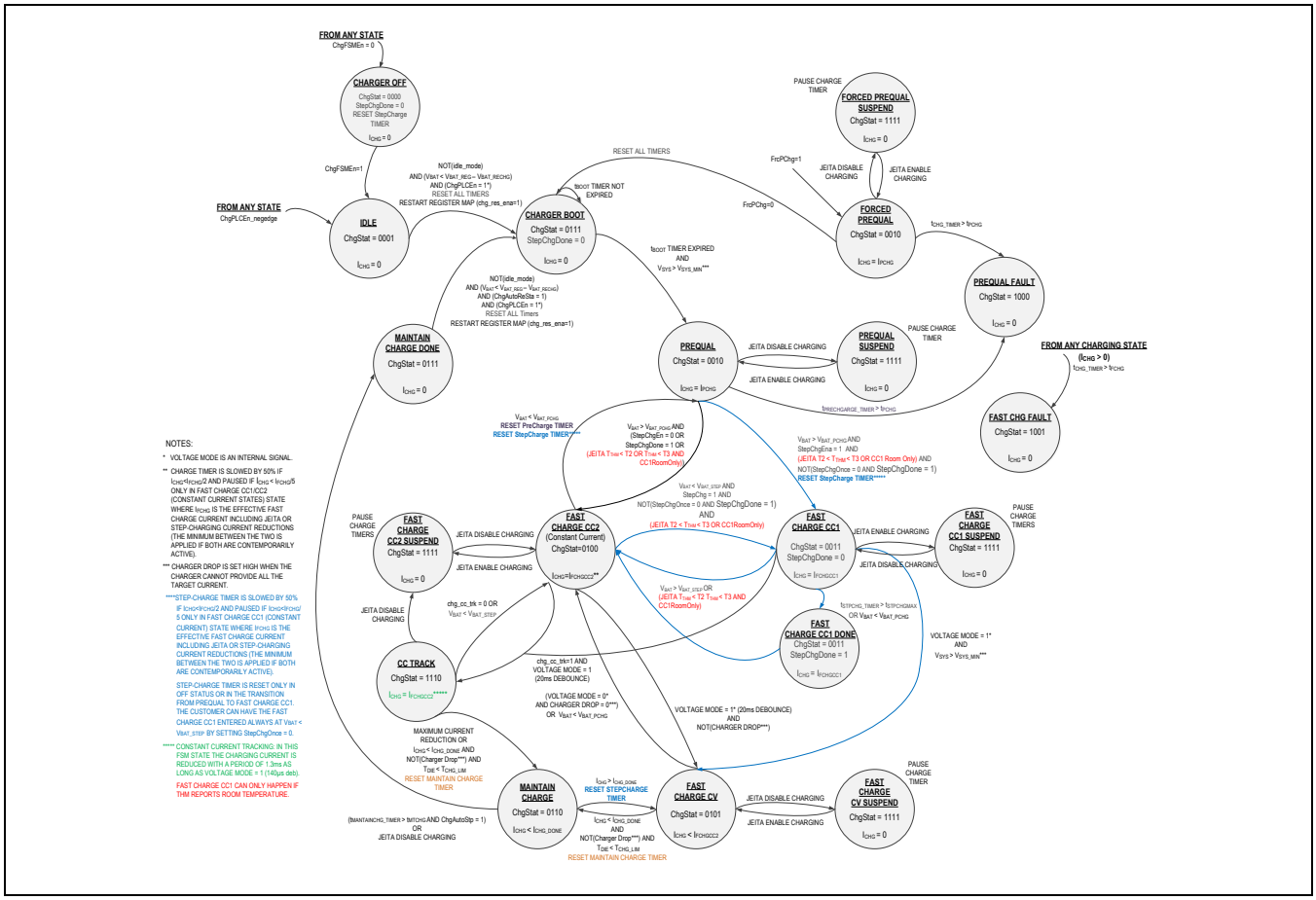


Figure 14. Battery Charger FSM Diagram

Charger-Off State

As shown in *Figure 14*, when PLC connection is not established, power is not applied from the MAX20355. The MAX20357 charger is in **Charger Off** state (ChgStat = 0b0000). After MAX20357 detects PLC connection, buck-boost voltage is applied to PLC pin, chn_con_sts status is set to 1 and chn_con_int interrupt is asserted at the first telemetry PING, signaling PLC connection is established. Charger transitions from **Charger Off** state to **Charger IDLE** state (ChgStat = 0b0001).

Charger IDLE state

As shown in *Figure 14*, the following events cause the charger to enter **Charger IDLE** state.

- PLC connection event. The charger transitions from **Charger Off** state to **Charger IDLE** state when the MAX20357 detects a PLC connection event.
- Disable charger when power is applied to PLC pin. If power is applied to PLC pin, the charger enters **Charger IDLE** state when charger is disabled ChgEn = 0.

The charger exits **Charger IDLE** state and starts boot sequence when all the following conditions are met:

- System is not in PLC IDLE mode. System could be put into PLC IDLE mode to reduce power dissipation after earbud battery is fully charged. In PLC IDLE mode, if charger is enabled ChgEn = 1 and charger auto-restart is enabled (ChgAutoReSta = 1), the system resumes from PLC IDLE mode automatically when battery voltage drops below recharge threshold BatReg – BatReChg.
- Charger is enabled ChgEn = 1.
- Battery voltage < BatReg – BatReChg (recharge threshold).

When the charger enters **Charger Boot** state, all charger timers reset. If chg_res_ena = 1, charger resets all charger-related registers when it goes through boot sequence.

Charger IDLE state

As shown in *Figure 14*, the following events cause the charger to enter **Charger IDLE** state.

- PLC connection event. The charger transitions from **Charger Off** state to **Charger IDLE** state when the MAX20357 detects a PLC connection event.
- Disable charger when power is applied to PLC pin. If power is applied to PLC pin, the charger enters **Charger IDLE** state when charger is disabled ChgEn = 0.

The charger exits **Charger IDLE** state and starts boot sequence when all the following conditions are met:

- System is not in PLC IDLE mode. System could be put into PLC IDLE mode to reduce power dissipation after earbud battery is fully charged. In PLC IDLE mode, if charger is enabled ChgEn = 1 and charger auto-restart is enabled (ChgAutoReSta = 1), the system resumes from PLC IDLE mode automatically when battery voltage drops below recharge threshold BatReg – BatReChg.
- Charger is enabled ChgEn = 1.
- Battery voltage < BatReg – BatReChg (recharge threshold) or skipCRFStart is set to 1.

When the charger enters **Charger Boot** state, all charger timers reset. If chg_res_ena = 1, charger resets all charger-related registers when it goes through boot sequence.

Precharge State

As shown in *Figure 14*, the charger enters the precharge state (ChgStat = 0b0010) after charger boot sequence is completed and SYS pin voltage is regulated higher than or equal to minimum system voltage SysMin. If battery voltage is lower than VPChg or FrcPChg = 1, the charger remains in precharge state. In the precharge state, the battery charging current is IPChg.

The following events cause the charger to exit precharge state:

- Battery voltage rises above VPChg. If step-charging is enabled CC1Enable = 1, CC1 is not configured to run at room temperature only CC1RoomOnly = 0, or CC1 is configured to run at room temperature only CC1RoomOnly = 1 and the thermistor monitoring reports room temperature, the charger enters **Fast-Charge Constant Current Mode 1** (CC1) state. By default, step-charging is enabled CC1Enable = 1 and CC1 is configured to run at any temperature CC1RoomOnly = 0.
- Battery voltage rises above VPChg. If step-charging is disabled CC1Enable = 0, or CC1Enable = 1 and CC1 is configured to run at room temperature only CC1RoomOnly = 1 but battery is in cool or warm temperature zone, the charger enters **Fast-Charge Constant Current Mode 2** (CC2) state.
- Precharge timeout. If the charger remains in this state for longer than the charger precharge timer PChgTmr, the charger enters **Charger Fault-Precharge Timer PChgTmr Expired** state (ChgStat = 0b1000) and suspends charging.
- Charger safety timeout. If the charger safety timer ChgTmr expires while in precharge state, the charger enters **Charger Fault-Safety Timer ChgTmr Expired** state (ChgStat = 0b1001) and suspends charging.
- JEITA disable charging. The charger suspends charging due to temperature. See the *JEITA compliance* section for detailed description.
- Forced precharge. Charger can be forced to operate with precharge current IPChg in **Force precharge** state by setting FrcPChg = 1. The charger transitions to the charger boot sequence when disable forced precharge FrcPChg = 0.

Fast-Charge Constant Current CC1 State

Once the battery voltage rises above precharge threshold VPChg, the charger allows a higher charge rate CC1IFChg at the beginning of the charge cycle during **Fast-Charge Constant Current Mode 1** (CC1) state. Set register bit CC1Enable = 0 to disable the Step-charging feature, and the Charger transits from **precharge** state directly to **CC2** state. In the JEITA compliant thermistor temperature monitoring control, CC1 can be configured to run at room temperature only by setting CC1RoomOnly = 1. In **CC1** state, charge current is regulated less than or equal to CC1FChg. See the *Reduced Charge Current* section for reasons that charge current may be less than CC1IFChg.

The following events cause the charger state machine to exit **CC1** state:

- Battery voltage rises to ChgStepRise. The charger enters **CC2** state.

- Battery voltage drops below VPChg. The charger goes through **Fast-Charge CC1 Done**, **CC2 state** and eventually goes back to **precharge** state. During this process, charge marks internal signal StepChgDone = 1. If battery voltage rises above VPChg again, it skips **CC1** state to protect battery.
- CC1 timeout. If the step-charge timer is enabled CC1TmoLimit = 1 and charger remains in this state for longer than CC1FChgTmr, it enters **CC2** state.
- Charger safety timeout. If the charger safety timer ChgTmr expires while in **CC1** state, the charger enters **Charger Fault-Safety Timer ChgTmr Expired** state (ChgStat = 0b1001) and suspends charging.
- Temperature measured from THM is out of room temperature zone and CC1 is allowed to operate in room temperature only. If CC1RoomOnly = 1 and the battery temperature transitions from Room to Cool or Warm, the charger enters **CC2** state.
- JEITA disable charging. The charger suspends charging due to temperature. See the *JEITA compliance* section for detailed description.

The battery charger dissipates the most power in the fast-charge constant current mode, which causes the die temperature to rise. If the die temperature approaches ChgThrmLim = 115°C, see the *Thermal Regulation* section for charger operation details.

Fast-Charge Constant Current (CC2) State

The step-charge feature is enabled by default on the MAX20357. Once the battery voltage rises above step-charge threshold ChgStepRise, the charger enters **Fast-Charge Constant Current Mode 2** (CC2) state with a lower charge rate CC2IFChg in order to avoid lithium plating and prolong the lifetime of the battery. ChgStepHys field sets the hysteresis for the step charge function to avoid hopping between **CC1** state and **CC2** state caused by high voltage drop from current reduction. In **CC2** state, charge current is regulated less than or equal to CC2IFChg. See the *Reduced Charge Current* section for reasons that charge current may be less than CC2IFChg.

The following events cause the charger state machine to exit **CC2** state:

- Battery voltage rises to BatReg. CC Track is enabled by default chg_cc_trk = 1, the charger enters **CC Track** state. If CC Track is disabled chg_cc_trk = 0, the charger enters **Fast-Charge Constant Voltage** (CV) state. It is highly recommended to keep CC Track enabled for better performance.
- Battery voltage drops below ChgStepRise – ChgStepHys. Charger goes back to **CC1** state.
- Battery voltage drops below VPChg. Charger goes back to **Precharge** state.
- Charger safety timeout. If the charger safety timer ChgTmr expires while in **CC2** state, the charger enters **Charger Fault-Safety Timer ChgTmr Expired** state (ChgStat = 0b1001) and suspends charging.
- JEITA disable charging. The Charger suspends charging due to temperature. See thess *JEITA compliance* section for detailed description.

Pogo pin resistance may impose limit on maximum allowed step-charge threshold and CC2 charging current at termination voltage BatReg in order to prevent PLC communication failure.

Constant Current Tracking State CC Track

The charger enters **Constant Current Tracking** (CC Track) state when the battery voltage is close to termination voltage BatReg if CC track is enabled chg_cc_trk = 1. In **CC Track** state, charger current is evaluated roughly every 1.3ms. If charge current hits the CV mode charger current at the same battery voltage, charger reduce charge current by one fixed step 1/64 of CC2IFChg as shown in *Figure 13*. Charge current is reduced with controlled steps until charge current is less than termination current threshold IChgDone.

The following events cause the charger state machine to exit **CC Track** mode:

- Maximum charger current reduction is reached (charger current is reduced to 0.2 x CC2IFChg) or charger current is reduced below IChgDone, and charger is not in any current reduction mode. The charger enters **Maintain Charge** state and starts Maintain Charge timer.
- Charger safety timeout. If the charger safety timer ChgTmr expires while in **CC Track** state, the charger enters **Charger Fault-Safety Timer ChgTmr Expired** state (ChgStat = 0b1001) and suspends charging.
- JEITA disable charging. The Charger suspends charging due to temperature. See the *JEITA compliance* section for detailed description.

- **CC Track** state maintains a clean PLC line for data transfer and keeps battery voltage below regulation point in the meantime. By default, CC track is enabled. It is highly recommended to use this feature for more reliable PLC communication when earbud battery voltage is near fully charged.

Fast-Charge Constant Voltage (CV) State

As shown in *Figure 14*, if CC track is disabled, charger enters **Fast-Charge Constant Voltage** (CV) state when the battery voltage is close to top-off voltage BatReg. In the **CV** state, the charger regulates the battery voltage at BatReg and the charge current decreases from CC2IFChg as the battery voltage increases. Battery regulation voltage can be less than BatReg due to temperature. See the *JEITA Compliance* section for JEITA reduction of battery regulation voltage.

The following events cause the charger state machine to exit **CV** state:

- Charge current drops below IChgDone and charger is not in any current reduction mode, it enters **Maintain Charge** state and starts Maintain Charge timer MtChgTmr.
- Charger safety timeout. If the charger safety timer ChgTmr expires while in CV state, the charger enters **Charger Fault-Safety Timer ChgTmr Expired** state (ChgStat = 0b1001) and suspends charging.
- JEITA disable charging. The charger suspends charging due to temperature. See the *JEITA compliance* section for detailed description.
- Battery voltage drops. Reduced battery voltage does not directly lead to **CV** state exit. As battery voltage drops, charge current keep increasing. The charger enters **CC2** state when charge current hits CC2IFChg.

In **CV** mode, there might be transient in charger current in order to regulate battery voltage, especially during telemetry PING. This current transient is present on PLC line and could lead to potential PLC communication failure. It is recommended to use **CC track** mode during this charging phase.

Maintain Charge State

Charger enters **Maintain Charge** state from the **CC Track** state or **CV** state when the charge current drops below IChgDone. In **Maintain Charge** state, the charger regulates the battery voltage at BatReg and starts Maintain Charge timer. The charge current is equal or lower than IChgDone. The charge current keeps decreasing in **Maintain Charge** state while the battery voltage is regulated at BatReg.

The following events cause the charger state machine to exit Maintain Charge state:

- If charger auto-stop is enabled (ChgAutoStop=1) and the maintain charge timer MtChgTmr expires, the charger enters Maintain Charge Timer Done state and stops charging.
- If charge current rises above IChgDone, charger goes back to **CV** state and reset the step charge timer CC1FChgTmr.
- JEITA disable charging. The Charger suspends charging due to temperature and enters **Maintain Charge Timer Done** state. See *JEITA compliance* section for detailed description.

If charger auto-stop is disabled (ChgAutoStop = 0), charger ignores maintain charger timer and stays in **Maintain Charge** state even if charger current drops below IChgDone. When the charger transitions in and out of **Maintain Charge** state, charger safety timer does not reset. Only local timer resets. If charger enters **Maintain Charge** state, maintain charge timer MtChgTmr resets and starts counting. If charger exits **Maintain Charge** state and enters **CV** state, step charge timer CC1IFChgTmr resets.

Maintain Charge Timer Done State

Charger enters **Maintain Charge Timer Done** state from **Maintain Charge** state after the Maintain Charge timer MtChgTmr is expired and charger auto-stop enabled ChgAutoStop = 1 or when JEITA suspends charging. In **Maintain Charge Timer Done** state, charger stops charging. If charger is enabled ChgEn = 1 and the charger auto-restart is enabled ChgAutoReSta = 1, the charger exits **Maintain Charge Timer Done** state and resumes charging once the battery voltage falls below recharge threshold BatReg - BatReChg. If the charger auto-restart is enabled ChgAutoReSta = 1 and the system is placed in PLC IDLE mode after earbud battery is fully charged, the MAX20357 automatically exits PLC IDLE mode and resumes charging once the battery voltage falls below recharge threshold BatReg - BatReChg.

Charger Timers

The battery charger provides a global charger safety timer ChgTmr and three local timers, precharge timer PChgTmr, step-charge timer CC1FChgTmr, and maintain charge timer MtChgTmr to ensure safe charging. These timers prevent the battery from being overcharged.

The safety timer ChgTmr runs through all charging states that have non-zero charger current, including **Precharge**, **CC1**, **CC2**, **CC Track**, **CV**, and **Maintain Charge**. When charger safety timer ChgTmr expires, charger enters **Charger Fault - Safety Timer ChgTmr Expired** state (ChgStat = 0b1001) and stops charging.

Precharge timer PChgTmr runs in Precharge state. Precharge timer PChgTmr resets when charger enters **Precharge** state, except from JEITA suspend charging state (ChgStat = 0b1111). When precharge timer PChgTmr expires, the charger enters **Charger Fault – PChgTmr Expired** state (ChgStat = 0b1000) and stops charging.

The charger can exit safety timer fault or precharge timer fault state by toggling ChgEn, soft reset or removal and re-connection of PLC. When charger enters **Charger Off** state (ChgStat = 0b000) or **Charger IDLE** state (ChgStat = 0b0001) by the above behavior, charger can exit from charger fault state.

Step-charge timer CC1FChgTmr runs in **CC1** state. The step-charge timeout does not lead to any fault state. When it expires, charger is forced to enter CC2 state. Step-charge timer CC1IFChgTmr resets when the charger enters **CC1** state from **Precharge** state, or when the charger goes from **Maintain Charge** state to **CV** state. Due to battery internal resistance and cable/PCB trace resistance, it is common that battery voltage detected from BAT pin drops when charger goes from **CC1** to **CC2** state. It is caused by reduced charge current from CC1IFChg to CC2IFChg. If charger enters **CC2** due to step-charge timeout, even if battery voltage detected from BAT pin drops below step-charge threshold ChgStepRise - ChgStepHys, it stays in **CC2** state. StepChgDone is reset to 0 when the charger enters charger boot sequence.

In **CC1** state, **CC2** state and **CC Track** state, both the local step-charge timer CC1FChgTmr (in CC1 state) and the global charger safety timer ChgTmr are slowed by 50% the fast-charge current is reduced to be between 20% and 50% of CC1/CC2 charge current. These two timers are paused when the fast-charge current is reduced to be below 20% of CC1/CC2 charge current. Note the slowdown of the above timers applies to any type of fast-charge current reduction, see the *Reduced Charge Current* section.

Reduced Charge Current

Charger current can be less than the programmed value (IPChg, CC1IFChg, CC2IFChg) for any of the following reasons:

- JEITA controlled fast-charging current (CC1IFChg, CC2IFChg). When thermistor monitoring is enabled and the fast-charging current in cool, room, or warm temperature zone is programmed to be lower than 1xCC1IFChg/CC2IFChg.
- The SYS LDO is enabled, and the PLC current limit is reached. The charge current is reduced in favor of the system load. System load always gets priority over the charger current.
- The SYS LDO is disabled, but the PLC current limit is lower than the programmed charger current. The charger current is regulated at the PLC current limit.
- The charger is under thermal regulation, see the *Thermal Regulation* section.

If the charger drop-out voltage drops down to the programmable threshold PLC_DROP, charger current is actively reduced to maintain the charger input and output voltage difference $V_{PLC} – V_{BAT}$ at PLC_DROP. As shown in *Figure 14*, when charger current is being actively reduced, some charger state transitions are unavailable.

JEITA Compliance

To enhance safety when charging Li+ batteries, the MAX20357 features JEITA compliant temperature monitoring. Temperature measurement using an external NTC thermistor places the battery into one of five temperature zones: cold, cool, room, warm, and hot. When JEITA compliant thermistor monitoring is enabled, charging is always inhibited in cold and hot regions or if the thermistor cannot be detected. Charging behavior is configurable in warm, room, and cool regions using the I^2C-controlled ThmEn parameter, as demonstrated in *Figure 15* – *Figure 18*. Maintain charge state (ChgStat = 0b0110) only runs in room temperature zone when thermistor monitoring is enabled.

CC1 state has its dedicated I^2C programmed temperature thresholds, which can be configured using the ChgT1ThrCC1-ChgT4ThrCC1. I^2C-programmed temperature thresholds of precharge state, CC2 state, CC Track state and CV state can be configured using ChgT1ThrDef-ChgT4ThrDef. JEITA current control strategy in cool, room, and warm zone is programmable with the ThmCfg0-ThmCfg2 as shown in *Figure 15* – *Figure 18*.

Note that JEITA measurements are continuous only if PLC is present. If PLC is not present and ThmEn setting is higher than 0x3, JEITA measurement is performed based on ModelGauge m5 EZ measurements at a maximum rate set by jta_eoc_sel.

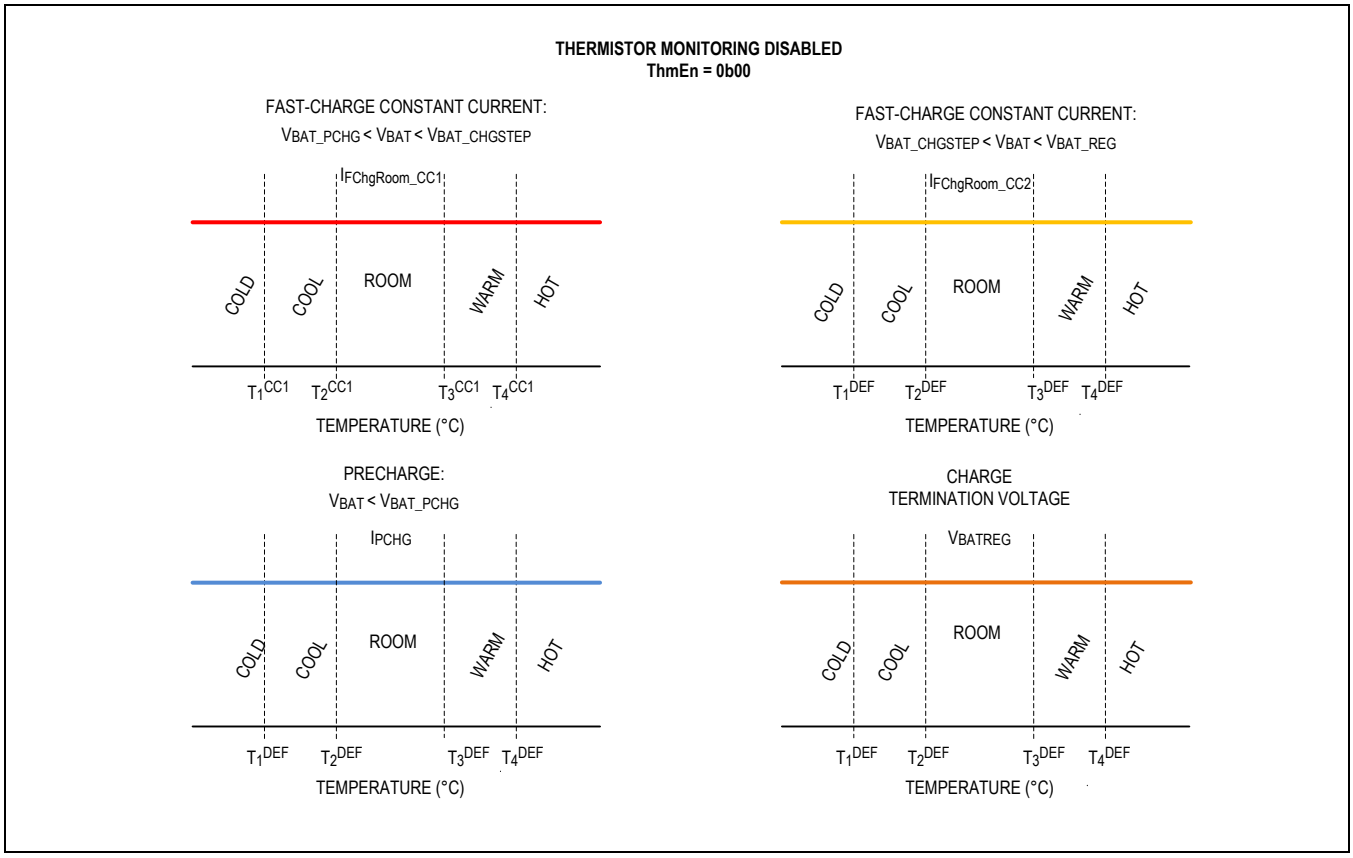


Figure 15. Temperature Monitoring Disabled

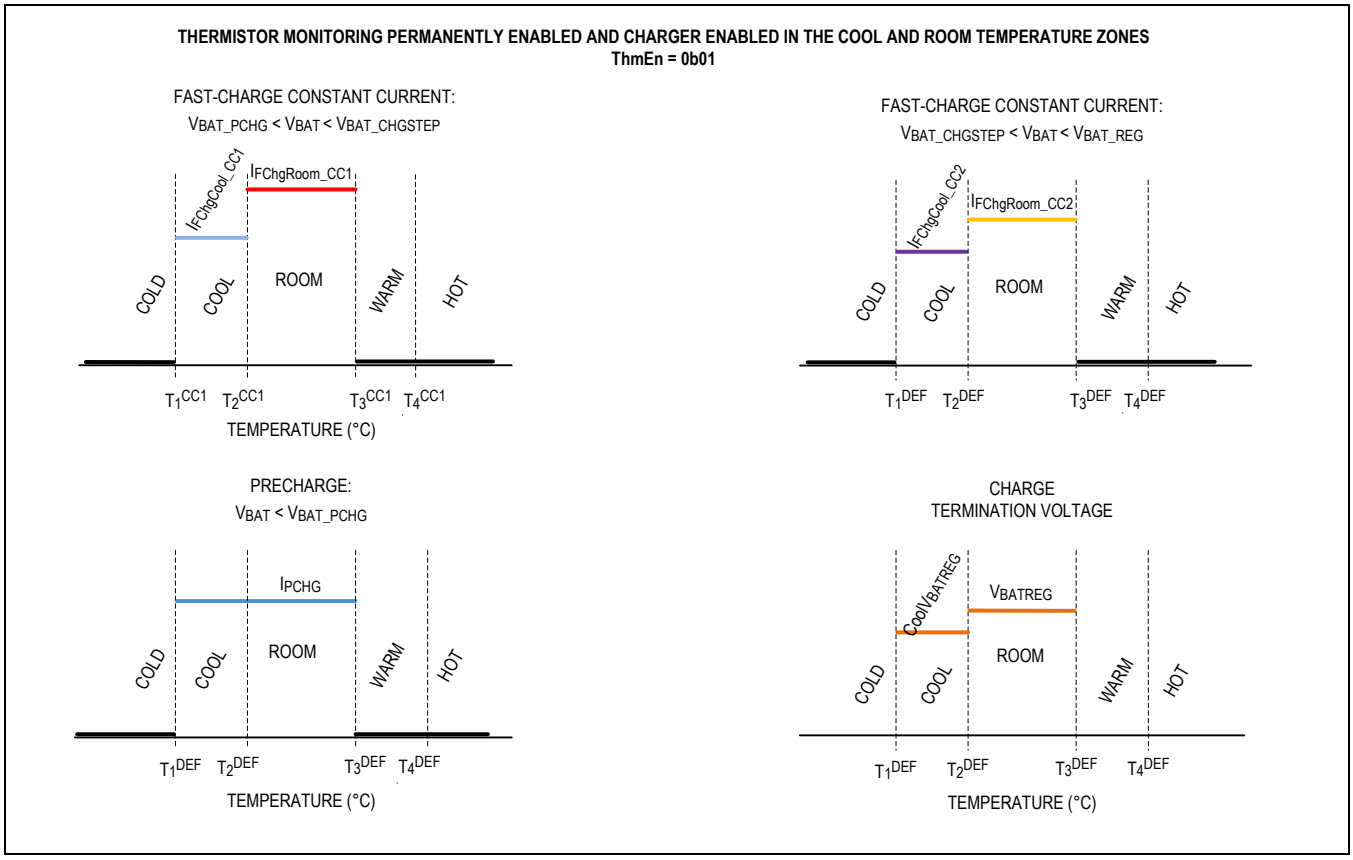


Figure 16. Charging Enabled in Cool and Room Regions

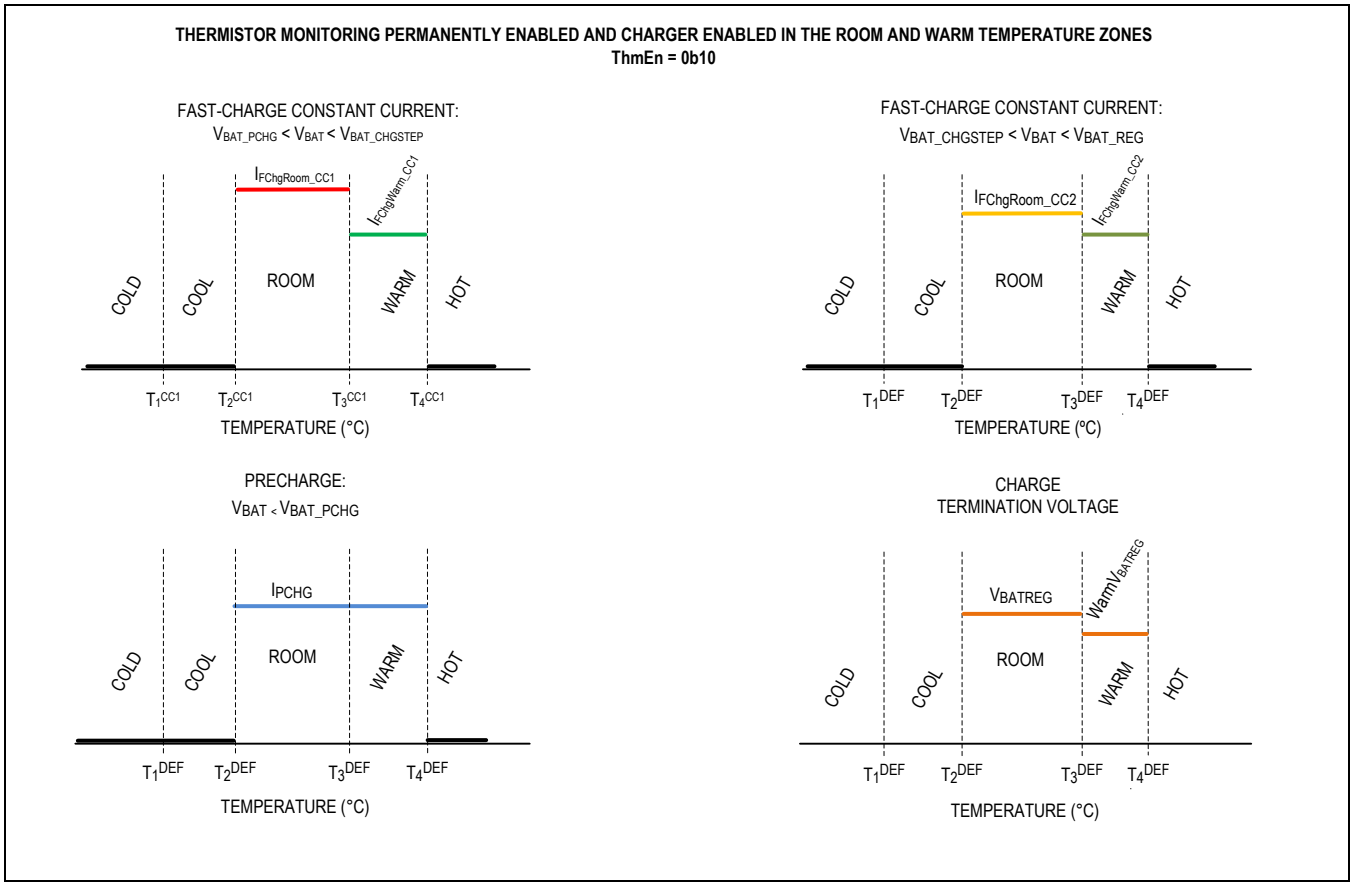


Figure 17. Charging Enabled in Room and Warm Regions

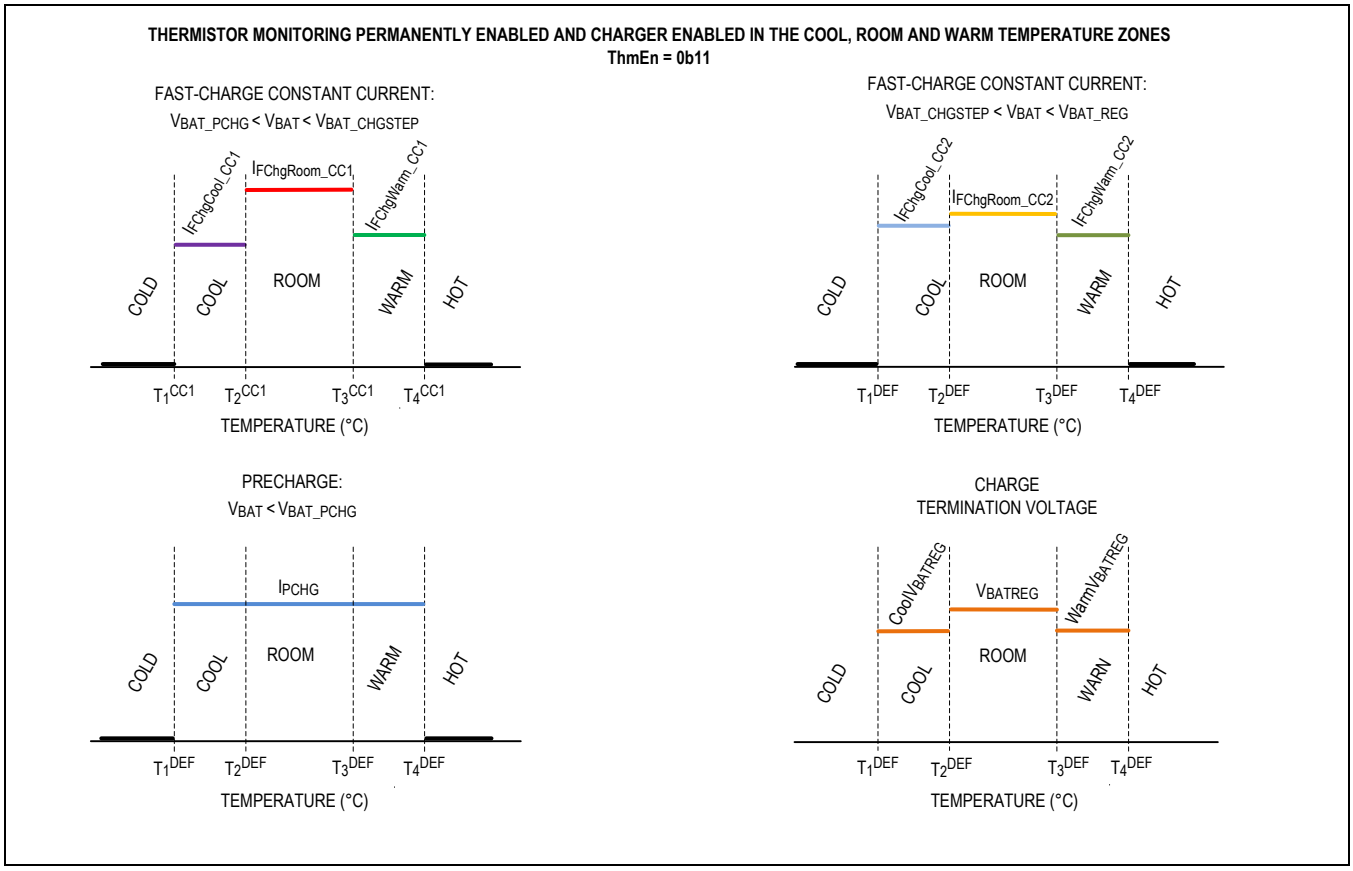


Figure 18. Charging Enabled in Cool Room and Warm Regions

Thermal Regulation

In addition to PLC input current limit, the MAX20357 features thermal charge current regulation. This circuit acts to reduce charge current when the die temperature reaches a programmed thermal limit T_{SHDN_PLC} – 3°C, preventing further temperature increase. T_{SHDN_PLC} is I^2C programmable through ChgThrmLim. If the SYS LDO is enabled, the thermal regulation loop first reduces charge current in favor of the SYS load. As the charge current is reduced to zero, the charger is off. If the die temperature continues to increase, the thermal regulation loop reduces SYS LDO current, and the system load is supplemented by the battery. ChgThrmReg and its corresponding interrupt indicate if charger is under thermal regulation. If current is reduced to 0 but temperature still hits T_{SHDN_PLC}, the MAX20357 enters thermal shutdown mode, waiting for temperature to drop below the threshold. The MAX20357 resumes operation once the temperature drops below thermal threshold. Note that all the registers reset to default when the MAX20357 goes out from thermal shutdown. This feature is designed to provide second overheating protection for earbud in addition to JEITA current operation.

SYS LDO and Power Path

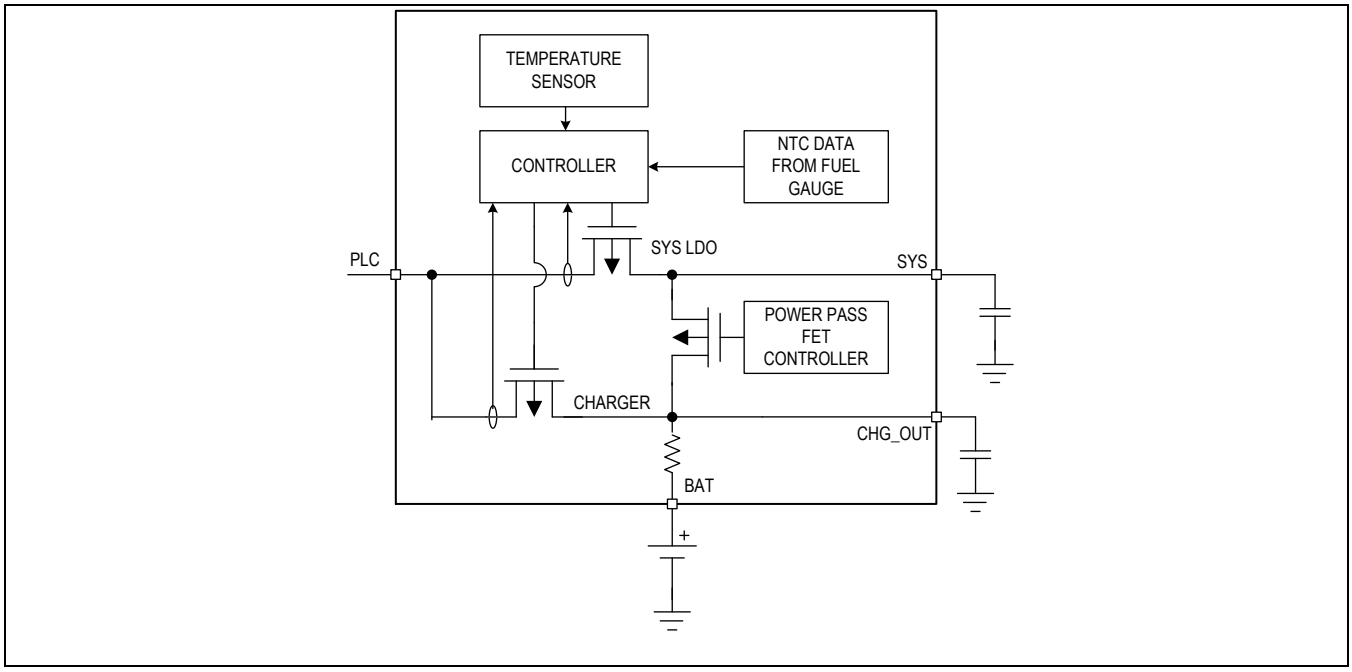


Figure 19. Input Limiter, Power Path, and Charger Block Diagram

SYS LDO Default Mode

After power on reset, SYS LDO delivers power to the SYS output from the PLC line. When PLC is present, the SYS LDO output voltage reference is set based on the following rule:

$$V_{SYS} = MAX\ (V_{BAT}, SysMin)$$

If V_{BAT} is lower than minimum system voltage SysMin, SYS LDO regulates SYS voltage at SysMin to maintain a constant supply voltage to prevent the earbud SoC from UVLO. If V_{BAT} is higher than minimum system voltage SysMin, the SYS LDO works in parallel with the charger by default and regulates $V_{SYS} = V_{BAT}$.

It should be noted that SYS LDO also decouples the SYS capacitance from the PLC line. On PLC pin, no capacitance should be attached in order to allow full data rate communication.

SYS LDO Bypass Mode

As illustrated in the previous sections, PLC line is sensitive to load change, which may cause abrupt voltage change and corrupt PING packet. The MAX20357 features to bypass SYS LDO and support any transient load directly from the battery. When PLC is present, set SysMinForce = 1 to force the SYS LDO to regulate V_{SYS} = SysMin. The SYS pin voltage is regulated based on the following rule:

$$V_{SYS} = MAX\ (V_{BAT} - PP_drp, SysMin)$$

When the battery voltage is sufficiently higher than minimum system voltage SysMin (V_{BAT} – PP_drp > SysMin), the power path FET is turned on and battery to SYS voltage drop is regulated to the programmable value PP_drp. The SYS LDO attempts to regulate V_{SYS} = SysMin. However, due to the power path, V_{SYS} is clamped at PP_drp lower than battery voltage, which is higher than SysMin. SYS LDO eventually turns off. All system load is supplied by battery. The PLC line current is regulated by the charger constant current control loop. PLC line is protected from any significant fluctuation caused by system load transient. To achieve reliable PLC communication and maintain a clean PLC channel, it is highly recommended to set SysMinForce = 1 when the battery voltage is sufficiently higher than SysMin. When battery voltage is not sufficiently higher than SysMin (V_{BAT} – PP_drp < SysMin), power path is open and the SYS LDO regulates V_{SYS}

= SysMin. System load is supplied from the PLC line. System designer needs to avoid applying any transient load during PLC PING since it may cause PLC communication failure and disconnection of PLC.

Battery Only Mode

When the PLC is not present and the battery is alive, the power path FET is fully ON and the system load is supplied by the battery.

Reverse Protection

The SYS LDO and the charger feature reverse protection preventing reverse conduction when V_{SYS} or V_{BAT} is higher than the PLC charging voltage. When the voltage difference between the two earbud batteries is large, and the minimum algorithm is elected in the MAX20355, PLC charging voltage is adjusted to track the lower earbud battery of the two. In the earbud with the higher battery voltage, V_{SYS} and V_{BAT} are higher than PLC charging voltage. In this condition, the SYS LDO and the charger are in reverse protection and current is not back driving PLC line. During reverse protection, the MAX20355 and MAX20357 are still exchanging battery voltage and SOC information through telemetry PINGs. The reverse protection feature allows the MAX20355 to track either battery without concern of back driving the PLC line.

Mono-slave and Dual-slave Mode

The MAX20357 supports dual-slave mode to connect to PLC1 or PLC2 on the MAX20355, or mono-slave mode if PLC1 and PLC2 on MAX20355 are shorted. PLC input current upper limit is programmable through PLCCurr with maximum value of 200mA or 400mA depending on the state of the Ichg_x2 bit. The function Ichg_x2 bit is summarized as follows:

1. Ichg_x2 = 0. In dual-slave mode, PLC input current limit is set to operate in the range up to 200mA, SYS LDO output current and the charger current are both limited to PLCCurr, up to 200mA.
2. Ichg_x2 = 1. When PLC1 and PLC2 of the MAX20355 are shorted in mono-slave mode, Ichg_x2 can be set to 1 to double the PLC input current PLCCurr to 400mA. SYS LDO output current is limited by PLCCurr, up to 200mA. Charge current is limited by 2xPLCCurr, up to 400mA.

By setting Ichg_x2 to 1, the MAX20357 doubles PLC current limit PLCCurr and charger current CC1IFChg/CC2IFChg. The MAX20357 achieves up to 400mA charge current in mono-slave mode. Note that since the MAX20355 needs to short PLC1 and PLC2, it may cause current imbalance between two channels (Refer to the MAX20355 data sheet for detailed description). The PLC solution does not support to toggle between mono-slave and dual-slave mode during operation. Once the system is configured to mono-slave mode, PLC current sink PLCSnkSel and PLC voltage threshold PLCThrSel on both MAX20355 and MAX20357 are doubled automatically to compensate for higher buck-boost output voltage ripple created by PLC1 and PLC2 tied together.

Battery Presence Detection

When pack protectors open due to a discharge-related fault, the pack protector turns off the discharge FET, placing a reverse-biased body diode in the discharge path and preventing further discharge. In this state, the system designer can decide that the battery has been damaged and that they would like to prevent a full charge cycle in the future. Even if the system designer does decide that the battery can be recovered, they can have concerns that the diode drop of the pack protector can cause the charger to believe that the battery is above the precharge voltage threshold, which would mean that the fast-charge current is applied.

In this scenario, it is useful for the system to understand before starting a full charge cycle whether a pack is present on the BAT node (with an open protector) or if the battery has simply been removed. The MAX20357 contains all of the necessary circuitry to allow the system designer to implement such a check.

One example of a simple algorithm to check for such a condition is to run the below check every time before starting a battery charging cycle:

1. Before enabling the charger, set BattPullDown = 1 to enable the pulldown resistor on the BAT node and monitor BatUVLOB status bit. This pulldown resistor discharges the capacitance on the BAT node in case the battery is not present or the pack protector is open. After some time, check BatUVLOB status and disable the BAT pulldown resistor. If BatUVLOB = 1 (V_{BAT} > BAT_UVLO), then the battery is present, and charging can be enabled. If BatUVLOB = 0, the BAT voltage is below the UVLO threshold. There are two possibilities for BatUVLOB = 0:
   a. The battery is not present.
   b. The pack protector is open.

2. To distinguish between the above two possibilities, set FrcPChg = 1 and ChgEn = 1 to enable charging and force the charger to operate in the Precharge state (ChgStat = 0b0010) and monitor ChgVoltMode status bit. Such charging current and duration can close the pack protector if there is a battery present. After some time, if ChgVoltMode = 0 ($V_{BAT} < V_{BAT_REG}$), this indicates that the pack protector is closed, and the battery is sinking the precharge current IPChg. Set FrcPChg = 0 to disable force precharge and the charger enters the normal charging states determined by the battery voltage. If ChgVoltMode = 1 ($V_{BAT} \geq V_{BAT_REG}$), set FrcPChg = 0 and ChgEn = 0 to disable charging. There are two possibilities for ChgVoltMode = 1:
   a. The battery is not present. The precharge current IPChg quickly charges the capacitance at the CHG_OUT node.
   b. The battery is present and the forced precharge current IPChg closes the pack protector. However, the battery voltage is higher than termination voltage BatReg. Repeat step 1, if BatUVLOB = 1, this indicates the battery is present as the pack protector has closed and V_{BAT} > BAT_UVLO.

Note that if the ChgGMD = 1 ($V_{PLC} - V_{BAT} <$ PLC_DROP), the battery presence detection mentioned above is not reliable as the limiter is not allowing the charger to force any current into the BAT node.

If THM pin is connected to the thermistor inside the battery pack, battery insertion/removal detection can also be reported by the integrated fuel gauge. If THM pin is connected to the thermistor on the PCB, use the procedure mentioned above to detect battery presence.

PLC Operation Modes

The MAX20357 features multiple modes of operation that are designed to minimize power consumption in the end user's application. The transitions between modes and general operation are shown in *Figure 21*. Behavior of main functional blocks in SEAL mode, OFF mode, and SYSUVLO mode is summarized in *Table 6*.

Table 5. Functional Block Status in Low Power Modes

	SYSUVLO	SEAL	OFF	DISABLE PLC (plc_fsm_ena = 0)
Charger	OFF	OFF	OFF	OFF
SYS LDO	OFF	OFF	OFF	OFF
Power Path FET	OFF	OFF	Fully ON	Fully ON
Fuel Gauge	OFF	OFF	OFF	ON
PLC	Passive impedance network	Passive impedance network	Passive impedance network	Passive network not connected
I^2C Access	No	No	No	Yes
After Exiting	OTP reload	OTP reload	OTP reload	No OTP reload

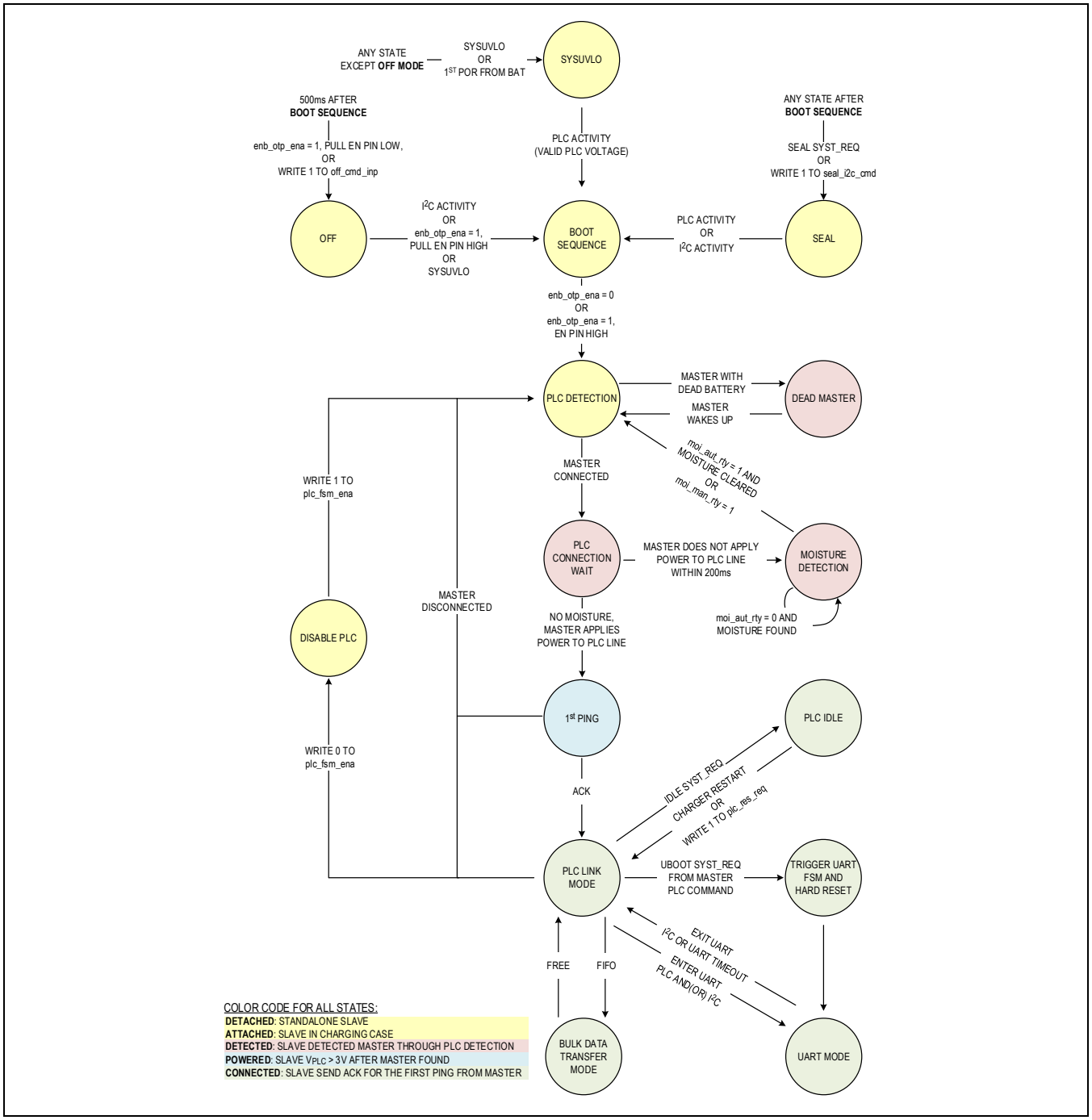


Figure 20. MAX20357 Device Operating Modes

The MAX20357 features multiple modes of operation that are designed to minimize power consumption in the end user's application. The transitions between modes and general operation are shown in *Figure 21*. Behavior of main functional blocks in SEAL mode, OFF mode, and SYSUVLO mode is summarized in *Table 6*.

Table 6. Functional Block Status in Low Power Modes

	SYSUVLO	SEAL	OFF	DISABLE PLC (plc_fsm_ena = 0)

Charger	OFF	OFF	OFF	OFF
SYS LDO	OFF	OFF	OFF	OFF
Power Path FET	OFF	OFF	OFF	Fully ON
Fuel Gauge	OFF	OFF	ON	ON
PLC	Passive impedance network	Passive impedance network	Passive impedance network	Passive network not connected
I^2C Access	No	No	Yes	Yes
After Exiting	OTP reload	OTP reload	No OTP reload	No OTP reload

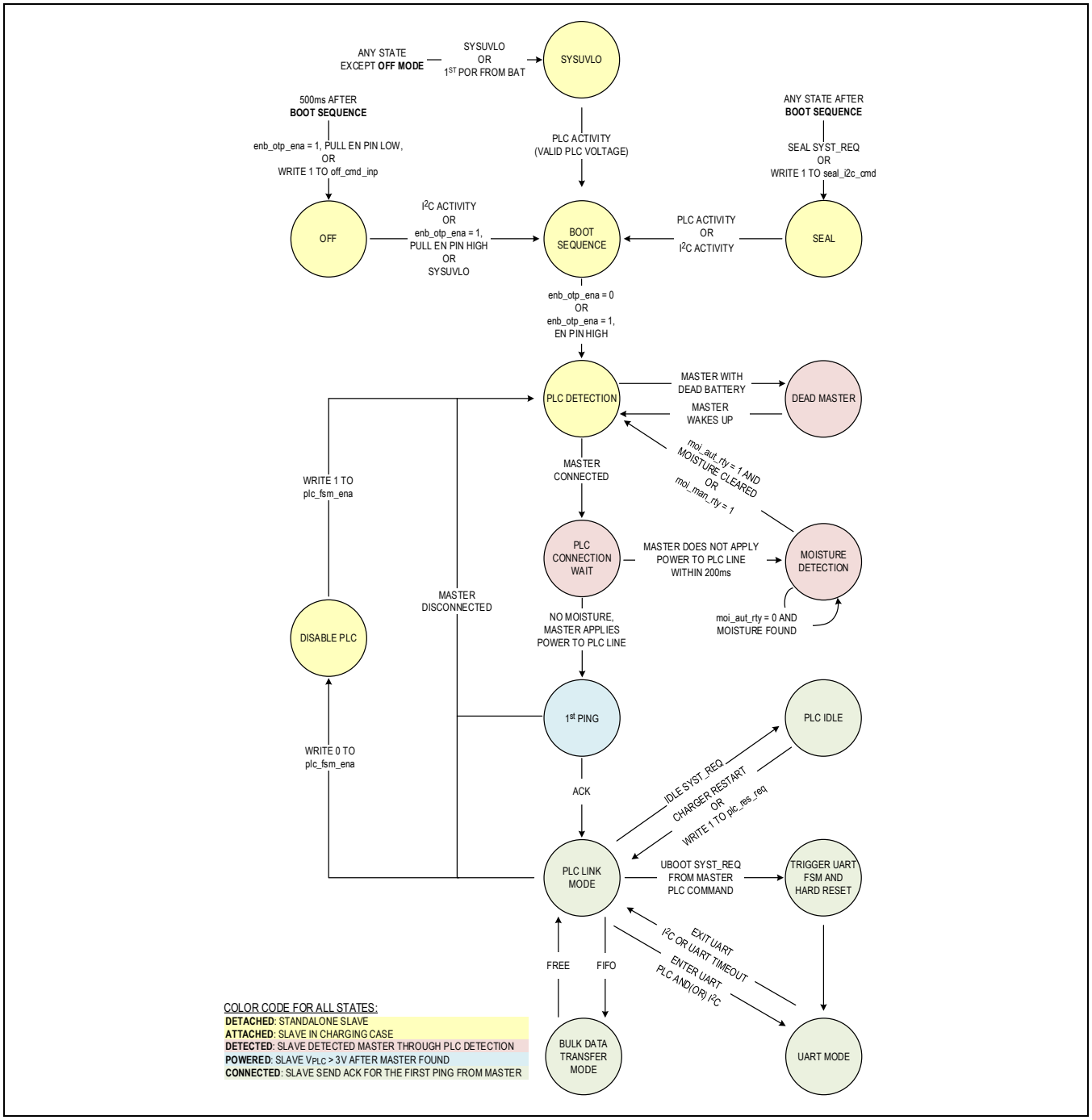


Figure 21. MAX20357 Device Operating Modes

SYSULVO Mode

The MAX20357 enters SYSUVLO mode after first power up from BAT pin, or when SYS pin voltage drops below SYSUVLO threshold. The device exits SYSUVLO mode when the device detects PLC voltage higher than 3V. OTP registers are reloaded after the device exits SYSUVLO mode.

SEAL Mode

The MAX20357 features SEAL mode, which puts the device into low-power mode for shipping. The MAX20357 enters SEAL mode by SEAL SYST_REQ PLC command issued from the MAX20355, or by I2C SEAL request (write 1 to seal_i2c_cmd). The supply current in SEAL mode is reduced to 170nA (typ), power path FET is turned off, fuel gauge is shutdown, and all other blocks are placed into low-power mode. The device exits SEAL mode when the device detects PLC voltage higher than 3V or I2C activity. OTP registers are reloaded after the device exits SEAL mode.

OFF Mode

The MAX20357 enters OFF mode by driving the EN low if EN pin function is enabled (enb_otp_ena = 1, default is 0), or by issuing OFF mode request through I2C (write 1 to off_cmd_inp). The supply current in OFF mode is reduced to 0.6µA (typ), I2C data is retained, power path FET is fully ON, fuel gauge is shutdown, and all other blocks are placed into a low-power mode. The device exits OFF mode when the EN bit is driven high in case enb_otp_ena = 1 or the device detects I2C activity. OTP registers are reloaded after device exits OFF mode. Note that enb_otp_ena is also reset to its default OTP setting after the device exits OFF mode.

OFF Mode

The MAX20357 enters OFF mode by issuing OFF mode request through I2C (write 1 to off_cmd_inp), or by driving the EN low if EN pin function is enabled (enb_otp_ena = 1, default is 0). In the OFF mode, SYS power is cut off, I2C access is retained, and all other blocks are placed into a low-power mode. The device exits OFF mode when the device detects PLC voltage higher than 3V (default) or the EN bit is driven high (enb_otp_ena = 1). OFF mode offers a low power mode for the charge done use case, when battery is fully charged but the slave device remains in charging case.

PLC Detection Mode

Standalone master or slave operates in PLC detection mode when the device is active. The PLC and moisture detection block diagram is shown in *Figure 22*. In PLC detection mode, master sends PLC detection pulse through an internal pullup/pulldown resistor every 380ms. Slave sends PLC detection pulse through a similar pullup/pulldown resistor every 240ms. Master PLC is active, fuel gauge is on, and other blocks are in low-power mode; slave PLC is active, fuel gauge is on, power path FET is fully on, and other blocks are in low-power state. Both the master and slave contain a passive impedance clamp network, which allows the PLC device to detect its counterpart device even when the counterpart device has a dead battery. See the following sections for a detailed description of the master and slave connection detection scheme under various circumstances. PLC detection pulse or moisture measurement launched by the counterpart device is shown in a dashed line.

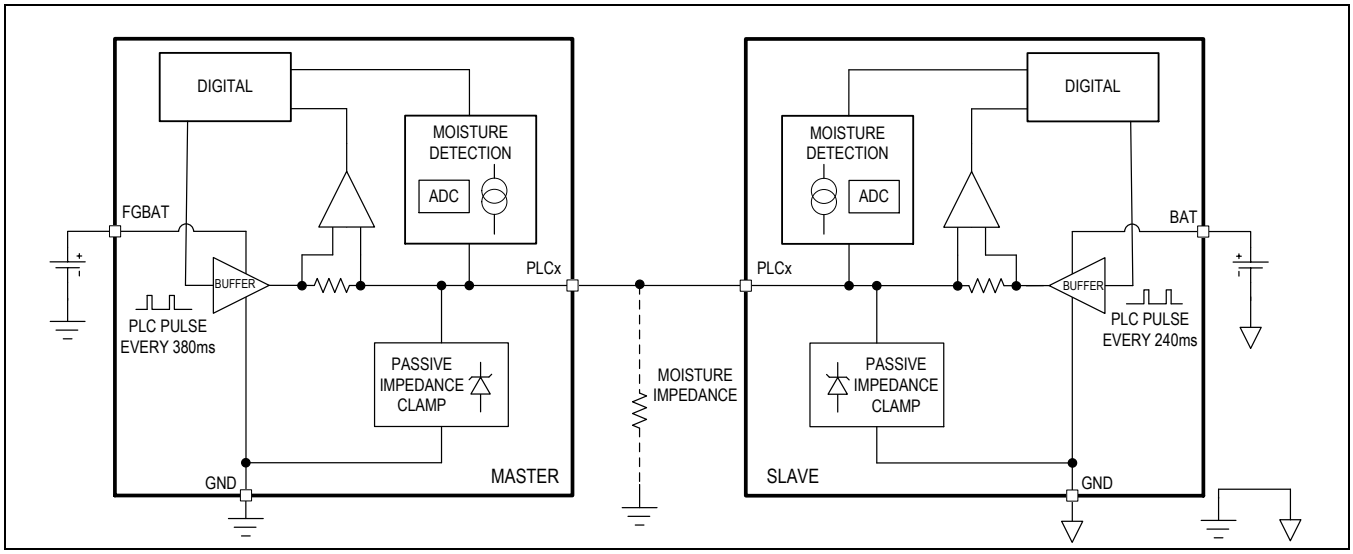


Figure 22. PLC and Moisture Detection Block Diagrams

Active Master and Active Slave

As shown in *Figure 23*, both the master and slave are in the PLC detection mode before the slave attached. After receiving slave's PLC detection pulse on the PLC line, the master sends a signature pulse (3x pulse) and automatically launches a moisture measurement. If there is no moisture, master connects the PLC line to a buck-boost output and holds PLC voltage to default charge voltage (default 3.5V) for 100ms. Then master increases PLC voltage to communication voltage (default 5.5V) and PING the slave. If master received ACK from slave, both devices enter PLC Link mode. After the master and slave build connection, ch1/2_con_sts status bit of MAX20355 and chn_con_sts status bit of MAX20357 are set, the corresponding interrupt bits are asserted accordingly.

If there is moisture found, the master does not turn on buck-boost to supply PLC1/2 pin and no power is applied to the slave. Moisture-related status and interrupt registers in MAX20355 are set indicating moisture detected. If the slave does not detect power applied through the PLC line within 200ms, it launches moisture measurement automatically. If moisture is not cleared, the slave stays in moisture detection mode and launches automatic moisture detection every 16s. Once the slave detects moisture is cleared, it proceeds to PLC detection mode to connect with the master. See the *Moisture Detection* section for a detailed description of the moisture feature.

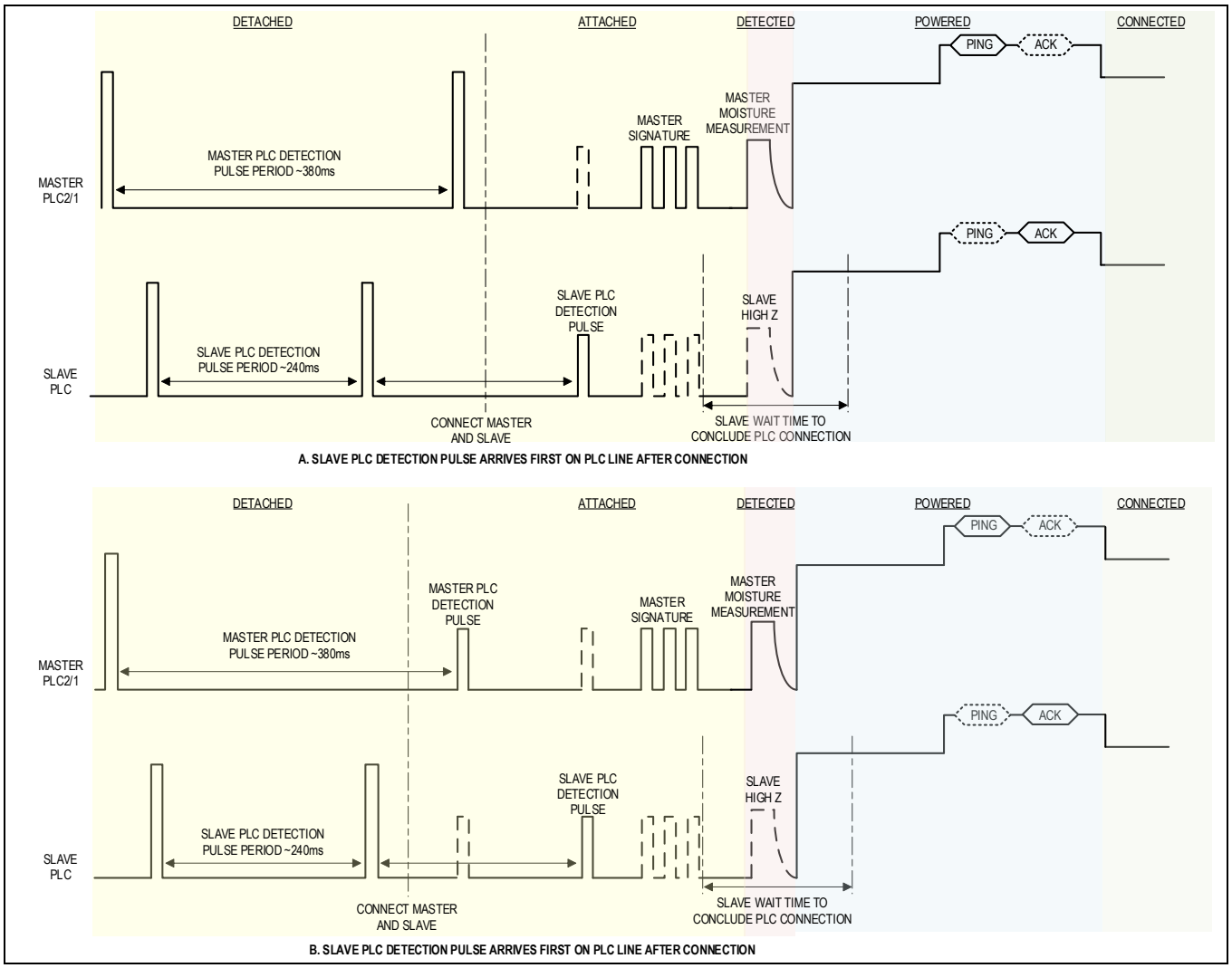


Figure 23. Active Master and Active Slave Connection

Active Master and Dead Slave

Both master and slave offer passive impedance clamp networks for dead slave battery detection and moisture detection. As shown in *Figure 24*, before connection, master is in PLC detection mode and slave is connected to a dead battery.

After the slave is attached to the master, the amplitude of the master's PLC detection pulse is clamped to 1.8V by slave's internal passive impedance clamp network. Master perceives its PLC detection pulse with reduced amplitude as 'something connected'. After 3x consecutive 'something connected' pulse, the master launches moisture measurement automatically. If there is no moisture, the master connects the PLC line to the buck-boost output and holds the PLC voltage to default charge voltage (default 3.5V) for 100ms. Then the master increases PLC voltage to communication voltage (default 5.5V) and PING the slave. If master received ACK from slave, both devices enter the PLC Link mode. After the master and slave build connection, ch1/2_con_sts status bit of MAX20355 and chn_con_sts status bit of MAX20357 are set, the corresponding interrupt bits are asserted accordingly.

Note that not only does the passive impedance clamp on slave creates a 'something connected' pulse on the master, but moisture between the PLC line and the ground can also create similar behavior. Master is not able to determine if it is real slave or moisture impedance before launching moisture detection. If there is moisture found, master does not connect the buck-boost output to PLC1/2 pin, and power is not applied to the slave. Moisture-related status and interrupt registers in MAX20355 are set indicating moisture detected. The MAX20357 remains in SYSUVLO mode.

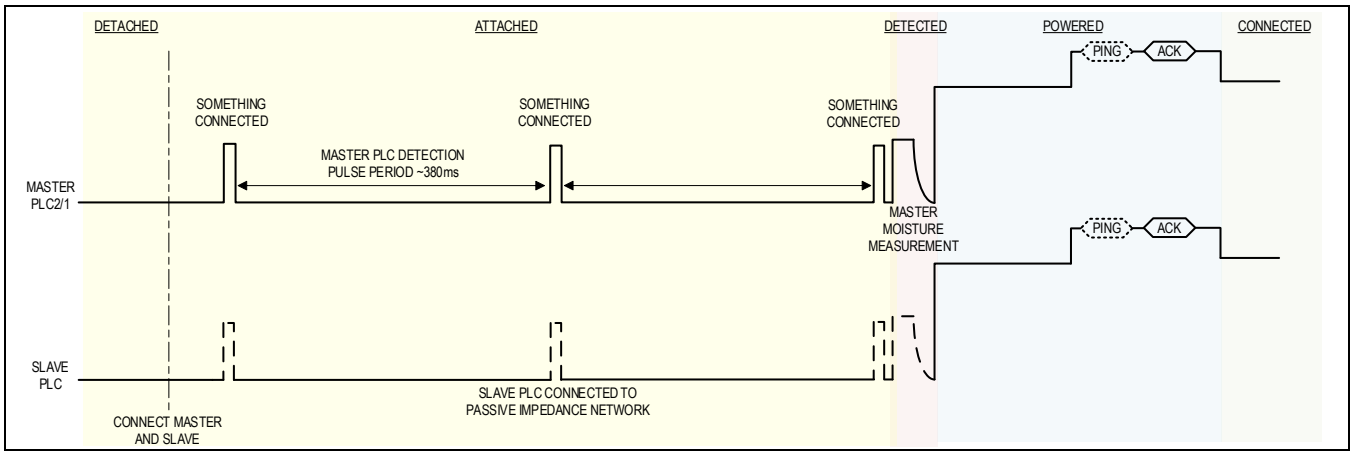


Figure 24. Active Master and Dead Slave Connection

Dead Master and Active Slave

As shown in *Figure 25* before connection, the slave is in PLC Detection mode and master is connected to a dead battery. After slave is attached to the master, the slave's PLC detection pulse is clamped to 1.8V by master's passive impedance clamp network. The slave perceives its PLC detection pulse with reduced amplitude as 'something connected'. After 3x consecutive 'something connected' pulse, dead_found interrupt is asserted in MAX20357 signaling dead master is detected, MAX20357 automatically launches a moisture measurement and continues sending PLC detection pulse. After master wakes up, master and slave follow the procedure described in 'Active Master and Active Slave' to build a connection.

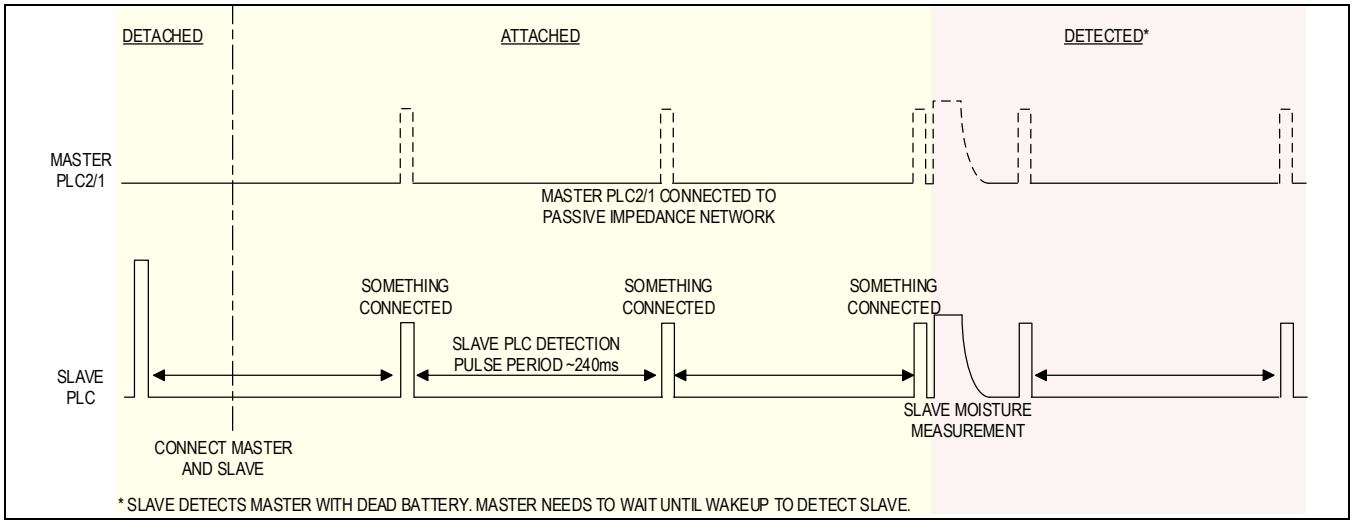


Figure 25. Dead Master and Active Slave Connection

Moisture Detection

To prevent corrosion of the contacts if moisture is present on the PLC outputs, both the MAX20355 and MAX20357 offer a build-in moisture detection feature to check the resistance from the PLC output to GND. If the impedance detected is less than the I²C programmable moisture threshold, corresponding interrupts are flagged on both devices. The MAX20355 does not connect the buck-boost output to the PLC lines to start the charging process whenever moisture is detected. For both MAX20355 and MAX20357, moisture target current is set by RaccDetMIp (default 1µA) and voltage threshold is set by RaccDetMThr (default 700mV). The moisture threshold is then calculated as RaccDetMThr/RaccDetMIp (default 700kΩ). Both the MAX20355 and MAX20357 can launch moisture detection before the PLC line is connected to the buck-boost output. After MAX20355 and MAX20357 build the PLC connection and enters the PLC link mode, manual moisture request is queued and proceeded after the PLC disconnection event. Note that after MAX20355 and MAX20357 build connection and starts charging, it is not able to measure moisture by applying source current and measuring voltage from ADC, since PLC voltage is already regulated by the buck-boost converter. The MAX20355 offers overcurrent protection for this use case to maintain system safety. The detailed description is in the overcurrent protection section. After POR, if no moisture is found previously, MAX20355 launches moisture detection under the following conditions:

3. After MAX20355 detects PLC pulse from the MAX20357 and sends signature pulse.
4. After MAX20355 detects 3x consecutive ‘something connected’ pulse. If the MAX20355 detects an equivalent resistance less than 17kΩ (typ) applied between PLC line and ground, the amplitude of PLC detection pulse reduces and MAX20355 recognizes it as ‘something connected’ pulse.
5. After manual moisture detection request through I²C bit moi_man_pl1/2. Manual moisture request is queued when buck-boost voltage is applied.
6. Automatic moisture detection every 16s if it is enabled through I²C bit moi_det_aut1/2. By default, moi_det_aut1/2 is set to 0 and automatic moisture detection is disabled.

After POR, if no moisture is found previously, the MAX20357 launches moisture detection under the following conditions:

7. After MAX20357 detects 3x consecutive ‘something connected’ pulse. If the MAX20357 detects an equivalent resistance less than 17kΩ (typ) applied between PLC line to ground, the amplitude of PLC detection pulse reduces and MAX20357 recognizes it as ‘something connected’ pulse.
8. After manual moisture detection request through I²C bit moi_man_pl. Manual moisture request is queued when buck-boost voltage is applied.
9. Automatic moisture detection every 16s. Automatic moisture detection is enabled by default.

During moisture detection, the MAX20355 and MAX20357 source a current through PLC pin and measure PLC voltage with built-in ADC. Moisture detection logic always starts from 1µA source current. If the ADC voltage reading RaccDetMThr is less than 0x3F – AdcRng, it increases current to 4 times and repeats the same measurement until the measured value is larger than 0x3F – AdcRng or maximum source current 64µA is reached. The moisture measurement

algorithm ensures that the target moisture sink current RaccDetMIp can be reached for the best accuracy. The ADC voltage readings are reported in ADCAvg and source current is reported in IP_RES_DET. Moisture resistance is calculated as ADCAvg/IP_RES_DET. Once the moisture measurement is completed, based on the measured result, corresponding interrupts are asserted as shown in *Figure 25*. Note that the designed chip-level impedance measurement error is ±10%. However, the actual measurement error in the application can be higher than ±10% due to leakage current on PCB. Especially when moisture impedance is approaching 1.5MΩ, the leakage current is comparable to ADC source current. Since the leakage current varies depending on application schematic and layout design, the actual measurement error also varies from design to design.

Table 7. Moisture Interrupt

MOISTURE INTERRUPT	MOISTURE RESISTANCE
res_det_gnd	R_{MOI} < 458Ω ± 92Ω
moi_irq_det	R_{MOI} < RaccDetMThr / RaccDetMIp (default 700kΩ)
moi_dne_int	RaccDetMThr / RaccDetMIp (default 700kΩ) < R_{MOI} < 1.5MΩ
res_det_opn	R_{MOI} > 1.5MΩ
res_det_abr	Significant variation during moisture measurement
plc2/1_moi_det (MAX20355)	R_{MOI} < RaccDetMThr / RaccDetMIp (default 700kΩ) Set by automatic moisture detection conditions 1, 2 and 4
plc_moi_det (MAX20357)	R_{MOI} < RaccDetMThr / RaccDetMIp (default 700kΩ) Set by automatic moisture detection conditions 1 and 3

If moisture is detected, the MAX20355/MAX20357 continues sending PLC detection pulse by default to check resistance on the PLC line through its internal pullup resistor. If the equivalent moisture resistance measured is larger than 17kΩ, MAX20355 and MAX20357 perceive it as moisture removed and clears corresponding interrupts. Note that even moisture is detected in one standalone PLC device, if it is attached to its counterpart device, they are still able to pass the ATTACHED phase of the PLC connection detection process. After entering the DETECTED phase, MAX20355 launches moisture detection and fails to build a connection with the MAX20357. The system cycles between ATTACHED and DETECTED back and forth until moisture condition is removed. Automatic moisture retry on the MAX20355 can be disabled by setting moi_aut_rty1/2 = 0. Automatic retry on the MAX20357 cannot be disabled.

PLC IDLE Mode

Once the MAX20357 battery is fully charged, either MAX20355 or MAX20357 can put the system into PLC IDLE mode by IDLE SYST_REQ PLC command to reduce unnecessary power losses. The current consumption of the MAX20357 in PLC IDLE mode is reduced to 11µA. In PLC IDLE mode, master and slave suspend charging by removing power from the PLC line and starts handshaking pulsing protocol to check the presence of the other device. Both master and slave can request to resume PLC communication from PLC IDLE mode by writing 1 to plc_res_req through I^2C. The system automatically resumes from the PLC IDLE mode if the MAX20357 charger auto-restart is enabled and MAX20357 battery voltage falls below charger restart threshold. *Figure 26* shows the waveform of the MAX20355 issuing IDLE SYST_REQ PLC command to put the system into PLC IDLE mode.

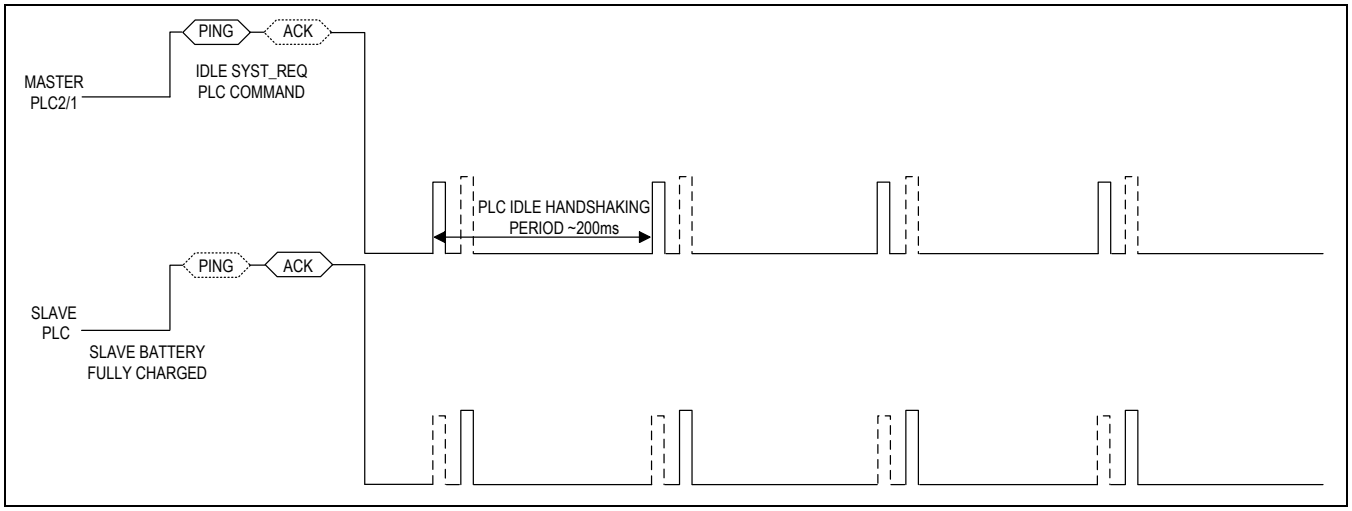


Figure 26. Enter PLC IDLE Mode After Slave Battery is Fully Charged.

Both MAX20355 and MAX20357 could detect the PLC disconnection (earbud removal) while in PLC IDLE mode, as shown in *Figure 27*.

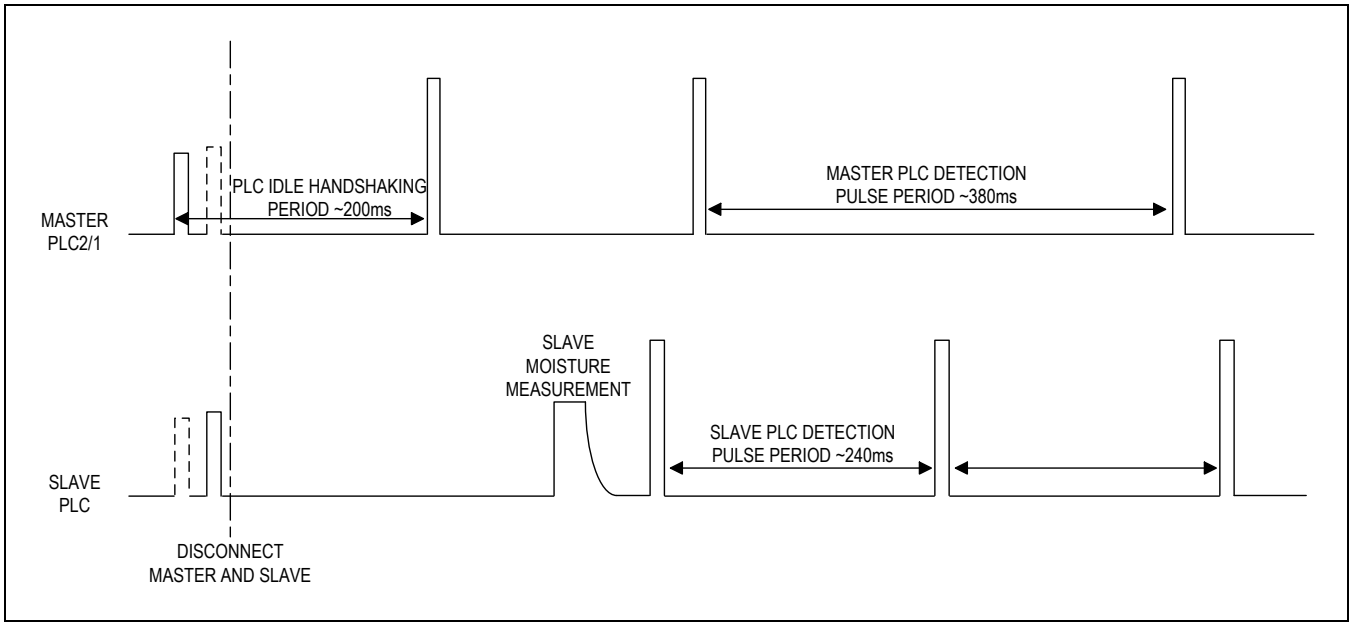


Figure 27. Master and Slave Disconnection While in PLC IDLE Mode

Master/Slave Resets and UBOOT Mode

The MAX20357 has PLC and I2C controllable resets. All the resets can be performed by local I2C write or by PLC command from its counterpart device. The MAX20355/MAX20357 performs reset for its counterpart device through SYST_REQ PLC command. See *Table 1* and *Table 2* for a detailed decode chart for reset commands. Different reset types are summarized in *Table 8*.

Table 8. Reset Types and Description

	DESCRIPTION	MASTER		SLAVE	
		PLC*	I2C	PLC*	I2C
Fuel Gauge Reset	Reset fuel gauge register	SYST_REQ FG reset	fg_ena_byp fg_ena_val	SYST_REQ FG reset	fg_ena_byp fg_ena_val
Soft Reset	Reset internal registers and FSMs Only PLC, not including RAM or fuel gauge	SYST_REQ Soft reset	soft_reset	SYST_REQ Soft reset	soft_reset
Hard Reset	Cycle the power at MAX20357 SYS pin MAX20357 charger is temporarily turned off	SYST_REQ Hard reset	—	—	hard_reset
Hard + Soft Reset	Soft reset + Hard reset	SYST_REQ X reset	—	—	sft_hrd_rst
UBOOT	Hard reset and enters UART mode	SYST_REQ UBOOT	—	—	uboot_i2c_cmd
Off Mode	Off mode	—	off_cmd_inp	—	off_cmd_inp
Seal Mode	MAX20357 Seal mode	SYST_REQ SEAL	—	—	seal_i2c_cmd

**PLC column lists the PLC commands that put its counterpart into the corresponding reset state*

General-Purpose Input Output (GPIO)

The MAX20355/MAX20357 each feature four general-purpose input/outputs (GPIO) controllable by its counterpart through PLC or local I2C write. Set GPIOPLCCtrx = 1 to control GPIOx by PLC, set GPIOPLCCtrx = 0 to control GPIO by I2C. When GPIOx is controlled by I2C, set GPIOEnResx = 1 to configure GPIOx as general-purpose input, set GPIOEnResx = 0 to configure GPIOx as general-purpose output.

When GPIOx is configured as general-purpose input (GPI), set GPIOEnPupx = 1 to have the GPIOx internally pulled up to the maximum of PLC line voltage and battery voltage, set GPIOEnPupx = 0 to have the GPIOx internally pulled down.

When GPIOx is configured as a general-purpose output (GPO), the GPO is in open-drain mode and requires an external pullup resistor (typically 10kΩ–100kΩ). Connect the external pullup resistor to a voltage rail that is higher than 1.4V (TYP). Set GPIODoutx = 1 to turn on the open-drain FET and output low, set GPIODoutx = 0 to turn off the open-drain FET and output high.

The GPI input status GPIODAInp4–GPIODAInp1 still functions properly and does not collide when the GPIO is configured as an output. In other words, GPIO status, either configured as input or as output, is stored in GPIODAInp4–GPIOAInp1.

Watchdog

The MAX20357 provides a watchdog function to reset the chip in case there is malfunction in slave SoC. Watchdog feature is enabled through wd_eoc_sel. There are three reset types: soft reset, hard reset, soft and hard reset. The reset types are I2C programmable also through wd_rst_type. wd_eoc_sel sets watchdog reset timer. If the watchdog is not serviced by reading wd__itr_clr with a period smaller than the timer limit, MAX20357 places a reset. Note that if the MAX20357 is in UART mode, hard reset, soft reset, hard and soft reset, or JEITA reset, the watchdog reset requests are queue and implemented until MAX20357 exits the listed modes. If the device is in SYSUVLO mode, OFF mode or SEAL mode, watchdog is disabled.

High ESD Protected ESD Outputs

High-ESD protection on the MAX20357 PLC pin protect the device from high energy ESD damage up to 8kV contact discharge.

ModelGauge M5 EZ Fuel Gauge with Integrated Sense Resistor

The MAX20355 and MAX20357 implement the Maxim ModelGauge m5 algorithm. The IC measures voltage, current, and temperature accurately to produce fuel gauge results. The ModelGauge m5 robust algorithm provides tolerance against battery diversity. This additional robustness enables simpler implementation for most applications and batteries by avoiding time-consuming battery characterization.

The ModelGauge m5 algorithm combines the short-term accuracy and linearity of a coulomb-counter with the long-term stability of a voltage-based fuel gauge, along with temperature compensation to provide industry-leading fuel gauge accuracy. The IC automatically compensates for aging, temperature, and discharge rate and provides an accurate state of charge (SOC) in percentage (%) and remaining capacity in milliampere-hours (mAhr) over a wide range of operating conditions. Fuel gauge error always converges to 0% as the cell approaches empty. The IC provides accurate estimation of time-to-empty and time-to-full and provides three methods for reporting the age of the battery: reduction in capacity, increase in battery resistance, and cycle odometer.

The IC contains a unique serial number. It can be used for cloud-based authentication. See the *Serial Number Feature* section for more information.

Communication to the host occurs over the standard I^2C interface.

ModelGauge m5 EZ Performance

The ModelGauge m5 EZ performance provides plug-and-play operation when the IC is connected to most lithium batteries. While the IC can be custom-tuned to the application's specific battery through a characterization process for ideal performance, the IC can provide good performance for most applications with no custom characterization required. *Table 9* and *Figure 28* show the performance of the ModelGauge m5 algorithm in applications using the ModelGauge m5 EZ configuration.

The ModelGauge m5 EZ provides good performance for most cell types. For some chemistries, such as lithium-iron-phosphate ($LiFePO_4$) and Panasonic NCR/NCA series cells, it is suggested that the customer request a custom model from Maxim for best performance.

For even better fuel-gauging accuracy than ModelGauge m5 EZ, contact Maxim for information regarding cell characterization.

Table 9. ModelGauge m5 EZ Performance

DESCRIPTION	AFTER FIRST CYCLE* (%)	AFTER SECOND CYCLE* (%)
Tests with less than 3% error	95	97
Tests with less than 5% error	98.7	99
Tests with less than 10% error	100	100

**Test conditions: +20°C and +40°C, run time of > 3 hours.*

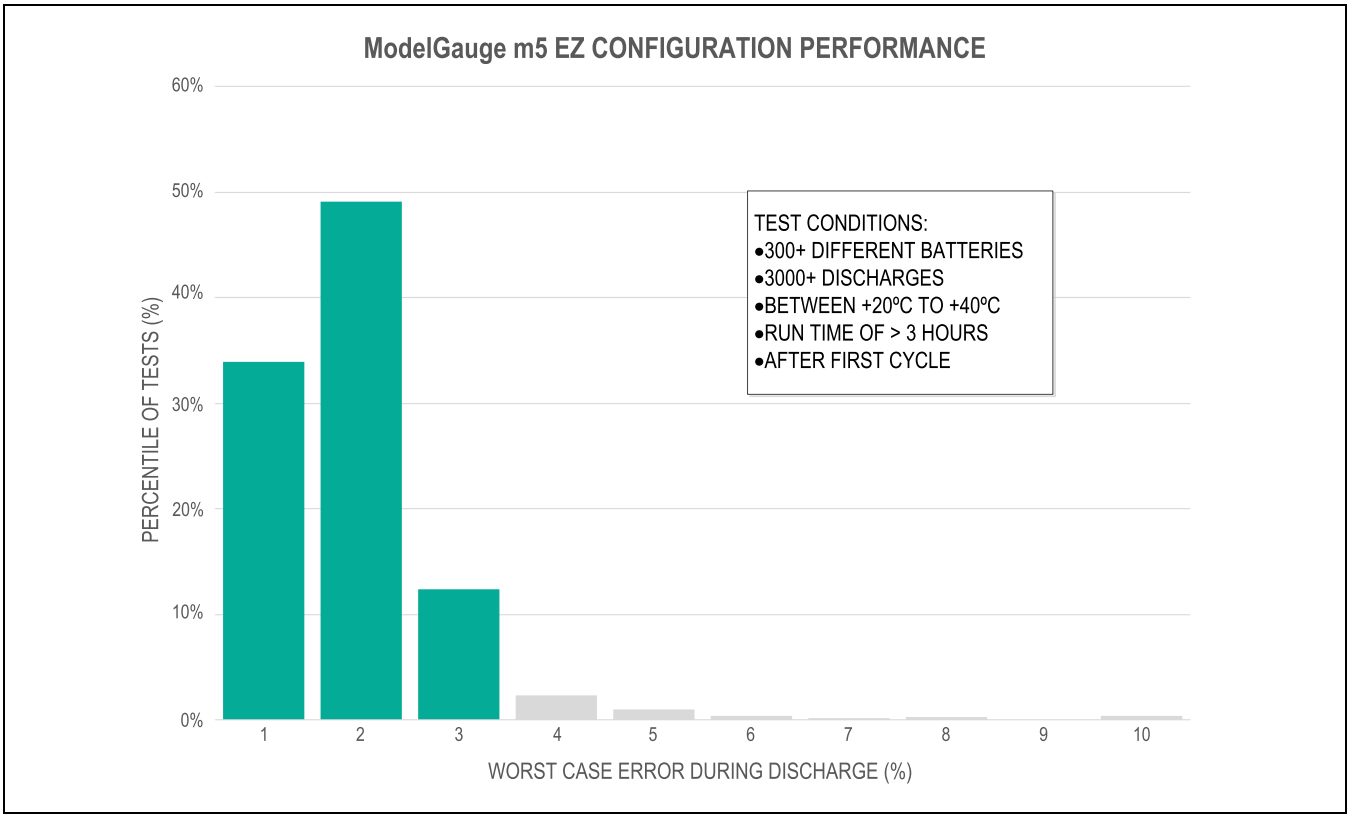


Figure 28. ModelGauge m5 EZ Configuration Performance

Application Notes

Refer to the following application notes for additional reference material:

User Guide 6597: MAX1726x ModelGauge m5 EZ User Guide

- Documents full register set
- More details about ModelGauge m5 algorithm
- Discusses additional applications

User Guide 6595: MAX1726x Software Implementation Guide

- Guidelines for software drivers including example code

Standard Register Formats

Unless otherwise stated during a given register's description, all fuel gauge registers of the MAX77658 follow the same format depending on the type of register. See *Table 10* for the resolution and range of any register described hereafter.

Table 10. ModelGauge m5 Register Standard Resolutions

REGISTER TYPE	LSB SIZE	MINIMUM VALUE	MAXIMUM VALUE	NOTES
Capacity	0.125mAh	0.0mAh	8191.9mAh	
Percentage	1/256%	0.0%	255.9961%	1% LSb when reading only the upper byte.
Voltage	1.25mV/16	0.0V	5.11992V	
Current	39.06µA	-1.28A	1.27996A	Signed two's-complement format.
Temperature	1/256°C	-128.0°C	127.996°C	Signed two's-complement format. 1°C LSb when reading only the upper byte.
Resistance	1/4096Ω	0.0Ω	15.99976Ω	
Time	5.625s	0.0s	102.3984h	

Special				Format details are included with the register description.

ModelGauge m5 Algorithm

Classical coulomb-counter-based fuel gauges have excellent linearity and short-term performance. However, they suffer from drift due to the accumulation of the offset error in the current-sense measurement. Although the offset error is often very small, it cannot be eliminated. It causes the reported capacity error to increase over time and requires periodic corrections. Corrections are traditionally performed at full or empty. Some other systems also use the relaxed battery voltage to perform corrections. These systems determine the true state-of-charge (SOC) based on the battery voltage after a long time of no current flow. Both have the same limitation: if the correction condition is not observed over time in the actual application, the error in the system is boundless. The performance of classic coulomb counters is dominated by the accuracy of such corrections. Voltage measurement-based SOC estimation has accuracy limitations due to imperfect cell modeling but does not accumulate offset error over time.

The MAX20355/MAX20357 includes an advanced voltage fuel gauge (VFG) that estimates open-circuit voltage (OCV), even during current flow, and simulates the nonlinear internal dynamics of a Li+ battery to determine the SOC with improved accuracy. The model considers the time effects of a battery caused by the chemical reactions and impedance in the battery to determine SOC. This SOC estimation does not accumulate offset error over time. The IC performs a smart empty compensation algorithm that automatically compensates for the effect of temperature condition and load condition to provide accurate state-of-charge information. The converge-to-empty function eliminates error toward an empty state. The IC learns battery capacity over time automatically to improve long-term performance. The age information of the battery is available in the output registers.

The ModelGauge m5 algorithm combines a high-accuracy coulomb counter with a VFG. See *Figure 29*. The complementary combined result eliminates the weaknesses of both the coulomb counter and the VFG while providing the strengths of both. A mixing algorithm combines the VFG capacity with the coulomb counter and weighs each result so that both are used optimally to determine the battery state. In this way, the VFG capacity result is used to continuously make small adjustments to the battery state, cancelling the coulomb-counter drift.

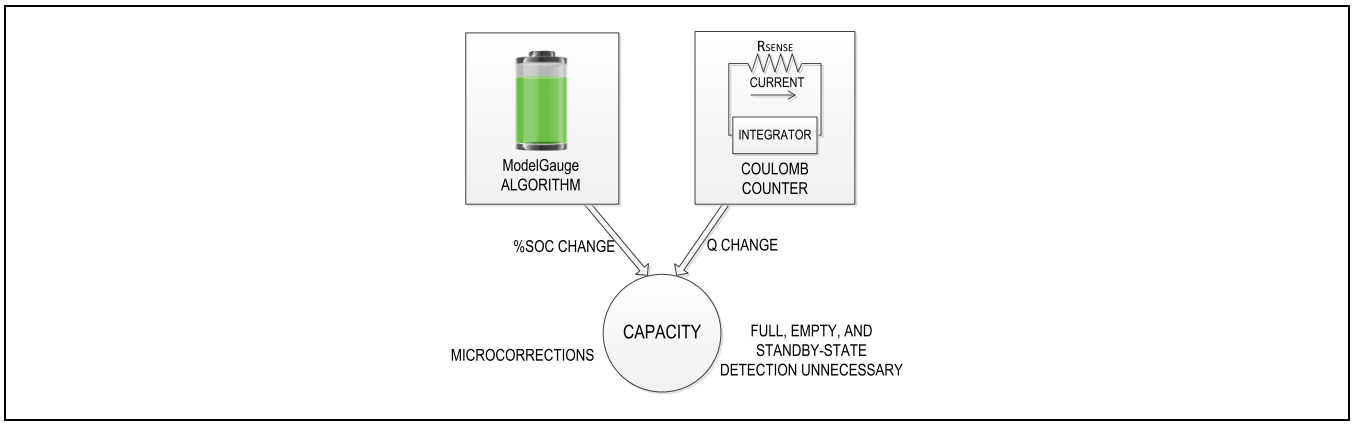


Figure 29. ModelGauge m5 Algorithm

The ModelGauge m5 algorithm uses this battery state information and accounts for temperature, battery current, age, and application parameters to determine the remaining capacity available to the system. As the battery approaches the critical region near empty, the ModelGauge m5 algorithm invokes a special error correction mechanism that eliminates any error.

The ModelGauge m5 algorithm continually adapts to the cell and application through independent learning routines. As the cell ages, its change in capacity is monitored and updated and the voltage-fuel-gauge dynamics adapt based on cell-voltage behavior in the application.

Analog Measurements

Voltage Measurement

VCell Register (0x09)

Register Type: Voltage
VCell reports the voltage measured between BATT and GND

AvgVCell Register (0x19)

Register Type: Voltage
The AvgVCell register reports an average of the VCell register readings.

MaxMinVolt Register (0x1B)

Register Type: Special

Initial Value: 0x00FF

The MaxMinVolt register maintains the maximum and minimum of VCell register values since the device reset. At power-up, the maximum voltage value is set to 0x00 (the minimum) and the minimum voltage value is set to 0xFF (the maximum). Therefore, both values are changed to the voltage register reading after the first update. Host software can reset this register by writing it to its power-up value of 0x00FF. The maximum and minimum voltages are each stored as 8-bit values with a 20mV resolution.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MaxVCELL								MinVCELL							

MaxVCELL: Maximum VCell register reading

MinVCELL: Minimum VCell register reading

Current Measurement

Current Register (0x0A)

Register Type: Current

The MAX20355/MAX20357 uses internal current sensing to monitor the current through the SYS FG pin. The measurement value is stored in two's-complement format. Measurement that exceeds maximum and minimum current range is stored as maximum and minimum values. The current register has a LSB value of 31.25µA, a register scale range of ±1.024A, and an allowable measurement range as described in the *Absolute Maximum Ratings*.

AvgCurrent Register (0x0B)

Register Type: Current

The AvgCurrent register reports an average of current register readings.

MaxMinCurr Register (0x1C)

Register Type: Special

Initial Value: 0x807F

The MaxMinCurr register maintains the maximum and minimum current register values since the last IC reset or until cleared by host software. At power-up, the maximum current value is set to (most negative) and the minimum current value is set to 7Fh (most positive). Therefore, both values are changed to the current register reading after the first update. Host software can reset this register by writing it to its power-up value of 0x807F. The maximum and minimum currents are each stored as two's complement 8-bit values with 160mA resolution.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MaxCurrent								MinCurrent							

MaxCurrent: Maximum Current register reading

MinCurrent: Minimum Current register reading

Temperature Measurement

Temp Register (0x08)

Register Type: Temperature

The Temp register provides the temperature measured by the thermistor or die temperature based on the Conifg register setting.

MaxMinTemp Register (0x1A)

Register Type: Special Initial Value: 0x807F

The MaxMinTemp register maintains the maximum and minimum Temp register (0x08) values since the last fuel-gauge reset or until cleared by host software. At power-up, the maximum value is set to 0x80 (most negative) and the minimum value is set to 0x7F (most positive). Therefore, both values are changed to the Temp register reading after the first update. Host software can reset this register by writing it to its power-up value of 0x807F. The maximum and minimum temperatures are each stored as two's complement 8-bit values with 1°C resolution.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MaxTemperature								MinTemperature							

MaxTemperature: Maximum Temp register reading

MinTemperature: Minimum Temp register reading

DieTemp Register (0x34)

Register Type: Temperature

The DieTemp register provides the internal die temperature measurement. If Config.TSel = 0, DieTemp and Temp registers have the value of the die temperature.

Power Measurement

Power Register (0xB1)

Instant power calculation from immediate current and voltage. The LSB is 1.6mW.

AvgPower Register (0xB3)

Filtered Average Power from the power register. LSB is 1.6mW.

Alert Function

The Alert Threshold registers allow interrupts to be generated by detecting a high or low voltage, current, temperature, or state-of-charge. Interrupts are generated on the $\overline{ALRT}$ pin open-drain output driver. An external pullup is required to generate a logic-high signal. Alerts can be triggered by any of the following conditions:

- Battery removal: ($V_{TH} > V_{BAT} - V_{DET}$) and battery removal detection enabled (Ber = 1).
- Battery insertion: ($V_{TH} < V_{BAT} - V_{DET-HYS}$) and battery insertion detection enabled (Bei = 1).
- Over/undervoltage: VAlrtTh register threshold violation (upper or lower) and alerts enabled (Aen = 1).
- Over/undertemperature: TAlrtTh register threshold violation (upper or lower) and alerts enabled (Aen = 1).
- Over/undercurrent: IAlrtTh register threshold violation (upper or lower) and alerts enabled (Aen = 1).
- Over/under SOC: SAlrtTh register threshold violation (upper or lower) and alerts enabled (Aen = 1).
- 1% SOC change: RepSOC register bit d8 (1% bit) changed (dSOCen = 1).

To prevent false interrupts, the threshold registers should be initialized before setting the Aen bit. Alerts generated by battery insertion or removal can only be reset by clearing the corresponding bit in the Status (0x00) register. Alerts generated by a threshold-level violation can be configured to be cleared only by software or cleared automatically when

the threshold level is no longer violated. See the Config (1Dh) and Config2 (BBh) register descriptions for details of the alert function configuration.

Serial Number Feature

Each IC provides a unique serial number ID. To read this serial number, clear the AtRateEn and the DPEn bit in the Config2 register. The 128-bit serial information overwrites the Dynamic Power and AtRate output registers. To continue Dynamic Power and AtRate operations after reading the serial number, the host should set Config2.AtRateEn and Config2.DPEn to 1.

Table 11. Serial Number Format

ADDRESS	Config2.AtRateEn = 1 || Config2.DPEn = 1	Config2.AtRateEn = 0 && Config2.DPEn = 0
0xD4	MaxPeakPower	Serial Number Word0
0xD5	SusPeakPower	Serial Number Word1
0xD9	MPPCurrent	Serial Number Word2
0xDA	SPPCurrent	Serial Number Word3
0xDC	AtQResidual	Serial Number Word4
0xDD	AtTTE	Serial Number Word5
0xDE	AtAvSoc	Serial Number Word6
0xDF	AtAvCap	Serial Number Word7

ModelGauge m5 Memory Space

Registers that relate to functionality of the ModelGauge m5 fuel gauge are located on pages 0h-4h and are continued on pages Bh and Dh. See the *ModelGauge m5 Algorithm* section for details of specific register operation. Register locations marked reserved should not be written to.

Table 12. ModelGauge m5 Register Memory Map

PAGE/WORD	00h	10h	20h	30h	40h	B0h	D0h
0h	Status	FullCapRep	TTF	Reserved	Reserved	Status2	RSense / UserMem3
1h	VAlrtTh	TTE	DevName	Reserved	Reserved	Power	ScOcvLim
2h	TAlrtTh	QRTable00	QRTable10	QRTable20	QRTable30	ID / UserMem2	VGain
3h	SAlrtTh	FullSocThr	FullCapNom	Reserved	RGain	AvgPower	SOCHold
4h	AtRate	RCell	Reserved	DieTemp	Reserved	IAlrtTh	MaxPeakPower
5h	RepCap	Reserved	Reserved	FullCap	dQAcc	TTFCfg	SusPeakPower
6h	RepSOC	AvgTA	Reserved	Reserved	dPAcc	CVMixCap	PackResistance
7h	Age	Cycles	AIN	Reserved	Reserved	CVHalfTime	SysResistance
8h	Temp	DesignCap	LearnCfg	RComp0	Reserved	CGTempCo	MinSysVoltage
9h	VCell	AvgVCell	FilterCfg	TempCo	ConvgCfg	Curve	MPPCurrent
Ah	Current	MaxMinTemp	RelaxCfg	VEmpty	VFRemCap	HibCfg	SPPCurrent
Bh	AvgCurrent	MaxMinVolt	MiscCfg	Reserved	Reserved	Config2	ModelCfg
Ch	QResidual	MaxMinCurr	TGain	Reserved	Reserved	VRipple	AtQResidual
Dh	MixSOC	Config	TOff	FStat	QH	RippleCfg	AtTTE
Eh	AvSOC	IChgTerm	CGain	Timer	Reserved	TimerH	AtAvSOC
Fh	MixCap	AvCap	COff	ShdnTimer	Reserved	Reserved	AtAvCap

I²C Serial Communication

General Description

The IC features a revision 3.0 I²C-compatible, 2-wire serial interface consisting of a bidirectional serial data line (SDA) and a serial clock line (SCL). This device acts as a slave-only device, relying on the master to generate a clock signal. SCL clock rates from 0Hz to 400kHz are supported.

I²C is an open-drain bus and therefore SDA and SCL require pullups. Optional resistors (24Ω) in series with SDA and SCL protect the device inputs from high-voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot on bus signals.

Figure 30 shows the functional diagram for the I²C based communications controller. For additional information on I²C, refer to the I²C Bus Specification and User Manual which is available for free through the internet.

Features

- I²C Revision 3.0 compatible serial communications channel
- Compatible with any bus timing up to 400kHz
- Does not utilize I²C clock stretching

I²C Simplified Block Diagram

There are three pins (aside from GND) for the I²C-compatible interface. V_{IO} determines the logic level, SCL is the clock line, and SDA is the data line. Note that the interface cannot drive the SCL line.

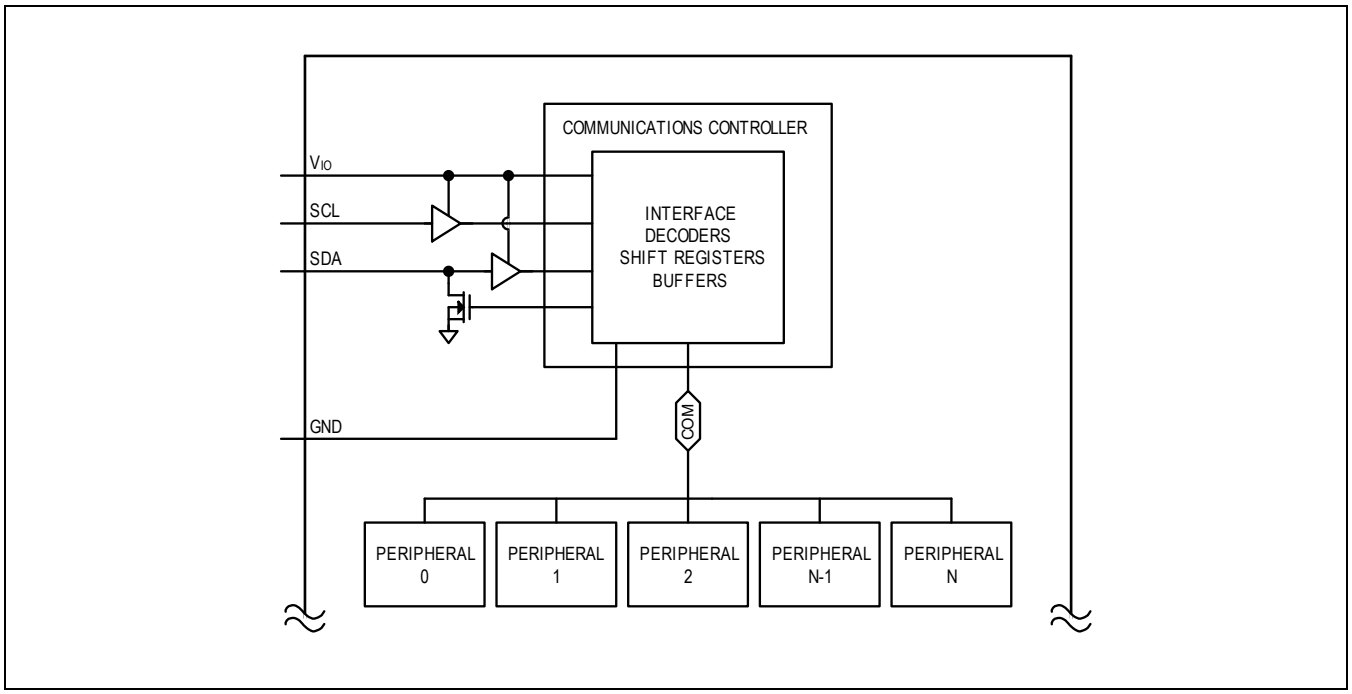


Figure 30. I²C Simplified Block Diagram

I²C System Configuration

The I²C-compatible interface is a multimaster bus. The maximum number of devices that can attach to the bus is only limited by bus capacitance.

A device on the I²C bus that sends data to the bus is called a transmitter. A device that receives data from the bus is called a receiver. The device that initiates a data transfer and generates the SCL clock signals to control the data transfer

is a master. Any device that is being addressed by the master is considered a slave. The I2C-compatible interface operates as a slave on the I2C bus with transmit and receive capabilities.

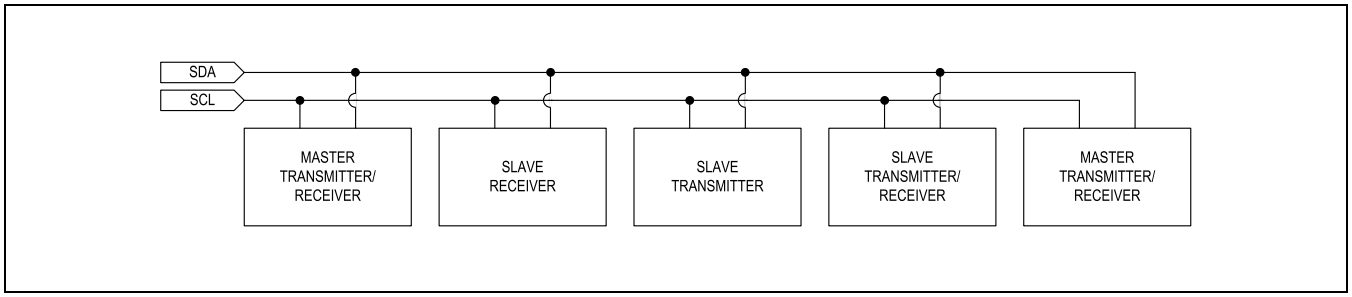


Figure 31. I2C System Configuration

I2C Interface Power

The I2C interface derives its power from V_{IO}. Typically, a power input such as V_{IO} would require a local 0.1µF ceramic bypass capacitor to ground. However, in highly integrated power distribution systems, a dedicated capacitor might not be necessary. If the impedance between V_{IO} and the next closest capacitor (≥ 0.1µF) is less than 100mΩ in series with 10nH, then a local capacitor is not needed. Otherwise, bypass V_{IO} to GND with a 0.1µF ceramic capacitor.

V_{IO} accepts voltages from 1.7V to 3.6V (V_{IO}). Cycling V_{IO} does not reset the I2C registers. When V_{IO} is less than V_{IOUVLO} and V_{SYSA} is less than $V_{SYSAUVLO}$, SDA and SCL are high impedance.

I2C Data Transfer

One data bit is transferred during each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA, while SCL is high, are control signals. See the *I2C Start and Stop Conditions* section. Each transmit sequence is framed by a START (S) condition and a STOP (P) condition. Each data packet is nine bits long: eight bits of data followed by the acknowledge bit. Data is transferred with the MSB first.

I2C Start and Stop Conditions

When the serial interface is inactive, SDA and SCL idle high. A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA, while SCL is high. See *Figure 32*.

A START condition from the master signals the beginning of a transmission to the device. The master terminates transmission by issuing a not-acknowledge followed by a STOP condition (see the *I2C Acknowledge Bit* section for information on not-acknowledge). The STOP condition frees the bus. To issue a series of commands to the slave, the master can issue repeated start (Sr) commands instead of a STOP command to maintain control of the bus. In general, a repeated start command is functionally equivalent to a regular start command.

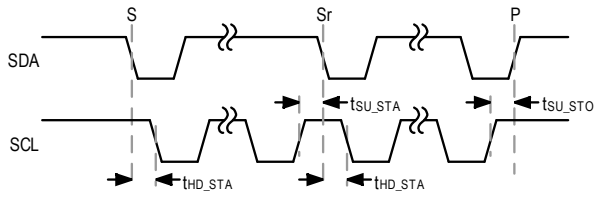


Figure 32. I2C Start and Stop Conditions

I2C Acknowledge Bit

Both the I2C bus master and slave devices generate acknowledge bits when receiving data. The acknowledge bit is the last bit of each ninth-bit data packet. To generate an acknowledge (A), the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse. See *Figure 33*. To generate a not-acknowledge (nA), the receiving device allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse and leaves it high during the high period of the clock pulse.

Monitoring the acknowledge bits allows for the detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time.

This device issues an ACK for all register addresses in the possible address space even if the particular register does not exist.

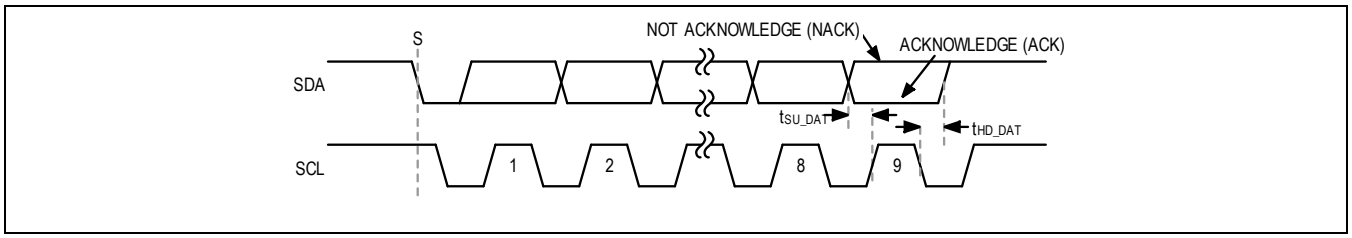


Figure 33. Acknowledge Bit

I²C Slave Address

The I²C controller implements 7-bit slave addressing. The registers of the MAX20355/MAX20357 are divided into three blocks with separate slave addresses:

- The main block includes all the registers for the global resource, the power line communication, and the buck-boost regulator (MAX20355)/the charger (MAX20357). All the registers in the main block are 8-bit registers.
- The fuel gauge block includes all the registers for the fuel gauging. The fuel gauge registers are in 16-bit word.
- The RAM block is 128-byte space for mailbox and bulk data transfer. The RAM registers are 8-bit.

MAX20355 ADDRESS	7-BIT SLAVE ADDRESS	8-BIT WRITE ADDRESS	8-BIT READ ADDRESS
PLC Address	0x28, 0b 010 1000	0x50, 0b 0101 0000	0x51, 0b 0101 0001
Fuel Gauge Address	0x36, 0b 011 0110	0x6C, 0b 0110 1100	0x6D, 0b 0110 1101
RAM Address	0x40, 0b 100 0000	0x80, 0b 1000 0000	0x81, 0b 1000 0001
MAX20357 ADDRESS	**7-BIT SLAVE ADDRESS**	**8-BIT WRITE ADDRESS**	**8-BIT READ ADDRESS**
PLC Address	0x15, 0b 001 0101	0x2A, 0b 0010 1010	0x2B, 0b 0010 1011
Fuel Gauge Address	0x36, 0b 011 0110	0x6C, 0b 0110 1100	0x6D, 0b 0110 1101
RAM Address	0x55, 0b 101 0101	0xAA, 0b 1010 1010	0xAB, 0b 1010 1011

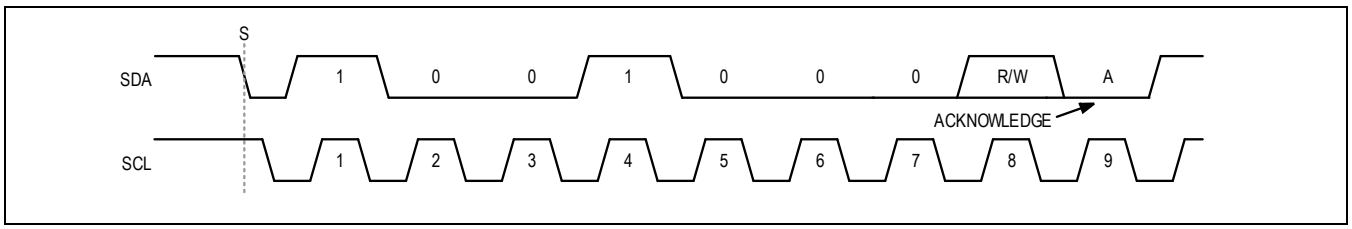


Figure 34. Slave Address Example

I²C Clock Stretching

In general, the clock signal generation for the I²C bus is the responsibility of the master device. The I²C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. The IC does not use any form of clock stretching to hold down the clock line.

I²C General Call Address

This device does not implement the I²C specifications general call address and does not acknowledge the general call address (0b0000_0000).

I²C Device ID

This device does not support the I²C Device ID feature.

I²C Communication Speed

This device is compatible with any bus timing up to 400kHz. The main consideration when changing bus speed through this range is the combination of the bus capacitance and pullup resistors. Larger values of bus capacitance and pullup resistance increase the time constant (C x R), slowing bus operation. Therefore, when increasing bus speeds, the pullup resistance must be decreased to maintain a reasonable time constant. Refer to the *Pullup Resistor Sizing* section of the I²C Bus Specification and User Manual (available for free on the internet) for detailed guidance on the pullup resistor selection. In general, for bus capacitances of 200pF, a 100kHz bus needs 5.6kΩ pullup resistors, and a 400kHz bus needs about 1.5kΩ pullup resistors. Remember that, while the open-drain bus is low, the pullup resistor is dissipating power, and lower value pullup resistors dissipate more power (V^2/R).

Operating in high-speed mode requires some special considerations. For a full list of considerations, refer to the publicly available I²C Bus Specification and User Manual. Major considerations concerning this part are:

- The I²C bus master uses current source pullups to shorten the signal rise.
- The I²C slave must use a different set of input filters on its SDA and SCL lines to accommodate for the higher bus.
- The communication protocols need to utilize the high-speed master code.

At power-up and after each stop condition, the bus input filters are set for standard mode, fast mode, and fast-mode plus (i.e., 0Hz to 1MHz). To switch the input filters for high-speed mode, use the high-speed master code protocols that are described in the *I2C Communication Protocols* section.

I²C Communication Protocols

Both writing to and reading from registers are supported as described in the following subsections.

Writing to a Single 8-bit Register

Figure 35 shows the protocol for the I²C master device to write one byte of data to this device. This protocol is the same as the SMBus specification's write-byte protocol.

The write byte protocol is as follows:

1. The master sends a start command (S).
2. The master sends the 7-bit slave address followed by a write bit ($R/\overline{W} = 0$).
3. The addressed slave asserts an acknowledge (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave updates with the new data.
8. The slave acknowledges or not acknowledges the data byte. The next rising edge on SDA loads the data byte into its target register and the data becomes active.
9. The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

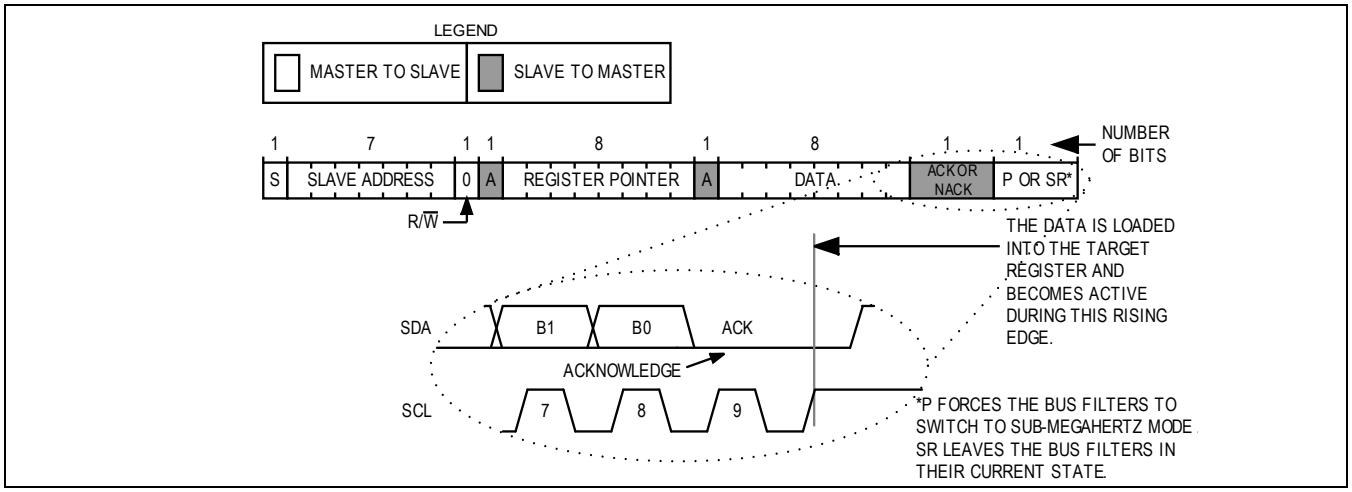


Figure 35. Writing to a Single 8-bit Register with the Write Byte Protocol

Writing Multiple Bytes to Sequential Registers

Figure 36 shows the protocol for writing to sequential registers. This protocol is similar to the write byte protocol above, except the master continues to write after it receives the first byte of data. When the master is done writing, it issues a stop or repeated start.

The writing to sequential registers protocol is as follows:

1. The master sends a start command (S).
2. The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).
3. The addressed slave asserts an acknowledge (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave acknowledges the data byte. The next rising edge on SDA loads the data byte into its target register and the data becomes active.
8. Steps 6 to 7 are repeated as many times as the master requires.
9. During the last acknowledge-related clock pulse, the master can issue an acknowledge or a not acknowledge.
10. The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

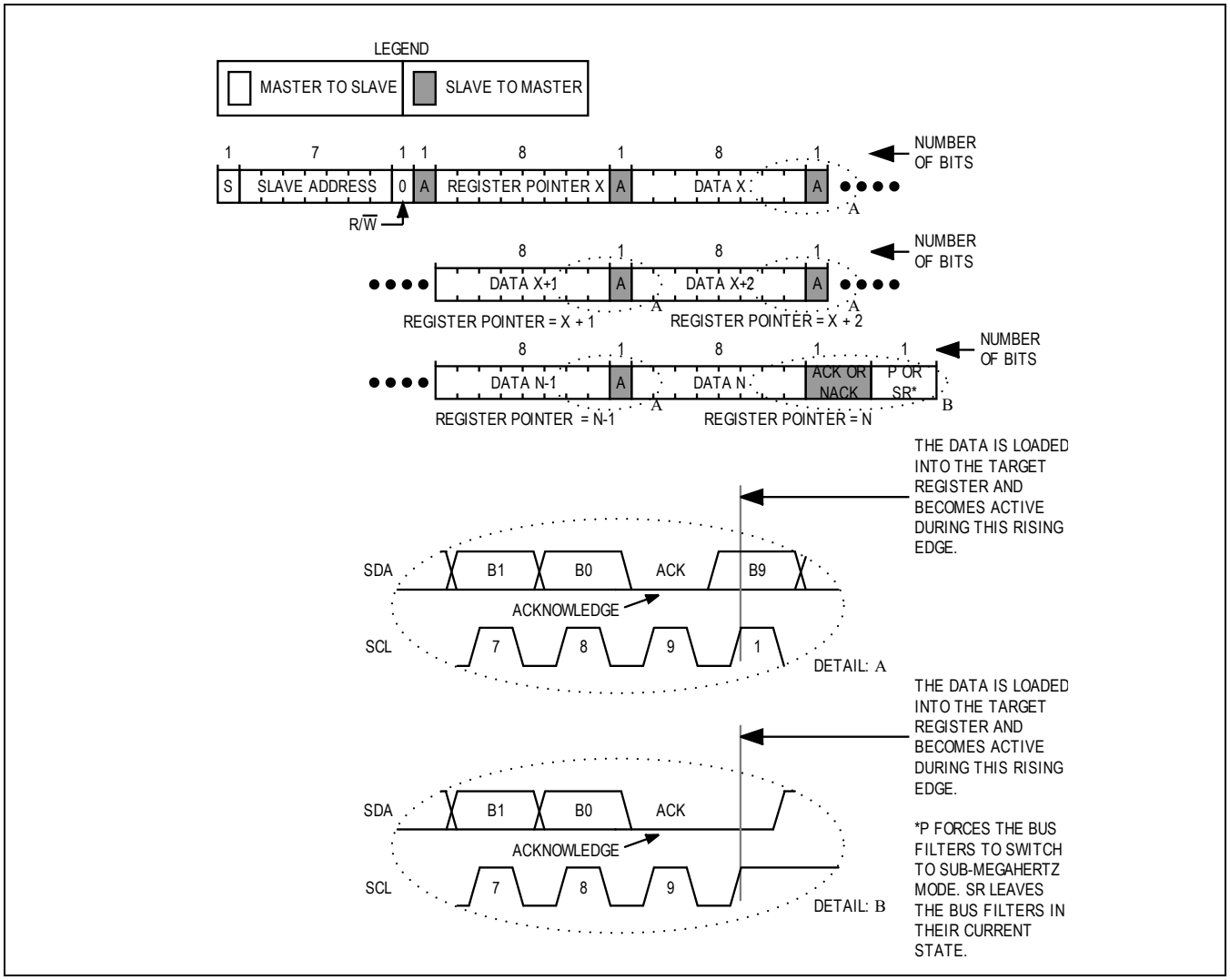


Figure 36. Writing to Sequential Registers X to N

Writing to 16-bit Registers

The Write Data protocol is used to transmit data to the registers of the fuel gauge at memory addresses from 00h to FFh. Addresses 00h to FFh can be written as a block. The memory address is sent by the bus master as a single byte value immediately after the slave address. The LSB of the data to be stored is written immediately after the memory address byte is acknowledged. Because the address is automatically incremented after the last bit of each 16-bit word received by the IC, the LSB of the data at the next memory address can be written immediately after the acknowledgment of the MSB of data at the previous address. The master indicates the end of a write transaction by sending a STOP or Repeated START after receiving the last acknowledge bit. If the bus master continues an auto-incremented write transaction beyond address FFh, the IC ignores the data. Data is also ignored on writes to read-only addresses but not reserved addresses. Do not write to reserved address locations. See *Figure 37* for an example of the Write Data communication sequence.

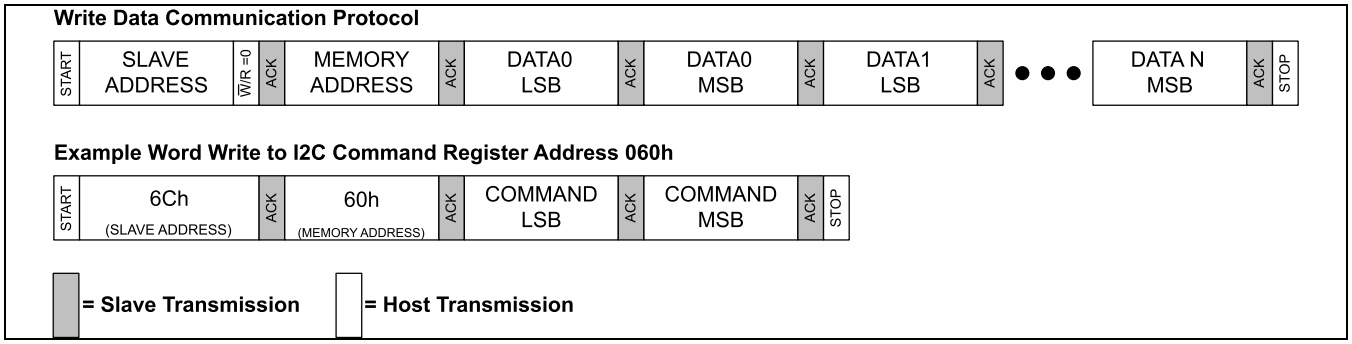


Figure 37. Example I²C Write 16-bit Data Communication Sequence

Reading from a Single Register

Figure 38 shows the protocol for the I²C master device to read one byte of data. This protocol is the same as the SMBus specification's read-byte protocol.

The read byte protocol is as follows:

1. The master sends a start command (S).
2. The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).
3. The addressed slave asserts an acknowledge (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a repeated start command (Sr).
7. The master sends the 7-bit slave address followed by a read bit (R/$\overline{W}$ = 1).
8. The addressed slave asserts an acknowledge by pulling SDA low.
9. The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
10. The master issues a not acknowledge (nA).
11. The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

Note that when this device receives a stop, the register pointer is not modified. Therefore, if the master re-reads the same register, it can immediately send another read command, omitting the command to send a register pointer.

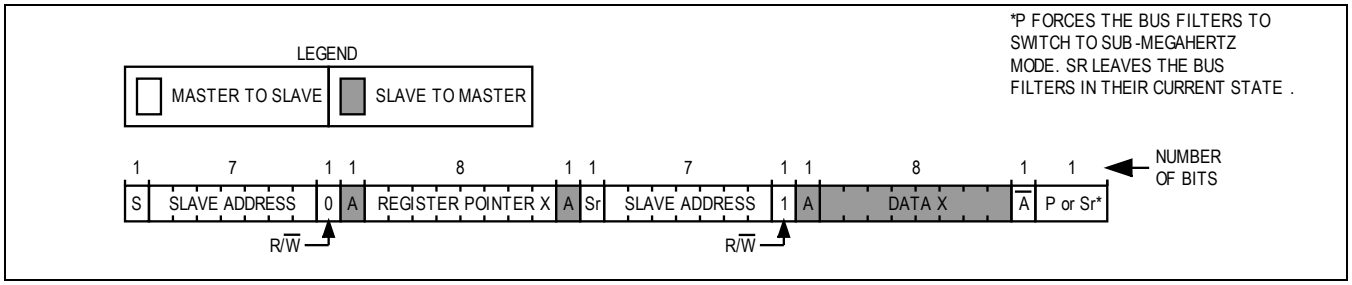


Figure 38. Reading from a Single Register with the Read Byte Protocol

Reading from Sequential Registers

Figure 39 shows the protocol for reading from sequential registers. This protocol is similar to the read byte protocol except the master issues an acknowledge to signal the slave that it wants more data: when the master has all the data it requires it issues a not acknowledge (nA) and a stop (P) to end the transmission.

The continuous read from sequential registers protocol is as follows:

1. The master sends a start command (S).
2. The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).
3. The addressed slave asserts an acknowledge (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.

5. The slave acknowledges the register pointer.
6. The master sends a repeated start command (Sr).
7. The master sends the 7-bit slave address followed by a read bit (R/$\overline{W}$ = 1).
8. The addressed slave asserts an acknowledge by pulling SDA low.
9. The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
10. The master issues an acknowledge (A) signaling the slave that it wishes to receive more data.
11. Steps 9 to 10 are repeated as many times as the master requires. Following the last byte of data, the master must issue a not acknowledge (nA) to signal that it wishes to stop receiving data.
12. The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a stop (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

Note that when this device receives a stop it does not modify its register pointer. Therefore, if the master re-reads the same register, it can immediately send another read command, omitting the command to send a register pointer.

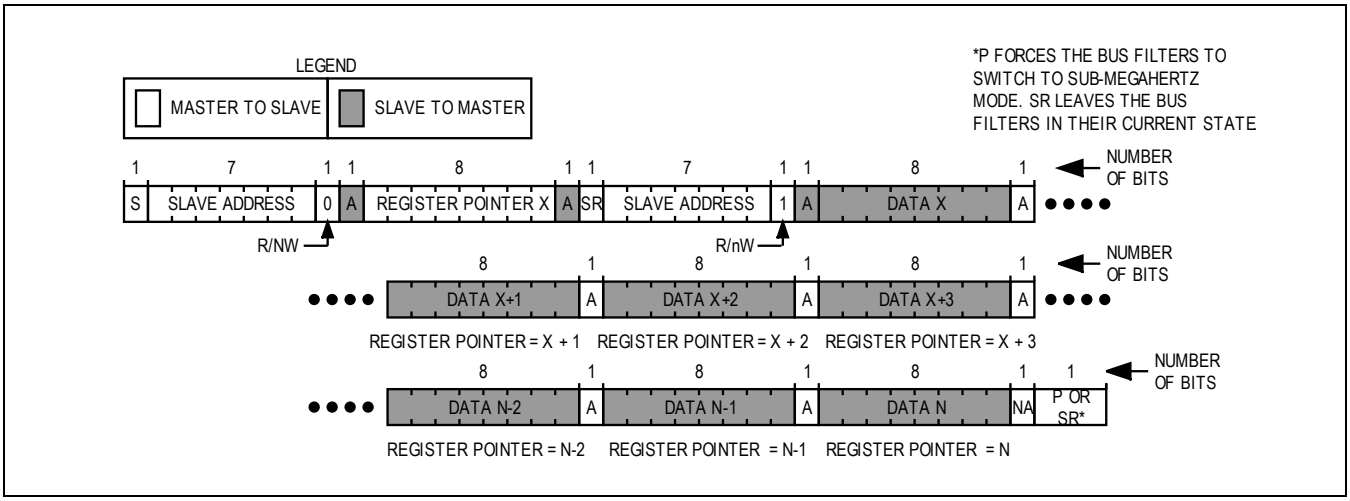


Figure 39. Reading Continuously from Sequential Registers X to N

Applications Information

PLC Current Sink and Detection Threshold

The MAX20355 and MAX20357 PLC sink current and detection threshold are specially paired to maintain good performance. Buck-boost ripple is the major source of noise inside the system. The MAX20355 self-cancels the effect of the buck-boost ripple since the noise is created by itself. The MAX20357 is not able to cancel the noise. To compensate for the ripple noise, all the PLC sink current PLCSnkSel options of the MAX20355 are higher than MAX20357 PLC sink current as shown in *Table 13* and *Table 14*.

Table 13. PLC Detection Pair (MAX20355 Data Packet)

DECODE	MAX20355 PLCSnkSel	MAX20357 PLCThrSel
0b00	88mA	75mV
0b01	105.4mA	90mV
0b10	123mA	105mV
0b11	140.5mA	120mV

Table 14. PLC Detection Pair (MAX20357 Data Packet)

DECODE	MAX20357 PLCSnkSel	MAX20355 PLCThrSel
0b00	50.3mA	40mV
0b01	70.4mA	56mV
0b10	90.4mA	70mV

0b11	110.5mA	84mV

PLC voltage detection threshold needs to be placed in the middle of the PLC signal for better performance. For each MAX20355 sink current PLCSnkSel, the MAX20357 offers one paired voltage detection threshold PLCThrSel. Make sure always use the same code for the MAX20355 PLCSnkSel and the MAX20357 PLCThrSel (*Table 13*). Similarly, use the same code for the MAX20357 PLCSnkSel and the MAX20355 PLCThrSel (*Table 14*). It is recommended to start from code '00'. If the external noise is too strong and code '00' does not offer good performance, increase the sink current by moving to larger codes. Note there is a tradeoff between susceptibility to noise and power consumption. Higher sink current offers a better anti-interference ability, but also higher power consumption.

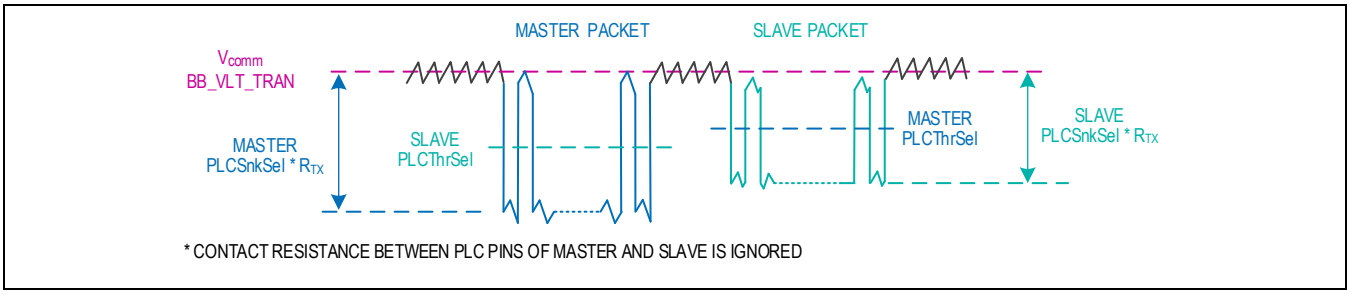


Figure 40. PLC Current Sink and Detection Threshold

Typical Application Circuit

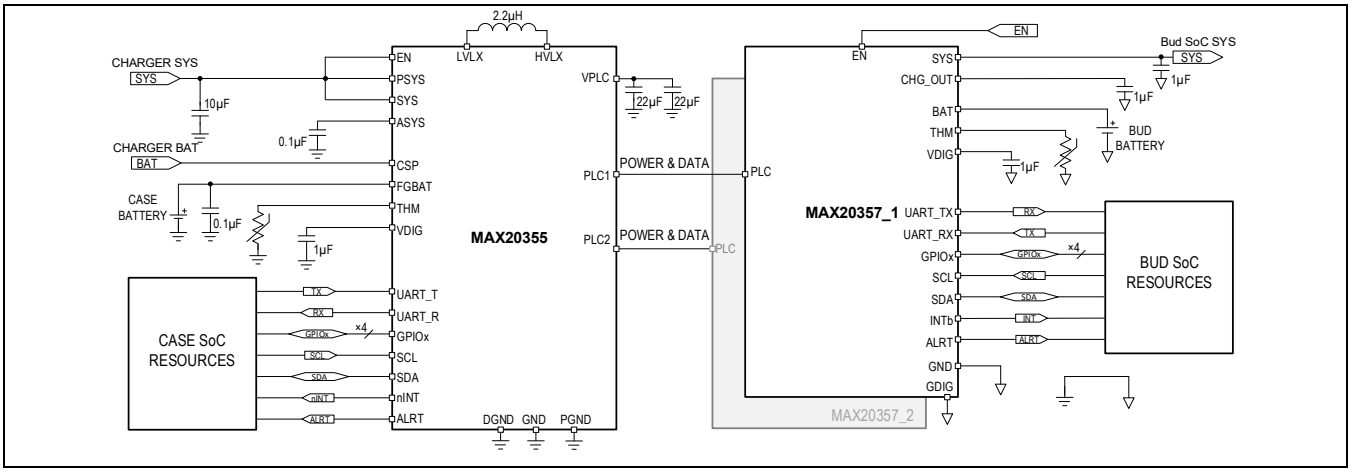


Figure 41. Typical Application Circuit

PCB Layout Guidelines

Figure 42 shows a PCB layout example. Please take following guidelines as references to design the PCB:

1. Place the SYS capacitor (C_{SYS}) close to the SYS pin.
2. Place the CHG_OUT capacitor (C_{CHG_OUT}) close to the CHG_OUT pin.
3. Place the VDIG capacitor (C_{VDIG}) close to the VDIG pin. Proximity to the IC provides a stable supply for the internal circuitry.
4. Keep the power traces and load connections short and wide. This is to minimize PCB conduction loss and to improve the heat dissipation.
5. Multiple vias are recommended for all paths that carry high currents (PLC, SYS, and BAT). Placements of vias should create the shortest possible current loops and must not obstruct the flow of currents or mirror currents in the ground plane.
6. Do not neglect ceramic capacitor DC voltage derating. Choose capacitor values and case sizes carefully. Select ceramic capacitors that maintain capacitance over temperature and DC bias.

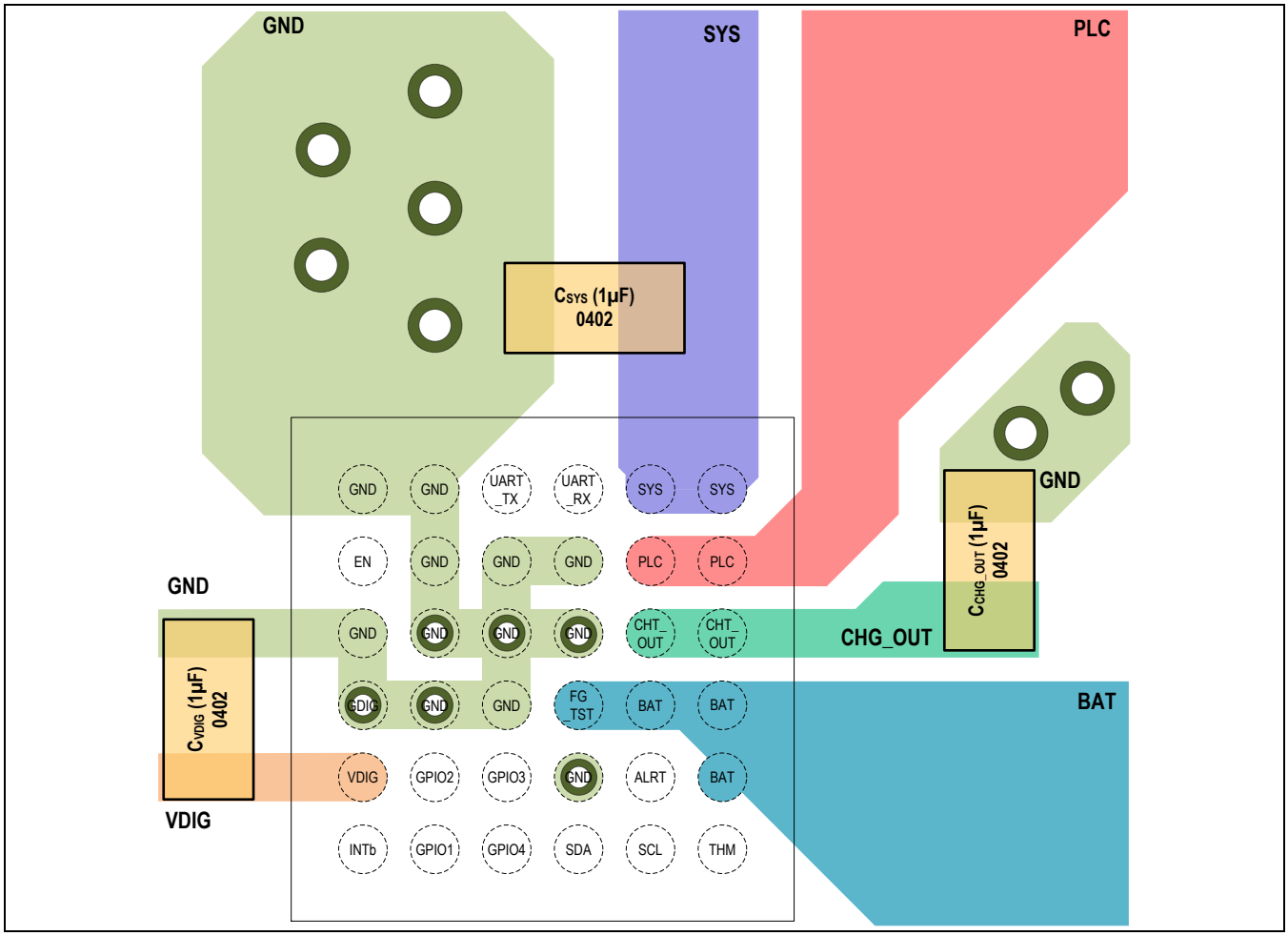


Figure 42. Layout Guideline

Register Map

MAX20357 (Slave address 0x15)

ADDRESS	NAME	MSB							LSB
USER_INTERRUPT									
0x00	REVISION_ID[7:0]	Revision_id[7:0]							
0x01	Status0[7:0]	chn_con_sts	chn_wty_sts	chn_idl_sts	srt_xfer	lng_xfer	ThmStat[2:0]		
0x02	Status1[7:0]	JeitaIsReg	ChgRestaB	ChgThrmReg	CC1Tmo	ChgStat[3:0]			

ADDRESS	NAME	MSB							LSB
0x03	Status2[7:0]	PLCSumAct	PLCSumCurr[5:0]						–
0x04	Status3[7:0]	SysMinReg	ChgRev	ChgVoltMode	ChgVoltStp	ChgGMD	LDOGMD	PLCOk	SysRev
0x05	Status4[7:0]	plc_status[7:0]							
0x06	Status5[7:0]	itf_rdy_sts	BatUVLOB	dead_batt	plc_moi_det	botcode_ltc[3:0]			
0x07	Status6[7:0]	–	–	–	urt_swc_opn	chg_prq_inp	swc_off_mod[2:0]		
0x08	Int0[7:0]	PLCSumActInt	PLCSumCurrInt	ChgThrmRegInt	CC1TmoInt	ChgStatInt	SysMinRegInt	ChgRestaBInt	ThmStatInt
0x09	Int1[7:0]	JeitaIsRegInt	ChgRevInt	ChgVoltModeInt	ChgVoltStpInt	ChgGMDInt	LDOGMDInt	PLCokInt	SysRevInt
0x0A	Int2[7:0]	chn_con_Int	chn_wty_Int	chn_idl_Int	srt_xfer_Rise	srt_xfer_Fall	plc_new_dat	plc_cmd_dne	plc_cmd_err
0x0B	Int3[7:0]	lng_xfer_Int	BatUVLOBInt	moi_dne_int	plc_moi_detInt	moi_irq_det	res_det_abr	res_det_opn	res_det_gnd
0x0C	Int4[7:0]	urt_tmo_flt	urt_modfail	urt_moddone	urt_swc_opnInt	dead_found	–	swc_off_modIrq	chg_prq_inpIrq
0x0D	Int5[7:0]	itf_rdy_stsInt	–	–	–	–	wd__itr_clr	–	–
0x0E	IntMask0[7:0]	PLCSumActIntM	PLCSumCurrIntM	ChgThrmRegIntM	CC1TmoIntM	ChgStatIntM	SysMinRegIntM	ChgRestaBIntM	ThmStatIntM
0x0F	IntMask1[7:0]	JeitaIsRegIntM	ChgRevIntM	ChgVoltModeIntM	ChgVoltStpIntM	ChgGMDIntM	LDOGMDIntM	PLCokIntM	SysRevIntM
0x10	IntMask2[7:0]	chn_con_IntM	chn_wty_IntM	chn_idl_IntM	srt_xfer_RiseM	srt_xfer_FallM	plc_new_datM	plc_cmd_dneM	plc_cmd_errM
0x11	IntMask3[7:0]	lng_xfer_IntM	BatUVLOBIntM	moi_dne_intM	plc_moi_detIntM	moi_irq_detM	res_det_abrM	res_det_opnM	res_det_gndM
0x12	IntMask4[7:0]	urt_tmo_fltM	urt_modfailM	urt_moddoneM	urt_swc_opnIntM	dead_foundM	0	swc_off_modIrqM	chg_prq_inpIrqM
0x13	IntMask5[7:0]	itf_rdy_stsIntM	0	0	–	–	wd__itr_clrM	–	–
USER_BOT									

ADDRESS	NAME	MSB							LSB
0x1A	SYSTEM_REG0[7:0]	off_cmd_inp	soft_reset	hard_reset	sft_hrd_rst	seal_i2c_cmd	0	Stay_ON	enb_otp_ena
0x1B	BOT_CMD[7:0]	fg____reset	fg_ena_byp	fg_ena_val	–	–	–	–	jta_hrs_ena
0x1C	BOT_RDB[7:0]	reset_mode[2:0]			–	–	–	–	–
USER_UART									
0x20	UART_Ctr0[7:0]	–	–	–	–	–	urt_auto_en	rxs_tmo_tim[1:0]	
0x21	UART_Ctr1[7:0]	–	tmo_tmr_ena	i2c_urt_mod	i2c_urt_ena	i2c_urt_abr	i2c_urt_swc	i2c_tx__swc	i2c_rx__swc
USER_SYSTEM_CONFIG									
0x30	SYSTEM_CONFIG0[7:0]	chg_wkp_ena	low_pwr_ena	–	Ichg_x2	chg_res_ena	i2c_ldo_ena	SYSUVLOThSel[1:0]	
0x31	PLC_CONFIG0[7:0]	PLCSnkSel[1:0]		–	–	–	–	PLCThrSel[1:0]	
0x32	PLC_CONFIG1[7:0]	otp_sum_rev	frc_i2c_sum	PLCCurr[5:0]					
0x33	PLC_CONFIG2[7:0]	plc_dsc_otp	PLC_DROP[2:0]			PLC_HLD[1:0]		PLC_HREF[1:0]	
0x34	PLC_CONFIG3[7:0]	plc_monitor	plc_con_sts	plc_config[2:0]			DAT_MAX_RTY[2:0]		
0x35	PLC_CONFIG4[7:0]	plc_fsm_ena	RAM_is_full	fifo_master	fifo__slave	plc_is_full	png_timeout	plc_res_req	cont_stream
0x36	PLC_CONFIG5[7:0]	no_fifo_slave	no_seal_mde	no_uart_mde	no_idle_mde	–	–	–	swp_plc_ram
0x37	PLC_ARG[7:0]	plc_cmd_arg[7:0]							
0x38	PLC_CMD[7:0]	plc_run_trg	plc_command[6:0]						
0x39	PLC_RX[7:0]	–	plc_rx_bytes[6:0]						
0x3A	Master_feed_back0[7:0]	mst_SOC_val[7:0]							
0x3B	Master_feed_back1[7:0]	mst_FGready	–	–	–	–	–	–	–

ADDRESS	NAME	MSB							LSB
0x3C	WATCHDOG0[7:0]	–	–	–	–	wd_rst_type[1:0]		wd__eoc_sel[1:0]	
0x3D	SYS_MIN0[7:0]	PP_drp[2:0]			SysMinForce	SysMin[3:0]			
USER_CHARGER									
0x40	ILimCtrlChg[7:0]	–	–	–	–	ChgThrmLim[3:0]			
0x41	ChgCur0[7:0]	–	CC1IFChg[6:0]						
0x42	ChgCur1[7:0]	–	CC2IFChg[6:0]						
0x43	ChgCntl0[7:0]	ChgEn	ChgAutoStop	ChgAutoReSta	–	–	CC1RoomOnly	CC1TmoLimit	CC1Enable
0x44	ChgCntl1[7:0]	BatReChg[1:0]		BatReg[5:0]					
0x45	ChgCntl2[7:0]	–	VPChg[2:0]			IPChg[1:0]		IChgDone[1:0]	
0x46	ChgTmr[7:0]	MtChgTmr[1:0]		PChgTmr[1:0]		CC1FChgTmr[1:0]		ChgTmr[1:0]	
0x47	ChgCfg0[7:0]	–	ChgStepHys[2:0]			ChgStepRise[3:0]			
0x48	ThmCfg0[7:0]	ChgCoolCC1IFChg[2:0]			ChgCoolBatReg[1:0]		ChgCoolCC2IFChg[2:0]		
0x49	ThmCfg1[7:0]	ChgRoomCC1IFChg[2:0]			ChgRoomBatReg[1:0]		ChgRoomCC2IFChg[2:0]		
0x4A	ThmCfg2[7:0]	ChgWarmCC1IFChg[2:0]			ChgWarmBatReg[1:0]		ChgWarmCC2IFChg[2:0]		
0x4B	ThmCfg3[7:0]	–	–	ChgT1ThrDef[2:0]			ChgT1ThrCC1[2:0]		
0x4C	ThmCfg4[7:0]	–	–	ChgT2ThrDef[2:0]			ChgT2ThrCC1[2:0]		
0x4D	ThmCfg5[7:0]	–	–	ChgT3ThrDef[2:0]			ChgT3ThrCC1[2:0]		
0x4E	ThmCfg6[7:0]	–	–	ChgT4ThrDef[2:0]			ChgT4ThrCC1[2:0]		
0x4F	ThmCfg7[7:0]	jta_eoc_sel[1:0]		–	–	THMPUSel	ThmEn[2:0]		
0x50	ChgCtr1[7:0]	i2c_crf_ena	chg_cc_trk	ChgStsFCMrg	vlt_dne_ena	–	lng_xfer_opt	–	–
0x51	ChgCtr2[7:0]	BattUvloEna	BattPullDown	FrcPChg	–	–	–	vlt_ctr_plc[1:0]	
USER_GPIO									

ADDRESS	NAME	MSB							LSB
0x58	GPIO1[7:0]	–	–	–	GPIOCmpEna1	GPIOPLCCtr1	GPIOEnRes1	GPIOEnPup1	GPIODout_1
0x59	GPIO2[7:0]	–	–	–	GPIOCmpEna2	GPIOPLCCtr2	GPIOEnRes2	GPIOEnPup2	GPIODout_2
0x5A	GPIO3[7:0]	–	–	–	GPIOCmpEna3	GPIOPLCCtr3	GPIOEnRes3	GPIOEnPup3	GPIODout_3
0x5B	GPIO4[7:0]	–	–	–	GPIOCmpEna4	GPIOPLCCtr4	GPIOEnRes4	GPIOEnPup4	GPIODout_4
0x5C	GPIO_rdb1[7:0]	GPIODAInp_4	GPIODAInp_3	GPIODAInp_2	GPIODAInp_1	–	–	–	GPIOCmosEn
0x5D	GPIO_rdb2[7:0]	–	–	–	–	master_GPIO4	master_GPIO3	master_GPIO2	master_GPIO1
USER_DOP_PORT									
0x60	SOC_byte_1[7:0]	AVGVCELL_byte_1[7:0]							
0x61	SOC_byte_0[7:0]	AVGVCELL_byte_0[7:0]							
0x62	VCELL_byte_1[7:0]	VCELL_byte_1[7:0]							
0x63	VCELL_byte_0[7:0]	VCELL_byte_0[7:0]							
0x64	TTE_byte_1[7:0]	TTE_byte_1[7:0]							
0x65	TTE_byte_0[7:0]	TTE_byte_0[7:0]							
0x66	AVGVCELL_byte_1[7:0]	SOC_byte_1[7:0]							
0x67	AVGVCELL_byte_0[7:0]	SOC_byte_0[7:0]							
0x68	TTF_byte_1[7:0]	TTF_byte_1[7:0]							
0x69	TTF_byte_0[7:0]	TTF_byte_0[7:0]							
0x6A	READY_REG[7:0]	dop_rdy_sig	–	dop_i2c_ena	ttf_reg_rdy	soc_reg_rdy	tte_reg_rdy	vcell_reg_rdy	avgvcell_reg_rdy
USER_MOISTURE_DETECTION									

ADDRESS	NAME	MSB							LSB
0x70	ADC_CTRL1[7:0]	–	AdcGndTrh[3:0]				ResDetRty[2:0]		
0x71	ADC_CTRL2[7:0]	–	–	AdcRng[5:0]					
0x72	ADC_CTRL3[7:0]	–	–	–	–	–	AdcAvgNum[2:0]		
0x73	ADC_CTRL4[7:0]	–	–	AdcNoiseCtr[5:0]					
0x74	MOI_DET_REG1[7:0]	–	–	–	–	–	–	RaccDetMIp[1:0]	
0x75	MOI_DET_REG2[7:0]	RaccDetMThr[7:0]							
0x76	MOI_DET_REG3[7:0]	–	moi_det_aut	–	moi_man__pl	–	moi_man_rty	–	moi_aut_rty
0x77	IP RES_REG[7:0]	–	–	–	–	–	–	IP__RES_DET[1:0]	
0x78	ADC_VAL1[7:0]	ADCAvg[7:0]							
0x79	ADC_VAL2[7:0]	ADCMax[7:0]							
0x7A	ADC_VAL3[7:0]	ADCMin[7:0]							

Register Details

REVISION_ID (0x0)

BIT	7	6	5	4	3	2	1	0
Field	Revision_id[7:0]							
Reset	0x11							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
Revision_id	7:0	Information about the hardware revision.

Status0 (0x1)

BIT	7	6	5	4	3	2	1	0

Field	chn_con_sts	chn_wty_sts	chn_idl_sts	srt_xfer	lng_xfer	ThmStat[2:0]
Reset	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
chn_con_sts	7	PLC connection status.	0x0: Disconnected 0x1: Connected
chn_wty_sts	6	Waiting status to conclude connection with master.	0x0: Not in waiting state 0x1: In waiting state
chn_idl_sts	5	PLC idle status	0x0: Not in idle state 0x1: Idle state
srt_xfer	4	Short transfer. Set for PLC PING and all PLC command.	0x0: No short transfer 0x1: Short transfer ongoing
lng_xfer	3	Long transfer. Set for DOUT_REQ PLC command and bulk data transfer.	0x0: No long transfer 0x1: Long transfer ongoing
ThmStat	2:0	JEITA status from thermistor monitoring.	0x0: Cold zone ($V_{THM_COLD} < V_{THM} < V_{THM_DIS}$) 0x1: Cool zone($V_{THM_COOL} < V_{THM} < V_{THM_COLD}$) 0x2: Room zone ($V_{THM_WARM} < V_{THM} < V_{THM_COOL}$) 0x3: Warm zone ($V_{THM_HOT} < V_{THM} < V_{THM_WARM}$) 0x4: Hot zone ($V_{THM} < V_{THM_HOT}$) 0x5: No thermistor detected ($V_{THM} > V_{THM_DIS}$) 0x6: Thermistor monitoring disabled. ThmEn = 0x0. 0x7: Thermistor monitoring disabled. PLC voltage is not present. ThmEn is not 0x0.

Status1 (0x2)

BIT	7	6	5	4	3	2	1	0
Field	JeitaIsReg	ChgRestaB	ChgThrmReg	CC1Tmo	ChgStat[3:0]			
Reset	0x0	0x0	0x0	0x0	0x0			
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
JeitaIsReg	7	JEITA status of charge current/voltage.	0x0: Charge current/voltage is not reduced because of JEITA settings 0x1: Charge current/voltage is reduced because of JEITA settings
ChgRestaB	6	Charger restart status. Auto-cleared after charger restart complete. Valid only when charger is enabled ChgEn = 1.	0x0: No charger restart event 0x1: Charger restarts
ChgThrmReg	5	Charger thermal shutdown status. Valid only when PLC voltage is present and charger is enabled ChgEn = 1.	0x0: Charger operating normally or disabled. 0x1: Charger current being actively reduced due to die temperature approaching thermal shutdown limit.

BITFIELD	BITS	DESCRIPTION	DECODE
CC1Tmo	4	CC1 timeout status. CC1 timer is set by CC1FChgTmr.	0x0: CC1 timeout not expired 0x1: CC1 Timeout expired
ChgStat	3:0	Charger mode status.	0x0: Charger off 0x1: Charger IDLE mode 0x2: Pre-charge in progress 0x3: Fast-charge constant current mode 1 (CC1) in progress 0x4: Fast-charge constant current mode 2 (CC2) in progress 0x5: Fast-charge constant voltage mode (CV) in progress 0x6: Maintain charge in progress 0x7: Maintain charge done 0x8: Charger Fault - PChgTmr Expired 0x9: Charger Fault - ChgTmr Expired 0xE: CC Tracking in progress 0xF: Charging suspended due to violation of JEITA temperature limits Other: Reserved

Status2 (0x3)

BIT	7	6	5	4	3	2	1	0
Field	PLCSumAct	PLCSumCurr[5:0]						–
Reset	0x0	0x0						–
Access Type	Read Only	Read Only						–

BITFIELD	BITS	DESCRIPTION	DECODE
PLCSumAct	7	PLC current limit status.	0x0: PLC input current is less than PLCCurr 0x1: PLC input current is equal to PLCCurr
PLCSumCurr	6:1	Realtime PLC input current limit. PLC input current is sum current of charger and SYS LDO.	Decode chart same as PLCCurr.

Status3 (0x4)

BIT	7	6	5	4	3	2	1	0
Field	SysMinReg	ChgRev	ChgVoltMode	ChgVoltStp	ChgGMD	LDOGMD	PLCOk	SysRev
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
SysMinReg	7	SYS voltage reference.	0x0: V_{SYS} is regulated at BAT 0x1: V_{SYS} is regulated at SysMin

BITFIELD	BITS	DESCRIPTION	DECODE
ChgRev	6	Charger reverse protection status.	0x0: $V_{BAT} < V_{PLC}$ Charger is in reverse protection 0x1: $V_{PLC} > V_{BAT}$
ChgVoltMode	5	Charger battery voltage regulation status.	0x0: $V_{BAT} < V_{BAT_REG}$ 0x1: $V_{BAT} \geq V_{BAT_REG}$
ChgVoltStp	4	Charger step charge status. Valid only when charger is enabled ChgEn = 1.	0x0: $V_{BAT} < V_{BAT_STPCHG}$ 0x1: $V_{BAT} \geq V_{BAT_STPCHG}$
ChgGMD	3	Charger dropout status. Valid only when PLC voltage is present and charger is enabled ChgEn = 1.	0x0: Charger current is not reduced due to dropout condition $V_{PLC} - V_{CHG_OUT} > V_{PLC_DROP}$ 0x1: Charger current is actively reduced due to a dropout condition $V_{PLC} - V_{CHG_OUT} < V_{PLC_DROP}$
LDOGMD	2	SYS LDO dropout status. Valid only when PLC voltage is present and SYS LDO is active.	0x0: SYS LDO current is not reduced due to dropout condition $V_{PLC} - V_{SYS} > V_{PLC_DROP}$ 0x1: SYS LDO current is actively reduced due to a dropout condition $V_{PLC} - V_{SYS} < V_{PLC_DROP}$
PLCOk	1	PLC voltage status.	0: $V_{PLC} < V_{PLCDET}$: PLC input voltage not present 1: $V_{PLC} > V_{PLCDET}$
SysRev	0	SYS LDO reverse protection status.	0x0: $V_{PLC} < V_{SYS}$ SYS LDO is in reverse protection 0x1: $V_{PLC} > V_{SYS}$

Status4 (0x5)

BIT	7	6	5	4	3	2	1	0
Field	plc_status[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
plc_status	7:0	PLC communication status. Valid on plc_cmd_dne or plc_cmd_err interrupt.	0x00: NO_PLC_ERROR. No error. 0x10: NACK_TO__CMD. Master sends NACK to slave command request. 0x11: NACK_TO_DATA. Master sends NACK to slave data packet. Only valid for short data transfer. 0x12: NOPLC_ON_CMD. PLC voltage disappears during PING. 0x14: NACK_N_DOUTR. NACK limit to DOUT_REQ is hit. Only valid for bulk data transfer. NACK limit is set by plc_config. 0x15: ERR__N_DOUTR. NACK limit to data packet is hit. Only valid for bulk data transfer. NACK limit is set by DAT_MAX_RTY. 0x18: MST_TMO__ERR. Slave is waiting for a (N)ACK from master but there is no response until timeout. 0x19: PLC_BUSY_ERR. Timer expired and slave receives more than 128 bytes of data. 0x1B: BAD__CMD__TX, Write wrong command or command argument in PLC_CMD and PLC_ARG. 0x1C: BAD__CMD__RX, Expect (N)ACK from master but receive other packect. 0x1D: PLC_DATA_ERR, Received corrupted (N)ACK

BITFIELD	BITS	DESCRIPTION	DECODE
			packects from master. Other: Reserved

Status5 (0x6)

BIT	7	6	5	4	3	2	1	0
Field	itf_rdy_sts	BatUVLOB	dead_batt	plc_moi_det	botcode_ltc[3:0]			
Reset	0x1	0x0	0x0	0x0	0x0			
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
itf_rdy_sts	7	OTP Loading Complete.	0x0: OTP loading not completed 0x1: OTP loading completed
BatUVLOB	6	Battery voltage UVLO status. Valid only when PLC input voltage is present, PLCOk = 1, chn_con_sts = 1 and chn_wty_sts = 0.	0x0: $V_{BAT} < V_{BAT_UVLO}$ 0x1: $V_{BAT} > V_{BAT_UVLO}$
dead_batt	5	Dead battery found. Dead battery check is performed when device is waked up from SYSUVLO, SEAL and soft + hard reset by discharging BAT pin.	0x0: Active battery 0x1: Dead battery
plc_moi_det	4	PLC moisture detection status.	0x0: No moisture detected 0x1: Moisture detected
botcode_ltc	3:0	Specify what cause the device to restart	0x0: Nothing 0x1: OFF 0x2: SEAL 0x4: SYSUVLO 0x8: Thermal shutdown Others: NA

Status6 (0x7)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	urt_swc_opn	chg_prq_inp	swc_off_mod[2:0]		
Reset	–	–	–	0x0	0x0	0x0		
Access Type	–	–	–	Read Only	Read Only	Read Only		

BITFIELD	BITS	DESCRIPTION	DECODE
urt_swc_opn	4	UART switches are open due to UART timeout after 0.5s of UART line idle. Valid only when tmo_tmr_ena = 1.	0x0: No UART switch open event due to timeout 0x1: UART switch is open due to timeout.
chg_prq_inp	3	Pre-charge status. Valid only when ChgEn = 1.	0x0: $V_{BAT} < V_{BAT_PCHG}$ 0x1: $V_{BAT} \geq V_{BAT_PCHG}$
swc_off_mod	2:0	Indicator for device shutdown within 20ms.	0x0: Nothing 0x1: OFF (in 20ms) 0x2: SEAL (in 20ms) 0x3: SYSUVLO (in 20ms) 0x4: Others Others: NA

Int0 (0x8)

BIT	7	6	5	4	3	2	1	0
Field	PLCSumActInt	PLCSumCurrInt	ChgThrmRegInt	CC1TmoInt	ChgStatInt	SysMinRegInt	ChgRestaBInt	ThmStatInt
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
PLCSumActInt	7	PLC sum current limit interrupt. Asserted if a change occurs on PLCSumAct.	0x0: Status is not changed 0x1: Status is changed
PLCSumCurrInt	6	PLC sum current interrupt. Asserted if a change occurs on PLCSumCurr.	0x0: Status is not changed 0x1: Status is changed
ChgThrmRegInt	5	Charger thermal shutdown interrupt. Asserted if a change occurs on ChgThrmReg.	0x0: Status is not changed 0x1: Status is changed
CC1TmoInt	4	CC1 timeout interrupt. Asserted if a change occurs on CC1Tmo.	0x0: Status is not changed 0x1: Status is changed
ChgStatInt	3	Charger mode interrupt. Asserted if a change occurs on ChgStat.	0x0: Status is not changed 0x1: Status is changed
SysMinRegInt	2	SYS voltage reference interrupt. Asserted if a change occurs on SysMinReg.	0x0: Status is not changed 0x1: Status is changed
ChgRestaBInt	1	Charger restart interrupt. Asserted if a change occurs on ChgRestaB.	0x0: Status is not changed 0x1: Status is changed
ThmStatInt	0	JEITA thermal monitoring interrupt. Asserted if a change occurs on ThmStat.	0x0: Status is not changed 0x1: Status is changed

Int1 (0x9)

BIT	7	6	5	4	3	2	1	0
Field	JeitaIsRegInt	ChgRevInt	ChgVoltModeInt	ChgVoltStpInt	ChgGMDInt	LDOGMDInt	PLCokInt	SysRevInt
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
JeitaIsRegInt	7	JEITA charger current/voltage interrupt. Asserted if a change occurs on JeitaIsReg.	0x0: Status is not changed 0x1: Status is changed
ChgRevInt	6	Charger reverse protection interrupt. Asserted if a change occurs on ChgRev.	0x0: Status is not changed 0x1: Status is changed
ChgVoltModeInt	5	Charger battery voltage regulation interrupt. Asserted if a change occurs on ChgVoltMode.	0x0: Status is not changed 0x1: Status is changed
ChgVoltStpInt	4	Charger step charge interrupt. Asserted if a change occurs on ChgVoltstp.	0x0: Status is not changed 0x1: Status is changed
ChgGMDInt	3	Charger dropout interrupt. Asserted if a change occurs on ChgGMD.	0: Charger current is not actively being reduced to regulate V_{CHGOUT} 1: Charger current actively being reduced to regulate V_{CHGOUT}
LDOGMDInt	2	SYS LDO dropout interrupt. Asserted if a change occurs on LDOGMD.	0x0: Status is not changed 0x1: Status is changed
PLCokInt	1	PLC voltage interrupt. Asserted if a change occurs on PLCOk.	0x0: Status is not changed 0x1: Status is changed
SysRevInt	0	SYS LDO reverse protection interrupt. Asserted if a change occurs on SysRev.	0x0: Status is not changed 0x1: Status is changed

Int2 (0xA)

BIT	7	6	5	4	3	2	1	0
Field	chn_con_Int	chn_wty_Int	chn_idl_Int	srt_xfer_Rise	srt_xfer_Fall	plc_new_dat	plc_cmd_dne	plc_cmd_err
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
chn_con_Int	7	PLC connection interrupt. Asserted if a change occurs on chn_con_sts.	0x0: Status is not changed 0x1: Status is changed

BITFIELD	BITS	DESCRIPTION	DECODE
chn_wty_Int	6	PLC waiting interrupt. Asserted if a change occurs on chn_wty_sts .	0x0: Status is not changed 0x1: Status is changed
chn_idl_Int	5	PLC idle interrupt. Asserted if a change occurs on chn_idl_sts.	0x0: Status is not changed 0x1: Status is changed
srt_xfer_Rise	4	Short transfer rising interrupt. Asserted if srt_xfer changes from 0 to 1.	0x0: Status does not change from 0 to 1 0x1: Status changes from 0 to 1
srt_xfer_Fall	3	Short transfer rising interrupt. Asserted if srt_xfer changes from 1 to 0.	0x0: Status does not change from 1 to 0 0x1: Status changes from 1 to 0
plc_new_dat	2	PLC new data interrupt.	0x0: No new data available 0x1: New data available in RAM
plc_cmd_dne	1	PLC command done interrupt.	0x0: PLC command not completed 0x1: PLC command done
plc_cmd_err	0	PLC command error interrupt.	0x0: PLC command no error 0x1: PLC command error occured

Int3 (0xB)

BIT	7	6	5	4	3	2	1	0
Field	lng_xfer_Int	BatUVLOBInt	moi_dne_int	plc_moi_detInt	moi_irq_det	res_det_abr	res_det_opn	res_det_gnd
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
lng_xfer_Int	7	Long transfer interrupt. Asserted if a change occurs on lng_xfer.	0x0: Status is not changed 0x1: Status is changed
BatUVLOBInt	6	Battery voltage UVLO interrupt. Asserted if a change occurs on BatUVLOB.	0x0: Status is not changed 0x1: Status is changed
moi_dne_int	5	Moisture detection done interrupt. It occurs when a moisture measure is completed.	0x0: Moisture measurement is not completed 0x1: Moisture measurement is completed
plc_moi_detInt	4	Moisture detection interrupt for PLC. It occurs when a moisture is detected on PLC. Asserted if a change occurs on plc_moi_det.	0x0: Status is not changed 0x1: Status is changed
moi_irq_det	3	Moisture detection measurement valid result interrupt.	0x0: Moisture detection valid value not detected 0x1: Moisture detection valid value detected
res_det_abr	2	Abort resistive measurement result interrupt.	0x0: Abort resistive value not detected 0x1: Abort resistive value detected
res_det_opn	1	Open resistive measurement result interrupt.	0x0: Open resistive value not detected 0x1: Open resistive value detected
res_det_gnd	0	Ground resistive measurement result interrupt.	0x0: Ground resistive value not detected 0x1: Ground resistive value detected

Int4 (0xC)

BIT	7	6	5	4	3	2	1	0
Field	urt_tmo_flt	urt_modfail	urt_moddone	urt_swc_opnInt	dead_found	–	swc_off_modIrq	chg_prq_inpIrq
Reset	0x0	0x0	0x0	0x0	0x0	–	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
urt_tmo_flt	7	UART timeout interrupt.	0x0: UART mode timeout not expired 0x1: UART mode timeout expired
urt_modfail	6	UART mode fail interrupt.	0x0: UART mode not failed 0x1: UART mode failed
urt_moddone	5	UART mode done interrupt. Asserted when device enters/exits UART mode.	0x0: No UART mode done event 0x1: UART mode done
urt_swc_opnInt	4	UART switch open due to timeout interrupt. Asserted if a change occurs on urt_swc_opn.	0x0: Status is not changed 0x1: Status is changed
dead_found	3	PLC detection found master in dead battery condition.	0x0: No dead master 0x1: Dead master found
swc_off_modIrq	1	Asserted if a change occurs on swc_off_mod.	0x0: Status is not changed 0x1: Status is changed
chg_prq_inpIrq	0	Asserted if a change occurs on chg_prq_inp.	0x0: Status is not changed 0x1: Status is changed

Int5 (0xD)

BIT	7	6	5	4	3	2	1	0
Field	itf_rdy_stsInt	–	–	–	–	wd__itr_clr	–	–
Reset	0x1	–	–	–	–	0x0	–	–
Access Type	Write, Read	–	–	–	–	Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
itf_rdy_stsInt	7	OTP loading complete. Device is ready to communicate via I2C after this bit is asserted. Asserted if a change occurs on itf_rdy_sts.	0x0: Status is not changed 0x1: Status is changed
wd__itr_clr	2	Read this bit with in watchdog time limit to prevent device reset. This bit may reset itself if watchdog type choose to reset the device.	0x0: Bit read. Device will not reset 0x1: Bit not read since last timeout

IntMask0 (0xE)

BIT	7	6	5	4	3	2	1	0
Field	PLCSumActIntM	PLCSumCurrIntM	ChgThrmRegIntM	CC1TmoIntM	ChgStatIntM	SysMinRegIntM	ChgRestaBIntM	ThmStatIntM
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
PLCSumActIntM	7	PLCSumActInt interrupt mask.	0x0: Masked 0x1: Unmasked
PLCSumCurrIntM	6	PLCSumCurrInt interrupt mask.	0x0: Masked 0x1: Unmasked
ChgThrmRegIntM	5	ChgThrmRegIntM interrupt mask.	0x0: Masked 0x1: Unmasked
CC1TmoIntM	4	CC1TmoInt interrupt mask.	0x0: Masked 0x1: Unmasked
ChgStatIntM	3	ChgStatInt interrupt mask.	0x0: Masked 0x1: Unmasked
SysMinRegIntM	2	SysMinRegInt interrupt mask.	0x0: Masked 0x1: Unmasked
ChgRestaBIntM	1	ChgRestaBInt interrupt mask.	0x0: Masked 0x1: Unmasked
ThmStatIntM	0	ThmStatInt interrupt mask.	0x0: Masked 0x1: Unmasked

IntMask1 (0xF)

BIT	7	6	5	4	3	2	1	0
Field	JeitaIsRegIntM	ChgRevIntM	ChgVoltModeIntM	ChgVoltStpIntM	ChgGMDIntM	LDOGMDIntM	PLCokIntM	SysRevIntM
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
JeitaIsRegIntM	7	JeitaIsRegInt interrupt mask.	0x0: Masked 0x1: Unmasked
ChgRevIntM	6	ChgRevInt interrupt mask.	0x0: Masked 0x1: Unmasked
ChgVoltModeIntM	5	ChgVoltModeInt interrupt mask.	0x0: Masked 0x1: Unmasked
ChgVoltStpIntM	4	ChgVoltStpInt interrupt mask.	0x0: Masked 0x1: Unmasked
ChgGMDIntM	3	ChgGMDInt interrupt mask.	0x0: Masked 0x1: Unmasked

BITFIELD	BITS	DESCRIPTION	DECODE
LDOGMDIntM	2	LDOGMDInt interrupt mask.	0x0: Masked 0x1: Unmasked
PLCokIntM	1	PLCokInt interrupt mask.	0x0: Masked 0x1: Unmasked
SysRevIntM	0	SysRevInt interrupt mask.	0x0: Masked 0x1: Unmasked

IntMask2 (0x10)

BIT	7	6	5	4	3	2	1	0
Field	chn_con_IntM	chn_wty_IntM	chn_idl_IntM	srt_xfer_RiseM	srt_xfer_FallM	plc_new_datM	plc_cmd_dneM	plc_cmd_errM
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
chn_con_IntM	7	chn_con_Int interrupt mask.	0x0: Masked 0x1: Unmasked
chn_wty_IntM	6	chn_wty_Int interrupt mask.	0x0: Masked 0x1: Unmasked
chn_idl_IntM	5	chn_idl_Int interrupt mask.	0x0: Masked 0x1: Unmasked
srt_xfer_RiseM	4	srt_xfer_Int interrupt mask.	0x0: Masked 0x1: Unmasked
srt_xfer_FallM	3	srt_xfer_Int interrupt mask.	0x0: Masked 0x1: Unmasked
plc_new_datM	2	plc_new_dat interrupt mask.	0x0: Masked 0x1: Unmasked
plc_cmd_dneM	1	plc_cmd_dne interrupt mask.	0x0: Masked 0x1: Unmasked
plc_cmd_errM	0	plc_cmd_err interrupt mask.	0x0: Masked 0x1: Unmasked

IntMask3 (0x11)

BIT	7	6	5	4	3	2	1	0
Field	lng_xfer_IntM	BatUVLOBIntM	moi_dne_intM	plc_moi_detIntM	moi_irq_detM	res_det_abrM	res_det_opnM	res_det_gndM
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
lng_xfer_IntM	7	lng_xfer_Int interrupt mask.	0x0: Masked 0x1: Unmasked
BatUVLOBIntM	6	BatUVLOBInt interrupt mask.	0x0: Masked 0x1: Unmasked
moi_dne_intM	5	moi_dne_int interrupt mask.	0x0: Masked 0x1: Unmasked
plc_moi_detIntM	4	plc_moi_detInt interrupt mask.	0x0: Masked 0x1: Unmasked
moi_irq_detM	3	moi_irq_det interrupt mask.	0x0: Masked 0x1: Unmasked
res_det_abrM	2	res_det_abr interrupt mask.	0x0: Masked 0x1: Unmasked
res_det_opnM	1	res_det_opn interrupt mask.	0x0: Masked 0x1: Unmasked
res_det_gndM	0	res_det_gnd interrupt mask.	0x0: Masked 0x1: Unmasked

IntMask4 (0x12)

BIT	7	6	5	4	3	2	1	0
Field	urt_tmo_fltM	urt_modfailM	urt_moddoneM	urt_swc_opnIntM	dead_foundM	0	swc_off_modIrqM	chg_prq_inpIrqM
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
urt_tmo_fltM	7	urt_tmo_flt interrupt mask.	0x0: Masked 0x1: Unmasked
urt_modfailM	6	urt_modfail interrupt mask.	0x0: Masked 0x1: Unmasked
urt_moddoneM	5	urt_moddone interrupt mask.	0x0: Masked 0x1: Unmasked
urt_swc_opnIntM	4	urt_swc_opnInt interrupt mask.	0x0: Masked 0x1: Unmasked
dead_foundM	3	dead_found interrupt mask.	0x0: Masked 0x1: Unmasked
0	2	Reserved.	Keep 0. Do not change.
swc_off_modIrqM	1	swc_off_modIrq interrupt mask.	0x0: Masked 0x1: Unmasked
chg_prq_inpIrqM	0	chg_prq_inpIrq interrupt mask.	0x0: Masked 0x1: Unmasked

IntMask5 (0x13)

BIT	7	6	5	4	3	2	1	0

Field	itf_rdy_stsIntM	0	0	–	–	wd__itr_clrM	–	–
Reset	0x1	0b0	0b0	–	–	0x0	–	–
Access Type	Write, Read	Write, Read	Write, Read	–	–	Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
itf_rdy_stsIntM	7	itf_rdy_stsInt interrupt mask.	0x0: Masked 0x1: Unmasked
0	6	Reserved	Keep 0. Do not change.
0	5	Reserved	Keep 0. Do not change.
wd__itr_clrM	2	wd__itr_clr interrupt mask.	0x0: Masked 0x1: Unmasked

SYSTEM_REG0 (0x1A)

BIT	7	6	5	4	3	2	1	0
Field	off_cmd_inp	soft_reset	hard_reset	sft_hrd_rst	seal_i2c_cmd	0	Stay_ON	enb_otp_ena
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x1	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
off_cmd_inp	7	OFF mode request.	0x0: No request 0x1: Request to enter OFF mode
soft_reset	6	soft reset request.	0x0: No request 0x1: Request soft reset
hard_reset	5	Hard reset request. Autoclear after hard reset.	0x0: No request 0x1: Request hard reset
sft_hrd_rst	4	Soft and hard reset request.	0x0: No request 0x1: Request soft and hard reset
seal_i2c_cmd	3	SEAL request.	0x0: No request 0x1: Request to enter SEAL mode
0	2	Reserved.	Keep 0. Do not change.
Stay_ON	1	Device stays on after turn on.	0x0: 500ms shutdown timer enabled 0x1: Device remains ON
enb_otp_ena	0	EN pin functionality.	0x0: EN pin does not control OFF mode 0x1: EN pin controls OFF mode

BOT_CMD (0x1B)

BIT	7	6	5	4	3	2	1	0
Field	fg____reset	fg_ena_byp	fg_ena_val	–	–	–	–	jta_hrs_ena

Reset	0x0	0x0	0x0	–	–	–	–	0x0
Access Type	Write, Read	Write, Read	Write, Read	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
fg____reset	7	Fuel Gauge reset. Autoclear when done.	0x0: No request 0x1: Request fuel gauge reset
fg_ena_byp	6	Fuel gauge manual enable functionality.	0x0: Fuel gauge manual enable feature disabled 0x1: Fuel gauge manual enable feature enabled
fg_ena_val	5	Fuel gauge manual enable. Valid if fg_ena_byp = 1.	0x0: Fuel gauge off 0x1: Fuel gauge on
jta_hrs_ena	0	Enable JEITA hard reset when there is no PLC present. Valid only when ThmEn > 0x3.	0x0: Disable 0x1: Enable

BOT_RDB (0x1C)

BIT	7	6	5	4	3	2	1	0
Field	reset_mode[2:0]			–	–	–	–	–
Reset	0x0			–	–	–	–	–
Access Type	Read Only			–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
reset_mode	7:5	Last reset conducted by the device since the device is on.	0x0: No reset 0x1: Soft reset 0x2: Hard reset 0x3: Hard and soft reset 0x4: UBOOT Reset Others: NA

UART_Ctr0 (0x20)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	urt_auto_en	rxs_tmo_tim[1:0]	
Reset	–	–	–	–	–	0x0	0x0	
Access Type	–	–	–	–	–	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
urt_auto_en	2	UART automtatic switch enable.	0x0: Disable 0x1: Enable

BITFIELD	BITS	DESCRIPTION	DECODE
rxs_tmo_tim	1:0	UART automatic switch timeout from RX to TX. Valid only when urt_auto_en = 1.	0x0: 8µs 0x1: 32µs 0x2: 64µs 0x3: 128µs

UART_Ctr1 (0x21)

BIT	7	6	5	4	3	2	1	0
Field	–	tmo_tmr_ena	i2c_urt_mod	i2c_urt_ena	i2c_urt_abr	i2c_urt_swc	i2c_tx__swc	i2c_rx__swc
Reset	–	0b1	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
tmo_tmr_ena	6	UART timeout.	0x0: Disable 0x1: Enable
i2c_urt_mod	5	UART enter/exit through PLC or I2C control.	0x0: UART enter and exit controlled by PLC 0x1: UART enter and exit controlled by I2C
i2c_urt_ena	4	Enter UART mode (I2C).	0x0: Not enter UART mode 0x1: Enter UART mode
i2c_urt_abr	3	Abort UART mode (I2C).	0x0: Not abort 0x1: Abort
i2c_urt_swc	2	UART switch PLC or I2C control.	0x0: PLC control 0x1: I2C control
i2c_tx__swc	1	TX switch I2C enable.	0x0: Open 0x1: Closed
i2c_rx__swc	0	RX switch I2C enable.	0x0: Open 0x1: Closed

SYSTEM_CONFIG0 (0x30)

BIT	7	6	5	4	3	2	1	0
Field	chg_wkp_ena	low_pwr_ena	–	Ichg_x2	chg_res_ena	i2c_ldo_ena	SYSUVLOThSel[1:0]	
Reset	0x1	0x1	–	0x0	0x0	0x1	0x0	
Access Type	Write, Read	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
chg_wkp_ena	7	Charger wakeup control when V_{BAT} is less than recharge voltage threshold.	0x0: VBAT greater than recharge voltage threshold doesn't wake up the PLC FSM 0x1: VBAT less than re-charge voltage threshold wakes up the PLC FSM
low_pwr_ena	6	Low power mode enable.	0x0: Disable 0x1: Enable

BITFIELD	BITS	DESCRIPTION	DECODE
Ichg_x2	4	PLC, charger and SYS LDO current limit control.	0x0: PLCCurr default setting. PLC can sink up to 200mA (typ). SYS LDO can sink up to 200mA (typ), Charge current register default setting. Charger can sink up to 200mA (typ). 0x1: PLCCurr register setting doubled. PLC can sink up to 400mA (typ). SYS LDO can sink up to 200mA (typ), Charge current register setting doubled. can sink up to 400mA (typ).
chg_res_ena	3	Enable Initialization reset for charger section of the register map: ILimCtrChg, ChgCur0/1, ChgCntl0/1/2, ChgTmr, ChgCfg0, ThmCfg0/1/2/3/4/5/6/7, ChgCtr1/2.	0x0: No Initialization reset for the charger section of the register map 0x1: Initialization reset for the charger section of the register map. Initialization occurs when charger FSM starts.
i2c_ldo_ena	2	SYS LDO enable control.	0x0: SYS LDO Disabled 0x1: SYS LDO Enabled
SYSUVLOThSel	1:0	SYSUVLO falling voltage threshold.	0x0: 2.7V 0x1: 2.9V 0x2: 3.0V 0x3: 3.2V

PLC_CONFIG0 (0x31)

BIT	7	6	5	4	3	2	1	0
Field	PLCSnkSel[1:0]		–	–	–	–	PLCThrSel[1:0]	
Reset	0x1		–	–	–	–	0x1	
Access Type	Write, Read		–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
PLCSnkSel	7:6	PLC trasmission sink current.	0x0: 50.3 mA 0x1: 70.4 mA 0x2: 90.4 mA 0x3: 110.5 mA
PLCThrSel	1:0	PLC pulse voltage threshold.	0x0: 75 mV 0x1: 90 mV 0x2: 105 mV 0x3: 120 mV

PLC_CONFIG1 (0x32)

BIT	7	6	5	4	3	2	1	0
Field	otp_sum_rev	frc_i2c_sum	PLCCurr[5:0]					
Reset	0x1	0x0	0x3F					
Access Type	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
otp_sum_rev	7	Minimize the PLC Current in case $V_{PLC} < V_{SYS}$ or $V_{PLC} < V_{BAT}$. Valid only if frc_i2c_sum=0.	0x0: PLC Current does not set to minimum value on $V_{PLC} < V_{SYS}$ or $V_{PLC} < V_{BAT}$ 0x1: PLC Current set to its minimum value on $V_{PLC} < V_{SYS}$ or $V_{PLC} < V_{BAT}$
frc_i2c_sum	6	Force PLC current limit to PLCCurr.	0x0: PLC current limit internally controlled. PLC current limit can be lower than PLCCurr depending on charger operating condition. 0x1: PLC Current limit directly controlled by PLCCurr.
PLCCurr	5:0	PLC input current limit. Sum of SYS LDO and charge current.	LSB is 3.125mA. The full scale is 200mA.

PLC_CONFIG2 (0x33)

BIT	7	6	5	4	3	2	1	0
Field	plc_dsc_otp	PLC_DROP[2:0]			PLC_HLD[1:0]		PLC_HREF[1:0]	
Reset	0b1	0x2			0b1		0x1	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
plc_dsc_otp	7	PLC discharge enable control under SYSUVLO.	0x0: No discharge 0x1: Discharge
PLC_DROP	6:4	Charger dropout (V_{PLC} - V_{CHG_OUT}) and SYS LDO (V_{PLC}-V_{SYS}) dropout threshold.	0x0: 50mV 0x1: 75mV 0x2: 100mV 0x3: 125mV 0x4: 150mV 0x5: 175mV 0x6: 200mV 0x7: 225mV
PLC_HLD	3:2	V_{BAT} + V_{PLC_HREF} - V_{PLC_HLD} defines lower limit of the PLC voltage.	0x0: 50 mV 0x1: 62.5 mV 0x2: 75 mV 0x3: 87.5 mV
PLC_HREF	1:0	V_{BAT} + V_{PLC_HREF} defines upper limit of PLC voltage.	0x0: 112.5 mV 0x1: 125 mV 0x2: 137.5 mV 0x3: 150 mV

PLC_CONFIG3 (0x34)

BIT	7	6	5	4	3	2	1	0
Field	plc_monitor	plc_con_sts	plc_config[2:0]			DAT_MAX_RTY[2:0]		
Reset	0x0	0x0	0x7			0x7		
Access Type	Write, Read	Write, Read	Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
plc_monitor	7	Slave monitors PLC line for PLC communication as soon as PLC supply is present if master detection FSM is disabled.	0x0: Slave monitors PLC line 0x1: Slave does not monitor PLC line
plc_con_sts	6	Toggle to choose slave connection state indicator.	0x0: Enter connect state after first PING 0x1: Enter connect state when PLC is present
plc_config	5:3	Bulk transfer auto-retry of DOUT_REQ. Maximun NACK to DOUT_REQ from master before slave detect an error in DATA transfers. Only works in bulk data transfer mode.	0x0: 1 0x1: 2 0x2: 4 0x3: 8 0x4: 16 0x5: 32 0x6: 64 0x7: 128
DAT_MAX_RTY	2:0	Auto-retry numbers of data packet. Maximun NACK to data packet from master before error flag is asserted in data transfers. Valid for bulk data transfer only.	0x0: 1 0x1: 2 0x2: 3 0x3: 4 0x4: 5 0x5: 6 0x6: 7 0x7: 8

PLC_CONFIG4 (0x35)

BIT	7	6	5	4	3	2	1	0
Field	plc_fsm_ena	RAM_is_full	fifo_master	fifo__slave	plc_is_full	png_timeout	plc_res_req	cont_stream
Reset	0b1	0b0	0b0	0x0	0x0	0x0	0b0	0b0
Access Type	Write, Read	Write, Read	Read Only	Read Only	Read Only	Read Only	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
plc_fsm_ena	7	PLC FSM enable control.	0x0: PLC FSM disabled 0x1: PLC FSM enabled
RAM_is_full	6	Valid for both bulk data transfer and mailbox data transfer. When data is received, this bit is set togheter with plc_new_dat and plc_rx_bytes. RAM_is_full remains at 1 until write 1 from I^2C to clear. Make sure to clear RAM_is_full after PLC data is read through I^2C. Writing RAM_is_full to one will signal to the device that RAM is ready to receive new data packet. If the device receives new DOUT_REQ but RAM_is_full remains to 1, the device will NACK to DOUT_REQ.	0x0: No new data received on PLC line 0x1: New data received via PLC line, Ready to be read. Write to 1 to clear.
fifo_master	5	FIFO master.	0x0: Not in FIFO master mode 0x1: FIFO master mode
fifo__slave	4	FIFO slave.	0x0: Not in FIFO slave mode 0x1: FIFO slave mode

BITFIELD	BITS	DESCRIPTION	DECODE
plc_is_full	3	Valid only for bulk data transfer. It indicates the RAM buffer is full. Data received via PLC is not read yet. Device will NACK to next PLC DOUT_REQ.	0x0: At least one RAM is free 0x1: Both RAMs are full
png_timeout	2	Indicator to show last PING packet from master is 268.5ms ago. This is just a flag to monitor the condition. Device does not take any action after timer is expired.	0x0: Last PING packect was received less than 268.5ms ago (typ) 0x1: Last PING packect was received more than 268.5ms ago (typ)
plc_res_req	1	PLC IDLE resume request. Autocleared when done.	0x0: No request 0x1: Request to resume from PLC IDLE
cont_stream	0	Valid only for bulk data transfer. If device is sending data in bulk transfer mode, when this bit is set to 1, only first packet transfer must be triggered with plc_run_trg. Other packets will be sent automatically after plc_cmd_dne interrupt. New data packet needs to filled in to RAM via I^2C before plc_cmd_dne of previous DOUT_REQ command.	0x0: No continuous stream 0x1: Continuos stream

PLC_CONFIG5 (0x36)

BIT	7	6	5	4	3	2	1	0
Field	no_fifo_slave	no_seal_mde	no_uart_mde	no_idle_mde	–	–	–	swp_plc_ram
Reset	0x0	0x0	0x1	0x0	–	–	–	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
no_fifo_slave	7	Nack to FIFO SYST_REQ PLC command.	0x0: Disable. Send ACK to FIFO SYST_REQ 0x1: Enable. Send NACK to FIFO SYST_REQ
no_seal_mde	6	Nack to SEAL SYST_REQ PLC command.	0x0: Disable. Send ACK to SEAL SYST_REQ PLC command 0x1: Enable. Send NACK to SEAL SYST_REQ PLC command
no_uart_mde	5	Nack to UART_REQ PLC command.	0x0: Disable. Send ACK to UART_REQ 0x1: Enable. Send NACK to UART_REQ
no_idle_mde	4	NACK to IDLE SYST_REQ PLC command.	0x0: Disable. Send ACK to IDLE_REQ 0x1: Enable. Send NACK to IDLE_REQ
swp_plc_ram	0	Swap PLC RAM control. Set this bit to 1 to read back data filled to RAM from master SoC in mailbox data transfer. Make sure to keep this bit to 0 when triggering data transfer.	0x0: Automatic control 0x1: RAM readback on I2C

PLC_ARG (0x37)

BIT	7	6	5	4	3	2	1	0
Field	plc_cmd_arg[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
plc_cmd_arg	7:0	PLC command argument.	**SET_GPIO:** {GPIOEnRes4, GPIOEnRes3, GPIOEnRes2, GPIOEnRes1, GPIODout_4, GPIODout_3, GPIODout_2, GPIODout_1} **DOUT_REQ:** Number of bytes = plc_cmd_arg1 + 1 **UART_REQ:** 0x0: Manual configuration of UART direction via I2C command (All switches are OFF) 0x1: Master PLC1 master receiving, slave transimitting (RX switches are ON) 0x2: Master PLC1 master transmitting, slave receiving (TX switches are ON) 0x3: Master PLC1 local loop back (TX and RX switches are ON) 0x4: Master PLC2 master receiving, slave transimitting (RX switches are ON) 0x8: Master PLC2 master transmitting, slave receiving (TX switches are ON) 0xC: Master PLC2 local loop back (TX and RX switches are ON) **SYST_REQ:** 0x1: Soft reset 0x3: Fuel gauge reset 0x4: FIFO request 0x5: Free request 0x6: PLC IDLE mode request

PLC_CMD (0x38)

BIT	7	6	5	4	3	2	1	0
Field	plc_run_trg	plc_command[6:0]						
Reset	0b0	0x0						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
plc_run_trg	7	PLC command trigger. Write 1 to trigger a PLC command. Autocleared when command is sent out through PLC line during PING.	0x0: No command in progress 0x1: Command running
plc_command	6:0	Command to send on PLC interface:	0x00: SYST_REQ 0x03: SET_GPIO 0x05: DOUT_REQ 0x06: UART_REQ

PLC_RX (0x39)

BIT	7	6	5	4	3	2	1	0
Field	–	plc_rx_bytes[6:0]						
Reset	–	0x0						
Access Type	–	Read Only						

BITFIELD	BITS	DESCRIPTION	DECODE
plc_rx_bytes	6:0	Number of bytes received on PLC line during last DOUT_REQ command. This register is set together with plc_new_dat interrupt and RAM_is_full flag.	Number of bytes = plc_rx_bytes + 1.

Master_feed_back0 (0x3A)

BIT	7	6	5	4	3	2	1	0
Field	mst_SOC_val[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
mst_SOC_val	7:0	Master SOC byte1 from master fuel gauge. Valid if mst_FGready = 1.	LSB is 1% of full charge. The full scale is 256%.

Master_feed_back1 (0x3B)

BIT	7	6	5	4	3	2	1	0
Field	mst_FGready	–	–	–	–	–	–	–

Reset	0x0	–	–	–	–	–	–	–
Access Type	Read Only	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
mst_FGready	7	Master SOC is reliable.	0x0: Not reliable 0x1: Reliable

WATCHDOG0 (0x3C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	wd_rst_type[1:0]		wd__eoc_sel[1:0]	
Reset	–	–	–	–	0x0		0x0	
Access Type	–	–	–	–	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
wd_rst_type	3:2	Watchdog reset type	0x0: Watchdog is OFF 0x1: Hard reset 0x2: Soft reset 0x3: Hard + soft reset
wd__eoc_sel	1:0	Watchdog timer. Device skips the the first watchdog timeout reset after UART exit, soft reset, hard reset, soft + hard reset and JEITA reset.	0x0: 4s 0x1: 8s 0x2: 16s 0x3: 32s

SYS_MIN0 (0x3D)

BIT	7	6	5	4	3	2	1	0
Field	PP_drp[2:0]			SysMinForce	SysMin[3:0]			
Reset	0x2			0x0	0x0			
Access Type	Write, Read			Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
PP_drp	7:5	CHG_OUT-SYS drop. Valid when PLC is present and power path FET is active.	0x0: 25mV 0x1: 37.5mV 0x2: 50mV 0x3: 62.5mV 0x4: 75mV 0x5: 87.5mV 0x6: 100mV 0x7: 112.5mV
SysMinForce	4	Control bit to force V_{SYS} reference to SysMin.	0x0: V_{SYS} regulated to V_{BAT} 0x1: V_{SYS} regulated to SysMin

BITFIELD	BITS	DESCRIPTION	DECODE
SysMin	3:0	Minimum SYS regulating voltage.	0x0: 3.0V 0x1: 3.1V 0x2: 3.2V 0x3: 3.3V 0x4: 3.4V 0x5: 3.5V 0x6: 3.6V 0x7: 3.7V 0x8: 3.8V 0x9: 3.9V 0xA: 4.0V 0xB: 4.1V 0xC: 4.2V 0xD: 4.3V 0xE: 4.4V 0xF: 4.5V

ILimCtrlChg (0x40)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	ChgThrmLim[3:0]			
Reset	–	–	–	–	0xF			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
ChgThrmLim	3:0	Thermal shutdown threshold.	0x0: 40°C 0x1: 45°C 0x2: 50°C 0x3: 55°C 0x4: 60°C 0x5: 65°C 0x6: 70°C 0x7: 75°C 0x8: 80°C 0x9: 85°C 0xA: 90°C 0xB: 95°C 0xC: 100°C 0xD: 105°C 0xE: 110°C 0xF: 115°C

ChgCur0 (0x41)

BIT	7	6	5	4	3	2	1	0

Field	–	CC1IFChg[6:0]
Reset	–	0x43
Access Type	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CC1IFChg	6:0	Fast charge constant current zone 1 charge current.	0x0 to 0x3C: 5mA to 65mA. LSB 1mA. 0x3D to 0x4F: 70mA to 160mA. LSB 5mA. 0x50 to 0x53: 170mA to 200mA. LSB 10mA. 0x54 to 0xFF: 200mA.

ChgCur1 (0x42)

BIT	7	6	5	4	3	2	1	0
Field	–	CC2IFChg[6:0]						
Reset	–	0x2D						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
CC2IFChg	6:0	Fast charge constant current zone 2 charge current.	0x0 to 0x3C: 5mA to 65mA. LSB 1mA. 0x3D to 0x4F: 70mA to 160mA. LSB 5mA. 0x50 to 0x53: 170mA to 200mA. LSB 10mA. 0x54 to 0xFF: 200mA.

ChgCntl0 (0x43)

BIT	7	6	5	4	3	2	1	0
Field	ChgEn	ChgAutoStop	ChgAutoReSta	–	–	CC1RoomOnly	CC1TmoLimit	CC1Enable
Reset	0x0	0x1	0x1	–	–	0x0	0x0	0x1
Access Type	Write, Read	Write, Read	Write, Read	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ChgEn	7	Charger enable control.	0x0: Disable 0x1: Enable

BITFIELD	BITS	DESCRIPTION	DECODE
ChgAutoStop	6	Charger auto-stop control. This bit controls if charger is allowed to transit from maintain charge state to maintain charge done state.	0x0: Auto-stop disabled 0x1: Auto-stop enabled
ChgAutoReSta	5	Charger auto-restart control.	0x0: Charger remains in maintain-charge done even when V_{BAT} is less than recharge threshold. 0x1: Charger automatically restarts when V_{BAT} drops below recharge threshold.
CC1RoomOnly	2	Run charger in CC1 state under room temperature only. Temperature is detected from THM pin.	0x0: Run CC1 in any temperatrue range 0x1: Run CC1 in Room temperature only
CC1TmoLimit	1	This bit controls if charger skips CC1 phase and proceeds to CC2 phase after CC1 timeout. CC1 timer is set by CC1FChgTmr.	0x0: Run CC1 phase with timer limitation 0x1: Run CC1 phase with no timer limitation
CC1Enable	0	Enable CC1 charging phase. Write to 0 to skip or disable CC1 charging phase.	0x0: CC1 phase disabled 0x1: CC1 phase enabled

ChgCntl1 (0x44)

BIT	7	6	5	4	3	2	1	0
Field	BatReChg[1:0]		BatReg[5:0]					
Reset	0x2		0xF					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BatReChg	7:6	Charger re-charge threshold in relation to BatReg[3:0].	0x0: V_{BatReg} - 50mV 0x1: V_{BatReg} - 100mV 0x2: V_{BatReg} - 150mV 0x3: V_{BatReg} - 200mV
BatReg	5:0	Charger battery regulation voltage.	Battery regulation voltage = BatReg x 0.01V + 4.05V. Capped to 4.6V. Do not recommend to set the value > 0x38.

ChgCntl2 (0x45)

BIT	7	6	5	4	3	2	1	0
Field	–	VPChg[2:0]			IPChg[1:0]		IChgDone[1:0]	
Reset	–	0x3			0x2		0x2	
Access Type	–	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
VPChg	6:4	Charger pre-charge voltage rising threshold.	0x0: 2.70V 0x1: 2.80V 0x2: 2.90V 0x3: 3.00V 0x4: 3.10V 0x5: 3.20V 0x6: 3.30V 0x7: 3.40V
IPChg	3:2	Charger pre-charge current.	0x0: 0.05 x $I_{CC2IFChg}$ 0x1: 0.10 x $I_{CC2IFChg}$ 0x2: 0.20 x $I_{CC2IFChg}$ 0x3: 0.30 x $I_{CC2IFChg}$
IChgDone	1:0	Charger charge-done current threshold.	0b00: 0.025 x $I_{CC2IFChg}$ 0b01: 0.05 x $I_{CC2IFChg}$ 0b10: 0.10 x $I_{CC2IFChg}$ 0b11: 0.20 x $I_{CC2IFChg}$

ChgTmr (0x46)

BIT	7	6	5	4	3	2	1	0
Field	MtChgTmr[1:0]		PChgTmr[1:0]		CC1FChgTmr[1:0]		ChgTmr[1:0]	
Reset	0x0		0x0		0x0		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MtChgTmr	7:6	Charger maintain charge timer.	0x0: 0min 0x1: 15min 0x2: 30min 0x3: 60min
PChgTmr	5:4	Charger pre-charge timer.	0x0: 30min 0x1: 60min 0x2: 120min 0x3: 240min
CC1FChgTmr	3:2	Charger fast charge CC1 timer.	0x0: 30min 0x1: 60min 0x2: 120min 0x3: 240min
ChgTmr	1:0	Charger Safety Timer. Runs during Pre-charge, CC1, CC2, and CC track/CV charge phases.	0x0: 75min 0x1: 150min 0x2: 300min 0x3: 600min

ChgCfg0 (0x47)

BIT	7	6	5	4	3	2	1	0
Field	–	ChgStepHys[2:0]			ChgStepRise[3:0]			
Reset	–	0x5			0x2			

Access Type	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ChgStepHys	6:4	Charger step charge voltage threshold hysteresis.	0x0: 100mV 0x1: 200mV 0x2: 300mV 0x3: 400mV 0x4: 500mV Others: 600mV
ChgStepRise	3:0	Charger step charge voltage rising threshold.	0x0: 3.80V 0x1: 3.85V 0x2: 3.90V 0x3: 3.95V 0x4: 4.00V 0x5: 4.05V 0x6: 4.10V 0x7: 4.15V 0x8: 4.20V 0x9: 4.25V 0xA: 4.30V 0xB: 4.35V 0xC: 4.40V 0xD: 4.45V 0xE: 4.50V 0xF: 4.55V

ThmCfg0 (0x48)

BIT	7	6	5	4	3	2	1	0
Field	ChgCoolCC1IFChg[2:0]			ChgCoolBatReg[1:0]		ChgCoolCC2IFChg[2:0]		
Reset	0x4			0x2		0x4		
Access Type	Write, Read			Write, Read		Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
ChgCoolCC1IFChg	7:5	Charger cool zone CC1 fast-charge current reduction.	0x0: 0.2 x $I_{CC1IFChg}$ 0x1: 0.3 x $I_{CC1IFChg}$ 0x2: 0.4 x $I_{CC1IFChg}$ 0x3: 0.5 x $I_{CC1IFChg}$ 0x4: 0.6 x $I_{CC1IFChg}$ 0x5: 0.7 x $I_{CC1IFChg}$ 0x6: 0.8 x $I_{CC1IFChg}$ 0x7: 1.0 x $I_{CC1IFChg}$
ChgCoolBatReg	4:3	Charger cool zone battery regulation voltage reduction.	0x0: V_{BatReg} - 150mV 0x1: V_{BatReg} - 100mV 0x2: V_{BatReg} - 50mV 0x3: V_{BatReg}
ChgCoolCC2IFChg	2:0	Charger cool zone CC2 fast-charge current reduction.	0x0: 0.2 x $I_{CC2IFChg}$ 0x1: 0.3 x $I_{CC2IFChg}$ 0x2: 0.4 x $I_{CC2IFChg}$ 0x3: 0.5 x $I_{CC2IFChg}$ 0x4: 0.6 x $I_{CC2IFChg}$ 0x5: 0.7 x $I_{CC2IFChg}$ 0x6: 0.8 x $I_{CC2IFChg}$ 0x7: 1.0 x $I_{CC2IFChg}$

ThmCfg1 (0x49)

BIT	7	6	5	4	3	2	1	0
Field	ChgRoomCC1IFChg[2:0]			ChgRoomBatReg[1:0]		ChgRoomCC2IFChg[2:0]		
Reset	0x7			0x3		0x7		
Access Type	Write, Read			Write, Read		Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
ChgRoomCC1IFChg	7:5	Charger room zone CC1 fast-charge current reduction.	0x0: 0.2 x $I_{CC1IFChg}$ 0x1: 0.3 x $I_{CC1IFChg}$ 0x2: 0.4 x $I_{CC1IFChg}$ 0x3: 0.5 x $I_{CC1IFChg}$ 0x4: 0.6 x $I_{CC1IFChg}$ 0x5: 0.7 x $I_{CC1IFChg}$ 0x6: 0.8 x $I_{CC1IFChg}$ 0x7: 1.0 x $I_{CC1IFChg}$
ChgRoomBatReg	4:3	Charger room zone battery regulation voltage reduction.	0x0: V_{BatReg} - 150mV 0x1: V_{BatReg} - 100mV 0x2: V_{BatReg} - 50mV 0x3: V_{BatReg}
ChgRoomCC2IFChg	2:0	Charger room zone CC2 fast-charge current reduction.	0x0: 0.2 x $I_{CC2IFChg}$ 0x1: 0.3 x $I_{CC2IFChg}$ 0x2: 0.4 x $I_{CC2IFChg}$ 0x3: 0.5 x $I_{CC2IFChg}$ 0x4: 0.6 x $I_{CC2IFChg}$ 0x5: 0.7 x $I_{CC2IFChg}$ 0x6: 0.8 x $I_{CC2IFChg}$ 0x7: 1.0 x $I_{CC2IFChg}$

ThmCfg2 (0x4A)

BIT	7	6	5	4	3	2	1	0
Field	ChgWarmCC1IFChg[2:0]			ChgWarmBatReg[1:0]		ChgWarmCC2IFChg[2:0]		
Reset	0x3			0x1		0x3		
Access Type	Write, Read			Write, Read		Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
ChgWarmCC1IFChg	7:5	Charger warm zone CC1 fast-charge current reduction.	0x0: 0.2 x $I_{CC1IFChg}$ 0x1: 0.3 x $I_{CC1IFChg}$ 0x2: 0.4 x $I_{CC1IFChg}$ 0x3: 0.5 x $I_{CC1IFChg}$ 0x4: 0.6 x $I_{CC1IFChg}$ 0x5: 0.7 x $I_{CC1IFChg}$ 0x6: 0.8 x $I_{CC1IFChg}$ 0x7: 1.0 x $I_{CC1IFChg}$
ChgWarmBatReg	4:3	Charger warm zone battery regulation voltage reduction.	0x0: V_{BatReg} - 150mV 0x1: V_{BatReg} - 100mV 0x2: V_{BatReg} - 50mV 0x3: V_{BatReg}

BITFIELD	BITS	DESCRIPTION	DECODE
ChgWarmCC2IFChg	2:0	Charger warm zone CC2 fast-charge current reduction.	0x0: 0.2 x $I_{CC2IFChg}$ 0x1: 0.3 x $I_{CC2IFChg}$ 0x2: 0.4 x $I_{CC2IFChg}$ 0x3: 0.5 x $I_{CC2IFChg}$ 0x4: 0.6 x $I_{CC2IFChg}$ 0x5: 0.7 x $I_{CC2IFChg}$ 0x6: 0.8 x $I_{CC2IFChg}$ 0x7: 1.0 x $I_{CC2IFChg}$

ThmCfg3 (0x4B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	ChgT1ThrDef[2:0]			ChgT1ThrCC1[2:0]		
Reset	–	–	0x4			0x4		
Access Type	–	–	Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
ChgT1ThrDef	5:3	JEITA T1 cold default temperature threshold. V_{THM} rising threshold between cold and cool zone. Applies for BatReg and CC2 JEITA reduction settings.	0x0: -20ºC 0x1: -15ºC 0x2: -10ºC 0x3: -5ºC 0x4: 0ºC 0x5: 5ºC 0x6: 10ºC 0x7: 15ºC
ChgT1ThrCC1	2:0	JEITA T1 CC1 cold temperature threshold. V_{THM} rising threshold between cold and cool zone. Applies for CC1 JEITA reduction settings.	0x0: -20ºC 0x1: -15ºC 0x2: -10ºC 0x3: -5ºC 0x4: 0ºC 0x5: 5ºC 0x6: 10ºC 0x7: 15ºC

ThmCfg4 (0x4C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	ChgT2ThrDef[2:0]			ChgT2ThrCC1[2:0]		
Reset	–	–	0x5			0x5		
Access Type	–	–	Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
ChgT2ThrDef	5:3	JEITA T2 cool default temperature threshold. V_{THM} rising threshold between cool and room	0x0: -10ºC 0x1: -5ºC 0x2: 0ºC 0x3: 5ºC

BITFIELD	BITS	DESCRIPTION	DECODE
		zone. Applies for BatReg and CC2 JEITA reduction settings.	0x4: 10ºC 0x5: 15ºC 0x6: 20ºC 0x7: 25ºC
ChgT2ThrCC1	2:0	JEITA T2 CC1 cool temperature threshold. V_{THM} rising threshold between cool and room zone. Applies for CC1 JEITA reduction settings.	0x0: -10ºC 0x1: -5ºC 0x2: 0ºC 0x3: 5ºC 0x4: 10ºC 0x5: 15ºC 0x6: 20ºC 0x7: 25ºC

ThmCfg5 (0x4D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	ChgT3ThrDef[2:0]			ChgT3ThrCC1[2:0]		
Reset	–	–	0x2			0x2		
Access Type	–	–	Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
ChgT3ThrDef	5:3	JEITA T3 warm default temperature threshold. V_{THM} falling threshold between warm and room zone. Applies for BatReg and CC2 JEITA reduction settings.	0x0: 20ºC 0x1: 25ºC 0x2: 30ºC 0x3: 35ºC 0x4: 40ºC 0x5: 45ºC 0x6: 50ºC 0x7: 55ºC
ChgT3ThrCC1	2:0	JEITA T3 CC1 warm temperature threshold. V_{THM} falling threshold between warm and room zone. Applies for CC1 JEITA reduction settings.	0x0: 20ºC 0x1: 25ºC 0x2: 30ºC 0x3: 35ºC 0x4: 40ºC 0x5: 45ºC 0x6: 50ºC 0x7: 55ºC

ThmCfg6 (0x4E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	ChgT4ThrDef[2:0]			ChgT4ThrCC1[2:0]		
Reset	–	–	0x2			0x2		
Access Type	–	–	Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
ChgT4ThrDef	5:3	JEITA T4 hot default temperature threshold. V_{THM} falling threshold between hot and warm zone. Applies for BatReg and CC2 JEITA reduction settings.	0x0: 35ºC 0x1: 40ºC 0x2: 45ºC 0x3: 50ºC 0x4: 55ºC 0x5: 60ºC 0x6: 65ºC 0x7: 70ºC
ChgT4ThrCC1	2:0	JEITA T4 CC1 hot temperature threshold. V_{THM} falling threshold between hot and warm zone. Applies for CC1 JEITA reduction settings.	0x0: 35ºC 0x1: 40ºC 0x2: 45ºC 0x3: 50ºC 0x4: 55ºC 0x5: 60ºC 0x6: 65ºC 0x7: 70ºC

ThmCfg7 (0x4F)

BIT	7	6	5	4	3	2	1	0
Field	jta_eoc_sel[1:0]		–	–	THMPUSel	ThmEn[2:0]		
Reset	0x0		–	–	0x0	0x0		
Access Type	Write, Read		–	–	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
jta_eoc_sel	7:6	JEITA measurement period. Valid only when PLC is not present and ThmEn > 0x3. New setting of this bit can be effective only after ThmEn is set to 0 and then set to > 0x03 values.	0x0: Every 1s 0x1: Every 2s 0x2: Every 4s 0x3: Every 8s
THMPUSel	3	THM internal pullup resistance.	0x0: 10kΩ 0x1: 100kΩ
ThmEn	2:0	Charger thermistor monitoring control. JEITA temperature is measured from THM pin.	0x0: Thermistor monitoring disabled. 0x1: Thermistor monitoring enabled when PLC is present. Battery is charged in the cool and room temperature zones due to JEITA. 0x2: Thermistor monitoring enabled when PLC is present. Battery is charged in the room and warm temperature zones due to JEITA. 0x3: Thermistor monitoring enabled when PLC is present. Battery is charged in the cool, room and warm temperature zones due to JEITA. 0x4: Thermistor monitoring permanently enabled, but charger not affected by JEITA. 0x5: Thermistor monitoring permanently enabled. Battery is charged only in the cool and room temperature zones due to JEITA. 0x6: Thermistor monitoring permanently enabled. Battery is charged only in the room and warm temperature zones due to JEITA. 0x7: Thermistor monitoring permanently enabled. Battery is charged only in the cool, room and warm temperature zones due to JEITA.

ChgCtr1 (0x50)

BIT	7	6	5	4	3	2	1	0
Field	i2c_crf_ena	chg_cc_trk	ChgStsFCMrg	vlt_dne_ena	–	lng_xfer_opt	–	–
Reset	0x1	0x1	0x0	0x0	–	0x0	–	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	–	Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
i2c_crf_ena	7	Battery recharge threshold comparator enable.	0x0: Battery recharge monitor disabled 0x1: Battery recharge monitor enabled
chg_cc_trk	6	CC track enable. Charger uses CV mode if CC track is disabled. Recommend to keep this bit to 1 to enable CC track.	0x0: Disable 0x1: Enable
ChgStsFCMrg	5	Combine CC track/CV mode with CC2 reported in ChgStat.	0x0: All internal states are reported 0x1: CC track and CV mode are merged in CC2
vlt_dne_ena	4	Skip Mantain Charge status in case of JEITA voltage regulation.	0x0: Enable charging in Mantain Charge under JEITA battery voltage reduction condition. 0x1: Disable charging in Mantain Charge under JEITA battery voltage reduction condition. Skip charger Mantain Charge status.
lng_xfer_opt	2	Bit to enable charger's freeze during Long PLC xfer	0x0: Charger freeze only in short transfer: PING and PLC commands. 0x1: Charger freeze in all PLC transfers: PING, PLC command and bulk data transfer.

ChgCtr2 (0x51)

BIT	7	6	5	4	3	2	1	0
Field	BattUvloEna	BattPullDown	FrcPChg	–	–	–	vlt_ctr_plc[1:0]	
Reset	0x0	0x0	0x0	–	–	–	0x0	
Access Type	Write, Read	Write, Read	Write, Read	–	–	–	Read Only	

BITFIELD	BITS	DESCRIPTION	DECODE
BattUvloEna	7		
BattPullDown	6	Battery voltage pull down by internal pulldown resistor.	0: Pulldown resistor disabled 1: Pulldown resistor enabled
FrcPChg	5	Charger forced precharge mode. Valid only if ChgEn = 1.	0: Charger operating normally 1: Charge current is forced to precharge current
vlt_ctr_plc	1:0	PLC voltage up/down request from slave to master	0x1: Decrease 0x2: Increase Others: Hold

GPIO1 (0x58)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	GPIOCmpEna1	GPIOPLCCtr1	GPIOEnRes1	GPIOEnPup1	GPIODout_1
Reset	–	–	–	0x1	0x1	0x0	0x0	0x0
Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
GPIOCmpEna1	4	GPIO comparator enable.	0x0: Disable 0x1: Enable
GPIOPLCCtr1	3	GPIO I2C or PLC control	0x0: I2C control 0x1: PLC control
GPIOEnRes1	2	GPIO input or output configuration.	0x0: Output 0x1: Input
GPIOEnPup1	1	GPIO input pullup or pulldown resistor. Active if GPIOEnRes =1.	0x0: Pull down 0x1: Pull up
GPIODout_1	0	GPIO open drain output. Needs external pullup.	0x0: High 0x1: Low

GPIO2 (0x59)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	GPIOCmpEna2	GPIOPLCCtr2	GPIOEnRes2	GPIOEnPup2	GPIODout_2
Reset	–	–	–	0x1	0x1	0x0	0x0	0x0
Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
GPIOCmpEna2	4	GPIO comparator enable.	0x0: Disable 0x1: Enable
GPIOPLCCtr2	3	GPIO I2C or PLC control	0x0: I2C control 0x1: PLC control
GPIOEnRes2	2	GPIO input or output configuration.	0x0: Output 0x1: Input
GPIOEnPup2	1	GPIO input pullup or pulldown resistor. Active if GPIOEnRes =1.	0x0: Pull down 0x1: Pull up
GPIODout_2	0	GPIO open drain output. Needs external pull-up.	0x0: High 0x1: Low

GPIO3 (0x5A)

BIT	7	6	5	4	3	2	1	0

Field	–	–	–	GPIOCmpEna3	GPIOPLCCtr3	GPIOEnRes3	GPIOEnPup3	GPIODout_3
Reset	–	–	–	0x1	0x1	0x0	0x0	0x0
Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
GPIOCmpEna3	4	GPIO comparator enable.	0x0: Disable 0x1: Enable
GPIOPLCCtr3	3	GPIO I2C or PLC control	0x0: I2C control 0x1: PLC control
GPIOEnRes3	2	GPIO input or output configuration.	0x0: Output 0x1: Input
GPIOEnPup3	1	GPIO input pullup or pulldown resistor. Active if GPIOEnRes =1.	0x0: Pull down 0x1: Pull up
GPIODout_3	0	GPIO open drain output. Needs external pull-up.	0x0: High 0x1: Low

GPIO4 (0x5B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	GPIOCmpEna4	GPIOPLCCtr4	GPIOEnRes4	GPIOEnPup4	GPIODout_4
Reset	–	–	–	0x1	0x1	0x0	0x0	0x0
Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
GPIOCmpEna4	4	GPIO comparator enable.	0x0: Disable 0x1: Enable
GPIOPLCCtr4	3	GPIO I2C or PLC control	0x0: I2C control 0x1: PLC control
GPIOEnRes4	2	GPIO input or output configuration.	0x0: Output 0x1: Input
GPIOEnPup4	1	GPIO input pullup or pulldown resistor. Active if GPIOEnRes =1.	0x0: Pull down 0x1: Pull up
GPIODout_4	0	GPIO open drain output. Needs external pull-up.	0x0: High 0x1: Low

GPIO_rdb1 (0x5C)

BIT	7	6	5	4	3	2	1	0
Field	GPIODAInp_4	GPIODAInp_3	GPIODAInp_2	GPIODAInp_1	–	–	–	GPIOCmosEn
Reset	0x0	0x0	0x0	0x0	–	–	–	0x0

Access Type	Read Only	Read Only	Read Only	Read Only	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
GPIODAInp_4	7	GPIO input status. Valid only when GPIOCmpEna = 1.	0x0: Low 0x1: High
GPIODAInp_3	6	GPIO input status. Valid only when GPIOCmpEna = 1.	0x0: Low 0x1: High
GPIODAInp_2	5	GPIO input status. Valid only when GPIOCmpEna = 1.	0x0: Low 0x1: High
GPIODAInp_1	4	GPIO input status. Valid only when GPIOCmpEna = 1.	0x0: Low 0x1: High
GPIOCmosEn	0	GPIO input logic threshold.	0x0: 1.8V VDIG 0x1: VCCINT

GPIO_rdb2 (0x5D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	master_GPIO4	master_GPIO3	master_GPIO2	master_GPIO1
Reset	–	–	–	–	0x0	0x0	0x0	0x0
Access Type	–	–	–	–	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
master_GPIO4	3	Master GPIO4 status.	0x0: Low 0x1: High
master_GPIO3	2	Master GPIO3 status.	0x0: Low 0x1: High
master_GPIO2	1	Master GPIO2 status.	0x0: Low 0x1: High
master_GPIO1	0	Master GPIO1 status.	0x0: Low 0x1: High

SOC_byte_1 (0x60)

BIT	7	6	5	4	3	2	1	0
Field	AVGVCELL_byte_1[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
AVGVCELL_byte_1	7:0	Average cell voltage byte1 readback from fuel gauge. It is moving average of last 45 seconds.	Concatenate byte1 and byte0: LSB is 78.125uV. The full scale is 5.12V.

SOC_byte_0 (0x61)

BIT	7	6	5	4	3	2	1	0
Field	AVGVCELL_byte_0[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
AVGVCELL_byte_0	7:0	Average cell voltage byte0 readback from fuel gauge. It is moving average of last 45 seconds.	Concatenate byte1 and byte0: LSB is 78.125uV. The full scale is 5.12V.

VCELL_byte_1 (0x62)

BIT	7	6	5	4	3	2	1	0
Field	VCELL_byte_1[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
VCELL_byte_1	7:0	Cell voltage byte1 readback from fuel gauge.	Concatenate byte1 and byte0: LSB is 78.125uV. The full scale is 5.12V.

VCELL_byte_0 (0x63)

BIT	7	6	5	4	3	2	1	0
Field	VCELL_byte_0[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
VCELL_byte_0	7:0	Cell voltage byte0 readback from fuel gauge.	Concatenate byte1 and byte0: LSB is 78.125uV. The full scale is 5.12V.

TTE_byte_1 (0x64)

BIT	7	6	5	4	3	2	1	0
Field	TTE_byte_1[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
TTE_byte_1	7:0	Time to empty byte1 readback from fuel gauge.	Concatenate byte1 and byte0: LSB is 5.625s. The full scale is 102.4 hours.

TTE_byte_0 (0x65)

BIT	7	6	5	4	3	2	1	0
Field	TTE_byte_0[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
TTE_byte_0	7:0	Time to empty byte0 readback from fuel gauge.	Concatenate byte1 and byte0: LSB is 5.625s. The full scale is 102.4 hours.

AVGVCELL_byte_1 (0x66)

BIT	7	6	5	4	3	2	1	0
Field	SOC_byte_1[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
SOC_byte_1	7:0	SOC byte1 readback from fuel gauge.	Concatenate byte1 and byte0: LSB is 0.00390625% of full charge. The full scale is 256%.

AVGVCELL_byte_0 (0x67)

BIT	7	6	5	4	3	2	1	0
Field	SOC_byte_0[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
SOC_byte_0	7:0	SOC byte0 readback from fuel gauge.	Concatenate byte1 and byte0: LSB is 0.00390625% of full charge. The full scale is 256%.

TTF_byte_1 (0x68)

BIT	7	6	5	4	3	2	1	0
Field	TTF_byte_1[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
TTF_byte_1	7:0	Time to full byte1 readback from fuel gauge.	Concatenate byte1 and byte0: LSB is 5.625s. The full scale is 102.4 hours.

TTF_byte_0 (0x69)

BIT	7	6	5	4	3	2	1	0
Field	TTF_byte_0[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
TTF_byte_0	7:0	Time to full byte0 readback from fuel gauge.	Concatenate byte1 and byte0: LSB is 5.625s. The full scale is 102.4 hours.

READY_REG (0x6A)

BIT	7	6	5	4	3	2	1	0
Field	dop_rdy_sig	–	dop_i2c_ena	ttf_reg_rdy	soc_reg_rdy	tte_reg_rdy	vcell_reg_rdy	avgvcell_reg_rdy
Reset	0x0	–	0b1	0b0	0x0	0x0	0x0	0x0
Access Type	Read Only	–	Write, Read	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
dop_rdy_sig	7	DOP port ready.	0x0: Not ready 0x1: Ready
dop_i2c_ena	5	Enable the DOP PORT sniffer.	0x0: Disable 0x1: Enable
ttf_reg_rdy	4	TTF byte value is reliable.	0x0: Not reliable 0x1: Reliable
soc_reg_rdy	3	SOC byte value is reliable	0x0: Not reliable 0x1: Reliable
tte_reg_rdy	2	TTE byte value is reliable	0x0: Not reliable 0x1: Reliable
vcell_reg_rdy	1	VCELL byte value is reliable	0x0: Not reliable 0x1: Reliable
avgvcell_reg_rdy	0	AVGVCELL byte value is reliable	0x0: Not reliable 0x1: Reliable

ADC_CTRL1 (0x70)

BIT	7	6	5	4	3	2	1	0
Field	–	AdcGndTrh[3:0]				ResDetRty[2:0]		
Reset	–	0x4				0x1		
Access Type	–	Write, Read				Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
AdcGndTrh	6:3	ADC Ground Threshold.	LSB = 5.882mV
ResDetRty	2:0	Number of Resistive Measurement Retries. The device retries the measurement if one of the following conditions is true:	0x0: No retry. >0x0: Number of retry attempts.

BITFIELD	BITS	DESCRIPTION	DECODE
		1. (maximum ADC reading = 0xFF) AND (pullup current = 1µA) AND (average ADC reading < (0xFF - ADCNoiseClampRng[5:0])) 2. (maximum ADC reading = 0xFF) AND (pullup current ≠ 1µA) If the condition is still true after this number of retries, the Abort result is reported.	

ADC_CTRL2 (0x71)

BIT	7	6	5	4	3	2	1	0
Field	–	–	AdcRng[5:0]					
Reset	–	–	0x9					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
AdcRng	5:0	ADC Shift Factor. It applies to resistive measurements used in Moisture Detection. This register must NOT be set lower than the default value.	LSB = 5.882mV

ADC_CTRL3 (0x72)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	AdcAvgNum[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
AdcAvgNum	2:0	Number of Samples in ADC Reading Averaging. It applies to any resistive measurements used in moisture detection and accessory mode detection.	0x0: 1 sample 0x1: 2 samples 0x2: 4 samples 0x3: 8 samples 0x4: 16 samples 0x5: 32 samples 0x6: 64 samples 0x7: 128 samples

ADC_CTRL4 (0x73)

BIT	7	6	5	4	3	2	1	0
Field	–	–	AdcNoiseCtr[5:0]					
Reset	–	–	0x0					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
AdcNoiseCtr	5:0	ADC Result Margin to Account for External Noise and Avoid Result Clamping Close to Full-Scale. This register must NOT be changed from the default value.	LSB = 5.882mV

MOI_DET_REG1 (0x74)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	RaccDetMIp[1:0]	
Reset	–	–	–	–	–	–	0x0	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RaccDetMIp	1:0	Target current used to specify moisture resistance threshold.	0x0: 1µA 0x1: 4µA 0x2: 16µA 0x3: 64µA

MOI_DET_REG2 (0x75)

BIT	7	6	5	4	3	2	1	0
Field	RaccDetMThr[7:0]							
Reset	0x77							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RaccDetMThr	7:0	Moisture detection voltage threshold.	LSB = 5.882mV.

MOI_DET_REG3 (0x76)

BIT	7	6	5	4	3	2	1	0
Field	–	moi_det_aut	–	moi_man__pl	–	moi_man_rty	–	moi_aut_rty
Reset	–	0x1	–	0b0	–	0b0	–	0x1
Access Type	–	Write, Read	–	Write, Read	–	Write, Read	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
moi_det_aut	6	Enable automatic moisture detection on PLC, performed with 16s rate starting 16s after device turn on.	0x0: Disabled 0x1: Enabled
moi_man__pl	4	Manual moisture request on PLC. Write 1 to launch manual moisture detection. Autoclearing when done.	0x0: No moisture in progress 0x1: Moisture in progress
moi_man_rty	2	Manual retry for master detection in case of moisture found. Only valid when moisture is previously found. Write 1 to launch moisture retry. This allow the master detection to run moisture detection again. Autoclearing when retry is done.	0x0: No retry request 0x1: Retry request running
moi_aut_rty	0	Enable the automatic re-arm of mositure detection for PLC detection if moisture is found. System re-arm moisture automatically when moisture disappear.	0x0: Disable 0x1: Enabled

IP (0x77)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	IP__RES_DET[1:0]	
Reset	–	–	–	–	–	–	0x0	
Access Type	–	–	–	–	–	–	Read Only	

BITFIELD	BITS	DESCRIPTION	DECODE
IP__RES_DET	1:0	Final current used when moisture measurement is complete. It is set to 0x0 if the result is Abort or Open. It is set to 0x3 if the result is Short.	0x0: 1µA 0x1: 4µA 0x2: 16µA 0x3: 64µA

ADC_VAL1 (0x78)

BIT	7	6	5	4	3	2	1	0
Field	ADCAvg[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
ADCAvg	7:0	Final Average ADC Reading. It is set to 0x00 if the result is Abort or Ground, and to 0xFF if the result is Open.	LSB = 5.882mV = 0.392% typ.

ADC_VAL2 (0x79)

BIT	7	6	5	4	3	2	1	0
Field	ADCMax[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
ADCMax	7:0	Final Maximum ADC Reading. It is set to 0x00 if the result is Abort or Ground, and to 0xFF if the result is Open.	LSB = 5.882mV = 0.392% typ.

ADC_VAL3 (0x7A)

BIT	7	6	5	4	3	2	1	0
Field	ADCMin[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
ADCMin	7:0	Final Minimum ADC Reading. It is set to 0x00 if the result is Abort or Ground, and to 0xFF if the result is Open.	LSB = 5.882mV = 0.392% typ.

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX20357EWX+	-40°C to 85°C	36-WLP
MAX20357EWX+T	-40°C to 85°C	36-WLP

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/22	Release for Market Intro	—

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