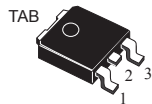
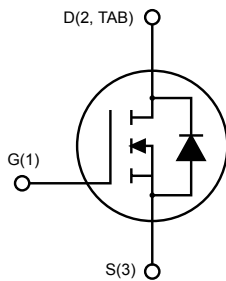



## Automotive-grade N-channel 60 V, 32 mΩ typ., 24 A, STripFET II Power MOSFET in a DPAK package


**DPAK**


AM01475v1\_noZen

### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>	P <sub>TOT</sub>
STD20NF06LAG	60 V	40 mΩ	24 A	60 W

- AEC-Q101 qualified 
- Exceptional dv/dt capability
- 100% avalanche tested
- Low gate charge

### Applications

- Switching applications

### Description

This Power MOSFET has been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.



#### Product status link

[STD20NF06LAG](#)

#### Product summary

<b>Order code</b>	STD20NF06LAG
<b>Marking</b>	D20NF06L
<b>Package</b>	DPAK
<b>Packing</b>	Tape and reel

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	60	V
$V_{GS}$	Gate-source voltage	±18	V
$I_D$	Drain current (continuous) at $T_{case} = 25\text{ °C}$	24	A
	Drain current (continuous) at $T_{case} = 100\text{ °C}$	17	
$I_{DM}^{(1)}$	Drain current (pulsed)	96	A
$P_{TOT}$	Total power dissipation at $T_{case} = 25\text{ °C}$	60	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	10	V/ns
$E_{AS}^{(3)}$	Single pulse avalanche energy	225	mJ
$T_{stg}$	Storage temperature range	-55 to 175	°C
$T_j$	Operating junction temperature range		

1. Pulse width is limited by safe operating area.
2.  $I_{SD} \leq 24\text{ A}$ ,  $di/dt \leq 300\text{ A/ns}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$
3. Starting  $T_j = 25\text{ °C}$ ,  $I_D = 14\text{ A}$ ,  $V_{DD} = 60\text{ V}$ .

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.5	°C/W
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	50	

1. When mounted on a 1-inch<sup>2</sup> FR-4, 2 Oz copper board.

## 2 Electrical characteristics

( $T_{\text{case}} = 25\text{ °C}$  unless otherwise specified)

**Table 3. Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	60			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}, V_{DS} = 60\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}, V_{DS} = 60\text{ V}, T_{\text{case}} = 125\text{ °C}^{(1)}$			10	
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 18\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1		2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 12\text{ A}$		32	40	m $\Omega$
		$V_{GS} = 5\text{ V}, I_D = 12\text{ A}$			50	

1. Defined by design, not subject to production test.

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}, f = 1\text{ MHz}, V_{GS} = 0\text{ V}$	-	660	-	$\mu\text{F}$
$C_{oss}$	Output capacitance		-	170	-	
$C_{riss}$	Reverse transfer capacitance		-	70	-	
$Q_g$	Total gate charge	$V_{DD} = 30\text{ V}, I_D = 20\text{ A}, V_{GS} = 5\text{ V}$ (see Figure 12. Test circuit for gate charge behavior)	-	13	-	nC
$Q_{gs}$	Gate-source charge		-	3.5	-	
$Q_{gd}$	Gate-drain charge		-	8	-	

**Table 5. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 30\text{ V}, I_D = 10\text{ A}, R_G = 4.7\text{ }\Omega, V_{GS} = 5\text{ V}$ (see Figure 11. Test circuit for resistive load switching times and Figure 16. Switching time waveform)	-	11	-	ns
$t_r$	Rise time		-	50	-	
$t_{d(off)}$	Turn-off delay time		-	20	-	
$t_f$	Fall time		-	12	-	

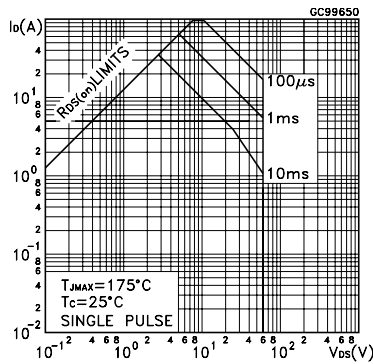
**Table 6. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		24	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		96	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 24\text{ A}$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 20\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 20\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 13. Test circuit for inductive load switching and diode recovery times</a> )	-	56		ns
$Q_{rr}$	Reverse recovery charge		-	108		nC
$I_{RRM}$	Reverse recovery current		-	4		A

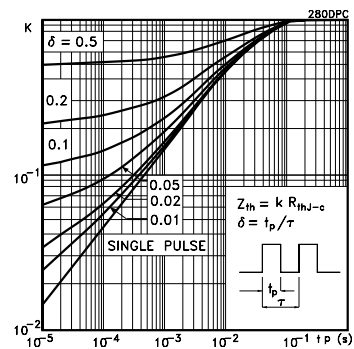
1. Pulse width is limited by safe operating area.
2. Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

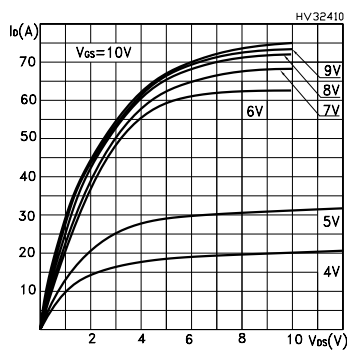
**Figure 1. Safe operating area**



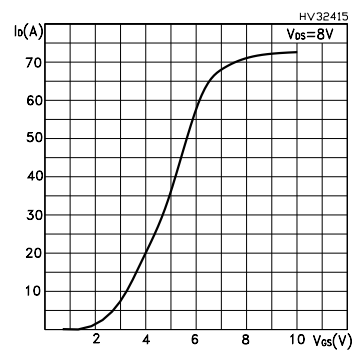
**Figure 2. Thermal impedance**



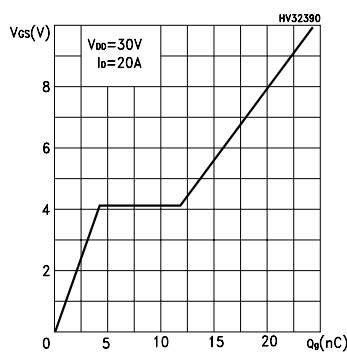
**Figure 3. Output characteristics**



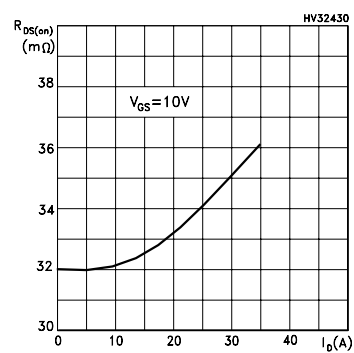
**Figure 4. Transfer characteristics**



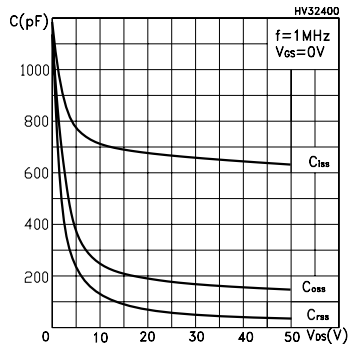
**Figure 5. Gate charge vs gate-source voltage**



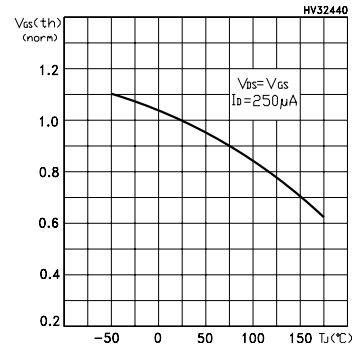
**Figure 6. Static drain-source on-resistance**



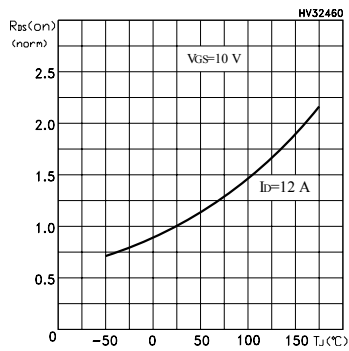
**Figure 7. Capacitance variations**



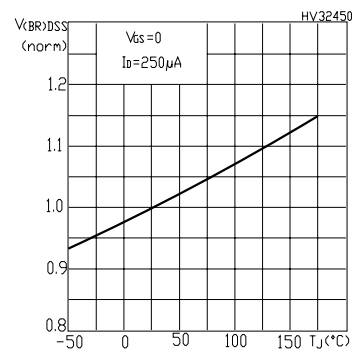
**Figure 8. Normalized gate threshold voltage vs temperature**



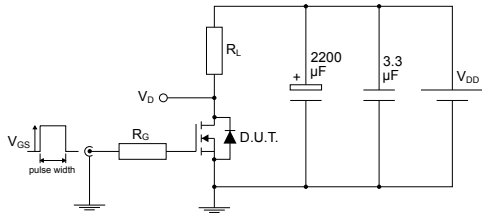
**Figure 9. Normalized on-resistance vs temperature**



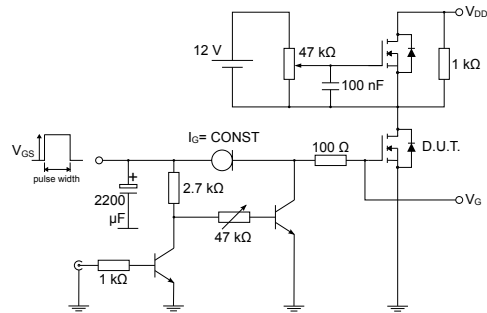
**Figure 10. Normalized V<sub>(BR)DSS</sub> vs temperature**



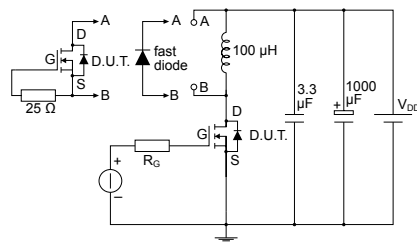
### 3 Test circuits

**Figure 11. Test circuit for resistive load switching times**


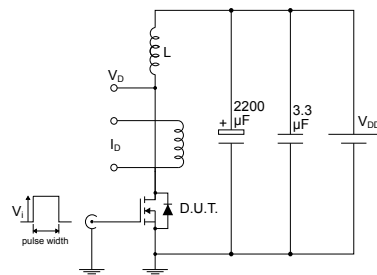
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**Figure 12. Test circuit for gate charge behavior**


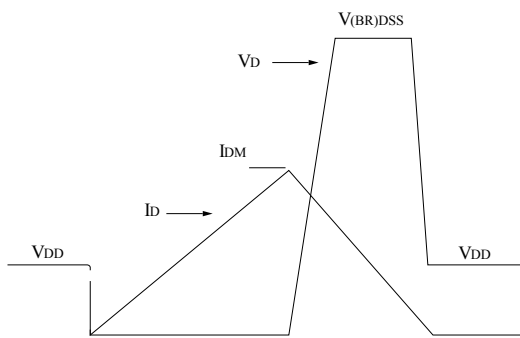
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**Figure 13. Test circuit for inductive load switching and diode recovery times**


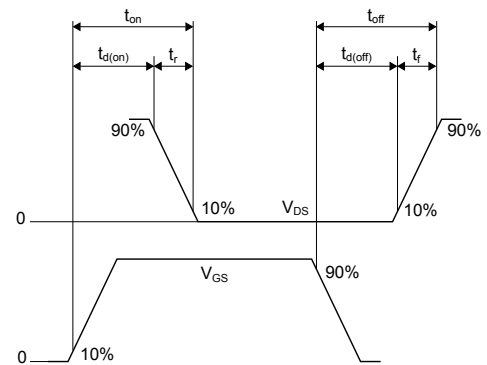
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**Figure 14. Unclamped inductive load test circuit**


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**Figure 15. Unclamped inductive waveform**


AM01472v1

**Figure 16. Switching time waveform**


AM01473v1

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## 4 Package information

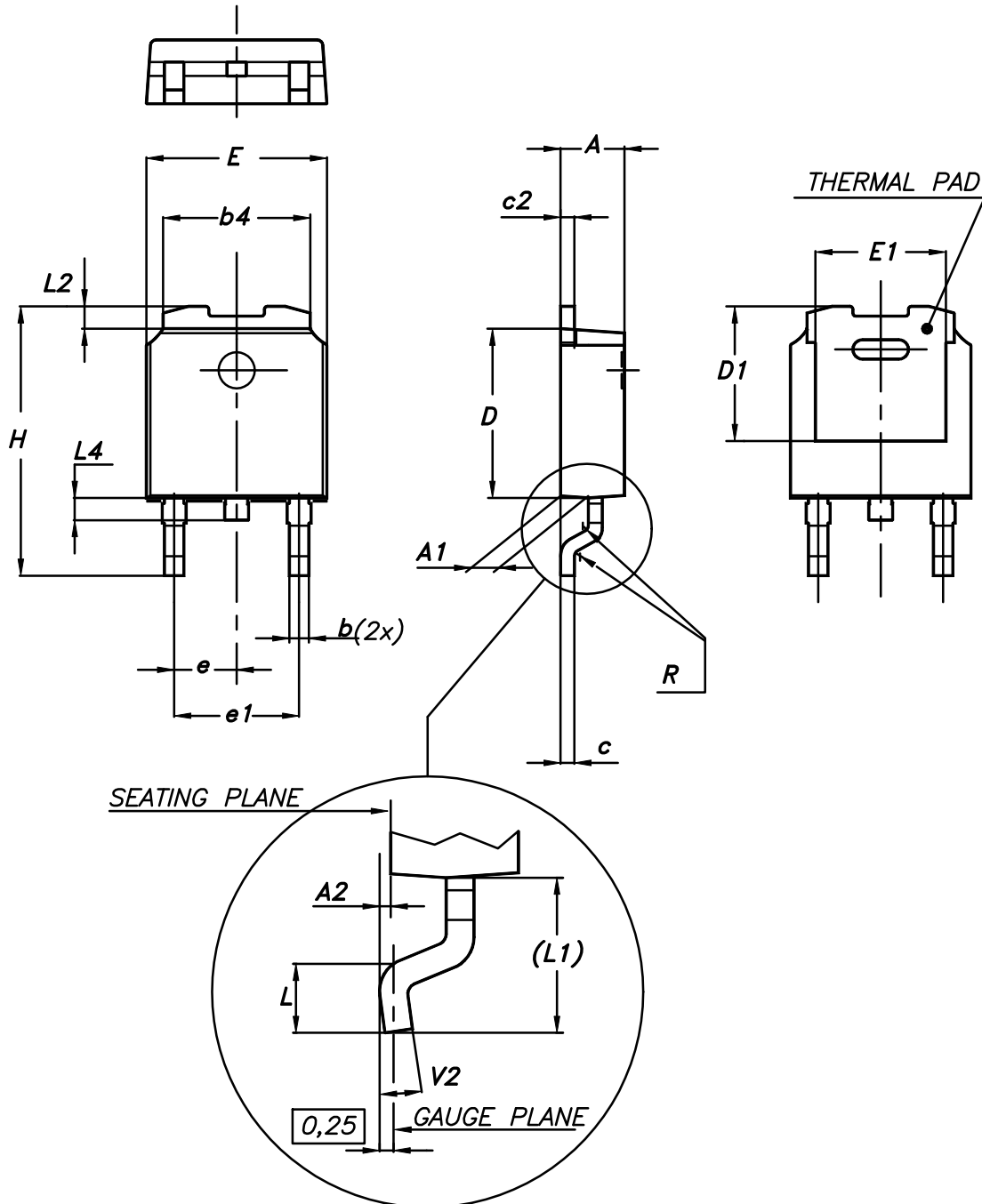
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In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.



### 4.1 DPAK (TO-252) type A package information

Figure 17. DPAK (TO-252) type A package outline

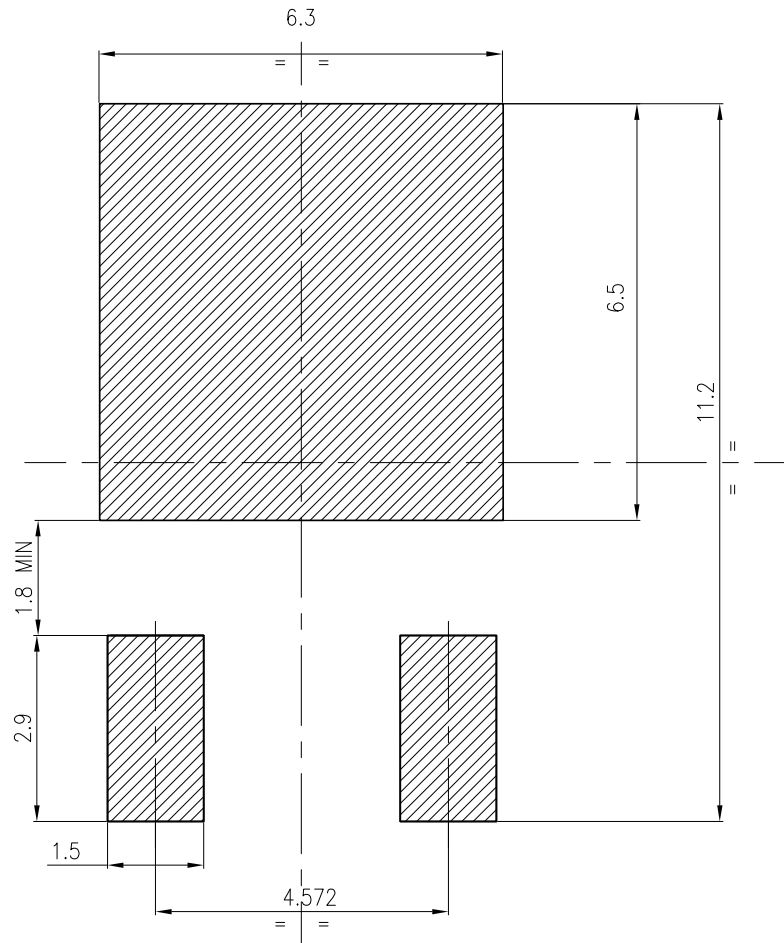


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**Table 7. DPAK (TO-252) type A mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

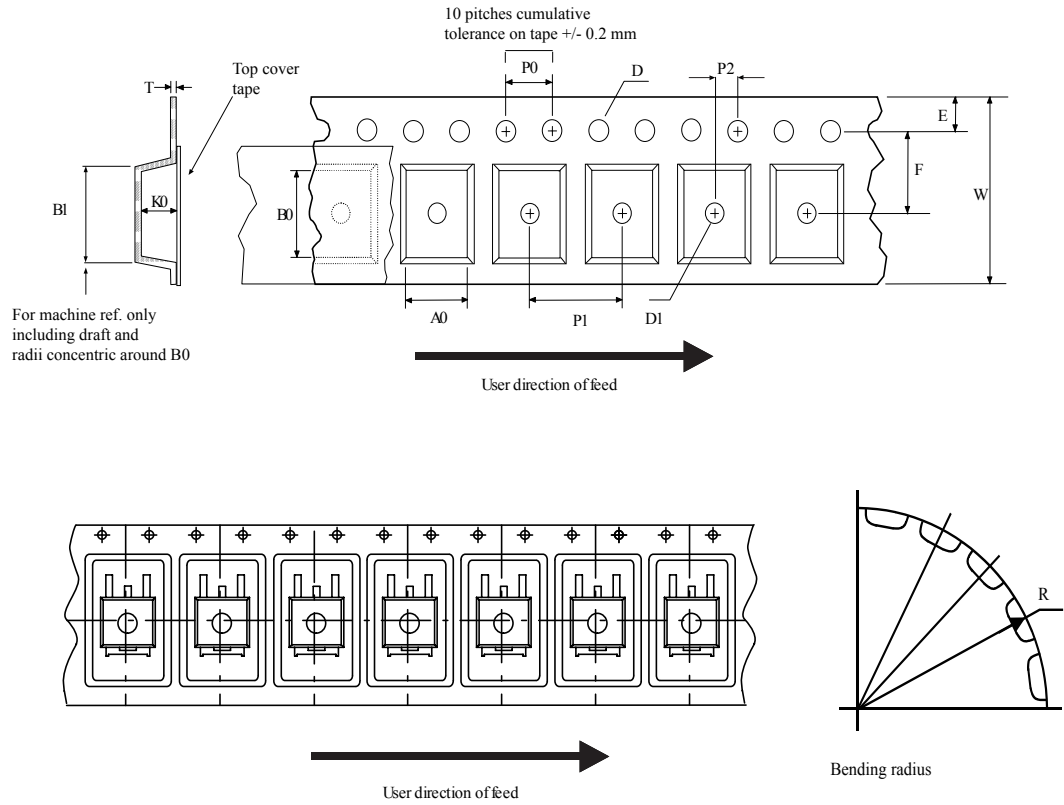
**Figure 18. DPAK (TO-252) type A recommended footprint (dimensions are in mm)**



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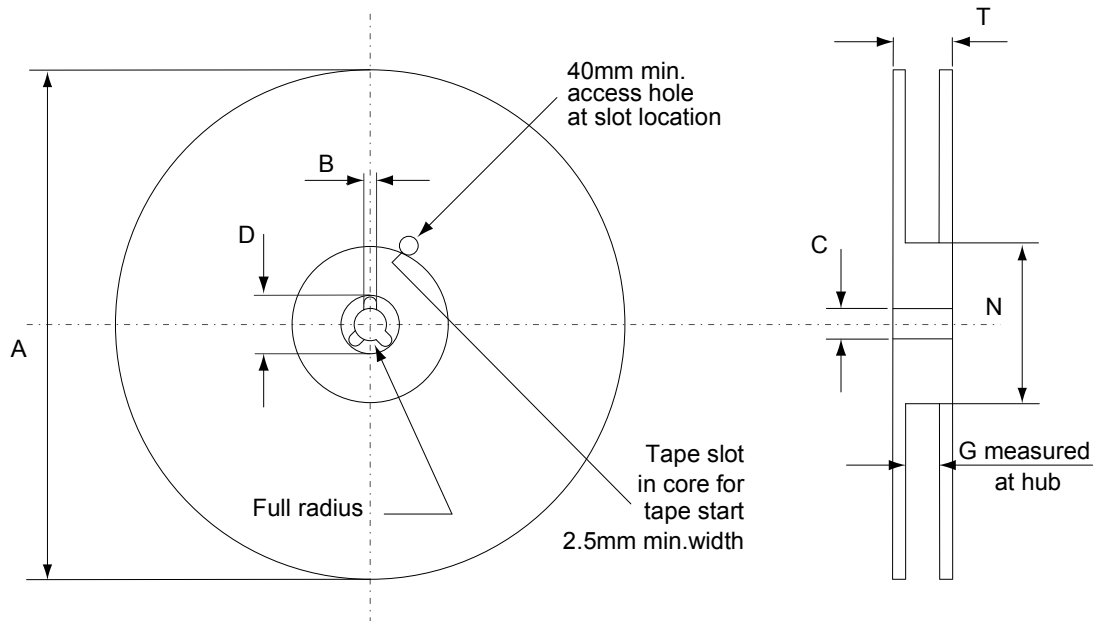
## 4.2 DPAK (TO-252) packing information

Figure 19. DPAK (TO-252) tape outline



AM08852v1

**Figure 20. DPAK (TO-252) reel outline**



AM06038v1

**Table 8. DPAK (TO-252) tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

## Revision history

**Table 9. Document revision history**

Date	Revision	Changes
25-Oct-2016	1	First release.
20-Mar-2017	2	Modified <i>Table 2: "Absolute maximum ratings"</i> , <i>Table 5: "Dynamic"</i> , <i>Table 6: "Switching times"</i> and <i>Table 7: "Source-drain diode"</i> . Modified <i>Figure 2: "Safe operating area"</i> and <i>Figure 10: "Normalized on-resistance vs temperature"</i> . Minor text changes
01-Oct-2019	3	Updated marking on cover page. Updated <a href="#">Table 2. Thermal data</a> . Minor text changes

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