EZR32HG Errata

This document contains information on the EZR32HG errata. The latest available revision of this device is revision C.

Errata that have been resolved remain documented and can be referenced for previous revisions of this device.

The device data sheet explains how to identify the chip revision, either from package marking or electronically.

Errata effective date: March 2021.

1. Errata Summary

The table below lists all known errata for the EZR32HG and all unresolved errata in revision C of the EZR32HG.

Table 1.1. Errata Overview

Designator	Title/Problem	Workaround Exists	Exists on Revision:	
			B	C
ADC_E118	Requirements for ADC_CLK > 7 MHz	Yes	X	X
BOOT_E102	Bootloader Requires a Crystal	Yes	X	—
BOOT_E103	Documented Bootloader Pin Location	Yes	X	X
CMU_E115	HFRCO 1 MHz Band Switching	Yes	X	X
EMU_E107	Interrupts During EM2 Entry	Yes	X	X
EMU_E109	Potential Brown Out in EM2	Yes	X	—
EMU_E110	Potential Hard Fault when Exiting EM2 or EM3	Yes	X	—
EZR_E101	Latched RSSI Feature May Not Work Properly	Yes	X	X
EZR_E102	Increased Harmonics in TX Mode When Using a Direct Tie Match	Yes	X	X
EZR_E103	LDC Mode Duty Cycling May Stop After First Packet Reception	Yes	X	X
EZR_E104	Auto RX Frequency Hop May Stop Hopping	Yes	X	X
EZR_E105	TX to TX Transition Timing May Vary	Yes	X	X
EZR_E106	RX Lock-Up May Occur When DSA is Enabled	Yes	X	X
EZR_E107	Sync Word Detection Timeout for Non-Standard Preamble May Not Work	Yes	X	X
EZR_E108	Invalid Sync Word Hardware Interrupt Prematurely Fires When Antenna Diversity is Enabled	Yes	X	X
IDAC_E101	IDAC Output Current Degradation	Yes	X	X
PCNT_E102	PCNT Pulse Width Filtering Does Not Work	No	X	X
RMU_E102	Regulator Output May Be 0 V After Supply Falls to Intermediate Voltage and Recovers	Yes	X	—
RMU_E103	Reset May Fail to Trigger During Supply Voltage Brownouts	Yes	X	—
USART_E113	IrDA Modulation and Transmission of PRS Input Data	Yes	X	X
USB_E111	Using EM2 with System Running on USHFRCO	Yes	X	X
USB_E112	SUSPEND in LEMOSCCTRL	Yes	X	X

2. Current Errata Descriptions

2.1 ADC_E118 — Requirements for ADC_CLK > 7 MHz

Description of Errata
If operating the ADC_CLK at frequencies greater than 7 MHz, the ADC_BIASPROG register default value of 0x747 may not be sufficient to achieve the published missing codes performance specification.
Affected Conditions / Impacts
Devices operating the ADC_CLK at frequencies greater than 7 MHz while using the default ADC_BIASPROG value of 0x747 may experience performance outside data sheet limits.
Workaround
For systems requiring an ADC_CLK rate > 7 MHz, it may be necessary to increase the ADC's bias current components via the COMPBIAS, BIASPROG, and/or HALFBIAS bit fields in the ADC_BIASPROG register depending on a given application's ADC performance requirements.
Resolution
There is currently no resolution for this issue.

2.2 BOOT_E103 — Documented Bootloader Pin Location

Description of Errata
The revision 1.0 data sheet lists the bootloader pins (BOOT_TX and BOOT_RX) on PD6 (BOOT_TX) and PD7 (BOOT_RX). However, this is incorrect. The correct locations for these pins is PF0 (BOOT_TX) and PF1 (BOOT_RX).
Affected Conditions / Impacts
Systems attempting to use the bootloader by communicating on these pins will be unable to do so.
Workaround
If the hardware has been created for the incorrect pin locations, the bootloader can be updated to use these pins. The source code is in the example code zip file for *AN0042: USB/UART Bootloader* available at http://www.silabs.com/32bit-appnotes or in Simplicity Studio. If the hardware has not yet been created, use the correct pins when creating the hardware.
Resolution
This issue will be resolved in a future revision of the data sheet.

2.3 CMU_E115 — HFRCO 1 MHz Band Switching

Description of Errata
Switching to or from the 1 MHz band of the HFRCO or AUXHFRCO may cause a hard fault even at the maximum supported number of wait states.
Affected Conditions / Impacts
When the HFRCO or AUXHFRCO is selected as a clock source (e.g., the HFRCO has been selected as the HFCLK source) and the device is running with the maximum supported number of wait states, switching to or from the 1 MHz band can possibly cause a clock glitch that results in unexpected behavior or a hard fault.
Workaround
Before switching to or from the 1 MHz band when the HFRCO or AUXHFRCO is selected as the clock source, first switch to another stable clock source (such as the LFRCO). For example, when switching from the 21 MHz band to the 1 MHz band, the following procedure needs to be followed: 1. Select another stable clock source by writing to the HFCLKSEL field of the CMU_CMD register. 2. Wait until the clock source shows that it has been selected in the CMU_STATUS register, (e.g., CMU_STATUS_LFRCOSEL = 1). 3. Program the CMU_HFRCOCTRL register to select the 1 MHz band and tuning value. 4. Wait until the HFRCO has stabilized at the new frequency by waiting for the HFRCORDY bit in the CMU_STATUS register to change for 0 to 1. 5. Select the HFRCO as the clock source by writing to the HFCLKSEL field of the CMU_CMD register.
Resolution
There is currently no resolution for this issue.

2.4 EMU_E107 — Interrupts During EM2 Entry

Description of Errata
An interrupt from a peripheral running from the high frequency clock that is received during EM2 entry will cause the EMU to ignore the SLEEPDEEP flag.
Affected Conditions / Impacts
During EM2 entry, the high frequency clocks that are disabled during EM2 will run for some clock cycles after WFI is issued to allow safe shutdown of the peripherals. If an enabled interrupt is requested from one of these non-EM2 peripherals during this shutdown period, the attempt to enter EM2 will fail, and the device will enter EM1 instead. As a result, the pending interrupt will immediately wake the device to EM0.
Workaround
Before entering EM2, disable all high frequency peripheral interrupts in the core.
Resolution
There is currently no resolution for this issue.

2.5 EZR_E101 — Latched RSSI Feature May Not Work Properly

Description of Errata
The Latched RSSI may not be captured properly if the latching instant is based on Tbit/Tsample.
Affected Conditions / Impacts
The Latched RSSI may not be captured properly if the latching instant is based on Tbit/Tsample. In other words, when MODEM_RSSI_CONTROL: Latch = RX_STATE1-RX_STATE5, or MODEM_RSSI_CONTROL: AVERAGE = Sample1 the returned Latched RSSI may be invalid.
Workaround
Apply patch (Patch ID: 0x311A).
Resolution
Apply the patch (Patch ID: 0x311A) to resolve this problem.

2.6 EZR_E102 — Increased Harmonics in TX Mode When Using a Direct Tie Match

Description of Errata
In TX mode, harmonic content may be excessive due to incorrect LNA configuration when using a direct tie match. Increase of the 3rd harmonic can be as high as 20 dB.
Affected Conditions / Impacts
Increased harmonics levels in the TX spectrum. No impact when operating in RX state or when using a split TX / RX match or a match with an RF switch and single antenna. Both EZRadio and EZRadioPRO parts are affected.
Workaround
Apply patch (Patch ID: 0x311A).
Resolution
Apply the patch (Patch ID: 0x311A) to resolve this problem.

2.7 EZR_E103 — LDC Mode Duty Cycling May Stop After First Packet Reception

Description of Errata
When LDC (Low Duty Cycling) mode is enabled, the radio may stop receiving packets after the first successfully received packet.
Affected Conditions / Impacts
The chip may stop entering RX state autonomously. Only EZRadioPRO parts are affected.
Workaround
There are two workarounds available. 1. After reading the RX FIFO, enter Sleep state. 2. Apply patch (Patch ID: 0x311A).
Resolution
Apply the patch (Patch ID: 0x311A) to resolve this problem.

2.8 EZR_E104 — Auto RX Frequency Hop May Stop Hopping

Description of Errata
Without any signal present, the radio may stop hopping after a while and stay in receive mode at a seemingly random channel.
Affected Conditions / Impacts
Automatic frequency hopping may stop working. The device is still functional and will respond to subsequent commands from the host. Only EZRadioPRO parts are affected.
Workaround
Apply patch (Patch ID: 0x311A).
Resolution
Apply the patch (Patch ID: 0x311A) to resolve this problem.

2.9 EZR_E105 — TX to TX Transition Timing May Vary

Description of Errata
RevC2A chips support TX to TX state transitions, however, the amount of time it takes to do so may be inconsistent.
Affected Conditions / Impacts
TX to TX state transition time may vary. Both EZRadio and EZRadioPRO parts are affected. This does not affect the manual TX_HOP timing.
Workaround
Apply patch (Patch ID: 0x311A).
Resolution
Apply the patch (Patch ID: 0x311A) to resolve this problem.

2.10 EZR_E106 — RX Lock-Up May Occur When DSA is Enabled

Description of Errata
RevC2A chips have a new block, Digital Signal Arrival detector (DSA), which can be used to detect preamble in a very short period of time. The DSA is used for Preamble Sense Mode (PSM) amongst other features, where the chip duty cycles between RX Idle and RX state while searching for a preamble. When the DSA is enabled an RX lock-up may occur.
Affected Conditions / Impacts
RX lock-up may occur. The device is still functional and will respond to subsequent commands from the host. Only EZRadioPRO parts are affected.
Workaround
Apply patch (Patch ID: 0x311A).
Resolution
Apply the patch (Patch ID: 0x311A) to resolve this problem.

2.11 EZR_E107 — Sync Word Detection Timeout for Non-Standard Preamble May Not Work

Description of Errata
It is possible to configure the device for non-standard preamble (i.e. other than a 1010, or a 0101 pattern), in which case the sync word timeout is controlled by the packet handler. When this feature is enabled, the sync word detection timeout may not work correctly.
Affected Conditions / Impacts
Without a sync word timeout, the chip may continue searching for a sync word instead of going back to searching for non-standard preamble. No impact if standard preamble is used. Only EZRadioPRO parts are affected.
Workaround
Apply patch (Patch ID: 0x311A).
Resolution
Apply the patch (Patch ID: 0x311A) to resolve this problem.

2.12 EZR_E108 — Invalid Sync Word Hardware Interrupt Prematurely Fires When Antenna Diversity is Enabled

Description of Errata
If Invalid Sync Word hardware interrupt is enabled, it may fire right after PREAMBLE_VALID signal without receiving enough number of bits to determine whether or not there is a Sync Word pattern match.
Affected Conditions / Impacts
Invalid Sync Word detect NIRQ hardware interrupt cannot be used when Antenna Diversity is enabled. Only EZRadioPRO parts are affected.
Workaround
Disable Invalid Sync Word detect NIRQ hardware interrupt when Antenna Diversity is enabled.
Resolution
There is currently no resolution for this issue.

2.13 IDAC_E101 — IDAC Output Current Degradation

Description of Errata
The current output of the IDAC might degrade over time.
Affected Conditions / Impacts
Due to an undefined shut-down state of the IDAC, powered devices that do not use the IDAC continuously might experience some degradation in the current output over the lifetime of the device. The degradation is very small when the device is used at room temperature, but the output current will fall well outside specs if the device is exposed to higher temperatures for longer periods of time.
Workaround
If the IDAC output current stability is crucial to the application, the IDAC should never be completely disabled while the device is powered. Leaving the IDAC enabled in the lowest output code setting with duty-cycling enabled consumes ~50 nA extra current and eliminates the problem.
Resolution
There is currently no resolution for this issue.

2.14 PCNT_E102 — PCNT Pulse Width Filtering Does Not Work

Description of Errata
PCNT pulse width filtering does not work.
Affected Conditions / Impacts
The PCNT pulse width filter does not work as intended.
Workaround
Do not use the pulse width filter, i.e., ensure FILT = 0 in PCNTn_CTRL.
Resolution
There is currently no resolution for this issue.

2.15 USART_E113 — IrDA Modulation and Transmission of PRS Input Data

Description of Errata
If the USART IrDA modulator is configured to accept input from a PRS channel, the incoming data stream will not be transmitted because the required clock from the baud rate generator is never enabled.
Affected Conditions / Impacts
It is not possible for the USART IrDA modulator to directly transmit data from a source other than the USART's own transmitter. The USART_IRCTRL_IRPRSEN bit should remain at its reset state of 0.
Workaround
Assuming the data to be sent via the PRS is also data that could be received by the EFM32/EFR32 USART, then the data can be received using the USART's PRS RX feature (USART_INPUT_RXPRS = 1), stored in RAM (e.g., using DMA), and then transmitted with IrDA mode enabled. In cases where IrDA operation is transmit-only, the PRS RX data can be received on the same USART doing the transmission. If IrDA operation is bidirectional, then another USART must be used to receive the PRS data. If the data to be sent is in some other format (e.g., pulses from a timer output), then there is no direct way to transmit it using the IrDA modulator. It would be necessary to capture the data in some other way and reformat it as serial data timed according to the clock generated by the USART.
Resolution
There is currently no resolution for this issue.

2.16 USB_E111 — Using EM2 with System Running on USHFRCO

Description of Errata
Running the system on USHFRCO will not work with EM2 in USB applications.
Affected Conditions / Impacts
Entering EM2 when both the system clock (HFCLK) and the USB core clock (USBCCLK) are running on USHFRCO will result in a lock-up.
Workaround
Use either HFRCO or HFXO for the system clock (HFCLK) if EM2 is employed in USB applications. Alternatively, the EMVREG bit in EMU_CTRL can be set. This allows EM2 to be used at the cost of extra current consumption in EM2.
Resolution
There is currently no resolution for this issue.

2.17 USB_E112 — SUSPEND in LEMOSCCTRL

Description of Errata
Do not use the SUSPEND mode of LEMOSCCTRL in USB_CTRL.
Affected Conditions / Impacts
In rare cases with high data throughput, a transmission can fail when this mode is enabled.
Workaround
Use the GATED mode of LEMOSCCTRL for the best energy efficiency. The NONE mode can be used to disable energy savings.
Resolution
There is currently no resolution for this issue.

3. Resolved Errata Descriptions

This section contains previous errata for EZR32HG devices.

For errata on the latest revision, refer to the beginning of this document. The device data sheet explains how to identify chip revision, either from package marking or electronically.

3.1 BOOT_E102 — Bootloader Requires a Crystal

Description of Errata
Versions of the production bootloader prior to v2.06 require a crystal. All devices with the affected date codes use a version of the bootloader prior to v2.06 and will require a crystal to use the production bootloader. Version 2.06 of the bootloader will be updated to no longer require a crystal, since one is not needed on these products.
Affected Conditions / Impacts
Systems intending to use versions older than v2.06 of the production bootloader that do not include a crystal will not be able to run the bootloader on affected devices.
Workaround
For systems intending to use the production bootloader on affected devices, add a temporary crystal to the design that can later be removed when it's no longer needed.
Resolution
This issue has been resolved. Devices with a date code greater than or equal to 1801 will not have this issue.

3.2 EMU_E109 — Potential Brown Out in EM2

Description of Errata
There is an error with the calibration algorithm for a voltage regulator that is active during EM2 mode.
Affected Conditions / Impacts
There is an error with the calibration algorithm for a voltage regulator that is active during EM2 mode. This error can, in rare instances, cause the device to brown out and reset while operating in EM2 mode.
Workaround
The issue has been corrected with an updated and validated test program. Devices with a date code greater than or equal to 1618 have been tested with the corrected test program. Firmware can also work around this issue by writing the calibration value for the low current regulator active in EM2 to 0x6 after any reset or wakeup from EM4. More information on this firmware workaround including example code can be found at the following KB article URL: https://www.silabs.com/community/mcu/32-bit/knowledge-base.entry.html/2016/11/04/emu_e109_-_potential-gBa3
Resolution
The issue has been corrected with an updated and validated test program. Devices with a date code and PROD_REV greater than or equal to 1618 and 0x81 respectively have been tested with the corrected test program.

3.3 EMU_E110 — Potential Hard Fault when Exiting EM2 or EM3

Description of Errata
The flash is powered down in EM2 and EM3 to save power. Some control registers in the flash can rarely enter an invalid state upon power-on, causing the first read of flash to be incorrect. If this occurs after exiting EM2 or EM3, the core attempts to fetch the interrupt address, but the value will be incorrect and may be invalid. In the case of an invalid value, the core will then jump to the hard fault handler for attempting to execute code from an invalid address. All subsequent reads from the flash are unaffected, and it is only the first flash read after exit from EM2 or EM3 that is potentially erroneous.
Affected Conditions / Impacts
When exiting EM2 or EM3, some devices may intermittently execute code incorrectly or enter the hard fault handler instead of entering the expected ISR associated with the wake source.
Workaround
To workaround this issue, move the interrupt vector table and interrupt service routines for EM2 or EM3 wake sources to RAM and perform a dummy read of the flash in the ISR. Additional information on the workaround and examples provided is available from the following Knowledge Base article URL: https://www.silabs.com/community/mcu/32-bit/knowledge-base.entry.html/2017/05/09/emu_e110_-_potential-i2Pn
Resolution
This issue has been resolved. Devices with a date code greater than or equal to 1801 will not have this issue.

3.4 RMU_E102 — Regulator Output May Be 0 V After Supply Falls to Intermediate Voltage and Recovers

Description of Errata
Output of the on-chip regulator (DECOUPLE pin) may be approximately 0 V, and the device will not respond to a pin reset.
Affected Conditions / Impacts
The device supply voltage is specified as 1.98 V minimum. For certain supply waveforms, similar to disconnecting a battery, allowing the supply to decay to approximately 0.9 V (and stopping the decay at approximately 0.9 V), then reconnecting the battery, the output of the regulator (DECOUPLE pin) may be approximately 0 V. In this state, code will not execute, and the device will not respond to a pin reset. More information on this issue can be found at the following KB article URL: https://www.silabs.com/community/mcu/32-bit/knowledge-base.entry.html/2019/01/09/rmu_e102_por_bodres-AQh7
Workaround
Hold the RESETn pin logic low, starting before the supply is disconnected, and keep RESETn pin logic low until the supply reaches a valid voltage. If the DECOUPLE pin measures approximately 0 V, power cycle the supplies by pulling them all the way to 0 V before connecting supplies again.
Resolution
This issue is resolved in revision C devices.

3.5 RMU_E103 — Reset May Fail to Trigger During Supply Voltage Brownouts

Description of Errata
Reset may fail to trigger when the device supplies (AVDD_0, AVDD_2, VDD_DREG) fall to a voltage in the 1.25 - 1.45 V range.
Affected Conditions / Impacts
If the device supplies (AVDD_0, AVDD_2, VDD_DREG) fall to a voltage in the 1.25 - 1.45 V range, the device may fail to reset, allowing code execution while the supply voltage remains in the 1.25 - 1.45 V range. More information on this issue can be found at the following KB article URL: https://www.silabs.com/community/mcu/32-bit/knowledge-base.entry.html/2019/01/09/rmu_e103_por_bodres-N3MD
Workaround
Hold the RESETn pin in logic low, starting before the device supplies fall below 1.6 V, and keep the RESETn pin logic low until the device supplies reach a valid voltage again.
Resolution
This issue is resolved in revision C devices.

4. Revision History

Revision 1.6

March, 2021
- Added CMU_E115
- Migrated to new errata document format.

Revision 1.5

August, 2019
- Changed current device revision to revision C.
- BOOT_E102, EMU_E109, EMU_E110, RMU_E102 and RMU_E103 resolved and moved to .

Revision 1.40

January, 2019
- Added EMU_E107, RMU_E102, RMU_E103, and USART_E113.
- Resolved BOOT_E102 and EMU_E110.
- Resolution date code for BOOT_E102 and EMU_E110 changed from 1751 to 1801 to align with EFM32 Happy Gecko.
- EMU_E109 workaround URL updated.

Revision 1.31

January, 2017
- Updated BOOT_E102 and EMU_E110 resolution text.
- Updated revision history format.

Revision 1.30

October, 2017
- Updated EMU_E110 to refer to both EM2 and EM3.
- Added BOOT_E102 and BOOT_E103.

Revision 1.20

April, 2017
- Added EMU_E110.
- Updated errata formatting.
- Merged all errata documents for EZR32HG devices into one document.
- Merged errata history and errata into one document.

Revision 1.10

August, 2016
- Added EMU_E109.

Revision 1.00

April, 2016
- Initial preliminary release.

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