*Click **here** for production status of specific part numbers.*

MAX5996A/MAX5996B/ MAX5996C

IEEE 802.3bt-Compliant, Powered Device with Power Telemetry and Power/Current Limit

General Description

The MAX5996A/MAX5996B/MAX5996C provides a complete interface for a powered device (PD) to comply with the IEEE® 802.3af/at/bt standard in a Power-Over-Ethernet (PoE) system with a detection signature, classification signature, and an integrated power switch with startup inrush current control. During the startup period, the devices limit the current to 135mA and it switches to a higher current limit when the power MOSFET is fully enhanced. The devices feature a Multi-Event classification, Intelligent MPS, Autoclass, and an input UVLO with wide hysteresis and deglitch time to assure glitch-free transition during power-on/off. The devices can withstand a maximum voltage of 100V at the input.

The devices can detect the presence of a wall adapter power and allow a smooth switch-over from the PoE power source to the wall adapter. The devices also provide a power-good (PG) signal, two-step current limit, and foldback control, overtemperature protection.

The Intelligent Maintain Power Signature (IMPS) feature allows to automatically enable MPS current by detecting the port current. Autoclass feature is to enable advanced applications that allow the PSE to optimize power allocation to PD.

When working with dc-dc controller IC, the MAX5996C features a constant power/current limit when the port power/current consumption reaches PSE power/current limit. Multi-Event indication feature provides patterned signals to indicate power level allocated from PSE to PD in 7 different scenarios, and accurate real-time power telemetry reporting. LLDP pin of the MAX5996C allows to read power/current limit configuration from system microcontroller and overwrite power/current limit from classification process.

The MAX5996A/MAX5996B/MAX5996C are available in a 16-pin, 5mm x 5mm, TQFN power package. These devices are rated over the -40°C to 125°C temperature range.

Benefits and Features

- Accurate Power Telemetry (Patent Pending)
- Constant Power/Current Limit (Patent Pending)
- LLDP Power/Current Level Reading (Patent pending)
- IEEE802.3bt Compliant
- Built-in 90W Isolation Switch
- Multi-Classification
- Multi-Event Power Level Indication
- Simplified Wall Adapter Interface
- Inrush Current Limit During Startup
- Current Limit During Normal Operation
- Overtemperature Protection
- AutoClass
- Selectable Green MPS
- Intelligent MPS (Patent US9152161)
- 5mm x 5mm, 16-Pin TQFN

Applications

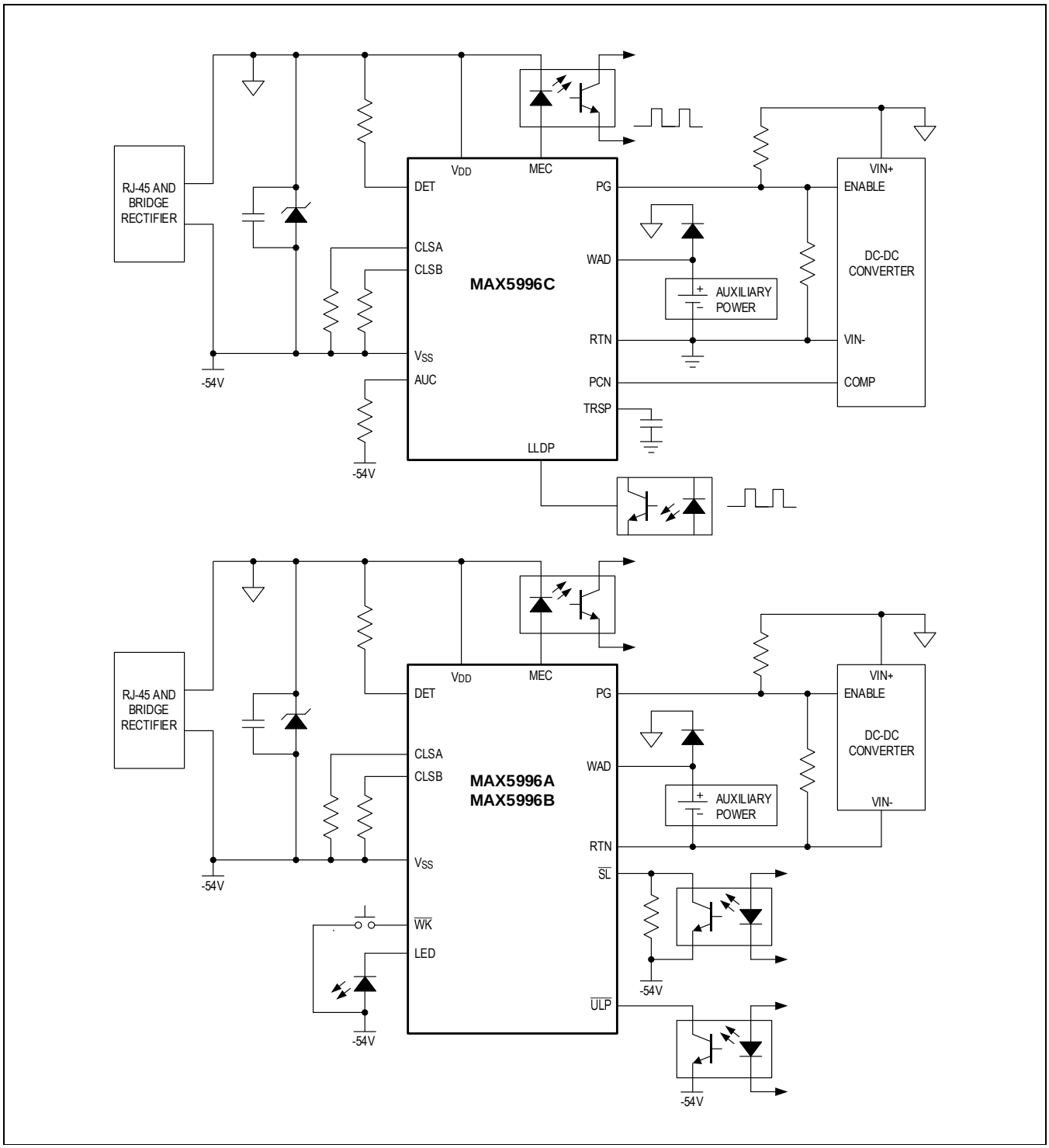
- IEEE 802.3bt Powered Devices
- VOIP Phones, IP Security Cameras
- Wireless Access Point
- Small Cell, Pico Cell
- Lighting
- Building Automation

***Ordering Information** appears at end of data sheet.*

19-101124; Rev 0; 9/21

maxim integrated™

Simplified Block Diagram



Absolute Maximum Ratings

V_{DD} to V_{SS} .....-0.3V to +100V

RTN, WAD, MEC, PG, DET to V_{SS} .....-0.3V to +100V

PCN to V_{SS} .....-0.3V to +100V

TRSP, LLDP, CLSA, CLSB, to V_{SS} .....-0.3V to +6V

Maximum Current on CLSA, CLSB (100ms Maximum) 100mA

Continuous Power Dissipation ((T_A = +70°C) (Note 1) (TQFN (derate 28.6mW/°C above +70°C)) (Multilayer Board) 2285.7mW

Operating Temperature Range .....-40°C to +125°C

Maximum Junction Temperature ..... +150°C

Storage Temperature Range .....-65°C to +150°C

Lead Temperature (soldering, 10s) ..... +300°C

Soldering Temperature (reflow)..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

16 TQFN-EP

Package Code	T1655+5
Outline Number	*21-100484*
Land Pattern Number	*90-100171*
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	35°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	2.7°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/ thermal-tutorial*.

Electrical Characteristics

(V_{IN} = (V_{DD} - V_{SS}) = 48V, R_{CLSA} = 619Ω, R_{CLSB} = 619Ω, RTN, WAD, PG, MEC, PCN, LLDP are unconnected, all voltages are referenced to V_{SS}, unless otherwise noted. T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25ºC. (Note 3))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DETECTION MODE						
Input Offset Current	I_{OFFSET}	V_{IN} = 1.4V up to 10.1V (Note 4)			10	µA
Effective Differential Input Resistance	D_R	V_{IN} = 1.4V up to 10.1V with 1V step, V_{DD} = RTN = WAD = PG = MEC (Note 5)	23.95	25	25.5	kΩ
CLASSIFICATION MODE						
Classification Disable Threshold	$V_{TH,CLS}$	V_{IN} rising (Note 6)	22	22.8	23.6	V
Classification Stability Time				0.2		ms
Classification Current	I_{CLASS}	V_{IN} = 12.5V to 20.5V, V_{DD} = RTN = WAD = PG, $R_{CLS_}$ = 619Ω	0		3.96	mA
		V_{IN} = 12.5V to 20.5V, V_{DD} = RTN = WAD = PG, R_{CLS} = 118Ω	9.12		11.88	
		V_{IN} = 12.5V to 20.5V, V_{DD} = RTN = WAD = PG, $R_{CLS_}$ = 66.5Ω	17.2		19.8	
		V_{IN} = 12.5V to 20.5V, V_{DD} = RTN = WAD = PG, $R_{CLS_}$ = 43.2Ω	26.3		29.7	
		V_{IN} = 12.5V to 20.5V, V_{DD} = RTN = WAD = PG, $R_{CLS_}$ = 30.9Ω	36.4		43.6	
Mark Event Threshold	V_{THM}	V_{IN} falling	10.1	10.7	11.6	V
Hysteresis on Mark Event Threshold				0.82		V
Mark Event Current	I_{MARK}	V_{IN} falling to enter mark event, 5.2V < V_{IN} < 10.1V	1.0		3.5	mA
Reset Event Threshold	V_{THR}	V_{IN} falling	2.8	3.8	5.2	V
POWER MODE						
V_{IN} Supply Voltage Range					60	V
V_{IN} Supply Current	I_Q	MOSFET is ON and No load		1.2	1.8	mA
V_{IN} Turn-On Voltage	V_{ON}	V_{IN} rising	34.3	35.4	36.6	V
V_{IN} Turn-Off Voltage	V_{OFF}	V_{IN} falling	30			V
V_{IN} Turn-On/-Off Hysteresis	V_{HYST_UVLO}	(Note 7)		4.2		V

(V_{IN} = (V_{DD} - V_{SS}) = 48V, R_{CLSA} = 619Ω, R_{CLSB} = 619Ω, RTN, WAD, PG, MEC, PCN, LLDP are unconnected, all voltages are referenced to V_{SS}, unless otherwise noted. T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25ºC. (Note 3))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Deglitch Time	T_{OFF_DLY}	V_{IN} falling from 40V to 20V (Note 8)		30	120		µs
Mode Delay	T_{DELAY}	From PG pulled low to high when entering into power mode, V_{IN} = 48V, C_{OUT} = 47µF		90	96	102	ms
Isolation Power MOSFET On-Resistance	R_{ON_ISO}	I_{RTN} = 950mA, T_J = +25°C			0.1	0.2	Ω
		I_{RTN} = 950mA, T_J = +85°C			0.15	0.25	Ω
		I_{RTN} = 950mA, T_J = +125°C			0.2		
RTN Leakage Current	I_{RTN_LKG}	V_{RTN} = 12.5V to 30V				10	µA
OVERCURRENT LIMIT							
Inrush Current Limit	I_{INRUSH}	During initial turn-on period, V_{RTN} - V_{VSS}= 1.5V		90	135	182	mA
Overcurrent Limit during Normal Operation	I_{MAX}	MAX5996C–1 to 5 Event Detected	After inrush completed, V_{RTN} = 1V (Note 9)	1800	2400	3000	mA
		MAX5996A/ MAX5996B–5 Event Detected	After inrush completed, V_{RTN} = 1V (Note 9)	1800	2400	3000	
		MAX5996A/ MAX5996B–1 to 4 Event Detected	After inrush completed, V_{RTN} = 1V (Note 9)	1600	1800	2250	
Overcurrent Limit in Foldback Condition	I_{MAX_FLDBK}	Both during inrush and after inrush completed V_{RTN} - V_{VSS} = 7.5V			45		mA
Foldback Threshold		V_{RTN} (Note 10)		6.5	7	7.5	V
WAD							
WAD Detection Threshold	$V_{WAD-REF}$	V_{WAD} rising, V_{IN} = 14V to 48V (referenced to RTN)		8	9	10	V
WAD Detection Threshold Hysteresis		V_{WAD} rising, V_{RTN} = 0V, V_{SS} unconnected			0.35		V
WAD Input Current	I_{WAD_LKG}	V_{WAD} = 10V (referenced to RTN)				3.5	µA
PG							
PG Sink Current	I_{PG}	V_{RTN} = 1.5V, V_{PG} = 0.8V, during inrush period		125	230	375	µA
PG Off-Leakage Current	I_{PG_LEAK}	V_{PG} = 60V				1	µA

(V_{IN} = (V_{DD} - V_{SS}) = 48V, R_{CLSA} = 619Ω, R_{CLSB} = 619Ω, RTN, WAD, PG, MEC, PCN, LLDP are unconnected, all voltages are referenced to V_{SS}, unless otherwise noted. T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25ºC. (Note 3))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MEC						
Pulse Width of START Bit for Class Indication				250		µs
Pulse Width of START Bit for Power Monitoring				900		µs
50% Pulse Width				500		µs
75% Pulse Width				750		µs
Repetitive Period				1000		µs
MEC Sink Current		V_{MEC} = 3.5V (referenced to RTN), V_{SS} disconnected	0.9	1.5	2.35	mA
MEC Off-Leakage Current		V_{MEC} = 48V			1	µA
MEC Power Limiting Alert Threshold				PMAX – 1.8		W
MEC Power Limiting Alert Hysteresis				1.8		W
MEC Current Limiting Alert Threshold				ILIM – 60		mA
MEC Current Limiting Alert Hysteresis				60		mA
MEC Power/Current Limiting Alert Time	T_{ALERT}	MEC to V_{SS}		2		ms
MEC Power/Current Limiting Alert Period	T_{ALRT_P}	MEC to V_{SS}		64		ms
SLEEP MODE/ULTRA-LOW-POWER SLEEP MODE (MAX5996A/MAX5996B)						
$\overline{WK}$ and $\overline{ULP}$ Logic Threshold	V_{TH}	$\overline{WK}$ falling and $\overline{ULP}$ rising and falling	1.5		3	V
$\overline{WK}$, $\overline{ULP}$ Voltage	V_{PUP}	$\overline{WK}$, $\overline{ULP}$ pins unconnected			5	V
$\overline{WK}$ Pullup Current	I_{PUP}	$V_{\overline{WK}}$ = 0V		2		mA
$\overline{ULP}$ Pullup Current	I_{PUP}	$V_{\overline{ULP}}$ =0V		500		µA
$\overline{SL}$ Logic Threshold		$\overline{SL}$ falling	0.75	0.8	0.85	V
$\overline{SL}$ Current		$R_{\overline{SL}}$ = 0Ω		140		µA
LED Current Amplitude	I_{LED}	$R_{\overline{SL}}$ = 60.4kΩ, V_{LED} = 3.5V (MAX5996A/MAX5996B)	10	10.5	11.5	mA
		$R_{\overline{SL}}$ = 30.1kΩ, V_{LED} = 3.75V	19.5	20.9	22.5	
		$R_{\overline{SL}}$ = 30.1kΩ, V_{LED} = 4V	19			
LED Current Programmable Range			10		20	mA

(V_{IN} = (V_{DD} - V_{SS}) = 48V, R_{CLSA} = 619Ω, R_{CLSB} = 619Ω, RTN, WAD, PG, MEC, PCN, LLDP are unconnected, all voltages are referenced to V_{SS}, unless otherwise noted. T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25ºC. (Note 3))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LED Current with Grounded $\overline{SL}$		$V_{\overline{SL}}$ = 0V	20.5	24.5	28.5	mA
LED Current Frequency	f_{ILED}	Sleep and Ultra-Low-Power sleep modes		250		Hz
LED Current Duty Cycle	D_{ILED}	Sleep and Ultra-Low-Power sleep modes		25		%
V_{DD} Current Amplitude	I_{VDD}	Normal sleep mode, V_{LED} = 3.5V	10	11	12.2	mA
Internal Current Duty Cycle	D_{IVDD}	Normal and Ultra-Low-Power sleep modes		75		%
Internal Current Enable Time	T_{ULP}	Ultra-Low-Power sleep mode	80	84	90	ms
Internal Current Disable Time	T_{ULP_DIS}	Ultra-Low-Power sleep mode	217	228	240	ms
$\overline{SL}$ Delay Time	$T_{\overline{SL}}$	Time $V_{\overline{SL}}$ must remain below the $\overline{SL}$ logic threshold to enter sleep and Ultra-Low-Power modes (MAX5996A)	5.4	6	6.6	s
AUTOCLASS (MAX5996C)						
AUTOCLASS Detection Time			76		87	ms
AUC (MAX5996C)						
AUC Pullup Current	I_{AUC_PUP}		8.5	9	9.5	µA
AUC Voltage Threshold	V_{AUC1}		0.47	0.5	0.53	V
			1.73	1.8	1.87	
			4.31	4.4	4.49	
MAINTAIN POWER SIGNATURE						
PoE MPS Current Rising Threshold	I_{MPS_RISE}			28.7		mA
PoE MPS Current Falling Threshold	I_{MPS_FALL}			24		mA
PoE MPS Current Threshold Hysteresis	I_{MPS_HYS}			4.3		mA
PoE MPS Time High	t_{MPS_HIGH}	AUC floating	80	84	90	ms
PoE MPS Time Low	t_{MPS_LOW}	AUC floating	217	228	240	ms
PoE MPS Time High	t_{MPS_HIGH}	AUC 332K 1% tolerance to V_{SS}	75	80	85	ms
PoE MPS Time Low	t_{MPS_LOW}	AUC 332K 1% tolerance to V_{SS}	218	232	246	ms
PoE MPS Time High	t_{MPS_HIGH}	AUC 121K 1% tolerance to V_{SS}	30	32	34	ms
PoE MPS Time Low	t_{MPS_LOW}	AUC 121K 1% tolerance to V_{SS}	268	280	292	ms
PoE MPS Time High	t_{MPS_HIGH}	AUC short to V_{SS}	14	16	18	ms
PoE MPS Time Low	t_{MPS_LOW}	AUC short to V_{SS}	280	296	308	ms

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold	T_{SD}	T_J rising		150		°C
Thermal-Shutdown Hysteresis	V_{CDLY_HYS}	T_J falling		30		°C
POWER LEVEL IDENTIFICATION						
Maximum Power Level	P_{MAX}	CLASS 0~3		12.65		W
		CLASS 4		24.96		
		CLASS 5		37.27		
		CLASS 6		49.57		
		CLASS 7		59.41		
		CLASS 8		69.26		
Current Threshold	I_{TH1}	EVENT 4	4.5	6.5	8.5	mA
	I_{TH2}	EVENT 5	21	23	25	
CURRENT LIMIT THRESHOLD (MAX5996C)						
Maximum Current Limit	I_{LIM}	CLASS 0~3		302		mA
		CLASS 4		591		
		CLASS 5		886		
		CLASS 6		1181		
		CLASS 7		1413		
		CLASS 8		1645		
POWER MONITORING (THROUGH MEC PIN)						
Power Report Offset				±0.5		W
Power Report Accuracy		12.65W ≤ P_{MAX} < 24.96W, V_{IN} = 8V	-5		+5	%
		24.96W ≤ P_{MAX} < 69.26W, V_{IN} = 48V	-3		+3	
ADC						
Resolution				8		bits
Power Reading Range	P_{MEC}	All classes		90		W
Power LSB Step Size	P_{LSB}			351.6		mW
POWER LIMIT LOOP (MAX5996C)						
Power Loop Response Time				20		ms
Power Limit Accuracy		12.65W ≤ P_{MAX} < 69.26W, V_{IN} = 48V	-3.5		+3.5	%
Current Limit Accuracy		302mA ≤ I_{LIM} < 1645mA, V_{IN} = 48V	-3.5		+3.5	%
TRSP Pin pullup current during Detecting Time	I_{TRSP}	V_{TRSP} = V_{VSS}		333		µA

(V_{IN} = (V_{DD} - V_{SS}) = 48V, R_{CLSA} = 619Ω, R_{CLSB} = 619Ω, RTN, WAD, PG, MEC, PCN, LLDP are unconnected, all voltages are referenced to V_{SS}, unless otherwise noted. T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25ºC. (Note 3))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TRSP Pin Detecting Time	T_{DETEC}	T_{RSP} CAP = 50nF		60		µs
TRSP Pin Source Current		I_{RTN} = 0A, CLASS 0~3, V_{TRSP} = 2V		10		µA
TRSP Pin Sink Current		I_{RTN} = 0.6A, CLASS 0~3, V_{TRSP} = 2V		10		µA
PCN Pin Sink Current		PCN = 1.8V to 4V, I_{RTN} = 0.6A, CLASS 0~3	500			µA
PCN Pin Leakage Current		PCN = 2, I_{RTN} = 0A, CLASS 0~3			10	µA
PCN Pin Leakage Current		T_A = -40°C to +125°C (Note 9) TRSP Float			10	µA
LLDP (MAX5996C)						
LLDP Logic Threshold	V_{TH_LLDP}	Falling and Rising	1.5		3	V
LLDP Pullup Current	I_{PUP_LLDP}	V_{LLDP} = 0V		500		µA
LLDP Input Pulse Period	T_{LLDP}			1		ms
LLDP Input Reference 50% Pulse Duration	T_{LLDP_1}	Note 10		500		µs
LLDP Input Reference 75% Pulse Duration	T_{LLDP_2}	Note 11		750		µs
LLDP Input Pulse Tolerance		Note 12	-20		+20	µs
Detection Watchdog Timeout	T_{DEC}			2		ms
LLDP DAC Resolution				8		bits
LLDP DAC Power Reading Range	P_{LLDP}	Power Mode		90		W
LLDP DAC Power LSB Step Size	P_{LSB}	Power Mode		351.6		mW
LLDP DAC Current Reading Range	I_{LLDP}	Current Mode		1.8		A
LLDP DAC Current LSB Step Size	I_{LSB}	Current Mode		7.03		mA
LLDP Minimum Power Limit Threshold Setting	P_{LIM_MIN}	Power Mode		10		W
LLDP Minimum Current Limit Threshold Setting	I_{LIM_MIN}	Current Mode		140		mA

Note 1: All devices are 100% production tested at T_A = +25°C. Limits over temperature are guaranteed by design.

Note 2: The input offset current is illustrated in the *Detailed Description*.

Note 3: Effective differential input resistance is defined as the differential resistance between V_{DD} and V_{SS}.

Note 4: The classification current is turned off whenever the device is in power mode.

Note 5: UVLO hysteresis is guaranteed by design, not production tested.

Note 6: 20V glitch on input voltage, which takes V_{DD} below V_{ON} shorter than or equal to t_{OFF_DLY} does not cause the MAX5996 to exit power-on mode.

Note 7: The maximum current limit during normal operation is guaranteed by design; not production tested.

Note 8: In power mode, current-limit foldback is used to reduce the power dissipation in the isolation MOSFET during an overload condition across V_{DD} and RTN.

Note 9: The specification is guaranteed by GBD data. In the production test it will be only tested at 25°C.

Note 10: 500µs LLDP pulse as bit “0” reference pulse for following data pulses.

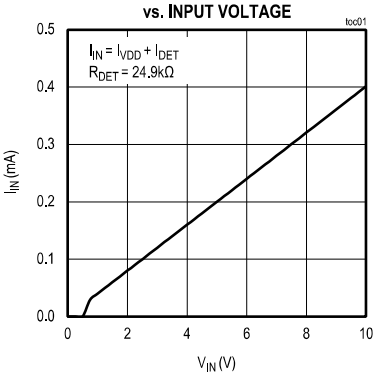
Note 11: 750µs LLDP pulse as bit “1” reference pulse for following data pulses.

Note 12: LLDP data pulse duration tolerances with respect to two 50% and 75% reference pulse durations.

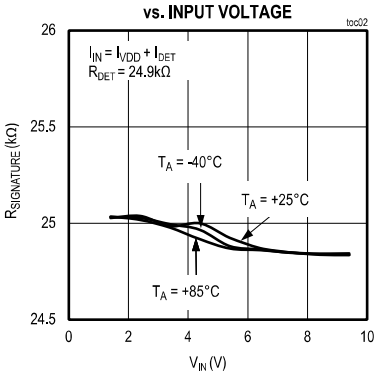
Typical Operating Characteristics

V_{IN} = V_{DD} - V_{SS} = +54V, R_{CLSA} = 30.9Ω, R_{CLSB} = 619Ω, R_{DET} = 24.9kΩ. AUC, WAD, MEC, and LLDP unconnected. All voltages are referenced to V_{SS}.

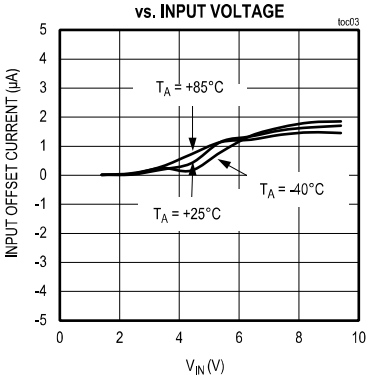
DETECTION CURRENT vs. INPUT VOLTAGE



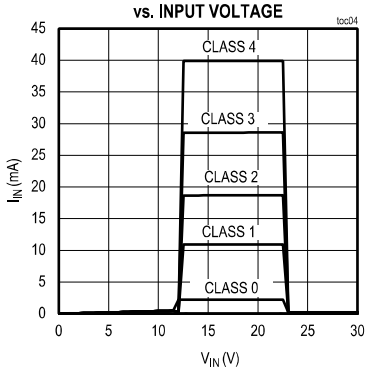
SIGNATURE RESISTANCE vs. INPUT VOLTAGE



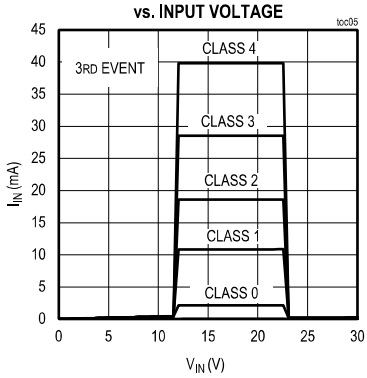
INPUT OFFSET CURRENT vs. INPUT VOLTAGE



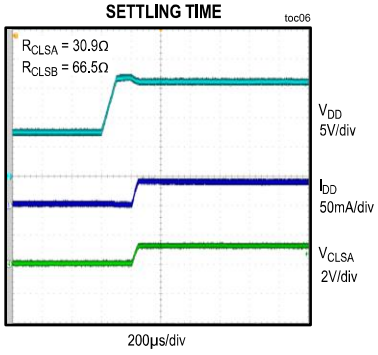
CLASSIFICATION CURRENT vs. INPUT VOLTAGE



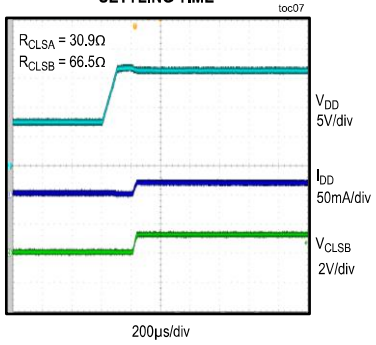
CLASSIFICATION CURRENT vs. INPUT VOLTAGE



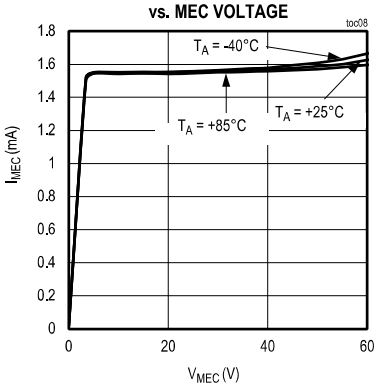
CLASSIFICATION SETTLING TIME



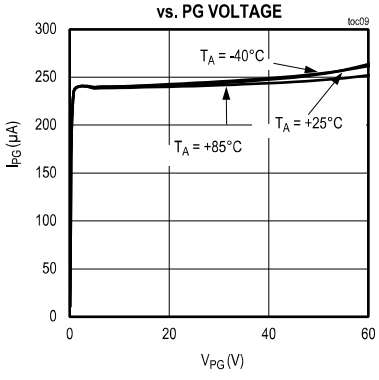
CLASSIFICATION SETTLING TIME



MEC SINK CURRENT vs. MEC VOLTAGE

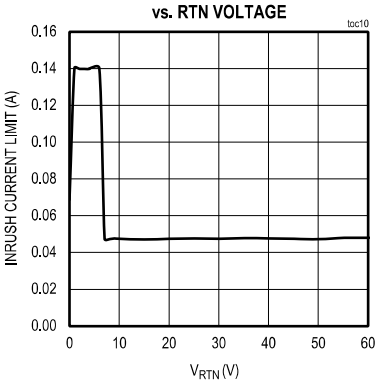


PG SINK CURRENT vs. PG VOLTAGE

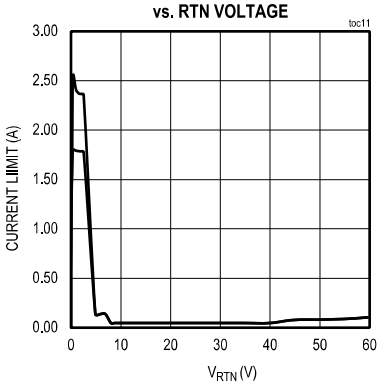


V_{IN} = V_{DD} - V_{SS} = +54V, R_{CLSA} = 30.9Ω, R_{CLSB} = 619Ω, R_{DET} = 24.9kΩ. AUC, WAD, MEC, and LLDP unconnected. All voltages are referenced to V_{SS}.

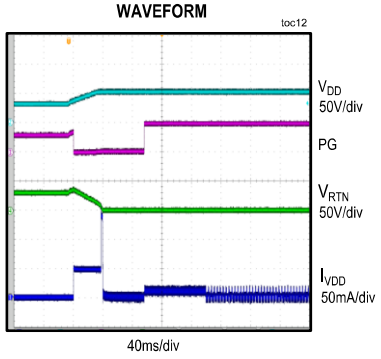
INRUSH CURRENT LIMIT vs. RTN VOLTAGE



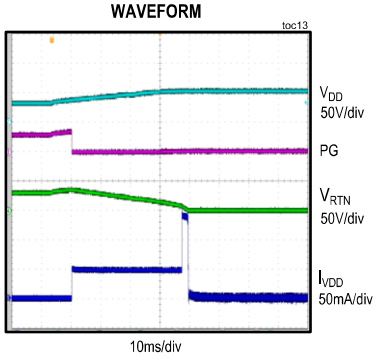
NORMAL OPERATION LIMIT vs. RTN VOLTAGE



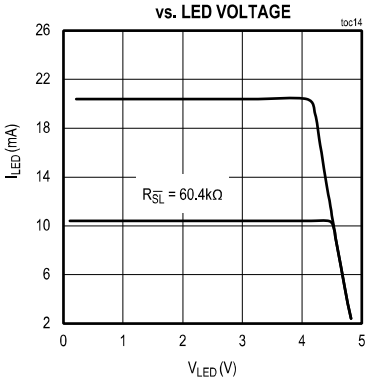
STARTUP INRUSH CONTROL WAVEFORM



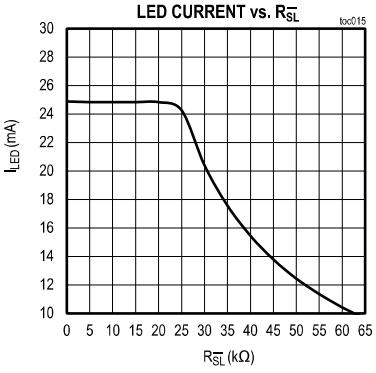
STARTUP INRUSH CONTROL WAVEFORM



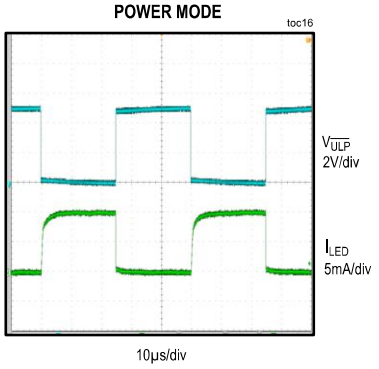
LED CURRENT vs. LED VOLTAGE



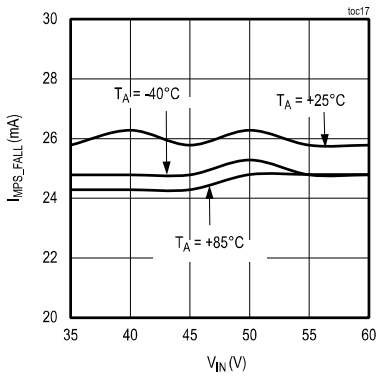
LED CURRENT vs. $R_{\overline{SL}}$



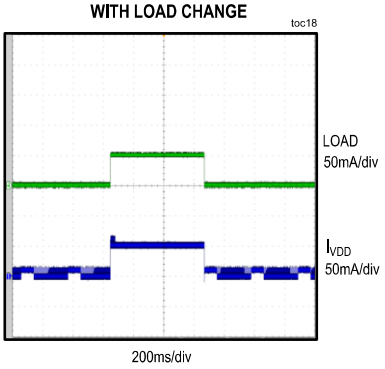
DRIVING LED WITH $\overline{ULP}$ IN POWER MODE



MPS CURRENT FALLING THRESHOLD vs. INPUT VOLTAGE

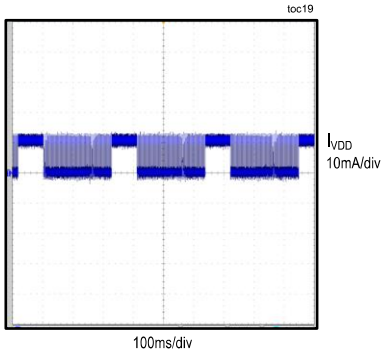


MPS CURRENT WAVEFORM WITH LOAD CHANGE

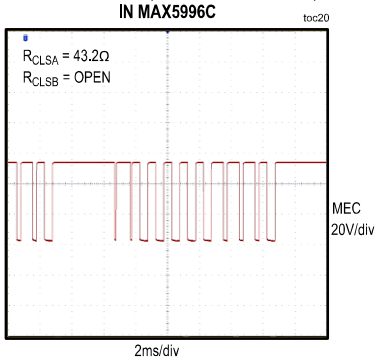


V_{IN} = V_{DD} - V_{SS} = +54V, R_{CLSA} = 30.9Ω, R_{CLSB} = 619Ω, R_{DET} = 24.9kΩ. AUC, WAD, MEC, and LLDP unconnected. All voltages are referenced to V_{SS}.

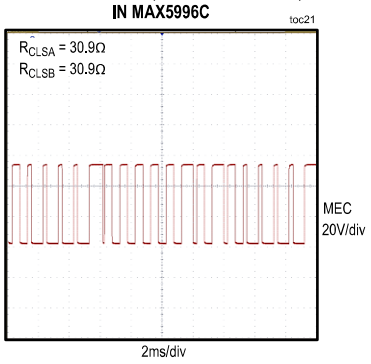
MPS CURRENT WAVEFORM



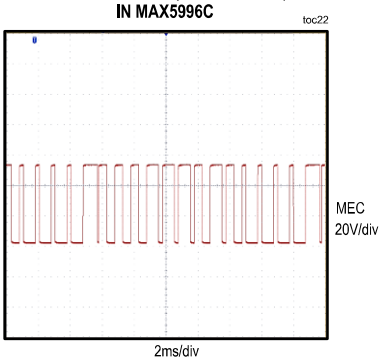
MEC WAVEFORM (CLASS 0~3, NO LOAD) IN MAX5996C



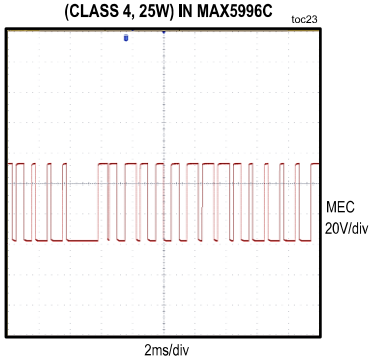
MEC WAVEFORM (CLASS 4, NO LOAD) IN MAX5996C



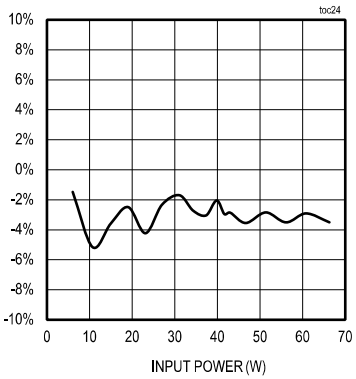
MEC WAVEFORM (CLASS 4, 10W) IN MAX5996C



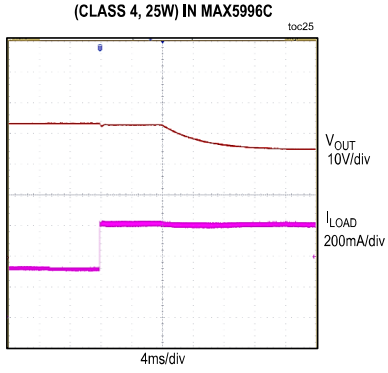
MEC WAVEFORM WITH POWER LIMIT ALERT (CLASS 4, 25W) IN MAX5996C



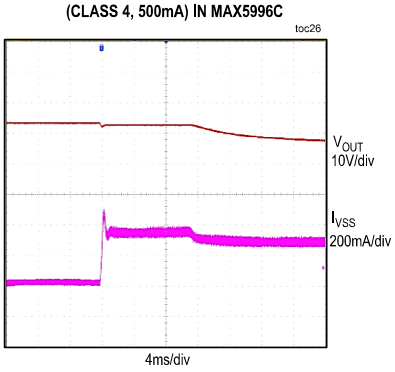
MEC POWER TELEMETRY REPORT ACCURACY



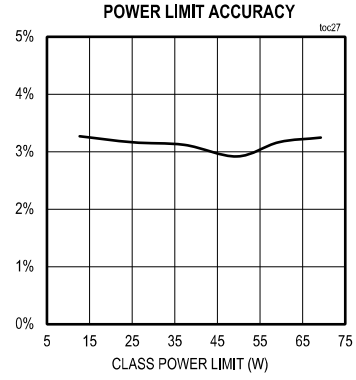
POWER LIMIT RESPONSE with DC-DC CONVERTER (CLASS 4, 25W) IN MAX5996C



CURRENT LIMIT RESPONSE with DC-DC CONVERTER (CLASS 4, 500mA) IN MAX5996C

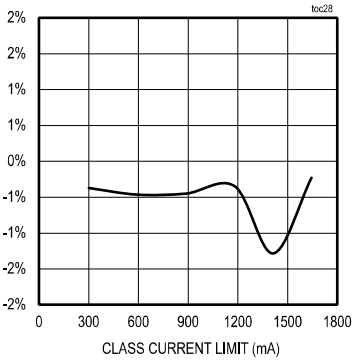


POWER LIMIT ACCURACY

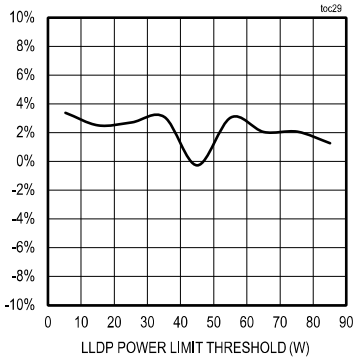


V_{IN} = V_{DD} - V_{SS} = +54V, R_{CLSA} = 30.9Ω, R_{CLSB} = 619Ω, R_{DET} = 24.9kΩ. AUC, WAD, MEC, and LLDP unconnected. All voltages are referenced to V_{SS}.

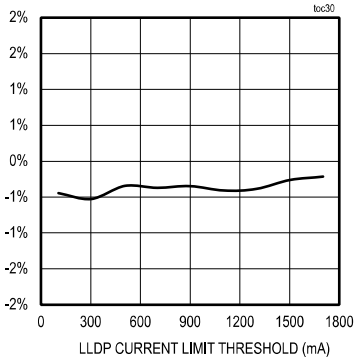
CURRENT LIMIT ACCURACY



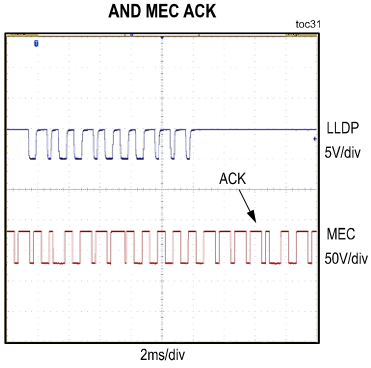
LLDP POWER LIMIT ACCURACY



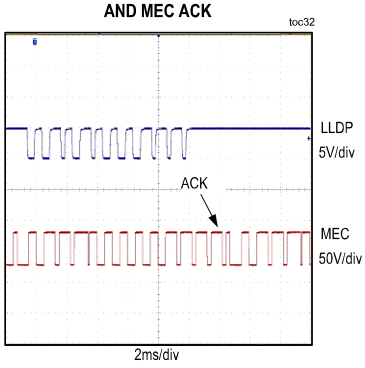
LLDP CURRENT LIMIT ACCURACY



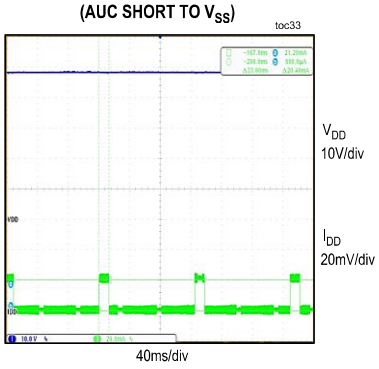
LLDP POWER MODE INPUT (25W) AND MEC ACK



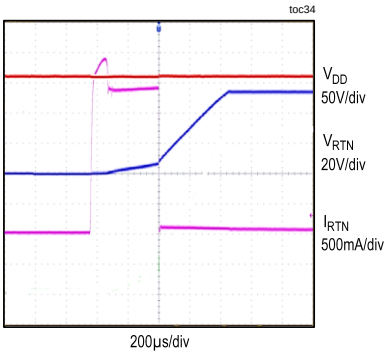
LLDP LIMIT MODE INPUT (500mA) AND MEC ACK



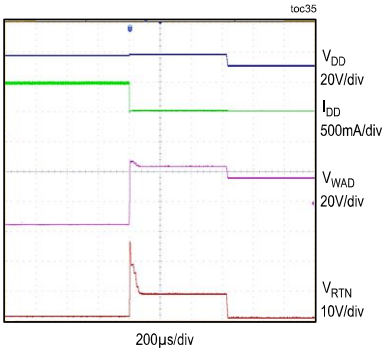
MPS CURRENT (AUC SHORT TO V_{SS})



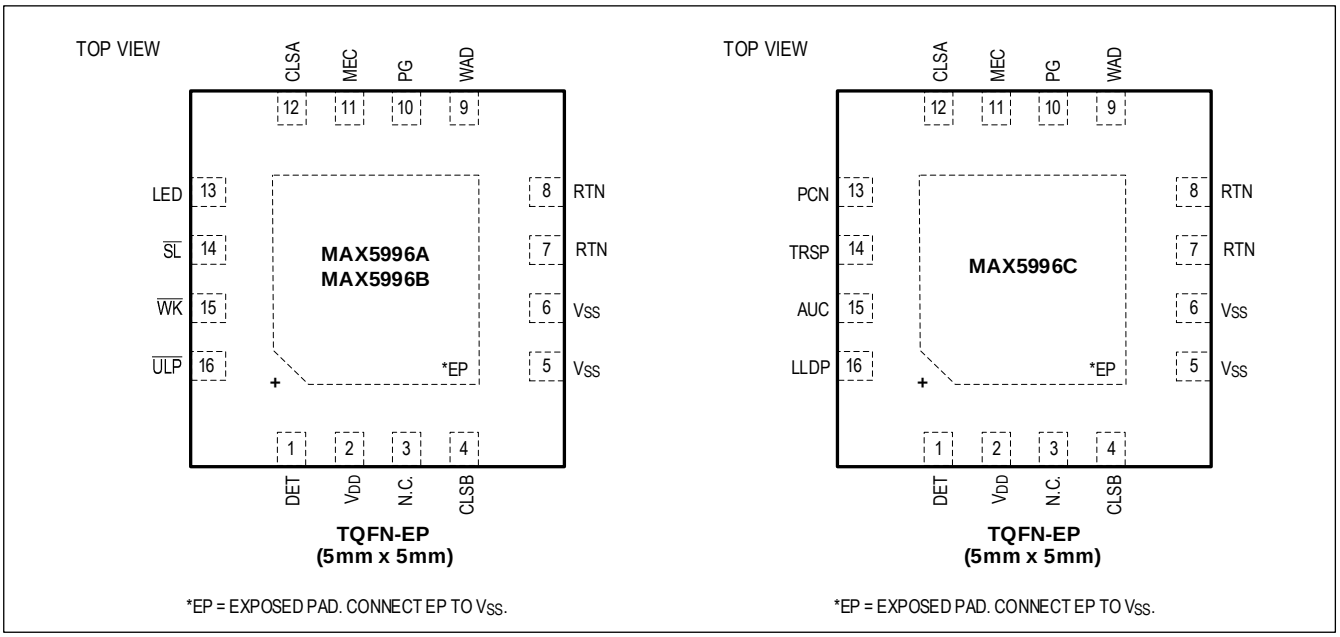
OVERLOAD CURRENT LIMIT



48V WALL ADAPTER PLUG IN



Pin Configurations



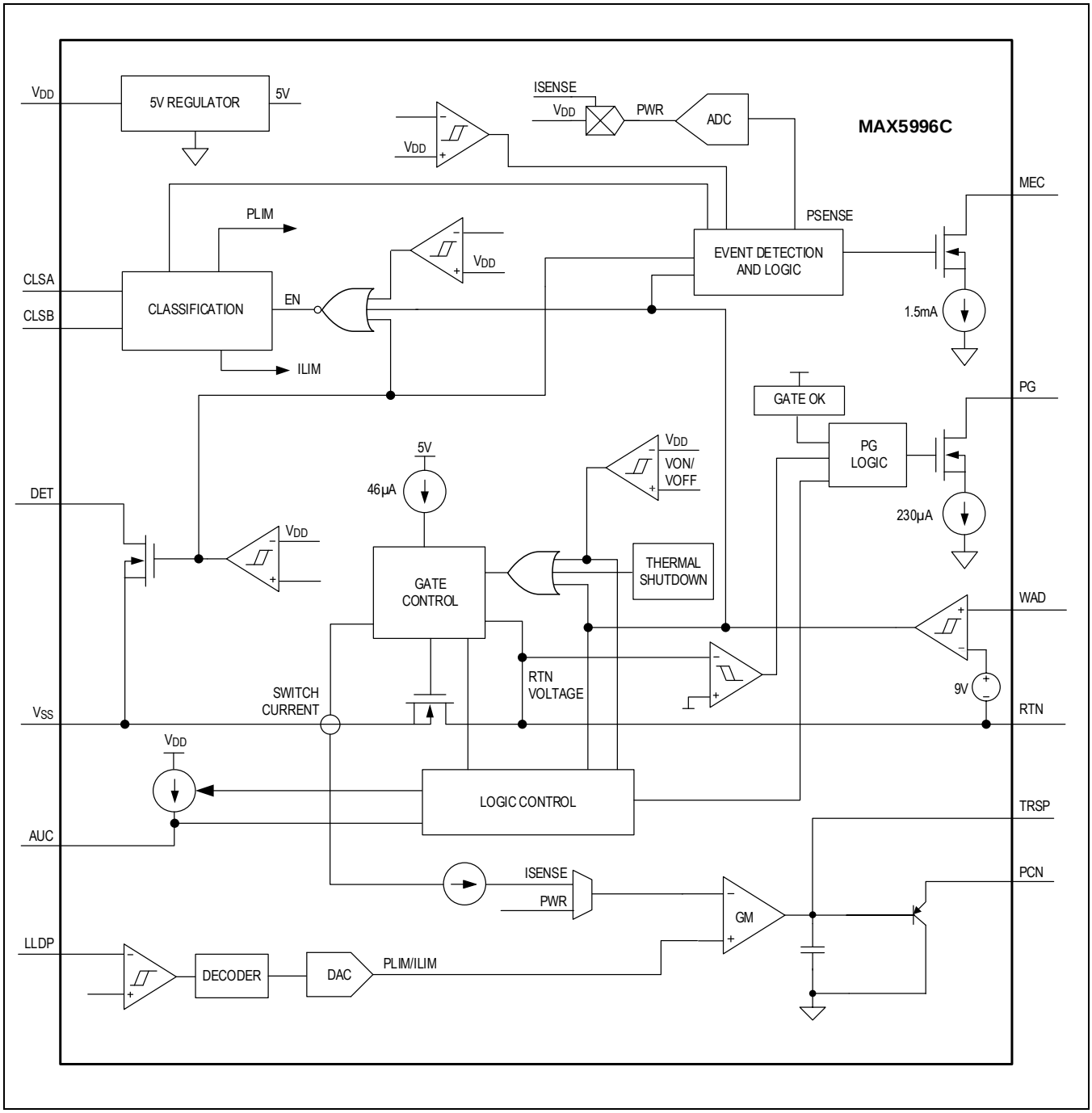
Pin Descriptions

PIN		NAME	FUNCTION
MAX5996A/ MAX5996B	MAX5996C		
1	1	DET	Detection Resistor Input. Connect a signature resistor (R_{DET} = 24.9kΩ) from DET to V_{DD}.
2	2	V_{DD}	Positive Supply Input. Connect minimum 68nF bypass capacitor between V_{DD} and V_{SS}.
3	3	N.C.	No Connection. Not internally connected.
4	4	CLSB	Classification Resistor Input. Connect a resistor (R_{CLS}) from CLSB to V_{SS} to set classification current for 3bt Standard. See the classification of current specifications in the *Electrical Characteristics* table to find the resistor value for a particular PD classification.
5,6	5,6	V_{SS}	Negative Supply Input. V_{SS} connects to the source of the integrated isolation n-channel power MOSFET.
7,8	7,8	RTN	The Drain of Isolation MOSFET. RTN connects to the drain of the integrated isolation n-channel power MOSFET. Connect RTN to the downstream DC-DC converter ground, as shown in the *Typical Application Circuits*.
9	9	WAD	Wall Power Adapter Detector Input. Wall adapter detection is enabled the moment V_{DD} - V_{SS} crosses the mark event threshold. Detection occurs when the voltage from WAD to RTN is greater than 9V. When a wall power adapter is present, the isolation n-channel power MOSFET turns off. Connect WAD directly to RTN when the wall power adapter or other auxiliary power source is not used.
10	10	PG	Open-Drain, Power-Good Indicator Output. PG sinks 230µA to disable the downstream DC-DC converter while turning on the MOSFET switch. PG current sink is disabled during detection, classification, and in the steady-state power mode. The PG current sink is turned on to disable the downstream DC-DC converter when the device is in sleep mode or Ultra-Low-Power sleep mode.

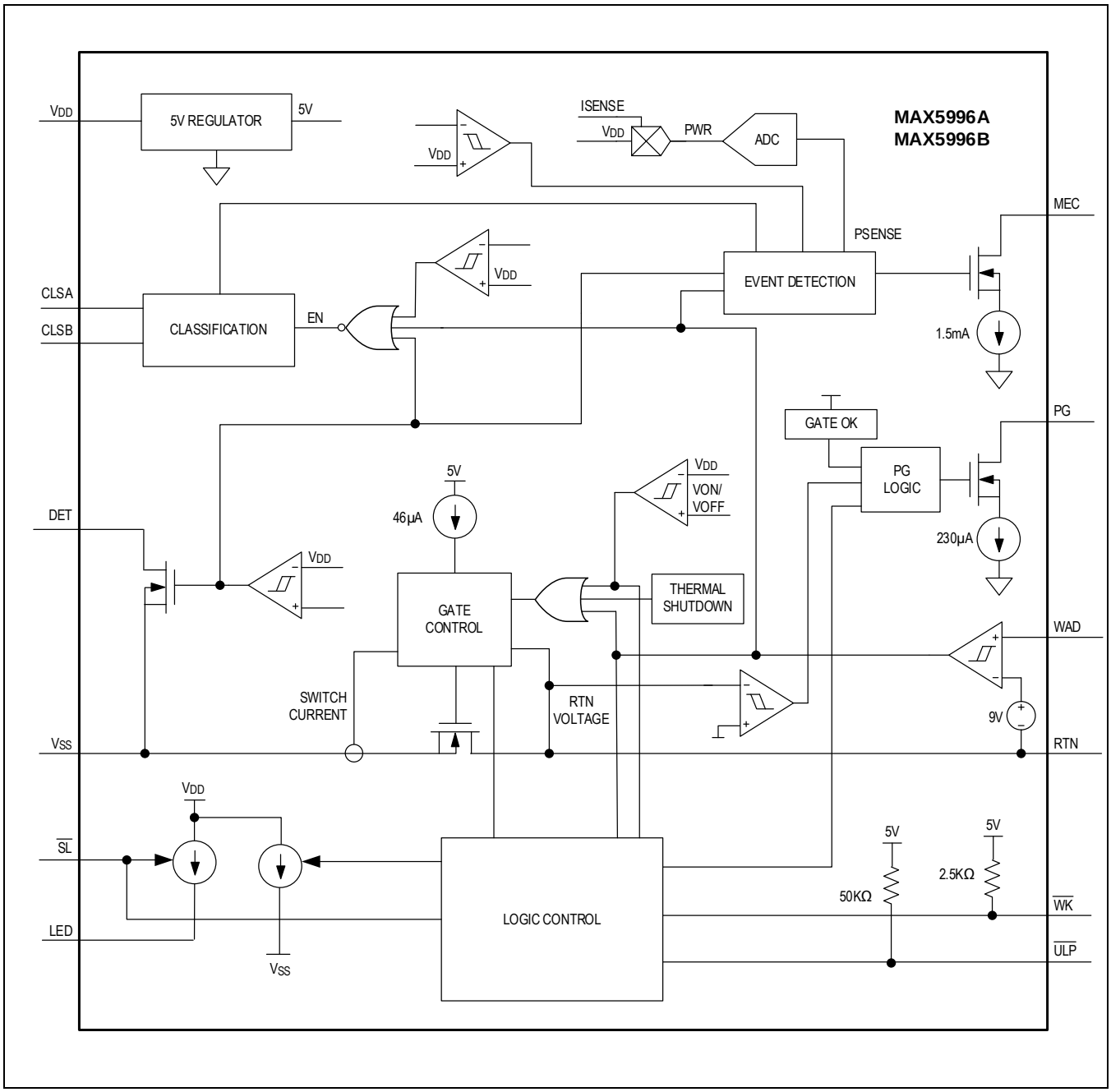
11	11	MEC	Multi-Event Classification, Power Telemetry Report or Wall Adapter Indication Output. This pin is an Open-drain output, and it generates duty cycle patterns to indicate power level allocated by PSE, and also to report real-time power consumption, and wall adapter presence. MEC is turned off when the device is in sleep mode and Ultra-Low-Power mode. MEC only generates pattern pulses after the MOSFET is fully turned on and PG asserts. MEC also sends out ACK pulse when the device detects a valid LLDP data frame. When enter power or current limiting mode, MEC is pulled low for 2ms and repeats every 64ms to "alert" the system.
12	12	CLSA	Classification Resistor Input. Connect a resistor (R_{CLS}) from CLSA to V_{SS} to set the classification current for 3at/af. See the classification of current specifications in the *Electrical Characteristics* table to find the resistor value for a particular PD classification.
13	—	LED	LED Driver Output. During sleep mode/Ultra-Low-Power sleep mode (MAX5996A/B). The LED sources a periodic current pulse at 250Hz with a 25% duty cycle and the current amplitude is set by the resistor connected from SL to V_{SS}.
—	13	PCN	Power/Current Control Output pin. Connect PCN pin to dc-dc controller IC COMP pin to sink current to limit converter output power/current when port power/current reaches the limit.
14	—	$\overline{SL}$	Sleep Mode Enable Input. In the MAX5996B, a falling edge on $\overline{SL}$ brings the device into sleep mode ($V_{\overline{SL}}$ must drop below 0.75V). In the MAX5996A, $V_{\overline{SL}}$ must remain below the threshold (0.75V) for a period of at least 6s after falling edge to bring the device into sleep mode. An external resistor ($R_{\overline{SL}}$) connected between $\overline{SL}$ and V_{SS} sets the LED current (I_{LED}) amplitude.
—	14	TRSP	Power/Current Control Loop Transconductance Amplifier Output. Connect a capacitor to RTN for setting power/current loop response time. Floating TRSP pin disables the Power Limiting function.
15	—	$\overline{WLK}$	Wake Mode Enable Input. $\overline{WK}$ has an internal 2.5kΩ pullup resistor to the internal 5V bias rail. A falling edge on $\overline{WK}$ brings the device out of sleep mode or Ultra-Low-Power sleep mode and resume normal operation.
—	15	AUC	Connect a resistor (no worse than 1% accuracy) between AUC and V_{SS} to program the duty cycle of MPS current to further reduce the power consumption in MPS mode. There are 4 settings: floating, 332kΩ,121kΩ, and short to V_{SS} for MPS current duty cycle and amplitude. Floating AUC or connecting to 332KΩ disables the Autoclass feature.
16	—	$\overline{ULP}$	Ultra-Low-Power Sleep Enable Input (in Sleep Mode). $\overline{ULP}$ has an internal 50kΩ pullup resistor to the internal 5V bias rail. A falling edge on $\overline{SL}$ in the MAX5996B (and a 6s period below the $\overline{SL}$ threshold in the MAX5996A), while $\overline{ULP}$ is asserted low enables Ultra-Low-Power sleep mode. When Ultra-Low-Power sleep mode is enabled, the power consumption of the device is reduced even lower than normal sleep mode to comply with Ultra-Low-Power sleep power requirements while still generating MPS current.
—	16	LLDP	LLDP pin is an input pin to recognize power limit level requests from system management micro-controller through a series of pulses. This power limit request overwrites the power/current limit identification from classification. Leave LLDP pin floating if not used. When LLDP is left floating the device is in power mode and when LLDP is shorted to V_{SS} or receiving "Current Limit" pulses the device is in the current mode.
—	—	EP	Exposed Pad. Do not use EP as an electrical connection to V_{SS}. EP is internally connected to V_{SS} through a resistive path and must be connected to V_{SS} externally. To optimize power dissipation, solder the exposed pad to a large copper power plane.

Functional Diagrams

MAX5996C Block Diagram



MAX5996A/MAX5996B Block Diagram



Detailed Description

Operation Mode

Depending on the input voltage (V_{IN} = V_{DD} - V_{SS}), the devices operate in four different modes: PD detection, PD classification, mark event, and PD power. The devices enter PD detection mode when the input voltage is between 1.4V and 10.1V. The device enters PD classification mode when the input voltage is between 12.5V and 20.5V. The devices enter PD power mode once the input voltage exceeds V_{ON}.

Detection Mode

In detection mode, the power source equipment (PSE) applies two voltages on V_{IN} in the 1.4V to 10.1V range (1V step minimum) and then records the current measurements at the two points. The PSE then computes ΔV/ΔI to ensure the presence of the 24.9kΩ signature resistor.

In detection mode, most of the device internal circuitry is off and the offset current is less than 10µA. If the voltage applied to the PD is reversed, install protection diodes at the input terminal to prevent internal damage to the devices (see the *Typical Application Circuits*). Since the PSE uses a slope technique (ΔV/ΔI) to calculate the signature resistance, the DC offset due to the protection diodes is subtracted and does not affect the detection process.

Classification Mode

In the classification mode, the PSE classifies the PD based on the power consumption required by the PD. This allows the PSE to efficiently manage power distribution. Two external resistors connected CLSA/CLSB to V_{SS} set classification signature to the PSE and define the power consumption requested from the PD. R_{CLSA} sets classification current for the 1st and 2nd class events for 0~4 class PD compliant with IEEE 802.3af/at standard, and R_{CLSB} sets classification current for the 3rd to 5th class event for 0~8 class PD compliant with IEEE 802.3bt standard.

The PSE classifies the PD by applying a voltage at the PD input and measuring the current sourced out of the PSE. When the PSE applies a voltage between 12.5V and 20.5V, the devices exhibit a series of events with current characteristics. *Table 1* shows the R_{CLSA} and R_{CLSB} resistor values needed to set for the PD class and the PD power consumption defined by standards. The PSE uses the number of class events and classification current information to classify the power requirement of the PD. The classification current includes the current drawn by R_{CLSA} and R_{CLSB} and the supply current of the devices, so the total current drawn by the PD is within the IEEE 802.3bt standard. The classification current is turned off whenever the device is in power mode.

Table 1. PSE Type and PD Class with Classification Resistor R_{CLSA} and R_{CLSB}

PD CLASS	POWER REQUESTED BY PD	RCLSA	RCLSB
0	12.95W	619	OPEN
1	3.84W	118	OPEN
2	6.49W	66.5	OPEN
3	12.95W	43.2	OPEN
4	25.5W	30.9	30.9
5	38.25W	30.9	619
6	51W	30.9	118
7	61W	30.9	66.5
8	71W	30.9	43.2

Multi-Event Classification and Detection

IEEE 802.3bt defines physical classification to allow a PD to communicate its power classification to the connected PSE and to allow the PSE to inform the PD of the PSE's available power. The PD classes (0~8) and PD power requests during Multi-Event Classification is configured by setting the R_{CLSA} and R_{CLSB} resistor values in *Table 1*. This configuration is compatible with IEEE 802.3af/at standard.

In a 1-Event classification, the PD is a 3af/at Class 0~3 PD. In a 2-Event classification, the PD is 3at Class 4 PD. In a 3-Event classification, the PD can be a 3bt PD at Class 0 to Class 4 depending on the classification current levels, and in this case, the PD can take as high as 30W power from a 3bt PSE. In a 4-Event classification, the PD can be 3bt Class 5 PD with 45W, or 3bt Class 6 PD with 60W input power from PSE. If the third and fourth event the classification current are 10mA/20mA, it means PD power requests gets demotion from PSE. In a 5-Event classification, the PD can be 3bt PD Class 7 with 75W, Or a 3bt PD Class 8 with 90W input power from PSE.

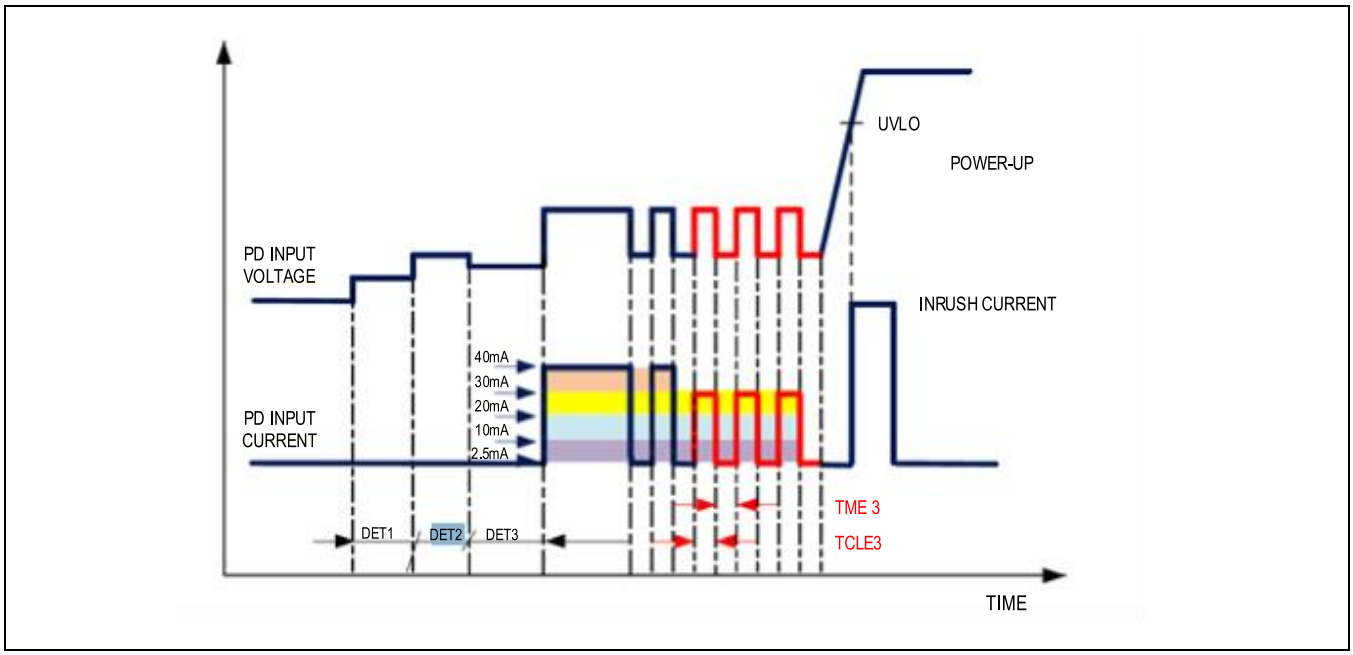


Figure 1. Multi-Event Classification

Power Mode

The MAX5996A/MAX5996B/MAX5996C devices enter power mode when V_{IN} rises above the undervoltage-lockout threshold (V_{ON}). When V_{IN} rises above V_{ON}, the devices turn on the internal n-channel isolation MOSFET to connect V_{SS} to RTN with inrush current limit internally set to 53mA (typ) when V_{RTN} - V_{SS} > 7V and 135mA (typ) when V_{RTN} - V_{SS} < 7V. The isolation MOSFET is fully turned on when the voltage at RTN is near V_{SS} and the inrush current is reduced below the inrush limit. Once the isolation MOSFET is fully turned on, the devices change to the normal operation current limit. The open-drain power good output (PG) remains low for a t_{DELAY} time (*Electrical Characteristics*) until the power MOSFET fully turns on to keep the downstream DC-DC converter disabled during inrush. Note that using larger output capacitors will result in longer start-up t_{DELAY} time.

Power Demotion

The power demotion feature is provided for the situation where the power level PD requested is not available at the PSE. When power demotion occurs, the PD must operate in a reduced power mode while connected to lower power PSE. In Power Demotion mode, the PSE is going to provide the power that its classification indicates. For example, a 3af PSE only issues a single event even there is a Class 4 PD connected.

This feature is applicable in 4P PoE as well. For example, when a Class 5/6 PD is connected to a PSE, the PSE only initiates a 3-Event. It indicated the PSE supports 4P operation but can only deliver power up to 30W. See *Table 1* for more details.

Multi-Event Indication (MEC)

The device communicates its available power level to the system user through the MEC pin. The MEC pin state is a result of the number of classification/mark events, and whether the PD is in PoE or auxiliary power operation. The MEC pin can indicate power allocated from PSE to PD in 5 different cases. The devices use a unique encoding method on the MEC pin to indicate the power levels that are higher than 12.95W. The first pulse sent from MEC is START bit (256µs, 25% duty) for the system to detect. Then the pattern of 2nd, 3rd, and 4th pulse width that is the double or triple pulse width of the START bit (50% and 75% duty) is issued to indicate the type of PSE and power allocated from PSE. This pulse train is repeatable at a certain frequency.

The number of events and the maximum power granted from the PSE at PD input are listed in *Table 2*. 1-Event and 2-Event are with IEEE802.3af/at standard. 3-Event, 4-Event, and 5-Event indicate PD Class (0~8) in IEEE802.3bt standard.

MEC is enabled after the isolation MOSFET is fully on until V_{IN} drops below the UVLO threshold. The MEC is turned off when the device is in sleep mode and Ultra-Low-Power mode.

Table 2. MEC Pattern with Number of Events and PD Class

CLASS	NUMBER OF EVENTS	MAXIMUM POWER GRANTED AT PD INPUT
0-3	1	12.95W
	Wall Adapter	
4	2 or 3	25.5W
5	4	if R_{CLSB} = 619Ω, 38.25W
6	4	if R_{CLSB} not = 619Ω, 51W
7	5	if R_{CLSB} = 66.5Ω; 61W
8	5	if R_{CLSB} not = 66.5Ω; 71W

The MEC pin also reports real-time power consumption as shown in *Figure 2*. The 90% pulse (900µs) is the start bit of power telemetry, and the 50% pulse (500µs) represents bit “0” and the 75% pulse (750µs) represents bit “1”. There are total 8-bit digitized pulses representing the power consumption at PD.

The last pulse in the MEC pulse series is the ACK pulse for the LLDP pin. The 75% duration pulse is ACK pulse, and the 50% duration pulse is NACK pulse. Once the LLDP pin detects valid LLDP data an ACK pulse is sent out from MEC to acknowledge the system MCU. If there are no LLDP input pulses or the LLDP input pulses are not valid, a NACK pulse will be sent out in MEC pulses.

When the device enters power or current limiting mode, MEC will be pulled low immediately for 2ms and repeat this 2ms “low” pulse every 64ms to “alert” system for power/current limiting mode until the device exits power or current limiting mode. The power report pulses will be interrupted by this 2ms “low” pulse intermittently in this case while the device continuously sends out power report pulses.

When there is an overload condition, and the device enters current limiting/foldback mode the MEC pin stops giving out data pulses and switches to high impedance. When the device exits the overload current limiting mode the MEC pin resumes pulse generating.

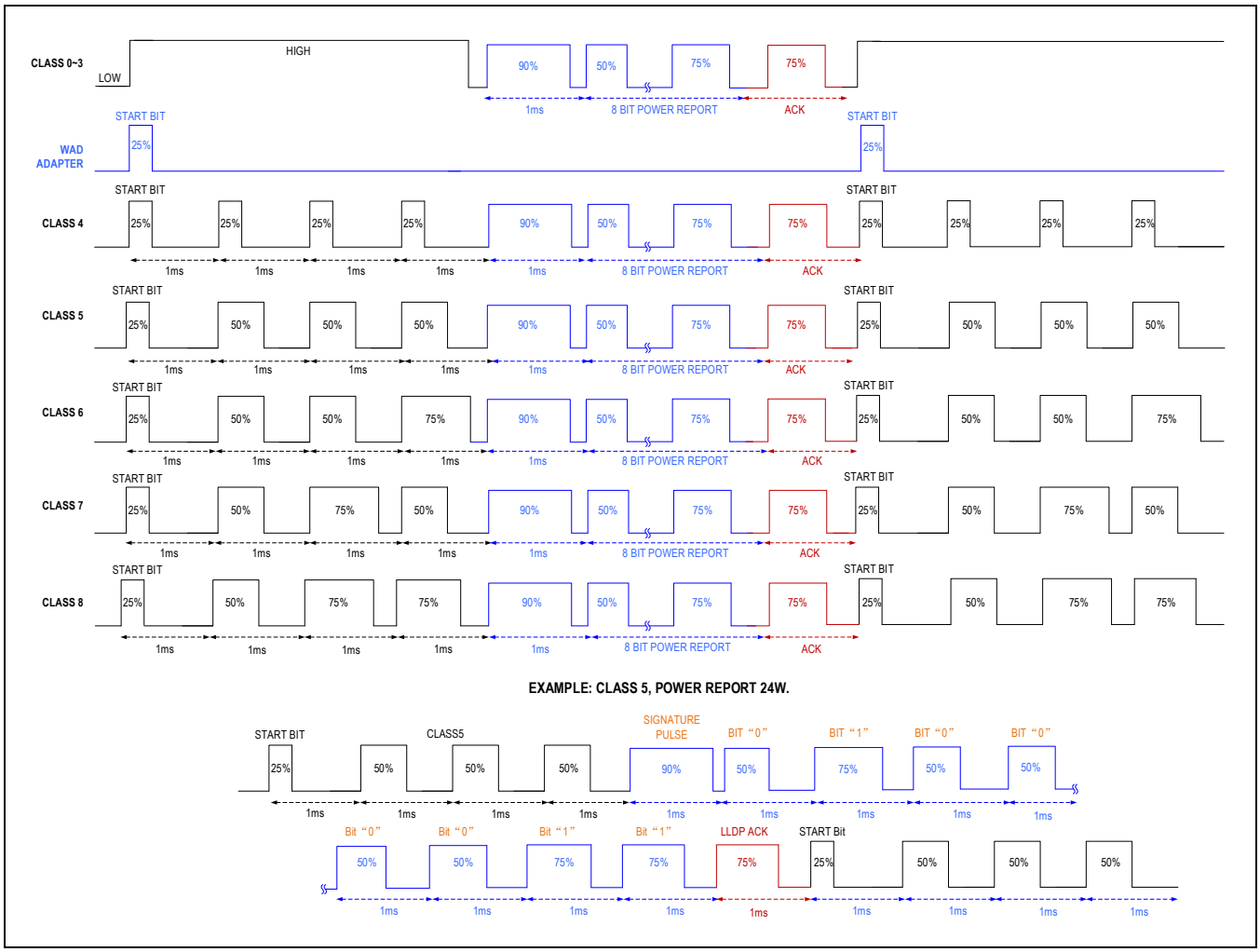


Figure 2. MEC Waveforms in Different Scenarios

Undervoltage Lockout

The MAX5996A/MAX5996B/MAX5996C devices operate up to a 60V supply voltage with a turn-on UVLO threshold (V_{ON}) at 35.4V and a turn-off UVLO threshold (V_{OFF}) at 30V. When the input voltage is above V_{ON}, the devices enter power mode and the internal MOSFET is turned on. When the input voltage goes below V_{OFF} for longer than t_{OFF_DLY}, the MOSFET turns off.

Intelligent MPS

The intelligent MPS feature is provided by the MAX5996B/MAX5996C. It enables applications that require low-power standby modes. The MPS current is generated to comply with the IEEE 802.3bt standard for PSE to maintain power on in standby modes. A minimum current (10mA) of the port is able to be maintained with MPS mode to avoid the power disconnection from the PSE. The devices automatically enter MPS mode when the port current is lower than 24mA (typ) and exit MPS mode when the port current is greater than 28.7mA (typ).

Figure 3 shows intelligent MPS behavior. The MPS comparator is an autozero comparator and it will sample the port current every 32µs. The MPS comparator is always switched on when the MOSFET is fully turned on. If the MPS comparator falling threshold is triggered continuously within 320µs, the part enters MPS mode and the MPS current is generated. Once the part enters MPS mode it waits for the TMPS timer to elapse before checking the MPS comparator again.

In MPS mode, the Intelligent MPS modulation scheme is shown in *Figure 3* (MPS Duty Cycle is 25% or 84ms), and the LED driver output (LED) sources periodic current pulses at 250Hz with 25% duty cycle and current amplitude can be configured by a resistor (R_{SL}) on SL pin. PG remains high to enable downstream dc-dc converter in MPS mode. Once MPS mode is entered, sleep mode or Ultra-Low-Power sleep mode will not take effect (MAX5996B).

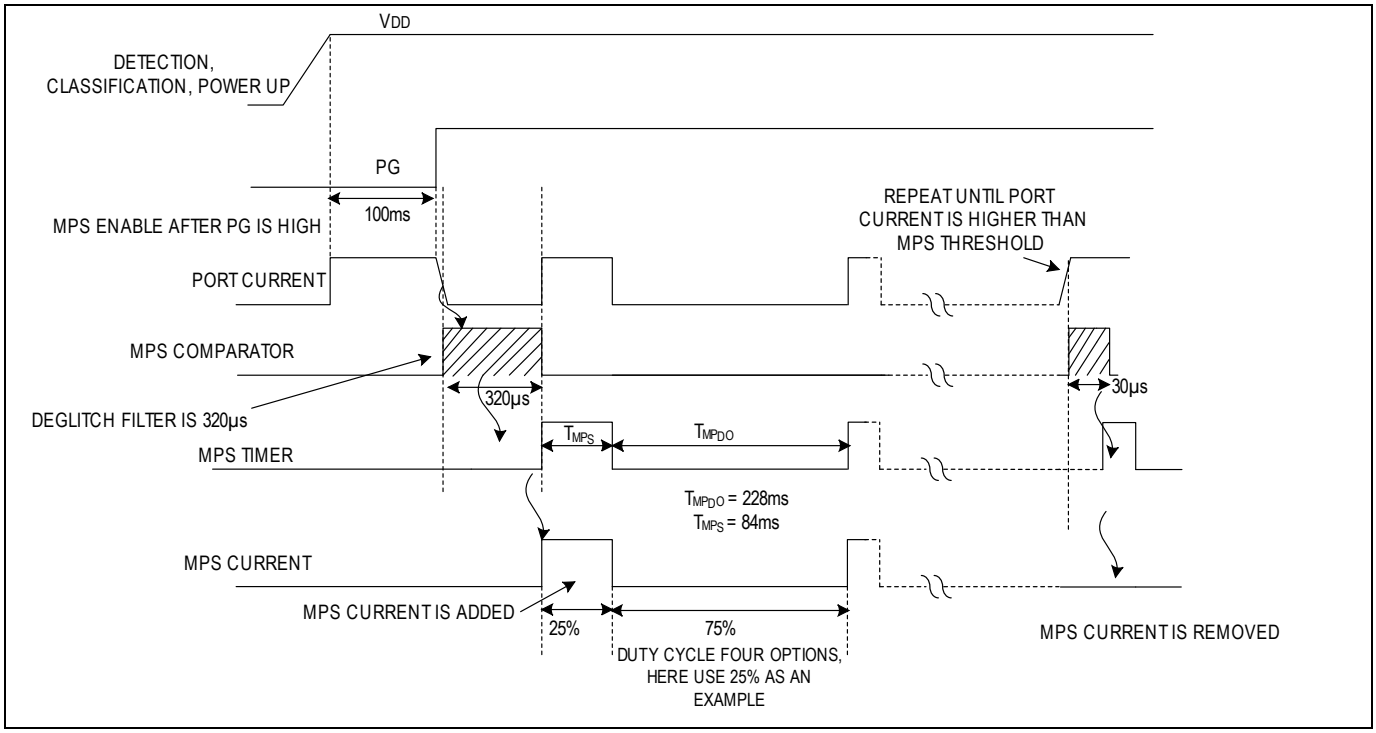


Figure 3. Intelligent MPS Behavior

Sleep and Ultra-Low-Power Sleep Modes (MAX5996A/MAX5996B)

The MAX5996A/MAX5996B features a sleep mode, which pulls PG low to disable downstream DC-DC converters to minimize the power consumption of the overall PD system, while at the same time still keeps the internal MOSFET turned on and generate an MPS current at V_{DD} to remain the PSE connection. However, when MAX5996B Intelligent MPS are enabled, and once the device enters MPS mode, sleep mode or Ultra-Low-Power sleep mode will not take effect. In sleep mode, the LED driver output (LED) sources a pulsating current and current amplitude can be configured by an external resistor ($R_{\overline{SL}}$) on an $\overline{SL}$ pin. To enable sleep mode, apply a falling edge to the $\overline{SL}$ pin (MAX5996B) or hold the $\overline{SL}$ pin low for a minimum of 6 seconds after a falling edge (MAX5996A).

An Ultra-Low-Power sleep mode allows the MAX5996A/MAX5996B to further reduce power consumption while still maintaining the pulsed MPS current required by the standard at V_{DD}. In Ultra-Low-Power sleep mode, the LED driver output (LED) sources periodic current pulses at 250Hz with 25% duty cycle, and current amplitude can be configured by a resistor ($R_{\overline{SL}}$) on $\overline{SL}$ pin; the Ultra-Low-Power sleep enable input $\overline{ULP}$ is internally held high with a 50kΩ pullup resistor to the internal 5V bias of the MAX5996A/MAX5996B. To enable Ultra-Low-Power sleep mode, set $\overline{ULP}$ pin to logic-low and apply a falling edge to $\overline{SL}$ (MAX5996B) or hold $\overline{SL}$ low for a minimum of 6s (MAX5996A).

Apply a falling edge on the wake-mode enable input ($\overline{WK}$) to disable sleep or Ultra-Low-Power sleep mode and resume normal operation. The PG pin is pulled low when the devices are in sleep mode or Ultra-Low-Power sleep mode and pulled high once enables $\overline{WK}$ to resumes normal operation.

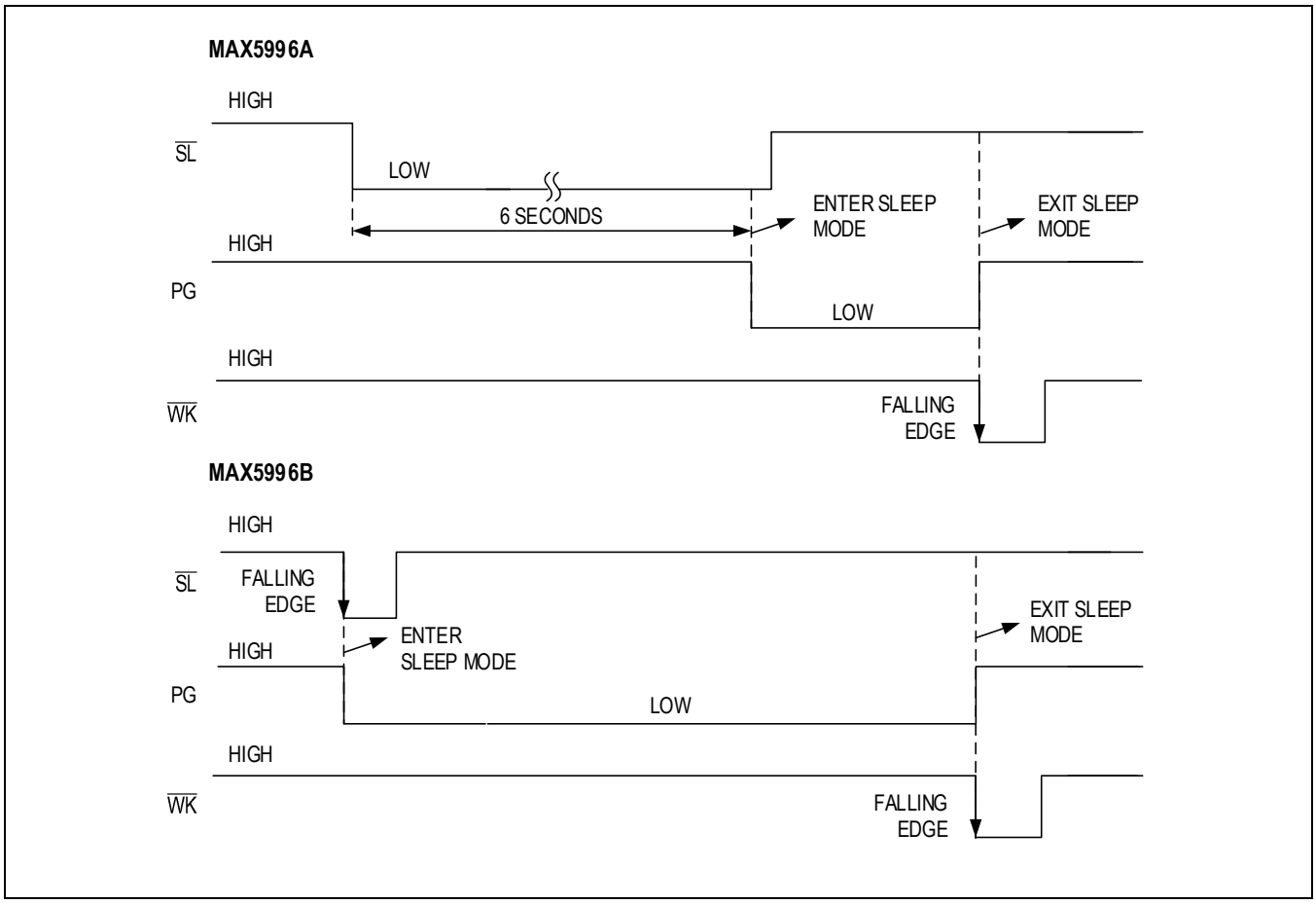


Figure 4. MAX5996A/MAX5996B Sleep Mode Behavior (Not in MPS Mode)

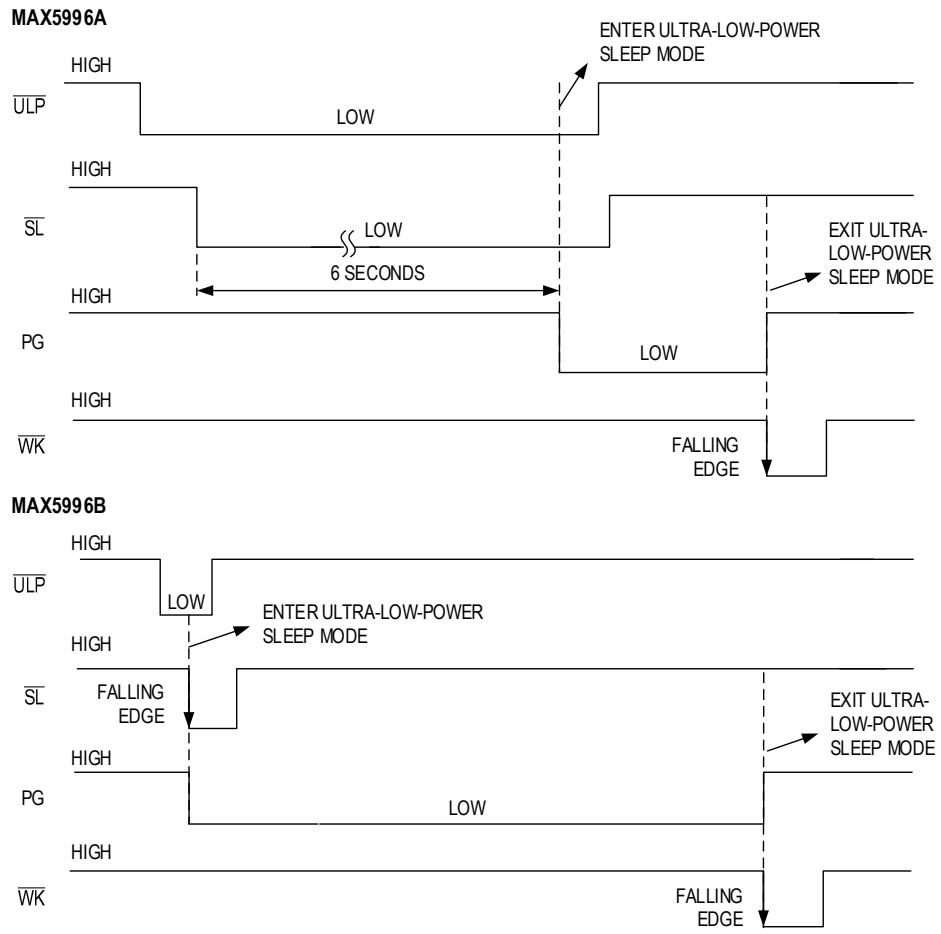


Figure 5. MAX5996A/MAX5996B Ultra-Low-Power Sleep Mode Behavior (Not in MPS Mode)

LED Driver (MAX5996A/MAX5996B)

The MAX5996A/MAX5996B drives an LED connected from the LED pin to V_{SS}. During sleep mode and Ultra-Low-Power sleep mode, the LED pin sources periodic current pulses at 250Hz with a 25% duty cycle. The current amplitudes in both cases can be programmed from 10mA to 20mA by the resistor connected from SL to V_{SS} according to the following formula.

$$I_{LED} = \frac{645.75}{R_{\overline{SL}} + 1200}$$

Power-Good Output

An open-drain output (PG) is used to allow disabling downstream DC-DC converter until the n-channel isolation MOSFET is fully turned on. PG is pulled low to V_{SS} for a period of t_{DELAY} and until the internal isolation, MOSFET is fully turned on. Using larger output capacitors will result in longer t_{DELAY} time. The PG is pulled low during sleep mode and Ultra-Low-Power sleep mode (in MAX5996A and MAX5996B, not in MPS mode). PG is also pulled low in an overtemperature event and pulled high once the device comes out of thermal shutdown and resumes normal operation.

AUTOCLASS (MAX5996C)

In AUTOCLASS mode, the PSE is allowed to determine the actual maximum power consumption from the connected PD. When AUTOCLASS mode is enabled, during the first-class event, the PD drops its current to class signature '0' no earlier than 76ms (min) and no later than 87ms (max). The AUTOCLASS feature is only in MAX5996C. Floating AUC pin or connecting 332kΩ disables AUTOCLASS mode, which means the PD does not drop the current during the first-class event If the PSE provides the Long First Event. Connecting a resistor (no worse than 1% accuracy) between AUC and V_{SS} enables AUTOCLASS mode. To program the duty cycle of MPS current to further reduce the power consumption in MPS mode. There are four settings: floating (> 25%), 332kΩ (25%), 121kΩ (10%), and short to V_{SS} (5%).

Table 3. AUC Configuration for MPS Current

AUC PIN CONFIGURATION	MPS DUTY CYCLE	MPS CURRENT AMPLITUDE	SUPPORT AUTOCLASS
AUC floating	> 25%	10mA	NO
Connect 332kΩ between AUC and V_{SS}	25%	20mA	NO
Connect 121kΩ between AUC and V_{SS}	10%	20mA	Yes
Short AUC to V_{SS}	5%	20mA	Yes

The device starts an 82ms timer on the first Classification Event. If the PSE does not provide the Long First Event, then the PD will not support AUTOCLASS and IMPS duty-cycle will be 25% pulses, as shown in *Figure 6*. If the PSE provides the Long First Event and AUC pin is not floated or connecting to 332kΩ, then the PD will truncate the classification current after 82ms to signature AUTOCLASS mode to the PSE, and the PD will modulate the IMPS duty-cycle current according to resistor values on AUC pin. IMPS modulation scheme is shown in *Figure 6*.

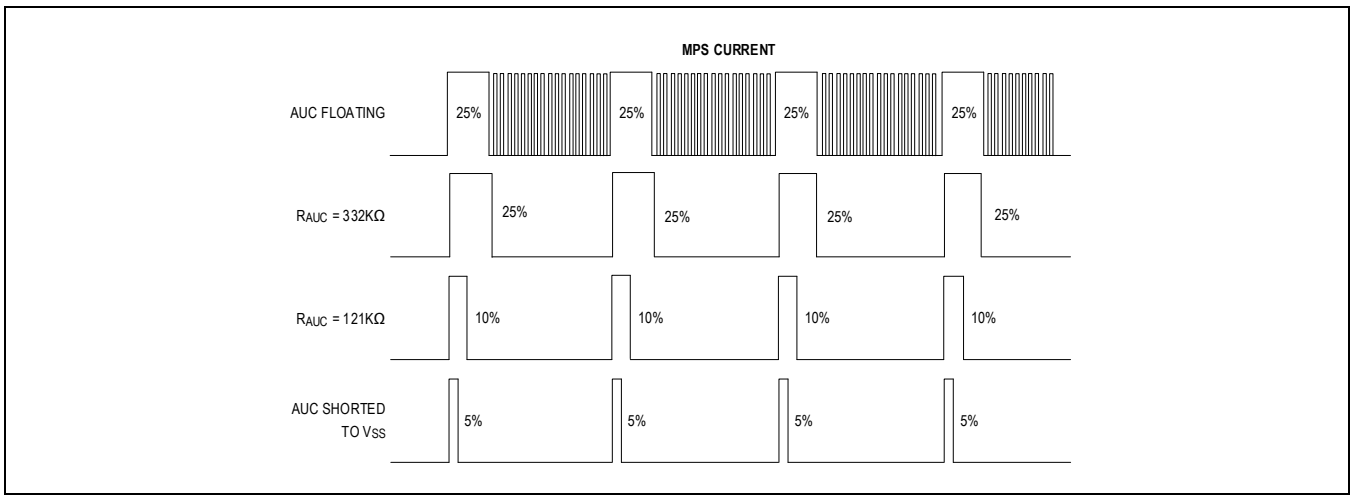


Figure 6. MPS Current with Different AUC Configuration

Thermal-Shutdown Protection

The MAX5996A/MAX5996B/MAX5996C devices include thermal protection from excessive heating. If the junction temperature exceeds the thermal-shutdown threshold of +150ºC, the devices turn off the internal power MOSFET, LED driver, and MEC current sink. When the junction temperature falls below +120ºC, the devices enter startup mode and then power mode. Startup mode ensures the downstream DC-DC converter is turned off by pulling PG low until the internal power MOSFET is fully turned on.

Wall Power Adapter Detection and Operation

The devices feature wall power adapter detection for applications where an auxiliary power source such as a wall power adapter is used to power the PD by connecting it to the WAD pin to RTN. Once the input voltage exceeds the mark event threshold, wall adapter detection is enabled. The devices give the priority to the wall adapter and smoothly switch the power supply to the wall adapter when the wall adapter is detected. These devices detect a wall power adapter when the voltage from WAD to RTN is greater than 9V. When a wall power adapter is detected, the internal isolation MOSFET turns off, MEC current sink turns on to indicate a certain pattern (see *Multi-Event Indication (MEC)* Section), the classification current is disabled if VIN is in the classification range, and the Intelligent MPS comparator is turned off.

Power Level Identification

The MAX5996 can identify power class levels by measuring the R_{CLSB} value and recognizing the number of the classification events. The power class level will be used to set the reference for the power/current control loop to implement power/current limiting when the power/current is reaching the limit. See *Table 2*.

Power Limiting (MAX5996C)

When the LLDP pin is floating or receiving Power Limit pulses the device works in power limit mode. Power limiting function is disabled during MOSFET power-up and enabled 1.2ms (typ) after the MOSFET is fully enhanced and stays enabled at normal operation. When the PD power reaches the limit the constant power loop starts to sink current from PCN pin and overdrive COMP pin of dc-dc controller IC (for example MAX5974 or MAX15158) to limit the output power of the converter. Once power limit control takes over, the loop will be dominated by a constant power loop.

Power limiting can be disabled by a floating TRSP pin.

When the PD current reaches the overload current limit (2.4A typical) the PD current limiting function takes control immediately to limit the current to protect the MOSFET from overheating.

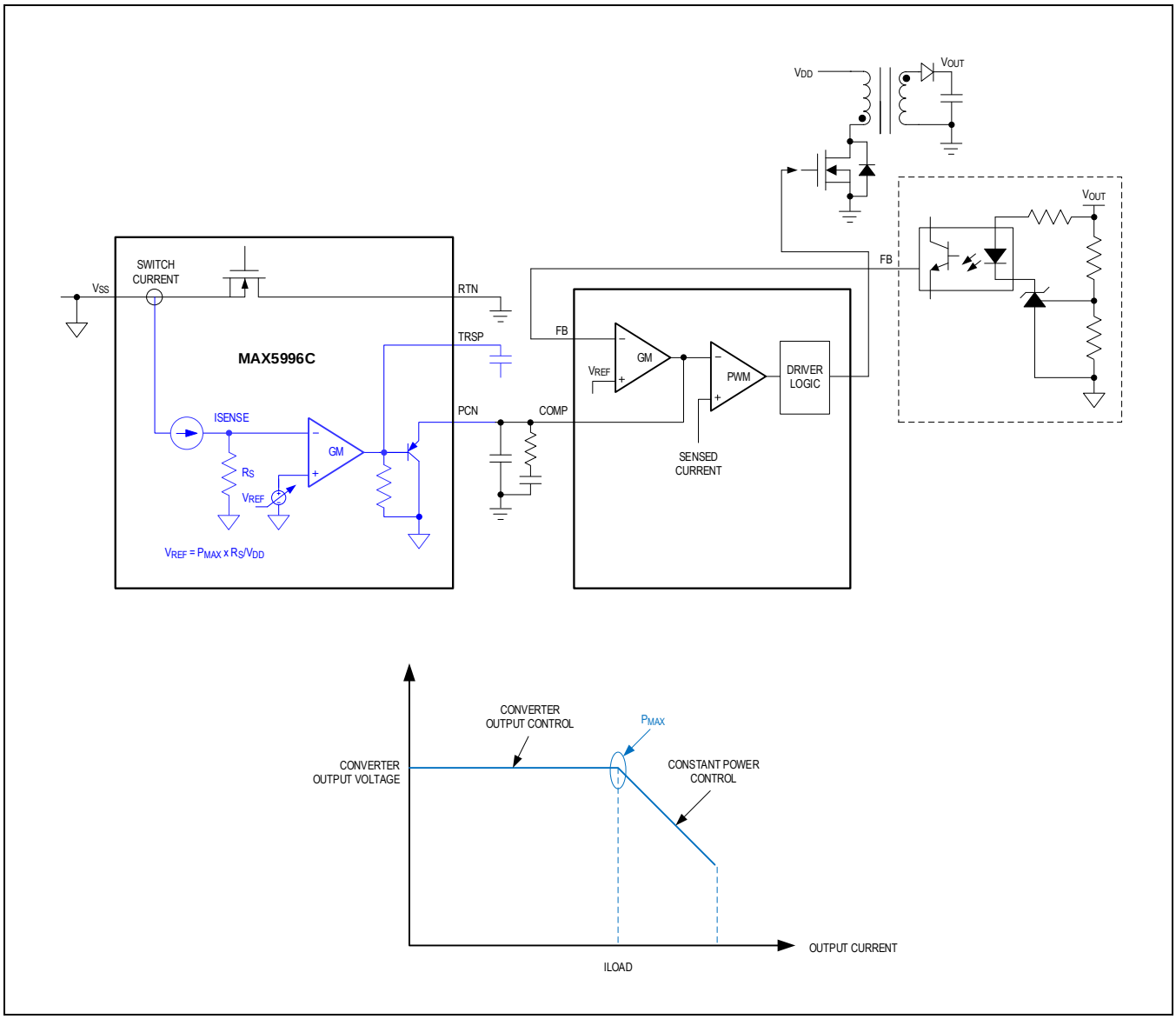


Figure 7. Constant Power Limiting

Current limit (MAX5996C)

When the LLDP pin is shorted to V_{SS} or receiving Current Limit pulses the device works in current limit mode. The current Limiting function is also disabled during MOSFET power-up and enabled 1.2ms (typ) after the MOSFET is fully enhanced and stays enabled at normal operation. Instead of limiting power in power mode, in current limiting mode, the device watches the MOSFET current and when the MOSFET current reaches the limit the loop starts to sink current from PCN pin and overdrive COMP pin of the MAX5974 (or other dc-dc controller IC) to limit output power, therefore limit the PD current. The current limit thresholds are determined from the Classification process, and each PD Class corresponds to specific current limit thresholds (See the *Electrical Characteristics* table). The current limiting function can be disabled by a floating TRSP pin.

When the PD current reaches overload current limit (2.4A typical) the PD current limiting function takes control immediately to limit the current to protect the MOSFET from overheating.

Overload Current Limit

The internal MOSFET is protected from output overload conditions with an overcurrent limit. An overload at the output results in the current being limited at the threshold (typical 2.4A for the MAX5996C) and output voltage droop. When VRTN – VVSS exceeds approximately 7.5V the overcurrent limit reverts to inrush current limit (45mA typical) to further reduce the power dissipation on the MOSFET.

Power Telemetry Report

The real-time input power consumption will be reported from the MEC pin through a series of patterned digitized pulses. The 90% pulse (900µs) is the start bit of power telemetry reporting, and the 50% pulse (500µs) represents “0” bit and the 75% pulse (750µs) represents “1” bit. The total 8-bit digitized pulse represents the real-time power up to 90W.

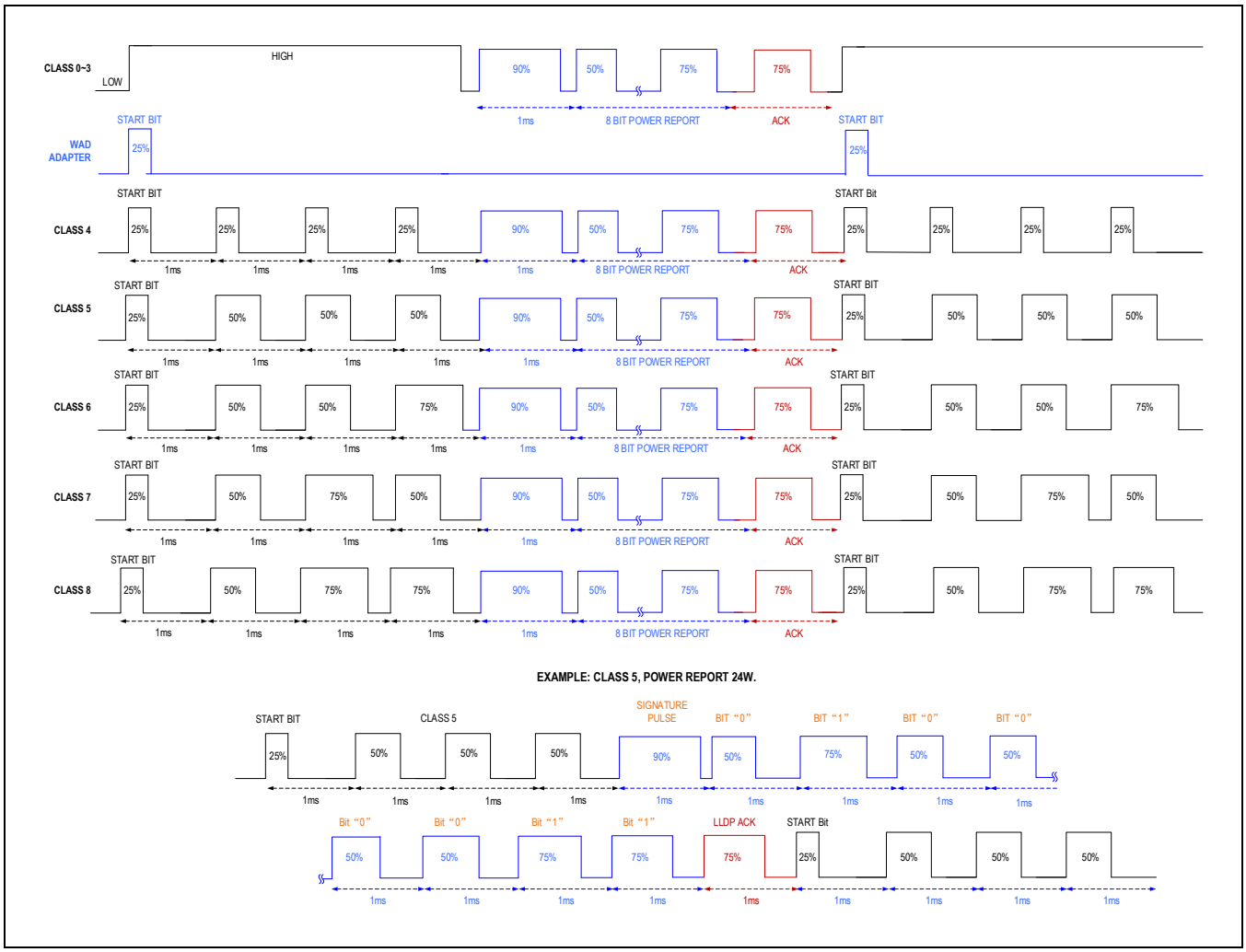


Figure 8. Power Telemetry Report

LLDP Power Level Identification

The Link Layer Discovery Protocol (LLDP) is a link layer protocol used by network devices to negotiate the power level. The main idea is that, after valid detection, PSE powers up the PD at type 1 for the PD system to build up the communication, and then PD will negotiate the power through software.

The MAX5996 LLDP pin enables the LLDP support by recognizing patterned input pulses from the system management micro-controller to configure the power or current level (P_{MAX} or IMAX) to the PD controller to limit the power or current consumption.

The MAX5996C supports power limiting and current limiting mode. The LLDP pin is used to configure which mode the device works with. See *Figure 9*. It is the device with a non-LLDP configuration, meaning there is no connection or communication from LLDP to system MCU. In this case

- When the LLDP pin is left floating the device works with the power mode.
- When the LLDP pin is shorted to V_{SS} the device works with the current mode.

Figure 10 shows the device with LLDP configuration, the LLDP pin behaves as an input pin to recognize power/current limit level requests from system MCU through a series of patterned pulses. The power/current limit level information overwrites the limits from the classification process.

Note that when there are no pulses coming from MCU, the LLDP pin is also “floating” and so it will be in power limiting mode unless certain patterned “current limiting mode” pulses come into the LLDP pin to switch the mode.

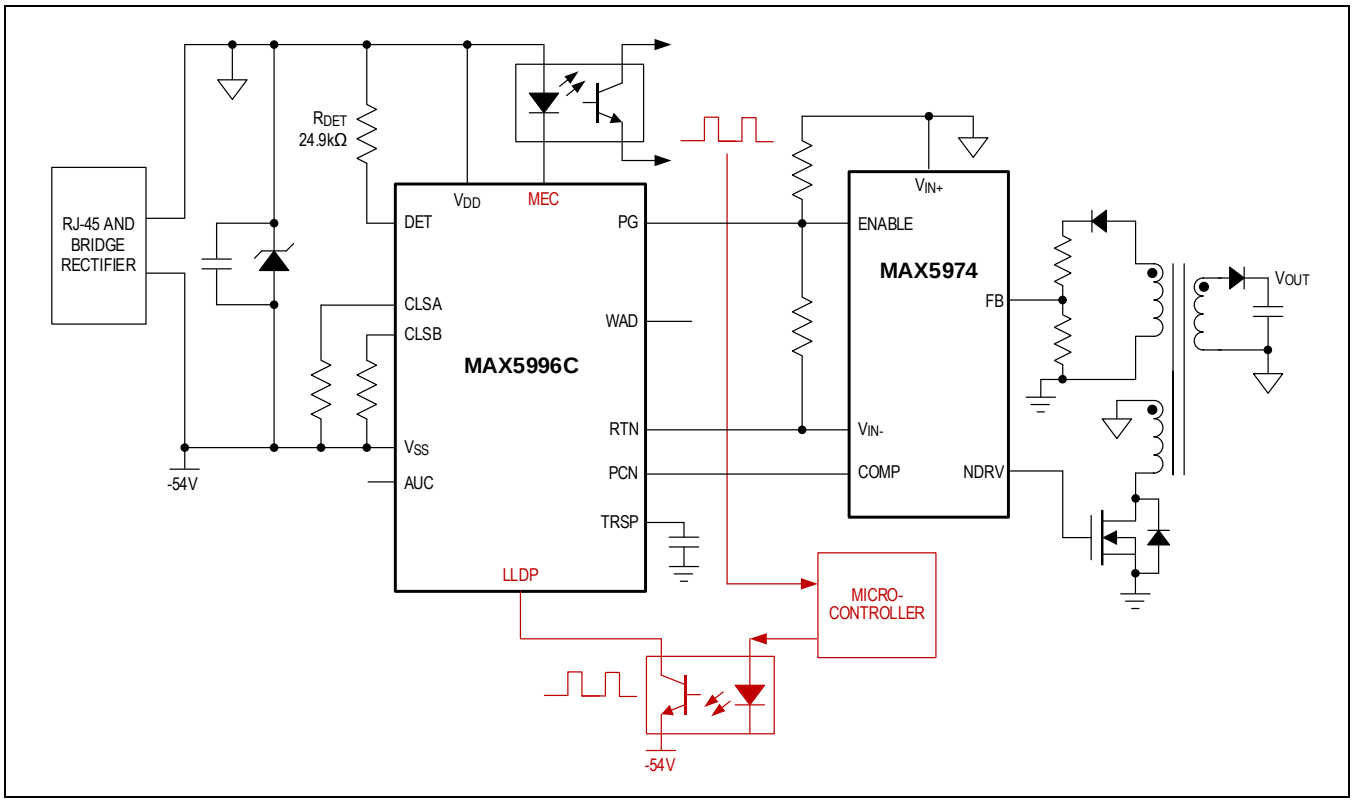


Figure 9. MEC Waveforms in Different Scenarios

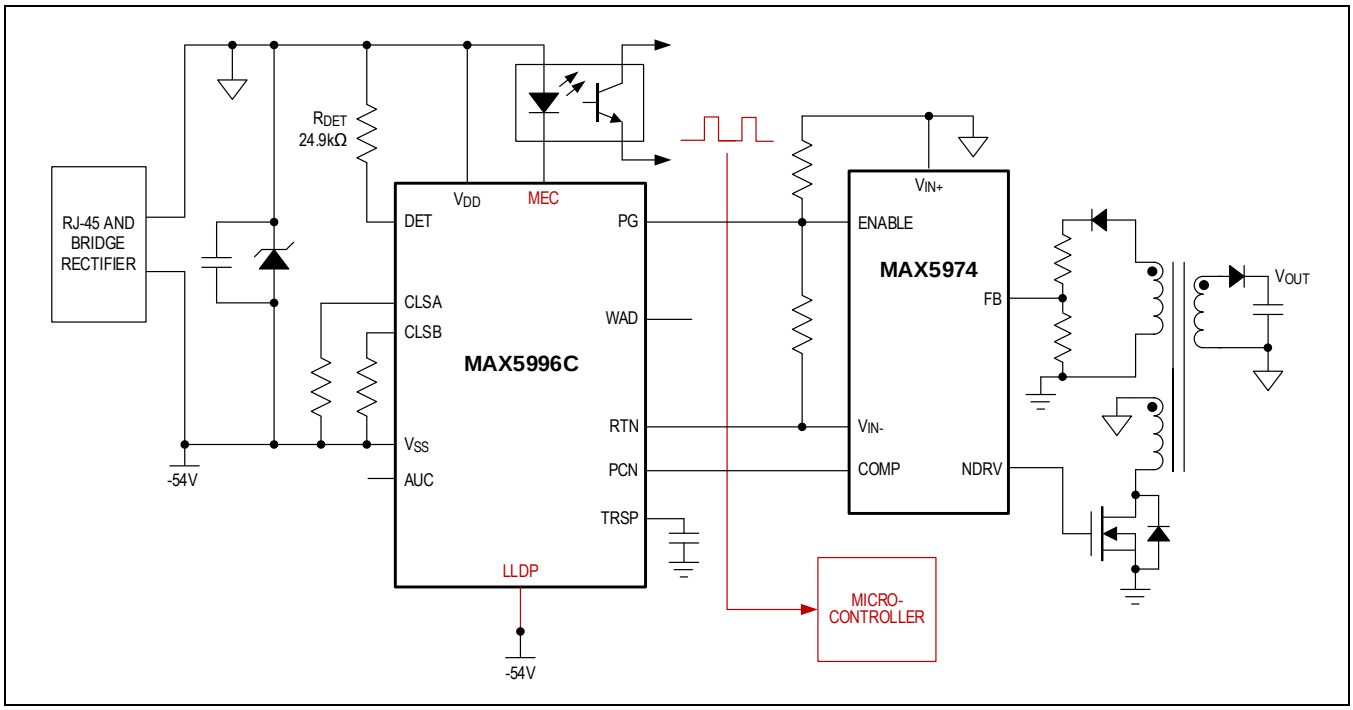


Figure 10. NQ85 is with Non-LLDP Configuration

The LLDP input pulses are a series of 50% (500µs) or 75% (750µs) pulses with 1000µs period. The first two 50% and 75% pulses are LLDP signature and references, and the following 8 pulses represent 8-bit power or current level. The 50% pulse represents bit “0” and the 75% pulse represents bit “1”. There needs at least a 22ms gap between two LLDP data frames.

- When two signature pulses are 50% first and 75% later, the device is in power limit mode. Following data pulse represents power limit information.
- When two signature pulses are 75% first and 50% later, the device is in a current limit mode. Following data pulse represents current limit information.

The device only allows mode changing when the power or current limit loop is not working.

Once the power/current limit level is recognized and identified from the LLDP pin the LLDP power/current limit level will overwrite the power/current level from the classification process. The PD controller will use the LLDP limit level as the power/current limiting control reference. The new LLDP power/current level reading overwrites the previous one.

When the MAX5996C powers down and up again the default power/current level is from the classification process till the LLDP reads back to power/current level and overwrites it.

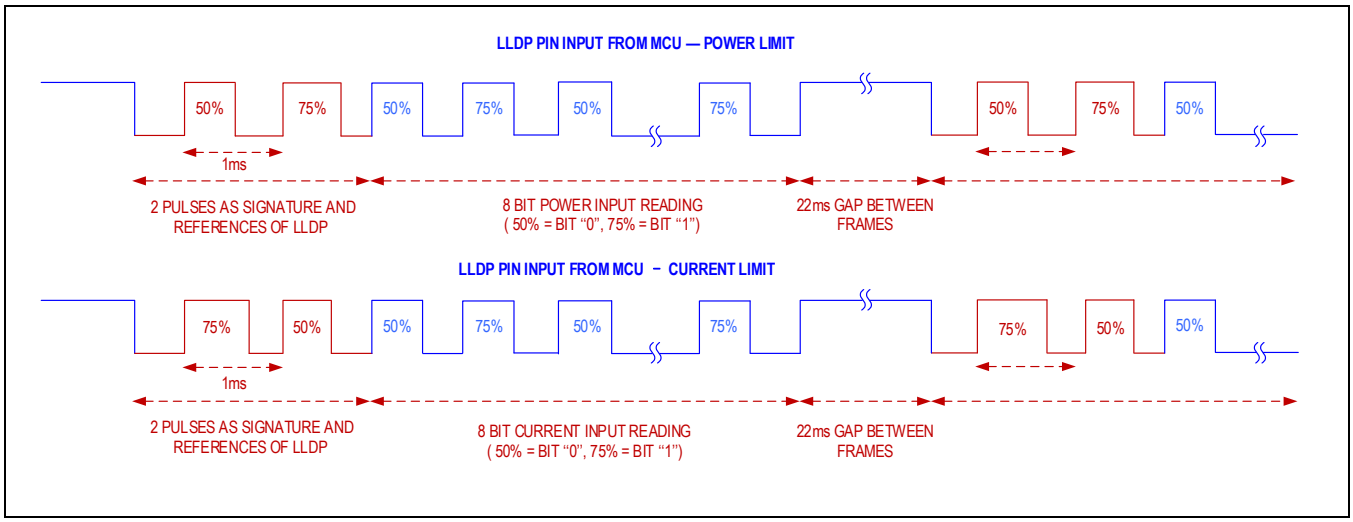
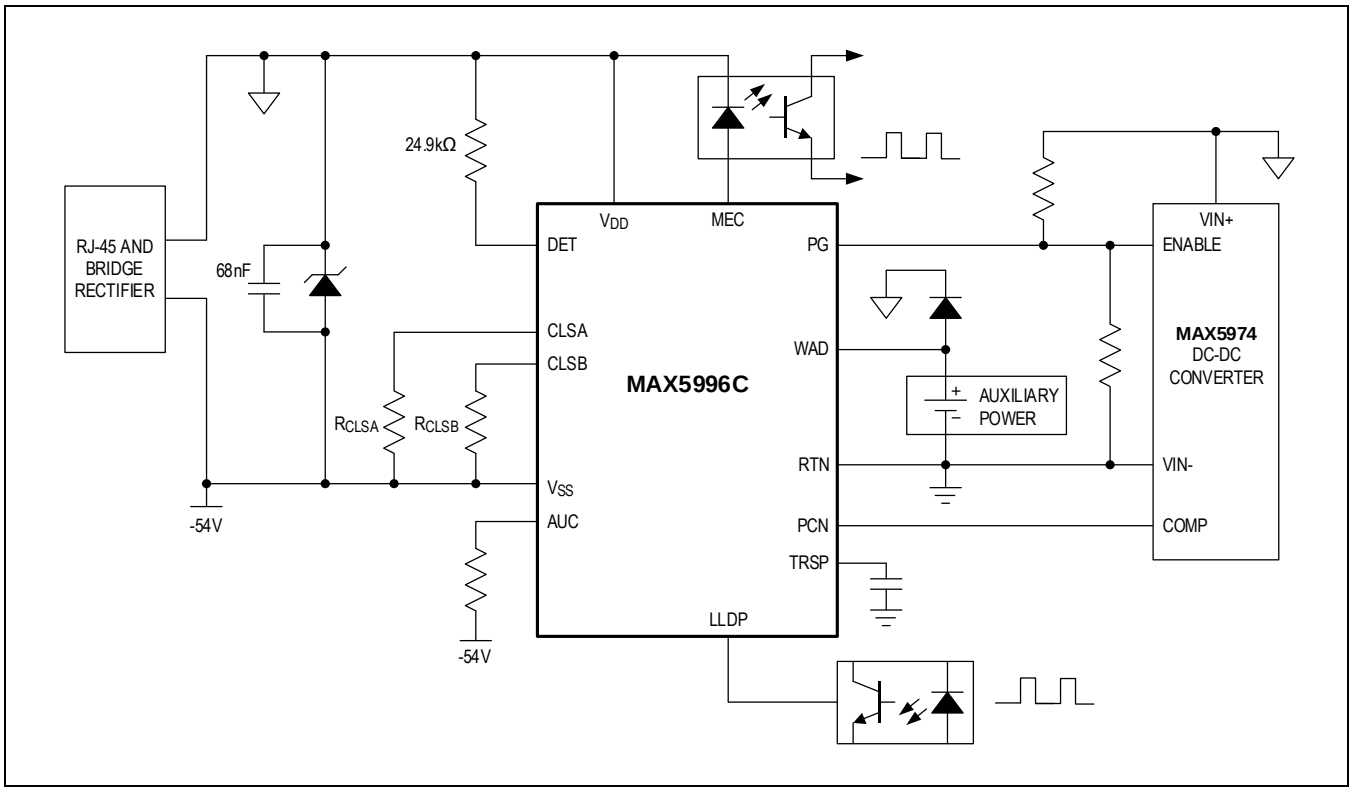
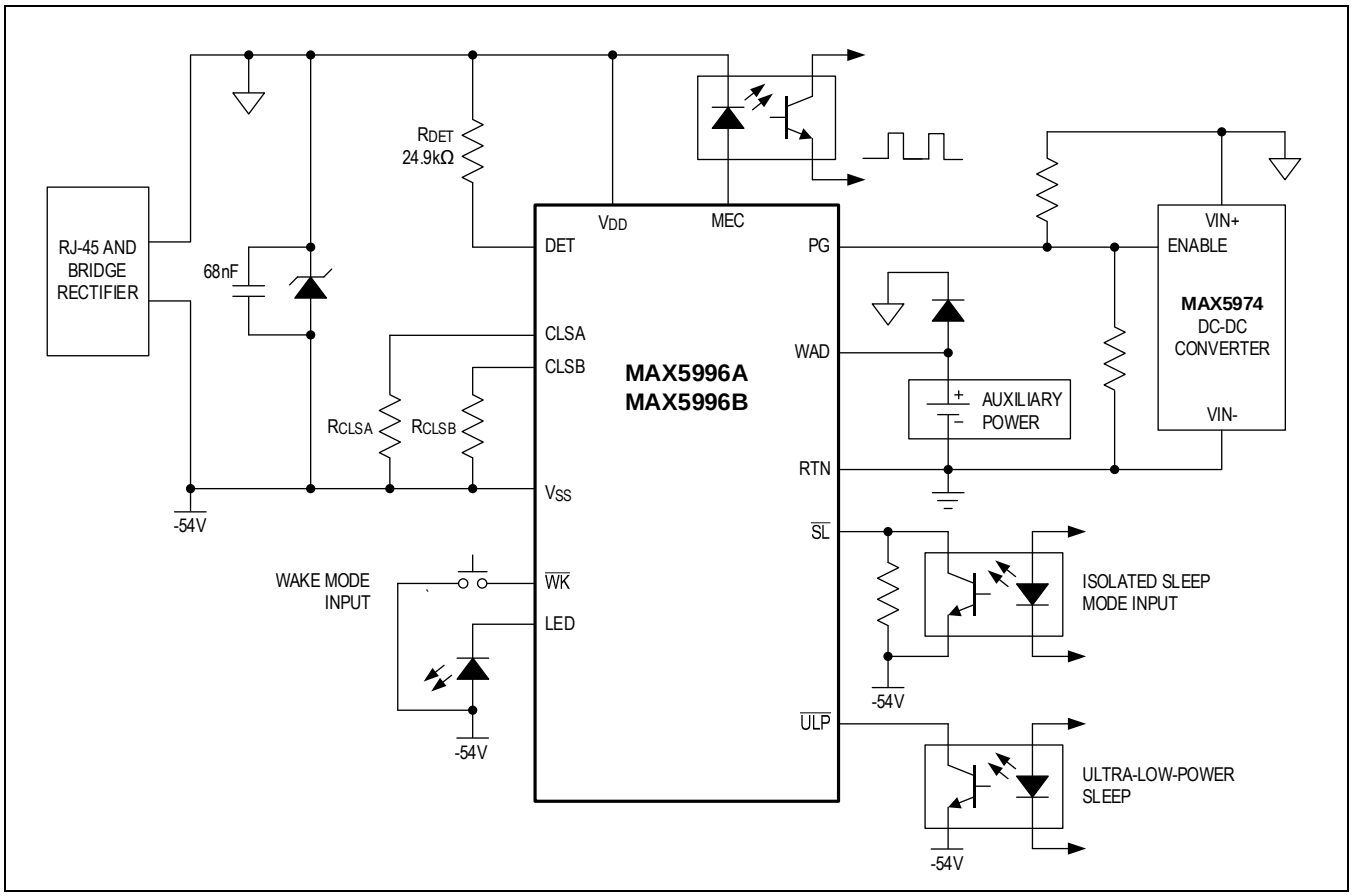


Figure 11. The LLDP Input Pulses

Typical Application Circuits





Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	INTELLIGENT MPS	SLEEP/ ULTRA-LOW-POWER MODE	6S FILTER DELAY ON SL	AUTO CLASS	CONSTANT POWER/ CURRENT LIMIT	LLDP	POWER TELEMETRY
MAX5996AATE+/ MAX5996AATE+T**	-40°C to +125°C	16 TQFN-EP	NO	YES	YES	NO	NO	NO	YES
MAX5996BATE+/ MAX5996BATE+T**	-40°C to +125°C	16 TQFN-EP	YES	YES	NO	NO	NO	NO	YES
MAX5996CATE+/ MAX5996CATE+T	-40°C to +125°C	16 TQFN-EP	YES	NO	NO	YES	YES	YES	YES

***Future product.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	09/21	Release for Market Intro	—

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