CY9266 HOTLink™ Evaluation Board User's Guide

Overview

This document describes the construction, interfaces, and operation of the CY9266–F (optical fiber), CY9266–P (plastic optical fiber), CY9266–T (shielded twisted pair/twinax), and CY9266–C (coaxial cable) HOTLink™ Evaluation Boards. These boards implement a complete bidirectional parallel-to-serial and serial-to-parallel communications link, capable of operation at serial rates of 150 to 400 Mbits/second (15 to 40 Mbytes/second). The supported rate of communication may be limited by the specific type and speed-grade of optical module or copper cable type used.

The CY9266 Evaluation Boards are optically, electrically, and mechanically compatible with the ANSI T11 Fibre Channel Interface, as documented in the ANSI standard ANS X3.230–1994. It provides three different methods of access for the TTL parallel interface and supervisor functions, for testing or exercising the serial data link.

Block Diagram

The block diagram in *Figure 1* illustrates the major functional blocks contained in the CY9266. These include:

- 10-bit TTL parallel transmit data input
- 10-bit TTL parallel receive data output
- Selectable Encoded or Bypass operation modes
- On-board socketed oscillator
- Selectable internal/external clocking
- Selectable signal-detect polarity
- Selectable local loopback
- Power supply voltage monitor
- Built-in self-test (BIST) pattern generation and checking hardware with error/status display

Board Connectors

This board offers three primary methods of TTL-level access:

- JP2—A 58-position (2 x 29) set of holes, capable of accepting a 0.025″ sq. pin-header on the top or bottom of the board
- JP3—A 60-position (2 x 30) 0.1″ spaced board-edge finger stock
- JP4—A 48-position (4 x 12 matrix) 0.025″ sq. pin-header mounted on the bottom of the board

Connectors JP2 and JP3 provide access to all data input and output buses as well as all BIST, control, and clocking signals for the HOTLink Transmitter and Receiver. These connectors may be used individually or together since all signals present on JP2 are also present on JP3. Power for the board is also brought in through these same connectors.

Connector JP4 is positioned and pinned to match up with the connector and signals present on other industry-standard Fibre Channel modules. Unlike these other modules (which may contain two full-duplex channels), this evaluation board only provides a single full-duplex channel. While sufficient room exists to build a board with two channels, other functionality was added (on-board oscillator, BIST PLD and display, etc.) in this space to allow better testing and demonstration of the enhanced capabilities present in the Cypress HOTLink parts.

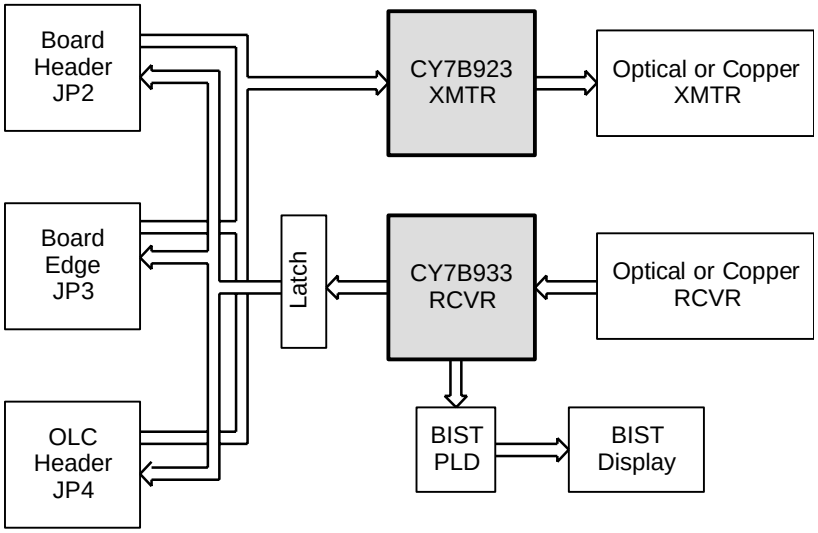


Figure 1. HOTLink Evaluation Board Block Diagram

An additional jumper block (JP1) is used to configure three of the operating characteristics of the board: clock sourcing, serial output enable (FOTO), and local loopback control.

Optical Modules

The CY9266–F Evaluation Board is designed to operate with industry-standard footprint optical modules. The evaluation board contains low-profile socket pins so the user may select and test optical modules from different vendors. This board accepts both the four-row DIP and the single-row 1X9 types of modules.

These modules are available from multiple vendors with either ST- or SC-type optical fiber connectors. Because these modules are all LED-based, they are not required to meet many of the safety standards (ANSI Z136.1 and Z136.2, F.D.A. regulation 21 CFR subchapter J, and IEC 825) necessary for LASER-based modules. These modules should be used with 62.5/125-mm multimode graded-index fiber.

For longer distance communications, LASER-based modules are also available that are compatible with the CY9266–F cards. However, when used with LASER transmitters, it is the responsibility of the user to receive what ever safety certifications are necessary.

The CY9266–P Evaluation Board is electrically identical to the CY9266–F, except that it is shipped with an optical module configured for low-cost plastic optical fiber, and set for a lower data rate (155 MBaud).

Coaxial Cables

The CY9266–C Evaluation Board is configured to support 75Ω coaxial cables that attach through BNC/TNC connectors. Other cable impedances may be used with the board by changing the value of the termination and driver bias resistors on the board.

Shielded-Pair Cables

The CY9266–T Evaluation Board is configured to support 150Ω shielded twisted-pair or twinaxial cable that attaches through a 9-pin D-sub connector. Other cable impedances may be used with the board by changing the value of the termination and driver bias resistors on the board.

BIST Support

The CY9266 contains an on-board control PLD and a two-digit error-count display that are used in conjunction with the BIST (Built-In Self-Test) capability of the Cypress Semiconductor HOTLink Transmitter and Receiver. This capability allows the parts, and any serial link, to be exercised and monitored at their full data rate without the use of expensive external test equipment.

The BIST PLD (CY7C344) contains a simple state machine that monitors the HOTLink Receiver BIST state, and an error-counter that drives an external display. The complete contents of this PLD are documented in Appendix C.

This BIST PLD also drives the four decimal point LEDs on the displays. These indicators are used to present additional status information about the state of the board, the BIST state machine, and the serial link.

Design Criteria

The CY9266 Evaluation Board was designed as a low-cost demonstration vehicle for the Cypress Semiconductor HOTLink family of data communications parts. The goals of this board are to:

- Present an interface board that is fully compliant with the mechanical, electrical, optical, coding, and protocol specifications in levels 0 and 1 of the ANSI X3.230 Fibre Channel standard
- Allow full data rate testing of the serial link without expensive test equipment
- Allow the user to exercise all modes of operation of the receiver and transmitter
- Offer various parallel attachment methods for simplified system interfacing
- Offer various media types for evaluation
- Allow simple interfacing to existing OLC-compatible test platforms

Because of the flexibility inherent in the HOTLink parts, these goals were easily achieved.

Three electrical connection methods are provided: a 60-pin board-edge connector, a 58-pin (2 x 29) 0.025″ square pin-header, and a 48-pin (4 x 12) 0.025″ square pin-header. These different connectors allow the user to select the connector form that best suits their desired mode of attachment.

The HOTLink Transmitter and Receiver contain a BIST capability. This capability was designed into the HOTLink parts to allow high-speed serial testing without expensive test equipment. All hardware necessary to exercise and monitor the BIST function is present on the CY9266 board. This hardware allows a bit-error-rate (BER) test to be performed without additional equipment.

The BIST capability of the HOTLink Transmitter and Receiver allows offline testing of the transmitter, receiver, and serial link, by performing a bit-by-bit comparison of the data while a 511-character pseudo-random data stream is repeatedly sent, received, and checked.

Through use of either JP2 or JP3, users may exercise all modes of operation of the parts. JP4 is configured as a functional system interface, and thus does not include all the mode, clock, and special control signals present on JP2 and JP3, all of which may be selected or controlled in JP1 or S1.

Connector Pin Numbering

JP2—58-Position Pin-Header

The 58-position pin-header (JP2) holes are located next to the board-edge connector. Pin 1 of this connector area is identified on the board by a square solder pad. The remaining pin locations use a round solder pad.

The connector hole pattern is made to accept fifty-eight 0.025″ square pins soldered into the board. The numbering for this connector is shown in *Figure 2*.

Note: The numbering of this connector is specified to match up with standard 0.050″ centerline flat cable connectors. Because of the location of pin 1 of this hole pattern, the mating pins for this connector should normally be on the bottom of the board. If a connector is instead attached to the top side of the board, the even- and odd-numbered pins of the connector are effectively swapped. This means that conductor 1 of a cable attached to the top side of the board is in reality connected to the signal listed for pin 2 in *Table 1*.

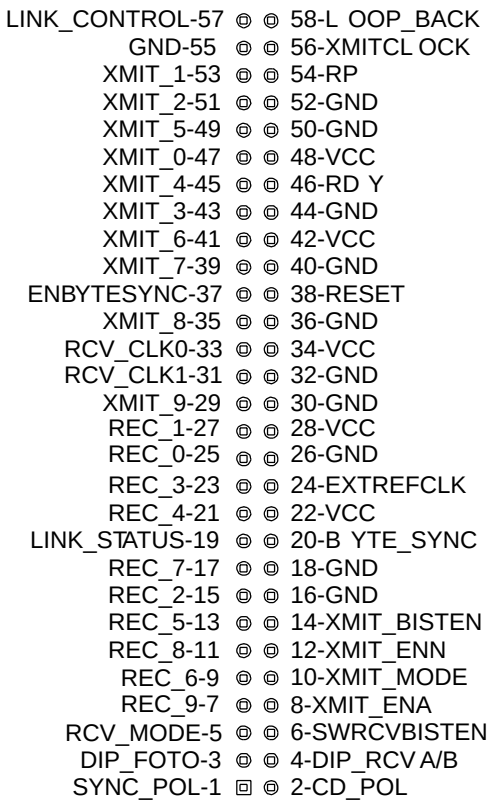


Figure 2. JP2 Pin Numbering, Top Side of Board View

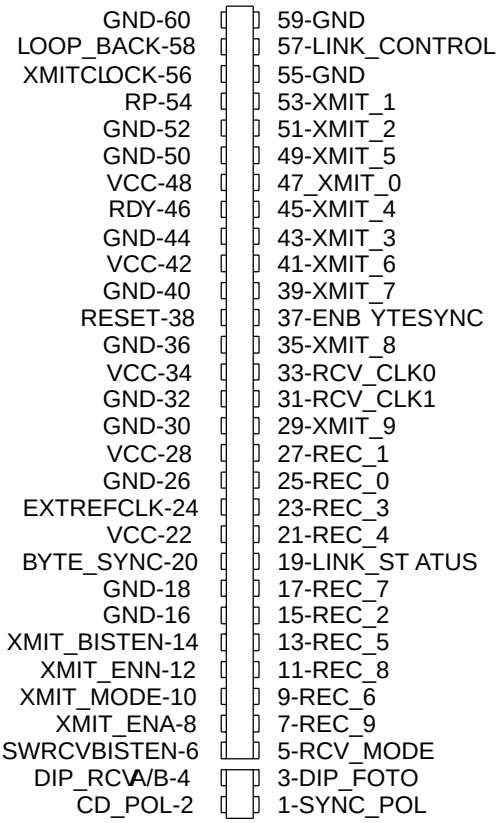


Figure 3. JP3 Pin Numbering, Edge of Board

JP3—60-Position Board-Edge

The 60-position board-edge connector (JP3) is a section of gold plated 0.062″ board finger-stock that connects to the same signals as JP2. Contact centerline for this connector is 0.1″, with even- and odd-numbered signals on opposing sides of the board.

To prevent the evaluation board from being plugged into a mating connector backwards (and possibly damaging it), a 0.040″ x 0.450″ keying slot is present between contacts 3/4 and 5/6. The pin numbering for this connector is shown in *Figure 3*.

Note: The numbering of this connector is specified to match up with standard 0.050″ centerline flat-cable connectors. Because of the location of pin 1 of this board-edge connector, the mating connector would normally be a mass-terminate board-edge to flat-cable type connector. If a standard board-edge connector is used instead, the even and odd numbered pins of the connector are effectively swapped. This means that pin 1 of a standard board-edge connector is in reality connected to the signal listed for pin 2 in *Table 1*.

JP4—OLC-Compatibility Connector

The JP4 (OLC-compatibility) connector is located on the bottom (passive-component) side of the board. Pin 1 of this connector is identified on the board by a square solder pad. The remaining pins use a round solder pad.

For the CY9266 Evaluation Board, pins of sufficient length are present so that analysis equipment may be attached to these signal pins on the top (active-component) side of the board

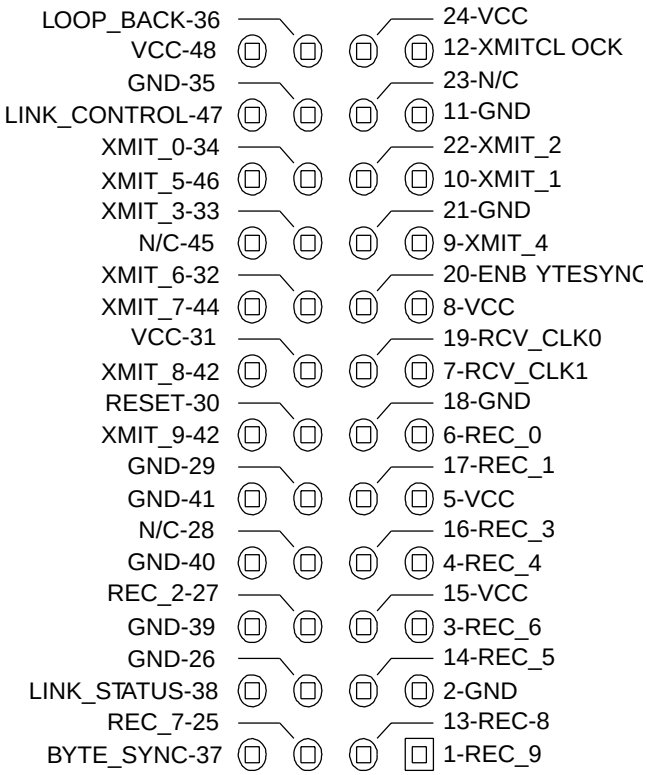


Figure 4. JP4 Pin Numbering, Top Side of Board View (Pins Are On the Bottom)

while it is plugged into a mating connector. The numbering sequence for the JP4 connector pins is shown in *Figure 4*.

The connector is made from forty-eight 0.025″ square pins soldered into the board. To allow full mating with an OLC-compatible connector, these pins must extend at least 0.250″ beyond the bottom surface of the board.

Connector Pinouts

The CY9266 provides three interface connectors to the user: JP2, JP3, and JP4. *Table 1* shows which signal is present on each connector pin.

Table 1. I/O Connector Pinouts

Pin No.	JP3	JP2	JP4	Pin No.	JP3	JP2	JP4
1	SYNC_POL	SYNC_POL	REC_9	31	RCV_CLK1	RCV_CLK1	VCC
2	CD_POL	CD_POL	GND	32	GND	GND	XMIT_6
3	DIP_FOTO	DIP_FOTO	REC_6	33	RCV_CLK0	RCV_CLK0	XMIT_3
4	DIP_RCVA/B	DIP_RCVA/B	REC_4	34	VCC	VCC	XMIT_0
5	RCV_MODE	RCV_MODE	VCC	35	XMIT_8	XMIT_8	GND
6	SWRCVBISTEN	SWRCVBISTEN	REC_0	36	GND	GND	LOOP_BACK
7	REC_9	REC_9	RCV_CLK1	37	ENBYTESYNC	ENBYTESYNC	BYTE_SYNC
8	XMIT_ENA	XMIT_ENA	VCC	38	RESET	RESET	LINK_STATUS
9	REC_6	REC_6	XMIT_4	39	XMIT_7	XMIT_7	GND
10	XMIT_MODE	XMIT_MODE	XMIT_1	40	GND	GND	GND
11	REC_8	REC_8	GND	41	XMIT_6	XMIT_6	GND
12	XMIT_ENN	XMIT_ENN	XMITCLOCK	42	VCC	VCC	XMIT_9
13	REC_5	REC_5	REC_8	43	XMIT_3	XMIT_3	XMIT_8
14	XMIT_BISTEN	XMIT_BISTEN	REC_5	44	GND	GND	XMIT_7
15	REC_2	REC_2	VCC	45	XMIT_4	XMIT_4	N/C
16	GND	GND	REC_3	46	RDY	RDY	XMIT_5
17	REC_7	REC_7	REC_1	47	XMIT_0	XMIT_0	LINK_CONTROL
18	GND	GND	GND	48	VCC	VCC	VCC
19	LINK_STATUS	LINK_STATUS	RCV_CLK0	49	XMIT_5	XMIT_5	
20	BYTE_SYNC	BYTE_SYNC	ENBYTESYNC	50	GND	GND	
21	REC_4	REC_4	GND	51	XMIT_2	XMIT_2	
22	VCC	VCC	XMIT_2	52	GND	GND	
23	REC_3	REC_3	N/C	53	XMIT_1	XMIT_1	
24	EXTREFCLK	EXTREFCLK	VCC	54	RP	RP	
25	REC_0	REC_0	REC_7	55	GND	GND	
26	GND	GND	GND	56	XMITCLOCK	XMITCLOCK	
27	REC_1	REC_1	REC_2	57	LINK_CONTROL	LINK_CONTROL	
28	VCC	VCC	N/C	58	LOOP_BACK	LOOP_BACK	
29	XMIT_9	XMIT_9	GND	59	GND		
30	GND	GND	RESET	60	GND		

Signal Naming Conventions

There are three types of signal names used throughout this document: I/O connector pin names, on-board signal names, and HOTLink Transmitter and Receiver pin names. Except for the transmit and receive data buses, these names are unique.

The names used for the transmit and receive data bus pins on connectors JP2, JP3, and JP4 are different from the signal names present on the HOTLink Transmitter and Receiver. The functional names for these signals also change depending on the current operating mode of the HOTLink Transmitter or Receiver. *Table 2* lists the transmit data bus signals and the names mapped to them in each transmitter mode.

The output data bus from the HOTLink Receiver is pipelined with a single register stage between the receiver outputs and the board output pins. *Table 3* lists the receive data bus signals and the names mapped to them in each receiver mode.

Table 2. Transmit Bus Signal Name Map

Transmit Bus Input Pin Name	HOTLink Transmitter Pin Name	
	Encoded Mode	Bypass Mode
XMIT_0	SC/$\overline{D}$	Da
XMIT_1	D0	Db
XMIT_2	D1	Dc
XMIT_3	D2	Dd
XMIT_4	D3	De
XMIT_5	D4	Di
XMIT_6	D5	Df
XMIT_7	D6	Dg
XMIT_8	D7	Dh
XMIT_9	SVS	Dj

Table 3. Receive Bus Signal Name Map

Receive Bus Output Pin Name	HOTLink Receiver Pin Name	
	Decode Mode	Bypass Mode
REC_0	SC/$\overline{D}$	Qa
REC_1	Q0	Qb
REC_2	Q1	Qc
REC_3	Q2	Qd
REC_4	Q3	Qe
REC_5	Q4	Qi
REC_6	Q5	Qf
REC_7	Q6	Qg
REC_8	Q7	Qh
REC_9	RVS	Qj

Signal Descriptions

The I/O signals listed in *Table 1* fall into six groups: power, switched control, control, status, clock, and data. These signals are described in *Table 4*.

Table 4. I/O Signal Descriptions

Signal Name	Group	Description
V_{CC}	Power	+5 VDC @ 1.0A typical
GND	Power	Ground
XMIT_BISTEN	Input, Switched Control	**Transmitter BIST Enable (S1-1).** When this signal is LOW, the HOTLink Transmitter is placed into its BIST mode. Exact operation of the transmitter is also determined by the settings of the $\overline{ENA}$ (S1-4) and $\overline{ENN}$ (S1-3) signals. With both $\overline{ENA}$ and $\overline{ENN}$ HIGH, the transmitter outputs an alternating 0–1 pattern (D10.2 or D21.5). If either $\overline{ENA}$ or $\overline{ENN}$ is LOW, the transmitter sends a repeating 511-character test sequence. The receiver contains a matching mode that allows this transmitter BIST mode to be used to test the entire serial link without external hardware. The transmitter BIST enable is kept separate from the receiver BIST enable on this board to allow each component to be tested with external patterns that are not part of the BIST sequence.
XMIT_MODE	Input, Switched Control	**Encoder Mode Select (S1-2).** This signal is used to select whether pre-encoded (10-bit) or non-encoded (8-bit) data is clocked into the HOTLink Transmitter. When LOW (Encoded mode), this input enables the internal 8B/10B encoder and accepts 8-bit parallel data from the transmitter data bus (D0–D7 as listed in *Table 2*). When HIGH (Bypass mode), the encoder is bypassed and a 10-bit pattern is accepted (Da–Dj as listed in *Table 2)*.
XMIT_ENN	Input, Switched Control	**Enable Next Parallel Transmitter Data (S1-3).** This signal is used to control when data is loaded into the HOTLink Transmitter. When this signal is LOW at the rising edge of CKW, the data present on the transmitter inputs at the next rising edge of CKW is loaded, processed, and sent. When this signal is HIGH, the transmitter ignores the data present on its inputs at the next rising edge of CKW and instead inserts a SYNC character (K28.5) to fill in the data stream. When $\overline{ENA}$ is used for data control, the $\overline{ENN}$ signal should be tied HIGH, but may be used to enable BIST mode.
XMIT_ENA	Input, Switched Control	**Enable Parallel Transmitter Data (S1-4).** This signal is used to control when data is loaded into the HOTLink Transmitter. When LOW at the rising edge of CKW, the data present on the transmitter inputs is loaded, processed, and sent. When this signal is HIGH, the transmitter ignores the data present on its inputs and instead inserts a SYNC character (K28.5) to fill in the data stream. When $\overline{ENN}$ is used for data control, the $\overline{ENA}$ signal should be tied HIGH, but may be used to enable BIST mode.
SWRCVBISTEN	Input, Switched Control	**Receiver BIST Enable (S1-5).** When this signal is LOW, the HOTLink Receiver monitors the data stream for the BIST loop initialization character (D0.0). This signal also enables the BIST PLD (CY7C344–U8), which is used to monitor the progress and status of the BIST loop through the receiver $\overline{RDY}$ and RVS outputs. When the receiver detects the initialization character, it begins comparing received data with a built-in data sequence that can be used to verify the proper functionality of the transmitter, receiver, and the serial link connecting them. The receiver BIST enable is kept separate from the transmitter BIST enable on this board to allow each component to be tested with external patterns that are not part of the BIST sequence.
RCV_MODE	Input, Switched Control	**Receiver Mode Select (S1-6).** This signal is used to select whether encoded (10-bit) or non-encoded (8-bit) data is output from the receiver. When LOW (Decode mode), this input enables the internal 10B/8B decoder and outputs 8-bit parallel data (Q0–Q7 as listed in *Table 3*). When HIGH (Bypass mode), the decoder is bypassed and a 10-bit pattern is output (Qa–Qj as listed in *Table 3*).

Table 4. I/O Signal Descriptions (continued)

Signal Name	Group	Description
DIP_RCVA/B	Input, Switched Control	**DIP-Switch Controlled Receiver A/$\overline{B}$ Port Select (S1-7).** This signal is used to determine which port (INA± or INB±) the receiver uses for the input serial data stream. When LOW, this signal selects the receiver B port that is directly connected to the C port on the transmitter. When HIGH, this signal selects the receiver A port that is connected to the optical receiver output. This signal is also routed through jumper block JP1. In order for this signal to control the port selection of the receiver, it is necessary to have a shorting jumper across the X and Y pins of JP1-C. To allow the LOOP_BACK signal on the I/O connectors (JP2, JP3, and JP4) to control the A/$\overline{B}$ port selection, this jumper should be moved to JP1-B.
DIP_FOTO	Input, Switched Control	**DIP-Switch Controlled FOTO (S1-8).** This signal is used to enable the A and B differential output drivers of the HOTLink Transmitter. When this signal is LOW, the differential outputs are allowed to follow the pattern of the data serialized by the transmitter. When this signal is HIGH, the A and B differential outputs of the transmitter are driven to a logic zero state (+ output is logic HIGH, – output is logic LOW). This places an attached optical transmitter in a state where no light is output. This signal is also routed through jumper block JP1. In order for this signal to control the FOTO (fiber-optic transmitter-off) enable on the transmitter, it is necessary to have a shorting jumper across the X and Y pins of JP1-E. To allow the LINK_CONTROL signal on the I/O connectors (JP2, JP3, and JP4) to control the FOTO enable, this jumper should be moved to JP1-F.
CD_POL	Input, Switched Control	**Signal-Detect Polarity Select (S1-9).** This input selects the output polarity of the LINK_STATUS signal. When LOW, the LINK_STATUS signal is HIGH when a valid signal is present. When HIGH, the LINK_STATUS signal is LOW when a valid signal is present.
SYNC_POL	Input, Switched Control	**Byte Sync Polarity Select (S1-10).** This input, in conjunction with the HOTLink Receiver MODE input, selects the active level of the BYTE_SYNC signal. When LOW with the receiver in Bypass mode, the BYTE_SYNC signal is LOW when a K28.5 SYNC character is present on the receive data bus. When HIGH with the receiver in Bypass mode, the BYTE_SYNC signal is HIGH when a K28.5 SYNC character is present on the receive data bus. When LOW with the receiver in Decode mode, the BYTE_SYNC output remains HIGH for strings of K28.5 SYNC characters, or while awaiting the first K28.5 SYNC character after being placed into Reframe mode (RF is set HIGH). When HIGH with the receiver in Decode mode, the BYTE_SYNC output remains LOW for strings of K28.5 SYNC characters, or while awaiting the first K28.5 SYNC character after being placed into Reframe mode (RF is set HIGH).
LOOP_BACK	Input, Control	**Loopback Control.** This signal is used to determine which port (A or B) the HOTLink Receiver uses for the input serial data stream. When LOW, this signal selects the receiver B port that is connected directly to the transmitter C port. When HIGH, this signal selects the receiver A port that is connected to the optical receiver output. This signal is also routed through jumper block JP1. In order for this signal to control the port selection of the receiver, it is necessary to have a shorting jumper across the X and Y pins of JP1-B. To allow the DIP_RCVA/B signal (S1-7, also present on JP2 and JP3) to control the A/$\overline{B}$ port selection, this jumper should be moved to JP1-C.
ENBYTESYNC	Input, Control	**Enable Byte Sync Detect.** This signal controls when the HOTLink Receiver is allowed to reframe to the incoming serial data (e.g., acquire character sync). When this signal is HIGH, each K28.5 SYNC character received in the shifter will frame the data that follows. When this signal is LOW, the framing logic in the receiver is disabled. Because the CKR output of the receiver must line up with the reframed data, it is possible to generate significant phase jumps in the CKR clock. To prevent the generation of very short high or low pulses on the CKR output (which could cause timing violations in downstream logic) the Cypress HOTLink Receiver uses look-ahead hardware to prevent these short pulses. Instead, a portion of the clock period for the character preceding the reframed data is lengthened.

Table 4. I/O Signal Descriptions (continued)

Signal Name	Group	Description
LINK_ CONTROL	Input, Control	**Link Control.** This signal is used to enable the A and B differential output drivers of the HOTLink Transmitter. When this signal is LOW, the differential outputs are allowed to follow the pattern of the data serialized by the transmitter. When this signal is HIGH, the A and B differential outputs of the transmitter are driven to a logic zero state (+ output is logic HIGH, – output is logic LOW). This places an attached optical transmitter in a state where no light is output. This signal is also routed through jumper block JP1. In order for this signal to control the FOTO enable on the transmitter, it is necessary to have a shorting jumper across the X and Y pins of JP1-F. To allow the DIP_FOTO signal on the I/O connectors (JP2 and JP3) to control the FOTO enable, this jumper should be moved to JP1-E.
RESET	Output, Status	**Reset/Power OK.** This output is used to emulate the voltage monitor function present on the OLC card. It remains active (LOW) until the V_{CC} input to the board is above 4.65V DC. This output also becomes active when the BIST RESET switch (S2) is pressed.
LINK_STATUS	Output, Status	**Link Status.** This signal operates as a signal-detect status for the serial interface. The polarity of this signal is determined by the CD_POL input (S1-9). When CD_POL is LOW, LINK_STATUS drives HIGH when a signal is present. When CD_POL is HIGH, LINK_STATUS drives LOW when a signal is present.
RP	Output, Clock	**Read Pulse.** This is a 60% LOW duty-cycle pulse train suitable for clocking data out of Cypress's CY7C42X family of asynchronous FIFOs. This pulse is generated by the HOTLink Transmitter in response to the XMIT_ENA input being active at the rising edge of CKW. For repeated pulses the $\overline{RP}$ period is the same as CKW, yet is totally independent of the duty cycle of CKW. When the transmitter is in BIST mode, the $\overline{RP}$ signal remains HIGH for all but the last character of the BIST loop, where it pulses LOW.
XMITCLOCK	Input, Output, Clock	**Transmitter External Clock.** This is the external character-rate clock input. This clock is used to drive the transmitter CKW input. To allow for operation using the on-board oscillator, the XMITCLOCK signal is run through jumper block JP1. To operate using an external HOTLink Transmitter clock source, a shorting jumper should be placed across pins X and Y of JP1-G. To use the on-board oscillator instead, this shorting jumper should be moved to connect pin JP1-GY to JP1-HY. When operated from XMITCLOCK, the receiver REFCLK may also be set to use this same clock. This is done by placing a shorting jumper across pins JP1-HX and JP1-IX. To allow the receiver REFCLK to operate from the on-board oscillator, this jumper should be moved to connect the X and Y pins of JP1-I. The on-board oscillator may also be driven out on the XMITCLOCK line by placing a shorting jumper across pins X and Y of JP1-H.
EXTREFCLK	Input, Output, Clock	**External Reference Clock.** This character-rate clock is used to drive the HOTLink Receiver REFCLK from an external source other than XMITCLOCK. This input may be used to test the tracking and capture range of the receiver PLL. It may also be used to operate the receiver at a different data rate from the transmitter. To allow the receiver PLL to properly lock to the received serial stream, this clock must be within 0.1% of the clock used to generate the received serial data. To drive the receiver REFCLK from this clock source, a shorting jumper should be placed across pins JP1-IX and JP1-JX. The on-board oscillator may also be selected to drive the EXTREFCLK line by placing a shorting jumper across pins X and Y of JP1-J. With this jumper in place it is still possible to drive the receiver REFCLK input from the on-board oscillator by placing a shorting jumper across the X and Y pins of JP1-I.
RCV_CLK0	Output, Clock	**Receive Clock 0.** This is the character-rate recovered clock used for received data. The period of this clock is determined by the serial data rate entering the HOTLink Receiver. The duty-cycle of this signal is determined by the receiver and is fixed at 50%. This clock may experience a large phase jump when reframing to a serial data stream. The phasing on this clock is such that the rising edge of the clock occurs coincident with the start of each interval where a character is present on the output received data bus. This signal is a buffered form of the HOTLink Receiver CKR clock.

Table 4. I/O Signal Descriptions (continued)

Signal Name	Group	Description
RCV_CLK1	Output, Clock	**Receive Clock 1.** This is the character-rate recovered clock used for received data. The period of this clock is determined by the serial data rate entering the HOTLink Receiver. The duty-cycle of this signal is determined by the receiver and is fixed at 50%. This clock may experience a large phase jump when reframing to a serial data stream. The phasing on this clock is such that the rising edge of the clock occurs near the center of each interval where a character is present on the output received data bus. This signal is a buffered and inverted form of the HOTLink Receiver CKR clock.
RDY	Output, Clock	**$\overline{\text{RDY}}$ (Ready).** This signal is used both as a HOTLink Receiver data output clock and a status indicator for the receiver when in BIST mode. This is an unbuffered output from the receiver. It is normally used to clock valid data from the receiver data bus into synchronous FIFOs. Because of the additional pipeline register in the data bus (added for OLC compatibility) this signal will operate one character *prior* to the data being available at the I/O connectors.
BYTE_SYNC	Output, Data	**Byte Sync Detected.** This signal is a pipelined form of the receiver $\overline{\text{RDY}}$ output. This additional pipeline stage for the $\overline{\text{RDY}}$ signal (and the rest of the receiver data bus) was added to match the specific timing of the OLC Byte Sync signal. The active level of this output is determined both by the operating mode of the HOTLink Receiver and by the state of the SYNC_POL input. With the HOTLink Receiver in Bypass mode, the BYTE_SYNC signal is used as a K28.5 SYNC character indicator. With SYNC_POL LOW, BYTE_SYNC is LOW when a K28.5 SYNC character is present on the receive data bus. With SYNC_POL HIGH, BYTE_SYNC is HIGH when a K28.5 SYNC character is present on the receive data bus. With the receiver in Decode mode, the BYTE_SYNC signal is used as a valid data indicator. With SYNC_POL LOW, BYTE_SYNC is LOW whenever a usable data character is present on the receive data bus. With SYNC_POL HIGH, BYTE_SYNC is HIGH whenever a usable data character is present on the receive data bus.
REC_9	Output, Data	**RVS(Qj).** This signal is a series-terminated, pipelined form of the HOTLink Receiver RVS(Qj) signal. This termination and additional pipeline stage for the RVS(Qj) signal (and the rest of the receive data bus) was added to match the specific timing and signal characteristics of the OLC card.
REC_8	Output, Data	**Q7(Qh).** This signal is a series-terminated, pipelined form of the HOTLink Receiver Q7(Qh) signal.
REC_7	Output, Data	**Q6(Qg).** This signal is a series-terminated, pipelined form of the HOTLink Receiver Q6(Qg) signal.
REC_6	Output, Data	**Q5(Qf).** This signal is a series-terminated, pipelined form of the HOTLink Receiver Q5(Qf) signal.
REC_5	Output, Data	**Q4(Qi).** This signal is a series-terminated, pipelined form of the HOTLink Receiver Q4(Qi) signal.
REC_4	Output, Data	**Q3(Qe).** This signal is a series-terminated, pipelined form of the HOTLink Receiver Q3(Qe) signal.
REC_3	Output, Data	**Q2(Qd).** This signal is a series-terminated, pipelined form of the HOTLink Receiver Q2(Qd) signal.
REC_2	Output, Data	**Q1(Qc).** This signal is a series-terminated, pipelined form of the HOTLink Receiver Q1(Qc) signal.
REC_1	Output, Data	**Q0(Qb).** This signal is a series-terminated, pipelined form of the HOTLink Receiver Q0(Qb) signal.
REC_0	Output, Data	**SC/$\overline{\text{D}}$(Qa)**. This signal is a series-terminated, pipelined form of the HOTLink Receiver SC/$\overline{\text{D}}$(Qa) signal.
XMIT_9	Input, Data	**SVS(Dj).** This signal is the SVS(Dj) input to the HOTLink Transmitter. It is latched into the transmitter in the rising edge of CKW, when enabled by $\overline{\text{ENA}}$ or $\overline{\text{ENN}}$.

Table 4. I/O Signal Descriptions (continued)

Signal Name	Group	Description
XMIT_8	Input, Data	**D7(Dh).** This signal is the D7(Dh) input to the HOTLink Transmitter. It is latched into the transmitter in the rising edge of CKW, when enabled by $\overline{ENA}$ or $\overline{ENN}$.
XMIT_7	Input, Data	**D6(Dg).** This signal is the D6(Dg) input to the HOTLink Transmitter. It is latched into the transmitter in the rising edge of CKW, when enabled by $\overline{ENA}$ or $\overline{ENN}$.
XMIT_6	Input, Data	**D5(Df).** This signal is the D5(Df) input to the HOTLink Transmitter. It is latched into the transmitter in the rising edge of CKW, when enabled by $\overline{ENA}$ or $\overline{ENN}$.
XMIT_5	Input, Data	**D4(Di).** This signal is the D4(Di) input to the HOTLink Transmitter. It is latched into the transmitter in the rising edge of CKW, when enabled by $\overline{ENA}$ or $\overline{ENN}$.
XMIT_4	Input, Data	**D3(De).** This signal is the D3(De) input to the HOTLink Transmitter. It is latched into the transmitter in the rising edge of CKW, when enabled by $\overline{ENA}$ or $\overline{ENN}$.
XMIT_3	Input, Data	**D2(Dd).** This signal is the D2(Dd) input to the HOTLink Transmitter. It is latched into the transmitter in the rising edge of CKW, when enabled by $\overline{ENA}$ or $\overline{ENN}$.
XMIT_2	Input, Data	**D1(Dc).** This signal is the D1(Dc) input to the HOTLink Transmitter. It is latched into the transmitter in the rising edge of CKW, when enabled by $\overline{ENA}$ or $\overline{ENN}$.
XMIT_1	Input, Data	**D0(Db).** This signal is the D0(Db) input to the HOTLink Transmitter. It is latched into the transmitter in the rising edge of CKW, when enabled by $\overline{ENA}$ or $\overline{ENN}$.
XMIT_0	Input, Data	**SC/$\overline{D}$(Da).** This signal is the SC/$\overline{D}$(Da) input to the HOTLink Transmitter. It is latched into the transmitter in the rising edge of CKW, when enabled by $\overline{ENA}$ or $\overline{ENN}$.

Power Signals

The CY9266 Evaluation Board is designed to operate from a single +5V ±10% DC supply capable of delivering 1.0A (typical). All V_{CC} and GND pins on JP2, JP3, and JP4 are (respectively) common to each other. There are no distinctions made for separate supplies pins for the different logic sections.

Switched Control Signals

The CY9266 Evaluation Board contains a 10-position DIP switch (S1). This switch is connected in parallel with a number of control signals on JP2 and JP3. Each of these control signals is pulled-up by a 5-kΩ resistor through R-pack R20. None of these Switched Control signals are available at the JP4 connector.

The signals present in this group are:

- XMIT_BISTEN (S1-1)
- XMIT_MODE (S1-2)
- XMIT_ENN (S1-3)
- XMIT_ENA (S1-4)
- SWRCVBISTEN (S1-5)
- RCV_MODE (S1-6)
- DIP_RCVA/B (S1-7)
- DIP_FOTO (S1-8)
- CD_POL (S1-9)
- SYNC_POL (S1-10)

To allow these signals to be controlled through the external connectors (JP2 and JP3), the corresponding S1 switch must be in the off (open) position. Care should be taken when driving these signals, as any switch inadvertently left in the closed position will present a direct short to ground for an attached driver.

Control Signals

In addition to the Switched Control signals that are only present on JP2 and JP3, three additional control inputs are present that connect to JP2, JP3, and JP4.

These control signals are:

- LOOP_BACK
- ENBYTSYNC
- LINK_CONTROL

These control inputs are connected directly to the HOTLink Transmitter or Receiver. Because the HOTLink parts contain internal pull-up resistors on their TTL compatible inputs, these signals may be driven with either open-collector buffers, CMOS, or TTL drive levels.

Status Signals

Two status output signals (RESET and LINK_STATUS) are provided at all three I/O connectors. The RESET signal is a slow-speed signal and does not require the series termination used with LINK_STATUS.

Clock Signals

Six signals are available at the I/O connectors that are used as clocks in some form. Two of these (XMITCLOCK and EXTREFCLK) are input/output clocks that are routed through the JP1 jumper block, and three are output clocks.

These clock signals are:

- XMITCLOCK
- EXTREFCLK
- $\overline{RP}$
- $\overline{RDY}$
- RCV_CLK0
- RCV_CLK1

Of the output clocks, the $\overline{RP}$ and $\overline{RDY}$ signals are only available at JP2 and JP3. The $\overline{RP}$ signal is generated in the HOTLink Transmitter and is used for reading data from asynchronous FIFOs, while the $\overline{RDY}$ signal is generated in the HOTLink Receiver and is used for writing data into asynchronous FIFOs. When interfacing to synchronous FIFOs , the $\overline{RP}$ signal is not normally used. Because these signals are not present in JP4, they are not series terminated.

The other two output clocks (RCV_CLK0 and RCV_CLK1) are a buffered form of the recovered CKR clock from the receiver. The RCV_CLK1 signal is an inverted form of RCV_CLK0.

Data Signals

The CY9266 Evaluation Board has two data buses: one input (to the HOTLink Transmitter) and one output (from the HOTLink Receiver).

The input data bus consists of ten parallel transmit data signals that are sampled at the rising edge of the HOTLink Transmitter CKW clock. In addition to these ten signals, $\overline{ENN}$ and $\overline{ENA}$ (while part of the Switched Control signals) may also be considered part of the data bus as they are also sampled at this same time. While the XMIT_BISTEN input is also sampled at this same time, it is not normally used to transfer data and is therefore not considered part of the input data bus.

The output data bus is comprised of ten parallel received data signals that are synchronous to the HOTLink Receiver CKR clock. To meet specific timing requirements for OLC compatibility, there is also an external pipeline register between the HOTLink Receiver data bus output, and the received data bus connected to JP2, JP3, and JP4.

One other signal, BYTE_SYNC, is also clocked through this pipeline register and is thus considered part of the data bus.

All signals on this output bus are series-terminated with a 22Ω inline resistor to minimize transmission line ringing.

Configuration Settings

The CY9266 board may be user-configured to allow many modes of operation. This configuration is performed through the jumper block JP1 and the option select switch S1.

JP1 Jumper Block

The JP1 jumper block is used for configuring those options of the CY9266 that are (primarily) either to protect the board from signal contention, or for those signals having multiple sources and destinations. These functions are:

- Receiver Mode Select
- Receiver Loopback Source Select
- Transmitter Mode Select
- Transmitter FOTO Source Select
- Transmitter Clock (CKW) Source Select
- Receiver Reference Clock (REFCLK) Source Select

JP1 exists as a 2 x 10 matrix of 0.025″ square pins on the top of the board. The rows in this matrix are identified on the top silk screen as A through J. The columns are identified as X and Y. A drawing of the JP1 jumper block is shown in *Figure 5*.

Receiver Mode Select

This jumper ties pins X and Y of JP1-A together. It is used to connect the receiver's MODE select pin to the option select switch (S1-6), and to allow the HOTLink Receiver mode to be set to the clock Test mode (see *Figure 13*). The three modes of receiver operation are:

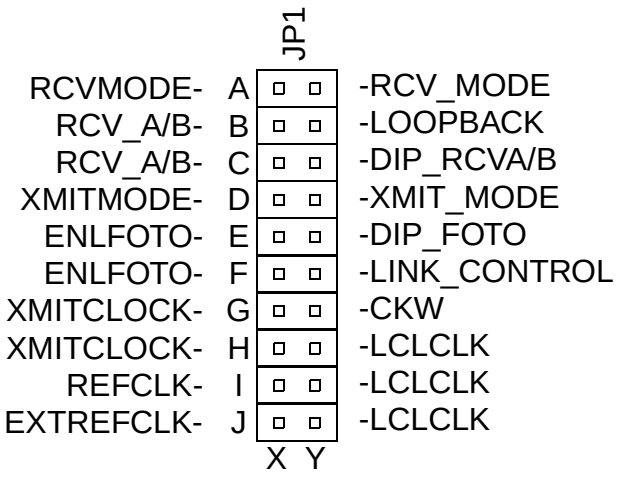


Figure 5. JP1, Top Side View

- Decode Mode—S1-6 ON (closed)
- Bypass Mode—S1-6 OFF (open)
- Test Mode—JP1-A, X and Y open

Because this clock Test mode is not normally used for communications testing, the jumper (JP1-A) is permanently wired in place with a foil trace on the bottom of the board. For those users who wish to actually place the receiver in Test mode, it may be necessary to cut this foil on the back of the board.

Once this foil has been cut, it will be necessary to use a shorting jumper across pins X and Y of JP1-A to allow the two data modes of the receiver to be set by the option select switch (S1-6) and the RCV_MODE signal on JP2 and JP3.

Receiver Source Loopback Select

This function uses two positions (JP1-B and JP1-C) of the jumper block to select the source of the HOTLink Receiver loopback signal. Because this jumper is used to select between one of two sources, only one of these two positions (JP1-B or JP1-C) may contain a shorting jumper at any one time (see *Figures 10* and *11*).

By placing a shorting jumper across pins X and Y of JP1-B, the receiver loopback (A/$\overline{B}$) input is then controlled by the LOOP_BACK signal on JP2, JP3, and JP4. If this shorting jumper is moved to JP1-C, then the receiver loopback input is controlled by the option select switch (S1-7) and the RCV_MODE signal on JP2 and JP3. If a jumper is not present in either position, the INA± path is selected (external serial data).

Transmitter Mode Select

This jumper ties pins X and Y of JP1-D together. It is used to connect the transmitter MODE select pin to the option select switch, and to allow the HOTLink Transmitter mode to be set to the clock Test mode (see *Figure 7*). The three modes of transmitter operation are:

- Encode Mode—S1-2 ON (closed)

- Bypass Mode—S1-2 OFF (open)
- Test Mode—JP1-D, X and Y open

Because this clock Test mode is not expected to be used for normal data communications testing, the jumper (JP1-D) is permanently wired in place with a foil trace on the bottom of the board. For those users who wish to actually place the transmitter in Test mode, it may be necessary to cut this foil on the back of the board.

Once this foil has been cut, it will be necessary to use a jumper across JP1-D to allow the two data modes of the transmitter to be set by the option select switch (S1-2) and the XMIT_MODE signal on JP2 and JP3.

Transmitter FOTO Source Select

This function uses two positions (JP1-E and JP1-F) of the jumper block to select the source of the HOTLink Transmitter FOTO signal. Because this jumper is used to select from one of two sources, only one of these two positions (E or F) may contain a jumper at any one time (see *Figures 8* and *9*).

By placing a shorting jumper across pins X and Y of JP1-F, the HOTLink Transmitter FOTO signal is then controlled by the LINK_CONTROL signal on JP2, JP3, and JP4. If this shorting jumper is moved to JP1-E, then the transmitter FOTO signal is controlled by the option select switch (S1-8) and the DIP_FOTO signal on JP2 and JP3. If a jumper is not present in either position, the transmitter OUTA± and OUTB± differential drivers are placed in a mode where a differential logic 0 is driven.

Transmitter Clock Source Select

The HOTLink Transmitter CKW clock can be sourced from two different signals: LCLCLK from the on-board oscillator and XMITCLOCK from JP2, JP3, and JP4 (see *Figure 7*).

To select the on-board oscillator, a shorting jumper should be placed across pins JP1-GY and JP1-HY. To select the XMITCLOCK signal, this shorting jumper should be moved to connect pins X and Y of JP1-G. To allow the transmitter to operate, it is necessary for a jumper to be in one (and only one) of these two positions.

Receiver Reference Clock Source Select

The HOTLink Receiver REFCLK signal can be sourced from three different signals: LCLCLK from the on-board oscillator, XMITCLOCK (from JP2, JP3, and JP4), and EXTREFCLK (from JP2 and JP3) (see *Figure 13*).

To select the on-board oscillator, a shorting jumper should be placed across the X and Y pins of JP1-I. To select the XMITCLOCK signal, this shorting jumper should be moved to connect pin X of JP1-I to pin X of JP1-H. To select the EXTREFCLK signal (used for PLL range testing), the shorting jumper should be placed across pin X of JP1-I and pin X of JP1-J. To allow the receiver to operate it is necessary for a jumper to be in one (and only one) of these three positions.

S1 Option Select Switch

The S1 Option Select Switch is used for configuring those options of the CY9266 that may be changed on a regular basis or are used to operate the board in a standalone mode. These functions are:

- Transmitter BIST Enable
- Encoder Mode Select
- Enable Next Parallel Transmitter Data
- Enable Parallel Transmitter Data
- Receiver BIST Enable
- Receiver Mode Select
- Receiver A/B Port Select
- Transmitter FOTO Enable
- Signal-Detect Polarity
- Byte Sync Polarity

S1 exists as a 10-position DIP switch. The switch positions (numbered 1 through 10) are identified on the top of the switch. When a switch is on (closed), the signal connected to that switch is tied directly to ground. When a switch is off (open), the signal on that switch is pulled up through a 5-kΩ resistor in R-pack R20.

These signals are also connected to pins on JP2 and JP3 to allow external logic to control these functions. A drawing of the S1 option select switch is shown in *Figure 6*.

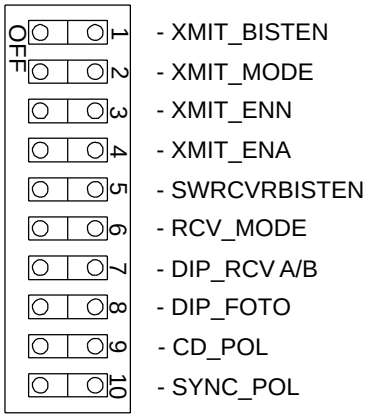


Figure 6. S1 Option Select Switch

Transmitter BIST Enable

Switch S1-1 (XMIT_BISTEN) is used to enable the HOTLink Transmitter BIST function. When this switch is on (closed), the BISTEN input to the transmitter is pulled LOW, placing the transmitter into its BIST loop. The exact patterns transmitted are determined by the levels on the XMIT_ENN and XMIT_ENA signals, located on S1-3 and S1-4 respectively (see *Figure 7*).

Encoder Mode Select

Switch S1-2 (XMIT_MODE) is used to select the data encoding mode of the HOTLink Transmitter. When this switch is on (closed), the internal 8B/10B encoder is enabled and the 8-bit data characters are encoded into 10-bit transmission characters. When this switch is off (open), the encoder is bypassed and the transmitter accepts 10-bit patterns for direct serialization (see *Figure 7*).

Enable Next Parallel Transmitter Data

Switch S1-3 (XMIT_ENN) is used, along with S1-1 (transmitter BIST enable) and S1-4 (XMIT_ENA), to select which data patterns are sent during HOTLink Transmitter BIST operations (see *Figure 7*).

If BIST is enabled (S1-1 on and S1-4 off), setting this switch off (open) causes the transmitter to send an alternating 1-0 pattern (D10.2 or D21.5). When turned on (closed), it enables an internal pattern generator in the transmitter that generates a repeating sequence of 511 10-bit patterns.

For normal data transfer operations this switch should remain off, with the XMIT_ENN signal controlled externally through JP2 and JP3.

Enable Parallel Transmitter Data

Switch S1-4 (XMIT_ENA) is used, along with S1-1 (transmitter BIST enable) and S1-3 (XMIT_ENN), to select which data patterns are sent by the HOTLink Transmitter during BIST operations (see *Figure 7*).

If BIST is enabled (S1-1 on and S1-3 off), setting S1-4 off (open) causes the transmitter to send an alternating 1-0 pattern (D10.2 or D21.5). When turned on (closed), it enables an internal pattern generator in the transmitter that produces a repeating sequence of 511 10-bit patterns.

For normal data transfer operations this switch should remain off, with the XMIT_ENA signal controlled externally through JP2 and JP3.

When operated from the JP4 system connector, this switch should be turned on (closed), because the system hardware is required to provide a valid 10-bit transmission character or data character for each CKW clock.

Receiver BIST Enable

Switch S1-5 (SWRCVBISTEN) is used to enable the HOTLink Receiver BIST function (see *Figure 13*). When this switch is on (closed), the receiver awaits a D0.0 transmission character (sent once per BIST loop). When this character is detected the BIST state machine in the receiver begins matching the following received transmission characters with its internal pattern generator. This pattern generator follows the same sequence of patterns as those sent by the HOTLink Transmitter when sending its BIST sequence.

When this switch is off (open), the HOTLink Receiver operates in one of its two data modes (Decode or Bypass).

Receiver Mode Select

Switch S1-6 (RCV_MODE) is used to select the data decoding mode of the HOTLink Receiver (see *Figure 13*). When this switch is on (closed), the internal 10B/8B decoder is enabled and the received 10-bit transmission characters are decoded into 8-bit data characters. When this switch is off (open), the decoder is bypassed and the receiver outputs 10-bit transmission characters directly to the output data and status pins.

Receiver A/$\overline{B}$ Port Select

Switch S1-7 (DIP_RCVA/B) is used to select which input port (A or B) the HOTLink Receiver should use for receiving serial data (see *Figures 10* and *11*). While the A/$\overline{B}$ input of the receiver is a 100K ECL (emitter-coupled logic) compatible input, it is connected here to allow control from a switch or TTL driver. This requires use of an external resistor network, connected between that input and the select switch, to allow full rail-to-rail swings to be used.

When this switch is on (closed), the INB+ input to the HOTLink Receiver is selected. This input is directly connected to the OUTC+ output from the HOTLink Transmitter. This is the Local Loopback mode for the CY9266 evaluation board that allows the transmitter and receiver to be tested without an external serial data cable or optical module.

When this switch is off (open), the INA± differential input of the receiver is enabled to accept data from the optical module (U4) or copper cable.

Transmitter FOTO Enable

Switch S1-8 (DIP_FOTO) is used to enable the OUTA± and OUTB± differential output drivers of the HOTLink Transmitter. When this switch is on (closed), the differential outputs are allowed to follow the pattern of the data serialized by the transmitter (see *Figures 8* and *9*). When this switch is off (open), the OUTA± and OUTB± differential outputs of the transmitter are driven to a logic zero state (+ output is logic LOW, – output is logic HIGH). This places an attached optical transmitter in a state where no light is output, or presents no transitions on a copper cable.

Signal-Detect Polarity

Switch S1-9 is used to control the active level of the signal-detect output signal, LINK_STATUS. When this switch is on (closed) LINK_STATUS is driven HIGH when a signal is present and LOW when one is not. When this switch is off (open) these levels are reversed (see *Figure 13*).

The signal-detect status is also displayed on one of the decimal point indicators of the two-digit BIST display. When the indicator is on, a signal is present. The state of S1-9 has no affect on the operation of this indicator.

Byte Sync Polarity

Switch S1-10 is used to control the active level of the BYTE_SYNC output signal. This level is also affected by the operating mode of the HOTLink Receiver (S1-6) (see *Figure 13*).

With the HOTLink Receiver in Bypass mode, the BYTE_SYNC signal is used as a K28.5 SYNC character indicator. With SYNC_POL LOW, BYTE_SYNC is LOW when a K28.5 SYNC character is present on the receive data bus. With SYNC_POL HIGH, BYTE_SYNC is HIGH when a K28.5 SYNC character is present on the receive data bus.

With the receiver in Decode mode, the BYTE_SYNC signal is used as a valid data indicator. With SYNC_POL LOW, BYTE_SYNC is LOW whenever a usable data character is present on the receive data bus. With SYNC_POL HIGH, BYTE_SYNC is HIGH whenever a usable data character is present on the receive data bus.

CY9266 Schematic

The complete schematic for the CY9266–F and CY9266–P Evaluation Boards is shown in Appendix A, and the schematic for the CY9266–C and CY9266–T Evaluation Boards is shown in Appendix B.

Sheet 1 of the top-level schematic contains four functional blocks, which are detailed on the remaining pages of the schematic.

Sheet 2 contains the power-supply filtering and bypass capacitors. It also contains a sacrificial Zener diode that is used to protect the components on the board in case of over voltage or incorrect connection of the power supply.

Sheet 3 contains the BIST PLD and the error/status displays.

Sheet 4 of Appendix A contains the HOTLink Transmitter and Receiver, as well as the optical interface module. It also contains the on-board oscillator and option-select DIP switch.

Sheet 4 of Appendix B contains the HOTLink Transmitter and Receiver, as well as the copper interface and signal-detect circuit. It also contains the on-board oscillator and option-select DIP switch.

Sheet 5 contains the parallel interface connectors, the voltage monitor/reset generator, and the OLC-compatibility registers.

Theory of Operation

The CY9266 Evaluation Board operation is broken down into five functional sections:

- Transmitter Parallel Interface
- Transmitter to Optical Module or Copper Serial Interface
- Optical Module or Copper to Receiver Serial Interface
- Receiver Parallel Interface
- BIST and Support Hardware

Transmitter Parallel Interface

The purpose of the transmitter parallel interface is to load parallel data from an external source and move that data to the shifter inside the transmitter. This portion of the design consists of three parts: the transmit data bus, transmitter control signals, and transmitter clocks. A simplified schematic of this interface is shown in *Figure 7*.

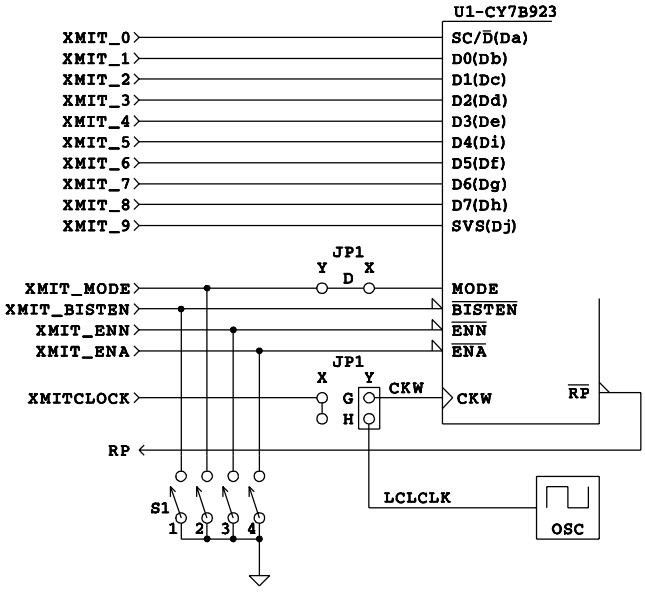


Figure 7. Transmitter Parallel Interface

Transmit Data Bus

The transmit data bus is composed of the ten signals named XMIT_0 through XMIT_9. This bus may be driven from any of three possible sources: JP2, JP3, or JP4. The data present on this bus is sampled by the HOTLink Transmitter (U1-CY7B923) at the rising edge of CKW.

The information present on the transmit data bus is interpreted by the HOTLink Transmitter in one of two ways, based on the setting of the MODE input to the transmitter. When MODE is HIGH (Bypass mode), all ten signals are accepted as the actual data to be transmitted and are fed directly to the shifter. The letter form (Da–Dj, as shown in *Figure 7*) of the bit identifiers is followed for this setting. These designators specify which encoded data bit is connected to a specific XMIT_0 to XMIT_9 signal. In this mode the user must encode the data into the 10-bit patterns used to send data across the serial interface. While it is not necessary to use the 8B/10B code described in the HOTLink datasheet, it is advised that this code be used for simplicity. If another code is used, it is the user's responsibility to insure that sufficient transitions are present in the serial data stream to allow the receiver to properly phase-lock to the serial data stream. For the HOTLink Receiver to provide character framing and synchronization, the K28.5 pattern must be used for framing initialization.

When the MODE input is LOW (Encode mode), the internal 8B/10B encoder is enabled. In this mode the ten input bits are partitioned into eight data bits (D0–D7) and two data-modifier bits (SC/$\overline{D}$ and SVS). For transmitting normal data patterns, both the SVS and SC/$\overline{D}$ pins must be LOW. In this setting the 8-bit data character present on D0–D7 is latched at the rising edge of CKW and presented to the encoder. The encoder then converts the data character into the appropriate 10-bit transmission character. Following conversion, the transmission character is loaded into the shifter.

The two data-modifier bits, SC/$\overline{D}$ (Special Character/Data Select) and SVS (Send Violation Symbol), are used to send transmission characters other than those used to represent data. When the SC/$\overline{D}$ input is HIGH, the normal 8B/10B encoding of the data characters present on D0–D7 is changed. Now special control codes are generated (see listing in the CY7B923/CY7B933 data sheet). These control codes are used to send framing, control, status, and other supervisory functions across the interface.

The SVS pin is used for diagnostic purposes. When this input is HIGH, the HOTLink Transmitter shifter is loaded with a 10-bit pattern that is *not* a valid 8B/10B transmission character. When the HOTLink Receiver detects this encoding violation it responds with its RVS (Received Violation Symbol) output.

Note: The SVS input is intended for diagnostic purposes *only*. If used within normal message traffic, it may cause unexpected receive errors.

Transmitter Control Signals

In addition to the transmit data bus, four other signals are used to control the serial data stream generated by the HOTLink Transmitter. Two of these signals ($\overline{BISTEN}$ and MODE) control operating modes of the transmitter. The other two signals ($\overline{ENN}$ and $\overline{ENA}$) are used to specify when valid data is present on the transmit data bus.

Unlike the transmit data bus, these control signals are not connected to JP4, but are instead connected to JP2, JP3, and separate switches of S1. These switches allow the control inputs to be set LOW or HIGH when an external controller is not present. These switches are used both to control BIST mode for standalone applications and to set the proper operating characteristics for systems which only connect to JP4.

The $\overline{BISTEN}$ and MODE inputs are used to control which transmission characters are generated by the HOTLink Trans-

mitter. Setting $\overline{\text{BISTEN}}$ LOW places the HOTLink Transmitter into one of two auto pattern-generation modes.

When $\overline{\text{BISTEN}}$ is LOW and both $\overline{\text{ENN}}$ and $\overline{\text{ENA}}$ are HIGH, the HOTLink Transmitter sends an alternating 1–0 pattern (D10.2 or D21.5). This pattern provides the highest baseband output frequency that the transmitter can generate, and is equal to 5x the frequency of CKW. This pattern may be useful to test or characterize various serial link components (i.e., fiber-optic modules, jitter tests, etc.).

When $\overline{\text{BISTEN}}$ is LOW and either $\overline{\text{ENN}}$ or $\overline{\text{ENA}}$ is also LOW, the HOTLink Transmitter begins a repeating test sequence that allows the transmitter and receiver to work together to test the functionality of the entire serial link. The repeating sequence is 511 characters in length and includes all standard codes as well as patterns that are normally considered code violations. This sequence may also be useful for performing serial link margin tests.

The MODE input pin is used to select both how the data on the transmit data bus is interpreted (encoded or non-encoded) and to place the HOTLink Transmitter into a clock Test mode. This input is capable of selecting one of these three possible modes from a single pin by use of an internal three-level comparator. These modes are:

- Encode Mode—S1-2 ON (closed)
- Bypass Mode—S1-2 OFF (open)
- Test Mode—JP1-D, X and Y open

When the MODE input is LOW (Encode mode), the internal 8B/10B encoder is enabled. This allows the transmit data bus to be interpreted as an 8-bit data bus (D0–D7) with two control bits (SC/$\overline{\text{D}}$ and SVS). When the MODE input is HIGH (Bypass mode), the internal encoder is bypassed. This allows the data bus to be interpreted as a 10-bit bus (Da–Dj). Either of these modes may be set from JP2, JP3, or S1-2.

The clock Test mode is accessed by allowing the MODE input pin to float. Through use of an internal bias network in the transmitter, the MODE input pin is placed at $V_{CC}/2$. This clock Test mode can be accessed two ways on the board. The easiest is to cut the foil on the bottom of the board that shorts the X and Y pins of JP1-D together. Once cut it will be necessary to place a shorting jumper across these pins to allow JP2, JP3, or S1 to place the transmitter into one of its normal data modes.

The other method of accessing this mode is to actively bias the XMIT_MODE pin on JP2 or JP3 to $V_{CC}/2$. When doing so, keep in mind that this input also has a 5-kΩ pull-up resistor attached to this signal.

The $\overline{\text{ENN}}$ (Enable Next Parallel Data) and $\overline{\text{ENA}}$ (Enable Parallel Data) inputs are normally used to specify when valid data is present on the transmit data bus. Both of these inputs are sampled on the rising edge of CKW at the same time as the 10-bit transmit data bus.

If $\overline{\text{ENA}}$ is LOW and $\overline{\text{ENN}}$ is HIGH at the rising edge of CKW, the data present on the transmit data bus is loaded, processed, and sent to the shifter. If both $\overline{\text{ENA}}$ and $\overline{\text{ENN}}$ are HIGH at the rising edge of CKW, the latched data is ignored and a K28.5 SYNC code is sent in its place.

If $\overline{\text{ENN}}$ is LOW and $\overline{\text{ENA}}$ is HIGH at the rising edge of CKW, the data present on the transmit data bus at the **next** rising edge of CKW is loaded, processed, and sent to the shifter. If both $\overline{\text{ENN}}$ and $\overline{\text{ENA}}$ are HIGH at the rising edge of CKW, the data latched on the next rising edge of CKW is ignored and a K28.5 SYNC code is sent in its place.

These two enable control signals are used to allow different hardware interfaces to be implemented with the least amount (usually none) of additional data pipelining hardware. When one of these enable inputs is used for enable control, the other is usually tied HIGH, but may be used in conjunction with BISTEN for link testing without affecting the data path controller.

Transmitter Clocks

The transmitter interface operates with both an Input Clock (CKW) and an Output Clock ($\overline{\text{RP}}$). The input clock is used to generate both the internal shifter clock and the output clock.

The CKW input clock can be sourced from either the on-board oscillator or from the XMITCLOCK signal. This selection is made through jumper block JP1.

All internal operations of the HOTLink Transmitter are based on the rising edge of the CKW clock. The CKW clock must be generated from a crystal-based source. While the duty cycle of the CKW clock source is relatively unimportant, it must still meet certain minimum pulsewidth times as listed in the CY7B923/CY7B933 data sheet.

The $\overline{\text{RP}}$ output clock pulse is a modified duty cycle pulse whose HIGH and LOW components are set for operation with asynchronous FIFOs (CY7C42X family). The phase relationship of this clock pulse to CKW, and its duty cycle (both set by the internal PLL), are positioned to have valid data on the transmit data bus at the rising edge of CKW.

This $\overline{\text{RP}}$ clock pulse may be directly connected to the read control pin ($\overline{\text{R}}$) of an attached FIFO. Because the presence of this pulse signifies a FIFO read operation, it is only generated in response to the $\overline{\text{ENA}}$ input being pulled LOW.

Transmitter to Optical Module Serial Interface

The transmitter has three differential output pairs that each output the same serial data stream from the shifter. Because of the switching speeds used for these serial outputs (and for compatibility with optical interface modules) they are all implemented using positive-referenced 100K ECL-compatible drivers. A simplified schematic of the interface present on the CY9266–F and CY9266–P is shown in *Figure 8*.

The normal mode of ECL operation is for all signaling to be done at voltages below ground. Because the ground point for ECL is only a reference, the same signaling can also be implemented above ground. When this is done the reference point changes from ground to V_{CC}. When operated in this mode ECL is often referred to as PECL (positive-ECL). This is the mode of operation for the serial outputs on the transmitter.

Two of the differential outputs (OUTA± and OUTB±) are also controlled by a TTL-level enable pin called FOTO (Fiber-Optic Transmitter-Off). This control input is used to disable all light output from the optical module. While not specifically necessary for LED-based optical modules, the ability to disable all light output is a safety requirement for all laser-based links (ANSI Z136.1 and Z136.2, F.D.A. regulation 21 CFR subchapter J, and IEC 825). When FOTO is HIGH, the OUTA± and OUTB± differential pairs are forced to a logic 0 state (OUT+ is LOW and OUT– is HIGH). When FOTO is LOW, the

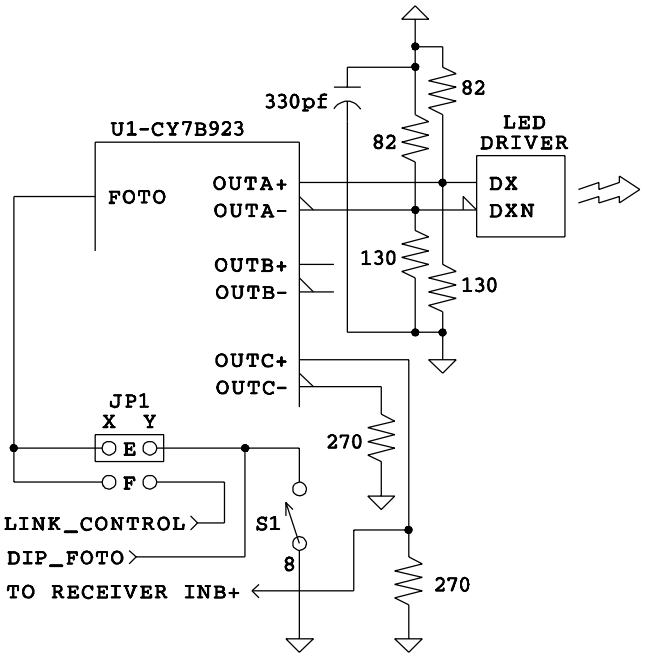


Figure 8. HOTLink Transmitter-to-Optical Serial Interface

OUTA± and OUTB± differential outputs are allowed to follow the serial data pattern from the shifter.

The FOTO pin on the HOTLink Transmitter may be configured to be controlled from either the JP2, JP3, or JP4 connectors (LINK_CONTROL) or from S1-8 (DIP_FOTO). To avoid possible signal contention from these sources, this signal is first run through jumper block JP1.

Placing a shorting jumper across the X and Y pins of JP1-F allows the transmitter FOTO pin to be controlled from the LINK_CONTROL signal. Moving this jumper to JP1-E allows this selection to be made through S1-8 or through the DIP_FOTO signal on JP2 and JP3. If the jumper is omitted from the board, the OUTA± and OUTB± outputs are placed in the disabled state.

The OUTC± differential output is not controlled by FOTO. This output continues to follow the serial shifter data at all times. Because it is never disabled, this signal is used for the local loopback. While this signal is available differentially, it is connected to the receiver single-ended. This allows the INB– input on the receiver to be used as an ECL-to-TTL translator for the receive optical module's signal-detect signal.

Because ECL signals are only *active* in one direction, it is necessary to provide a bias/load network of some type for the signals to properly switch. The typically specified load for ECL signals is 50Ω connected to V_{CC} – 2V (i.e., +3V for PECL).

This type of load can be created in many ways. For large ECL systems a separate power supply is usually present to generate this bias voltage. This provides the lowest power dissipation. For small systems (like this one), a simpler method is to use two resistors to create a network whose Thévenin equivalent is this same 50Ω connected to V_{CC} – 2V. This is used for the OUTA± differential pair. The capacitor present across the Thévenin pair is necessary to produce an AC short between the power and ground planes.

The OUTB± output pair is not used on this evaluation board. While normal ECL drivers left in this mode would still dissipate a significant amount of power, the HOTLink ECL outputs contain additional internal structures to sense if an output is used or left open, and disables the internal current sources of unused output drivers. This results in a current savings of approximately 5 mA (25 mW) for each unused output pair.

The OUTC± output pair is biased to V_{CC} – 5V (ground) through 270Ω resistors. This bias arrangement is used here to reduce the overall component count. This type of load may be used for short connections because it provides a similar current load to a Thévenin termination but, due to asymmetric rise and fall times, it induces more jitter into the data. This type of biasing should not be considered as a type of line termination. If the switching speeds and length of circuit traces dictate that the line should be terminated, a Thévenin bias network should be used to match the line impedance.

Even in those cases where the connection to the optical modules is short and a 270Ω resistor to V_{CC} – 5V may seem to be usable, it should not be used. While this type of connection may work for very short optical cable lengths, the jitter introduced by the bias network reduces the overall system jitter margin.

Transmitter to Copper Cable Serial Interface

On the CY9266–C and CY9266–T boards, the transmitter output is configured to drive either a coaxial or shielded-pair cable. A simplified schematic of this interface is shown in *Figure 9*.

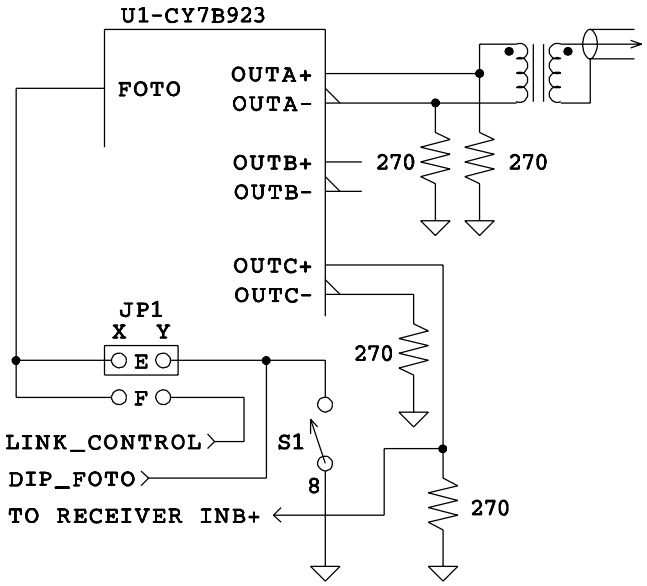


Figure 9. HOTLink Transmitter to Copper Serial Interface

The copper-based CY9266–C and CY9266–T boards use a transformer-coupled interface. Transformer coupling is supported in the ANSI Fibre Channel standard for copper-based interfaces. Its primary advantages are excellent common mode rejection, balanced-to-unbalanced conversion (for coaxial cables), and DC isolation (up to 2 kV hi-pot tested).

The CY9266–C and CY9266–T boards are designed to allow other modes of line biasing and coupling to be used for pre-

senting a signal into the cable. Pads are present on the board to allow a Thévenin bias to be used on OUTA±. These resistor locations are identified as R72 and R73 on Sheet 4 of the CY9266–C/T schematic (see Appendix B).

The CY9266–C and CY9266–T are designed to operate with cable systems providing a reflection coefficient of zero. This means that the receiving end of the cable should be terminated in the characteristic impedance of the cable.

Pads are also present to allow both source termination and capacitive coupling to the transformer. These components are identified as R54, R55, C25, and C26 on Sheet 4 of the CY9266–C/T schematic (see Appendix B). To use parts in these locations it is necessary to remove the foil shorts across the pads for these components on the circuit board.

The control signal inputs for copper-based interfaces operate identically to those of the optical interface. The difference in operation is that when the OUTA± outputs are disabled through the use of the FOTO signal, instead of disabling all light, all output transitions are disabled.

Optical Module to Receiver Serial Interface

The HOTLink Receiver has two differential input pairs (INA± and INB±) that can both be used to receive the high-speed serial data streams generated directly by the transmitter or as output from an optical receiver. These serial inputs are also PECL and are directly compatible with the HOTLink Transmitter. ECL was chosen for these signals for the same reasons (speed, low noise, compatibility with optical modules) it was used for the transmitter.

A separate PECL input signal (A/$\overline{B}$) is used to select which input pair (INA± or INB±) is actually fed to the receiver shifter and PLL. A simplified schematic of the optical module-to-receiver serial interface on the CY9266–F/P is shown in *Figure 10*.

Optical Module Signals

The optical receiver generates two signals; a 100K PECL differential received data signal, and a single-ended signal-detect signal. While the DIP package form of the optical module does provide both + and – forms of the signal-detect signal, only the + form is available on the endfire package. To allow the same circuitry to be used with either module type, only the + signal-detect signal is used.

Receiver Data Inputs

The HOTLink Receiver differential INA and INB inputs are similar, but not identical. While the INA± inputs must always operate as a differential pair, the INB± signals do not. This allows the INB± inputs to be split into two separate ECL inputs: INB+, which feeds the shifter and PLL, and INB–, which feeds an ECL-to-TTL translator.

The configuration of the INB± inputs is controlled by the SO output of the translator. While technically an output, the SO pin on the HOTLink Receiver also contains sense circuits that monitor the voltage level on the pin during power-up. If the SO output is connected to V_{CC}, the INB– input becomes part of the INB± differential serial input. If the SO output is normally loaded (no resistive pull-up to V_{CC}), the INB+ input becomes a single-ended serial data receiver and the INB– input becomes part of a PECL-to-TTL translator.

This split mode is used on the CY9266 Evaluation Board. It allows the INB– input to be used to convert the PECL signal-detect output of the optical module (SIGO) to the TTL-level signal needed on the receiver parallel interface.

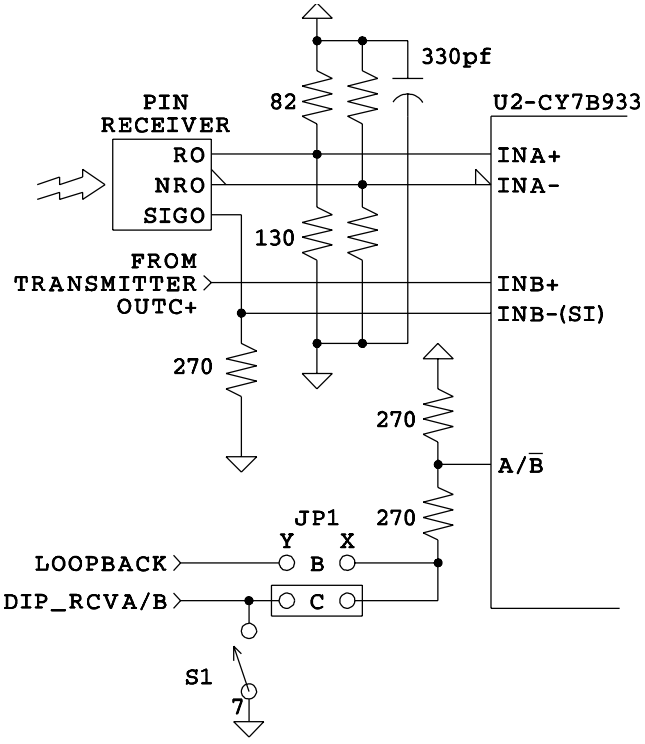


Figure 10. Optical-to-HOTLink Receiver Serial Interface

Receiver Port Select

The HOTLink Receiver uses a single-ended PECL input (A/$\overline{B}$) to control which serial input is fed to the shifter and PLL. When the A/$\overline{B}$ input is HIGH, the differential INA± pair is connected to the shifter and PLL. When the A/$\overline{B}$ input is LOW, the INB+ input is fed to the shifter and PLL. Because the INB+ input is directly connected to the OUTC+ output from the HOTLink Transmitter, this LOW setting is used for a local loopback and allows the transmitter and receiver to communicate without using an optical module.

The A/$\overline{B}$ input is a PECL input and normal TTL or CMOS logic swings will not work to control it. This input uses PECL (or larger) signal swings. These can still be achieved in a TTL environment through use of a resistive divider network as shown in *Figure 10*.

Using this network, a TTL LOW level on the input to the divider creates a PECL LOW at the A/$\overline{B}$ input to the receiver. With a TTL (or CMOS) HIGH into the divider, the A/$\overline{B}$ input is placed at (or above) a PECL HIGH. While standard 100K ECL inputs should never be taken above V_{CC} – 700 mV, the ECL inputs on the HOTLink Receiver may be connected directly to V_{CC} without degradation or damage.

The divider network on this evaluation board may be configured to be controlled from either the JP4 connector (LOOP_BACK) or from S1-7 (DIP_RCVA/B). To avoid possible signal contention from these sources the signal is first run through jumper block JP1.

Placing a shorting jumper across the X and Y pins of JP1-B allows the receiver port selection to be controlled from the LOOP_BACK signal. Moving this jumper to JP1-C allows this selection to be made through S1-7 or through the DIP_RCVA/B signal on JP2 and JP3. If the jumper is left off the board, the A± pair is selected.

Copper to Receiver Serial Interface

The CY9266–C and CY9266–T Evaluation Boards replace the optical module with a transformer-coupled electrical interface. The transformer used here provides the same functionality as the one used at the transmit end of the cable. A simplified schematic of the copper-cable-to-receiver serial interface on the CY9266–C/T is shown in *Figure 11*.

The output side of the transformer connects to two resistors. These resistors provide the line termination for the transmission line connected to the transformer. Two resistors are used for the termination network to allow a reference voltage to be set for the center of the received signal. This reference point is set by an external three-resistor divider, and is set in this circuit to V_{CC} – 1.3V. This is near the center of the common mode range of the MC10H116 ECL receiver that is used to build a signal detection circuit. If this signal-detect circuit is not used, it would be better to bias this point at V_{CC} – 1.5V, the center of the HOTLink Receiver's common mode range.

Both of these reference points must be bypassed to allow them to remain stable under dynamic signal conditions.

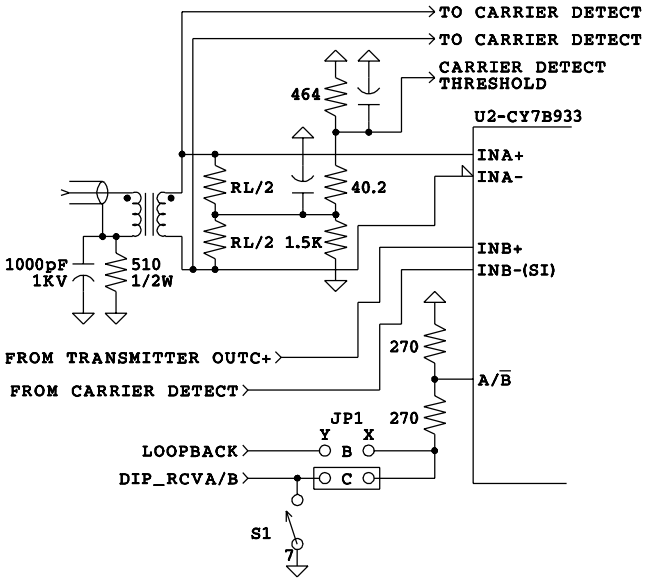


Figure 11. Copper-to-HOTLink Receiver Serial Interface

Unlike the optical receiver, which outputs a logic zero in the absence of light (INA+ = 0, INA– = 1), the AC-coupled interface used for copper connections does not. When the signal is removed, the INA+ and INA– inputs to the HOTLink Receiver are set to the same voltage. Because of the high gain present in the HOTLink Receiver to allow use with long cables (low amplitude received data), the HOTLink Receiver will probably oscillate. This oscillation under a no-signal condition can be corrected by forcing a small offset between the INA+ and INA– inputs, however, this offset will induce more jitter into the data stream and limit the usable length of a copper-based serial link. Rather than compromise operational length, a signal detection circuit can be added to validate the received data (in addition to the validation mechanisms present in the data itself).

The CY9266–C and CY9266–T boards also contain the pads and routing necessary for implementing an equalizer to allow longer cables to be used. The function of an equalizer is to present a frequency selective attenuation to the received signal that brings the amplitude and phase of the frequency components in that signal into the same amplitude and phase. Because signals transmitted over copper cables are effectively run through a high-frequency attenuator, the equalizer used for copper cables is a form of low-frequency attenuator (high-pass filter).

The equalizer is implemented in a bridged-H configuration that is designed for balanced line operation. It is shown on Sheet 4 of the CY9266–C schematic in Appendix B and is constructed using R64, R65, R66, R67, R68, R69, R70, R71, C29, C30, and L1. To implement this equalizer it is necessary to remove the foil shorts across R64 and R71.

Copper Signal-Detect

The signal-detect circuit used on the CY9266–C and CY9266–T boards is shown in *Figure 12*. This circuit uses two ECL s agreceivers as level comparators to detect the presence of 1- and 0-level pulses on the incoming signal. The gate connected to the top side of the transformer (shown in *Figure 11*) detects the presence of received 1 pulses while the gate connected to the bottom of this transformer detects the presence of received 0 pulses. The input capacitance of these comparators is isolated from the actual received signal through 100Ω resistors to prevent this additional load from distorting the received signal.

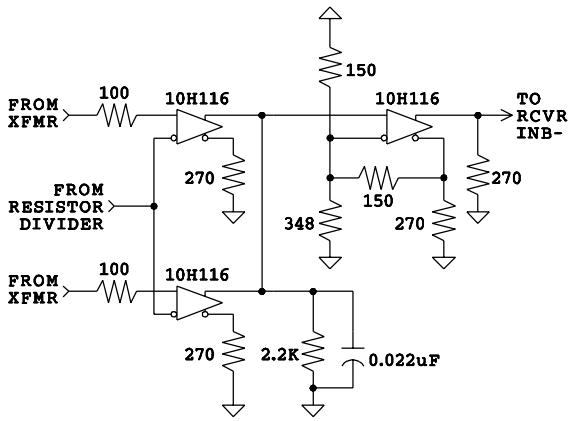


Figure 12. Copper Interface Signal-Detect

The input signal amplitude necessary to detect either a 1 or a 0 is set by the three-resistor divider shown in *Figure 11*. To prevent the 10H116 gate from oscillating it is recommended that this threshold be set to a minimum of 50 mV above the termination reference voltage.

The outputs of these two gates are then wire-ORed together to charge a capacitor. Because of the low on resistance of the

emitter follower output transistors of the 10H116 gates, the capacitor can be charged quite quickly. In the absence of 1 or 0 transitions above the set threshold level, this capacitor is discharged both by a bleeder resistor to V_{EE}, and through the input of the third gate.

The third gate is configured as a comparator with feedback to form a Schmitt trigger. This feedback is necessary because of the slow transition rate of the input signal to this gate. If feedback was not used, this gate would oscillate as the input signal slowly passes through the threshold region of the gate. The output of this Schmitt trigger is then connected to the HOTLink Receiver INB– input, which is configured as a PECL-to-TTL translator.

Receiver Parallel Interface

The receiver parallel interface is used to move the character framed in the HOTLink Receiver to the external world where it can be used. This portion of the design consists of five sections: receiver parallel data output, OLC-compatibility registers, receiver clocks, receiver control inputs, and receiver status outputs. A simplified schematic of this interface is shown in *Figure 13*.

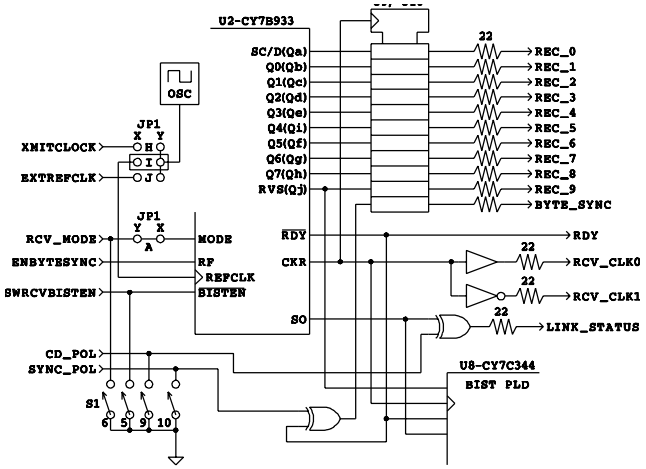


Figure 13. HOTLink Receiver Parallel Interface

Receiver Parallel Data Output

The receiver data bus is composed of ten signals named REC_0 through REC_9. This bus drives all three I/O connectors (JP2, JP3, and JP4). Due to the external register in the data path, these outputs change coincidental with the rising edge of RCV_CLK0 (CKR).

The information placed on the receiver data bus is determined by the HOTLink Receiver MODE select pin. When MODE is HIGH (Bypass mode), all ten outputs are the ten bits that were received and framed. The letter form (Qa–Qj, as shown in *Figure 13*) of the bit identifiers is followed for this setting. These designators specify which encoded data bit is connected to a specific REC_0 to REC_9 signal. In this mode the user must decode the data from the 10-bit patterns used to send the data across the serial interface.

While it is not necessary to use the 8B/10B code described in the HOTLink data sheet, it is advised that this code be used for simplicity. If another code is used, it is the user's responsibility to insure that sufficient transitions are present in the data stream to allow the HOTLink Receiver to properly phase-lock to the serial data stream.

For the HOTLink Receiver to maintain character framing and synchronization, the K28.5 pattern must also be used for framing initialization. For those systems that perform their own framing (SONET, SMPTE, etc.), the HOTLink Receiver will phase-lock to a serial data stream without K28.5 codes present and clock out a character every 10 bit-clocks. These systems must operate in Bypass mode as the HOTLink Receiver decoder requires operation with the 8B/10B code and must acquire character sync to recover valid data. These systems must provide external character framing.

When the HOTLink Receiver MODE input is LOW, the internal 10B/8B decoder is enabled. In this mode, the ten output bits from the shifter are sent to the decode register once every ten bit-clocks, as determined by the framer. The 8-bit output from this decoder is then placed on the receiver output data bus bits Q0–Q7, along with the two data status bits SC/$\overline{D}$ and RVS.

When receiving normal data patterns, both the RVS and SC/$\overline{D}$ pins are LOW. In this setting, the 8-bit data character present on Q0–Q7 is latched at the rising edge of CKR into the external register and presented to the output of the board.

The two status bits, SC/$\overline{D}$ (special character/data select) and RVS (received violation symbol), are used to indicate reception of characters other than those used to represent data. When the SC/$\overline{D}$ output is HIGH, special control codes (see listing in the CY7B923/CY7B933 data sheet) have been decoded. These control codes are used to indicate framing, control, status, and other supervisory functions across the interface.

The RVS pin is used for diagnostic purposes. When this output is HIGH, the HOTLink Receiver decoder has detected a 10-bit pattern that is **not** a valid 8B/10B transmission character or sequence. When the receiver detects this encoding violation, it asserts RVS and places information on the Q0–Q7 outputs to represent the type of error detected. Because all of these errors are represented with special codes (C0.7, C1.7, C2.7, and C4.7) the SC/$\overline{D}$ output is always HIGH whenever RVS is HIGH. These possible error-type codes are listed in the HOTLink datasheet.

OLC-Compatibility Registers

In order for this evaluation board to operate in an OLC-266 compatible system, the timing of the $\overline{RDY}$ signal has to be modified. This signal from the receiver is used for four functions: to indicate when a K28.5 SYNC character has been received, to indicate that valid data has been received, to clock valid data into an external asynchronous FIFO, and to indicate the end of a BIST loop.

To support these different functions from a single pin requires the addition of a single register to convert the waveform generated by the $\overline{RDY}$ signal into the BYTE_SYNC status signal the OLC card generates. Additional registers were then added to the data bits to keep them in the same character-phase relationship as the BYTE_SYNC signal (which is now delayed one clock).

Note: The CY7B9331 HOTLink receiver (rather than the CY7B933 receiver used on the CY9266 Evaluation board) is normally used in systems requiring OLC-266 compatibility. This special HOTLink receiver provides alternate timings and

logic levels for those signals that are different from the default signals on an OLC compatible interface. This allows an OLC interface to be implemented without additional registers or inverters.

The 22Ω series termination present on these signals should not be necessary for most systems, but are added here to allow a flat-cable-type attachment to this card.

Figure 14 shows the relative timing relationships between the HOTLink Receiver data, the $\overline{RDY}$ signal, the BYTE_SYNC signal, and the output clocks. For $\overline{RDY}$ to operate in this fashion, the RF (Reframe enable) control input must be HIGH and the receiver must be in Bypass mode (receiver MODE is HIGH).

When RF is LOW, the $\overline{RDY}$ and BYTE_SYNC outputs operate the same as that shown in *Figure 14*. The difference is that the clocks are not allowed to change phase or width upon detection of a K28.5 SYNC character.

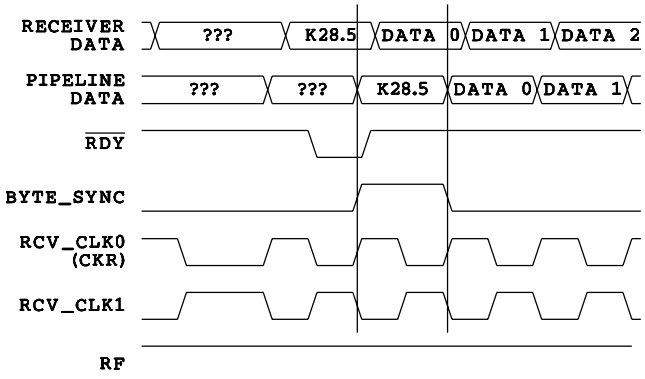


Figure 14. Receiver Data Timing, Bypass Mode, RF HIGH

The functionality of the $\overline{RDY}$ (and thus BYTE_SYNC) signal changes when the receiver is in Decode mode (receiver MODE is LOW). Here the $\overline{RDY}$ signal pulses LOW for every character received *including* the K28.5 SYNC character. When multiple consecutive SYNC characters are received, $\overline{RDY}$ is inhibited except for the last K28.5 character received. This is done to prevent overfilling a receiver FIFO with non-data information. *Figure 15* shows the relative timing relationships for this type of operation.

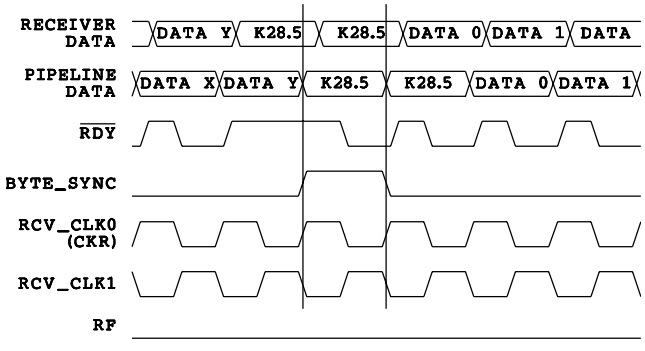


Figure 15. Receiver Data Timing, Decode Mode, RF LOW

Because RF is LOW in *Figure 15*, the CKR clock (and thus RCV_CLK0 and RCV_CLK1) is not allowed to reframe on new K28.5 SYNC characters detected. When RF is HIGH in Decode mode, the HOTLink Receiver $\overline{RDY}$ output ceases pulsing until the first K28.5 SYNC code is detected, after which the behavior shown in *Figure 15* is resumed.

Receiver Clocks

The HOTLink Receiver parallel interface (see *Figure 13*) operates with a single input clock (REFCLK) and two output clocks (CKR and $\overline{RDY}$).

The REFCLK input clock does not directly clock anything in the receiver, but is used as a reference for the receiver PLL. This clock is required to be both stable and reasonably accurate. It must match the character-rate frequency of the received data within ±0.1%. Unlike an OLC card, which requires a special sequencing of the LOCK_TO_REF signal to allow the receiver to track to a reference clock, the HOTLink Receiver PLL continuously operates in a mode that compares its frequency to that of the reference clock, even when valid data is being received.

If the frequency of the received data varies outside of specific fixed limits, the HOTLink Receiver stops locking to the serial data and reverts to the REFCLK. Once the received serial data stream returns to an acceptable frequency, the PLL again locks to the received data. Since it is likely that character sync has been lost, a reframe cycle should be performed to allow the framer to lock up again. Detection of this and the recovery process is normally handled automatically by higher-level functions in the communications system.

The REFCLK input to the receiver can be sourced from three different signals on the evaluation board: the on-board oscillator, the XMITCLOCK input, or the EXTREFCLK input. Selection of the clock source can only be done through jumper block JP1.

The on-board oscillator is used primarily for standalone operation and testing using the BIST capabilities of the HOTLink parts. This clock is selected by placing a shorting jumper across pins X and Y of JP1-I.

The XMITCLOCK input is used for normal data transmit/receive functions and for OLC-compatibility mode. This clock is selected by placing a shorting jumper across pins JP1-HX and JP1-IX.

The EXTREFCLK input is used for those instances when the transmitter and receiver are to be clocked with different frequency clocks. This is expected to be used only to test for PLL capture/lock range testing of the receiver, or when the HOTLink Receiver is connected to a transmitter operating at a different frequency from the local HOTLink Transmitter. This clock is selected by placing a shorting jumper across pins JP1-JX and JP1-IX.

The CKR output clock is generated in the HOTLink Receiver and is based directly on the internal PLL frequency. This output is synchronous with the receiver output data bus and may be used to clock the data into an associated register (as is done on this board) or into synchronous FIFOs.

The period and duty cycle of the CKR output clock are fixed by the logic in the receiver. To achieve compatibility with OLC-type systems, the CKR signal is used to generate two new clock signals (RCV_CLK0 and RCV_CLK1) that are true and complement copies of the CKR clock. To keep matched delays and to minimize the number of additional logic pack-

ages on the board, these two clocks are generated using XOR gates.

When framing occurs, the CKR clock can experience large phase changes. These changes are exhibited by a lengthening of either the HIGH or LOW portion of the CKR waveform. This can be seen in the waveforms shown in *Figure 14*. While this functionality is not required by the ANSI Fibre Channel Standard, it is included in the HOTLink Receiver to protect downstream clocked logic from the narrow pulses or glitches that can occur otherwise.

The $\overline{RDY}$ output signal is used both as a status output and as a clock. Its use as a clock is primarily for clocking data present on the receiver data bus outputs into asynchronous FIFOs. The duty cycle of the $\overline{RDY}$ pulse and its position relative to the output data is such that it may be directly connected to the $\overline{W}$ (write) input on CY7C42X FIFOs.

Receiver Control Inputs

The receiver parallel interface is controlled by three input signals: RF (Reframe), MODE (Receiver Mode select), and $\overline{BISTEN}$ (BIST Enable).

The RF input is used to select when the HOTLink Receiver is allowed to reframe (acquire character-sync) to the incoming serial data stream. This input is present to prevent the receiver from mis-framing on aliased K28.5 SYNC codes, which would cause long running decode errors.

When RF is LOW the framer is disabled; it does not change the starting bit location of each received character. Any received K28.5 SYNC code is treated as normal data and is clocked out with the CKR and $\overline{RDY}$ clocks. If this SYNC code is received across two character boundaries, the framer does not reframe. If the HOTLink Receiver is operating in Decode mode, the existence of such a non-aligned pattern may generate one or more characters in error.

When RF rises, the $\overline{RDY}$ output is inhibited. With RF held HIGH, the framer continuously monitors the serial data stream for either disparity form of the K28.5 SYNC character. When this character is detected, the bit counter used to count off serial data bits and specify received character boundaries is asynchronously reset to properly frame the subsequently received bits on character boundaries.

If the receiver is set to Decode mode, the $\overline{RDY}$ output assumes its normal function of pulsing LOW for each character after the first K28.5 SYNC code is detected. If the receiver is instead set to Bypass mode, the $\overline{RDY}$ signal pulses LOW only for the SYNC (K28.5) characters while RF is HIGH or LOW.

Because of characteristics of the 8B/10B code, it is possible to transmit legal character sequences that can cause incorrect framing (this requires sending control codes other than K28.5). These codes should be avoided while RF is HIGH. Once the framer is disabled (RF LOW) these sequences may be used to pass control information across the interface without causing the receiver to incorrectly frame the data that follows.

The MODE input pin on the HOTLink Receiver is used to select both how the received serial data is to be presented on the data bus (encoded 10-bit character or decoded 8-bit character), and to place the receiver into a clock Test mode. This input is capable of selecting one of these three possible modes from a single pin through use of an internal three-level comparator.

When the MODE input is LOW, the internal 10B/8B decoder is enabled (Decode mode). This allows the receiver output data bus to be interpreted as an 8-bit data bus (Q0–Q7) with two status bits (SC/$\overline{D}$ and RVS). When the MODE input is HIGH, the internal decoder is bypassed (Bypass mode). This allows the data bus to be interpreted as a 10-bit bus (Qa–Qj). Either of these modes may be set from JP2, JP3, or S1-6.

The clock Test mode is accessed by allowing the MODE input pin to float. Through use of an internal bias network in the receiver, the MODE input pin is placed at $V_{CC}/2$. This clock Test mode can be accessed two ways on the board. The easiest is to cut the foil on the bottom of the board that shorts the X and Y pins of JP1-A together. Following this, it will be necessary to place a shorting jumper across these pins to allow JP2, JP3, or S1-6 to place the receiver into one of its normal data modes.

The other method of accessing this mode is to actively bias the RCV_MODE pin on JP2 or JP3 to $V_{CC}/2$. When doing so, keep in mind that this input also has a 5-kΩ pull-up resistor attached to the signal.

The $\overline{BISTEN}$ input pin is used to place the HOTLink Receiver in a special pattern verification mode. This mode is designed to work in conjunction with a matching pattern generation mode in the transmitter. While not shown on the schematic in *Figure 13*, the $\overline{BISTEN}$ input is actually run through the BIST PLD (U8-CY7C344). This is not necessary but is done here to allow other conditioning of the $\overline{BISTEN}$ signal if desired.

When the HOTLink Receiver $\overline{BISTEN}$ input is set LOW, the receiver's BIST state machine is enabled and enters its self-test mode. At this point it sets $\overline{RDY}$ HIGH and begins looking for the BIST start-of-loop character (D0.0) in the serial data stream. Once this character is detected, the $\overline{RDY}$ output is driven LOW, where it remains until the end of the 511-character BIST loop. At this point $\overline{RDY}$ pulses HIGH for one character and starts the next 511-character loop.

While BIST mode is enabled, the RVS output is used to indicate that a pattern mismatch has occurred. This means that the 10-bit pattern received did not *exactly* match the 10-bit pattern that was expected (expected code violations are not errors).

Receiver Status Outputs

The HOTLink Receiver parallel interface generates two status output signals: $\overline{RDY}$ and SO.

The $\overline{RDY}$ output is used both for status information and as a clock. As a status output, its information is valid at the rising edge of CKR. This means that the $\overline{RDY}$ signal must be registered to present its status information. For normal data transfer modes, the registered form of $\overline{RDY}$ is used to identify the presence of multiple K28.5 SYNC characters (HIGH at rising edge of CKR) and of data or control characters (LOW at the rising edge of CKR). This registered form of $\overline{RDY}$ generates the BYTE_SYNC signal.

The $\overline{RDY}$ signal is also used to identify what phase the HOTLink Receiver BIST mode is in. When HIGH for two or more CKR clocks, the receiver is looking for the start character of the BIST loop. When LOW, the receiver is in the BIST loop. When HIGH for a single clock, the receiver has completed another BIST loop.

The SO output is used as part of an ECL-to-TTL translator to specify the current state of the signal on the serial interface,

and is used to drive the LINK_STATUS signal. When a valid signal is present and S1-9 (CD_POL) is off (open), LINK_STATUS is LOW. This polarity is reversed by turning S1-9 on (closed) or pulling SYNC_POL LOW.

BIST and Support Hardware

The CY9266 Evaluation Board contains not only those components necessary to form a serial link, but also a few support components to enhance OLC compatibility and to support the BIST capability in the HOTLink Transmitter and Receiver. A simplified schematic of these additional components is shown in *Figure 16*.

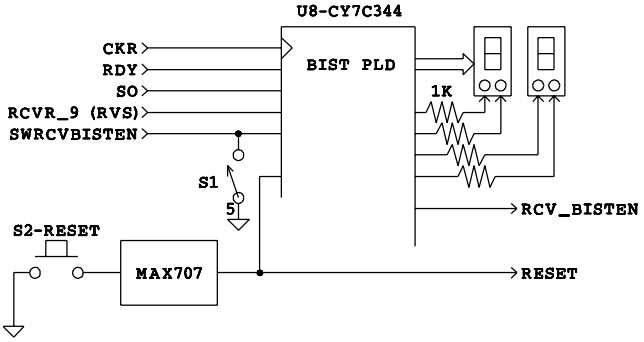


Figure 16. BIST Support Hardware

The MAX707 is used to monitor the power-supply voltage and remove the RESET signal when V_{CC} is above 4.65V. This is a close approximation to the 4.75V RESET threshold specified for the OLC card. This part also supports an external mechanical switch input that also controls the RESET output. This input is controlled by the BIST reset push-button switch (S2). When this switch is depressed, the RESET output is driven LOW until 200 ms after the switch is released. This RESET signal is used to clear the BIST error-counter located in the BIST PLD (U8). The PWR ON indicator is extinguished as long as RESET is active.

The BIST PLD is a Cypress CY7C344 MAX EPLD programmed with the counters and state machines necessary to monitor the status of the receiver outputs and count when BIST-compare errors are detected. This PLD also drives the decimal points on the attached displays to indicate four status signals. These status signals are:

- PWR ON—Lit when power is present and above the 4.65V sense threshold
- CAR DET—Lit when a valid signal is present
- BIST WAIT—Lit when BIST is enabled but the receiver has not detected the start of the BIST loop
- BIST OVFL—Lit when the BIST error count exceeds 99

BIST State Machine

The BIST state machine has six states that control when a counter is enabled to count pattern-match errors. A bubble diagram of this state machine is shown in *Figure 17* while the MAX+PLUS source file for this state machine is listed in Appendix C.

This state machine controls when the error counter is enabled to count. It operates off of two input signals: BISTEN and $\overline{RDY}$. Whenever BISTEN is not present, the machine is returned to the WAIT0 state (while all state transition arrows are shown for these transitions, not all of them are labeled).

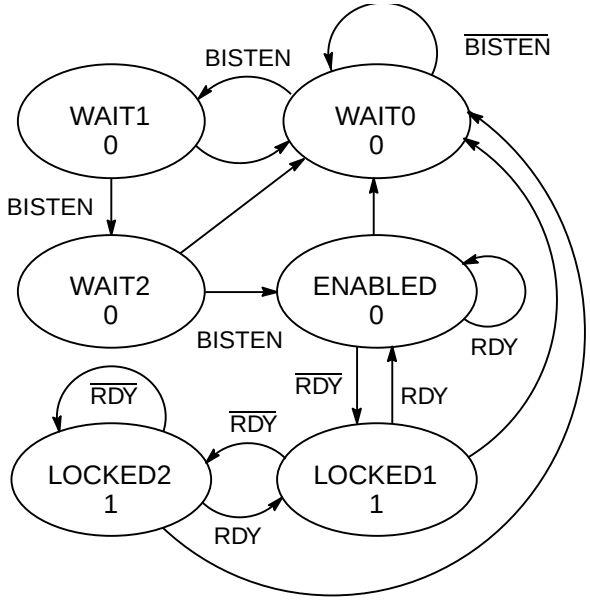


Figure 17. BIST State Machine Bubble Diagram

Once BISTEN becomes active, the machine goes through two secondary wait states (WAIT1 and WAIT2) before starting to look for $\overline{RDY}$ being active. These wait states are necessary to allow the receiver time to recognize the BISTEN signal and bring $\overline{RDY}$ HIGH.

When the ENABLED state is reached, the machine remains in this state until $\overline{RDY}$ goes LOW, causing the machine to move to the first of the two LOCKED states. This signifies that the receiver has received the start-of-loop character (D0.0) and is now performing matching of the received data bits to its internal pattern generator.

In the LOCKED states, the external counter is enabled to count errors. The reason two LOCKED states are present is to allow for the single pulse on $\overline{RDY}$ that indicates the end of a BIST loop. If $\overline{RDY}$ is ever HIGH for more than one clock, the HOTLink Receiver has determined that it is no longer in sync with the transmitter and it starts looking for the start-of-loop character again.

Other BIST PLD Functions

The complete schematic for the BIST PLD is shown in Appendix C. Other than the BIST state machine, the other main logic functions present in the part are for driving the four status indicators and the actual error counter.

Error Display

The error display is made from two hexadecimal LED displays (TIL311). These displays are each capable of showing the entire hexadecimal character set (0–9, A–F) as well as having two independent decimal points. These decimal points are used as individual status indicators for the board.

External Serial Interface Connections

The primary difference between the CY9266 card types is in the external high-speed serial interface. Each card type oper-

ates with not only a different media type (optical, coaxial, shielded twisted pair), but also different connectors and cable types.

CY9266–F/P Serial Interface Connections

The CY9266–F/P HOTLink Evaluation Boards implement a fiber-optic-based serial interface. This interface uses industry-standard LASER and LED-based fiber-optic modules that accept SC-type fiber-optic connectors.

Optical Modules

The CY9266–F/P HOTLink Evaluation Boards are designed to operate using *de facto* standard-footprint optical modules. Any optical module meeting the pinout and dimensions of this *de facto* standard (established originally for FDDI) should operate with the CY9266–F/P.

Note: These standard-footprint optical modules are available in a wide range of operating data rates. Because the operating data rate for some of these modules may be outside the 150- to 400-Mbit/second operating range of the HOTLink Transmitter and Receiver, care should be exercised when selecting an optical module.

This footprint supports two types of optical modules: those with four rows of vertical pins, and those with a single row of pins along the bottom edge. In vendor literature these are referred to as DIP, and 1X9 or endfire-type packages.

While specified originally for FDDI, modules meeting this footprint are also available for Fibre Channel and ATM data rates. *Figure 18* shows the mechanical footprint dimensions of this *de facto* standard package.

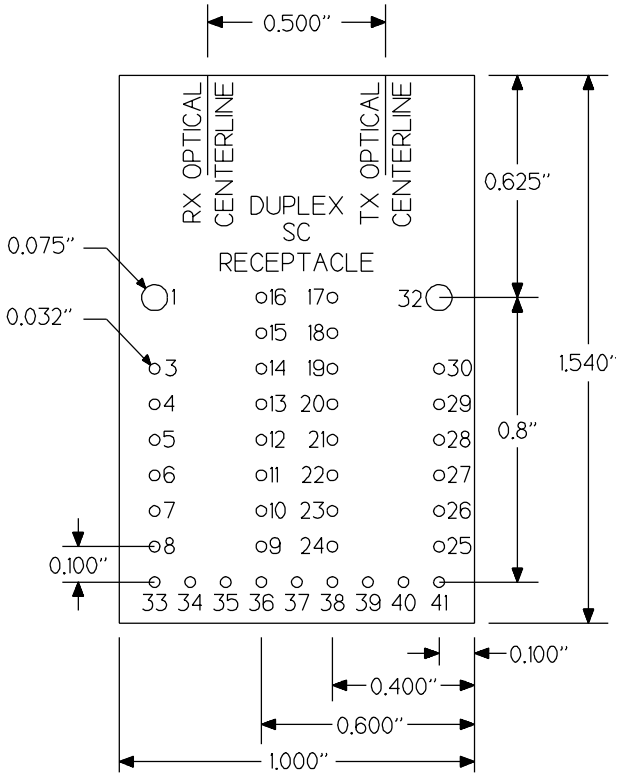


Figure 18. Optical Module, Top View Dimensions

Both package types operate from a +5V supply and interface directly with 100K ECL/PECL. The biggest mechanical difference between them is that the endfire-type packages have two oversized pins (1 and 32) that are used only to hold the package in place. The main electrical difference between the packages types is that the DIP package drives the Signal Detect output differentially while the endfire package only provides the active HIGH output. *Table 5* lists the pinouts for this standard-footprint optical module.

The active signals listed in *Table 5* are:

- SD—Signal Detect
- TD—Transmit Data
- RD—Receive Data
- Case—Outer Case of Module
- V_{CC}—Positive Supply Voltage
- V_{EE}—Negative Supply Voltage

Pins marked "Case" are not necessarily isolated pins. Because the optical module is used in the CY9266–F/P in a PECL mode, these Case pins are connected to the V_{EE} (ground) supply. When selecting an optical module, care should be taken to insure that the pins marked "Case" are either floating or are attached to the appropriate power supply rail.

To allow evaluation of different types of optical modules, the CY9266–F/P Evaluation Board is built using low-profile socket pins for the optical module. This allows the modules to be easily replaced. In addition, two slotted holes are provided for a cable-tie to hold the module in place.

Table 5. Optical Module Pinout

DIP Pin Assignments			
Pin	**Signal**	**Pin**	**Signal**
1	Case	2	No Pin
3	Case	4	V_{EE}
5	V_{EE}	6	+SD
7	–SD	8	Case
9	Case	10	–RD
11	+RD	12	V_{CC}
13	V_{CC}	14	V_{CC}
15	Case	16	Case
17	Case	18	Case
19	V_{CC}	20	V_{CC}
21	Case	22	+TD
23	–TD	24	Case
25	Case	26	V_{BB}
27	Case	28	Case
29	V_{EE}	30	V_{EE}
31	No Pin	32	Case
1X9 (Endfire) Pin Assignments			
Pin	**Signal**	**Pin**	**Signal**
33	V_{EE}	34	+RD
35	–RD	36	+SD
37	V_{CC}	38	V_{CC}
39	–TD	40	+TD
41	V_{EE}		

Fiber-Optic Connector

The optical modules specified for use on the CY9266–F HOTLink Evaluation Board (listed in Appendix A, item U4) are designed to accept SC-type fiber-optic connectors. These connectors are available in both simplex (single-fiber) and duplex (dual-fiber) versions. *Figure 19* shows a simplex SC fiber-optic connector. A duplex connector is formed either by joining two simplex connectors together with a clip (sometimes referred to as a "Z" clip) or by using a connector that supports two fibers in the same form factor. The standard optical fiber type used with these connectors and LED-based optical modules is 62.5/125-mm multimode graded-index fiber.

When using duplex connector cables, the cable construction controls which fiber is connected to the transmit LED and which is connected to the receive photodetector. When using simplex cables, this polarization control is left to the user. The transmit and receive connectors on the fiber-optic module are shown in *Figure 20*.

The optical modules specified for use on the CY9266-P HOTLink Evaluation Board (listed in Appendix A, item U4) are

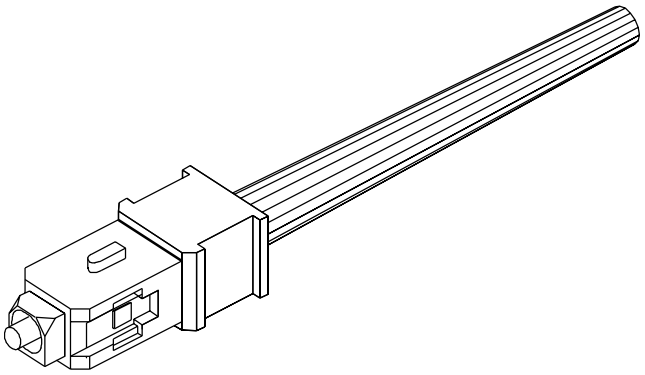


Figure 19. SC Simplex Fiber-Optic Connector

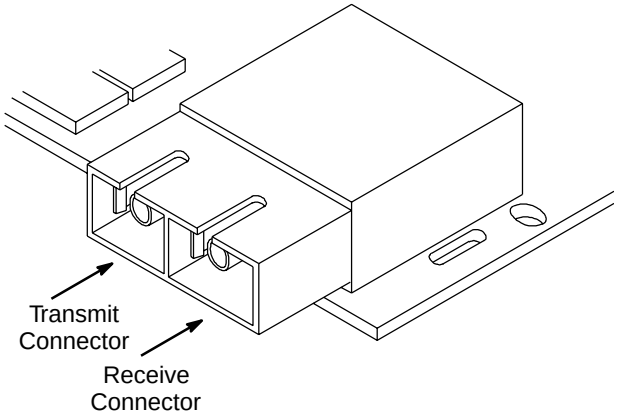


Figure 20. U4 Fiber-Optic Module Connectors

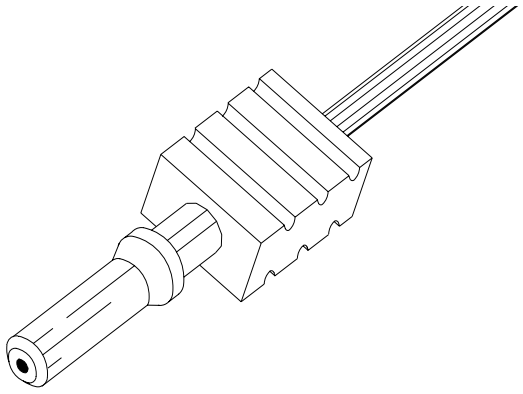


Figure 21. Versatile Link Plastic Optical Fiber Connector

designed to accept Hewlett Packard Versatile Link-type fiber-optic connectors. These connectors are available in both simplex (single-fiber) and duplex (dual-fiber) versions. *Figure 21* shows a simplex Versatile Link fiber-optic connector. A duplex connector is formed either by joining two simplex connector halves together or by using a connector that supports two fibers in the same form factor. The standard optical fiber type

used with these connectors and LED-based optical modules is 1-mm multimode step-index plastic fiber.

Versatile Link connectors offer no specific form of polarization. When used with simplex or duplex connectored cables, polarization control is left to the user. The transmit and receive Versatile Link connectors on the fiber-optic module are shown in *Figure 22*.

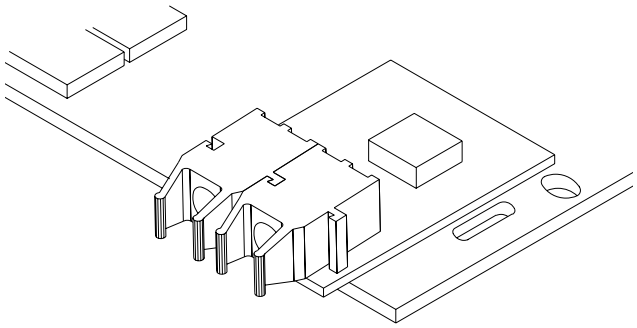


Figure 22. Versatile Link Board Connectors

CY9266–C Serial Interface Connections

The CY9266–C HOTLink Evaluation Board implements a copper-based serial interface. This interface uses 75Ω coaxial cables having BNC- and TNC-type connectors.

Coaxial Board Connectors

The CY9266–C HOTLink Evaluation Board has two right-angle female coaxial cable connectors: a BNC (Bayonet Neil-Councilman) for the J1 transmit connector, and a TNC (Threaded Neil-Councilman) as the J2 receive connector. These connectors and their location on the board are shown in *Figure 23*.

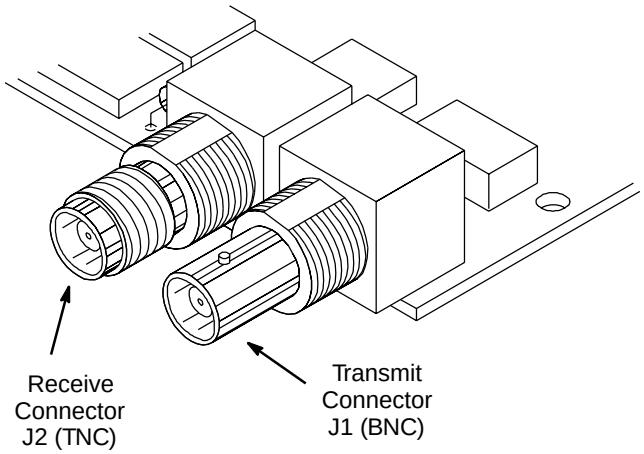


Figure 23. J1 and J2 Coaxial Board Connectors

Coaxial Cable Connectors

Many different coaxial cables may be used with the CY9266–C HOTLink Evaluation Board. The only requirements for the cable are 75Ω characteristic impedance and BNC/TNC connectors at each end to attach to the board. Other cable impedances may also be used, however, the termination (R40 and R41) and bias (R61 and R62) resistors on the board must then be changed for correct operation.

Coaxial cables for the CY9266–C should have a BNC connector on one end and a TNC connector on the other. This dual-connector mechanism is specified by ANSI to prevent the inadvertent cabling of a transmitter to another transmitter, or a receiver to another receiver. When connecting cables to a CY9266–C board, the cable BNC connector always attaches to a transmit port (J1) and the cable TNC connector always attaches to a receiver port (J2). TNC/BNC dual-female barrel connectors (e.g., Amphenol #76400) are available to allow splicing of cables to evaluate multiple lengths of cable. *Figure 24* illustrates typical TNC and BNC connectors.

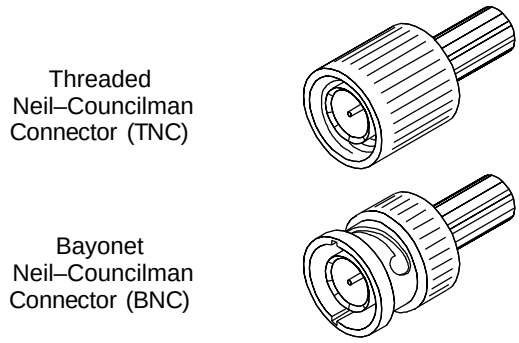


Figure 24. TNC/BNC Cable Connectors

CY9266–T Serial Interface Connections

The CY9266–T HOTLink Evaluation Board implements a copper-based serial interface. This interface uses 150Ω shielded twisted-pair (STP) cables with 9-pin male D-subminiature-type connectors.

STP Board Connectors

The CY9266–T HOTLink Evaluation Board has a right-angle female 9-pin D-subminiature connector. Unlike the coaxial cable version of the CY9266, which uses separate connectors for transmit and receive, the CY9266–T uses only a single connector (P1) for both. This connector and its location on the board is shown in *Figure 25*.

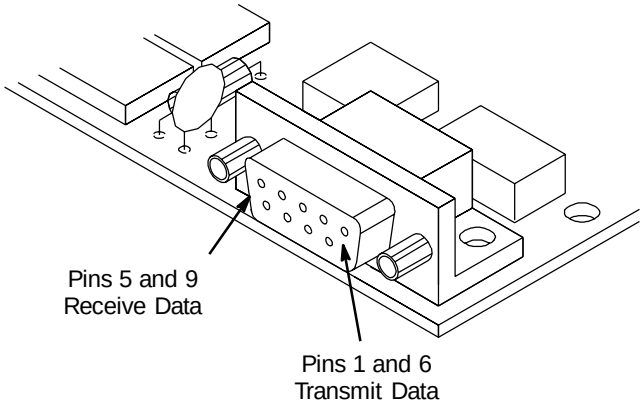


Figure 25. STP P1 Board Connector

STP Cable Connector

There are presently two STP cable types identified by ANSI for use with Fibre Channel; both specify 150Ω differential characteristic impedance. These cable types are known as either EIA/TIA568 Type-1 and Type-2, or more generically as IBM® Type-1 or Type-2. Both of these cable types contain two individually shielded pairs of solid conductors. The Type-2 cable also contains four non-shielded conductors that are often used for either low-speed signaling or voice-grade communications. The CY9266–T also accepts the twinax cable specified for Fibre Channel interfaces, when terminated in style-1 9-pin connectors.

For installations where the cables may see more flexing, a stranded conductor cable is available that meets the 150Ω impedance. This cable type is commonly known as IBM® Type-6. Other cable types may also be used with the CY9266–T HOTLink Evaluation Board. The only requirements for the cable are 150Ω differential characteristic impedance and a properly wired (see *Figure 27*) 9-pin male D-subminiature connector at each end of the cable. Other cable impedances may also be used, however, the termination (R40 and R41) and bias (R61 and R62) resistors on the board must then be changed for correct operation.

Figure 26 shows an example of a compatible STP cable connector and how the pins in the connector are numbered. This is a 9-pin male D-subminiature connector. While connectors of this type are available with a plastic housing, proper operation with STP cables requires using connectors having a metal or conductive shell. When properly connected, as shown in *Figure 27*, the shield of each pair in the cable is attached to the conductive front shell of the connector. To maintain shielding effectiveness it is recommended that the connector backshell/strain relief also be metallic or conductive.

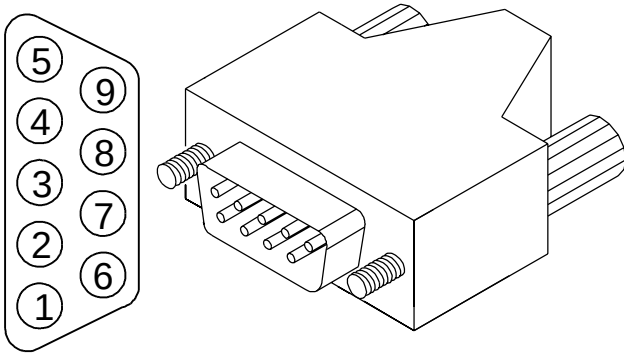


Figure 26. STP Cable Connector and Connector Pinout

The STP cable is wired in a crossover fashion where the transmit connections at one end of the cable are connected to the receive connections at the other end of the cable, as shown in *Figure 27*. The cable shields for both pairs are tied together and connected to the D-sub shell at each end.

OLC Mode Configuration

The CY9266 Evaluation Board may be configured to operate in an OLC-266 compatible system. This emulation is strictly at the TTL parallel interface level; the optical and electrical serial interfaces are not compatible. In addition, the CY9266

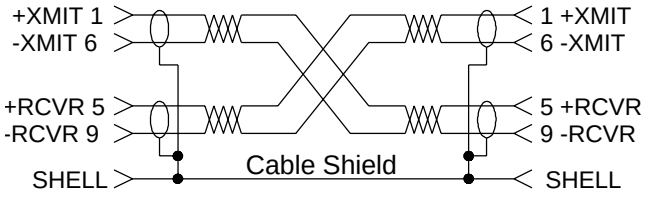


Figure 27. STP Cable Connectors

is only a single-channel board while the OLC-266 is available in either single- or dual-channel versions.

The TTL parallel interface attachment is provided through the JP4 connector. This connector is pinned and positioned to mate with host systems designed for the OLC-266 board.

The following configuration sets the CY9266 for 10-bit data and Bypass mode on both the transmitter and receiver. The transmitter and receiver are both clocked by the XMITCLOCK signal on JP4, and the receiver A/$\overline{B}$ selection is controlled by the LOOP_BACK signal on JP4.

JP1 Settings

The CY9266 jumper block JP1 controls many of the options on the board. For the CY9266 to operate in an OLC socket, jumper block JP1 must be configured with shorting jumpers as shown in *Figure 28*.

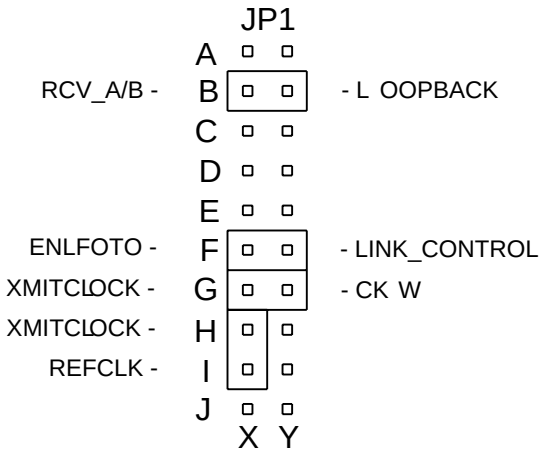


Figure 28. JP1 OLC-Compatibility Settings

The shorting jumper across pins X and Y of JP1-B allows the LOOP_BACK signal in the JP4 connector to control the A/$\overline{B}$ input selection on the HOTLink Receiver. The jumper across pins X and Y of JP1-F allows the LINK_CONTROL signal to control the FOTO enable of the HOTLink Transmitter. The jumper connecting pins X and Y of JP1-G connects the XMITCLOCK input to the HOTLink Transmitter CKW clock. The jumper connecting pins JP1-HX to JP1-IX connects the XMITCLOCK input to the HOTLink Receiver REFCLK input.

Note: The active signal level of the LOOPBACK signal, as implemented on the CY9266, is opposite that of an actual OLC-266 card. If this signal is under software control, it should be programmed to allow signal loopback when the signal is active LOW. For hardware controlled systems an ex-

ternal signal inversion is necessary, or the signal may be jumpered at JP1 for operation from the S1-7 DIP switch.

S1 Settings

The S1 DIP switch is also used to configure many of the HOTLink Transmitter and Receiver options. The settings for these switches are listed in *Table 6*.

The setting of switches S1-7 and S1-8 are not applicable when jumpers JP1-B and JP1-F are in place.

Table 6. S1 OLC-Compatibility Settings

DIP Switch Settings		
Sw #	**State**	**Controlled Signal**
1	Off	Transmitter BIST Enable
2	Off	Transmitter Mode Select
3	Off	Enable Next Parallel Xmit Data
4	On	Enable Parallel Xmit Data
5	Off	Receiver BIST Enable
6	Off	Receiver Mode Select
7	N/A	Switch Controlled Loopback
8	N/A	Switch Controlled FOTO
9	Off	Signal-Detect Polarity Select
10	Off	BYTE_SYNC Polarity Select

Assembly and Options

The design of the CY9266–F/P and CY9266–C/T Evaluation Boards offer many different assembly options for those users interested in making modifications for their own evaluation.

Optical Module

Optical module U4 on the CY9266–F/P is socketed for user evaluation of different optical modules. The hole pattern on the board supports direct soldering of the optical module to the board. This should not be attempted on a board that is already equipped with a socket for the module because removal of the socket pins may damage the board.

Transmitter

The HOTLink Transmitter B± differential output signals on the board are left open to conserve power. Pads are present on the bottom of the board (labeled R1, R2, R3, and R4) for bias/termination resistors for these outputs. While these resistors are present on the board schematic, they are not part of the delivered assembly. If the B± outputs are used for probing or test purposes, resistors must be added in these locations to enable the output drivers.

Oscillator

The on-board oscillator (U5) is used primarily for exercising the BIST capability of the board in a standalone mode. If the board is only used with an external clock, the oscillator does not need to be present. This part is socketed to allow the user to select the operating frequency.

When selecting an oscillator, care must be taken to insure the frequency stability and jitter characteristics of the oscillator are within the specifications of the HOTLink Receiver and Transmitter and the intended system application.

The hole pattern on the board supports direct soldering of the oscillator to the board. This should not be attempted on a board that is already equipped with a socket for the oscillator, as removal of the socket pins may damage the board.

BIST Support Hardware

The BIST support hardware does not interact with the functionality of the HOTLink Transmitter or Receiver and is not part of the communications link. If there is no requirement for BIST and display hardware, the following components may be removed from the board:

- U6 and U7—TIL311 Hex Displays
- U8—CY7C344 EPLD
- S2—Reset Switch
- R21, R22, R23, and R24—1 kΩ
- C13—0.022 µF
- C18—100 pF

Voltage Monitor

The voltage monitor (U11) is used as part of the BIST function and also drives the RESET signal on JP2, JP3, and JP4. If monitoring of the specific voltage is not necessary (and BIST capability is not used) this part may be removed.

If U11 is removed, it may be necessary to bias the RESET line to allow an external system controller to properly sense a high on the RESET output. This may be done by soldering a jumper wire from pin 7 of U11 to pin 2 of R20.

JP2

The area of the board labeled as JP2 provides a hole pattern designed to accept multiple types of headers and connectors. These connectors allow access to all the signals present on JP3 and JP4.

The current pin 1 designation for JP2 assumes a pin-header connector designed for flat cable is attached to bottom of the board. If this type of connector is instead attached to the top of the board, the even and odd pins are effectively swapped in the connector and cable, from those listed in *Table 1*.

OLC-Compatibility Registers

The 74F174 hex D-registers (U9 and U10) are used to provide compatibility with OLC-266 sockets. For those users not requiring this capability, or for those who wish to use the receiver $\overline{\text{RDY}}$ signal to clock received data into asynchronous FIFOs, these registers can be removed.

Once U9 and U10 are removed, it is necessary to short eleven adjacent pad pairs on U9 and U10 to allow the receiver data bus to connect to the output connectors. The pairs that must be shorted are listed in *Table 7*.

Table 7. OLC-Compatibility Register Bypass Connections

Register Pin Connections		
Part	**Pins**	**Signal Name**
U10	14, 15	RCVR_0
U10	12, 13	RCVR_1
U10	10, 11	RCVR_2
U10	6, 7	RCVR_3
U10	4, 5	RCVR_4
U10	2, 3	RCVR_5
U9	10, 11	RCVR_6
U9	12, 13	RCVR_7
U9	14, 15	RCVR_8
U9	6, 7	RCVR_9
U9	4, 5	RDY

Copper Cable Connectors

The CY9266–C and CY9266–T are assembled on the same substrate and may be configured for use with either coaxial or shielded-pair cables. Changing from coax to shielded-pair requires the removal of the J1 BNC and J2 TNC connectors and replacing them with a female 9-pin D-sub connector at location P1 (see Appendix B for manufacturer part numbers). Also, the foil traces that connect pins 6 and 9 of P1 to the shield of J1 and J2 (located on the bottom of the board) must be cut. Because the cable impedance used for shielded-pair cable is different from that of coax cable, the line termination resistors R40 and R41 must be replaced with 75Ω resistors, and coupling transformer T1 must also change to the higher inductance type.

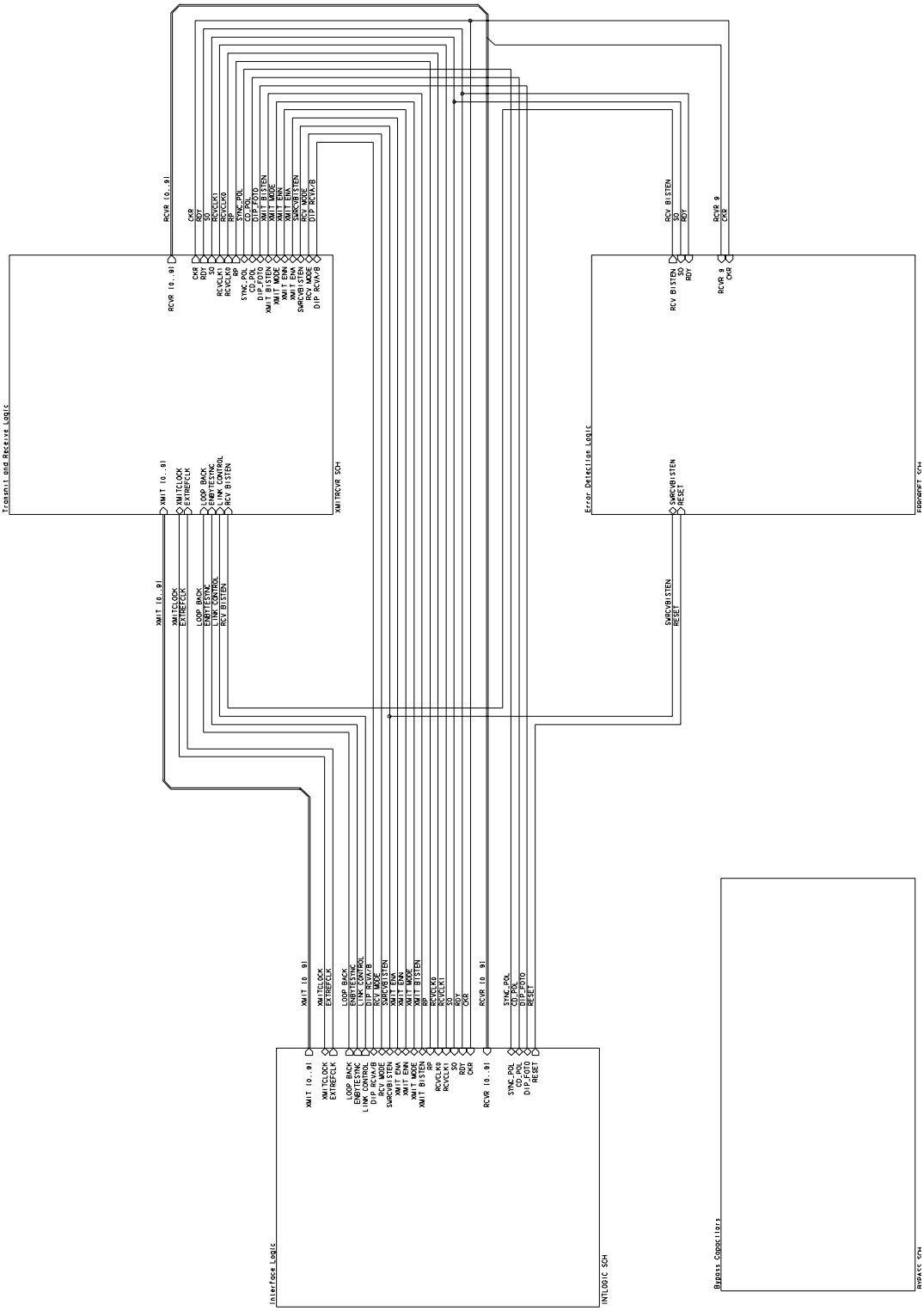
Changing from shielded-pair to coax requires removal of the P1 D-sub connector and the addition of connectors J1 and J2. It is necessary to connect pin 6 of the P1 pad set to the shield pin of J1, and pin 9 of P1 to the shield pin of J2. Because the cable impedance used for coax cable is different from that of shielded-pair cable, the line termination resistors R40 and R41 must be replaced with 37.4Ω resistors, and coupling transformer T1 must also change to the lower inductance type.

Redesign Capability

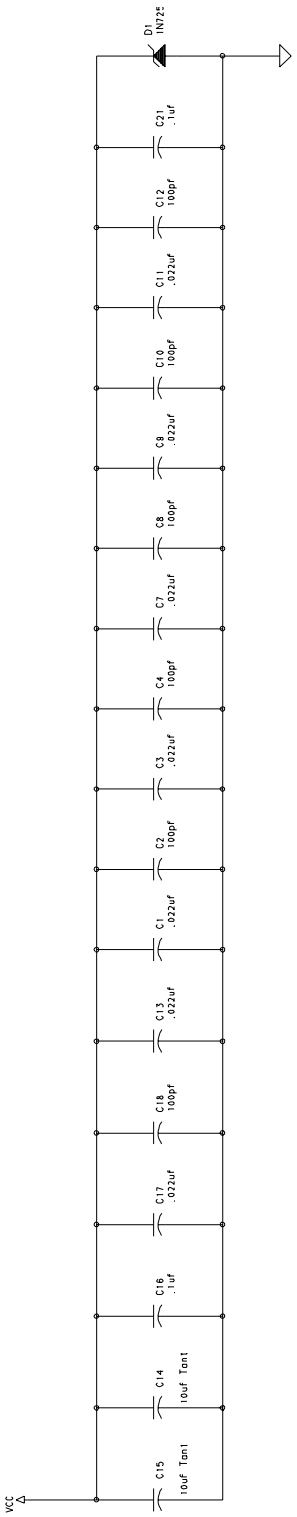
The CY9266–F, CY9266–P, CY9266–C, and CY9266–T boards were designed strictly as a demonstration vehicle for the Cypress Semiconductor HOTLink family of communications parts. The designs shown here may not be optimal for most applications, as these are expected to be more specialized and may not require all the configuration and BIST demonstration hardware contained on these boards.

Examination of the evaluation boards will show that the components necessary for creating a serial link are all on one half of the board, while the components used for configuration and BIST support are located on the other half of the board. This placement of parts was intentional, and shows that two complete channels may be placed on a board of the same size as the CY9266 *without* placing active components on both sides of the board.

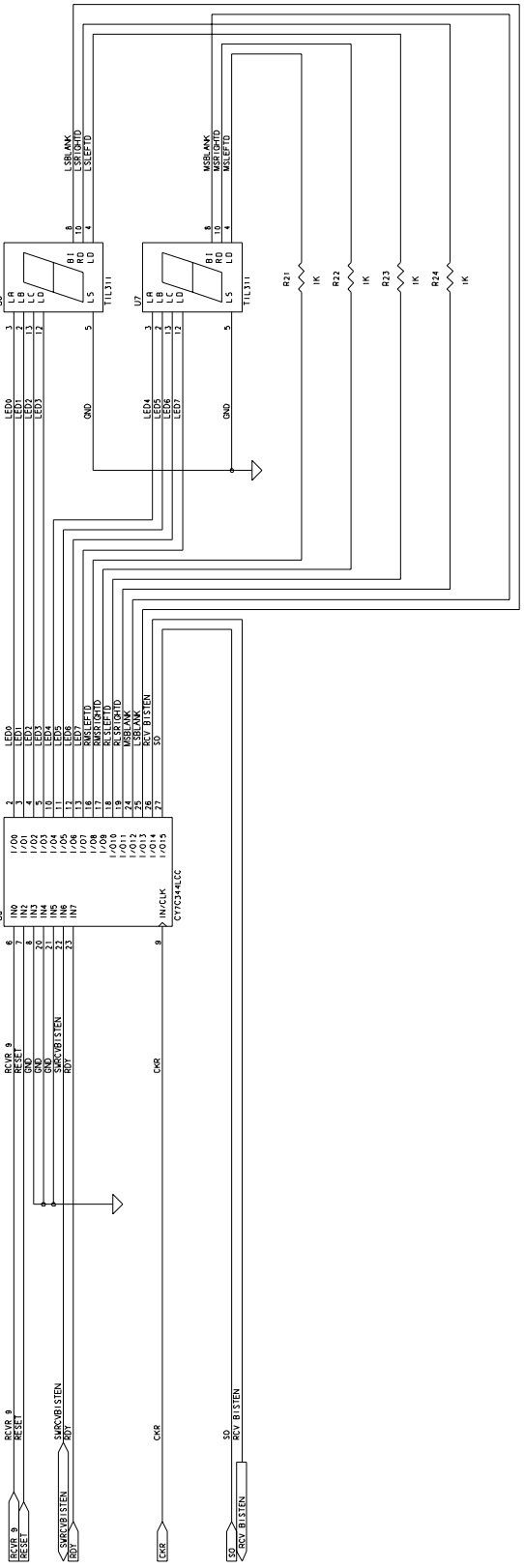
Appendix A. CY9266–F Schematic (Sheet 1 of 5)



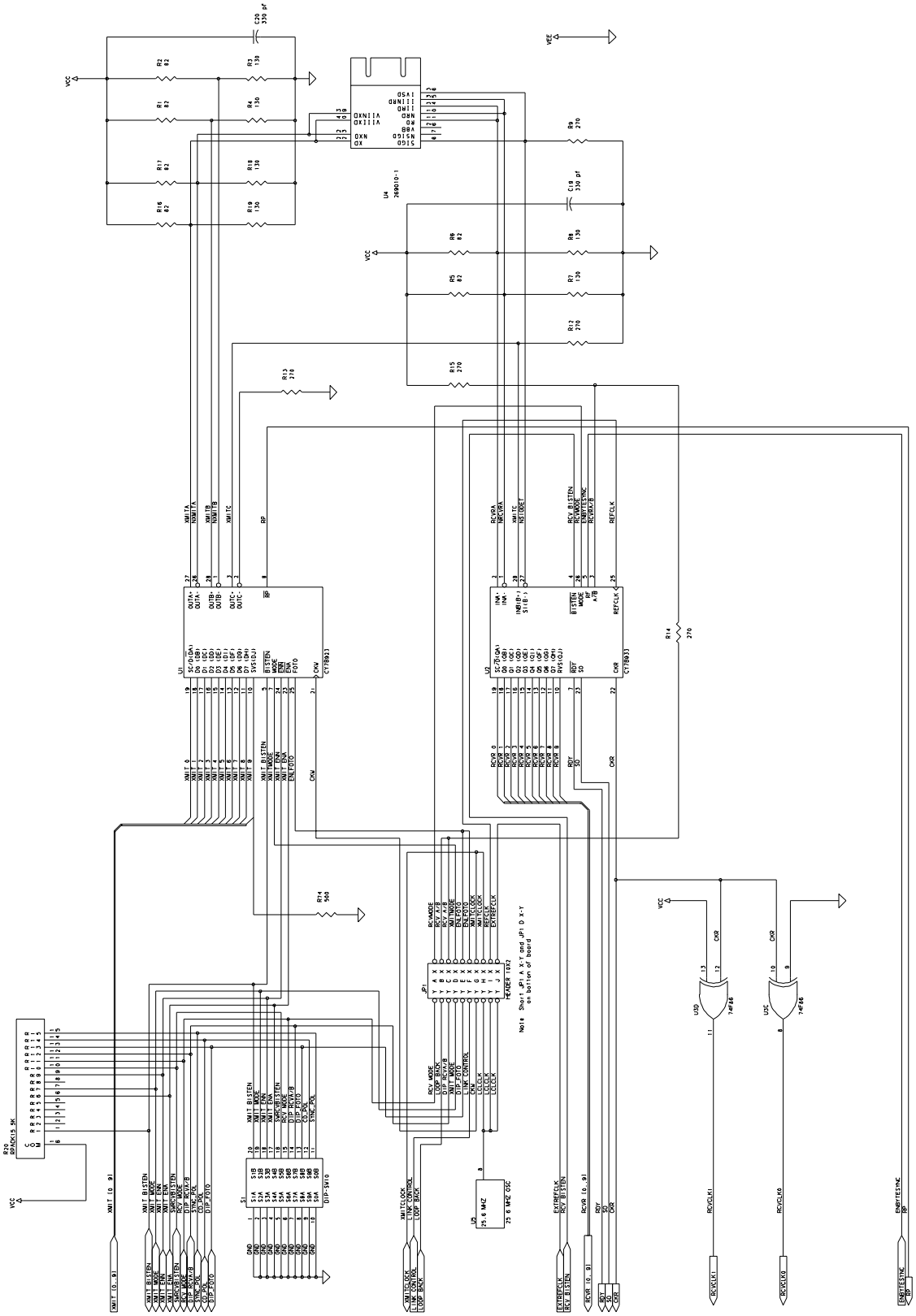
Appendix A. CY9266–F Schematic (Sheet 2 of 5)



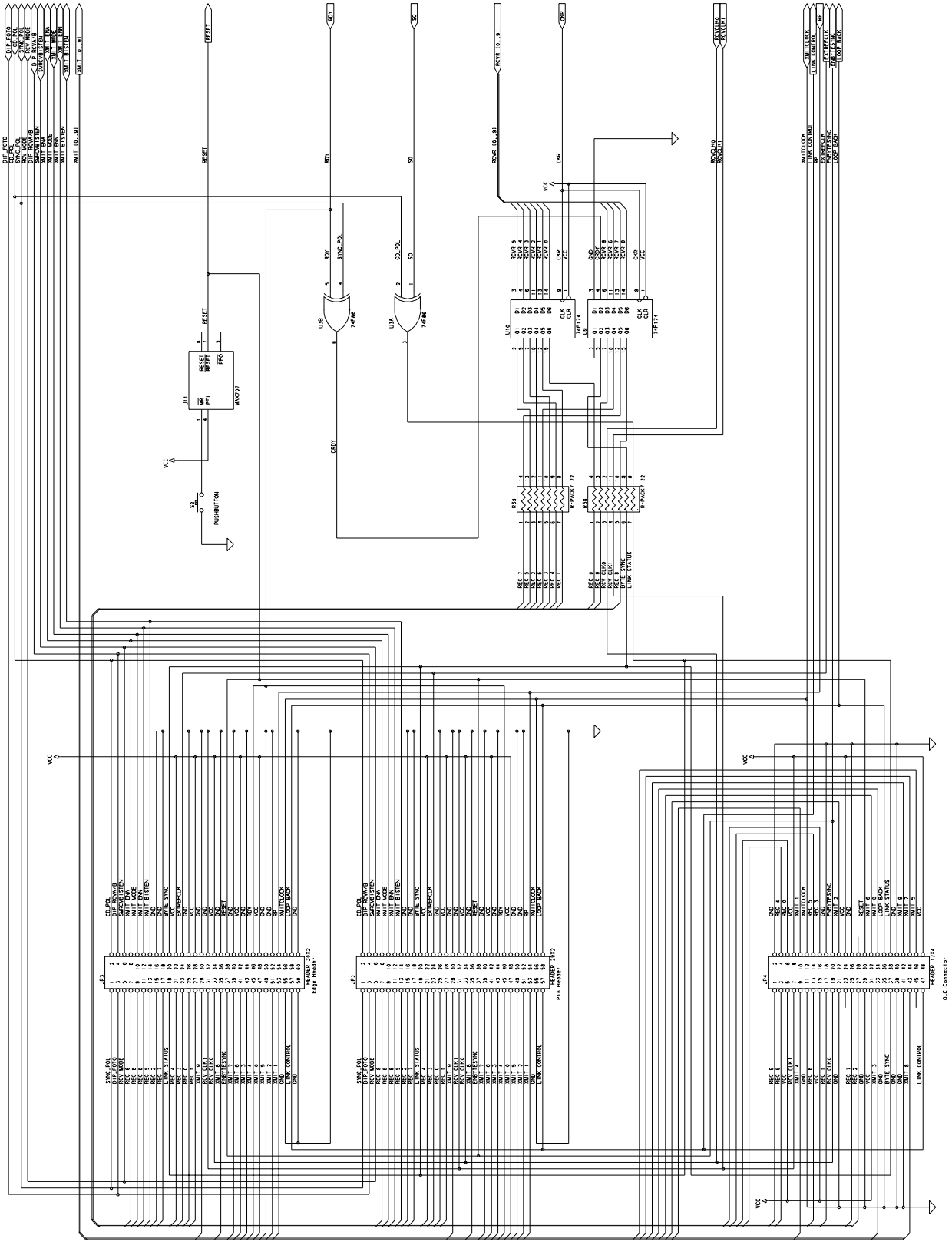
Appendix A. CY9266–F Schematic (Sheet 3 of 5)



Appendix A. CY9266–F Schematic (Sheet 4 of 5)



Appendix A. CY9266–F Schematic (Sheet 5 of 5)

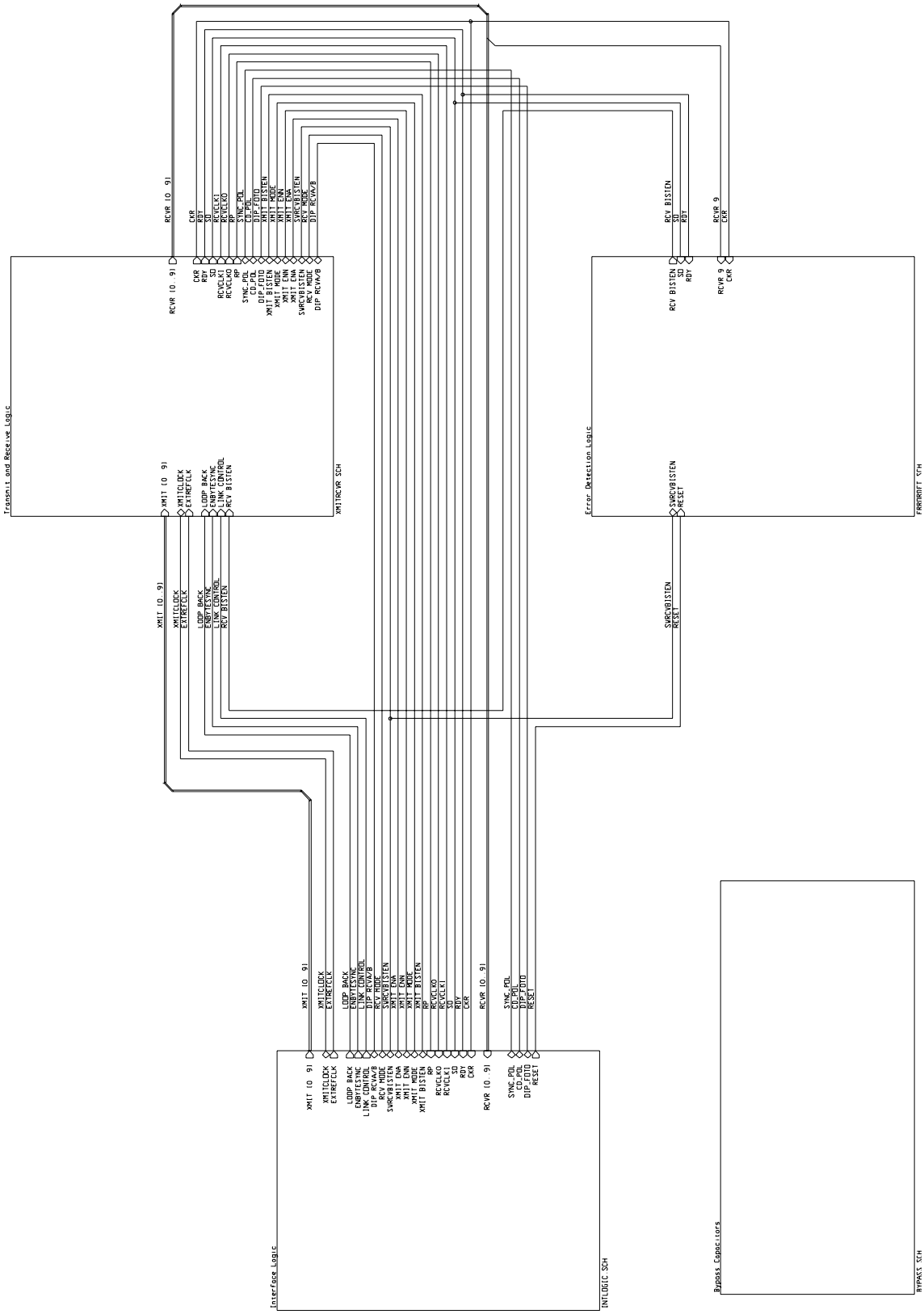


Appendix A. CY9266–F Parts List

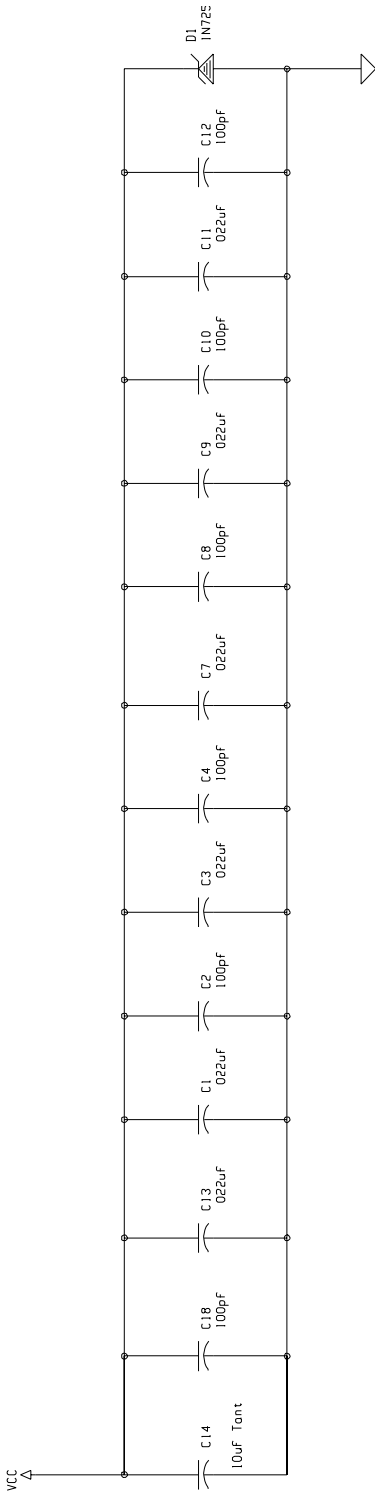
Instance	Part Number	Description
U1	Cypress CY7B923-JC	HOTLink Transmitter
U2	Cypress CY7B933-JC	HOTLink Receiver
U3	74F86	Quad XOR Gate, SOIC Package
U4 (CY9266–F)	AMP/Lytel 269063-1, Hewlett Packard HFBR-5302, Siemens TC-266C2EP, CTS 1408N, or Equivalent	266-MBaud 1300-nm LED Transceiver Module
U4 (CY9266–P)	See Cypress application note "Replacing Wire with Inexpensive Plastic Fiber Solutions" for module design and bill of materials	155-MBaud LED Transceiver Module for POF
U5* (CY9266–F)	CTS CTX126 or Equivalent	25-MHz TTL Clock Oscillator
U5* (CY9266–P)	Cypress ICD6233 QuiXTAL	15.5-MHz TTL Programmable Clock Oscillator
U6*, U7*	TI TIL311	Hex Display With Logic
U8*	Cypress CY7C344-15HC	32-Macrocell MAX EPLD
U9, U10	74F174	Hex D-Register, SOIC Package
U11*	Maxim MAX707CSA or Equivalent	Voltage Monitor
D1*	1N4735A	1W, 6.2V Zener Diode
S1*	AMP 3-435668-0 or Equivalent	10-position DIP Switch
S2*	ECG 520-01-3 or Equivalent	Momentary Pushbutton Switch
JP1*	Sullins PZC10DAAN or Equivalent	2 x 10 Position 0.25" Sq. Pin-Header
JP4	Sullins PZC12DFBN or Equivalent	2 – 2 x 12 Position 0.25" Sq. Pin-Header
C1, C3, C7, C9, C11, C13, C17	0.022 µF MLC X7R	0805 Chip Cap
C2, C4, C8, C10, C12, C18	100 pF MLC NPO	0805 Chip Cap
C14, C15	10 µF 16V Tantalum	Electrolytic Cap
C16, C21	0.1 µF MLC X7R	1206 Chip Cap
C19, C20	330 pF MLC NPO	0805 Chip Cap
R5, R6, R16, R17	82Ω 1/8W	1206 Chip Resistor
R7, R8, R18, R19	130Ω 1/8W	1206 Chip Resistor
R9, R12, R13, R14, R15	270Ω 1/8W	1206 Chip Resistor
R21*, R22*, R23*, R24*	1-kΩ 1/8W, 5%	1206 Chip Resistor
R74	510Ω 1/8W, 5%	1206 Chip Resistor
R20	CTS 766-161-R512 or Equivalent	5.1-kΩ R-Pack-15 SO16
R38, R39	CTS 766-143-R220 or Equivalent	22Ω R-Pack-7 SO14
	AMP 645955-2 or Equivalent	41 – Low Profile Socket-Pin
	3M 929955-06 or Equivalent	4 – 0.1" Centerline Shorting Jumper

* — Used only for supervisory functions. Not needed for communications.

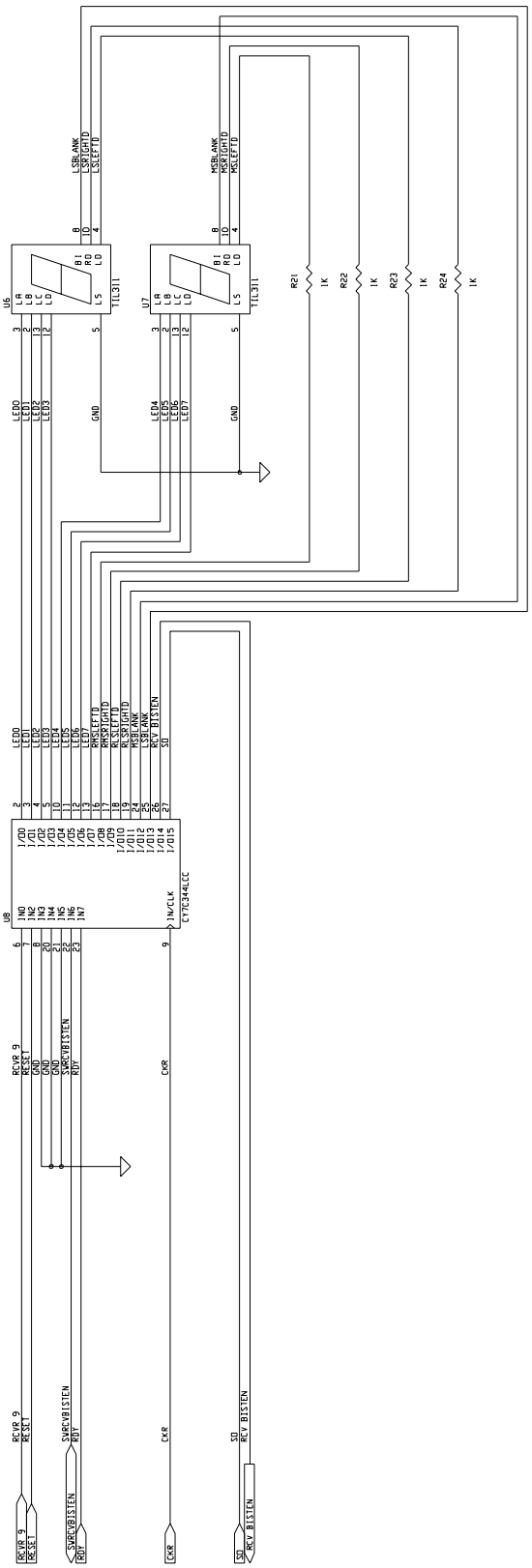
Appendix B. CY9266–C/T Schematic (Sheet 1 of 5)



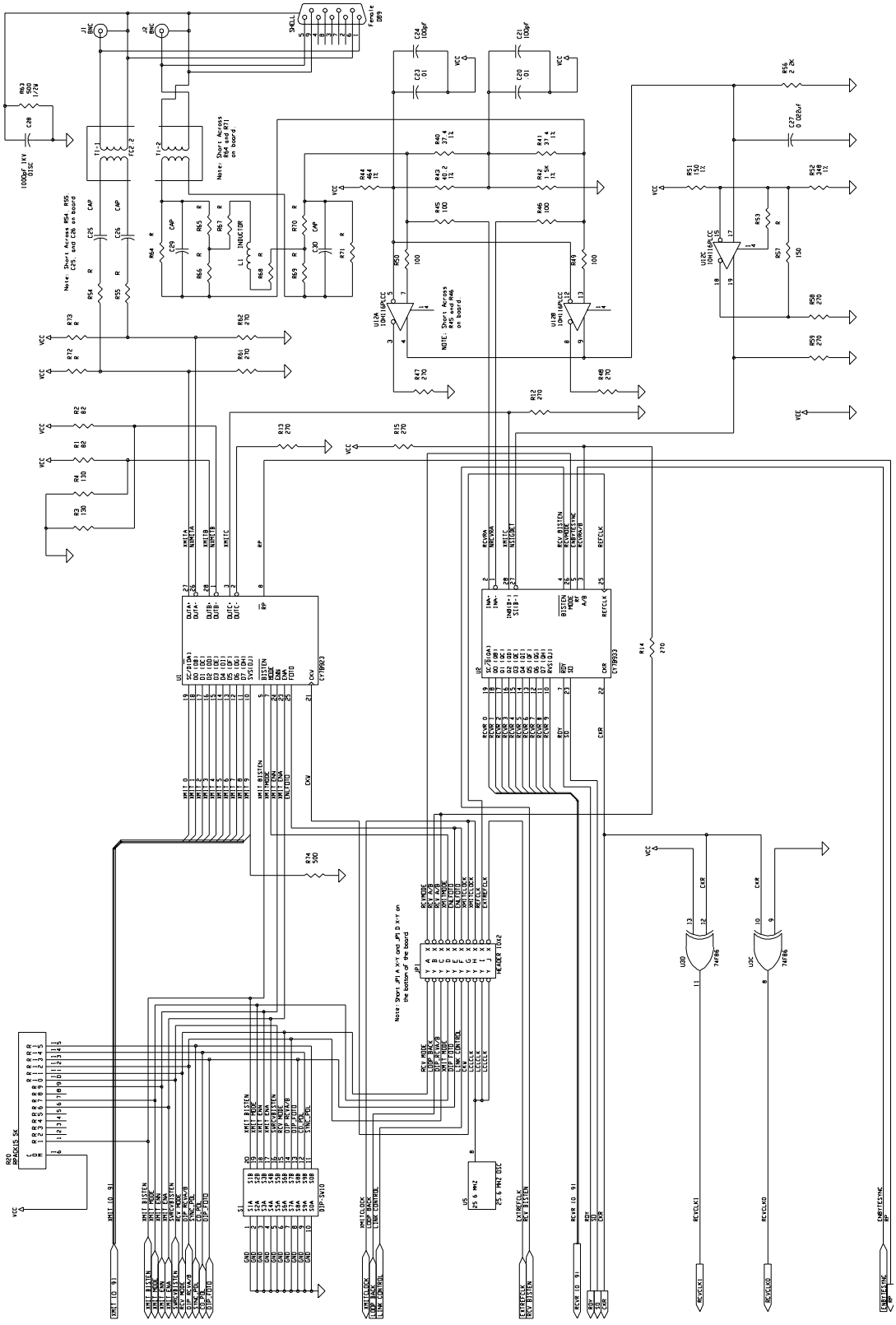
Appendix B. CY9266–C/T Schematic (Sheet 2 of 5)



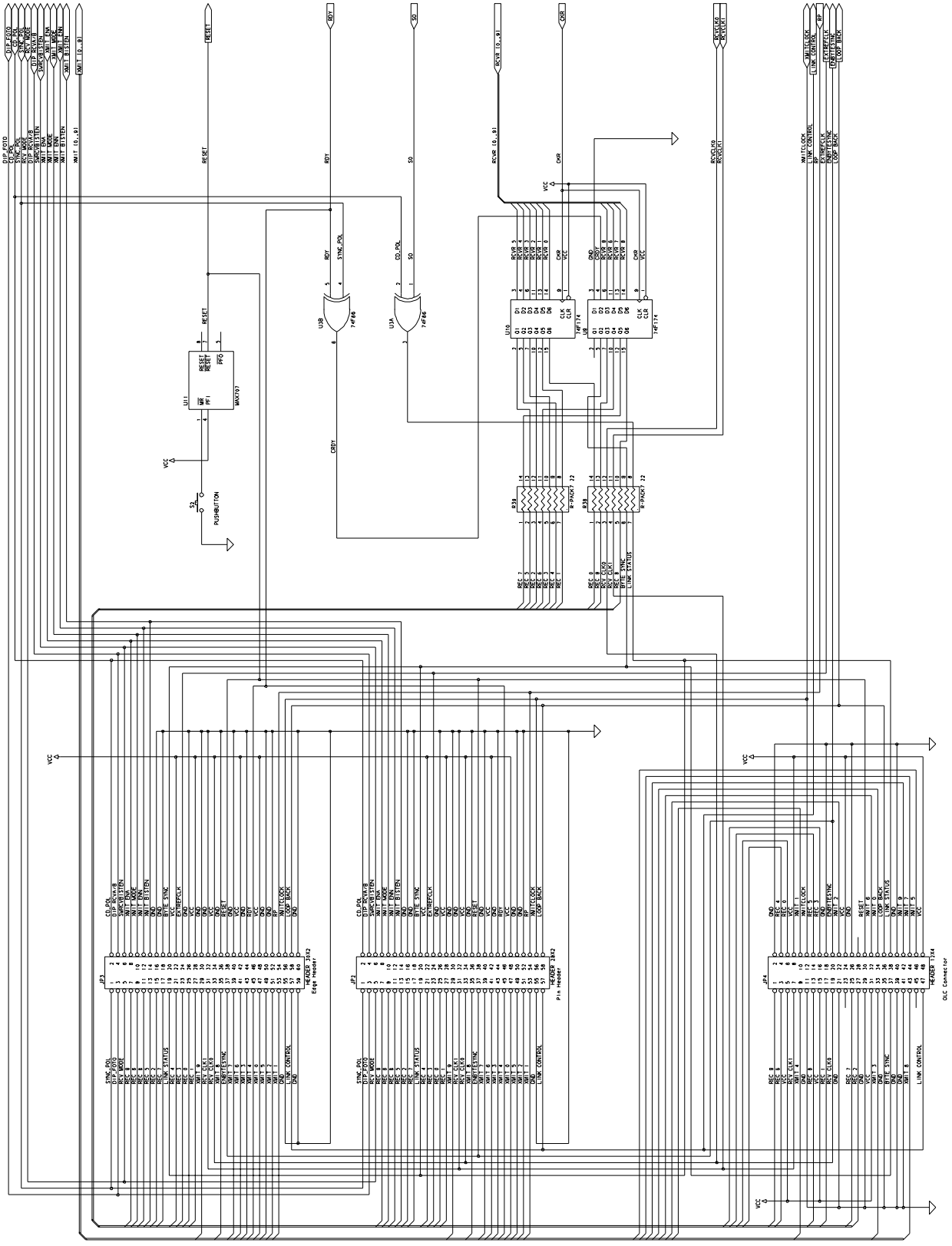
Appendix B. CY9266–C/T Schematic (Sheet 3 of 5)



Appendix B. CY9266–C/T Schematic (Sheet 4 of 5)



Appendix B. CY9266–C/T Schematic (Sheet 5 of 5)



Appendix B. CY9266–C/T Parts List

Instance	Part Number	Description
U1	Cypress CY7B923-JC	HOTLink Transmitter
U2	Cypress CY7B933-JC	HOTLink Receiver
U3	74F86	Quad XOR Gate, SOIC Package
U5*	CTS CTX126 or Equivalent	25-MHz TTL Clock Oscillator
U6*, U7*	TI TIL311	Hex Display With Logic
U8*	Cypress CY7C344-15HC	32-Macrocell MAX EPLD
U9, U10	74F174	Hex D-Register, SOIC Package
U11*	Maxim MAX707CSA or Equivalent	Voltage Monitor
U12*	Motorola MC10H116FN	ECL Triple Line Receiver
D1*	1N4735A	1W, 6.2V Zener Diode
S1*	AMP 3-435668-0 or Equivalent	10-Position DIP Switch
S2*	ECG 520-01-3 or Equivalent	Momentary Pushbutton Switch
J1	227161-3 or Equivalent	RA Female BNC Connector
J2	227818-1 or Equivalent	RA Female TNC Connector
JP1*	Sullins PZC10DAAN or Equivalent	2 x 10 Position 0.25" Sq. Pin-Header
JP4	Sullins PZC12DFBN or Equivalent	2 – 2 x 12 Position 0.25" Sq. Pin-Header
P1	747844-6 or Equivalent	RA Female 9-Pin D-Sub Connector
C14	10 µF 16V Tantalum	Electrolytic Cap
C1, C3, C7, C9, C11, C13, C27*	0.022 µF MLC X7R	0805 Chip Cap
C2, C4, C8, C10, C12, C18, C21, C24*	100 pF MLC NPO	0805 Chip Cap
C20, C23*	0.01 µF MLC X7R	0805 Chip Cap
C28	1000 pF 1 kV, Y5P	Disc Cap
T1	Pulse Engineering PE-65507 for STP Pulse Engineering PE-65508 for coax	Dual-Wideband Pulse Transformer
R12, R13, R14, R15	270Ω 1/8W, 5%	1206 Chip Resistor
R74	510Ω 1/8W, 5%	1206 Chip Resistor
R21*, R22*, R23*, R24*	1-kΩ 1/8W, 5%	1206 Chip Resistor
R40, R41	37.4Ω 1/10W, 1% for Coax 75.0Ω 1/10W, 1% for STP	0805 Chip Resistor
R43	40.2Ω 1/10W, 1%	0805 Chip Resistor
R49*, R50*	100Ω 1/10W, 5%	0805 Chip Resistor
R51*, R57*	150Ω 1/10W, 1%	0805 Chip Resistor
R47*, R48*, R58*, R59*	270Ω 1/10W, 5% for 150Ω cable	0805 Chip Resistor
R61, R62	200Ω 1/10W, 5% of 75Ω cable	0805 Chip Resistor
R52*	348Ω 1/10W, 1%	0805 Chip Resistor
R44	464Ω 1/10W, 1%	0805 Chip Resistor
R42	1.5-kΩ 1/10W, 1%	0805 Chip Resistor

Appendix B. CY9266–C/T Parts List (continued)

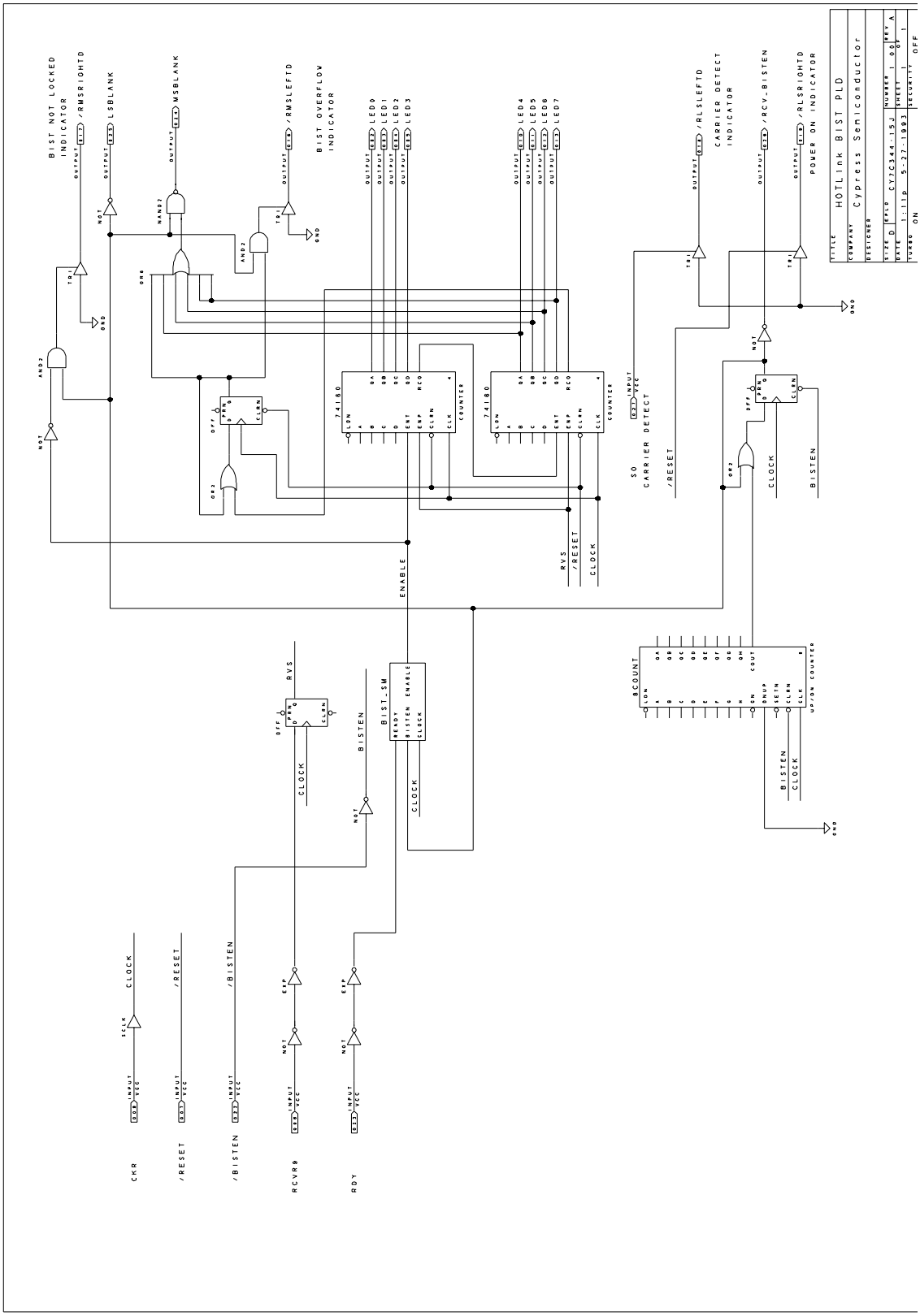
Instance	Part Number	Description
R56*	2.2-kΩ 1/10W, 5%	0805 Chip Resistor
R63	510Ω 1/2W	Axial Lead Resistor
R20	CTS 766-161-R512 or Equivalent	5.1-kΩ R-Pack-15 SO16
R38, R39	CTS 766-143-R220 or Equivalent	22Ω R-Pack-7 SO14
	AMP 645955-2 or Equivalent	4 – Low Profile Socket-Pin
	3M 929955-06 or Equivalent	4 – 0.1" Centerline Shorting Jumper

* — Used only for supervisory functions. Not needed for communications.

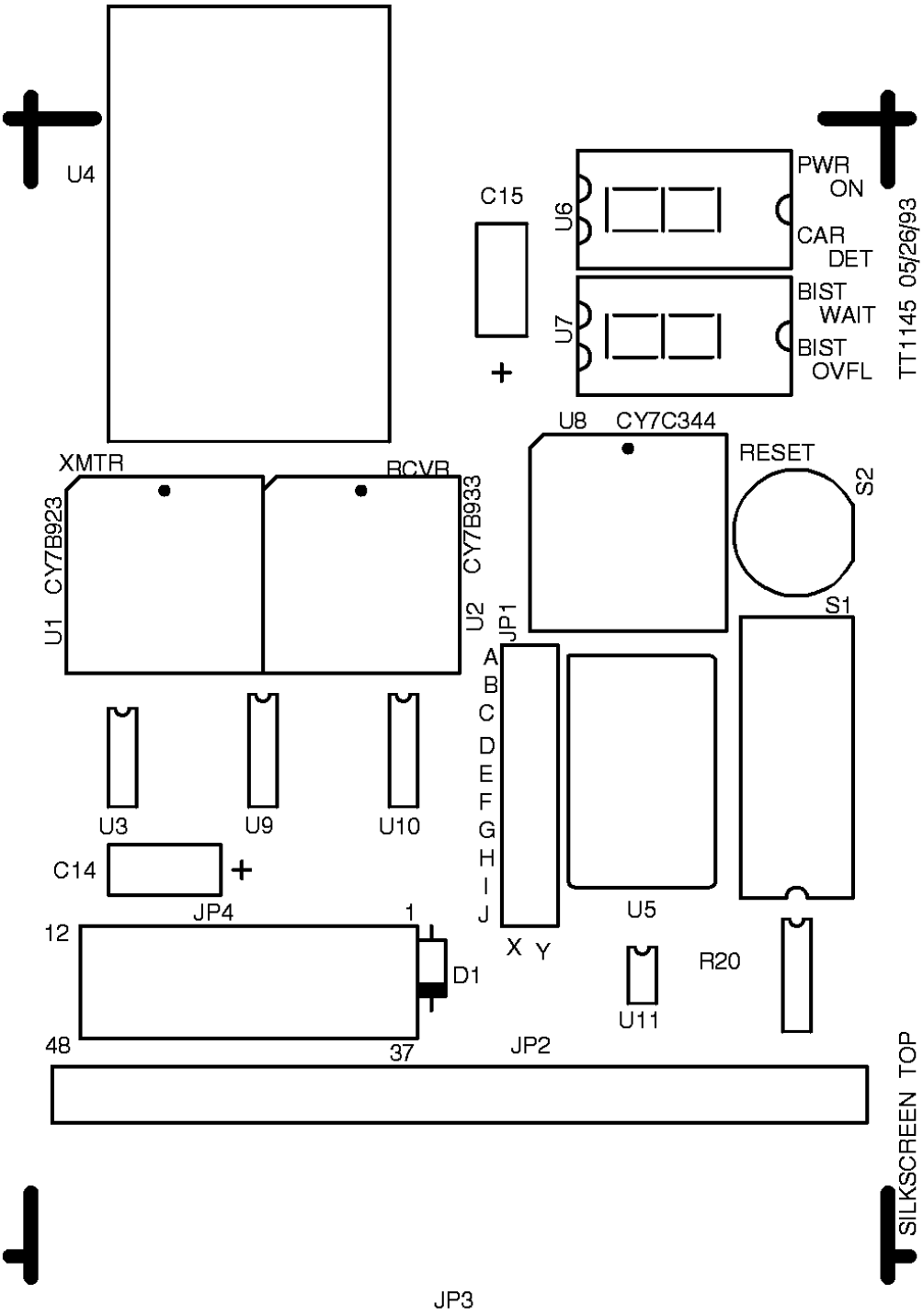
Appendix C. BIST PLD State Machine Source Code

```
SUBDESIGN bist_sm  (ready, bisten, clock : INPUT;
                    enable               : OUTPUT)


VARIABLE
       ss : MACHINE OF BITS  (enable_q)
                     %state    output%
            WITH STATES (wait0    =   0,
                         wait1    =   0,
                         wait2    =   0,
                         enabled  =   0,
                         locked1  =   1,
                         locked2  =   1);

BEGIN
       ss.clk = clock;              %assign machine clock%
       enable = enable_q;           %assign output of machine%

       TABLE
              %present    present            next %
              % state     inputs             state%
                 ss,   bisten, ready =>      ss;

       % define reset vectors %
                wait0,     0,   x    =>      wait0;
                wait1,     0,   x    =>      wait0;
                wait2,     0,   x    =>      wait0;
                enabled,   0,   x    =>      wait0;
                locked1,   0,   x    =>      wait0;
                locked2,   0,   x    =>      wait0;
       % define operational vectors %
                wait0,     1,   x    =>      wait1;
                wait1,     1,   x    =>      wait2;
                wait2,     1,   x    =>      enabled;
                enabled,   1,   1    =>      enabled;
                enabled,   1,   0    =>      locked1;
                locked1,   1,   1    =>      enabled;
                locked1,   1,   0    =>      locked2;
                locked2,   1,   1    =>      locked1;
                locked2,   1,   0    =>      locked2;
       END TABLE;
END;
```

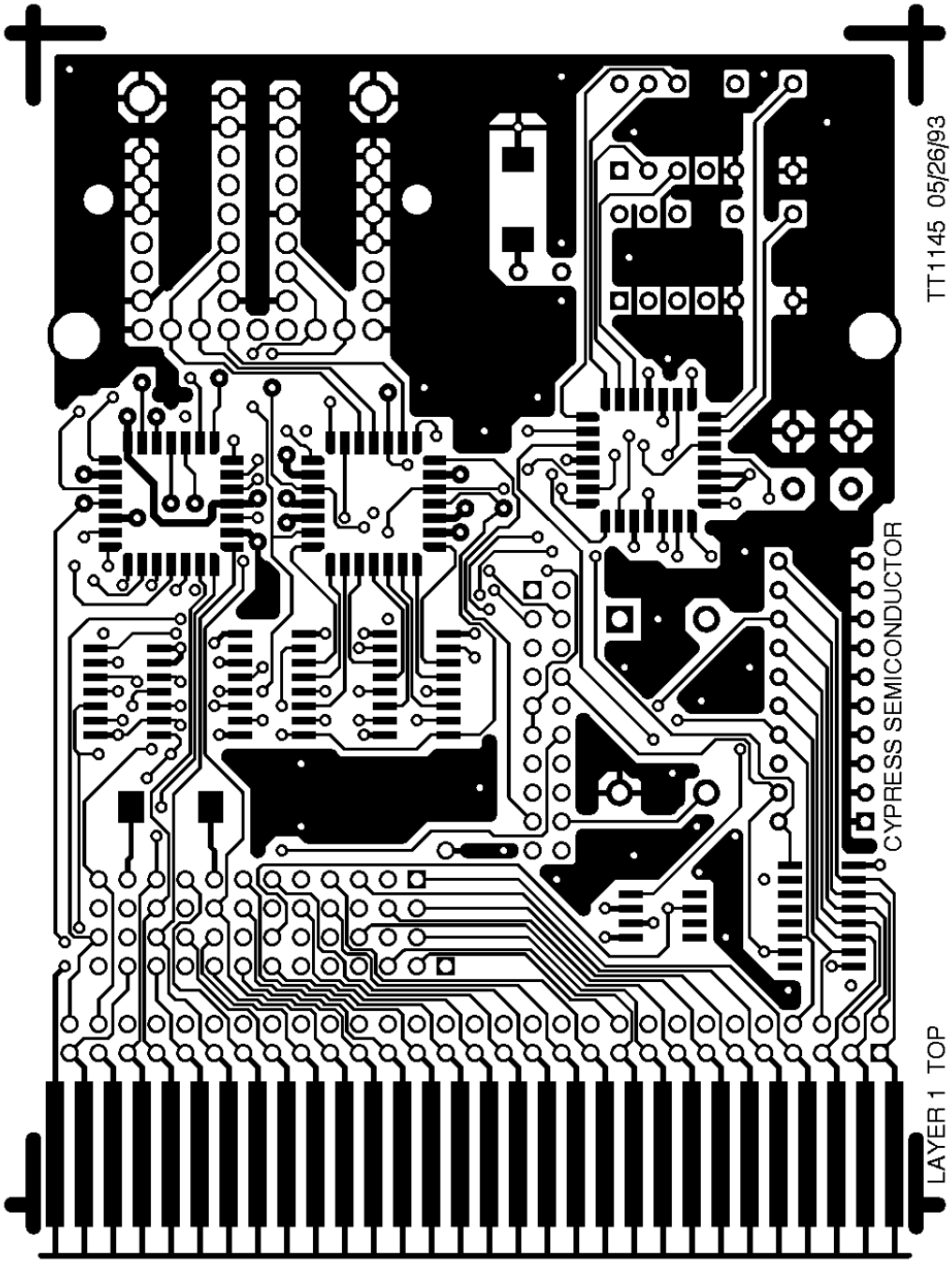
Appendix C. BIST PLD Logic Schematic



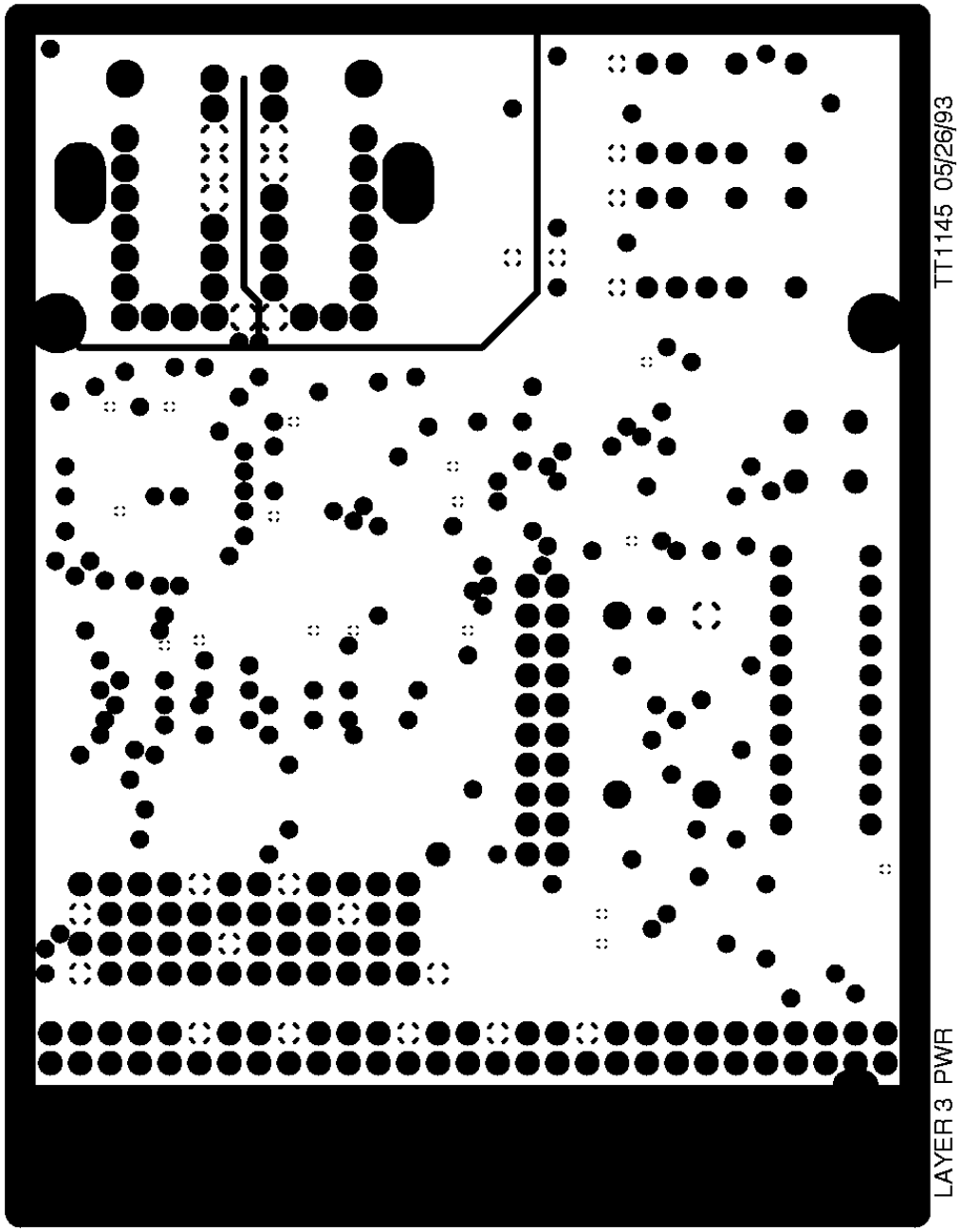
Appendix D. CY9266–F Artwork — Top Silkscreen



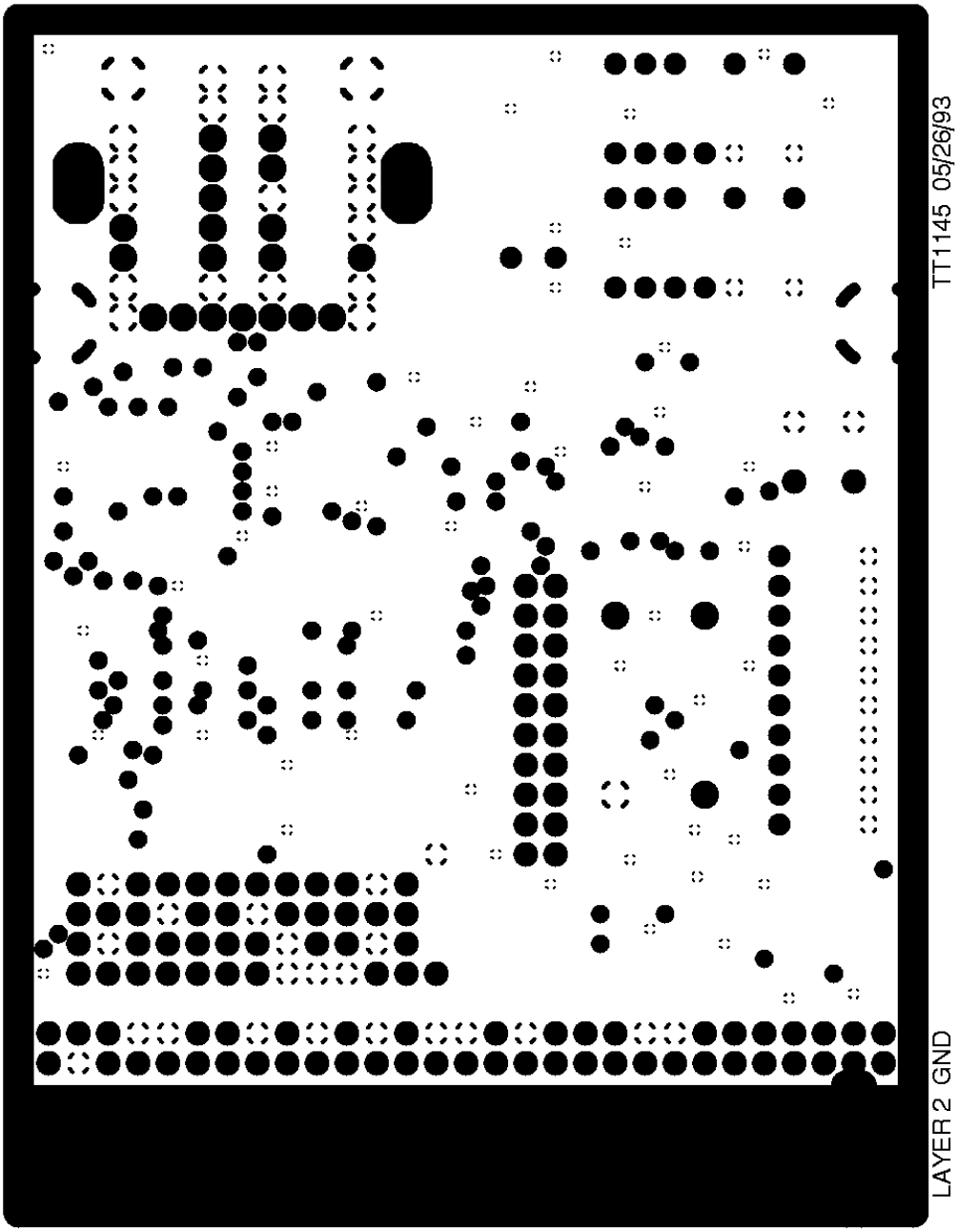
Appendix D. CY9266–F Artwork — Top Layer Copper



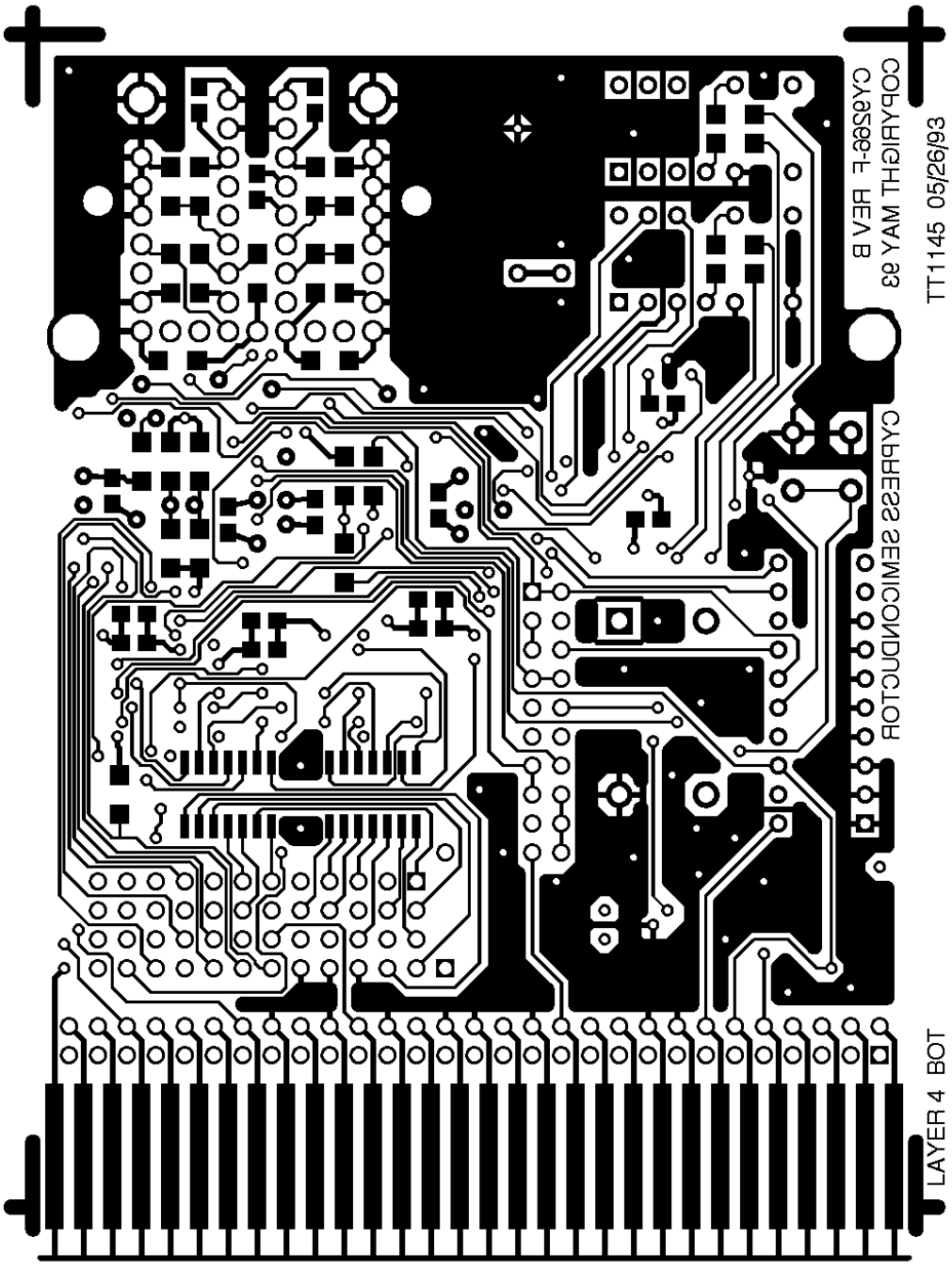
Appendix D. CY9266–F Artwork — Power Layer



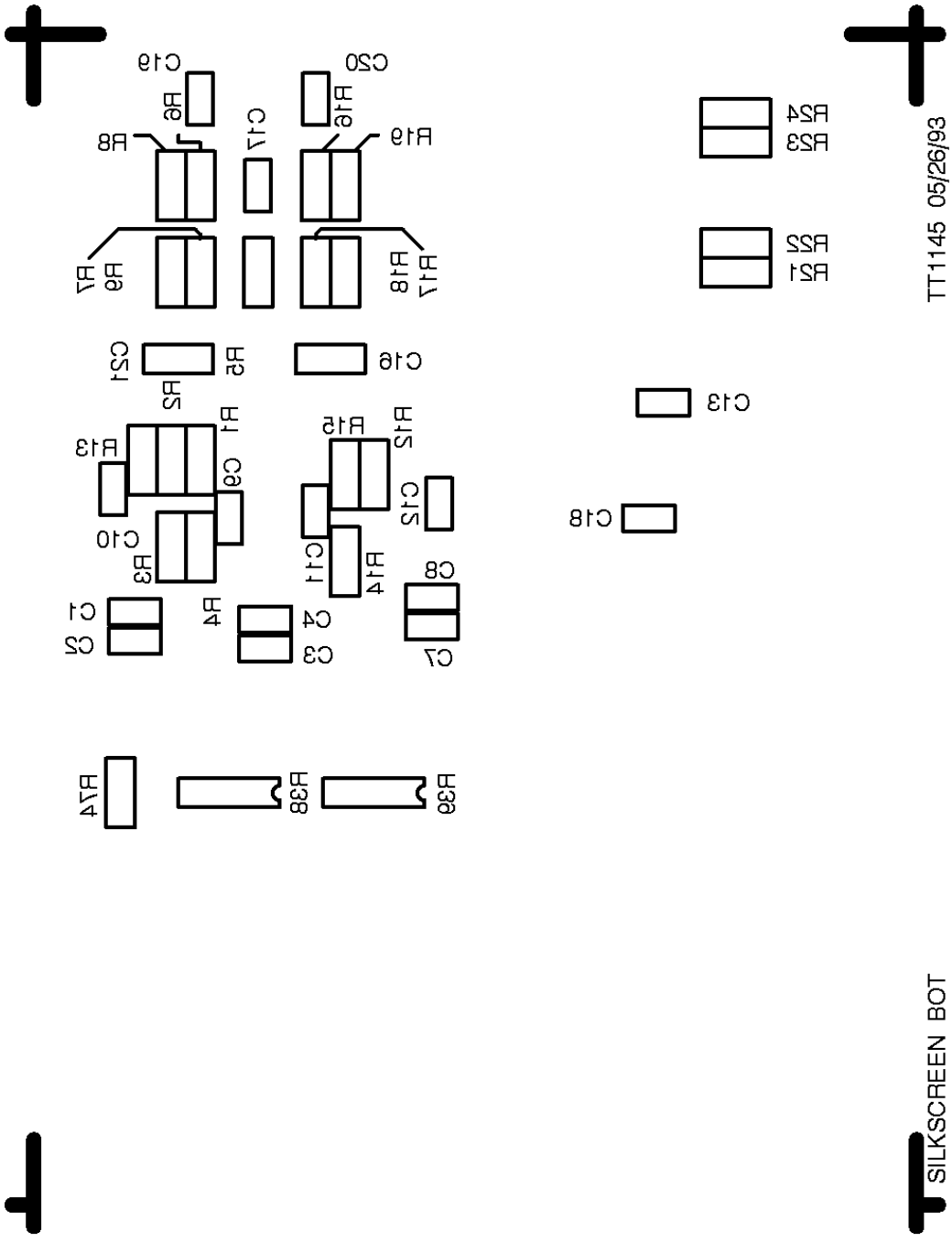
Appendix D. CY9266–F Artwork — Ground Layer



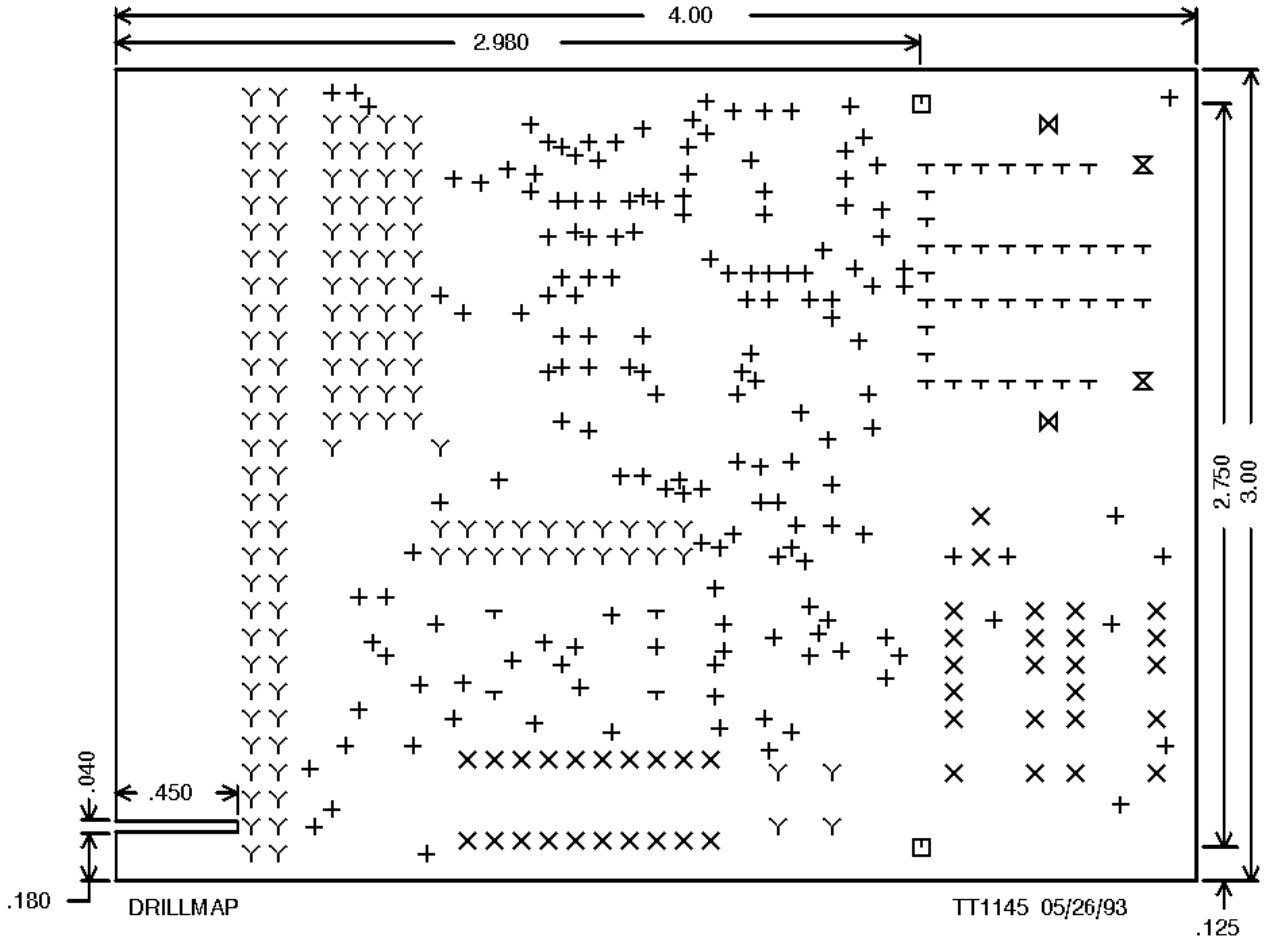
Appendix D. CY9266–F Artwork — Bottom Layer Copper



Appendix D. CY9266–F Artwork — Bottom Silkscreen



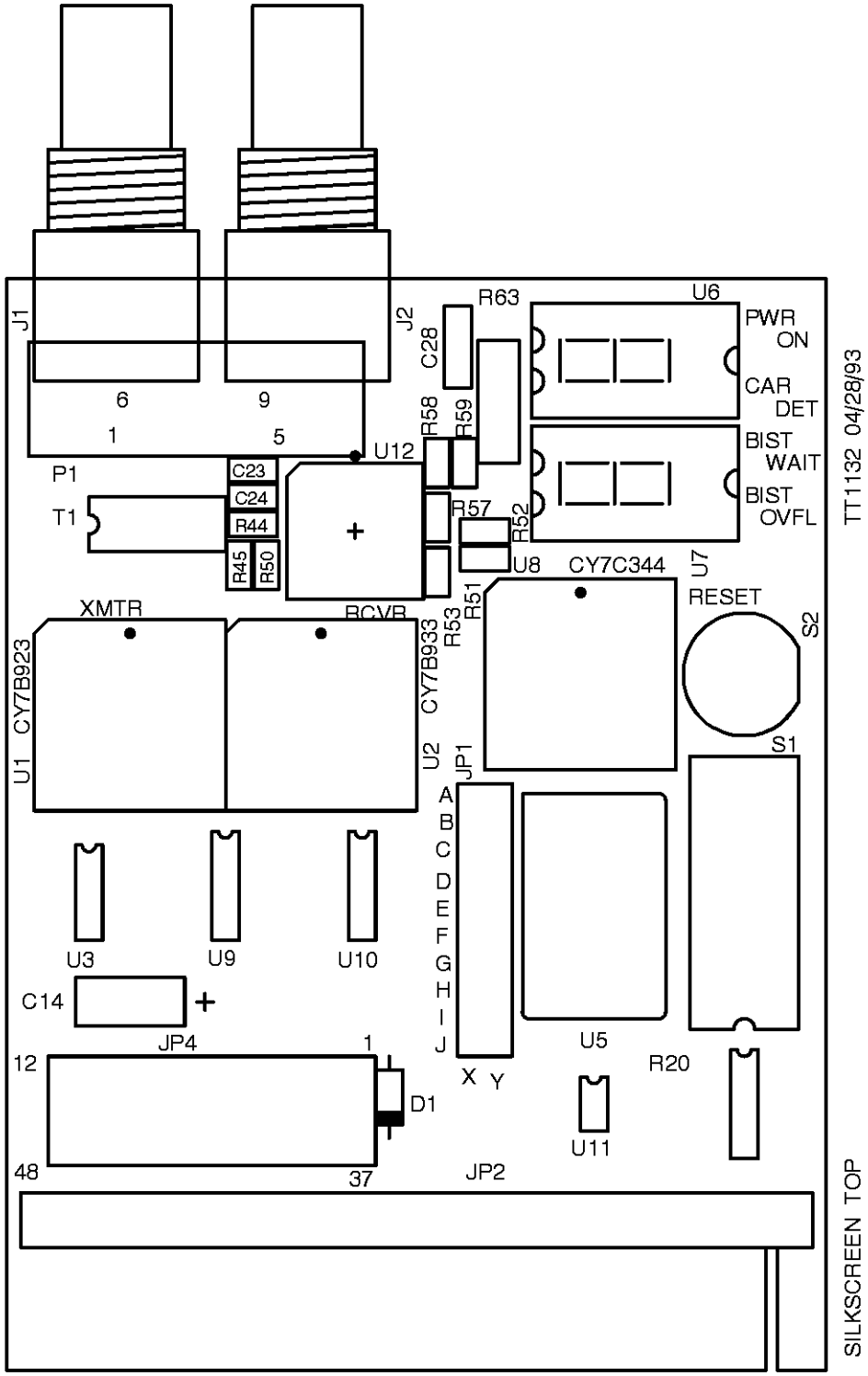
Appendix D. CY9266–F Artwork — Drill Chart



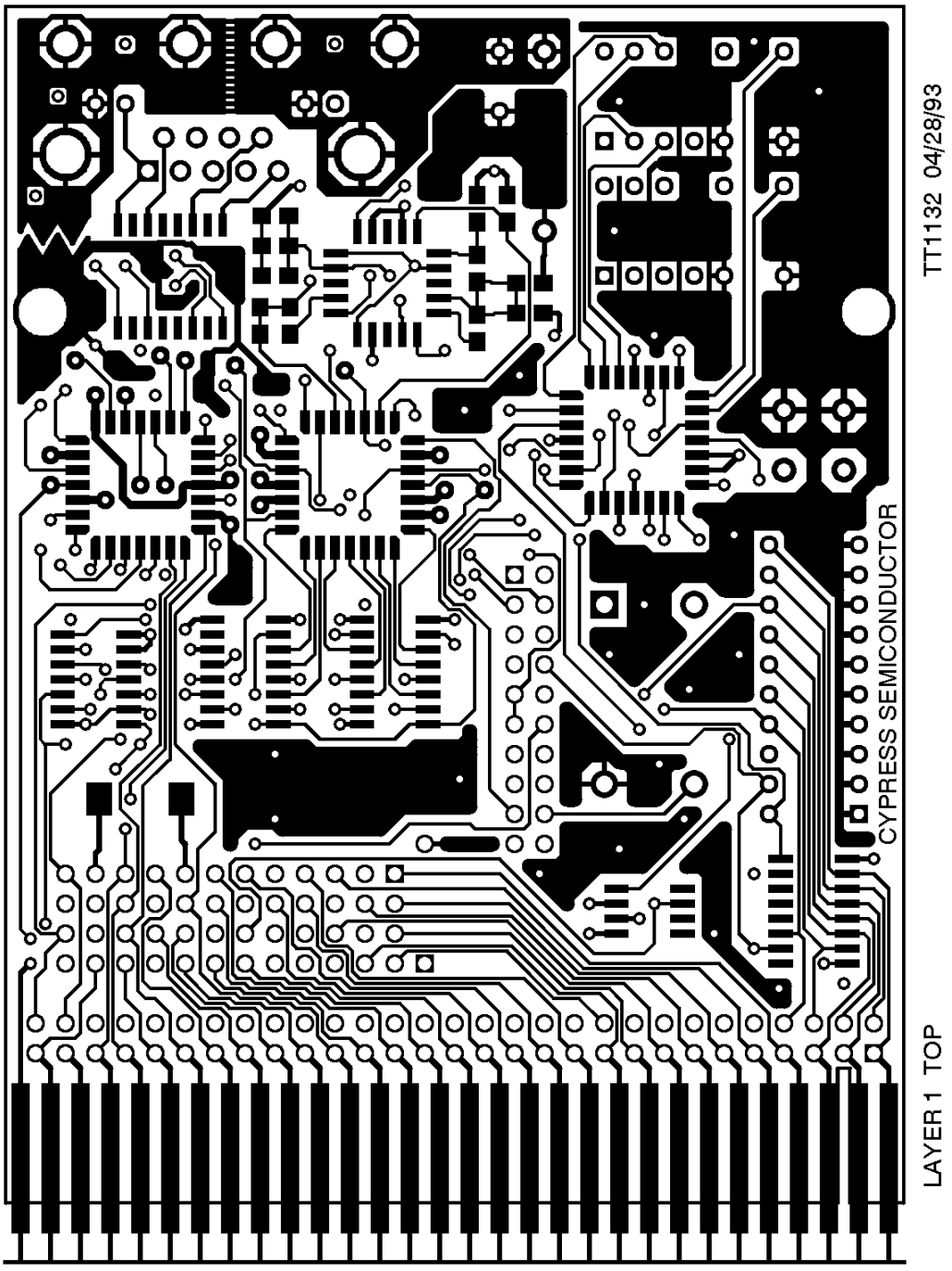
TOOL	SIZE	SYM	QTY	PLT
T01	.020	+	162	Y
T02	.032	X	44	Y
T03	.040	Y	132	Y
T04	.052	⊤	41	Y
T05	.085	⧖	4	Y
T06	.156	⊡	2	Y
T06	↓	⋈	2	Y

.200 X .100 OVAL HOLE

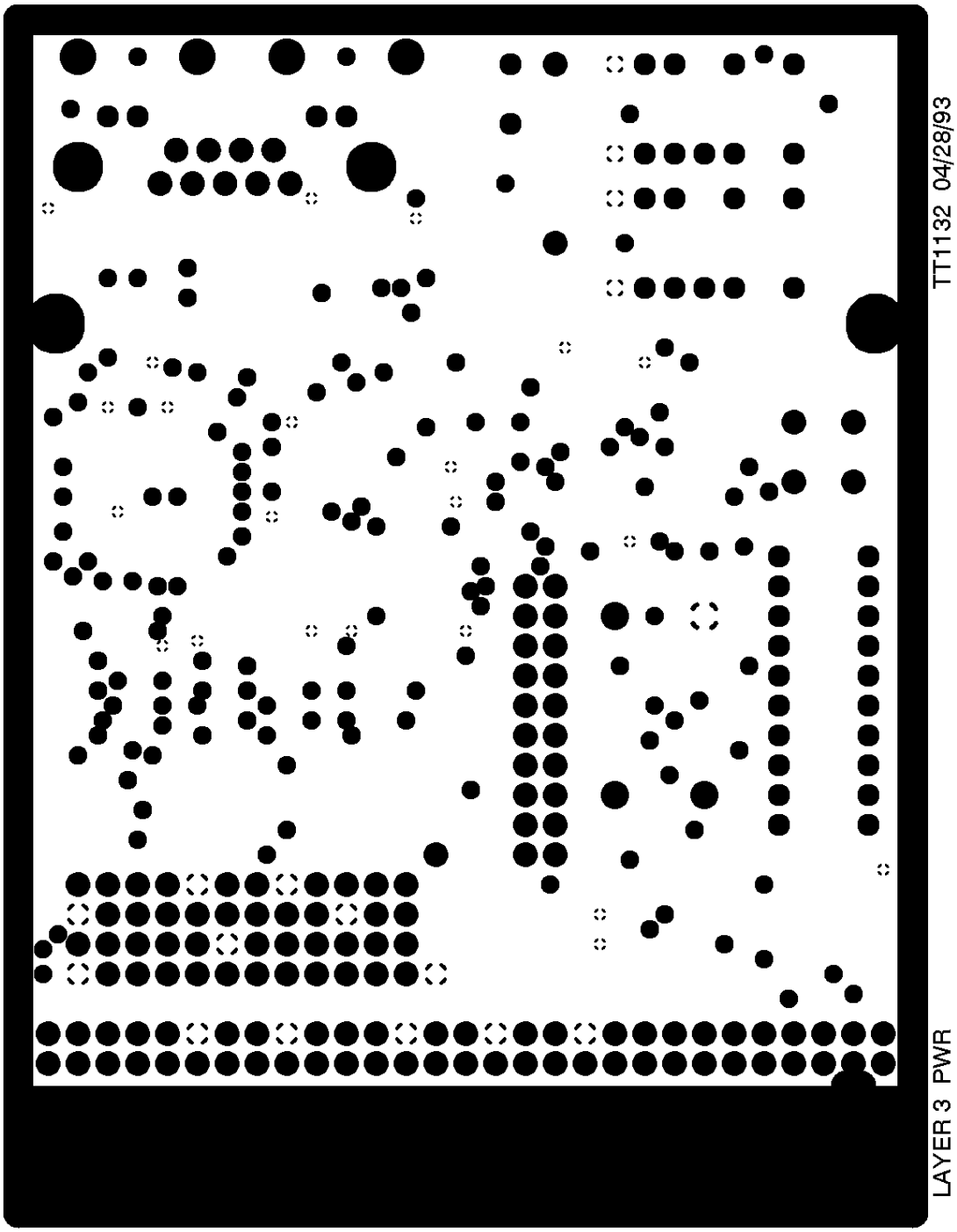
Appendix E. CY9266–C/T Artwork — Top Silkscreen



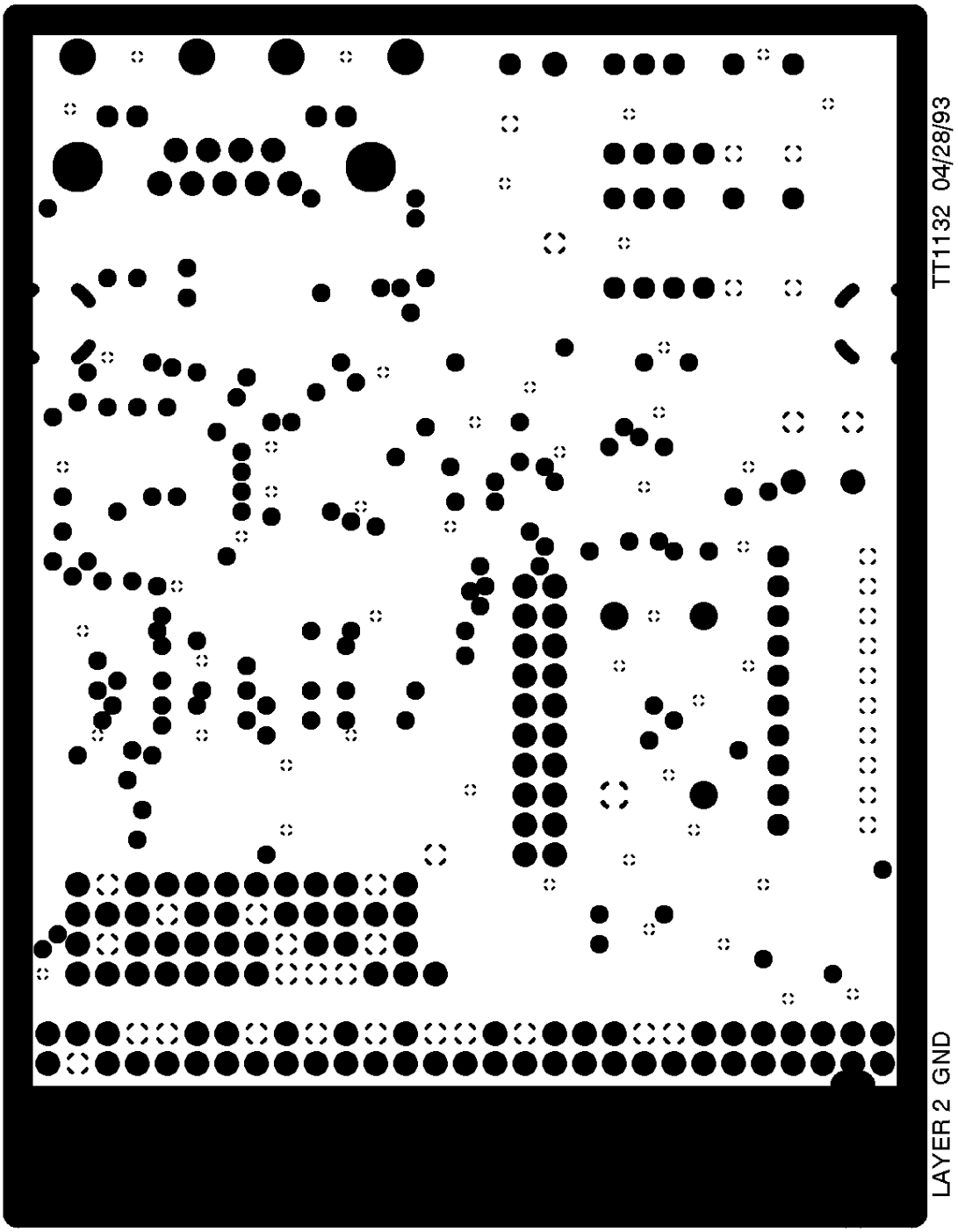
Appendix E. CY9266–C/T Artwork — Top Layer Copper



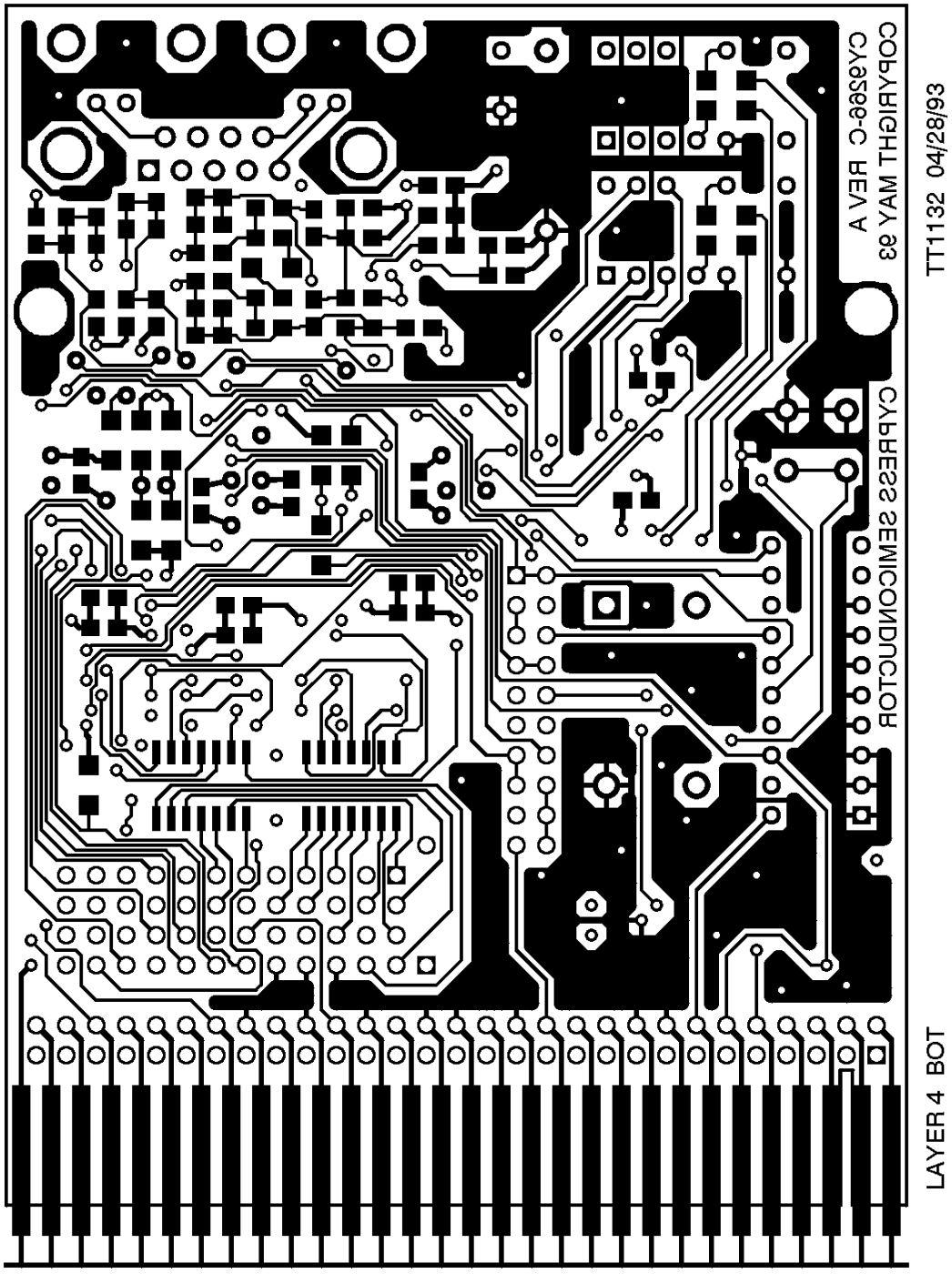
Appendix E. CY9266–C/T Artwork — Power Layer



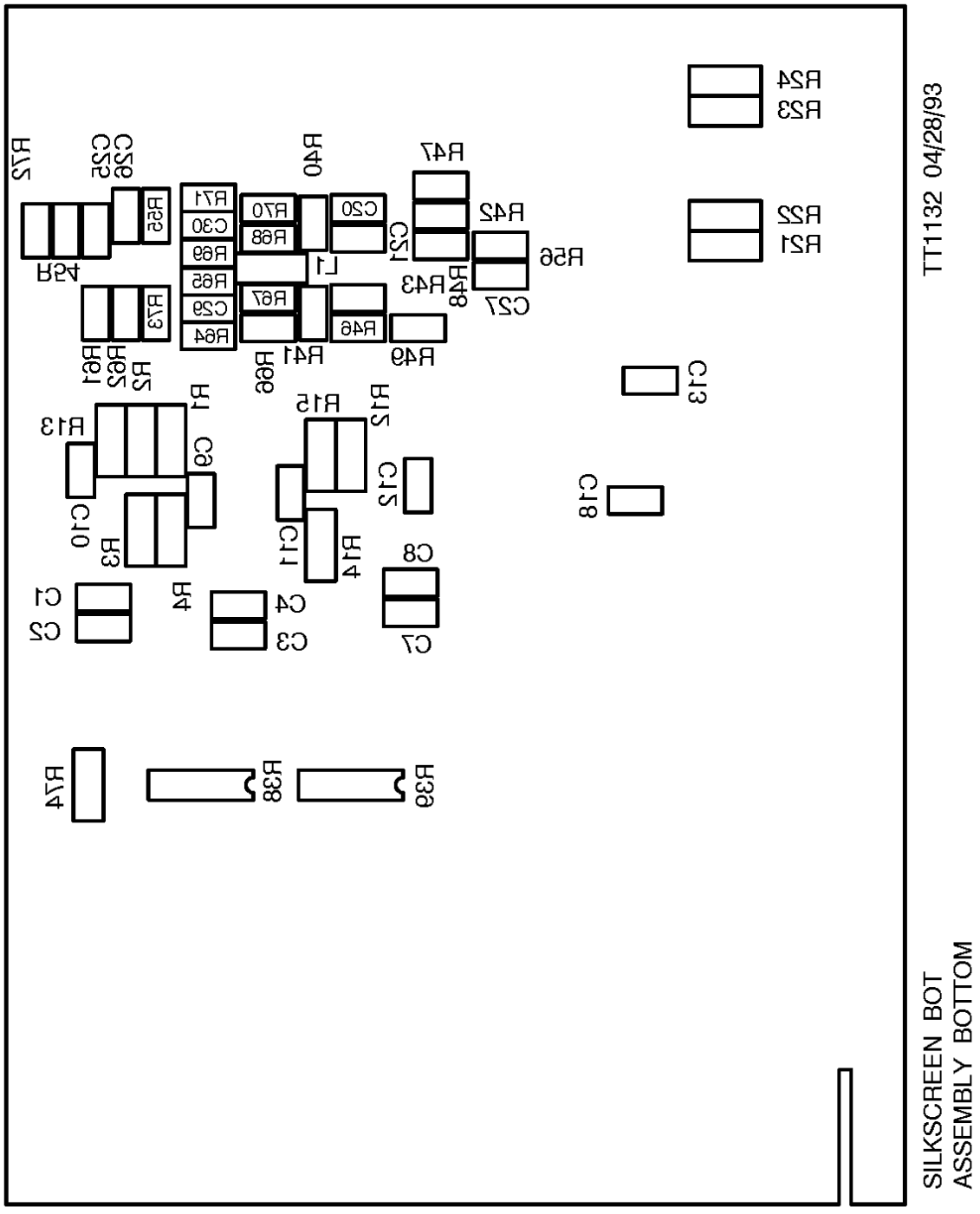
Appendix E. CY9266–C/T Artwork — Ground Layer



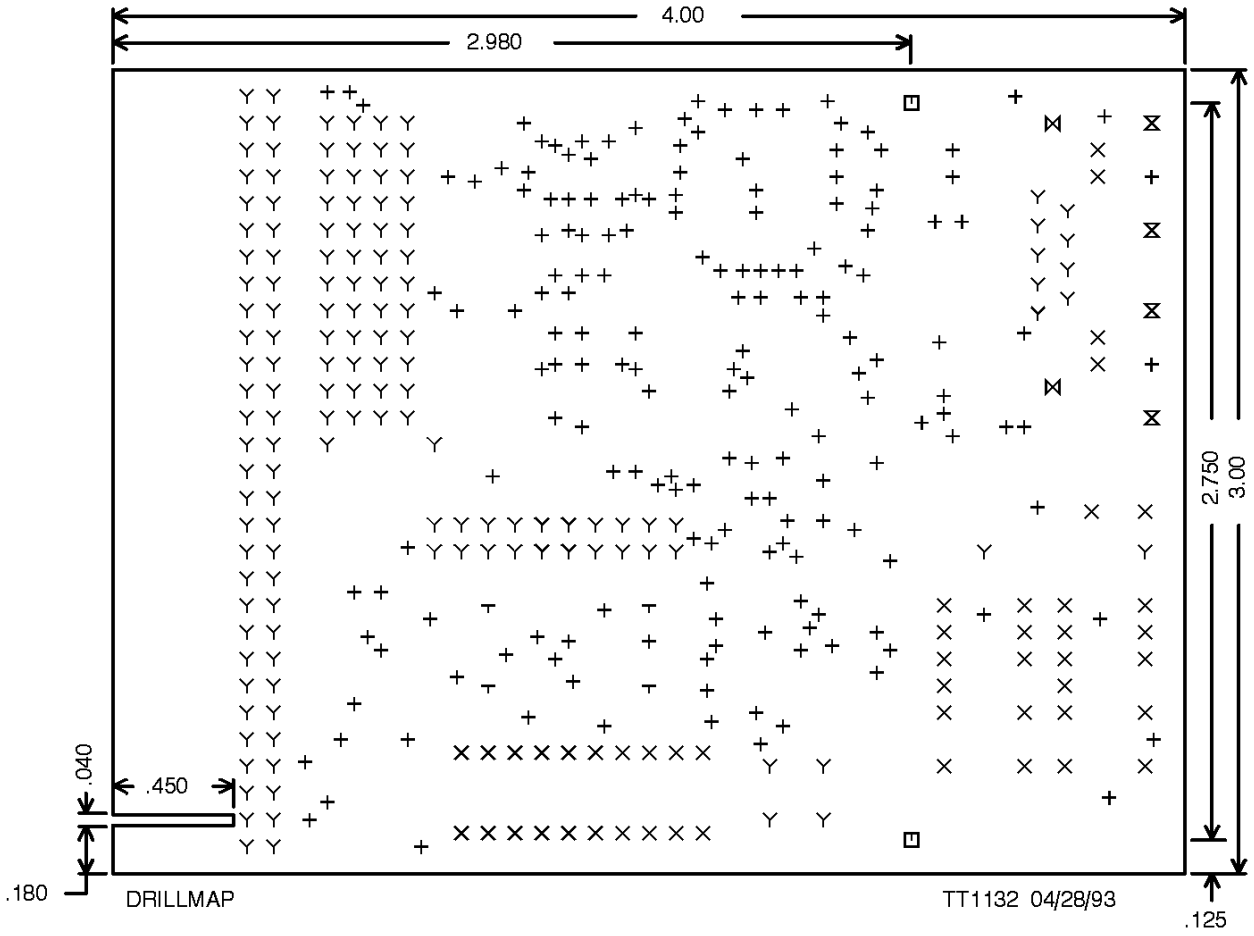
Appendix E. CY9266–C/T Artwork — Bottom Layer Copper



Appendix E. CY9266–C/T Artwork — Bottom Silkscreen



Appendix E. CY9266–C/T Artwork — Drill Chart



TOOL	SIZE	SYM	QTY	PLT
T01	.020	+	179	Y
T02	.032	×	48	Y
T03	.040	Y	143	Y
T04	.052	⊤	4	Y
T05	.080	⧖	4	Y
T06	.125	⋈	2	Y
T06	.156	⊡	2	Y

Appendix F. CY9266 Configuration Guide

Function	JP1 Jumper Settings	Switch SW1 Settings (0=on, 1 = off)									
		1	2	3	4	5	6	7	8	9	10
Xmtr BIST Enable *		0									
Xmtr BIST External *		1									
Xmtr Encode Mode *			0								
Xmtr Bypass Mode *			1								
Xmtr ENA Active *				0							
Xmtr ENA External *				1							
Xmtr ENN Active *					0						
Xmtr ENN External *					1						
Rcvr BIST Enable *						0					
Rcvr BIST External *						1					
Rcvr Decode Mode *							0				
Rcvr Bypass Mode *							1				
Rcvr Port A Selected *	CX–CY							1			
Rcvr Port B Selected *								0			
Xmtr Enabled (FOTO Off) *	EX–EY								0		
Xmtr External *									1		
Active HIGH Carrier Detect *										0	
Active LOW Carrier Detect *										1	
Active HIGH Byte Sync *							1				1
							0				0
Active LOW Byte Sync *							1				0
							0				1
Rcvr Port Select DIP	CX–CY										
Rcvr Port Select External	BX–BY										
FOTO Select DIP	EX–EY										
FOTO Select External	FX–FY										
Xmtr Clock Local Oscillator	GY–HY										
Xmtr Clock XMITCLOCK	GX–GY										
Rcvr Clock Local Oscillator	IX–IY										
Rcvr Clock XMITCLOCK	HX–IX										
Rcvr Clock EXTREFCLK	IX–JX										
OLC–266 Mode	BX–BY, FX–FY, GX–GY, HX–IX	1	1	1	0	1	1			1	1
BIST Mode w/Cable (Standalone)	CX–CY, EX–EY, GY–HY, IX–IY	0		0	1	0		1	0		
BIST Mode wo/Cable (Standalone)	CX–CY, EX–EY, GY–HY, IX–IY	0		0	1	0		0	0		

* – These SW1 controlled signals have a 5.1-kΩ pull-up resistor on the CY9266 card, and may be controlled externally when the SW1 switch is in the off position. With no attached external driver these signals go to a logic-1 state when the SW1 switch position is off.