

# TLD2252-2EP

## LITIX™ Basic+



### Features

- Dual channel device with integrated and protected output stage (current source), optimized to drive LEDs as additional low cost current source
- Optimized for low cost combined “stop”/ “tail” function in Rear Combination Light (RCL)
- Asymmetric output stages to enhance luminosity control for different functions
- High output current (up to 120 mA)
- Very low current consumption in sleep mode
- Very low output leakage when channel is “off”
- Low current consumption during fault
- Independent output currents’ control via low power resistors
- Additional output current demand supported by LITIX™ Companion direct drive
- PWM engine supports digital dimming with very high accuracy
- Intelligent fault management: up to 16 devices can share a common error network with only one external resistor
- Reverse polarity protection allows reduction of external components and improves system performance at low battery/input voltages
- Overload protection
- Wide temperature range:  $-40^{\circ}\text{C} < T_J < 150^{\circ}\text{C}$
- Output current control via external low power resistor
- Green product (RoHS compliant)



### Potential applications

- Cost effective “stop”/ “tail” function implementation with shared and separated LEDs per function
- Turn indicators
- Position, fog, rear lights and side markers
- Animated light functions like wiping indicators and “welcome/goodbye” functions
- Day Running Light
- Interior lighting functions like ambient lighting (including RGB color control), illumination and dash board lighting
- LED indicators for industrial applications and instrumentation

## Product validation

Qualified for Automotive Applications. Product Validation according to AEC-Q100/101.

## Description

The LITIX™ Basic+ TLD2252-2EP is a dual channel high-side driver IC with integrated output stages. It is designed to control LEDs with a current up to 120 mA. In typical automotive applications the device is capable of driving 3 red LEDs per chain (total 6 LEDs) with a current up to 100 mA and even above, if not limited by the overall system thermal properties. Practically, the output current is controlled by an external resistor or reference source, independently from load and supply voltage changes.

**Table 1 Product summary**

Parameter	Symbol	Values
Operating voltage	$V_{S(nom)}$	5.5 V ... 40 V
Maximum voltage	$V_{S(max)}$ $V_{OUT1/2(max)}$	40 V
Nominal output (load) currents	$I_{OUT1/2(nom)}$	50/100 mA (nominal) when using the automotive supply voltage range 8 V - 18 V. Currents up to $I_{OUT1/2(max)}$ are possible with low thermal resistance $R_{thJA}$
Maximum output (load) currents	$I_{OUT1/2(max)}$	60/120 mA depending on $R_{thJA}$
Current accuracy at $R_{SET} = 10\text{ k}\Omega$	$K_{RTx}$	300/600 $\pm$ 3.33%
Current consumption in sleep mode	$I_{S(sleep, typ)}$	0.1 $\mu$ A
Maximum current consumption during fault	$I_{S(fault, ERRN)}$	850 $\mu$ A or less when fault is detected from another device (disabled via ERRN) and all channels are deactivated (D-pin open)

Type	Package	Marking
TLD2252-2EP	PG-TSDSO-14	TLD2252

## Table of Contents

<b>1</b>	<b>Block diagram</b> .....	<b>4</b>
<b>2</b>	<b>Pin configuration</b> .....	<b>5</b>
2.1	Pin assignment .....	5
2.2	Pin definitions and functions .....	5
<b>3</b>	<b>General product characteristics</b> .....	<b>7</b>
3.1	Absolute maximum ratings .....	7
3.2	Functional range .....	8
3.3	Thermal resistance .....	9
<b>4</b>	<b>Internal supply</b> .....	<b>10</b>
4.1	Description .....	10
4.2	Electrical characteristics internal supply and ENx pins .....	12
<b>5</b>	<b>Power stages</b> .....	<b>14</b>
5.1	Protection .....	14
5.1.1	Thermal protection .....	14
5.1.2	Reverse battery protection .....	15
5.2	Output configuration via IN_SETx pins .....	15
5.2.1	IN_SETx pins .....	15
5.2.2	Output current adjustment via $R_{SET}$ .....	15
5.2.3	Output control via IN_SETx .....	16
5.2.4	IN_SETx pins behavior during device fault management .....	17
5.2.5	Timing diagrams .....	17
5.3	Electrical characteristics power stage .....	18
5.4	Electrical characteristics IN_SETx and PWMI pins for output settings .....	20
<b>6</b>	<b>Load diagnosis</b> .....	<b>21</b>
6.1	Error management via ERRN and D-pins .....	21
6.1.1	ERRN pin .....	21
6.1.2	D-pin .....	23
6.2	Overtemperature (OT), Open Load (OL) and short OUTx to GND (SC) .....	24
6.2.1	Fault management (D-pin open or connected with a capacitor to GND) .....	24
6.2.2	Fault management (D-pin connected to GND) .....	27
6.3	Electrical characteristics: Load diagnosis and Overload management .....	30
<b>7</b>	<b>PWM control (Digital dimming)</b> .....	<b>32</b>
7.1	PWM unit .....	32
7.2	Direct control of PWMI .....	33
7.3	Timing diagrams .....	34
7.4	Electrical characteristics PWM engine .....	34
<b>8</b>	<b>Application information</b> .....	<b>37</b>
<b>9</b>	<b>Package outline</b> .....	<b>38</b>
<b>10</b>	<b>Revision History</b> .....	<b>39</b>

Block diagram

# 1 Block diagram

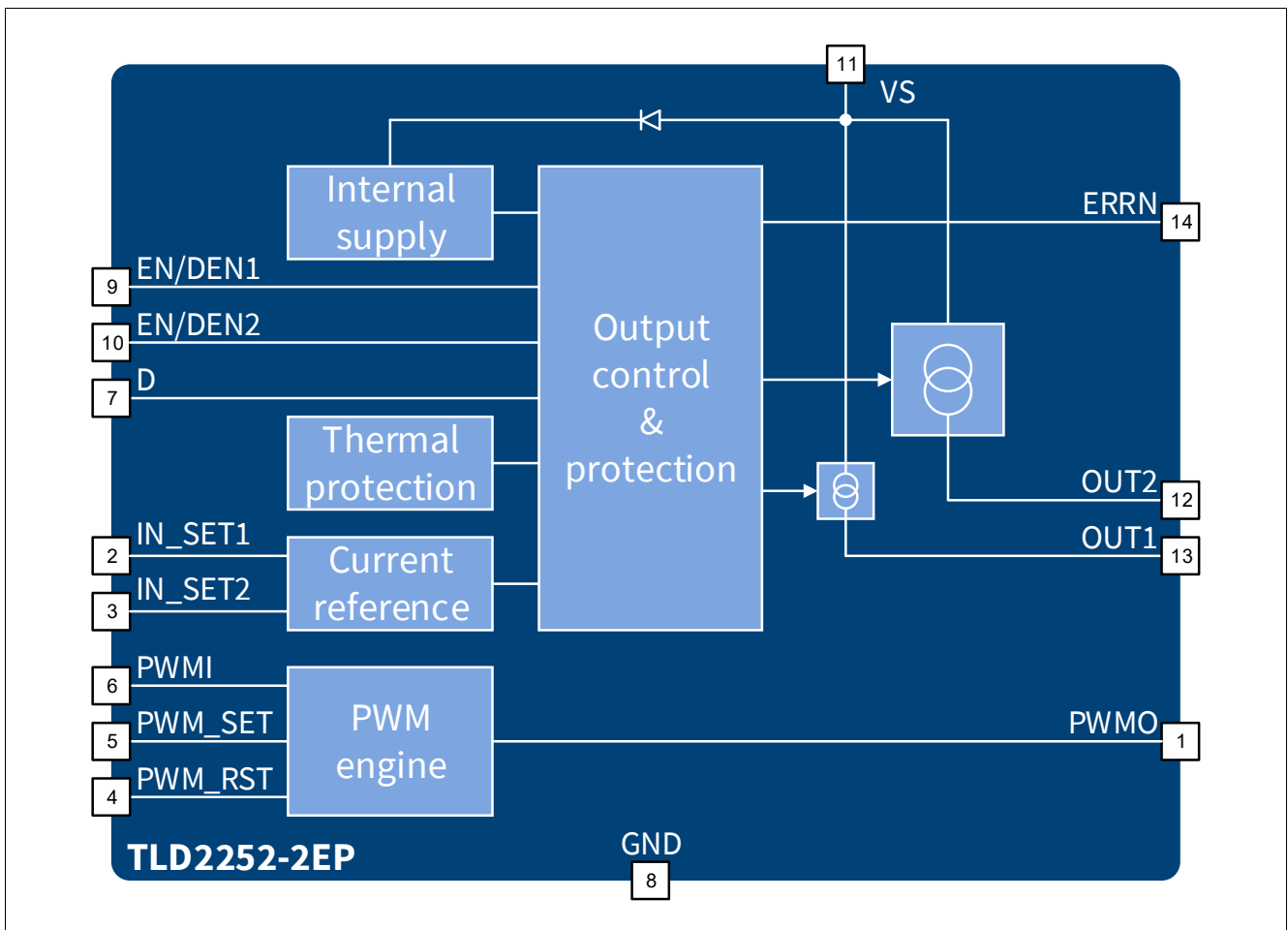


Figure 1 Block diagram

Pin configuration

## 2 Pin configuration

### 2.1 Pin assignment

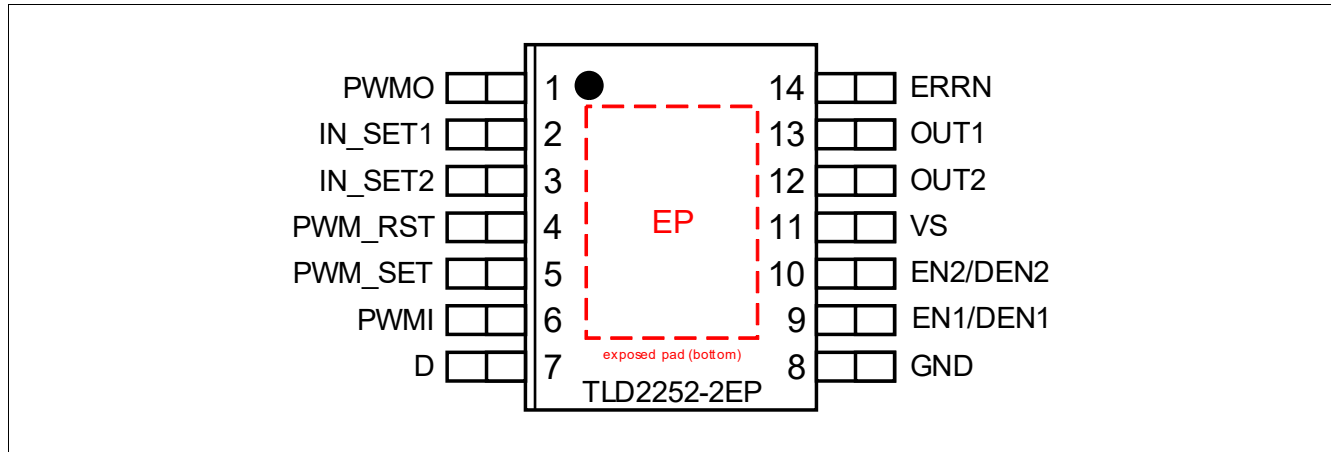


Figure 2 Pin configuration

### 2.2 Pin definitions and functions

Pin	Symbol	Function
11	VS	<b>Supply voltage;</b> Connected to battery or supply control switch, with EMC filter
8	GND	<b>Ground;</b> Signal ground
2	IN_SET1	<b>Control input for OUT1 channel;</b> Connect to a low power resistor to adjust OUT1 output current. Alternatively, a different current reference (i.e. the OUT_SET of another LITIX™ Basic+ LED Driver) may be connected
3	IN_SET2	<b>Control input for OUT2 channel;</b> Connect to a low power resistor to adjust OUT2 output current. Alternatively, a different current reference (i.e. the OUT_SET of another LITIX™ Basic+ LED Driver) may be connected
6	PWMI	<b>PWM input;</b> Connect to an external PWM controller or a ceramic capacitor (when internal PWM engine is intended to be used). If not used, connect to GND
1	PWMO	<b>PWM output;</b> Buffered PWMI logic state. Used to drive additional devices with same timing as PWMI. If not used, leave the pin open
4	PWM_RST	<b>PWM duty cycle reset input;</b> Connect to a low power resistor to adjust PWM frequency and duty cycle. If the internal PWM engine is not used (direct PWMI drive) it should be left open
5	PWM_SET	<b>PWM duty cycle set input;</b> Connect to a low power resistor to adjust PWM frequency and duty cycle. If the internal PWM engine is not used (direct PWMI drive) it should be left open
7	D	<b>Disable/delay error input;</b> Connect to a capacitor, leave open or connect to GND, depending on the required diagnosis management (see <a href="#">Chapter 6</a> for further details)

**Pin configuration**

<b>Pin</b>	<b>Symbol</b>	<b>Function</b>
14	ERRN	<b>ERROR flag I/O;</b> Open drain, active low. Connect to a pull-up resistor
9	EN1/DEN1	<b>Channel 1 output enable and diagnosis control input;</b> Connect to a control input (i.e. to VS via a resistor divider or a Zener diode) to enable OUT1 control and Diagnosis
10	EN2/DEN2	<b>Channel 2 output enable and diagnosis control input;</b> Connect to a control input (i.e. to VS via a resistor divider or a Zener diode) to enable OUT2 control and Diagnosis
13	OUT1	<b>Channel 1 output pin;</b> Connect to the target load
12	OUT2	<b>Channel 2 output pin;</b> Connect to the target load
Exposed Pad	EP	<b>Exposed Pad;</b> Connected to GND-pin in application

General product characteristics

### 3 General product characteristics

#### 3.1 Absolute maximum ratings

**Table 2 Absolute maximum ratings<sup>1)</sup>**

$T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ;  $R_{IN\_SETx} = 10\text{ k}\Omega$ ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>Voltage</b>							
Supply voltage	$V_S$	-18	–	40	V	–	P_4.1.1
EN/DENx voltages	$V_{EN/DENx}$	-18	–	40	V	–	P_4.1.3
EN/DENx voltages related to $V_S$ : $V_{EN/DENx} - V_S$	$V_{EN/DENx(VS)}$	-40	–	18	V	–	P_4.1.4
EN/DENx voltages related to $V_{OUTx}$ : $V_{EN/DENx} - V_{OUTx}$	$V_{EN/DENx(VOUTx)}$	-18	–	40	V	–	P_4.1.5
Output voltages	$V_{OUTx}$	-1	–	40	V	–	P_4.1.10
Output voltages related to $V_S$ : $V_{OUTx(VS)} - V_{OUTx}$	$V_{OUTx(VS)}$	-18	–	40	V	–	P_4.1.11
IN_SETx voltages	$V_{IN\_SETx}$	-0.3	–	6	V	–	P_4.1.12
PWMI voltage	$V_{PWMI}$	-0.3	–	6	V	–	P_4.1.14
PWMO voltage	$V_{PWMO}$	-0.3	–	6	V	–	P_4.1.15
PWM_RST voltage	$V_{PWM\_RST}$	-0.3	–	6	V	–	P_4.1.16
PWM_SET voltage	$V_{PWM\_SET}$	-0.3	–	6	V	–	P_4.1.17
ERRN voltage	$V_{ERRN}$	-0.3	–	40	V	–	P_4.1.18
D Voltage	$V_D$	-0.3	–	6	V	–	P_4.1.19
<b>Current</b>							
Output current (Output channel OUT1)	$I_{OUT1}$	0	–	70	mA	–	P_4.1.24
Output current (Output channel OUT2)	$I_{OUT2}$	0	–	130	mA	–	P_4.1.25
PWMI current	$I_{PWMI}$	-0.5	–	0.5	mA	–	P_4.1.26
PWMO current	$I_{PWMO}$	-2	–	2	mA	–	P_4.1.27
PWM_RST current	$I_{PWM\_RST}$	0	–	300	$\mu\text{A}$	–	P_4.1.28
PWM_SET current	$I_{PWM\_SET}$	0	–	300	$\mu\text{A}$	–	P_4.1.29
IN_SETx currents	$I_{IN\_SETx}$	0	–	300	$\mu\text{A}$	–	P_4.1.30
D current	$I_D$	-0.5	–	0.5	mA	–	P_4.1.31
<b>Temperature</b>							
Junction temperature	$T_J$	-40	–	150	$^\circ\text{C}$	–	P_4.1.33
Storage temperature	$T_{stg}$	-55	–	150	$^\circ\text{C}$	–	P_4.1.34

**General product characteristics**

**Table 2 Absolute maximum ratings<sup>1)</sup>** (cont'd)

$T_J = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ;  $R_{IN\_SETX} = 10\text{ k}\Omega$ ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>ESD susceptibility</b>							
ESD susceptibility all pins to GND	$V_{ESD}$	-2	–	2	kV	HBM <sup>2)</sup>	P_4.1.36
ESD susceptibility all pins to GND	$V_{ESD}$	-500	–	500	V	CDM <sup>3)</sup>	P_4.1.37
ESD susceptibility Pin 1, 7, 8, 14 (corner pins) to GND	$V_{ESD1,7,8,14}$	-750	–	750	V	CDM <sup>3)</sup>	P_4.1.38

1) Not subject to production test, specified by design

2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF)

3) ESD susceptibility, Charged Device Model “CDM” according JEDEC JESD22-C101

**Notes**

1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

**3.2 Functional range**

**Table 3 Functional range**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltage range for normal operation	$V_{S(nom)}$	5.5	–	18	V	–	P_4.2.1
Extended supply voltage for functional range	$V_{S(ext)}$	$V_{SUV(ON)}$	–	40	V	–	P_4.2.2
Junction temperature	$T_J$	-40	–	150	°C	–	P_4.2.4

Note: Within the Normal Operation range, the IC operates as described in the circuit description. Within the Extended Operation range, parameters deviations are possible. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.



**General product characteristics**

**3.3 Thermal resistance**

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to [www.jedec.org](http://www.jedec.org).

**Table 4 Thermal resistance<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to Case	$R_{thJC}$	–	–	10	K/W	<sup>1)2)</sup>	P_4.3.1
Junction to Ambient 1s0p board	$R_{thJA1}$	–	61 56	–	K/W	<sup>1)3)</sup> $T_A = 85^\circ\text{C}$ $T_A = 135^\circ\text{C}$	P_4.3.3
Junction to Ambient 2s2p board	$R_{thJA2}$	–	45 43	–	K/W	<sup>1)4)</sup> $T_A = 85^\circ\text{C}$ $T_A = 135^\circ\text{C}$	P_4.3.4

- 1) Not subject to production test, specified by design
- 2) Specified  $R_{thJC}$  value is simulated at natural convection on a cold plate setup (all pins and exposed pad are fixed to ambient temperature).  $T_A = 85^\circ\text{C}$ . Total power dissipation = 1.5 W
- 3) Specified  $R_{thJA}$  value is according to Jedec JESD51-3 at natural convection on FR4 1s0p board. The product (chip+package) was simulated on a  $76.2 \times 114.3 \times 1.5$  mm board with  $70 \mu\text{m}$  Cu,  $300 \text{ mm}^2$  cooling area. Total power dissipation 1.5 W distributed statically and homogenously over all power stages
- 4) Specified  $R_{thJA}$  value is according to Jedec JESD51-5,-7 at natural convection on FR4 2s2p board; The product (chip+package) was simulated on a  $76.2 \times 114.3 \times 1.5$  mm board with 2 inner copper layers ( $2 \times 70 \mu\text{m}$  Cu,  $2 \times 35 \mu\text{m}$  Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer. Total power dissipation 1.5 W distributed statically and homogenously over all power stages

Internal supply

## 4 Internal supply

This chapter describes the internal supply in its main parameters and functionality.

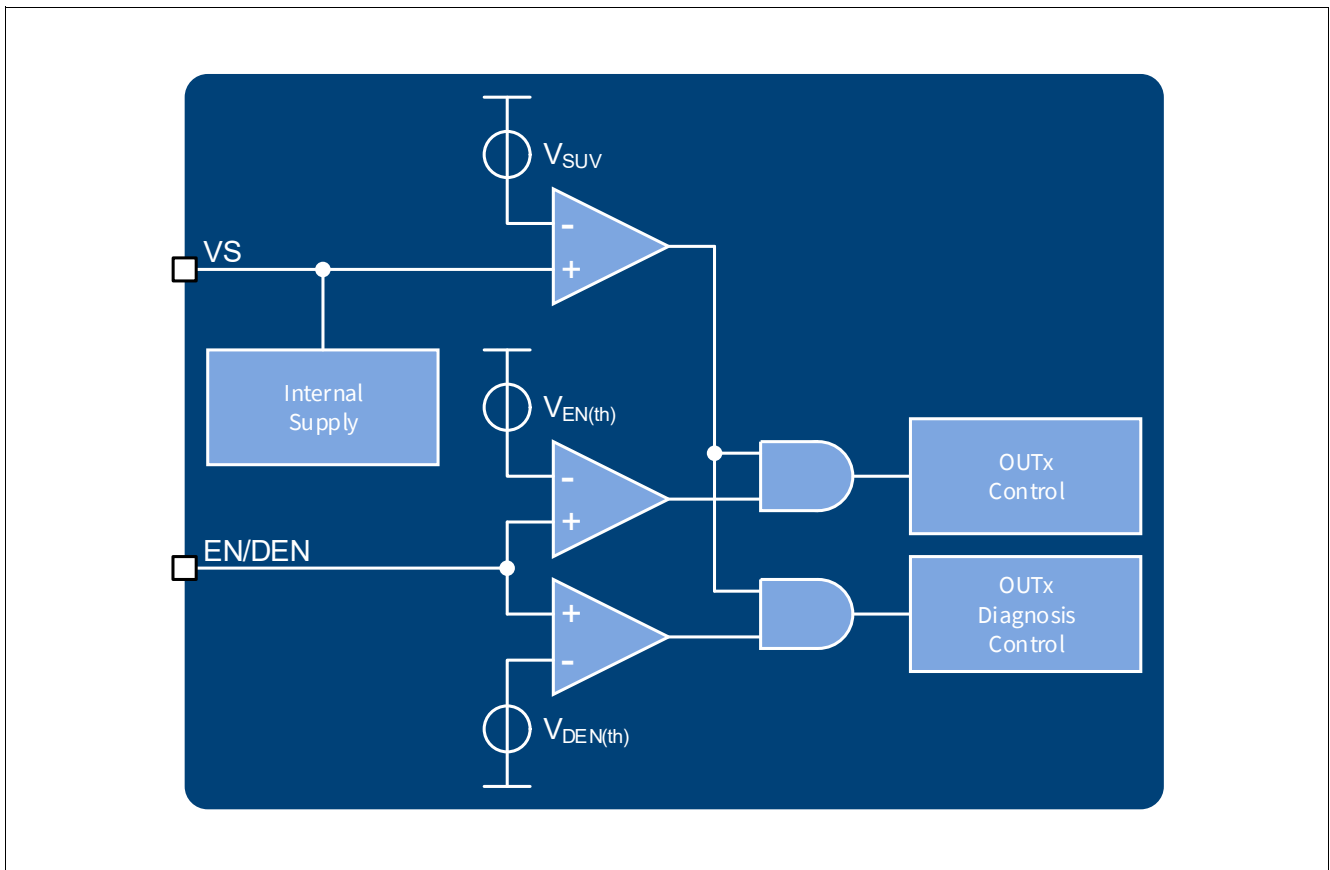
### 4.1 Description

The internal supply principle is highlighted in the concept diagram of [Figure 3](#).

If the voltage applied at both the EN/DEN pins are below  $V_{ENx(th)}$  the device enters sleep mode. In this state all internal functions are switched off and the current consumption is reduced to  $I_{S(sleep)}$ .

As soon as the voltage applied at the supply pin  $V_S$  is above  $V_{SUV(ON)}$  and the voltage applied at one of the EN/DEN pins are above  $V_{ENx(th)}$ , after the power-on reset time  $t_{POR}$ , the device is ready to deliver output current from the relative output stage. The power on reset time  $t_{POR}$  has to be taken into account also in relevant application conditions, i. e. with PWM control from  $V_S$  or EN/DEN lines.

Also if PWM control is done via the PWM engine, the conditions  $V_S > V_{SUV(ON)}$  and  $V_{ENn} > V_{ENx(th)}$  must be fulfilled for PWM engine (and, therefore, output) activation.



**Figure 3** Internal supply

Furthermore, as soon as the voltage applied at the supply pin  $V_S$  is above  $V_{SUV(ON)}$  and the voltage applied to one of the EN/DENx pins  $V_{ENx}$  are above  $V_{DENx(th)}$ , the device is ready to detect and report fault conditions via ERRN (error network pin) as described in [Chapter 6](#).

To program outputs enable and diagnosis enable via EN/DENx pins there are several possibilities, like a resistor divider from  $V_S$  to GND, a Zener diode from EN/DENx to  $V_S$  and also a logic control pin (e.g. from a microcontroller output).

Internal supply

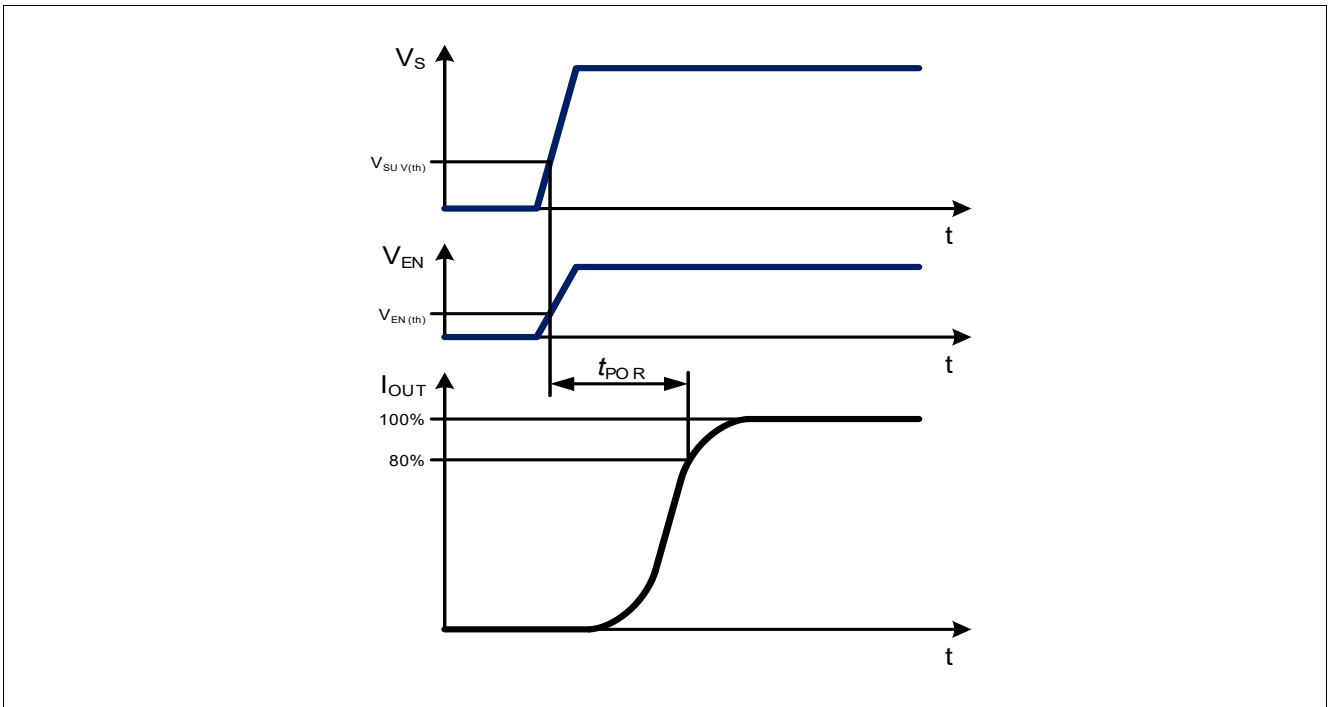


Figure 4 Power on reset timing diagram

Internal supply

4.2 Electrical characteristics internal supply and ENx pins

**Table 5 Electrical characteristics: Internal supply and ENx pins**

$T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ;  $V_S = 5.5\text{ V}$  to  $18\text{ V}$ ;  $R_{IN\_SETx} = 10\text{ k}\Omega$ ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption, sleep mode	$I_{S(\text{sleep})}$	–	0.1	2	$\mu\text{A}$	<sup>1)</sup> $V_{ENx} = 0\text{ V}$ $T_J < 85^\circ\text{C}$ $V_S = 18\text{ V}$ $V_{OUTx} = 3.6\text{ V}$	P_5.2.1
Current consumption, active mode (no fault)	$I_{S(\text{active})}$	–	1.5	3	$\text{mA}$	$V_{ENx} = 5.5\text{ V}$ $I_{IN\_SETx} = 0\text{ }\mu\text{A}$ $T_J < 105^\circ\text{C}$ $V_S = 18\text{ V}$ $V_{OUTx} = 3.6\text{ V}$ $I_{PWM\_SET} = I_{PWM\_RST} = 100\text{ }\mu\text{A}$	P_5.2.3
Current consumption during fault condition triggered from another device sharing ERRN bus (all channels deactivated)	$I_{S(\text{fault, ERRN})}$	–	–	850	$\mu\text{A}$	$V_{ENx} = 5.5\text{ V}$ $T_J < 105^\circ\text{C}$ $V_S = 18\text{ V}$ $V_{ERRN} = 0\text{ V}$ $V_{OUTx} = 3.6\text{ V}$ D open	P_5.2.4
Current consumption during fault condition (all channels deactivated)	$I_{S(\text{fault, OUT})}$	–	–	1.25	$\text{mA}$	$V_{ENx} = 5.5\text{ V}$ $T_J < 105^\circ\text{C}$ $V_S = 18\text{ V}$ $V_{OUT1} = 0\text{ V}$ $V_{OUT2}$ D open	P_5.2.16

**Supply thresholds**

Required supply voltage for output activation	$V_{SUV(\text{ON})}$	–	–	5.5	$\text{V}$	$V_{ENx} = V_S$ $V_{OUTx} = 3\text{ V}$ $R_{IN\_SETx} = 6.8\text{ k}\Omega$ $I_{OUTx} > 50\%$ $I_{OUTx(\text{nom})}$	P_5.2.5
Required supply voltage for output deactivation	$V_{SUV(\text{OFF})}$	4.5	–	–	$\text{V}$	$V_{ENx} = V_S$ $V_{OUTx} = 3\text{ V}$ $R_{IN\_SETx} = 6.8\text{ k}\Omega$ $I_{OUTx} < 50\%$ $I_{OUTx(\text{nom})}$	P_5.2.6
Supply voltage activation hysteresis: $V_{SUV(\text{ON})} - V_{SUV(\text{OFF})}$	$V_{SUV(\text{hys})}$	–	200	–	$\text{mV}$	<sup>1)</sup> $V_{ENx} > V_{EN(\text{th})}$	P_5.2.8

**Internal supply**

**Table 5 Electrical characteristics: Internal supply and ENx pins (cont'd)**

$T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ;  $V_S = 5.5\text{ V}$  to  $18\text{ V}$ ;  $R_{IN\_SETx} = 10\text{ k}\Omega$ ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>EN pins</b>							
ENx output enable threshold	$V_{ENx(th)}$	1.4	1.65	1.8	V	$V_S = 5.5\text{ V}$ $V_{PS} = 2\text{ V}$ $R_{IN\_SETx} = 6.8\text{ k}\Omega$ $I_{OUTx} = 50\%$ $I_{OUTx(nom)}$	P_5.2.9
DENx diagnosis enable threshold	$V_{DENx(th)}$	2.4	2.5	2.7	V	$V_S = 5.5\text{ V}$	P_5.2.11
DENx diagnosis enable hysteresis	$V_{DENx(hys)}$	–	120	–	mV	<sup>1)</sup> $R_{IN\_SETx} = 6.8\text{ k}\Omega$	P_5.2.12
EN/DENx pull-down current	$I_{EN/DENx(PD)}$	–	–	15	$\mu\text{A}$	<sup>1)</sup> $V_S > 8\text{ V}$ $V_{EN/DENx} = 2.8\text{ V}$	P_5.2.17
EN/DENx pull-down current	$I_{EN/DENx(PD)}$	–	–	35	$\mu\text{A}$	<sup>1)</sup> $V_S > 8\text{ V}$ $V_{EN/DENx} = 5.5\text{ V}$	P_5.2.14
EN/DENx pull-down current	$I_{EN/DENx(PD)}$	–	–	150	$\mu\text{A}$	<sup>1)</sup> $V_S > 8\text{ V}$ $V_{EN/DENx} = V_S$	P_5.2.15
<b>Timing</b>							
Power on reset delay time	$t_{POR}$	–	–	25	$\mu\text{s}$	<sup>1)</sup> $V_S$ rising from 0 V to 13.5 V $V_{OUTx} = 3.6\text{ V}$ $R_{IN\_SETx} = 6.8\text{ k}\Omega$ $I_{OUTx} = 80\%$ $I_{OUTx(nom)}$	P_5.2.13

1) Not subjected to production test: specified by design

Power stages

## 5 Power stages

The two asymmetric output stages are realized as high-side current sources with an output current up to 60/120mA. During off state the leakage current at the output stages is minimized in order to prevent a slightly glowing LED.

The maximum output current is limited by the power dissipation and used PCB cooling areas.

For an operating output current control loop, the supply and output voltages have to be considered according to the following parameters:

- Required supply voltage for current control  $V_{S(CC)}$
- Voltage drop over through the output stage during current control  $V_{PSx(CC)}$
- Required output voltage for current control  $V_{OUTx(CC)}$

### 5.1 Protection

The device provides embedded protective functions, which are designed to prevent IC damage under fault conditions described in this datasheet. Fault conditions are considered as “outside” normal operating range. Protective functions are not designed for continuous nor for repetitive operations.

#### 5.1.1 Thermal protection

A thermal protection circuitry is integrated in the device. It is realized by a temperature monitoring of the output stages.

As soon as the junction temperature exceeds the overtemperature threshold  $T_{JSD}$  the output current of both channels is disabled and (provided that D-pin is left open or capacitively connected to GND) the IN\_SETx pins go in a weak pull-down state with a current consumption  $I_{IN\_SETx(fault)}$ . If the junction temperature cools down below  $T_{JSD} - T_{J(hys)}$ , the IN\_SET pins rise again to  $V_{IN\_SETx(ref)}$  (within an additional time  $t_{IN\_SETx(del)}$ ) and consequently, the output currents rise again (see [Chapter 6](#) for a detailed description of fault management).

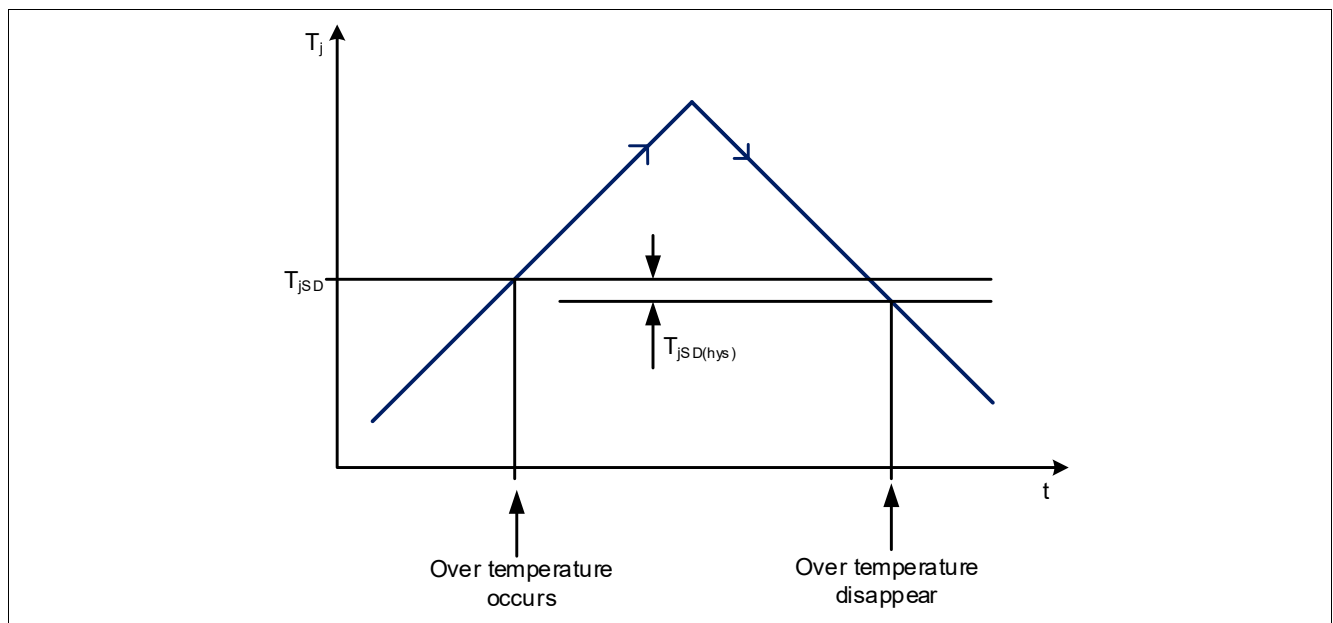


Figure 5 Overtemperature shut down auto-restart thresholds

As long as the device remains into overtemperature condition, ERRN pin remains low.

Power stages

### 5.1.2 Reverse battery protection

The device has an integrated reverse battery protection feature. This feature protects the driver IC itself and, potentially, also connected LEDs. The output reverse current is limited to  $I_{OUTx(REV)}$  by the reverse battery protection.

## 5.2 Output configuration via IN\_SETx pins

Outputs current can be defined via IN\_SETx and pins.

### 5.2.1 IN\_SETx pins

The IN\_SETx pins are multiple function pins for the outputs current definition and inputs control. Output currents definition and analog dimming control can be done defining accordingly the IN\_SETx currents.

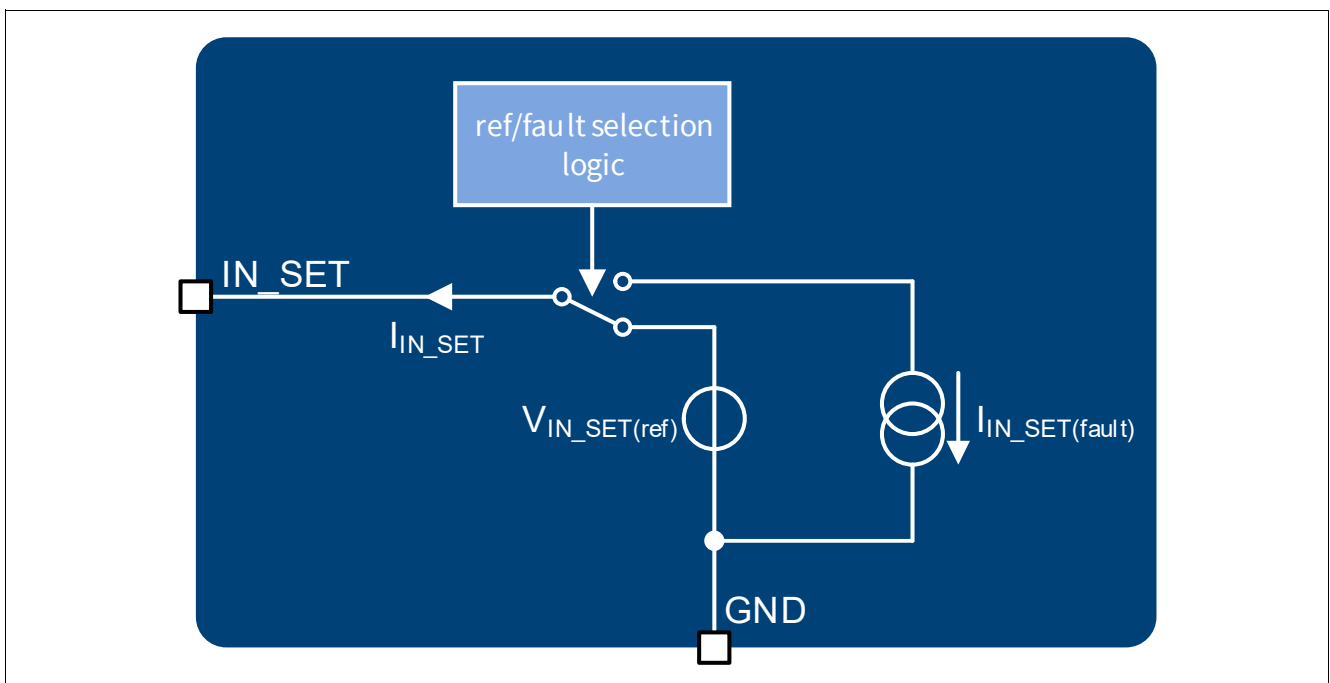


Figure 6 IN\_SETx pins block diagram

### 5.2.2 Output current adjustment via R<sub>SET</sub>

The output current for the channels can be defined connecting a low power resistor ( $R_{SETx}$ ) between the IN\_SETx pins and GND. The dimensioning of the resistors can be done using the formula:

$$I_{OUTx} = k \cdot I_{IN\_SETx} = k \cdot V_{IN\_SETx(ref)} / R_{SETx} \quad (5.1)$$

The gain factor  $k_x$  (defined as the ratio  $I_{OUTx}/I_{IN\_SETx}$ ) is graphically described in [Figure 7](#).

The current through the  $R_{SETx}$  is defined by the resistor itself and the reference voltage  $V_{IN\_SETx(ref)}$ , which is applied to the IN\_SETx pin when the device is supplied and the channel enabled.

Power stages

### 5.2.3 Output control via IN\_SETx

The IN\_SETx pins can be connected via their  $R_{SETx}$  to the open-drain outputs of a microcontroller or to an external NMOS transistor as described in [Figure 9](#). This signal can be used to turn off the relative output stages of the IC.

A minimum IN\_SETx current of  $I_{IN\_SETx(ACT)}$  is required to turn on the output stages. This feature is implemented to prevent glowing of LEDs caused by leakage currents on the IN\_SETn pins, see again [Figure 7](#) for details.

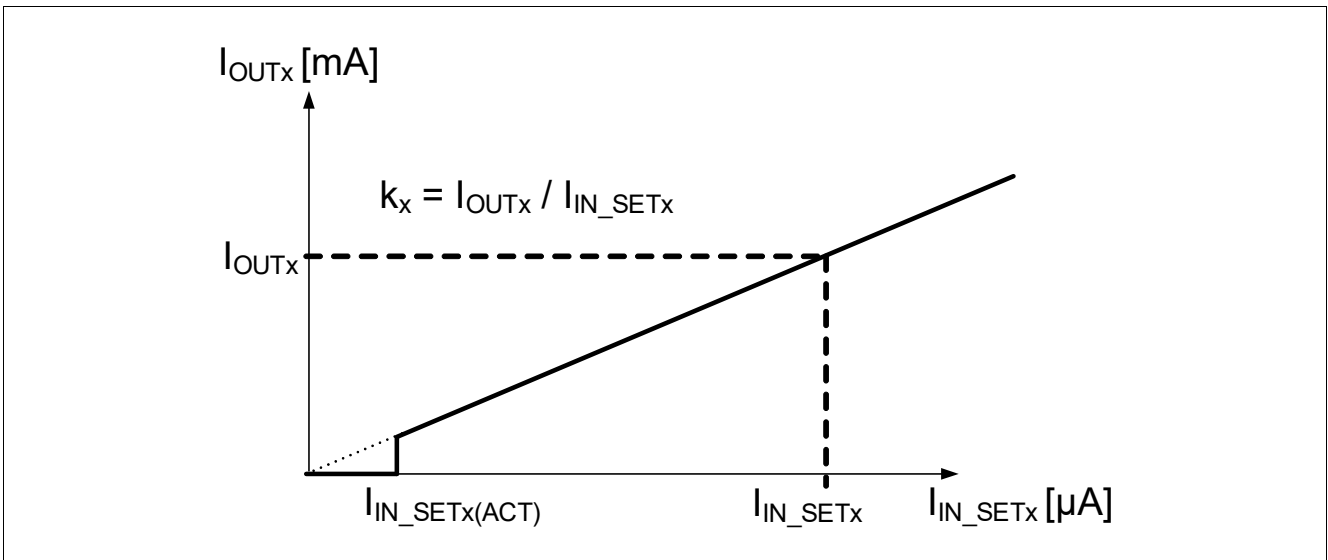


Figure 7  $I_{OUTx}$  vs  $I_{IN\_SETx}$

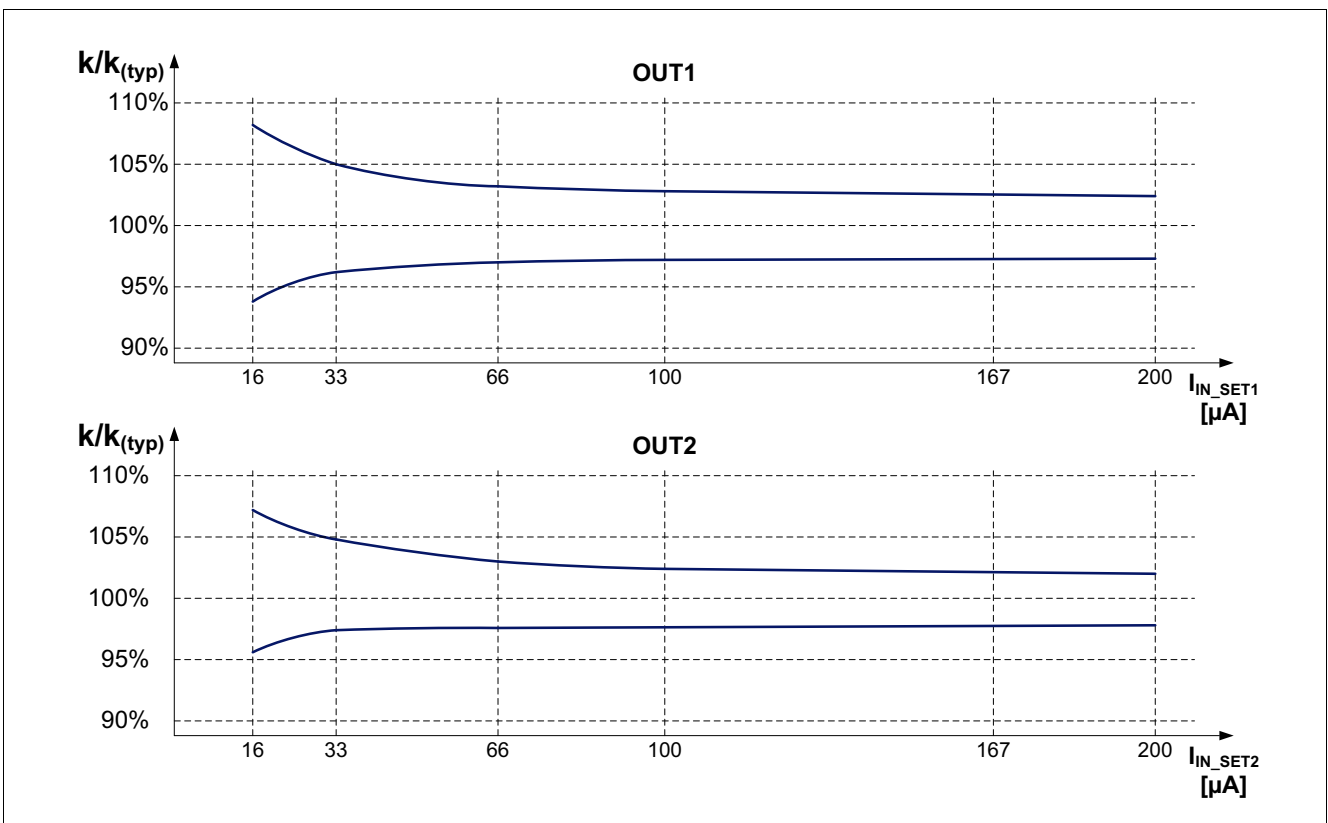


Figure 8 Typical output current accuracy  $I_{OUT} / I_{IN\_SET}$  at  $T_J = 25^\circ C$



Power stages

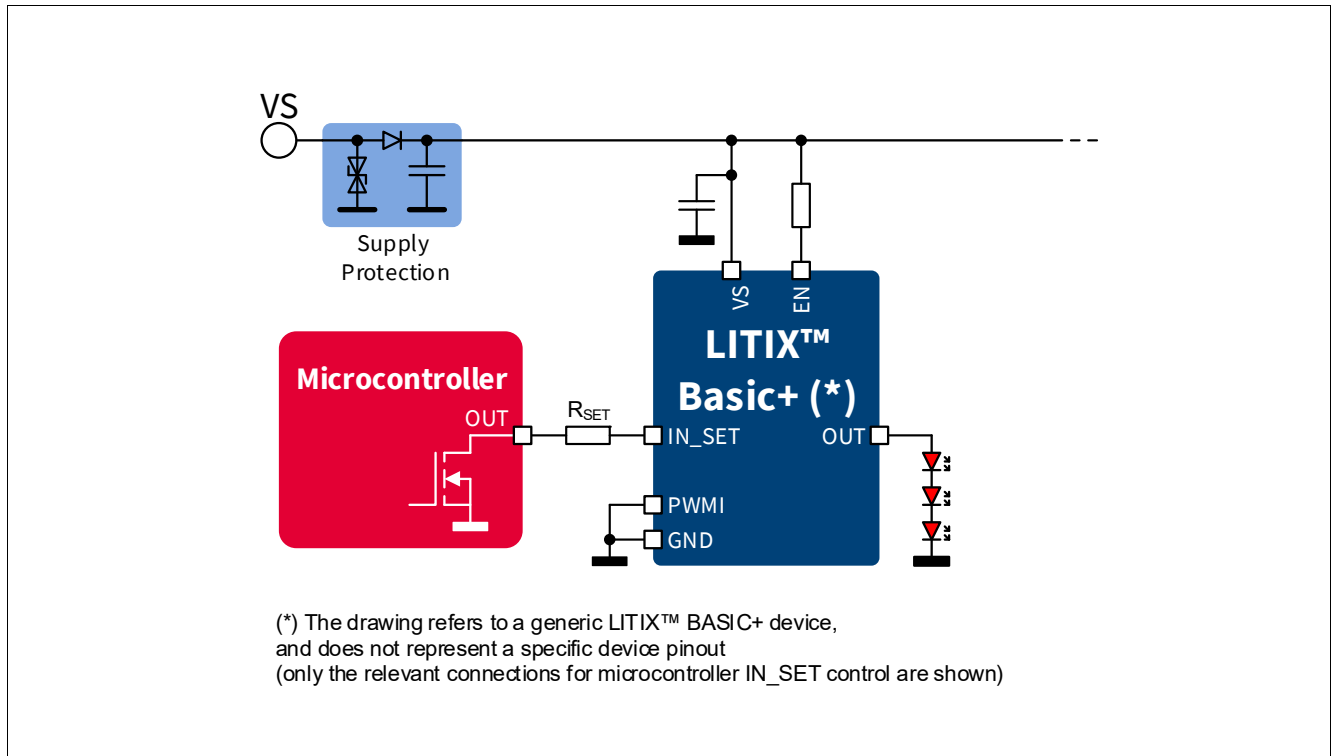


Figure 9 Output control via IN\_SET pin and open-drain microcontroller out (simplified diagram)

5.2.4 IN\_SETx pins behavior during device fault management

If a fault condition arises on the channel controlled by the IN\_SETx pins, once the D-pin reaches the high level threshold  $V_{D(th)}$ , the current of all the IN\_SETx pins is reduced to  $I_{IN\_SETx(fault)}$ , in order to minimise the current consumption of the whole device under fault condition (detailed description is in the load diagnosis section, Chapter 6).

5.2.5 Timing diagrams

In the following diagrams (Figure 10) the influences of input on output deactivation delays are shown.

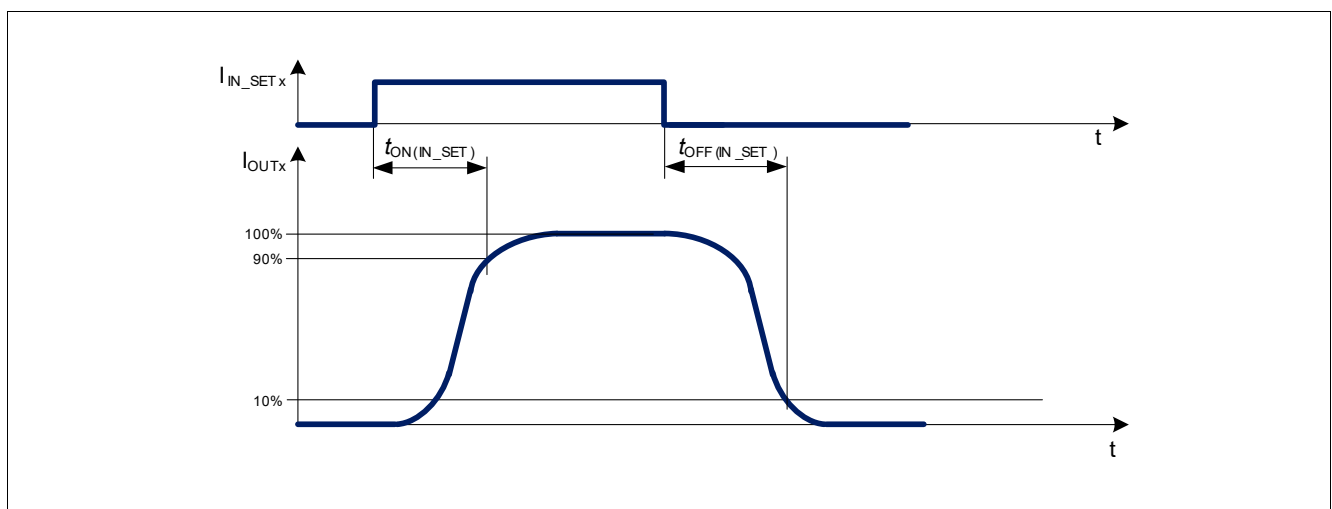


Figure 10 IN\_SET turn on and turn off delay timing diagram

Power stages

5.3 Electrical characteristics power stage

**Table 6 Electrical characteristics: Power stage**

$T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ;  $V_S = 5.5\text{ V}$  to  $18\text{ V}$ ;  $R_{IN\_SETx} = 10\text{ k}\Omega$ ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output leakage currents	$I_{OUTx(Leak)}$	–	–	3	$\mu\text{A}$	<sup>1)</sup> $V_{ENx} = 5.5\text{ V}$ $I_{IN\_SETx} = 0\text{ }\mu\text{A}$ $V_{OUTx} = 2.5\text{ V}$ $T_J = 85^\circ\text{C}$	P_6.5.1
Output leakage currents	$I_{OUTx(Leak)}$	–	–	7	$\mu\text{A}$	<sup>1)</sup> $V_{ENx} = 5.5\text{ V}$ $I_{IN\_SETx} = 0\text{ }\mu\text{A}$ $V_{OUTx} = 2.5\text{ V}$ $T_J = 150^\circ\text{C}$	P_6.5.59
Reverse output currents	$I_{OUTx(rev)}$	–	–	3	$\mu\text{A}$	<sup>1)</sup> $V_{ENx} = V_{Sx}$ $V_{Sx} = -18\text{ V}$ Output load: LED with break down voltage $< -0.6\text{ V}$	P_6.5.2

**Output current accuracy**

Output current accuracy	$K_{RT1}$	290	300	310	–	<sup>1)</sup> $T_J = 25^\circ\text{C}$ $V_S = 12.8\text{ V}$ $V_{PS1} = 2\text{ V}$ $I_{IN\_SET1} = 100\text{ }\mu\text{A}$	P_6.5.16
Output current accuracy	$K_{LT1}$	285	300	315	–	<sup>1)</sup> $T_J = 25\dots 150^\circ\text{C}$ $V_S = 8\dots 18\text{ V}$ $V_{PS1} = 2\text{ V}$ $I_{IN\_SET1} = 100\text{ }\mu\text{A}$	P_6.5.17
Output current accuracy	$K_{ALL1}$	282	300	318	–	<sup>1)</sup> $T_J = -40\dots 150^\circ\text{C}$ $V_S = 8\dots 18\text{ V}$ $V_{PS1} = 2\text{ V}$ $I_{IN\_SET1} = 100\text{ }\mu\text{A}$	P_6.5.18
Output current accuracy	$K_{RT2}$	580	600	620	–	<sup>1)</sup> $T_J = 25^\circ\text{C}$ $V_S = 12.8\text{ V}$ $V_{PS2} = 2\text{ V}$ $I_{IN\_SET2} = 66\text{ }\mu\text{A}$	P_6.5.21
Output current accuracy	$K_{LT2}$	570	600	630	–	<sup>1)</sup> $T_J = 25\dots 150^\circ\text{C}$ $V_S = 8\dots 18\text{ V}$ $V_{PS2} = 2\text{ V}$ $I_{IN\_SET2} = 66\text{ }\mu\text{A}$	P_6.5.22
Output current accuracy	$K_{ALL2}$	564	600	636	–	<sup>1)</sup> $T_J = -40\dots 150^\circ\text{C}$ $V_S = 8\dots 18\text{ V}$ $V_{PS1} = 2\text{ V}$ $I_{IN\_SET1} = 66\text{ }\mu\text{A}$	P_6.5.23

**Power stages**

**Table 6 Electrical characteristics: Power stage (cont'd)**

$T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ;  $V_S = 5.5\text{ V}$  to  $18\text{ V}$ ;  $R_{IN\_SETx} = 10\text{ k}\Omega$ ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Required voltage drop during current control $V_{PSx(CC)} = V_S - V_{OUTx}$	$V_{PSx(CC)}$	1.0	–	–	V	<sup>2)</sup> $V_S = 8\dots 18\text{ V}$ $I_{OUTx} > 90\%$ of $K_{x(typ)} * I_{IN\_SETx}$	P_6.5.36
Required voltage drop during current control $V_{PSx(CC)} = V_S - V_{OUTx}$	$V_{PSx(CC)}$	0.65	–	–	V	<sup>2)</sup> $V_S = 8\dots 18\text{ V}$ $I_{IN\_SETx} = 133\ \mu\text{A}$ $I_{OUTx} > 90\%$ of $K_{x(typ)} * I_{IN\_SETx}$ $T_J = -40^\circ\text{C}$	P_6.5.37
Required voltage drop during current control $V_{PSx(CC)} = V_S - V_{OUTx}$	$V_{PSx(CC)}$	0.75	–	–	V	<sup>2)</sup> $V_S = 8\dots 18\text{ V}$ $I_{IN\_SETx} = 133\ \mu\text{A}$ $I_{OUTx} > 90\%$ of $K_{x(typ)} * I_{IN\_SETx}$ $T_J = 25^\circ\text{C}$	P_6.5.38
Required voltage drop during current control $V_{PSx(CC)} = V_S - V_{OUTx}$	$V_{PSx(CC)}$	0.85	–	–	V	<sup>2)</sup> $V_S = 8\dots 18\text{ V}$ $I_{IN\_SETx} = 133\ \mu\text{A}$ $I_{OUTx} > 90\%$ of $K_{x(typ)} * I_{IN\_SETx}$ $T_J = 150^\circ\text{C}$	P_6.5.39
Required supply voltage for current control	$V_{S(CC)}$	5.5	–	–	V	$V_{EN} = 5.5\text{ V}$ $V_{OUTx} = 3\text{ V}$ $R_{IN\_SETx} = 6.8\text{ k}\Omega$ $I_{OUTx} > 90\%$ of $K_x * I_{IN\_SETx}$	P_6.5.40
Required output voltage for current control	$V_{OUTx(CC)}$	1.4	–	–	V	$V_S = 8\dots 18\text{ V}$ $I_{OUTx} > 90\%$ of $K_x * I_{IN\_SETx}$	P_6.5.41
Overtemperature shutdown threshold	$T_{JSD}$	150	175	190	$^\circ\text{C}$	<sup>1)</sup>	P_6.5.42
Overtemperature hysteresis	$T_{J(hys)}$	–	10	–	$^\circ\text{C}$	<sup>1)</sup>	P_6.5.43

1) Not subjected to production test: specified by design

2) In these test conditions, the parameter  $K_{x(typ)}$  represents the typical value of output current accuracy.

Power stages

## 5.4 Electrical characteristics IN\_SETx and PWM pins for output settings

**Table 7 Electrical characteristics: IN\_SETx and PWM pins**

$T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ;  $V_S = 5.5\text{ V}$  to  $18\text{ V}$ ;  $R_{IN\_SETx} = 10\text{ k}\Omega$ ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
IN_SETx reference voltage	$V_{IN\_SETx(\text{ref})}$	1.195	1.22	1.245	V	<sup>1)</sup> $V_{ENx} = 5.5\text{ V}$ $T_J = 25^\circ\text{C}$	P_6.6.1
IN_SETx reference voltage	$V_{IN\_SETx(\text{ref})}$	1.184	1.22	1.256	V	<sup>1)</sup> $V_{ENx} = 5.5\text{ V}$	P_6.6.17
IN_SETx output activation current	$I_{IN\_SETx(\text{ACT})}$	–	–	15	$\mu\text{A}$	$V_{ENx} = 5.5\text{ V}$ $V_{PSx} = 3\text{ V}$ $I_{OUTx} > 50\%$ of $K_x(\text{typ}) * I_{IN\_SETx}$	P_6.6.2

### Timing

IN_SETx turn on time	$t_{ON(IN\_SETx)}$	–	–	20	$\mu\text{s}$	<sup>1)2)</sup> $V_S = 13.5\text{ V}$ $V_{PSx} = 4\text{ V}$ $I_{IN\_SETx}$ rising from 0 to $180\text{ }\mu\text{A}$ $I_{OUTx} = 90\%$ of $K_x * I_{IN\_SETx}$	P_6.6.8
IN_SETx turn off time	$t_{OFF(IN\_SETx)}$	–	–	10	$\mu\text{s}$	<sup>1)2)</sup> $V_S = 13.5\text{ V}$ $V_{PSx} = 4\text{ V}$ $I_{IN\_SETx}$ falling from $180$ to $0\text{ }\mu\text{A}$ $I_{OUTx} = 10\%$ of $K_x * I_{IN\_SETx}$	P_6.6.9

1) Not subjected to production test: specified by design

2) Refer to [Figure 10](#)

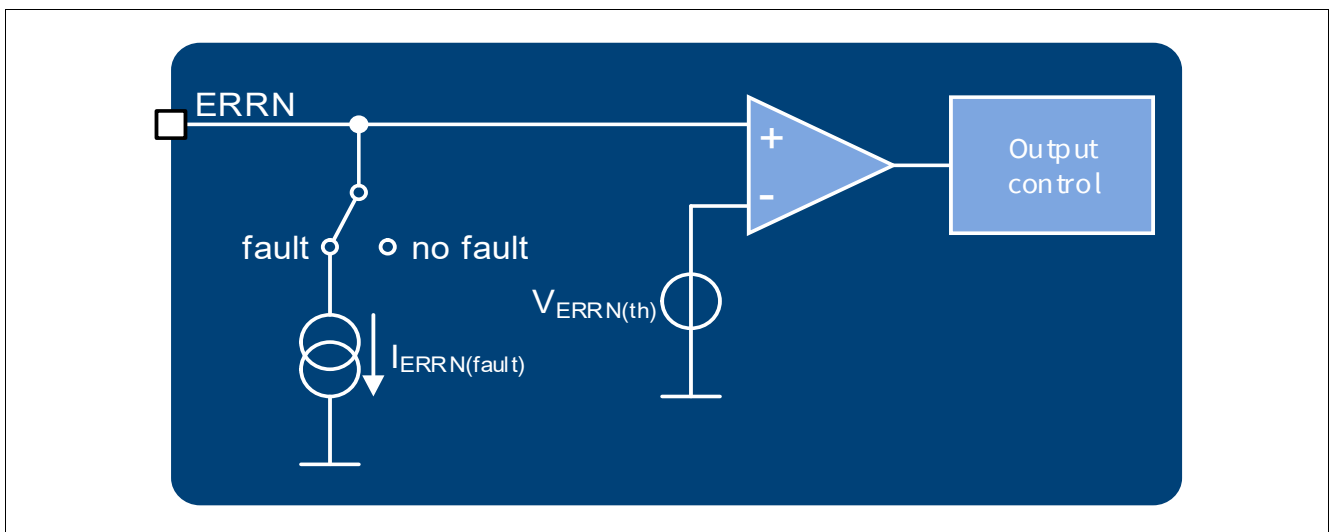
## 6 Load diagnosis

### 6.1 Error management via ERRN and D-pins

Several diagnosis features are integrated in the TLD2252-2EP:

- Open load detection (OL) for any of the output channels OUTx.
- Short circuit OUTx-GND (SC) for any of the output channels OUTx.

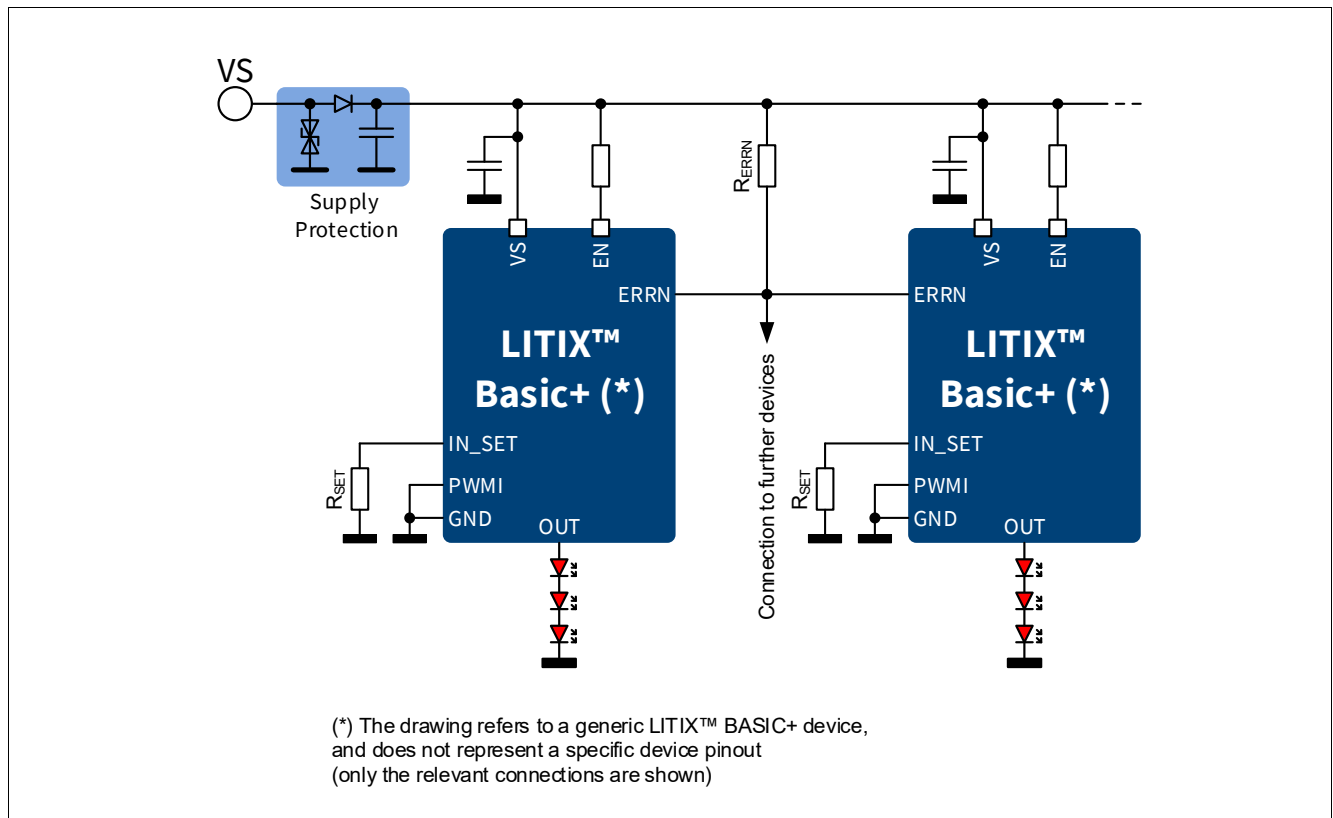
#### 6.1.1 ERRN pin



**Figure 11 ERRN pin (block diagram)**

The device is able to report a detected failure in one of its driven loads and react to a fault detected by another LED driver in the system if a shared error network is implemented (i. e. driving LED chains of the same light function). This is possible with the usage of an external pull-up resistor, allowing multiple devices to share the open drain diagnosis output pin ERRN. All devices sharing the common error network are capable to detect the fault from any of the channels driven by the LITIX™ Basic+ LED drivers and, if desired, to switch multiple loads off.

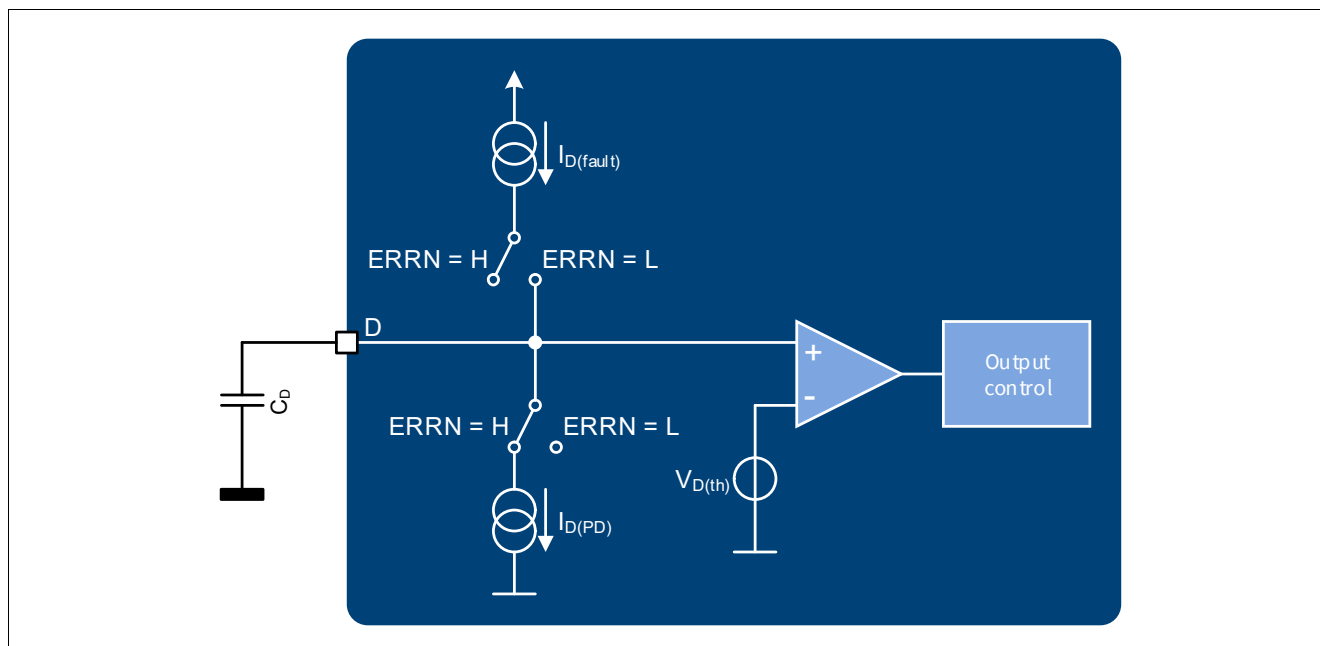
Load diagnosis



**Figure 12 Shared error network principle between LITIX™ Basic+ family devices**

When one of the channels is detected to be under fault conditions (for, at least, a filter time  $t_{\text{fault}}$ ), the open-drain ERRN pin sinks a pull-down current  $I_{\text{ERRN}(\text{fault})}$  toward GND. Therefore an active low state can be detected at ERRN pin when  $V_{\text{ERRN}} < V_{\text{ERRN}(\text{fault})}$  and if this condition is reached, provided the proper setup of the delay pin D, all the channels are switched off. Similarly, when the fault is removed, ERRN pin is put back in high impedance state, and the channels reactivation procedure can be completed once D-pin voltage is below the value  $V_{\text{D}(\text{th})}$ , as illustrated in the timing diagrams in this chapter.

### 6.1.2 D-pin



**Figure 13 D-pin (block diagram).**

The D-pin is designed for 2 main purposes:

- To react to error conditions in LED arrays according to the implemented fault management policy, in systems where multiple LED chains are used for a given light function.
- To extend the channels deactivation delay time of a value  $t_D$ , adding a small signal capacitor from the D-pin to GND. In this way, an unstable or noisy fault condition may be prevented from switching off all the channels of a given light function (i.e. driven by several driver ICs sharing the same error network).

The functionality of the D-pin is shown in the **Figure 13** simplified block diagram:

If one LED within one chain fails in open load condition or one of the device outputs are shorted to GND, the respective LED chain is off. Different automotive applications require a complete deactivation of a light function, if the desired brightness of the function (LED array) can not be achieved due to an internal error condition.

In normal operative status (no fault) a pull-down current  $I_{D(PD)}$  is sunk from the D-pin to GND. If there is a fault condition (for, at least, a filter time  $t_{fault}$ ) in one of the LED channels driven by the IC or in any of the devices sharing the same ERRN error network line, a pull-up current  $I_{D(fault)}$  is instead sourced from the D-pin. As a consequence, if a capacitive or open load is applied at this pin, its voltage starts rising.

When  $V_{D(th)}$  is reached at D-pin, all the channels driven by the device are switched off and if other devices share the same ERRN and D-pins nodes, all the devices turn their outputs off.

Alternatively, if the D-pin is tied to GND, only the channel that has been detected with a fault is safely deactivated.

## Load diagnosis

The capacitor value used at the D-pin,  $C_D$ , sets the delay times  $t_{D(\text{set/reset})}$  according to the following equations:

$$t_{D(\text{set})} = \frac{C_D \cdot V_{D(\text{th})}}{I_{D(\text{fault})}} \quad (6.1)$$

$$t_{D(\text{reset})} = \frac{C_D \cdot (V_{D(\text{CL})} - V_{D(\text{th})})}{I_{D(\text{PD})}} \quad (6.2)$$

### 6.2 Overtemperature (OT), Open Load (OL) and short OUTx to GND (SC)

The behavior of the device during overload conditions that lead to an excess of internal heating up to overtemperature condition, is already described in [Chapter 5](#).

Open load (OL) and OUTx shorted to GND (SC) diagnosis features are also integrated in the TLD2252-2EP.

An open load condition is detected if the voltage drop over one of the output stages  $V_{\text{PSx}}$  is below the threshold  $V_{\text{PSx(OL)}}$  at least for a filter time  $t_{\text{fault}}$ .

A short to GND condition is detected if the voltage of one output stages  $V_{\text{OUTx}}$  is below the threshold  $V_{\text{OUTx(SC)}}$  at least for a filter time  $t_{\text{fault}}$ .

#### 6.2.1 Fault management (D-pin open or connected with a capacitor to GND)

With D-pin open or connected with a capacitor to GND configuration, it is possible to switch off all the channels which share a common error network, without the need of an auxiliary microcontroller. For more details refer also to the timing diagram of [Figure 14](#), [Figure 15](#) and [Figure 16](#).

If there is an OL or SC condition on one of the outputs, a pull-up current  $I_{\text{OUT(fault)}}$  then flows out from the affected channel, replacing the configured output current (but limited by the actual load impedance, e.g. reduced to zero with an ideal open load). Under these conditions, the ERRN pin starts sinking a current  $I_{\text{ERRN(fault)}}$  toward GND and (with proper dimensioning of the external pull-up resistor) reaches a voltage level below  $V_{\text{ERRN(fault)}}$ .

After  $t_{D(\text{set})}$ , the voltage  $V_{D(\text{th})}$  is reached at D-pin, the PWM0 pin is pulled down and the IN\_SETx goes in a weak pull-down state with a current consumption  $I_{\text{IN\_SETx(fault)}}$  after an additional latency time  $t_{\text{IN\_SETx(del)}}$ . The ERRN low voltage can also be used as input signal for a microcontroller to perform the desired diagnosis policy.

The OL and SC error conditions are not latched: as soon as the fault condition is no longer present (at least for a filter time  $t_{\text{fault}}$ ) ERRN goes back to high impedance. When its voltage is above  $V_{\text{ERRN(fault)}}$ , the D-pin voltage starts decreasing and after  $t_{D(\text{reset})}$  goes below  $(V_{D(\text{th})} - V_{D(\text{th,hys})})$ . Then the IN\_SETx voltages go up to  $V_{\text{IN\_SETx(ref)}}$ , again after a time  $t_{\text{IN\_SETx(del)}}$ : at this point, the output stages are activated again. The total time between the fault removal and the IN\_SET reactivation  $t_{\text{ERR(reset)}}$  is extended by an additional latency which depends on the external ERRN pin pull-up and filter circuitry.



Load diagnosis

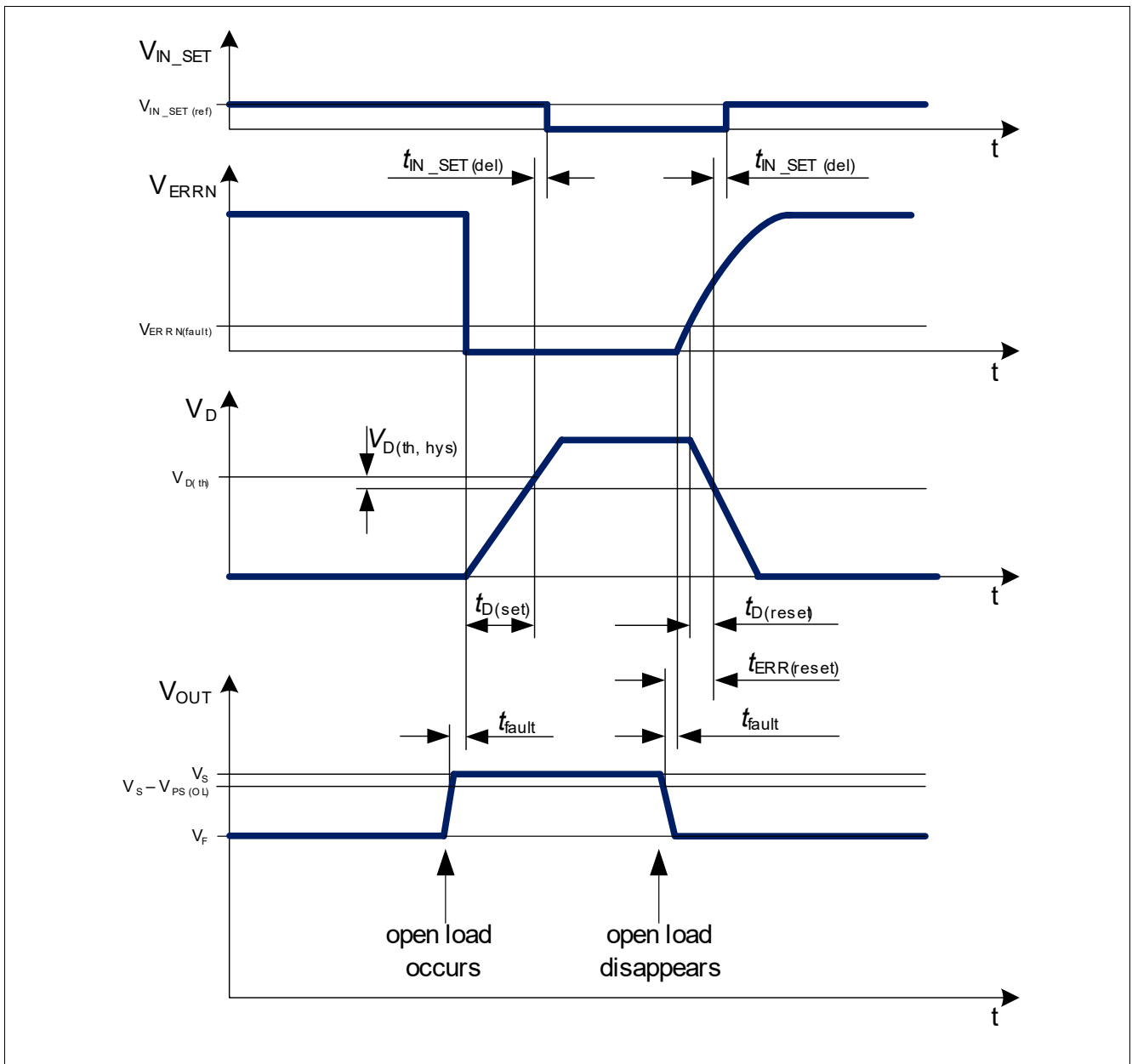
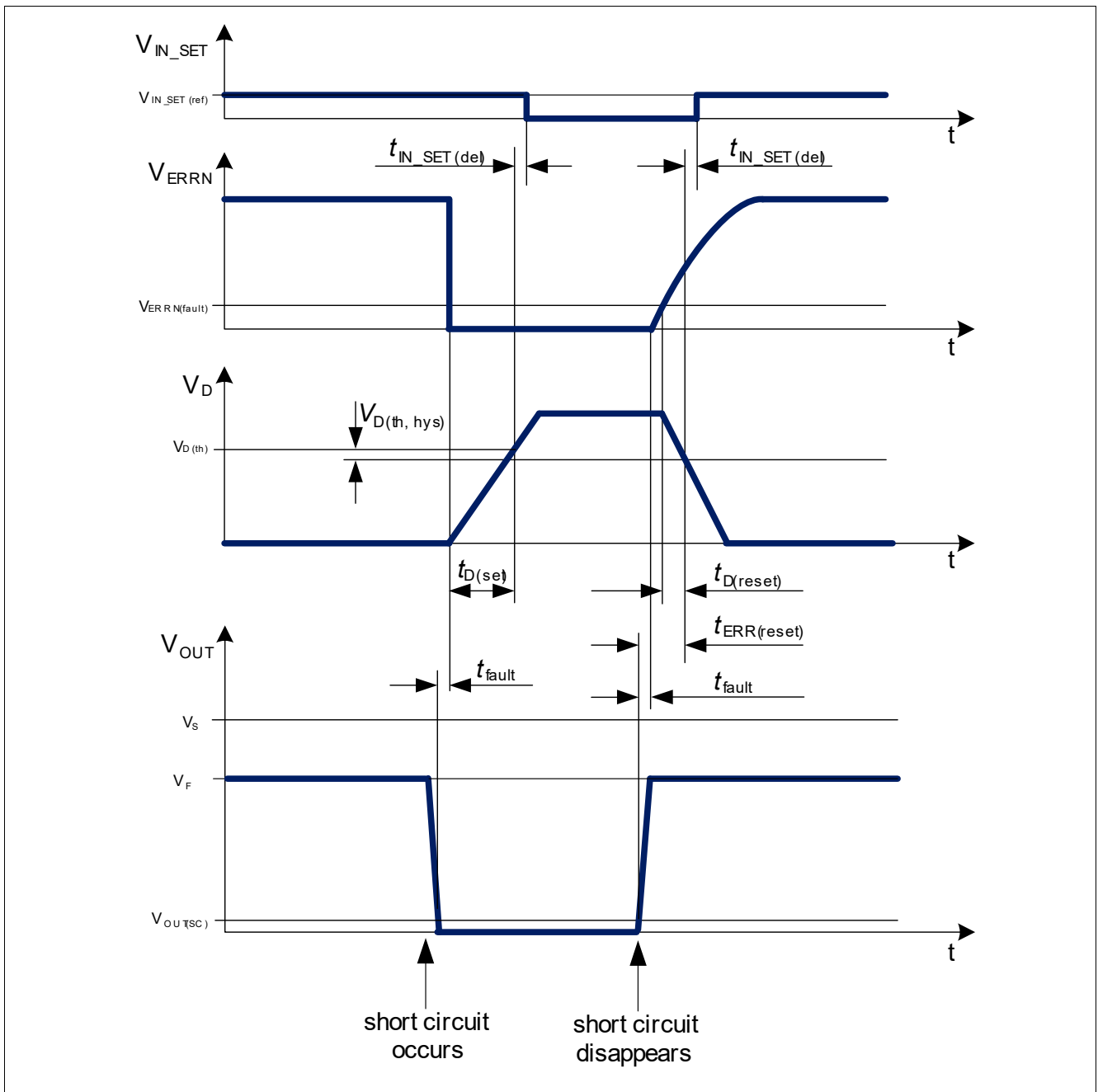


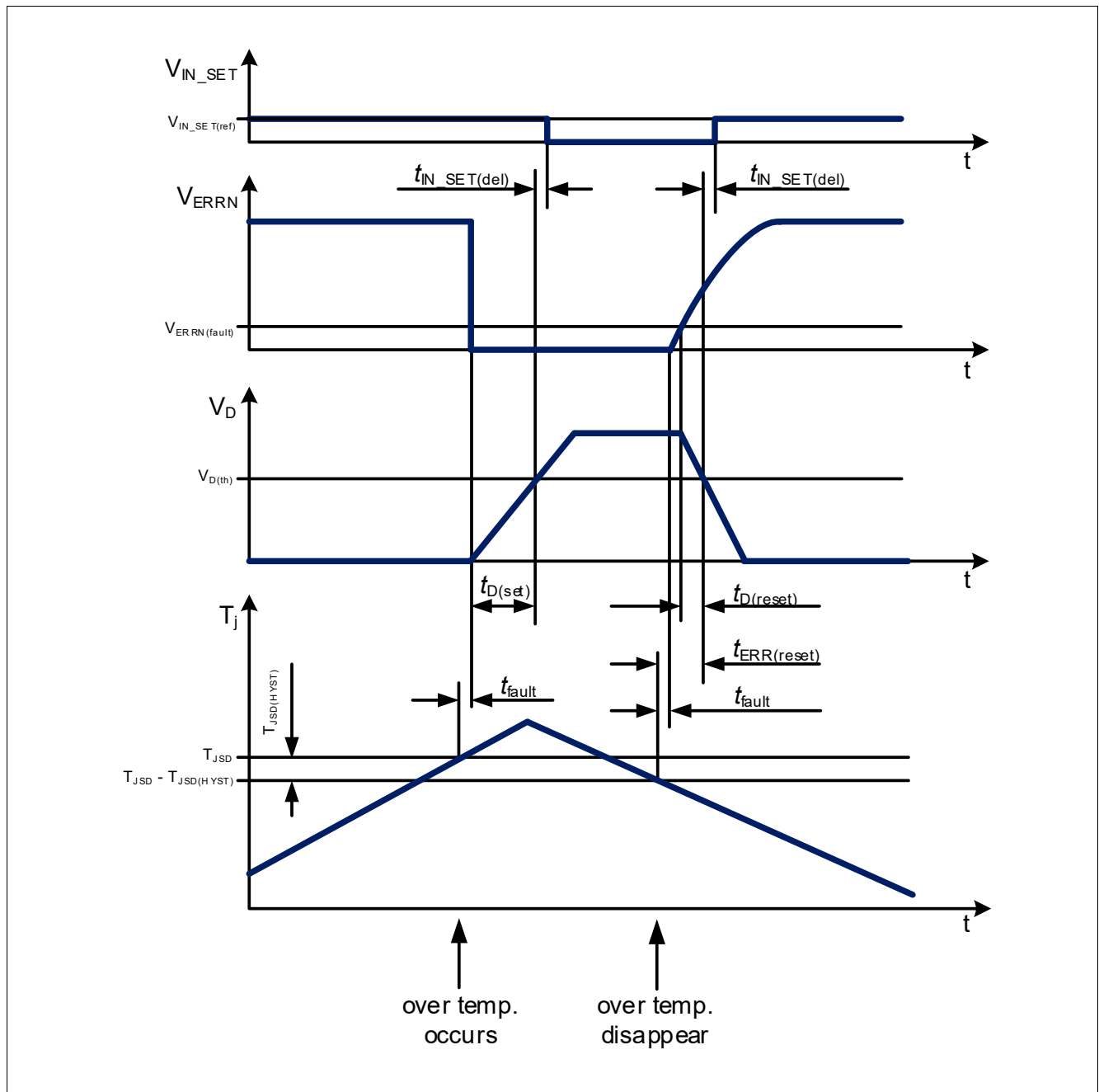
Figure 14 Open load condition timing diagram example (D-pin unconnected or connected to external capacitor to GND,  $V_F$  represents the typical forward voltage of the output load)

Load diagnosis



**Figure 15 Short circuit to GND condition timing diagram example (D-pin not connected or connected to external capacitor to GND, V<sub>Fxyz</sub> represents the forward voltage of the output loads)**

Load diagnosis



**Figure 16** Overtemperature condition timing diagram example (D-pin not connected or connected to external capacitor to GND)

### 6.2.2 Fault management (D-pin connected to GND)

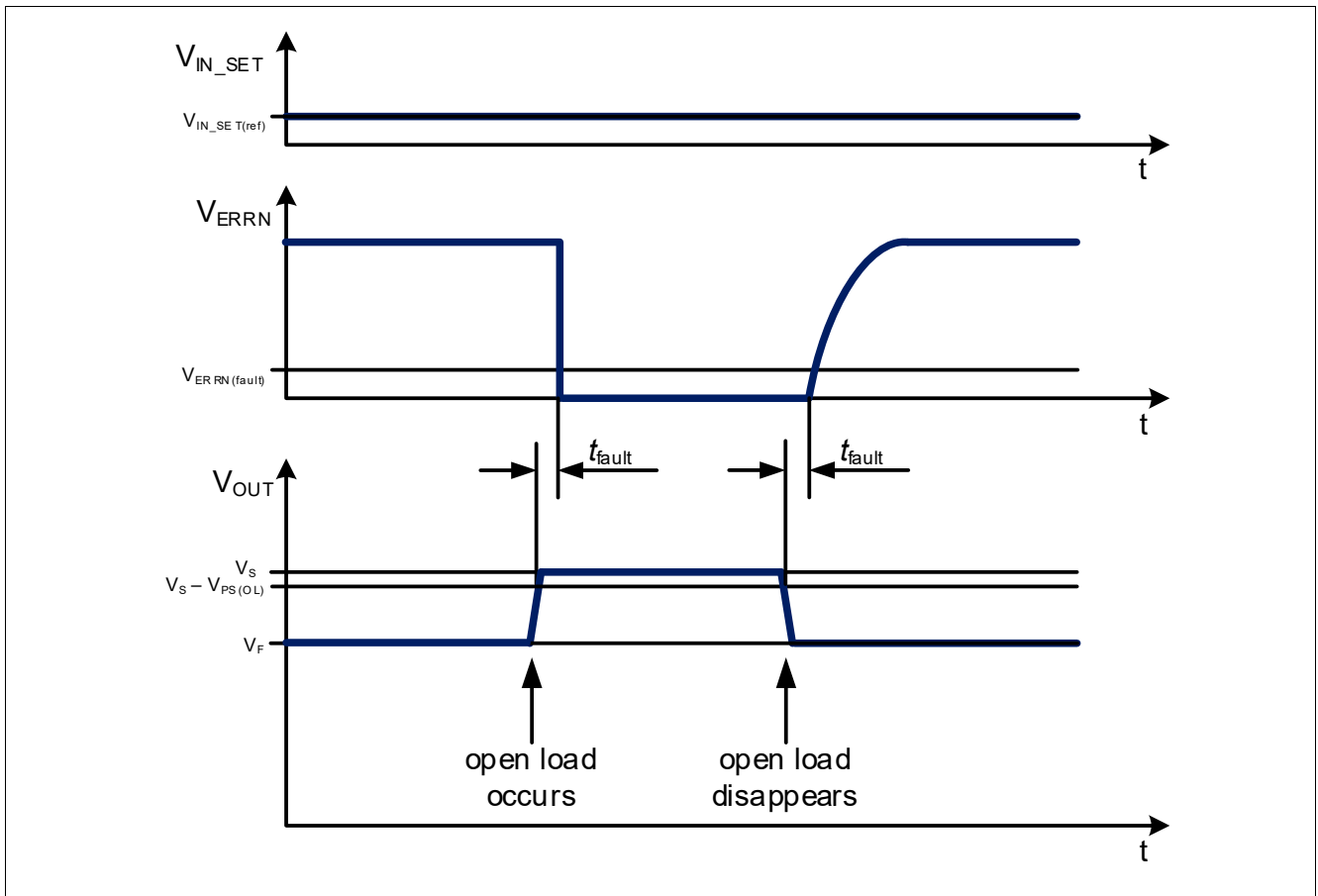
With D-pin connected to GND configuration, it is possible to deactivate only the channel under fault conditions, still sharing ERRN pin in a common error network with other devices of LITIX™ Basic+ family.

If there is fault condition on one of the outputs, a pull-up current  $I_{OUT(fault)}$  flows out from the affected channel, replacing the configured output current (but limited by the actual load impedance, e.g. reduced to zero with an ideal open load). Under fault conditions the ERRN pin starts sinking a current  $I_{ERRN(fault)}$  to ground and the voltage level on this pin will drop below  $V_{ERRN(fault)}$  if the external pull-up resistor is properly dimensioned. The ERRN low voltage can also be used as input signal for a  $\mu C$  to perform the desired diagnosis policy.

Load diagnosis

The fault status is not latched: as soon as the fault condition is no longer present (at least for a filter time  $t_{\text{fault}}$ ), ERRN goes back to high impedance and, once its voltage is above  $V_{\text{ERRN(fault)}}$ , finally the output stages are activated again.

Examples of open load or short to GND diagnosis with D-pin open or connected to GND are shown in the timing diagrams of **Figure 17** and **Figure 18**.



**Figure 17** Open load condition timing diagram example (D-pin connected to GND,  $V_{\text{F}}$  represents the forward voltage of the output load)

Load diagnosis

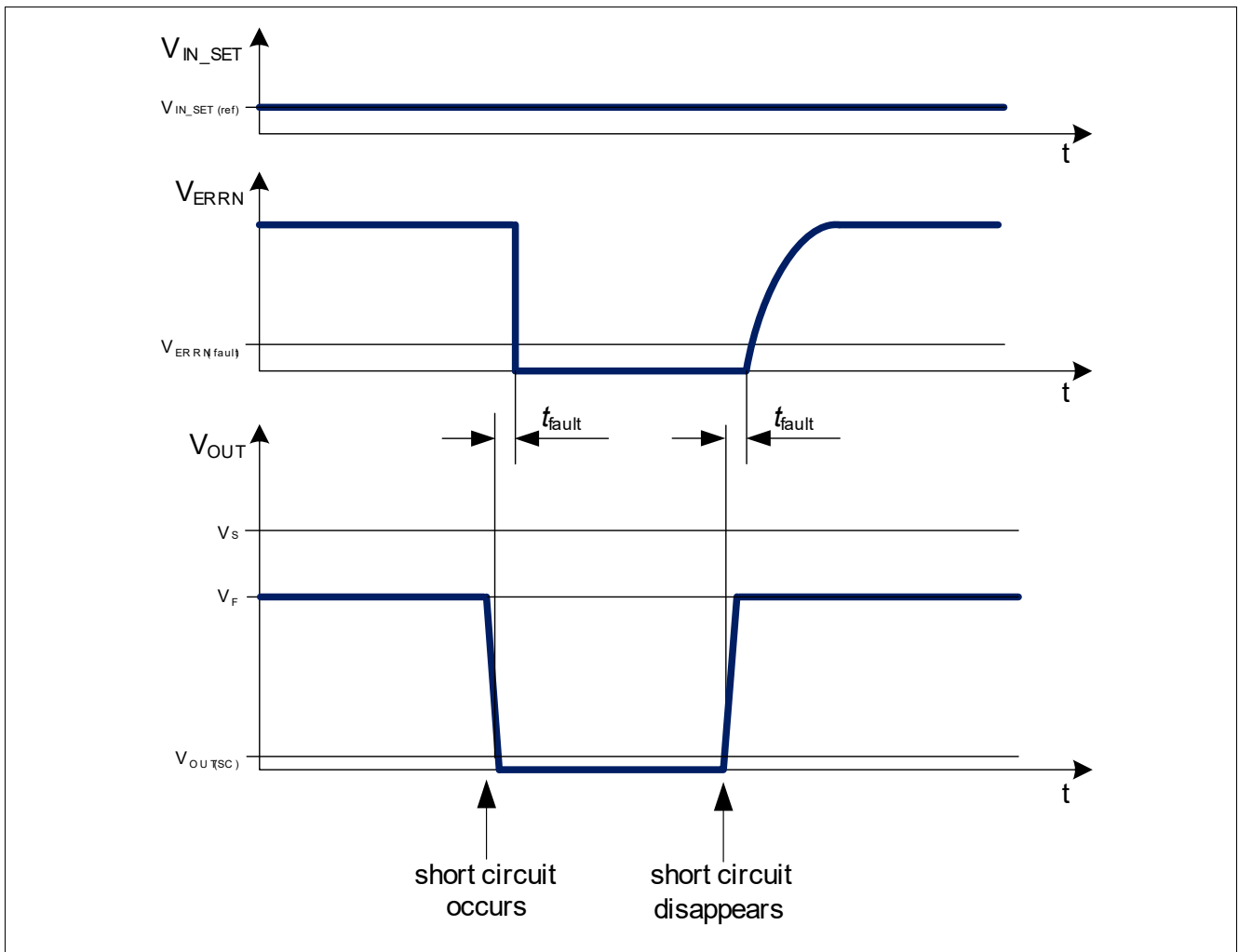


Figure 18 Short circuit condition timing diagram example (D-pin connected to GND,  $V_F$  represents the forward voltage of the output load)

Load diagnosis

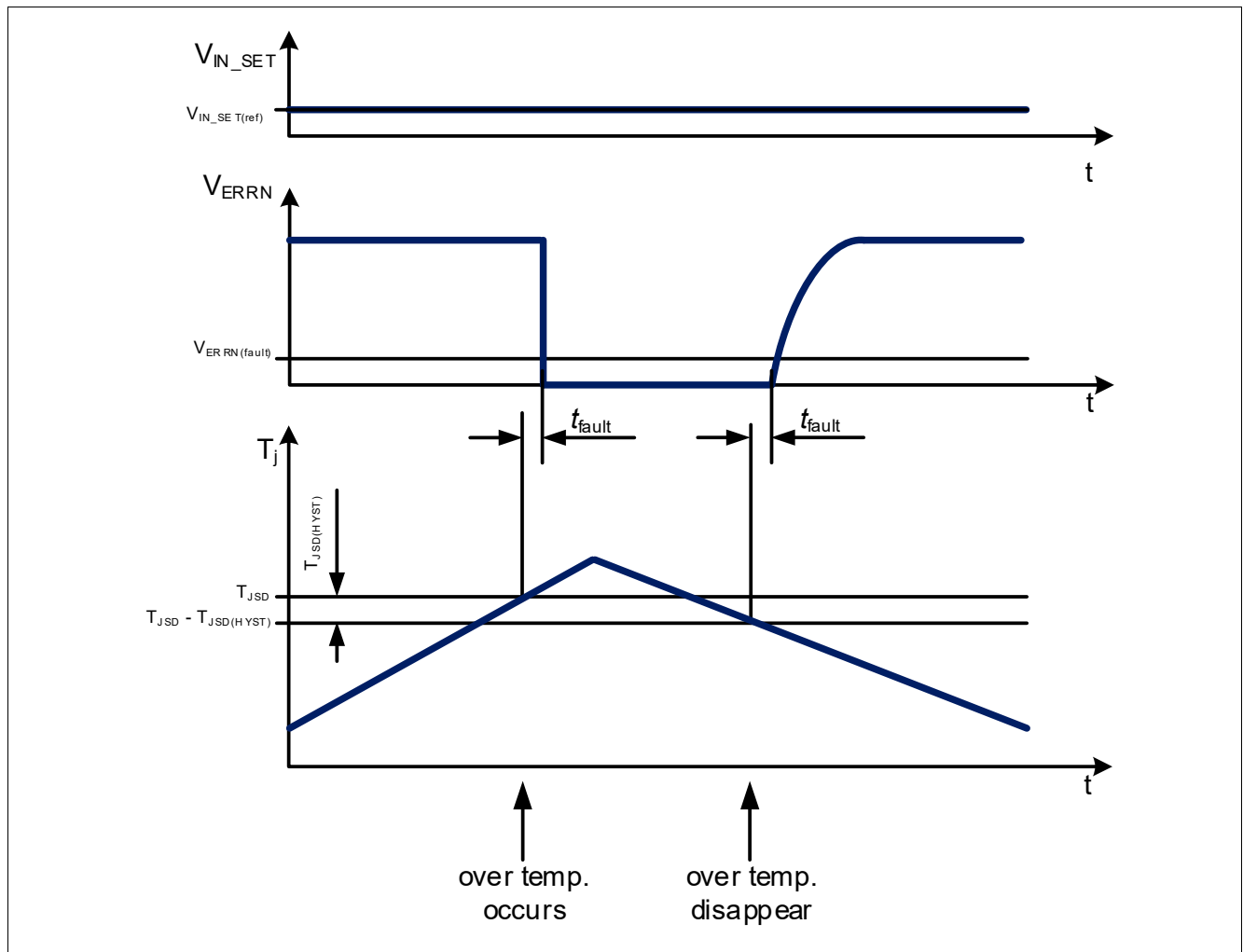


Figure 19 Overtemperature condition timing diagram example (D-pin connected to GND)

### 6.3 Electrical characteristics: Load diagnosis and Overload management

Table 8 Electrical Characteristics: Fault management

$T_J = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ;  $V_S = 5.5\text{ V}$  to  $18\text{ V}$ ;  $R_{IN\_SETx} = 10\text{ k}\Omega$ ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
IN_SET fault current	$I_{IN\_SETx(fault)}$	-	-	10	$\mu\text{A}$	<sup>1)</sup> $V_S > 8\text{ V}$ $V_{OUTx} = 3.6\text{ V}$ $V_{ERRN} = 0\text{ V}$ $V_{IN\_SETx} = 1\text{ V}$ D open $V_{ENx} > V_{DENx(th,max)}$	P_7.5.1
ERRN fault current	$I_{ERRN(fault)}$	2	-	-	mA	<sup>1)</sup> $V_S > 8\text{ V}$ $V_{ERRN} = 0.8\text{ V}$ Fault condition $V_{ENx} > V_{DENx(th,max)}$	P_7.5.2

**Load diagnosis**

**Table 8 Electrical Characteristics: Fault management (cont'd)**

$T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ;  $V_S = 5.5\text{ V}$  to  $18\text{ V}$ ;  $R_{IN\_SETx} = 10\text{ k}\Omega$ ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
ERRN input threshold	$V_{ERRN(th)}$	0.8	–	2.0	V	<sup>1)</sup> $V_S > 8\text{ V}$	P_7.5.3
OL detection threshold	$V_{PSx(OL)}$	0.2	–	0.4	V	$V_S > 8\text{ V}$ $V_{ENx} > V_{DENx(th, max)}$	P_7.5.5
SC detection threshold	$V_{OUTx(SC)}$	0.8	–	1.35	V	$V_S > 8\text{ V}$ $V_{ENx} > V_{DENx(th, max)}$	P_7.5.6
Fault detection current	$I_{OUTx(fault)}$	50	–	180	$\mu\text{A}$	$V_S > 8\text{ V}$ $V_{OUTx} = 0\text{ V}$ $V_{ENx} > V_{DENx(th, max)}$	P_7.5.7

**D-pin**

Threshold voltage for function de-activation	$V_{D(th)}$	1.4	1.7	2	V	$V_S > 8\text{ V}$ $V_{ENx} = 5.5\text{ V}$	P_7.5.8
Threshold hysteresis	$V_{D(hys)}$	–	100	–	mV	<sup>1)</sup> $V_S > 8\text{ V}$ $V_{ENx} = 5.5\text{ V}$ $V_{OUTx} = V_{OUTx(OL)}$	P_7.5.9
Fault pull-up current	$I_{D(fault)}$	20	35	50	$\mu\text{A}$	$V_S > 8\text{ V}$ $V_{OUTx} = V_{OUTx(OL)}$ $V_D = 2\text{ V}$	P_7.5.10
Pull-down current	$I_{D(PD)}$	40	60	95	$\mu\text{A}$	$V_S > 8\text{ V}$ $V_{ENx} = 5.5\text{ V}$ $V_D = 1.4\text{ V}$ $V_{ERRN} = 2\text{ V}$ $V_{PSx} = 3\text{ V}$ No fault conditions	P_7.5.11
Internal clamp voltage	$V_{D(CL)}$	4	–	6	V	$V_S > 8\text{ V}$ $V_{OUTx} = V_{OUTx(OL)}$ D-pin open	P_7.5.12

**Timing**

Fault to ERRN activation delay	$t_{fault}$	40	–	150	$\mu\text{s}$	<sup>1)</sup> $V_S > 8\text{ V}$ $V_{OUTx}$ rising from $5\text{ V}$ to $V_S$ $V_{ENx} > V_{DENx(th, max)}$	P_7.5.19
Fault appearance/removal to IN_SET deactivation/activation delay	$t_{IN\_SET(del)}$	–	–	10	$\mu\text{s}$	<sup>1)</sup> $V_S > 8\text{ V}$ OUTx open D rising from $0\text{ V}$ to $5\text{ V}$ $V_{ENx} > V_{DENx(th, max)}$	P_7.5.20

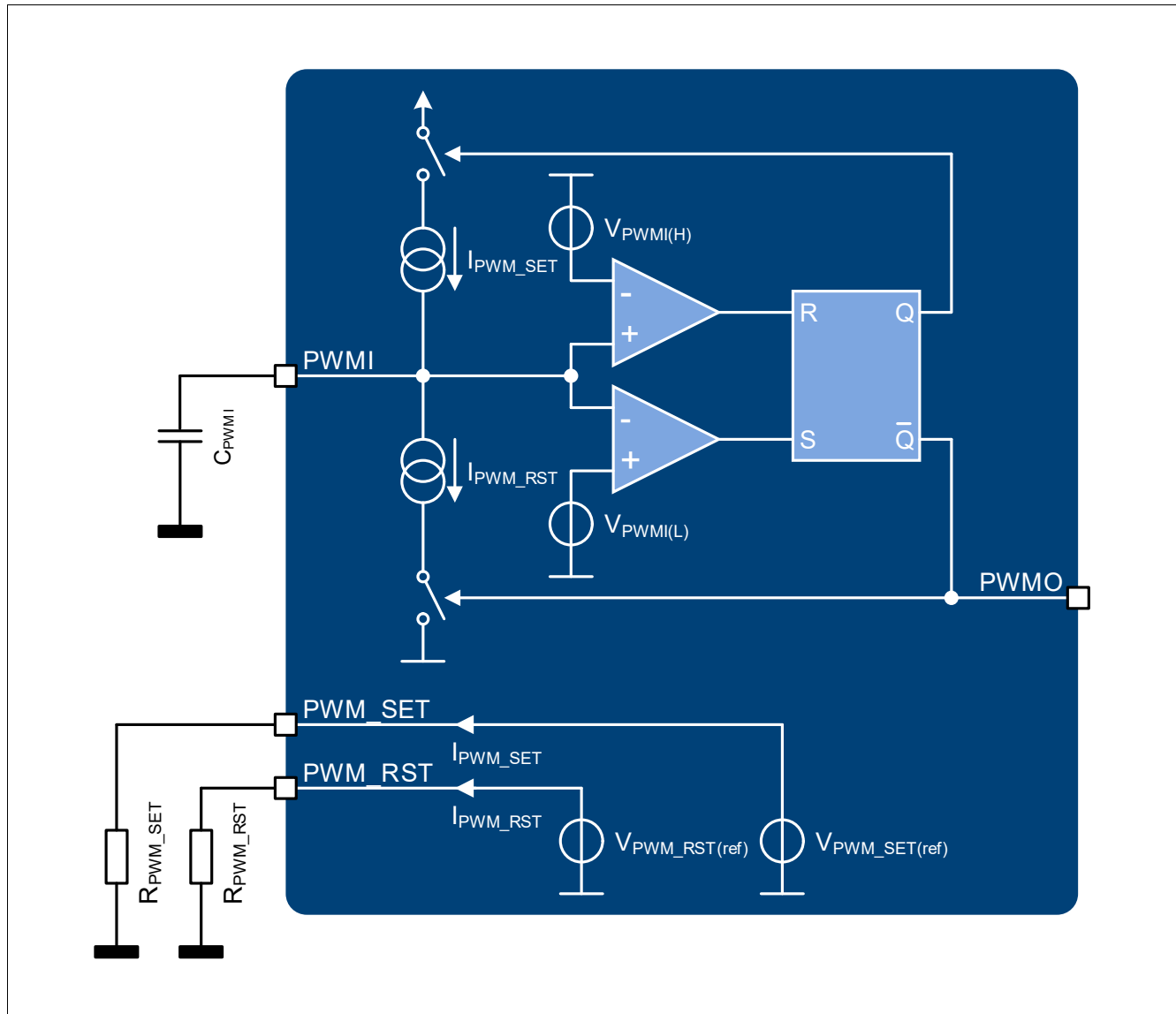
1) Not subjected to production test: specified by design.

PWM control (Digital dimming)

## 7 PWM control (Digital dimming)

Digital dimming via PWM control is commonly practiced to adjust luminous intensity, preventing color shift of the LED light source.

### 7.1 PWM unit



**Figure 20** PWM unit concept diagram (including PWMO drive and typical external circuitry)

The PWM unit can be configured connecting a resistor on each of PWM\_SET and PWM\_RST configuration pins and a capacitor to the PWMI pin. This setup (provided that  $V_{EN} > V_{EN(th)}$  and  $V_S > V_{SUV(ON)}$ ) enables the internal Pulse Width Modulation (PWM) generator to drive the PWMO pin with a digital signal, which represents the desired PWM frequency and Duty Cycle (DC).

With reference to the block diagram of [Figure 20](#) the current flowing through PWM\_SET and PWR\_RST reference pins ( $I_{PWM\_SET}$  and  $I_{PWM\_RST}$ ) are replicated to charge or discharge the capacitor  $C_{PWMI}$

The following figure shows the charging and discharging phases defined by the chosen external components, according to [Figure 21](#) and the internal PWM unit.



PWM control (Digital dimming)

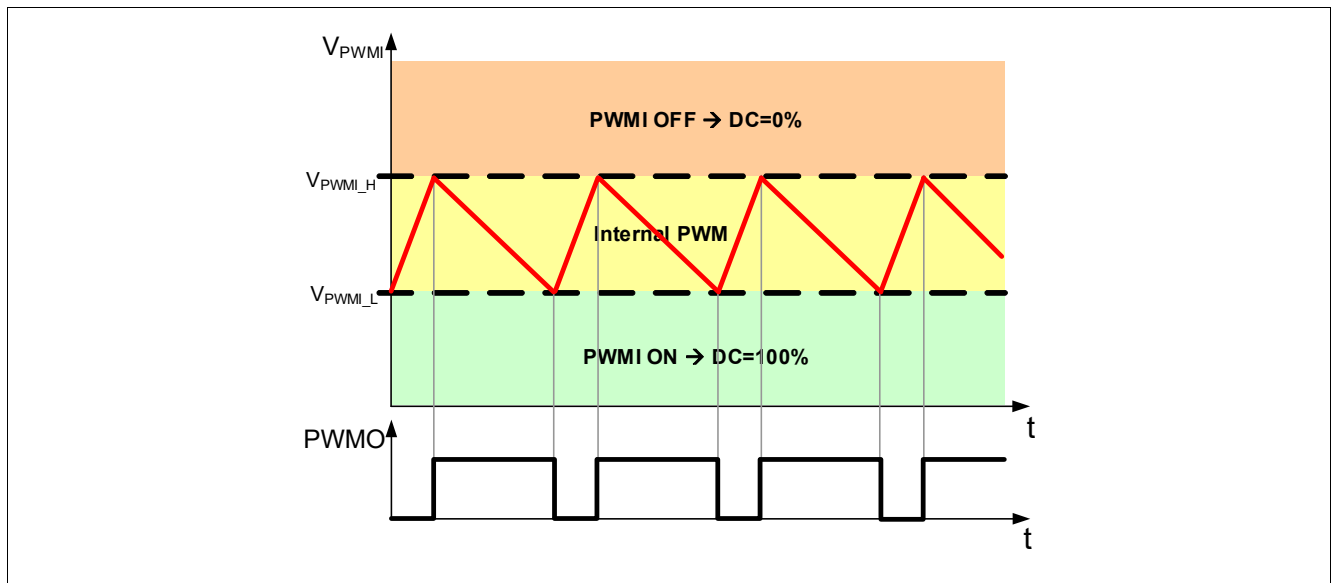


Figure 21 PWMI operating voltages and timing diagram example

The PWM typical characteristics can be adjusted using the formulas below.

$$t_{PWM(ON)} = \frac{C_{PWMI}}{I_{PWM\_SET}} (V_{PWM(H)} - V_{PWM(L)}) = \frac{R_{PWM\_SET} C_{PWMI}}{V_{REF\_SET}} (V_{PWM(H)} - V_{PWM(L)}) \quad (7.1)$$

$$t_{PWM(OFF)} = \frac{C_{PWMI}}{I_{PWM\_RST}} (V_{PWM(H)} - V_{PWM(L)}) = \frac{R_{PWM\_RST} C_{PWMI}}{V_{REF\_RST}} (V_{PWM(H)} - V_{PWM(L)}) \quad (7.2)$$

$$f_{PWM} = \frac{1}{t_{PWM(ON)} + t_{PWM(OFF)}} = \frac{V_{REF\_SET/RST}}{V_{PWM(H)} - V_{PWM(L)}} \cdot \frac{1}{(R_{PWM\_SET} + R_{PWM\_RST}) C_{PWMI}} \quad (7.3)$$

$V_{REF\_SET/RST}$  is equal to 1.22 V. See P\_8.4.12 and P\_8.4.13.

$$DC_{PWMI} = \frac{t_{PWM(ON)}}{t_{PWM(ON)} + t_{PWM(OFF)}} = \frac{R_{PWM\_SET}}{R_{PWM\_SET} + R_{PWM\_RST}} \quad (7.4)$$

From these equations, the proper value  $C_{PWMI}$ ,  $R_{PWM\_SET}$  and  $R_{PWM\_RST}$  can be calculated, according to the electrical characteristics defined in [Table 9](#).

## 7.2 Direct control of PWMI

The PWM engine does not drive directly the internal channels via the PWMO output pin, the PWM control can be used to externally synchronize both output channels as well as other devices of the LITIX™ Basic+ family.

PWMI input can be also controlled by the PWMO output of another device of LITIX™ Basic+ family or, alternatively, a push-pull output stage of a microcontroller: the host device decides the digital dimming characteristics by applying the proper control cycle in order to set the “on”/”off” timing, according to the chosen dimming function.

PWM control (Digital dimming)

### 7.3 Timing diagrams

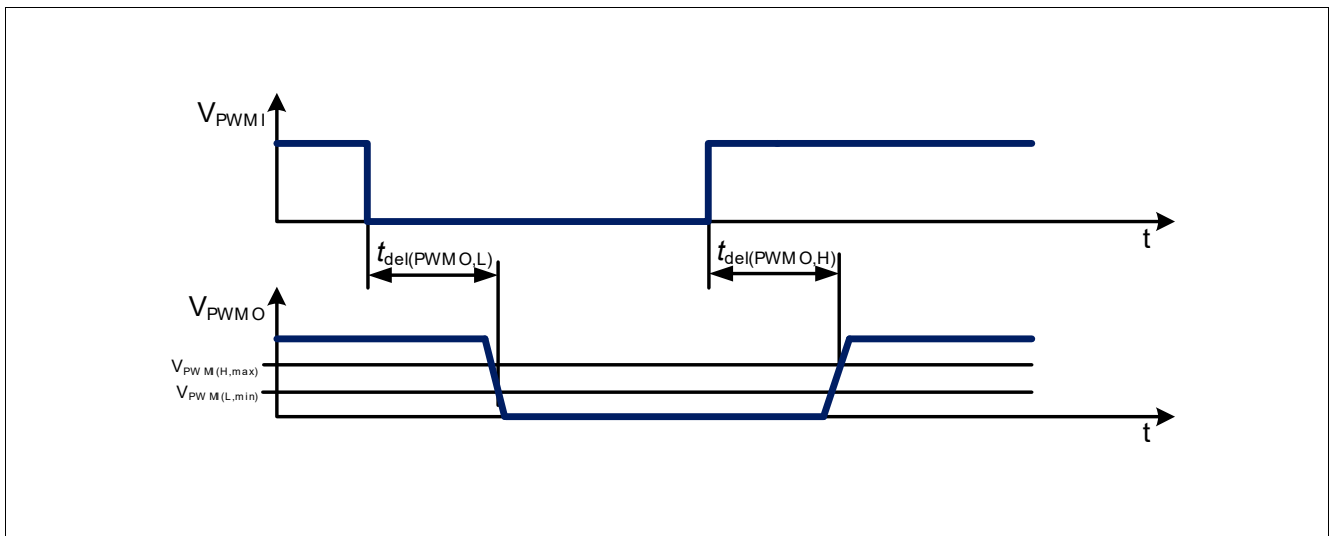


Figure 22 PWMO delay timing diagram

### 7.4 Electrical characteristics PWM engine

Table 9 Electrical characteristics: PWM engine

$T_J = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ;  $V_S = 5.5\text{ V}$  to  $18\text{ V}$ ;  $R_{IN\_SETn} = 10\text{ k}\Omega$ ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
PWMI low threshold	$V_{PWMI(L)}$	1.5	1.7	2	V	$V_S = 8\text{ V}$ to $18\text{ V}$ $V_{ENX} = 5.5\text{ V}$	P_8.4.1
PWMI high threshold	$V_{PWMI(H)}$	2.5	2.7	3	V	$V_S = 8\text{ V}$ to $18\text{ V}$ $V_{ENX} = 5.5\text{ V}$	P_8.4.2
PWMI switching threshold difference $V_{PWMI(H)} - V_{PWMI(L)}$	$\Delta V_{PWMI}$	0.85	1.0	1.15	V	<sup>1)2)</sup> $V_S = 8\text{ V}$ to $18\text{ V}$ $V_{ENX} = 5.5\text{ V}$ $V_{PSX} = 3\text{ V}$	P_8.4.3
PWMO Duty Cycle	$DC_{PWMO}$	9.5	10	10.5	%	<sup>1)2)</sup> $V_S = 8\text{ V}$ to $18\text{ V}$ $I_{PWM\_SET} = 270\text{ }\mu\text{A}$ $I_{PWM\_RST} = 30\text{ }\mu\text{A}$ $C_{PWMI} = 110\text{ nF}$ $C_{PWMO} = 50\text{ pF}$	P_8.4.9
PWMO Duty Cycle	$DC_{PWMO}$	47	50	53	%	<sup>1)2)</sup> $V_S = 8\text{ V}$ to $18\text{ V}$ $I_{PWM\_SET} = 55\text{ }\mu\text{A}$ $I_{PWM\_RST} = 55\text{ }\mu\text{A}$ $C_{PWMI} = 110\text{ nF}$ $C_{PWMO} = 50\text{ pF}$	P_8.4.8

PWM control (Digital dimming)

**Table 9 Electrical characteristics: PWM engine (cont'd)**

$T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ;  $V_S = 5.5\text{ V}$  to  $18\text{ V}$ ;  $R_{IN\_SETn} = 10\text{ k}\Omega$ ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
PWMO Duty Cycle	$DC_{PWMO}$	78	80	82	%	<sup>1)2)</sup> $V_S = 8\text{ V}$ to $18\text{ V}$ $I_{PWM\_SET} = 35\ \mu\text{A}$ $I_{PWM\_RST} = 140\ \mu\text{A}$ $C_{PWMI} = 110\ \text{nF}$ $C_{PWMO} = 50\ \text{pF}$	P_8.4.11
Combined output current accuracy $I_{IN\_SET1} * K_{RT1} * DC_{PWMO}$	$I_{RT1(\text{avg})}$	2.86	3	3.14	mA	<sup>1)</sup> $V_S = 12.8\text{ V}$ $V_{PS} = 2\text{ V}$ $R_{IN\_SET} = 12.2\text{ k}\Omega$ $R_{PWM\_SET} = 4.5\text{ k}\Omega$ $R_{PWM\_RST} = 40.5\text{ k}\Omega$ $C_{PWMI} = 110\ \text{nF}$ $C_{PWMO} = 50\ \text{pF}$ $T_J = 25^\circ\text{C}$	P_8.4.22
Combined output current accuracy $I_{IN\_SET2} * K_{RT2} * DC_{PWMO}$	$I_{RT2(\text{avg})}$	3.81	4	4.19	mA	<sup>1)</sup> $V_S = 12.8\text{ V}$ $V_{PS} = 2\text{ V}$ $R_{IN\_SET} = 18.3\text{ k}\Omega$ $R_{PWM\_SET} = 4.5\text{ k}\Omega$ $R_{PWM\_RST} = 40.5\text{ k}\Omega$ $C_{PWMI} = 110\ \text{nF}$ $C_{PWMO} = 50\ \text{pF}$ $T_J = 25^\circ\text{C}$	P_8.4.24
PWM_SET reference voltage	$V_{PWM\_SET(\text{ref})}$	1.184	1.22	1.256	–	<sup>1)</sup> $V_{ENx} = 5.5\text{ V}$ $V_{PSx} = 3\text{ V}$	P_8.4.12
PWM_RST reference voltage	$V_{PWM\_RST(\text{ref})}$	1.184	1.22	1.256	V	<sup>1)</sup> $V_{ENx} = 5.5\text{ V}$ $V_{PSx} = 3\text{ V}$	P_8.4.13
PWMO OFF pull-up current	$I_{PWMO(\text{OFF})}$	0.75	–	1.6	mA	$V_S = 8\text{ V}$ to $18\text{ V}$ $V_{ENx} = 5.5\text{ V}$ $V_{PWMI} = 3\text{ V}$ $V_{PWMO} = 3\text{ V}$ No fault conditions	P_8.4.14
PWMO ON pull-down current	$I_{PWMO(\text{ON})}$	-1.6	–	-0.75	mA	$V_S = 8\text{ V}$ to $18\text{ V}$ $V_{ENx} = 5.5\text{ V}$ $V_{PWMI} = 1.5\text{ V}$ $V_{PWMO} = 1.5\text{ V}$ No fault conditions	P_8.4.15
PWMO ON pull-down current	$I_{PWMO(\text{ON})}$	-1.6	–	-0.4	mA	<sup>1)</sup> $V_S = 8\text{ V}$ to $18\text{ V}$ $V_{ENx} = 5.5\text{ V}$ $V_{PWMI} = 1.5\text{ V}$ $V_{PWMO} = 1\text{ V}$ No fault conditions	P_8.4.25

PWM control (Digital dimming)

**Table 9 Electrical characteristics: PWM engine** (cont'd)

$T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ;  $V_S = 5.5\text{ V}$  to  $18\text{ V}$ ;  $R_{IN\_SETn} = 10\text{ k}\Omega$ ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>Timing</b>							
PWMO activation delay time	$t_{\text{del(PWMO,L)}}$	–	–	1	$\mu\text{s}$	<sup>1)3)</sup> $V_S = 8\text{ V}$ to $18\text{ V}$ $V_{\text{ENx}} = 5.5\text{ V}$ $C_{\text{PWMO}} = 50\text{ pF}$ $V_{\text{PWMI}}$ falling from $5\text{ V}$ to $0\text{ V}$ $V_{\text{PWMO}} = 1.5\text{ V}$	P_8.4.16
PWMO deactivation delay time	$t_{\text{del(PWMO,H)}}$	–	–	1	$\mu\text{s}$	<sup>1)3)</sup> $V_S = 8\text{ V}$ to $18\text{ V}$ $V_{\text{ENn}} = 5.5\text{ V}$ $C_{\text{PWMO}} = 50\text{ pF}$ $V_{\text{PWMI}}$ rising from $0\text{ V}$ to $5\text{ V}$ $V_{\text{PWMO}} = 3\text{ V}$	P_8.4.17
PWMO delay time matching $t_{\text{del(PWMO,H)}} - t_{\text{del(PWMO,L)}}$	$\Delta t_{\text{del(PWMO)}}$	-200	–	200	ns	<sup>1)3)</sup> $V_S = 12.8\text{ V}$ $T_J = 25^\circ\text{C}$	P_8.4.21

1) Not subjected to production test. specified by design

2) Measured at PWMO output waveform ( $V_{\text{PWMO}}$  crossing  $3\text{ V}$  when rising from  $V_{\text{PWMO(L)}}$ ,  $2\text{ V}$  when falling from  $V_{\text{PWMO(H)}}$ )

3) Refer to [Figure 22](#).

Application information

## 8 Application information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

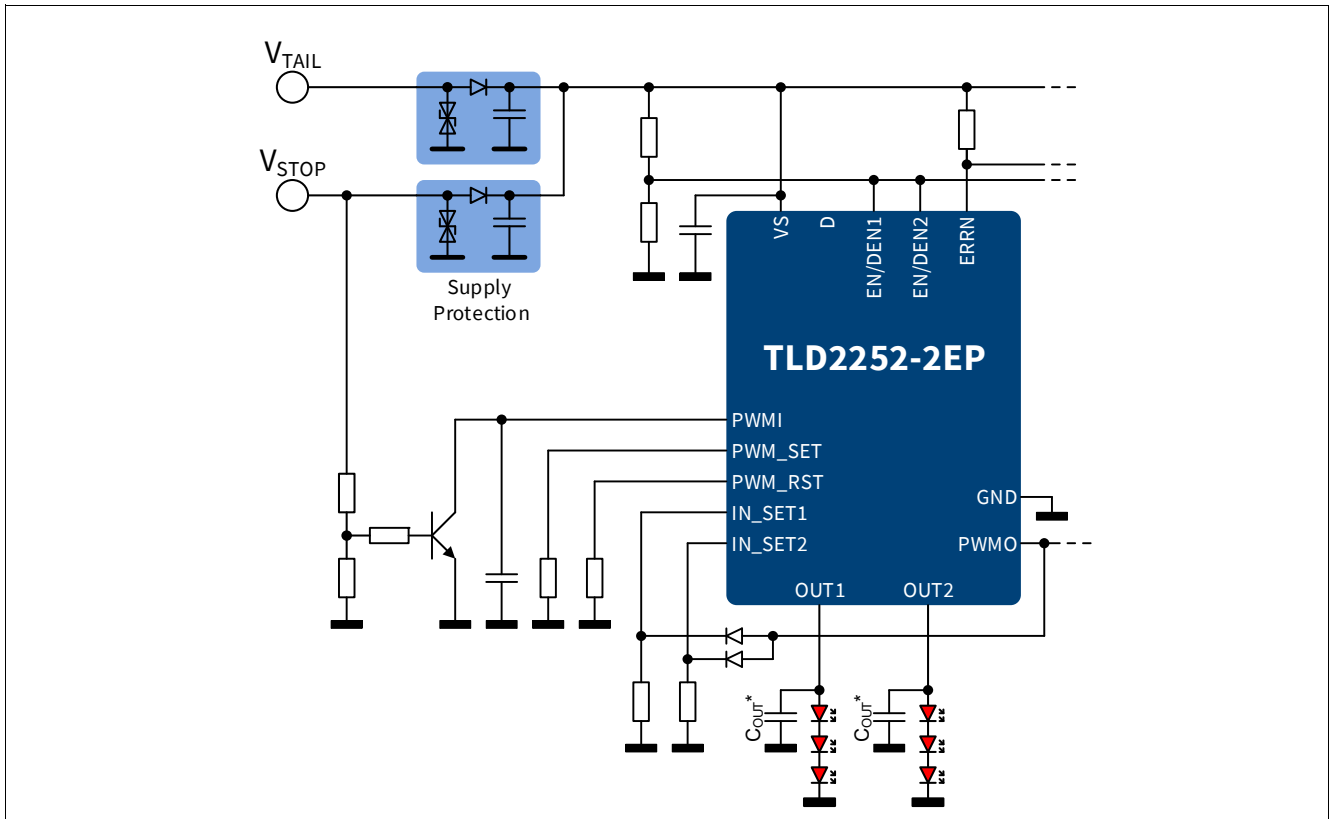


Figure 23 Application diagram example

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

Package outline

9 Package outline

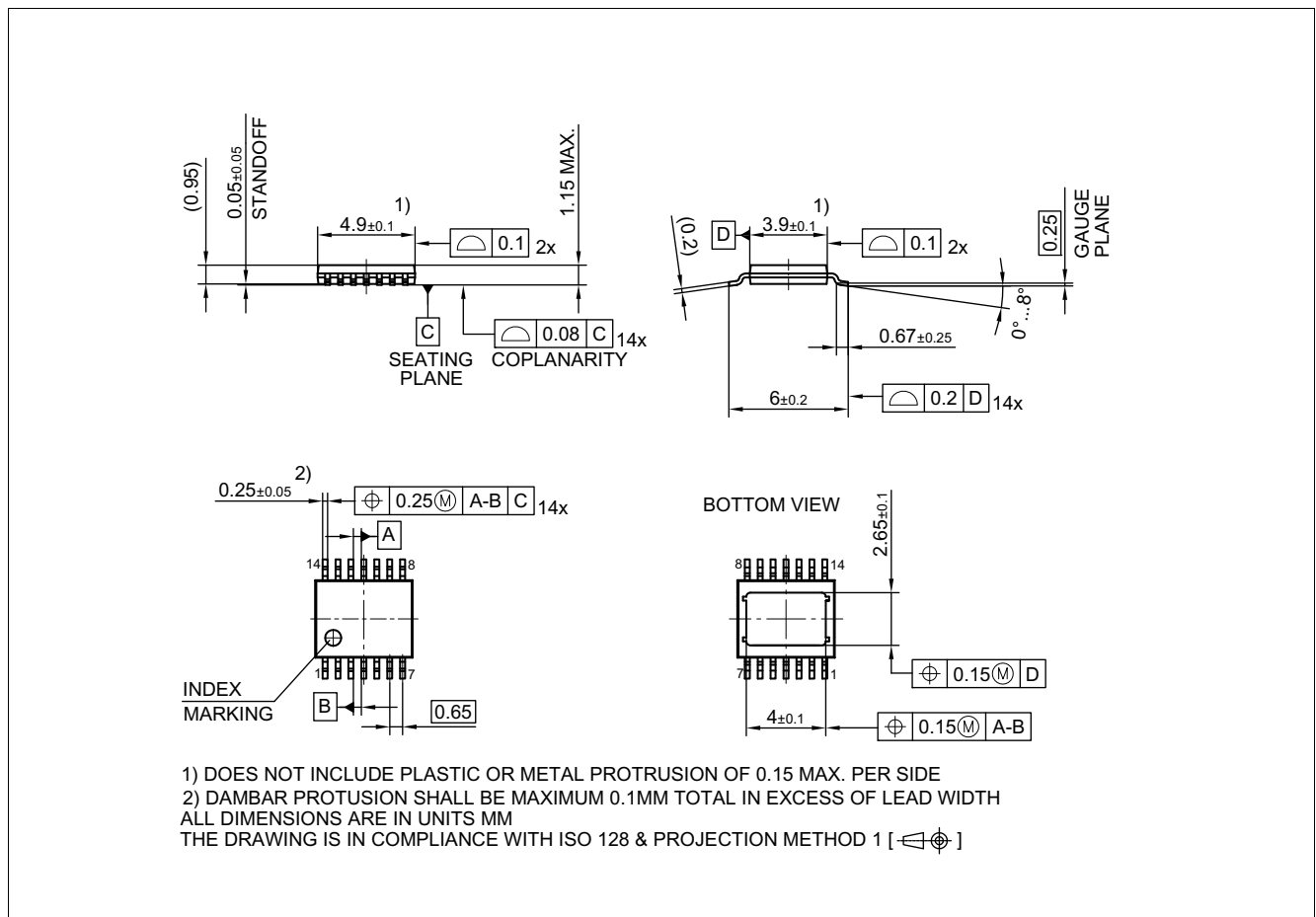


Figure 24 PG-TSDSO-14

Green product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

<https://www.infineon.com/packages>

---

**Revision History**

## **10 Revision History**

<b>Revision</b>	<b>Date</b>	<b>Changes</b>
1.10	2021-06-15	Updated P_5.2.17, P_5.2.14, P_5.2.15
1.00	2019-09-26	Initial datasheet created

## Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

**Edition 2021-06-15**

**Published by**

**Infineon Technologies AG**

**81726 Munich, Germany**

**© 2021 Infineon Technologies AG.**

**All Rights Reserved.**

**Do you have a question about any aspect of this document?**

**Email: [erratum@infineon.com](mailto:erratum@infineon.com)**

**Document reference**

**LITIX™ Basic+ TLD2252-2EP**

## IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffheitsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office ([www.infineon.com](http://www.infineon.com)).

## WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.