NTHD5904N

Power MOSFET

20 V, 4.5 A, Dual N−Channel, ChipFET™

Features

- Low $R_{DS(on)}$ and Fast Switching Speed
- Leadless ChipFET Package has 40% Smaller Footprint than TSOP−6. Ideal Device for Applications Where Board Space is at a Premium.
- ChipFET Package Exhibits Excellent Thermal Capabilities. Ideal for Applications Where Heat Transfer is Required.
- Pb−Free Packages are Available

Applications

- DC−DC Buck or Boost Converters
- Low Side Switching
- Optimized for Battery and Low Side Switching Applications in Computing and Portable Equipment

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	20	V
Gate−to−Source Voltage			V_{GS}	±8.0	V
Continuous Drain Current (Note 1)	Steady State	T_A=25°C	I_D	3.3	A
		T_A=85°C		2.4	
	t ≤ 5 s	T_A=25°C		4.5	
Power Dissipation (Note 1)	Steady State	T_A=25°C	P_D	1.13	W
Continuous Drain Current (Note 2)	Steady State	T_A=25°C	I_D	2.5	A
		T_A=85°C		1.8	
Power Dissipation (Note 2)		T_A=25°C	P_D	0.64	W
Pulsed Drain Current	t_p=10 μs		I_{DM}	10	A
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to 150	°C
Source Current (Body Diode)			I_S	2.6	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction−to−Ambient – Steady State (Note 1)	$R_{\theta JA}$	110	°C/W
Junction−to−Ambient – t ≤ 5 s (Note 1)	$R_{\theta JA}$	60	
Junction−to−Ambient – Steady State (Note 2)	$R_{\theta JA}$	195	

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
2. Surface Mounted on FR4 Board using the minimum recommended pad size (Cu area = 0.214 in sq).
3. ESD Rating Information: Human Body Model (HBM) Class 0.

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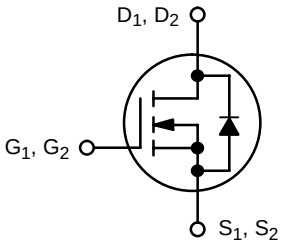
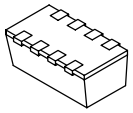
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
20 V	40 mΩ @ 4.5 V	4.5 A
	55 mΩ @ 2.5 V	

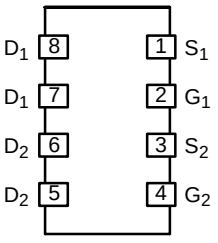
N−Channel MOSFET



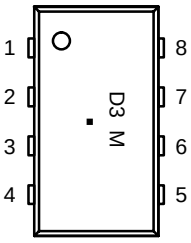


ChipFET
CASE 1206A
STYLE 2

PIN CONNECTIONS



MARKING DIAGRAM



(Top View)

D3 = Specific Device Code
M = Month Code
▪ = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V	20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 16 V			1.0	μA
		V_{GS} = 0 V, V_{DS} = 16 V, T_J = 125°C			10	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±8.0 V			±100	nA
ON CHARACTERISTICS (Note 4)						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA	0.6	0.75	1.2	V
Drain−to−Source On−Resistance	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 3.3 A		40	65	mΩ
		V_{GS} = 2.5 V, I_D = 2.3 A		55	105	
Forward Transconductance	g_{FS}	V_{DS} = 10 V, I_D = 3.3 A		6.0		S
CHARGES AND CAPACITANCES						
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 16 V		465		pF
Output Capacitance	C_{oss}			65		
Reverse Transfer Capacitance	C_{rss}			30		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 2.5 V, V_{DS} = 16 V, I_D = 3.3 A		4.0		nC
Threshold Gate Charge	$Q_{G(TH)}$			0.4		
Gate−to−Source Charge	Q_{GS}			0.8		
Gate−to−Drain Charge	Q_{GD}			2.0		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 10 V, I_D = 3.3 A		6.0		nC
Threshold Gate Charge	$Q_{G(TH)}$			0.5		
Gate−to−Source Charge	Q_{GS}			0.8		
Gate−to−Drain Charge	Q_{GD}			1.7		
SWITCHING CHARACTERISTICS (Note 5)						
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = 4.5 V, V_{DS} = 16 V, I_D = 3.3 A, R_G = 2.5 Ω		6.0		ns
Rise Time	t_r			17		
Turn−Off Delay Time	$t_{d(off)}$			17		
Fall Time	t_f			5.1		
DRAIN−SOURCE DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 2.6 A		0.8	1.15	V
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, I_S = 2.6 A, dI_S/dt = 100 A/μs		19.5		ns
Charge Time	t_a			6.0		
Discharge Time	t_b			13		
Reverse Recovery Charge	Q_{RR}			7.0		nC

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

ORDERING INFORMATION

Device	Package	Shipping†
NTHD5904NT1	ChipFET	3000 / Tape & Reel
NTHD5904NT1G	ChipFET (Pb−Free)	3000 / Tape & Reel
NTHD5904NT3	ChipFET	10,000 / Tape & Reel
NTHD5904NT3G	ChipFET (Pb−Free)	10,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

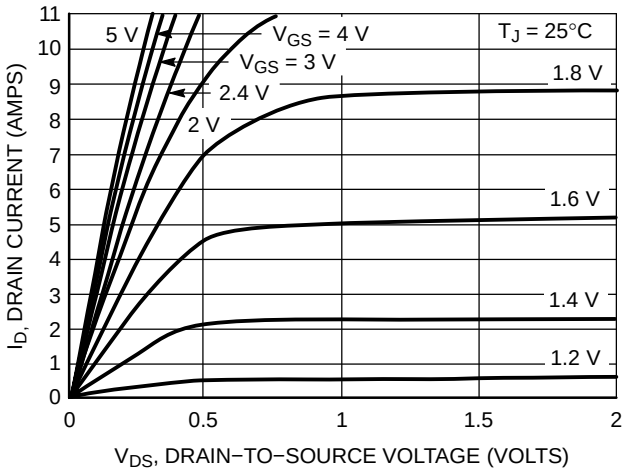


Figure 1. On−Region Characteristics

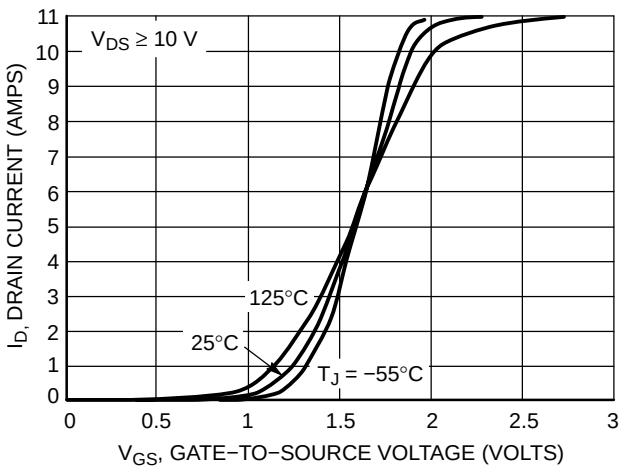


Figure 2. Transfer Characteristics

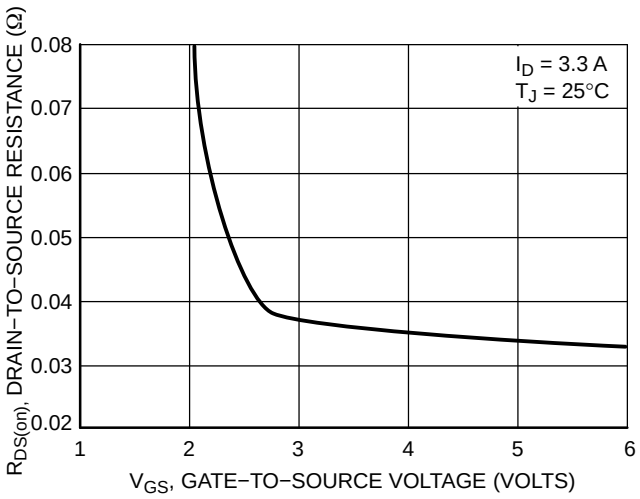


Figure 3. On−Resistance vs. Gate−to−Source Voltage

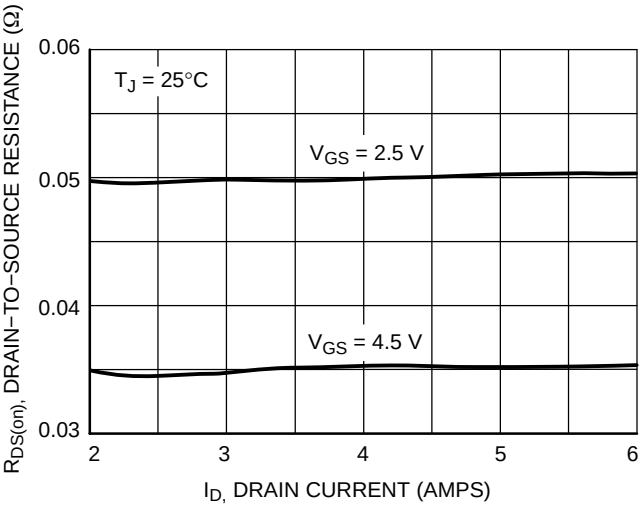


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

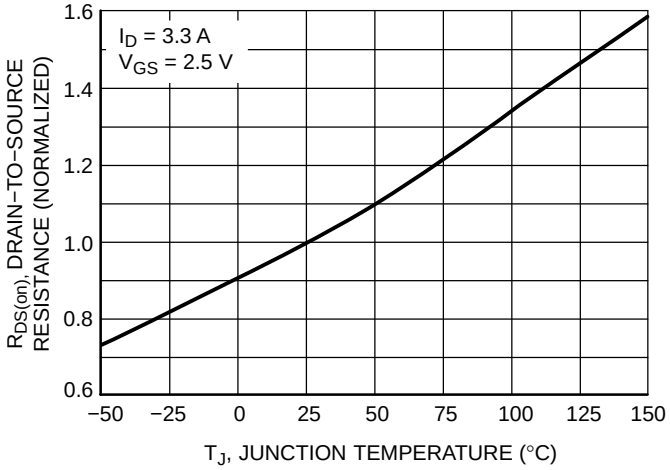


Figure 5. On−Resistance Variation with Temperature

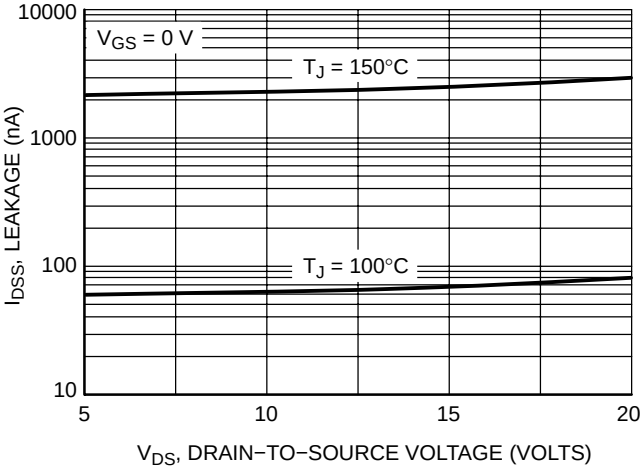


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

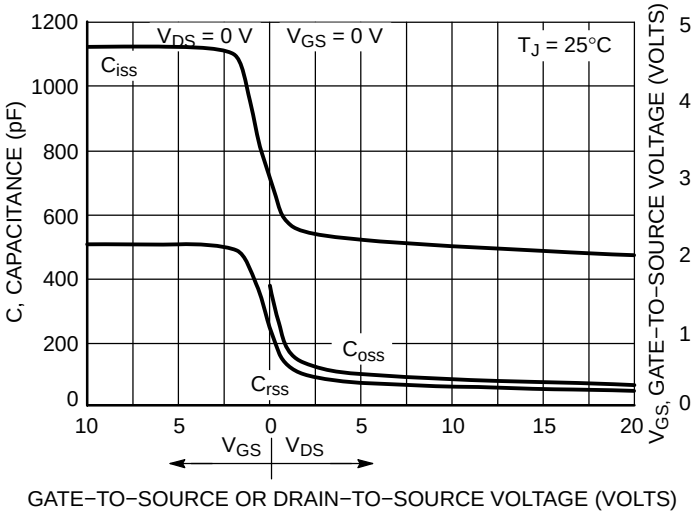


Figure 7. Capacitance Variation

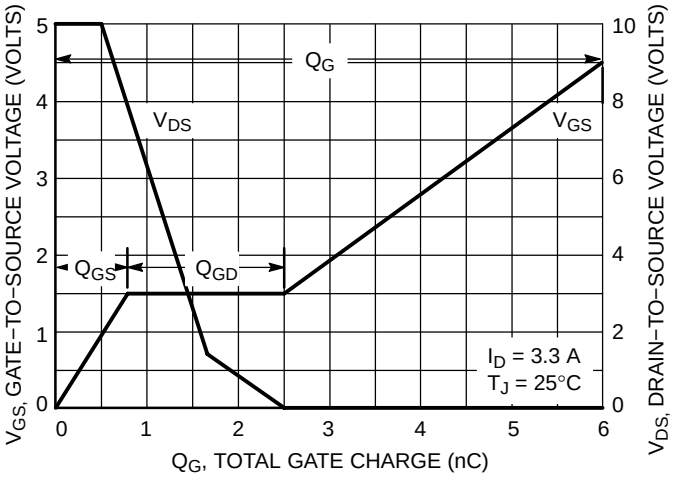


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

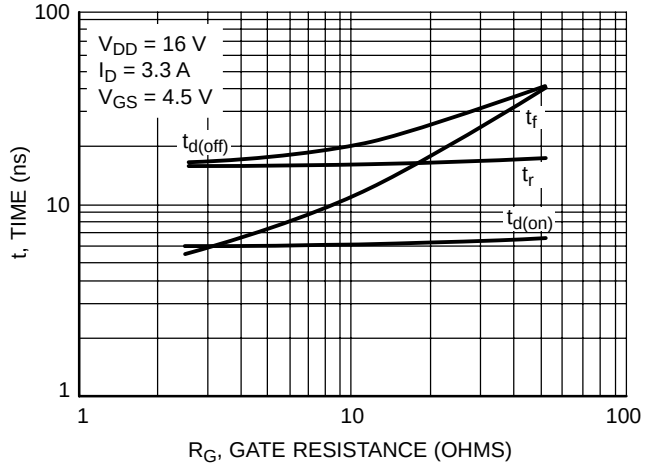


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

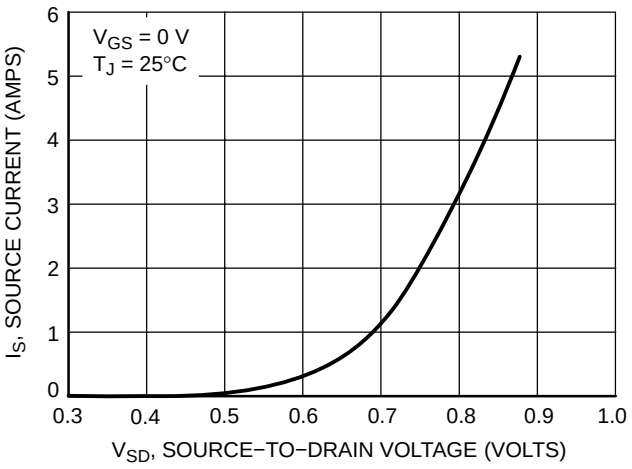


Figure 10. Diode Forward Voltage vs. Current

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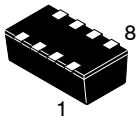
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

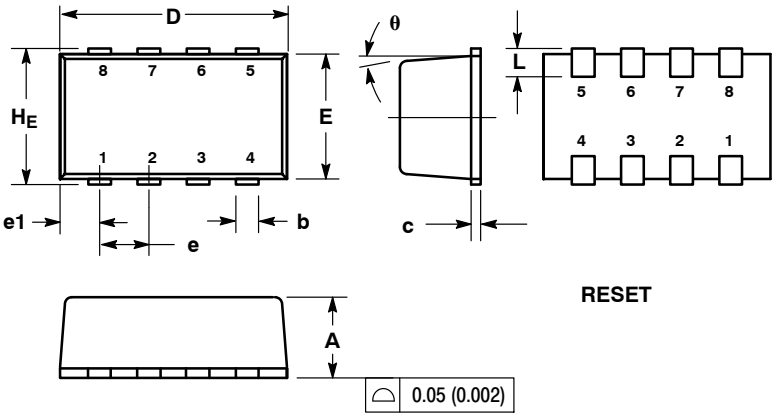
ON Semiconductor®

ChipFET™
CASE1206A−03
ISSUE K

DATE 19 MAY 2009



SCALE 1:1



RESET

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.05	1.10	0.039	0.041	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.55	1.65	1.70	0.061	0.065	0.067
e	0.65 BSC			0.025 BSC		
e1	0.55 BSC			0.022 BSC		
L	0.28	0.35	0.42	0.011	0.014	0.017
H_E	1.80	1.90	2.00	0.071	0.075	0.079
θ	5° NOM			5° NOM		

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. GATE
5. SOURCE
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

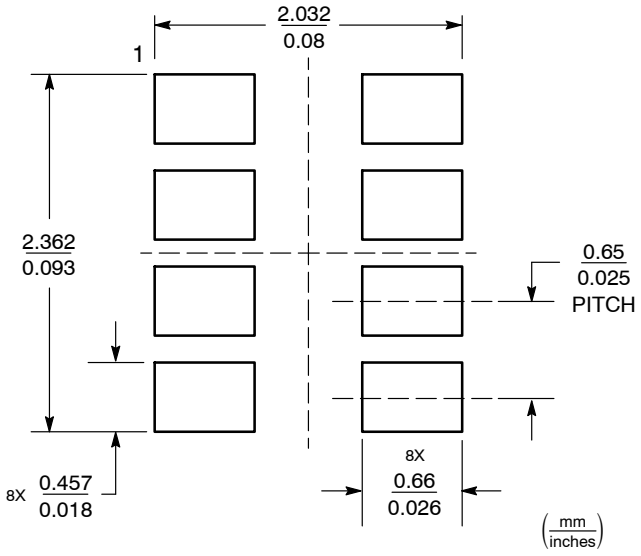
STYLE 3:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. COLLECTOR
4. BASE
5. EMITTER
6. COLLECTOR
7. COLLECTOR
8. COLLECTOR

STYLE 5:
PIN 1. ANODE
2. ANODE
3. DRAIN
4. DRAIN
5. SOURCE
6. GATE
7. CATHODE
8. CATHODE

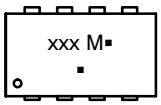
STYLE 6:
PIN 1. ANODE
2. DRAIN
3. DRAIN
4. GATE
5. SOURCE
6. DRAIN
7. DRAIN
8. CATHODE / DRAIN

SOLDERING FOOTPRINT



Basic Style

GENERIC MARKING DIAGRAM*



xxx = Specific Device Code
M = Month Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

OPTIONAL SOLDERING FOOTPRINTS ON PAGE 2

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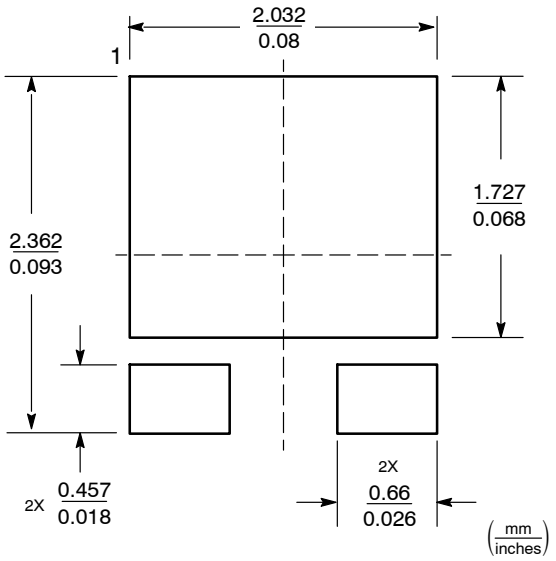
DESCRIPTION:	**ChipFET**	**PAGE 1 OF 2**

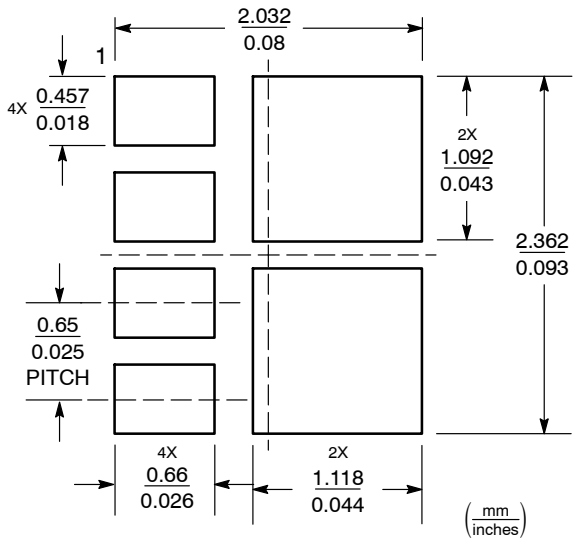
ChipFET™
CASE 1206A−03
ISSUE K

DATE 19 MAY 2009

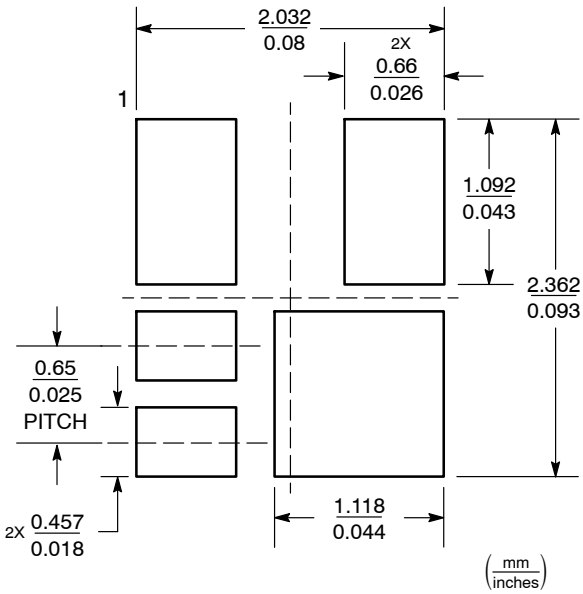
ADDITIONAL SOLDERING FOOTPRINTS*



Styles 1 and 4



Style 2



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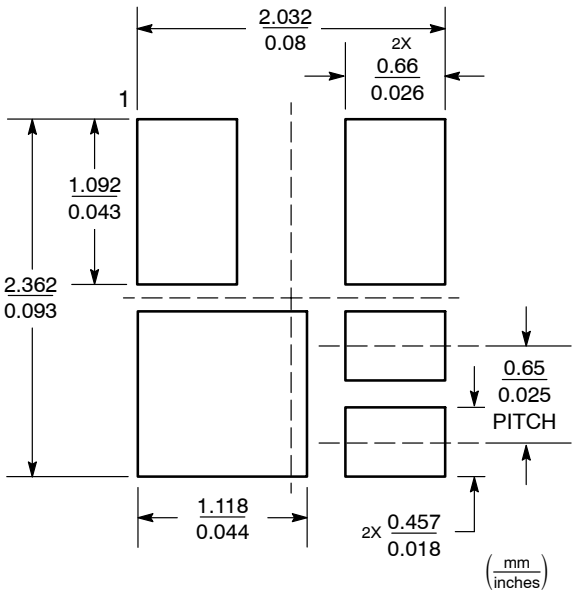

Style 5

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**ChipFET**	**PAGE 2 OF 2**

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