The following document contains information on Cypress products. The document has the series name, product name, and ordering part numbering with the prefix “MB”. However, Cypress will offer these products to new and existing customers with the series name, product name, and ordering part number with the prefix “CY”.

How to Check the Ordering Part Number

1. Go to www.cypress.com/pcn.
2. Enter the keyword (for example, ordering part number) in the **SEARCH PCNS** field and click **Apply**.
3. Click the corresponding title from the search results.
4. Download the Affected Parts List file, which has details of all changes

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PRELIMINARY

MB95F856K, MB95F866K, MB95F876K

New 8FX MB95850K/860K/870K Series Datasheet

Description

The MB95850K/860K/870K Series is a series of general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers of these series contain a variety of peripheral functions.

Features

■ F^{2}MC-8FX CPU core

Instruction set optimized for controllers

- ❒ Multiplication and division instructions
- ❒ 16-bit arithmetic operations
- ❒ Bit test branch instructions
- ❒ Bit manipulation instructions, etc.

■ Clock

- ❒ Selectable main clock source
  - Main oscillation clock (up to 16.25 MHz, maximum machine clock frequency: 8.125 MHz)
  - External clock (up to 32.5 MHz, maximum machine clock frequency: 16.25 MHz)
  - Main CR clock (4 MHz ±2%)
  - Main CR PLL clock

    The main CR PLL clock frequency becomes 8 MHz ±2% when the PLL multiplication rate is 2.

    The main CR PLL clock frequency becomes 10 MHz ±2% when the PLL multiplication rate is 2.5.

    The main CR PLL clock frequency becomes 12 MHz ±2% when the PLL multiplication rate is 3.

    The main CR PLL clock frequency becomes 16 MHz ±2% when the PLL multiplication rate is 4.
- ❒ Selectable subclock source
  - Suboscillation clock (32.768 kHz)
  - External clock (32.768 kHz)
  - Sub-CR clock (Typ: 100 kHz, Min: 50 kHz, Max: 150 kHz)

■ Timer

- ❒ 8/16-bit composite timer
  - MB95F856K: 1 channel
  - MB95F866K/F876K: 2 channels
- ❒ 8/16-bit PPG
  - MB95F856K: 1 channel
  - MB95F866K: 2 channels
  - MB95F876K: 3 channels
- ❒ Time-base timer × 1 channel
- ❒ Watch counter × 1 channel
- ❒ Watch prescaler × 1 channel

■ UART/SIO × 1 channel

- ❒ Full duplex double buffer
- ❒ Capable of clock asynchronous (UART) serial data transfer and clock synchronous (SIO) serial data transfer

■ I^{2}C bus interface × 1 channel

- ❒ Built-in wake-up function

■ External interrupt

- ❒ MB95F856K: 6 channels
- ❒ MB95F866K: 8 channels
- ❒ MB95F876K: 10 channels
- ❒ Interrupt by edge detection (rising edge, falling edge, and both edges can be selected)
- ❒ Can be used to wake up the device from different low power consumption (standby) modes

■ 8/10-bit A/D converter

- ❒ MB95F856K: 4 channels
- ❒ MB95F866K: 6 channels
- ❒ MB95F876K: 8 channels
- ❒ 8-bit or 10-bit resolution can be selected.

■ Low power consumption (standby) modes

There are four standby modes as follows:

- ❒ Stop mode
- ❒ Sleep mode
- ❒ Watch mode
- ❒ Time-base timer mode

In standby mode, two further options can be selected: normal standby mode and deep standby mode.

■ I/O port

- ❒ MB95F856K (number of I/O ports: 21)
  - General-purpose I/O ports (CMOS I/O): 17
  - General-purpose I/O ports (N-ch open drain): 4
- ❒ MB95F866K (number of I/O ports: 29)
  - General-purpose I/O ports (CMOS I/O): 25
  - General-purpose I/O ports (N-ch open drain): 4
- ❒ MB95F876K (number of I/O ports: 45)
  - General-purpose I/O ports (CMOS I/O): 41
  - General-purpose I/O ports (N-ch open drain): 4

■ On-chip debug

- ❒ 1-wire serial control
- ❒ Serial writing supported (asynchronous mode)

■ Hardware/software watchdog timer

- ❒ Built-in hardware watchdog timer
- ❒ Built-in software watchdog timer

■ Power-on reset

- ❒ A power-on reset is generated when the power is switched on.

■ Low-voltage detection (LVD) reset circuit

- Built-in low-voltage detection function (The combination of detection voltage and release voltage can be selected from four options.)

■ Comparator × 1 channel
- Built-in dedicated BGR
- The comparator reference voltage can be selected between the BGR voltage and the comparator pin.

■ Clock supervisor counter
- Built-in clock supervisor counter

■ Dual operation Flash memory
- The program/erase operation and the read operation can be executed in different banks (upper bank/lower bank) simultaneously.

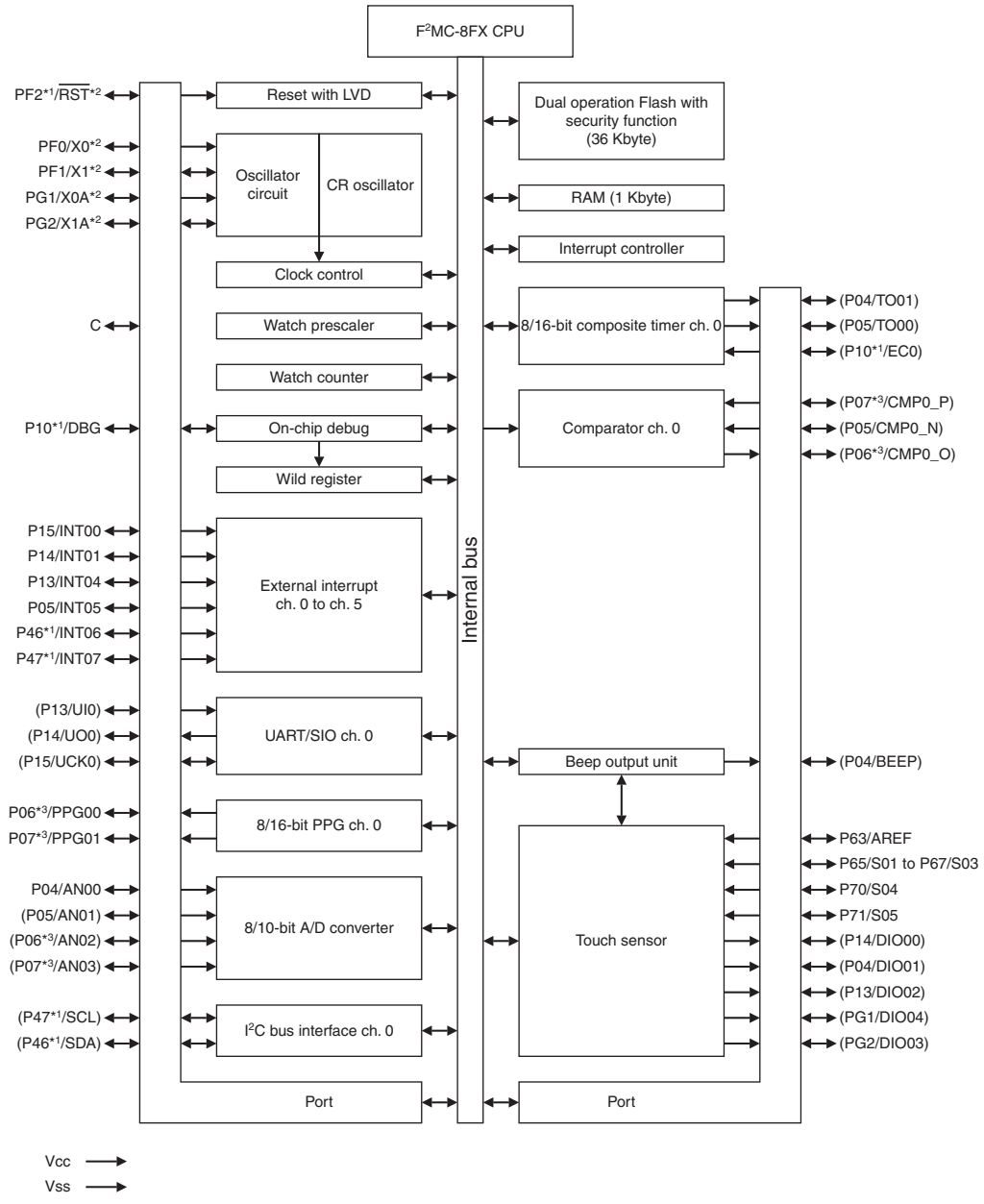
■ Flash memory security function
- Protects the content of the Flash memory.

■ Touch sensor (TS)
- Adjacent Pattern Interference Suppression (APIS™)
- Three modes in APIS: APIS mode 1, APIS mode 2 and APIS mode 3
- Configurable Automatic Impedance Calibration (AIC™)
- Direct output (DIO) function

Note: APIS and AIC are registered trademarks of ATLab, Inc., South Korea.

■ Beep output unit × 1 channel

Block Diagram (MB95850K Series)



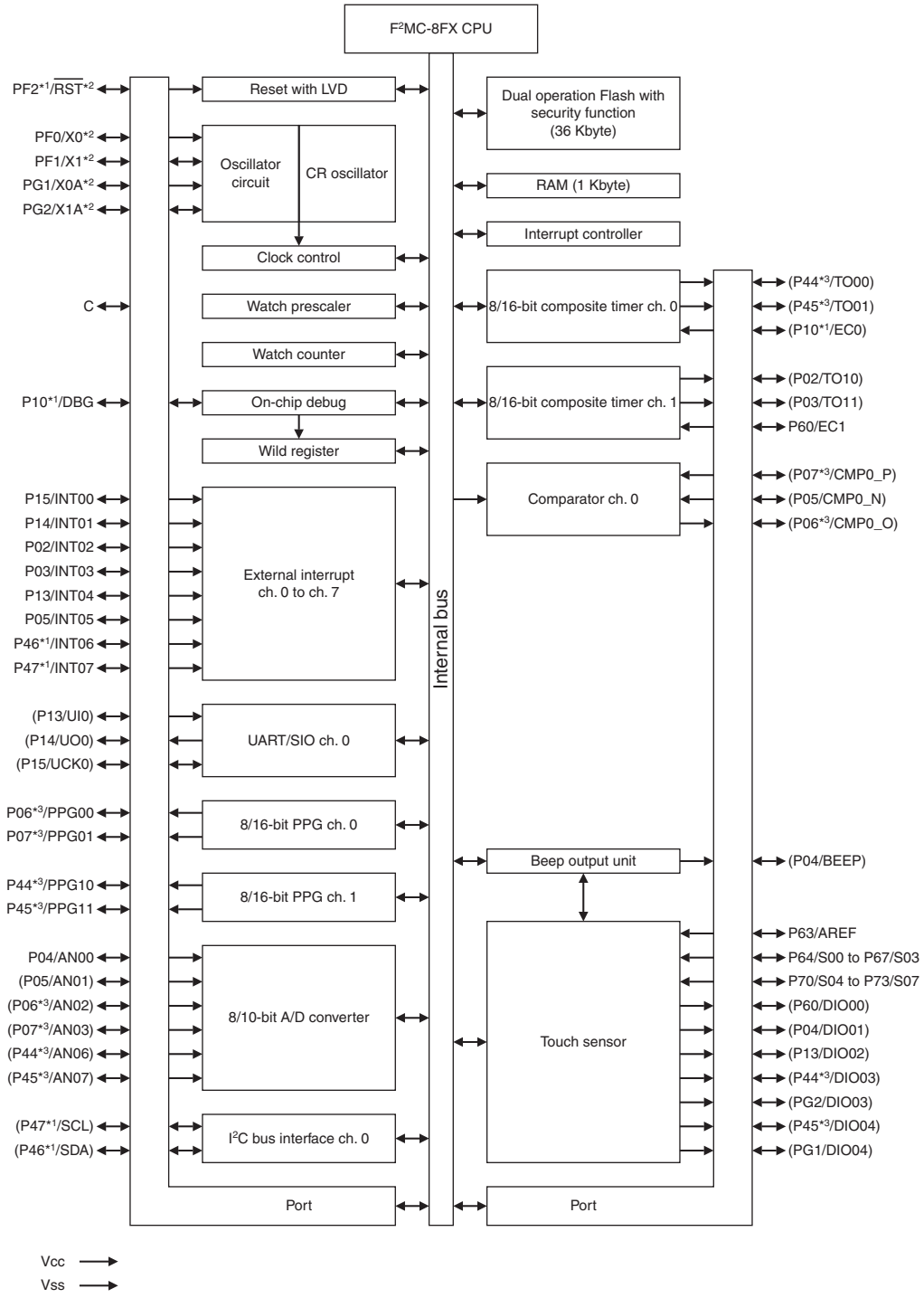
*1: P10, P46, P47 and PF2 are N-ch open drain pins.

*2: Software select

*3: P06 and P07 are high-current pins.

Note: Pins in parentheses indicate that those pins are shared among different peripheral functions.

Block Diagram (MB95860K Series)



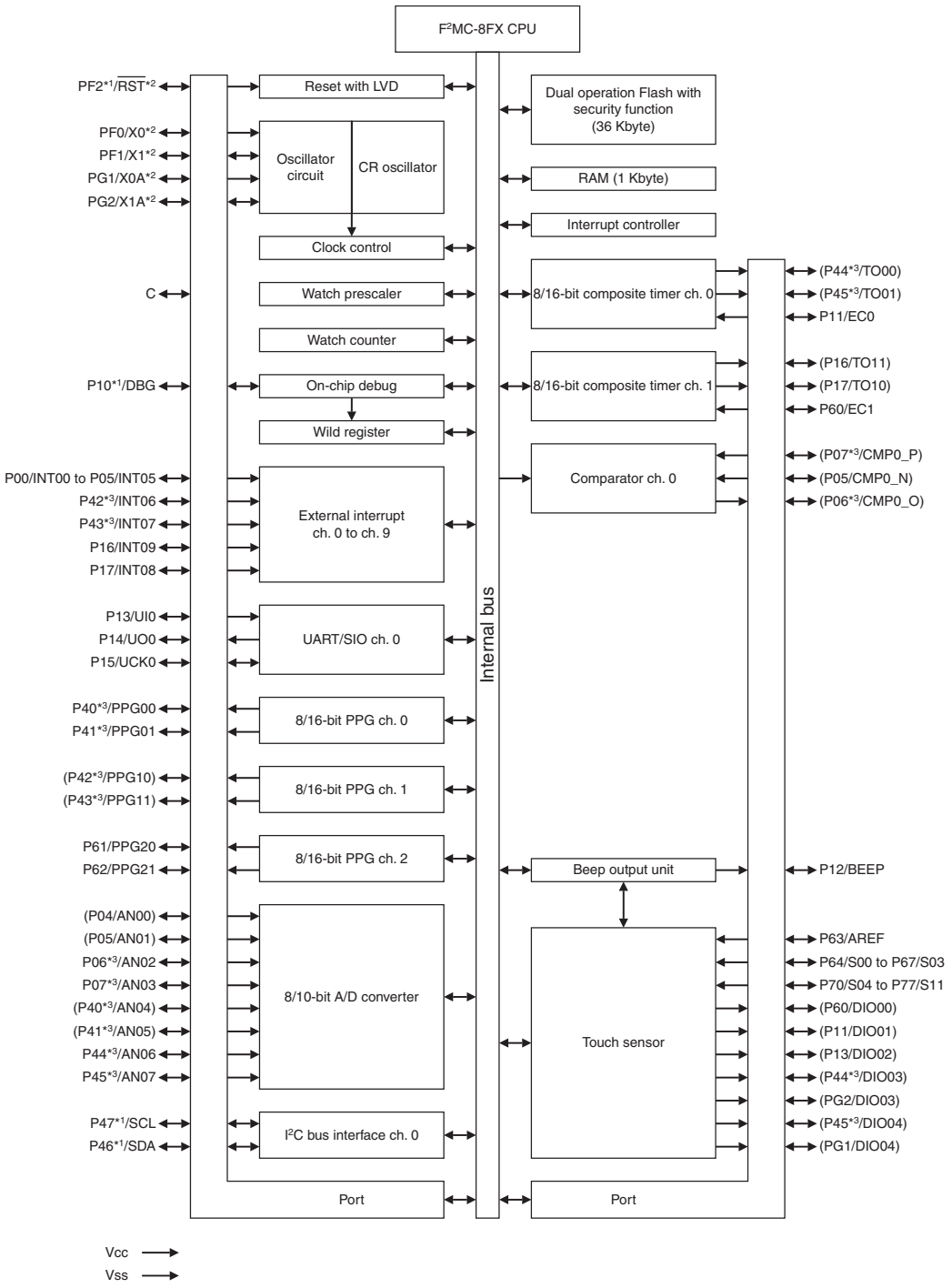
*1: P10, P46, P47 and PF2 are N-ch open drain pins.

*2: Software select

*3: P06, P07, P44 and P45 are high-current pins.

Note: Pins in parentheses indicate that those pins are shared among different peripheral functions.

Block Diagram (MB95870K Series)



*1: P10, P46, P47 and PF2 are N-ch open drain pins.
*2: Software select
*3: P06, P07, and P40 to P45 are high-current pins.

Note: Pins in parentheses indicate that those pins are shared among different peripheral functions.

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1. Product Line-up

Parameter	MB95F856K	MB95F866K	MB95F876K
Type	Flash memory product		
Clock supervisor counter	It supervises the main clock oscillation and the subclock oscillation.		
Flash memory capacity	36 Kbyte		
RAM capacity	1 Kbyte		
Power-on reset	Yes		
Low-voltage detection reset	Yes		
Reset input	Selected through software		
CPU functions	• Number of basic instructions: 136 • Instruction bit length: 8 bits • Instruction length: 1 to 3 bytes • Data bit length: 1, 8 and 16 bits • Minimum instruction execution time: 61.5 ns (machine clock frequency = 16.25 MHz) • Interrupt processing time: 0.6 µs (machine clock frequency = 16.25 MHz)		
General-purpose I/O	• I/O port:21 • CMOS I/O:17 • N-ch open drain:4	• I/O port:29 • CMOS I/O:25 • N-ch open drain:4	• I/O port:45 • CMOS I/O:41 • N-ch open drain:4
Time-base timer	Interval time: 0.256 ms to 8.3 s (external clock frequency = 4 MHz)		
Hardware/software watchdog timer	• Reset generation cycle - Main oscillation clock at 10 MHz: 105 ms (Min) • The sub-CR clock can be used as the source clock of the software watchdog timer.		
Wild register	It can be used to replace three bytes of data.		
8/10-bit A/D converter	4 channels	6 channels	8 channels
	8-bit or 10-bit resolution can be selected.		
8/16-bit composite timer	1 channel	2 channels	2 channels
	• The timer can be configured as an “8-bit timer × 2 channels” or a “16-bit timer × 1 channel”. • It has the following functions: interval timer function, PWC function, PWM function and input capture function. • Count clock: it can be selected from internal clocks (seven types) and external clocks. • It can output square wave.		
External interrupt	6 channels	8 channels	10 channels
	Interrupt by edge detection (The rising edge, falling edge, and both edges can be selected.) It can be used to wake up the device from different standby modes.		
On-chip debug	• 1-wire serial control • It supports serial writing (asynchronous mode).		
UART/SIO	1 channel		
	• Data transfer with UART/SIO is enabled. • It has a full duplex double buffer, variable data length (5/6/7/8 bits), an internal baud rate generator and an error detection function. • It uses the NRZ type transfer format. • LSB-first data transfer and MSB-first data transfer are available to use. • Both clock asynchronous (UART) serial data transfer and clock synchronous (SIO) serial data transfer are enabled.		

Parameter	MB95F856K	MB95F866K	MB95F876K
I^2C bus interface	1 channel		
	• Master/slave transmission and receiving • It has the following functions: bus error function, arbitration function, transmission direction detection function, wake-up function, and functions of generating and detecting repeated START conditions.		
8/16-bit PPG	1 channels	2 channels	3 channels
	• Each channel can be used as an “8-bit timer × 2 channels” or a “16-bit timer × 1 channel”. • The counter operating clock can be selected from eight clock sources.		
Touch sensor (TS)	5 touch channels	8 touch channels	12 touch channels
	• Two types of interrupt: GINT for general purpose and TINT for touch detection • 8-bit resolution of touch strength data (256 steps) • Five DIO pins as direct touch outputs • Beep generation for tactile feeling		
Beep output unit	The beep output unit can be activated by using the software or the TS.		
Watch counter	• Count clock: it can be selected from eight clock sources from the watch prescaler. • The counter value can be selected from 0 to 63. (The watch counter can count for one minute when the clock source of one second is selected and 60 is selected as the counter value.)		
Watch prescaler	Eight different time intervals can be selected.		
Comparator	1 channel		
	The comparator reference voltage can be selected between the BGR voltage and the comparator pin.		
Flash memory	• It supports automatic programming (Embedded Algorithm), and program/erase/erase-suspend/erase-resume commands. • It has a flag indicating the completion of the operation of Embedded Algorithm. • Flash security feature for protecting the content of the Flash memory		
	Number of program/erase cycles: 1000 / 10000 / 100000 Data retention time: 20 years / 10 years / 5 years		
Standby mode	There are four standby modes as follows: • Stop mode • Sleep mode • Watch mode • Time-base timer mode In standby mode, two further options can be selected: normal standby mode and deep standby mode.		
Package	STI024 SOL024 LQB032 LQA048 LQC052		

2. Packages and Corresponding Products

Package	MB95F856K	MB95F866K	MB95F876K
STI024	O	X	X
SOL024	O	X	X
LQB032	X	O	X
LQA048	X	X	O
LQC052	X	X	O

O: Available

X: Unavailable

3. Differences Among Products and Notes on Product Selection

■ Current consumption

When using the on-chip debug function, take account of the current consumption of Flash memory program/erase.

For details of current consumption, see Electrical Characteristics on page 135.

■ Package

For details of information on each package, see Packages and Corresponding Products and Package Dimension on page 163.

■ Operating voltage

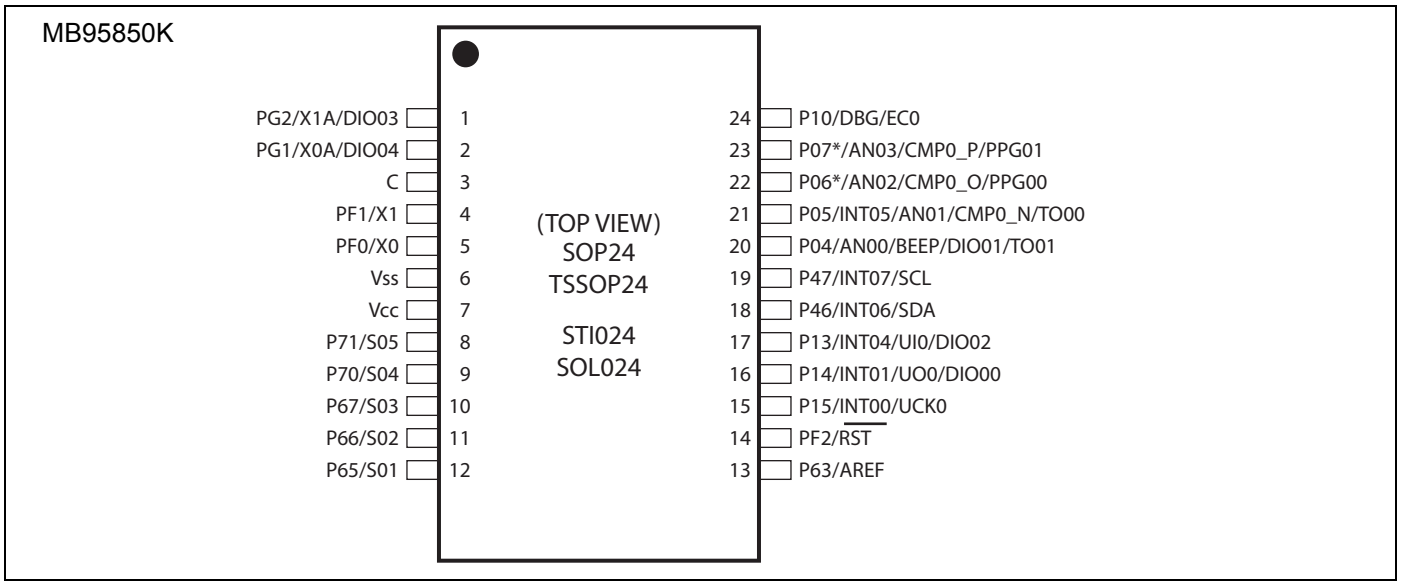
The operating voltage varies, depending on whether the on-chip debug function is used or not.

For details of operating voltage, see Electrical Characteristics on page 135.

■ On-chip debug function

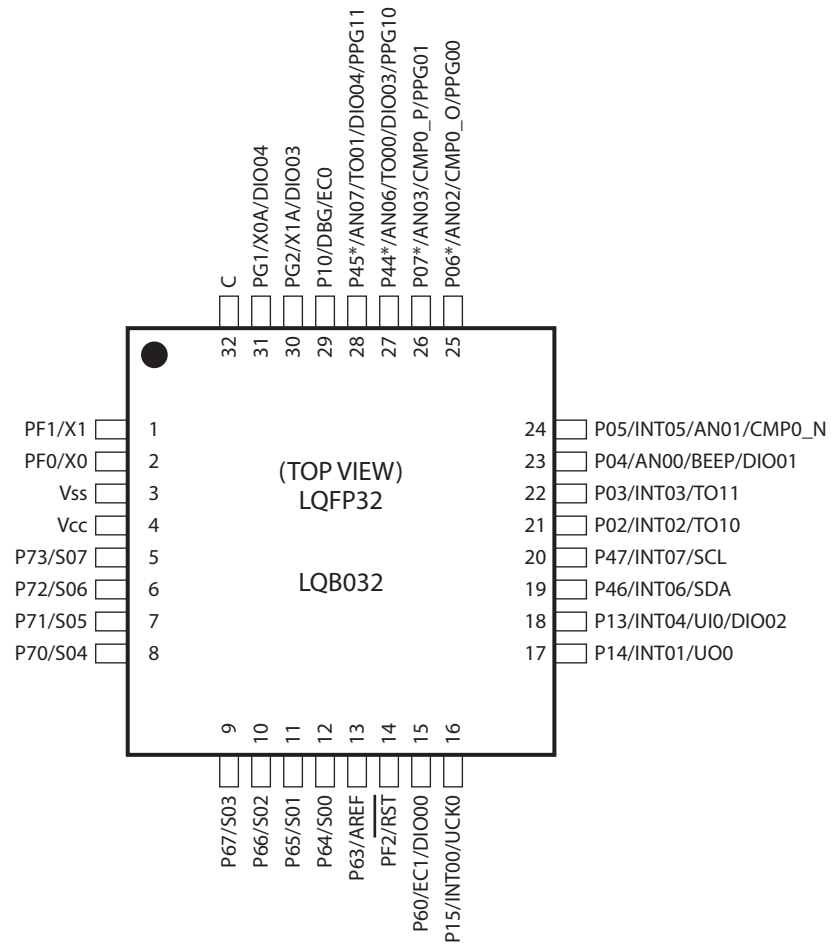
The on-chip debug function requires that V_{CC}, V_{SS} and one serial wire be connected to an evaluation tool. For details of the connection method, refer to “CHAPTER 24 EXAMPLE OF SERIAL PROGRAMMING CONNECTION” in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

4. Pin Assignment

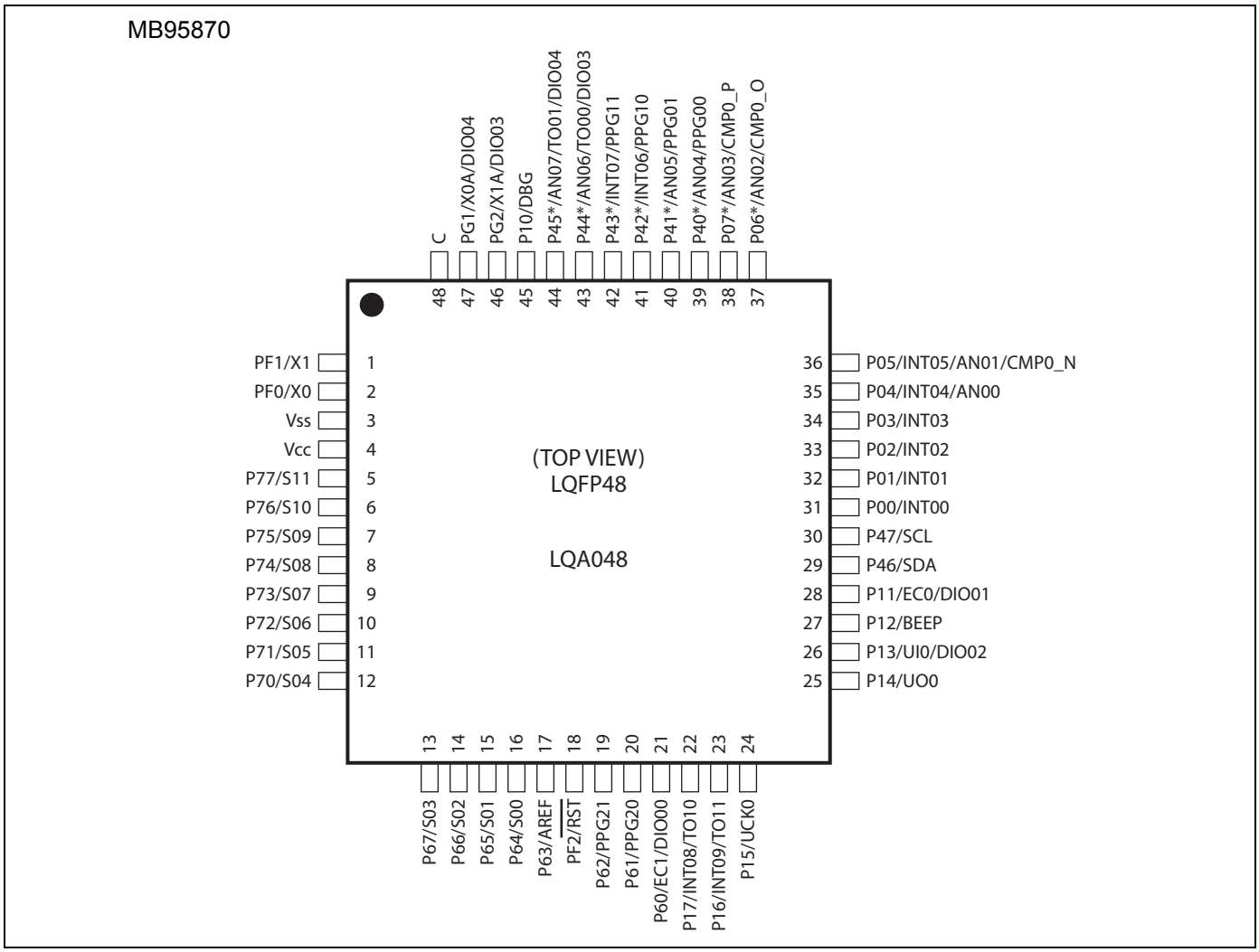


*: High-current pin (8 mA/12 mA)

MB95860K

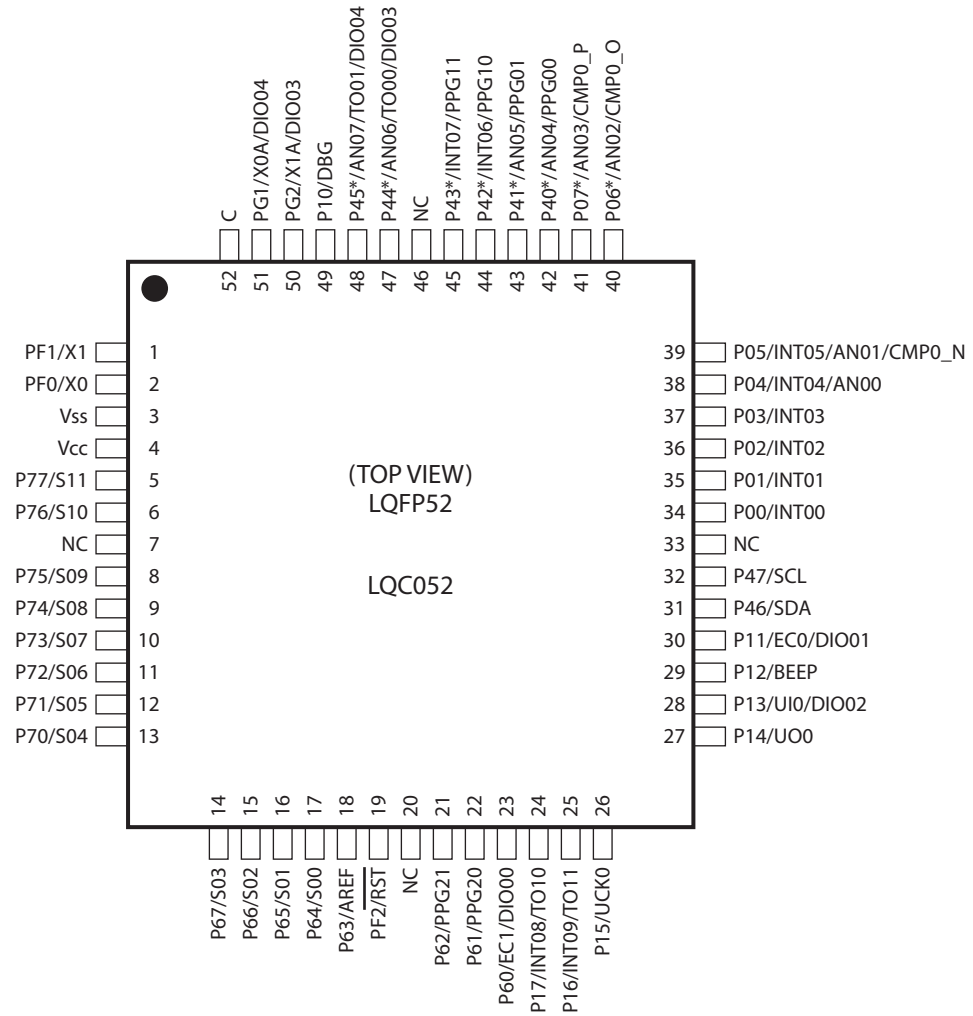


*: High-current pin (8 mA/12 mA)



*: High-current pin (8 mA/12 mA)

MB958



*: High-current pin (8 mA/12 mA)

5. Pin Functions

5.1 MB95850K Series

Pin no.	Pin name	I/O circuit type[1]	Function	I/O type			
				Input	Output	OD[2]	PU[3]
1	PG2	C	General-purpose I/O port	Hysteresis	CMOS	—	O
	X1A		Subclock I/O oscillation pin				
	DIO03		TS direct output ch. 3 pin				
2	PG1	C	General-purpose I/O port	Hysteresis	CMOS	—	O
	X0A		Subclock input oscillation pin				
	DIO04		TS direct output ch. 4 pin				
3	C	—	Decoupling capacitor connection pin	—	—	—	—
4	PF1	B	General-purpose I/O port	Hysteresis	CMOS	—	—
	X1		Main clock I/O oscillation pin				
5	PF0	B	General-purpose I/O port	Hysteresis	CMOS	—	—
	X0		Main clock input oscillation pin				
6	V_{SS}	—	Power supply pin (GND)	—	—	—	—
7	V_{CC}	—	Power supply pin	—	—	—	—
8	P71	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	S05		TS touch ch. 5 input pin				
9	P70	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	S04		TS touch ch. 4 input pin				
10	P67	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	S03		TS touch ch. 3 input pin				
11	P66	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	S02		TS touch ch. 2 input pin				
12	P65	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	S01		TS touch ch. 1 input pin				
13	P63	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	AREF		TS reference impedance input pin				
14	PF2	A	General-purpose I/O port	Hysteresis	CMOS	O	—
	RST		Reset pin				
15	P15	G	General-purpose I/O port	Hysteresis	CMOS	—	O
	INT00		External interrupt input pin				
	UCK0		UART/SIO ch. 0 clock I/O pin				
16	P14	G	General-purpose I/O port	Hysteresis	CMOS	—	O
	INT01		External interrupt input pin				
	UO0		UART/SIO ch. 0 data output pin				
	DIO00		TS direct output ch. 0 pin				

Pin no.	Pin name	I/O circuit type[1]	Function	I/O type			
				Input	Output	OD[2]	PU[3]
17	P13	J	General-purpose I/O port	CMOS	CMOS	—	O
	INT04		External interrupt input pin				
	UI0		UART/SIO ch. 0 data input pin				
	DIO02		TS direct output ch. 2 pin				
18	P46	I	General-purpose I/O port	CMOS	CMOS	O	—
	INT06		External interrupt input pin				
	SDA		I^2C bus interface ch. 0 data I/O pin				
19	P47	I	General-purpose I/O port	CMOS	CMOS	O	—
	INT07		External interrupt input pin				
	SCL		I^2C bus interface ch. 0 clock I/O pin				
20	P04	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	AN00		8/10-bit A/D converter analog input pin				
	BEEP		Beep output pin				
	DIO01		TS direct output ch. 1 pin				
	TO01		8/16-bit composite timer ch. 0 output pin				
21	P05	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	INT05		External interrupt input pin				
	AN01		8/10-bit A/D converter analog input pin				
	CMP0_N		Comparator ch. 0 inverting analog input (negative input) pin				
	TO00		8/16-bit composite timer ch. 0 output pin				
22	P06	K	General-purpose I/O port, High-current pin	Hysteresis/ analog	CMOS	—	O
	AN02		8/10-bit A/D converter analog input pin				
	CMP0_O		Comparator ch. 0 digital output pin				
	PPG00		8/16-bit PPG ch. 0 output pin				
23	P07	K	General-purpose I/O port High-current pin	Hysteresis/ analog	CMOS	—	O
	AN03		8/10-bit A/D converter analog input pin				
	CMP0_P		Comparator ch. 0 non-inverting analog input (positive input) pin				
	PPG01		8/16-bit PPG ch. 0 output pin				
24	P10	H	General-purpose I/O port	Hysteresis	CMOS	O	—
	DBG		DBG input pin				
	EC0		8/16-bit composite timer ch. 0 clock input pin				

O: Available

Notes
1. For the I/O circuit types, see I/O Circuit Type.
2. N-ch open drain
3. Pull-up

5.2 MB95860K Series

Pin no.	Pin name	I/O circuit type[4]	Function	I/O type			
				Input	Output	OD[5]	PU[6]
1	PF1	B	General-purpose I/O port	Hysteresis	CMOS	—	—
	X1		Main clock I/O oscillation pin				
2	PF0	B	General-purpose I/O port	Hysteresis	CMOS	—	—
	X0		Main clock input oscillation pin				
3	V_{SS}	—	Power supply pin (GND)	—	—	—	—
4	V_{CC}	—	Power supply pin	—	—	—	—
5	P73	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	S07		TS touch ch. 7 input pin				
6	P72	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	S06		TS touch ch. 6 input pin				
7	P71	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	S05		TS touch ch. 5 input pin				
8	P70	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	S04		TS touch ch. 4 input pin				
9	P67	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	S03		TS touch ch. 3 input pin				
10	P66	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	S02		TS touch ch. 2 input pin				
11	P65	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	S01		TS touch ch. 1 input pin				
12	P64	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	S00		TS touch ch. 0 input pin				
13	P63	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	AREF		TS reference impedance input pin				
14	PF2	A	General-purpose I/O port	Hysteresis	CMOS	O	—
	RST		Reset pin				
15	P60	G	General-purpose I/O port	Hysteresis	CMOS	—	O
	EC1		8/16-bit composite timer ch. 1 clock input pin				
	DIO00		TS direct output ch. 0 pin				
16	P15	G	General-purpose I/O port	Hysteresis	CMOS	—	O
	INT00		External interrupt input pin				
	UCK0		UART/SIO ch. 0 clock I/O pin				
17	P14	G	General-purpose I/O port	Hysteresis	CMOS	—	O
	INT01		External interrupt input pin				
	UO0		UART/SIO ch. 0 data output pin				

Pin no.	Pin name	I/O circuit type[4]	Function	I/O type			
				Input	Output	OD[5]	PU[6]
18	P13	J	General-purpose I/O port	CMOS	CMOS	—	O
	INT04		External interrupt input pin				
	UI0		UART/SIO ch. 0 data input pin				
	DIO02		TS direct output ch. 2 pin				
19	P46	I	General-purpose I/O port	CMOS	CMOS	O	—
	INT06		External interrupt input pin				
	SDA		I^2C bus interface ch. 0 data I/O pin				
20	P47	I	General-purpose I/O port	CMOS	CMOS	O	—
	INT07		External interrupt input pin				
	SCL		I^2C bus interface ch. 0 clock I/O pin				
21	P02	G	General-purpose I/O port	Hysteresis	CMOS	—	O
	INT02		External interrupt input pin				
	TO10		8/16-bit composite timer ch. 1 output pin				
22	P03	G	General-purpose I/O port	Hysteresis	CMOS	—	O
	INT03		External interrupt input pin				
	TO11		8/16-bit composite timer ch. 1 output pin				
23	P04	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	AN00		8/10-bit A/D converter analog input pin				
	BEEP		Beep output pin				
	DIO01		TS direct output ch. 1 pin				
24	P05	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	INT05		External interrupt input pin				
	AN01		8/10-bit A/D converter analog input pin				
	CMP0_N		Comparator ch. 0 inverting analog input (negative input) pin				
25	P06	K	General-purpose I/O port High-current pin	Hysteresis/ analog	CMOS	—	O
	AN02		8/10-bit A/D converter analog input pin				
	CMP0_O		Comparator ch. 0 digital output pin				
	PPG00		8/16-bit PPG ch. 0 output pin				
26	P07	K	General-purpose I/O port High-current pin	Hysteresis/ analog	CMOS	—	O
	AN03		8/10-bit A/D converter analog input pin				
	CMP0_P		Comparator ch. 0 non-inverting analog input (positive input) pin				
	PPG01		8/16-bit PPG ch. 0 output pin				
27	P44	K	General-purpose I/O port High-current pin	Hysteresis/ analog	CMOS	—	O
	AN06		8/10-bit A/D converter analog input pin				
	TO00		8/16-bit composite timer ch. 0 output pin				
	DIO03		TS direct output ch. 3 pin				
	PPG10		8/16-bit PPG ch. 1 output pin				

Pin no.	Pin name	I/O circuit type[4]	Function	I/O type			
				Input	Output	OD[5]	PU[6]
28	P45	K	General-purpose I/O port High-current pin	Hysteresis/ analog	CMOS	—	O
	AN07		8/10-bit A/D converter analog input pin				
	TO01		8/16-bit composite timer ch. 0 output pin				
	DIO04		TS direct output ch. 4 pin				
	PPG11		8/16-bit PPG ch. 1 output pin				
29	P10	H	General-purpose I/O port	Hysteresis	CMOS	O	—
	DBG		DBG input pin				
	EC0		8/16-bit composite timer ch. 0 clock input pin				
30	PG2	C	General-purpose I/O port	Hysteresis	CMOS	—	O
	X1A		Subclock I/O oscillation pin				
	DIO03		TS direct output ch. 3 pin				
31	PG1	C	General-purpose I/O port	Hysteresis	CMOS	—	O
	X0A		Subclock input oscillation pin				
	DIO04		TS direct output ch. 4 pin				
32	C	—	Decoupling capacitor connection pin	—	—	—	—

O: Available

Notes
4. For the I/O circuit types, see I/O Circuit Type.
5. N-ch open drain
6. Pull-up

5.3 MB95870K Series

Pin no.		Pin name	I/O circuit type[9]	Function	I/O type			
LQFP48[7]	LQFP52[8]				Input	Output	OD[10]	PU[11]
1	1	PF1	B	General-purpose I/O port	Hysteresis	CMOS	—	—
		X1		Main clock I/O oscillation pin				
2	2	PF0	B	General-purpose I/O port	Hysteresis	CMOS	—	—
		X0		Main clock input oscillation pin				
3	3	V_{SS}	—	Power supply pin (GND)	—	—	—	—
4	4	V_{CC}	—	Power supply pin	—	—	—	—
5	5	P77	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		S11		TS touch ch. 11 input pin				
6	6	P76	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		S10		TS touch ch. 10 input pin				
—	7	NC	—	It is an internally connected pin. Always leave it unconnected.	—	—	—	—
7	8	P75	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		S09		TS touch ch. 9 input pin				
8	9	P74	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		S08		TS touch ch. 8 input pin				
9	10	P73	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		S07		TS touch ch. 7 input pin				
10	11	P72	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		S06		TS touch ch. 6 input pin				
11	12	P71	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		S05		TS touch ch. 5 input pin				
12	13	P70	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		S04		TS touch ch. 4 input pin				
13	14	P67	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		S03		TS touch ch. 3 input pin				
14	15	P66	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		S02		TS touch ch. 2 input pin				
15	16	P65	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		S01		TS touch ch. 1 input pin				
16	17	P64	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		S00		TS touch ch. 0 input pin				
17	18	P63	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		AREF		TS reference impedance input pin				
18	19	PF2	A	General-purpose I/O port	Hysteresis	CMOS	O	—
		RST		Reset pin				
—	20	NC	—	It is an internally connected pin. Always leave it unconnected.	—	—	—	—

Pin no.		Pin name	I/O circuit type[9]	Function	I/O type			
LQFP48[7]	LQFP52[8]				Input	Output	OD[10]	PU[11]
19	21	P62	G	General-purpose I/O port	Hysteresis	CMOS	—	O
		PPG21		8/16-bit PPG ch. 2 output pin				
20	22	P61	G	General-purpose I/O port	Hysteresis	CMOS	—	O
		PPG20		8/16-bit PPG ch. 2 output pin				
21	23	P60	G	General-purpose I/O port	Hysteresis	CMOS	—	O
		EC1		8/16-bit composite timer ch. 1 clock input pin				
		DIO00		TS direct output ch. 0 pin				
22	24	P17	G	General-purpose I/O port	Hysteresis	CMOS	—	O
		INT08		External interrupt input pin				
		TO10		8/16-bit composite timer ch. 1 output pin				
23	25	P16	G	General-purpose I/O port	Hysteresis	CMOS	—	O
		INT09		External interrupt input pin				
		TO11		8/16-bit composite timer ch. 1 output pin				
24	26	P15	G	General-purpose I/O port	Hysteresis	CMOS	—	O
		UCK0		UART/SIO ch. 0 clock I/O pin				
25	27	P14	G	General-purpose I/O port	Hysteresis	CMOS	—	O
		UO0		UART/SIO ch. 0 data output pin				
26	28	P13	J	General-purpose I/O port	CMOS	CMOS	—	O
		UI0		UART/SIO ch. 0 data input pin				
		DIO02		TS direct output ch. 2 pin				
27	29	P12	G	General-purpose I/O port	Hysteresis	CMOS	—	O
		BEEP		Beep output pin				
28	30	P11	G	General-purpose I/O port	Hysteresis	CMOS	—	O
		EC0		8/16-bit composite timer ch. 0 clock input pin				
		DIO01		TS direct output ch. 1 pin				
29	31	P46	I	General-purpose I/O port	CMOS	CMOS	O	—
		SDA		I^2C bus interface ch. 0 data I/O pin				
30	32	P47	I	General-purpose I/O port	CMOS	CMOS	O	—
		SCL		I^2C bus interface ch. 0 clock I/O pin				
—	33	NC	—	It is an internally connected pin. Always leave it unconnected.	—	—	—	—
31	34	P00	G	General-purpose I/O port	Hysteresis	CMOS	—	O
		INT00		External interrupt input pin				
32	35	P01	G	General-purpose I/O port	Hysteresis	CMOS	—	O
		INT01		External interrupt input pin				
33	36	P02	G	General-purpose I/O port	Hysteresis	CMOS	—	O
		INT02		External interrupt input pin				
34	37	P03	G	General-purpose I/O port	Hysteresis	CMOS	—	O
		INT03		External interrupt input pin				

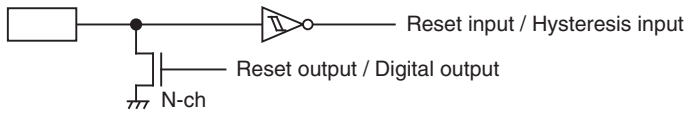
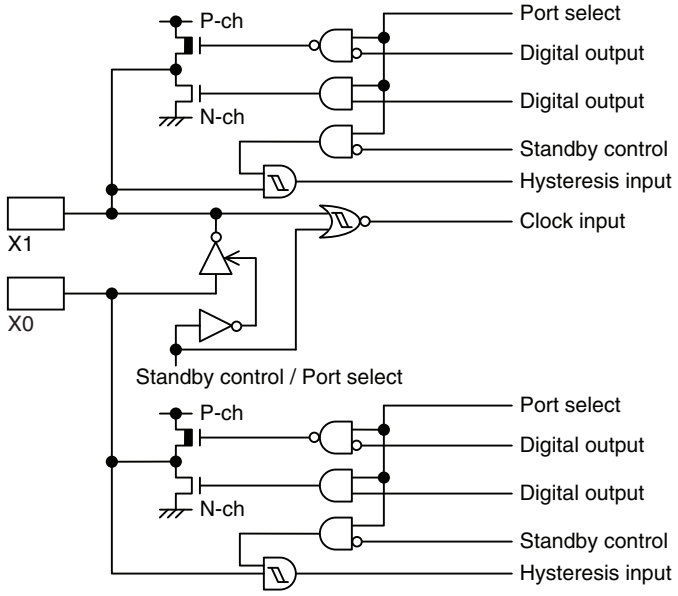
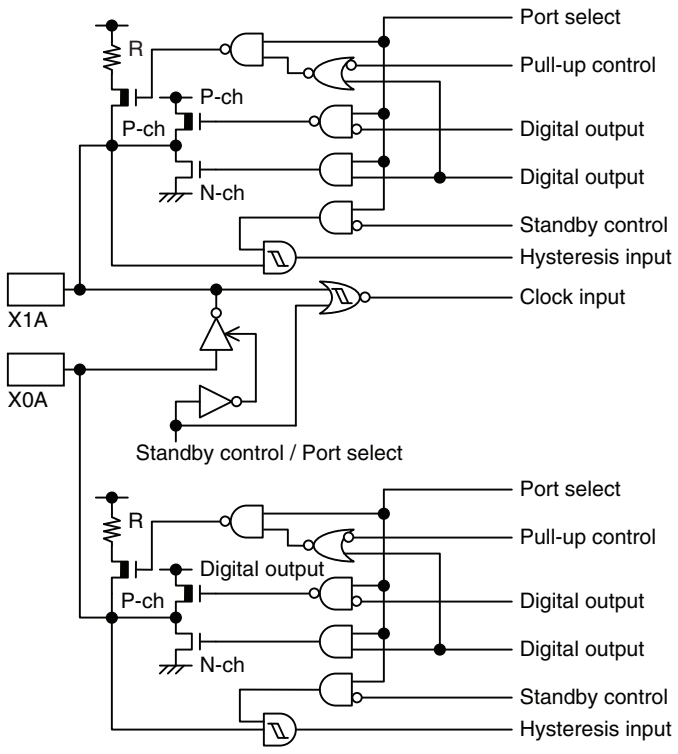
Pin no.		Pin name	I/O circuit type[9]	Function	I/O type			
LQFP48[7]	LQFP52[8]				Input	Output	OD[10]	PU[11]
35	38	P04	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		INT04		External interrupt input pin				
		AN00		8/10-bit A/D converter analog input pin				
36	39	P05	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		INT05		External interrupt input pin				
		AN01		8/10-bit A/D converter analog input pin				
		CMP0_N		Comparator ch. 0 inverting analog input (negative input) pin				
37	40	P06	K	General-purpose I/O port High-current pin	Hysteresis/ analog	CMOS	—	O
		AN02		8/10-bit A/D converter analog input pin				
		CMP0_O		Comparator ch. 0 digital output pin				
38	41	P07	K	General-purpose I/O port High-current pin	Hysteresis/ analog	CMOS	—	O
		AN03		8/10-bit A/D converter analog input pin				
		CMP0_P		Comparator ch. 0 non-inverting analog input (positive input) pin				
39	42	P40	K	General-purpose I/O port High-current pin	Hysteresis/ analog	CMOS	—	O
		AN04		8/10-bit A/D converter analog input pin				
		PPG00		8/16-bit PPG ch. 0 output pin				
40	43	P41	K	General-purpose I/O port High-current pin	Hysteresis/ analog	CMOS	—	O
		AN05		8/10-bit A/D converter analog input pin				
		PPG01		8/16-bit PPG ch. 0 output pin				
41	44	P42	D	General-purpose I/O port High-current pin	Hysteresis	CMOS	—	O
		INT06		External interrupt input pin				
		PPG10		8/16-bit PPG ch. 1 output pin				
42	45	P43	D	General-purpose I/O port High-current pin	Hysteresis	CMOS	—	O
		INT07		External interrupt input pin				
		PPG11		8/16-bit PPG ch. 1 output pin				
—	46	NC	—	It is an internally connected pin. Always leave it unconnected.	—	—	—	—
43	47	P44	K	General-purpose I/O port High-current pin	Hysteresis/ analog	CMOS	—	O
		AN06		8/10-bit A/D converter analog input pin				
		TO00		8/16-bit composite timer ch. 0 output pin				
		DIO03		TS direct output ch. 3 pin				

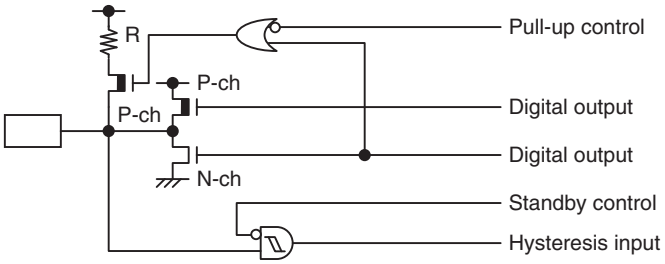
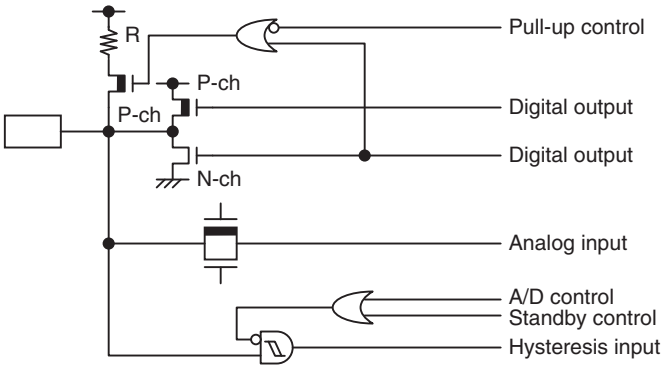
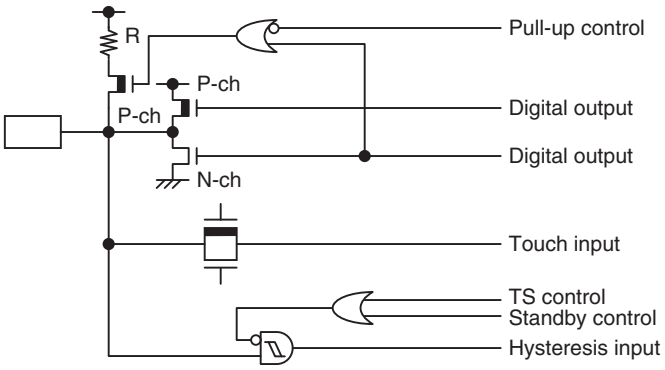
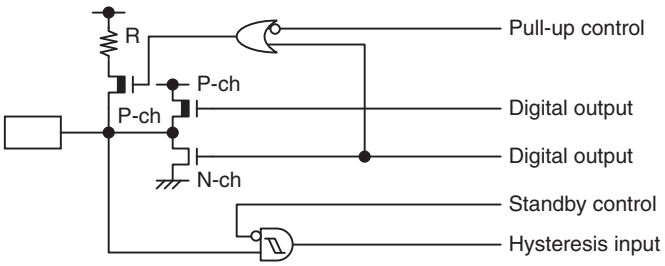
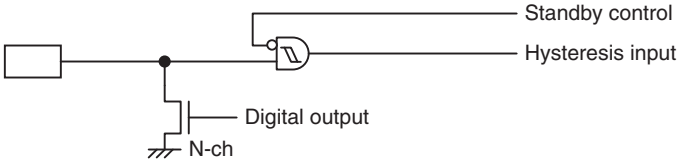
Pin no.		Pin name	I/O circuit type[9]	Function	I/O type			
LQFP48[7]	LQFP52[8]				Input	Output	OD[10]	PU[11]
44	48	P45	K	General-purpose I/O port High-current pin	Hysteresis/ analog	CMOS	—	O
		AN07		8/10-bit A/D converter analog input pin				
		TO01		8/16-bit composite timer ch. 0 output pin				
		DIO04		TS direct output ch. 4 pin				
45	49	P10	H	General-purpose I/O port	Hysteresis	CMOS	O	—
		DBG		DBG input pin				
46	50	PG2	C	General-purpose I/O port	Hysteresis	CMOS	—	O
		X1A		Subclock I/O oscillation pin				
		DIO03		TS direct output ch. 3 pin				
47	51	PG1	C	General-purpose I/O port	Hysteresis	CMOS	—	O
		X0A		Subclock input oscillation pin				
		DIO04		TS direct output ch. 4 pin				
48	52	C	—	Decoupling capacitor connection pin	—	—	—	—

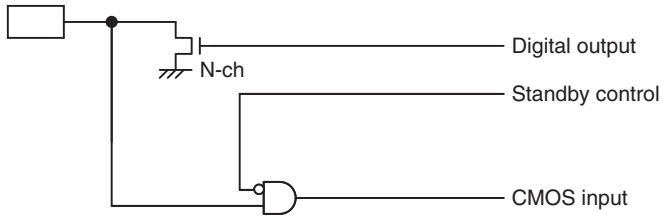
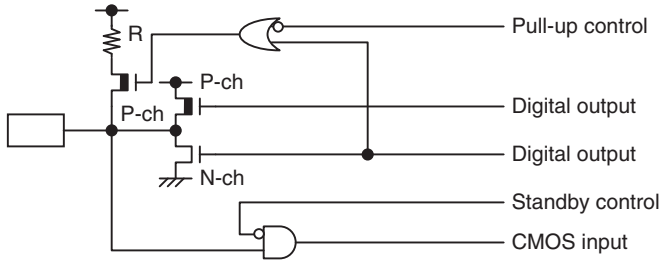
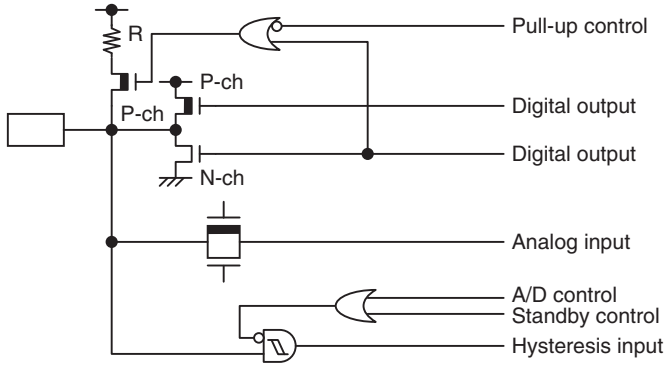
O: Available

Notes
7. LQA048
8. LQC052
9. For the I/O circuit types, see I/O Circuit Type.
10. N-ch open drain
11. Pull-up

6. I/O Circuit Type

Type	Circuit	Remarks
A		• N-ch open drain output • Hysteresis input • Reset output
B		• Oscillation circuit • High-speed side Feedback resistance: approx. 1 MΩ CMOS output • Hysteresis input
C		• Oscillation circuit • Low-speed side Feedback resistance: approx. 5 MΩ CMOS output • Hysteresis input • Pull-up control

Type	Circuit	Remarks
D		• CMOS output • Hysteresis input • Pull-up control • High current output
E		• CMOS output • Hysteresis input • Pull-up control • Analog input
F		• CMOS output • Hysteresis input • Pull-up control • Touch input • High electrostatic discharge (ESD)
G		• CMOS output • Hysteresis input • Pull-up control
H		• N-ch open drain output • Hysteresis input

Type	Circuit	Remarks
I		• N-ch open drain output • CMOS input
J		• CMOS output • CMOS input • Pull-up control
K		• CMOS output • Hysteresis input • Pull-up control • Analog input • High-current output

7. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

7.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

■ Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

■ Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

■ Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

❒ Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

❒ Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.

Therefore, avoid this type of connection.

❒ Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

■ Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

❒ Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

❒ Be sure that abnormal current flows do not occur during the power-on sequence.

■ Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

■ Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

■ Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

7.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress recommended conditions. For detailed information about mount conditions, contact your sales representative.

■ Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket. Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

■ Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

■ Lead-Free Packaging

When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

■ Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

- Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
- Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5 °C and 30 °C. When you open Dry Package that recommends humidity 40% to 70% relative humidity.
- When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
- Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

■ Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125 °C/24 h

■ Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

- Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
- Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
- Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ). Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
- Ground all fixtures and instruments, or protect with anti-static measures.
- Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

7.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

- Humidity: Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.
- Discharge of Static Electricity: When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.
- Corrosive Gases, Dust, or Oil: Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.
- Radiation, Including Cosmic Radiation: Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.
- Smoke, Flame:

Caution: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

8. Notes on Device Handling

■ Preventing latch-ups

When using the device, ensure that the voltage applied does not exceed the maximum voltage rating.

In a CMOS IC, if a voltage higher than V_{CC} or a voltage lower than V_{SS} is applied to an input/output pin that is neither a medium-withstand voltage pin nor a high-withstand voltage pin, or if a voltage out of the rating range of power supply voltage mentioned in "Absolute Maximum Ratings" of Electrical Characteristics on page 135 is applied to the V_{CC} pin or the V_{SS} pin, a latch-up may occur.

When a latch-up occurs, power supply current increases significantly, which may cause a component to be thermally destroyed.

■ Stabilizing supply voltage

Supply voltage must be stabilized.

A malfunction may occur when power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the V_{CC} power supply voltage.

As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in V_{CC} ripple (p-p value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard V_{CC} value, and the transient fluctuation rate does not exceed 0.1 V/ms at a momentary fluctuation such as switching the power supply.

■ Notes on using the external clock

When an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from subclock mode or stop mode.

9. Pin Connection

■ Treatment of unused pins

If an unused input pin is left unconnected, a component may be permanently damaged due to malfunctions or latch-ups. Always pull up or pull down an unused input pin through a resistor of at least 2 kΩ. Set an unused input/output pin to the output state and leave it unconnected, or set it to the input state and treat it the same as an unused input pin. If there is an unused output pin, leave it unconnected.

■ Power supply pins

To reduce unnecessary electro-magnetic emission, prevent malfunctions of strobe signals due to an increase in the ground level, and conform to the total output current standard, always connect the V_{CC} pin and the V_{SS} pin to the power supply and ground outside the device. In addition, connect the current supply source to the V_{CC} pin and the V_{SS} pin with low impedance.

It is also advisable to connect a ceramic capacitor of approximately 0.1 µF as a bypass capacitor between the V_{CC} pin and the V_{SS} pin at a location close to this device.

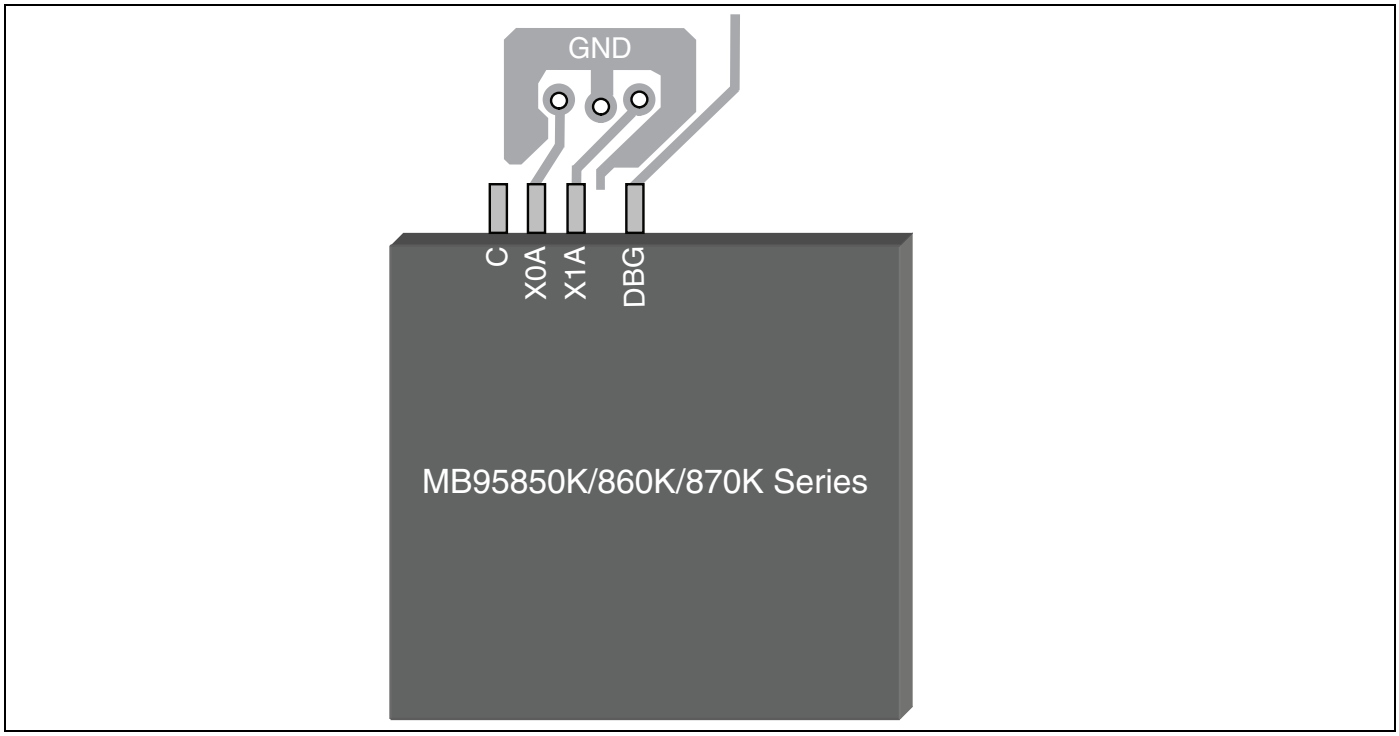
■ DBG pin

Connect the DBG pin to an external pull-up resistor of 2 kΩ or above.

After power-on, ensure that the DBG pin does not stay at “L” level until the reset output is released.

The DBG pin becomes a communication pin in debug mode. Since the actual pull-up resistance depends on the tool used and the interconnection length, refer to the tool document when selecting a pull-up resistor.

The recommended layout method illustrated in the following diagram aims to avoid noise coupled between the subclock I/O oscillation pin (X1A) and the DBG pin, which may cause the suboscillator to malfunction.



■ $\overline{\text{RST}}$ pin

Connect the $\overline{\text{RST}}$ pin to an external pull-up resistor of 2 kΩ or above.

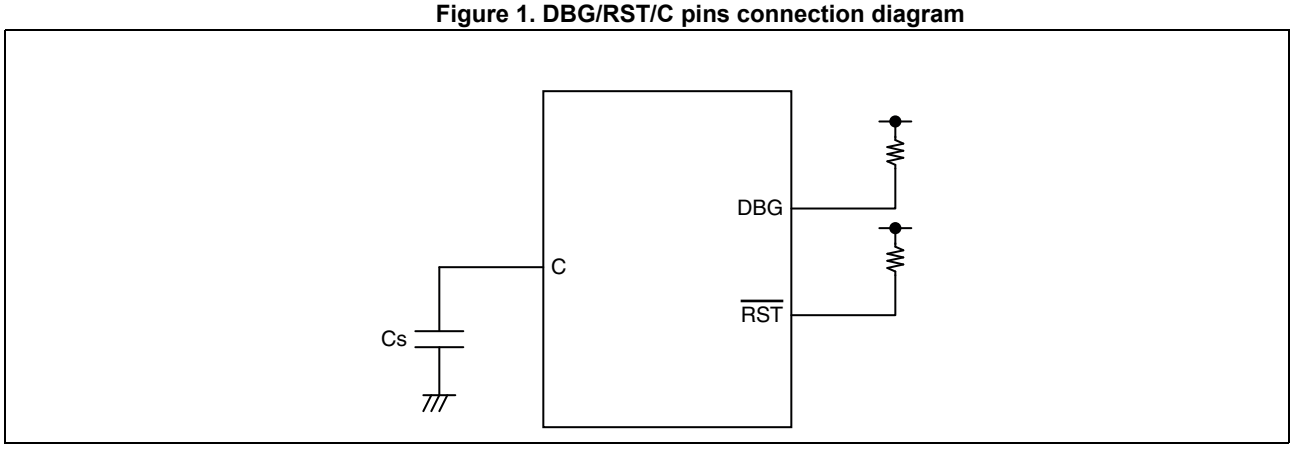
To prevent the device from unintentionally entering the reset mode due to noise, minimize the interconnection length between a pull-up resistor and the $\overline{\text{RST}}$ pin and that between a pull-up resistor and the V_{CC} pin when designing the layout of the printed circuit board.

The PF2/$\overline{\text{RST}}$ pin functions as the reset input/output pin after power-on. In addition, the reset output of the PF2/$\overline{\text{RST}}$ pin can be enabled by the RSTOE bit in the SYSC register, and the reset input function and the general purpose I/O function can be selected by the RSTEN bit in the SYSC register.

■ C pin

Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The bypass capacitor for the V_{CC} pin must have a capacitance larger than C_S. For the connection to a decoupling capacitor C_S, see the diagram below. To prevent the device from unintentionally entering a mode to which the device is not set to transit due to noise, minimize the distance between the C pin and C_S and the distance between C_S and the V_{SS} pin when designing the layout of a printed circuit board.

Figure 1. DBG/$\overline{\text{RST}}$/C pins connection diagram



■ Note on serial communication

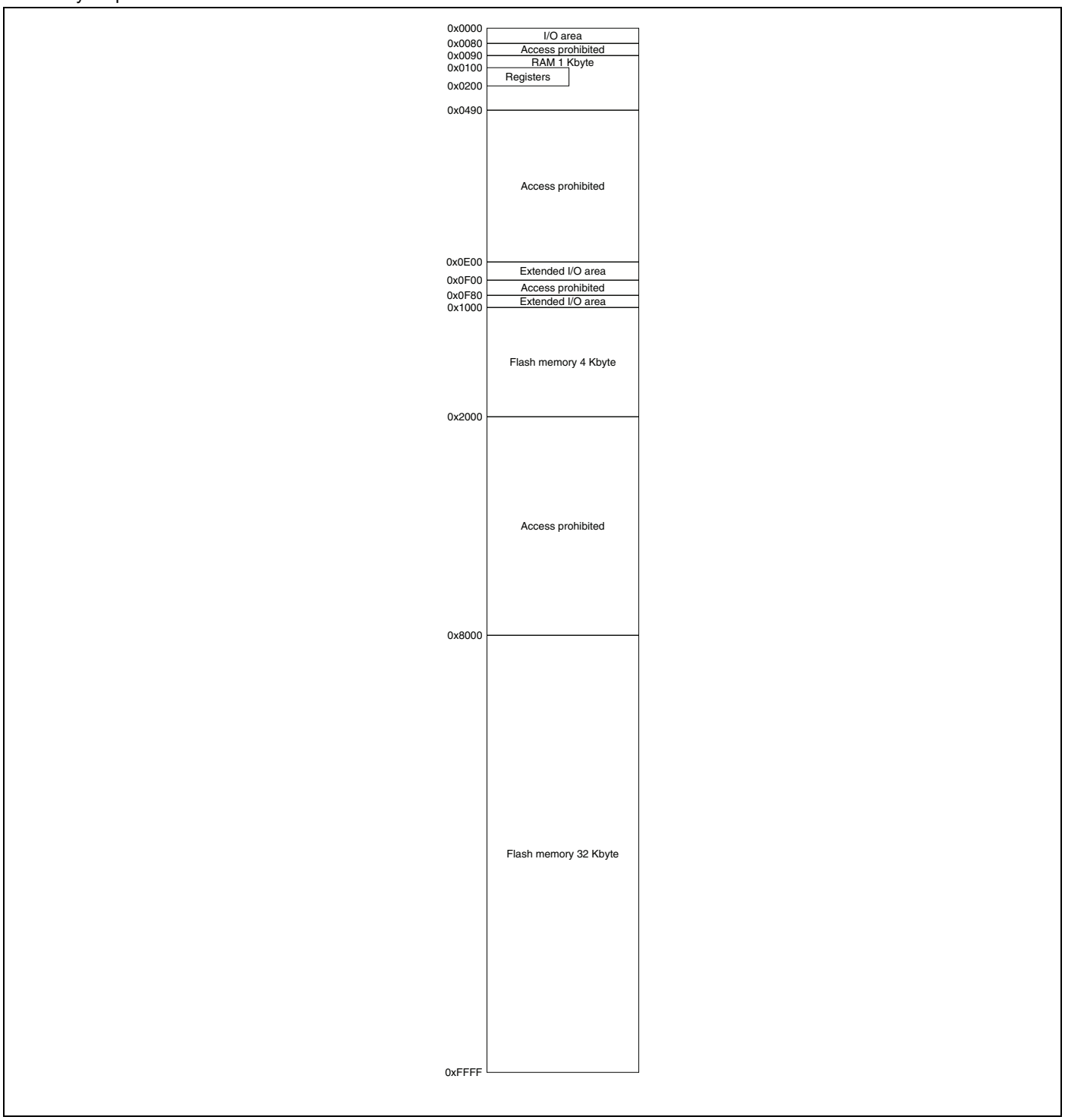
In serial communication, reception of wrong data may occur due to noise or other causes. Therefore, design a printed circuit board to prevent noise from occurring. Taking account of the reception of wrong data, take measures such as adding a checksum to the end of data in order to detect errors. If an error is detected, retransmit the data.

10. CPU Core

■ Memory space

The memory space of the MB95850K/860K/870K Series is 64 Kbyte in size, and consists of an I/O area, an extended I/O area, a data area, and a program area. The memory space includes areas intended for specific purposes such as general-purpose registers and a vector table. The memory maps of the MB95850K/860K/870K Series are shown below.

■ Memory maps

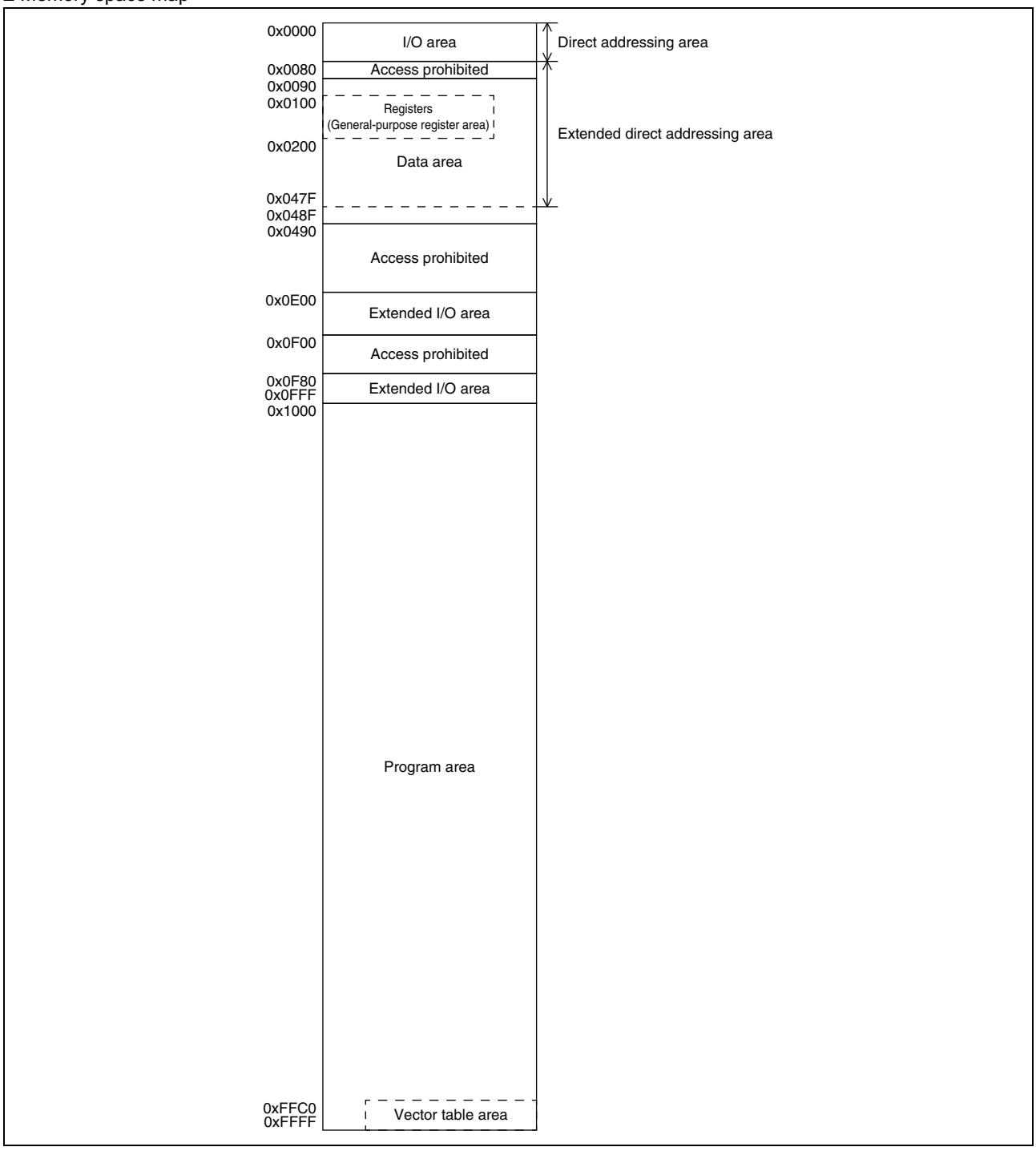


11. Memory Space

The memory space of the MB95850K/860K/870K Series is 64 Kbyte in size, and consists of an I/O area, an extended I/O area, a data area, and a program area. The memory space includes areas for specific applications such as general-purpose registers and a vector table.

- I/O area (addresses: 0x0000 to 0x007F)
  - This area contains the control registers and data registers for built-in peripheral functions.
  - As the I/O area forms part of the memory space, it can be accessed in the same way as the memory. It can also be accessed at high-speed by using direct addressing instructions.
- Extended I/O area (addresses: 0x0E00 to 0x0EFF and 0x0F80 to 0x0FFF)
  - This area contains the control registers and data registers for built-in peripheral functions.
  - As the extended I/O area forms part of the memory space, it can be accessed in the same way as the memory.
- Data area
  - Static RAM is incorporated in the data area as the internal data area.
  - The internal RAM size varies according to product.
  - The RAM area from 0x0090 to 0x00FF can be accessed at high-speed by using direct addressing instructions.
  - The area from 0x0090 to 0x047F is an extended direct addressing area. It can be accessed at high-speed by direct addressing instructions with a direct bank pointer set.
  - The area from 0x0100 to 0x01FF can be used as a general-purpose register area.
- Program area
  - The Flash memory is incorporated in the program area as the internal program area.
  - The Flash memory size varies according to product.
  - The area from 0xFFC0 to 0xFFFF is used as the vector table.
  - The area from 0xFFBB to 0xFFBF is used to store data of the non-volatile register.

■ Memory space map



12. Areas for Specific Applications

The general-purpose register area and vector table area are used for the specific applications.

- General-purpose register area (Addresses: 0x0100 to 0x01FF)
  - This area contains the auxiliary registers used for 8-bit arithmetic operations, transfer, etc.
  - As this area forms part of the RAM area, it can also be used as conventional RAM.
  - When the area is used as general-purpose registers, general-purpose register addressing enables high-speed access with short instructions.
- Non-volatile register data area (Addresses: 0xFFBB to 0xFFBF)
  - The area from 0xFFBB to 0xFFBF is used to store data of the non-volatile register. For details, refer to “CHAPTER 24 NON-VOLATILE REGISTER (NVR) INTERFACE” in “New 8FX MB95850K/860K/870K Series Hardware Manual”.
- Vector table area (Addresses: 0xFFC0 to 0xFFFF)
  - This area is used as the vector table for vector call instructions (CALLV), interrupts, and resets.
  - The top of the Flash memory area is allocated to the vector table area. The start address of a service routine is set to an address in the vector table in the form of data.

Interrupt Source Tables on page 125, MB95860K Series on page 126 and MB95870K Series on page 127 list the vector table addresses corresponding to vector call instructions, interrupts, and resets.

For details, refer to “CHAPTER 4 RESET”, “CHAPTER 5 INTERRUPTS” and “A.2 Special Instruction ■ Special Instruction ● CALLV #vct” in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

- Direct bank pointer and access area

Direct bank pointer (DP[2:0])	Operand-specified dir	Access area
0bXXX (It does not affect mapping.)	0x0000 to 0x007F	0x0000 to 0x007F
0b000 (Initial value)	0x0090 to 0x00FF	0x0090 to 0x00FF
0b001	0x0080 to 0x00FF	0x0100 to 0x017F
0b010		0x0180 to 0x01FF
0b011		0x0200 to 0x027F
0b100		0x0280 to 0x02FF
0b101		0x0300 to 0x037F
0b110		0x0380 to 0x03FF
0b111		0x0400 to 0x047F

13. I/O Maps

13.1 MB95850K Series

Address	Register abbreviation	Register name	R/W	Initial value
0x0000	PDR0	Port 0 data register	R/W	0b00000000
0x0001	DDR0	Port 0 direction register	R/W	0b00000000
0x0002	PDR1	Port 1 data register	R/W	0b00000000
0x0003	DDR1	Port 1 direction register	R/W	0b00000000
0x0004	—	(Disabled)	—	—
0x0005	WATR	Oscillation stabilization wait time setting register	R/W	0b11111111
0x0006	PLLC	PLL control register	R/W	0b000X0000
0x0007	SYCC	System clock control register	R/W	0bXXX11011
0x0008	STBC	Standby control register	R/W	0b00000000
0x0009	RSRR	Reset source register	R/W	0b000XXXXX
0x000A	TBTC	Time-base timer control register	R/W	0b00000000
0x000B	WPCR	Watch prescaler control register	R/W	0b00000000
0x000C	WDTC	Watchdog timer control register	R/W	0b00XX0000
0x000D	SYCC2	System clock control register 2	R/W	0bXXXX0011
0x000E to 0x0011	—	(Disabled)	—	—
0x0012	PDR4	Port 4 data register	R/W	0b00000000
0x0013	DDR4	Port 4 direction register	R/W	0b00000000
0x0014, 0x0015	—	(Disabled)	—	—
0x0016	PDR6	Port 6 data register	R/W	0b00000000
0x0017	DDR6	Port 6 direction register	R/W	0b00000000
0x0018	PDR7	Port 7 data register	R/W	0b00000000
0x0019	DDR7	Port 7 direction register	R/W	0b00000000
0x001A, 0x001B	—	(Disabled)	—	—
0x001C	STBC2	Standby control register 2	R/W	0b00000000
0x001D to 0x0027	—	(Disabled)	—	—
0x0028	PDRF	Port F data register	R/W	0b00000000
0x0029	DDRF	Port F direction register	R/W	0b00000000
0x002A	PDRG	Port G data register	R/W	0b00000000
0x002B	DDRG	Port G direction register	R/W	0b00000000
0x002C	PUL0	Port 0 pull-up register	R/W	0b00000000
0x002D	PUL1	Port 1 pull-up register	R/W	0b00000000
0x002E to 0x0031	—	(Disabled)	—	—
0x0032	PUL7	Port 7 pull-up register	R/W	0b00000000
0x0033	PUL6	Port 6 pull-up register	R/W	0b00000000
0x0034	—	(Disabled)	—	—
0x0035	PULG	Port G pull-up register	R/W	0b00000000
0x0036	T01CR1	8/16-bit composite timer 01 status control register 1	R/W	0b00000000
0x0037	T00CR1	8/16-bit composite timer 00 status control register 1	R/W	0b00000000
0x0038, 0x0039	—	(Disabled)	—	—

Address	Register abbreviation	Register name	R/W	Initial value
0x003A	PC01	8/16-bit PPG timer 01 control register	R/W	0b00000000
0x003B	PC00	8/16-bit PPG timer 00 control register	R/W	0b00000000
0x003C to 0x0047	—	(Disabled)	—	—
0x0048	EIC00	External interrupt circuit control register ch. 0/ch. 1	R/W	0b00000000
0x0049	—	(Disabled)	—	—
0x004A	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	0b00000000
0x004B	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	0b00000000
0x004C, 0x004D	—	(Disabled)	—	—
0x004E	LVDR	LVD reset voltage selection ID register	R/W	0b00000000
0x004F	LVDCC	LVD reset circuit control register	R/W	0b00000001
0x0050 to 0x0055	—	(Disabled)	—	—
0x0056	SMC10	UART/SIO serial mode control register 1 ch. 0	R/W	0b00000000
0x0057	SMC20	UART/SIO serial mode control register 2 ch. 0	R/W	0b00100000
0x0058	SSR0	UART/SIO serial status and data register ch. 0	R/W	0b00000001
0x0059	TDR0	UART/SIO serial output data register ch. 0	R/W	0b00000000
0x005A	RDR0	UART/SIO serial input data register ch. 0	R	0b00000000
0x005B	CMR0	Comparator control register ch. 0	R/W	0b11000101
0x005C to 0x005F	—	(Disabled)	—	—
0x0060	IBCR00	I^2C bus control register 0 ch. 0	R/W	0b00000000
0x0061	IBCR10	I^2C bus control register 1 ch. 0	R/W	0b00000000
0x0062	IBSR0	I^2C bus status register ch. 0	R/W	0b00000000
0x0063	IDDR0	I^2C data register ch. 0	R/W	0b00000000
0x0064	IAAR0	I^2C address register ch. 0	R/W	0b00000000
0x0065	ICCR0	I^2C clock control register ch. 0	R/W	0b00000000
0x0066 to 0x006B	—	(Disabled)	—	—
0x006C	ADC1	8/10-bit A/D converter control register 1	R/W	0b00000000
0x006D	ADC2	8/10-bit A/D converter control register 2	R/W	0b00000000
0x006E	ADDH	8/10-bit A/D converter data register (upper)	R/W	0b00000000
0x006F	ADDL	8/10-bit A/D converter data register (lower)	R/W	0b00000000
0x0070	WCSR	Watch counter control register	R/W	0b00000000
0x0071	FSR2	Flash memory status register 2	R/W	0b00000000
0x0072	FSR	Flash memory status register	R/W	0b000X0000
0x0073	SWRE0	Flash memory sector write control register 0	R/W	0b00000000
0x0074	FSR3	Flash memory status register 3	R	0b000XXXXX
0x0075	FSR4	Flash memory status register 4	R/W	0b00000000
0x0076	WREN	Wild register address compare enable register	R/W	0b00000000
0x0077	WROR	Wild register data test setting register	R/W	0b00000000
0x0078	—	Mirror of register bank pointer (RP) and direct bank pointer (DP)	—	—
0x0079	ILR0	Interrupt level setting register 0	R/W	0b11111111
0x007A	ILR1	Interrupt level setting register 1	R/W	0b11111111
0x007B	ILR2	Interrupt level setting register 2	R/W	0b11111111

Address	Register abbreviation	Register name	R/W	Initial value
0x007C	ILR3	Interrupt level setting register 3	R/W	0b11111111
0x007D	ILR4	Interrupt level setting register 4	R/W	0b11111111
0x007E	ILR5	Interrupt level setting register 5	R/W	0b11111111
0x007F	—	(Disabled)	—	—
0x0E10	BPFREQ	Beep output frequency register	R/W	0b00000000
0x0E11	TER0	TS touch channel enable register 0	R/W	0b00000000
0x0E12	TER1	TS touch channel enable register 1	R/W	0b00000000
0x0E13	PSC	TS prescaler control register	R/W	0b00100000
0x0E14	WRESET	TS warm reset register	R/W	0b00000000
0x0E15	RSEL0	TS sensitivity select register 0	R/W	0b00000010
0x0E16	RSEL1	TS sensitivity select register 1	R/W	0b00010010
0x0E17	RSEL2	TS sensitivity select register 2	R/W	0b00010010
0x0E18	RSEL3	TS sensitivity select register 3	R/W	0b00010010
0x0E19 to 0x0E1B	—	(Disabled)	—	—
0x0E1C	BPDUR	TS beep duration setting register	R/W	0b00000000
0x0E1D	DIOR1	TS direct output control register 1	R/W	0b00000000
0x0E1E	DIOR2	TS direct output control register 2	R/W	0b00000000
0x0E1F	DIOR3	TS direct output control register 3	R/W	0b00000000
0x0E20	FTSEL	TS feature select register	R/W	0b00000100
0x0E21	AICWAT	TS AIC wait time setting register	R/W	0b00100111
0x0E22	CALITV	TS calibration interval setting register	R/W	0b00110000
0x0E23	ITGTM	TS integration time setting register	R/W	0b00001111
0x0E24	IDLETM	TS idle time setting register	R/W	0b00001111
0x0E25	CONTROL	TS control register	R/W	0b00000000
0x0E26	INTMR	TS interrupt mask register	R/W	0b00011000
0x0E27	INTCR	TS interrupt clear register	R/W	0b00000000
0x0E28	FLTP	TS filter period setting register	R/W	0b00000000
0x0E29	FLTTH	TS filter threshold setting register	R/W	0b00000000
0x0E2A	REFDLY	TS reference delay setting register	R/W	0b00000000
0x0E2B to 0x0E30	—	(Disabled)	—	—
0x0E31	ALPH1	TS alpha value setting register ch. 1	R/W	0b00001000
0x0E32	ALPH2	TS alpha value setting register ch. 2	R/W	0b00001000
0x0E33	ALPH3	TS alpha value setting register ch. 3	R/W	0b00001000
0x0E34	ALPH4	TS alpha value setting register ch. 4	R/W	0b00001000
0x0E35	ALPH5	TS alpha value setting register ch. 5	R/W	0b00001000
0x0E36 to 0x0E3F	—	(Disabled)	—	—
0x0E40	BETA	TS beta value setting register	R/W	0b00000100
0x0E41 to 0x0E50	—	(Disabled)	—	—
0x0E51	STRTH1	TS touch strength threshold setting register ch. 1	R/W	0b00000001
0x0E52	STRTH2	TS touch strength threshold setting register ch. 2	R/W	0b00000001
0x0E53	STRTH3	TS touch strength threshold setting register ch. 3	R/W	0b00000001

Address	Register abbreviation	Register name	R/W	Initial value
0x0E54	STRTH4	TS touch strength threshold setting register ch. 4	R/W	0b00000001
0x0E55	STRTH5	TS touch strength threshold setting register ch. 5	R/W	0b00000001
0x0E56 to 0x0E60	—	(Disabled)	—	—
0x0E61	STR1	TS touch strength register ch. 1	R	0bXXXXXXXX
0x0E62	STR2	TS touch strength register ch. 2	R	0bXXXXXXXX
0x0E63	STR3	TS touch strength register ch. 3	R	0bXXXXXXXX
0x0E64	STR4	TS touch strength register ch. 4	R	0bXXXXXXXX
0x0E65	STR5	TS touch strength register ch. 5	R	0bXXXXXXXX
0x0E66 to 0x0E70	—	(Disabled)	—	—
0x0E71	CALIP1	TS calibrated impedance register ch. 1	R	0b0XXXXXXX
0x0E72	CALIP2	TS calibrated impedance register ch. 2	R	0b0XXXXXXX
0x0E73	CALIP3	TS calibrated impedance register ch. 3	R	0b0XXXXXXX
0x0E74	CALIP4	TS calibrated impedance register ch. 4	R	0b0XXXXXXX
0x0E75	CALIP5	TS calibrated impedance register ch. 5	R	0b0XXXXXXX
0x0E76 to 0x0E80	—	(Disabled)	—	—
0x0E81	IMPE1	TS impedance register ch. 1	R	0b0XXXXXXX
0x0E82	IMPE2	TS impedance register ch. 2	R	0b0XXXXXXX
0x0E83	IMPE3	TS impedance register ch. 3	R	0b0XXXXXXX
0x0E84	IMPE4	TS impedance register ch. 4	R	0b0XXXXXXX
0x0E85	IMPE5	TS impedance register ch. 5	R	0b0XXXXXXX
0x0E86 to 0x0E8F	—	(Disabled)	—	—
0x0E90	TOUCHL	TS touch data register (lower)	R	0bXXXXXXXX
0x0E91	TOUCHH	TS touch data register (upper)	R	0b0000XXXX
0x0E92	INTPR	TS interrupt pending register	R	0b000XXXXX
0x0E93 to 0x0F7F	—	(Disabled)	—	—
0x0F80	WRARH0	Wild register address setting register (upper) ch. 0	R/W	0b00000000
0x0F81	WRARL0	Wild register address setting register (lower) ch. 0	R/W	0b00000000
0x0F82	WRDR0	Wild register data setting register ch. 0	R/W	0b00000000
0x0F83	WRARH1	Wild register address setting register (upper) ch. 1	R/W	0b00000000
0x0F84	WRARL1	Wild register address setting register (lower) ch. 1	R/W	0b00000000
0x0F85	WRDR1	Wild register data setting register ch. 1	R/W	0b00000000
0x0F86	WRARH2	Wild register address setting register (upper) ch. 2	R/W	0b00000000
0x0F87	WRARL2	Wild register address setting register (lower) ch. 2	R/W	0b00000000
0x0F88	WRDR2	Wild register data setting register ch. 2	R/W	0b00000000
0x0F89 to 0x0F91	—	(Disabled)	—	—
0x0F92	T01CR0	8/16-bit composite timer 01 status control register 0	R/W	0b00000000
0x0F93	T00CR0	8/16-bit composite timer 00 status control register 0	R/W	0b00000000
0x0F94	T01DR	8/16-bit composite timer 01 data register	R/W	0b00000000
0x0F95	T00DR	8/16-bit composite timer 00 data register	R/W	0b00000000
0x0F96	TMCR0	8/16-bit composite timer 00/01 timer mode control register	R/W	0b00000000
0x0F97 to 0x0F9B	—	(Disabled)	—	—

Address	Register abbreviation	Register name	R/W	Initial value
0x0F9C	PPS01	8/16-bit PPG01 cycle setting buffer register	R/W	0b11111111
0x0F9D	PPS00	8/16-bit PPG00 cycle setting buffer register	R/W	0b11111111
0x0F9E	PDS01	8/16-bit PPG01 duty setting buffer register	R/W	0b11111111
0x0F9F	PDS00	8/16-bit PPG00 duty setting buffer register	R/W	0b11111111
0x0FA0 to 0x0FA3	—	(Disabled)	—	—
0x0FA4	PPGS	8/16-bit PPG start register	R/W	0b00000000
0x0FA5	REVC	8/16-bit PPG output inversion register	R/W	0b00000000
0x0FA6 to 0x0FBD	—	(Disabled)	—	—
0x0FBE	PSSR0	UART/SIO dedicated baud rate generator prescaler select register ch. 0	R/W	0b00000000
0x0FBF	BRSR0	UART/SIO dedicated baud rate generator baud rate setting register ch. 0	R/W	0b00000000
0x0FC0	TIDR0	Touch input disable register 0	R/W	0b00000000
0x0FC1	TIDR1	Touch input disable register 1	R/W	0b00000000
0x0FC2	—	(Disabled)	—	—
0x0FC3	AIDRL	A/D input disable register (lower)	R/W	0b00000000
0x0FC4	LVDPW	LVD reset circuit password register	R/W	0b00000000
0x0FC5 to 0x0FE2	—	(Disabled)	—	—
0x0FE3	WCDR	Watch counter data register	R/W	0b00111111
0x0FE4	CRTH	Main CR clock trimming register (upper)	R/W	0b000XXXXX
0x0FE5	CRTL	Main CR clock trimming register (lower)	R/W	0b000XXXXX
0x0FE6	—	(Disabled)	—	—
0x0FE7	CRTDA	Main CR clock temperature dependent adjustment register	R/W	0b000XXXXX
0x0FE8	SYSC	System configuration register	R/W	0b11000011
0x0FE9	CMCR	Clock monitoring control register	R/W	0b00000000
0x0FEA	CMDR	Clock monitoring data register	R	0b00000000
0x0FEB	WDTH	Watchdog timer selection ID register (upper)	R	0bXXXXXXXX
0x0FEC	WDTL	Watchdog timer selection ID register (lower)	R	0bXXXXXXXX
0x0FED, 0x0FEE	—	(Disabled)	—	—
0x0FEF	WICR	Interrupt pin selection circuit control register	R/W	0b01000000
0x0FF0 to 0x0FFF	—	(Disabled)	—	—

■ R/W access symbols
R/W : Readable/Writable
R : Read only

■ Initial value symbols
0 : The initial value of this bit is “0”.
1 : The initial value of this bit is “1”.
X : The initial value of this bit is undefined.

Note: Do not write to an address that is “(Disabled)”. If a “(Disabled)” address is read, an indeterminate value is returned.

13.2 MB95860K Series

Address	Register abbreviation	Register name	R/W	Initial value
0x0000	PDR0	Port 0 data register	R/W	0b00000000
0x0001	DDR0	Port 0 direction register	R/W	0b00000000
0x0002	PDR1	Port 1 data register	R/W	0b00000000
0x0003	DDR1	Port 1 direction register	R/W	0b00000000
0x0004	—	(Disabled)	—	—
0x0005	WATR	Oscillation stabilization wait time setting register	R/W	0b11111111
0x0006	PLLC	PLL control register	R/W	0b000X0000
0x0007	SYCC	System clock control register	R/W	0bXXX11011
0x0008	STBC	Standby control register	R/W	0b00000000
0x0009	RSRR	Reset source register	R/W	0b000XXXXX
0x000A	TBTC	Time-base timer control register	R/W	0b00000000
0x000B	WPCR	Watch prescaler control register	R/W	0b00000000
0x000C	WDTC	Watchdog timer control register	R/W	0b00XX0000
0x000D	SYCC2	System clock control register 2	R/W	0bXXXX0011
0x000E to 0x0011	—	(Disabled)	—	—
0x0012	PDR4	Port 4 data register	R/W	0b00000000
0x0013	DDR4	Port 4 direction register	R/W	0b00000000
0x0014, 0x0015	—	(Disabled)	—	—
0x0016	PDR6	Port 6 data register	R/W	0b00000000
0x0017	DDR6	Port 6 direction register	R/W	0b00000000
0x0018	PDR7	Port 7 data register	R/W	0b00000000
0x0019	DDR7	Port 7 direction register	R/W	0b00000000
0x001A, 0x001B	—	(Disabled)	—	—
0x001C	STBC2	Standby control register 2	R/W	0b00000000
0x001D to 0x0027	—	(Disabled)	—	—
0x0028	PDRF	Port F data register	R/W	0b00000000
0x0029	DDRF	Port F direction register	R/W	0b00000000
0x002A	PDRG	Port G data register	R/W	0b00000000
0x002B	DDRG	Port G direction register	R/W	0b00000000
0x002C	PUL0	Port 0 pull-up register	R/W	0b00000000
0x002D	PUL1	Port 1 pull-up register	R/W	0b00000000
0x002E, 0x002F	—	(Disabled)	—	—
0x0030	PUL4	Port 4 pull-up register	R/W	0b00000000
0x0031	—	(Disabled)	—	—
0x0032	PUL7	Port 7 pull-up register	R/W	0b00000000
0x0033	PUL6	Port 6 pull-up register	R/W	0b00000000
0x0034	—	(Disabled)	—	—
0x0035	PULG	Port G pull-up register	R/W	0b00000000
0x0036	T01CR1	8/16-bit composite timer 01 status control register 1	R/W	0b00000000

Address	Register abbreviation	Register name	R/W	Initial value
0x0037	T00CR1	8/16-bit composite timer 00 status control register 1	R/W	0b00000000
0x0038	T11CR1	8/16-bit composite timer 11 status control register 1	R/W	0b00000000
0x0039	T10CR1	8/16-bit composite timer 10 status control register 1	R/W	0b00000000
0x003A	PC01	8/16-bit PPG timer 01 control register	R/W	0b00000000
0x003B	PC00	8/16-bit PPG timer 00 control register	R/W	0b00000000
0x003C	PC11	8/16-bit PPG timer 11 control register	R/W	0b00000000
0x003D	PC10	8/16-bit PPG timer 10 control register	R/W	0b00000000
0x003E to 0x0047	—	(Disabled)	—	—
0x0048	EIC00	External interrupt circuit control register ch. 0/ch. 1	R/W	0b00000000
0x0049	EIC10	External interrupt circuit control register ch. 2/ch. 3	R/W	0b00000000
0x004A	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	0b00000000
0x004B	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	0b00000000
0x004C, 0x004D	—	(Disabled)	—	—
0x004E	LVDR	LVD reset voltage selection ID register	R/W	0b00000000
0x004F	LVDCC	LVD reset circuit control register	R/W	0b00000001
0x0050 to 0x0055	—	(Disabled)	—	—
0x0056	SMC10	UART/SIO serial mode control register 1 ch. 0	R/W	0b00000000
0x0057	SMC20	UART/SIO serial mode control register 2 ch. 0	R/W	0b00100000
0x0058	SSR0	UART/SIO serial status and data register ch. 0	R/W	0b00000001
0x0059	TDR0	UART/SIO serial output data register ch. 0	R/W	0b00000000
0x005A	RDR0	UART/SIO serial input data register ch. 0	R	0b00000000
0x005B	CMR0	Comparator control register ch. 0	R/W	0b11000101
0x005C to 0x005F	—	(Disabled)	—	—
0x0060	IBCR00	I^2C bus control register 0 ch. 0	R/W	0b00000000
0x0061	IBCR10	I^2C bus control register 1 ch. 0	R/W	0b00000000
0x0062	IBSR0	I^2C bus status register ch. 0	R/W	0b00000000
0x0063	IDDR0	I^2C data register ch. 0	R/W	0b00000000
0x0064	IAAR0	I^2C address register ch. 0	R/W	0b00000000
0x0065	ICCR0	I^2C clock control register ch. 0	R/W	0b00000000
0x0066 to 0x006B	—	(Disabled)	—	—
0x006C	ADC1	8/10-bit A/D converter control register 1	R/W	0b00000000
0x006D	ADC2	8/10-bit A/D converter control register 2	R/W	0b00000000
0x006E	ADDH	8/10-bit A/D converter data register (upper)	R/W	0b00000000
0x006F	ADDL	8/10-bit A/D converter data register (lower)	R/W	0b00000000
0x0070	WCSR	Watch counter control register	R/W	0b00000000
0x0071	FSR2	Flash memory status register 2	R/W	0b00000000
0x0072	FSR	Flash memory status register	R/W	0b000X0000
0x0073	SWRE0	Flash memory sector write control register 0	R/W	0b00000000
0x0074	FSR3	Flash memory status register 3	R	0b000XXXXX
0x0075	FSR4	Flash memory status register 4	R/W	0b00000000

Address	Register abbreviation	Register name	R/W	Initial value
0x0076	WREN	Wild register address compare enable register	R/W	0b00000000
0x0077	WROR	Wild register data test setting register	R/W	0b00000000
0x0078	—	Mirror of register bank pointer (RP) and direct bank pointer (DP)	—	—
0x0079	ILR0	Interrupt level setting register 0	R/W	0b11111111
0x007A	ILR1	Interrupt level setting register 1	R/W	0b11111111
0x007B	ILR2	Interrupt level setting register 2	R/W	0b11111111
0x007C	ILR3	Interrupt level setting register 3	R/W	0b11111111
0x007D	ILR4	Interrupt level setting register 4	R/W	0b11111111
0x007E	ILR5	Interrupt level setting register 5	R/W	0b11111111
0x007F	—	(Disabled)	—	—
0x0E10	BPFREQ	Beep output frequency register	R/W	0b00000000
0x0E11	TER0	TS touch channel enable register 0	R/W	0b00000000
0x0E12	TER1	TS touch channel enable register 1	R/W	0b00000000
0x0E13	PSC	TS prescaler control register	R/W	0b00100000
0x0E14	WRESET	TS warm reset register	R/W	0b00000000
0x0E15	RSEL0	TS sensitivity select register 0	R/W	0b00000010
0x0E16	RSEL1	TS sensitivity select register 1	R/W	0b00010010
0x0E17	RSEL2	TS sensitivity select register 2	R/W	0b00010010
0x0E18	RSEL3	TS sensitivity select register 3	R/W	0b00010010
0x0E19	RSEL4	TS sensitivity select register 4	R/W	0b00010010
0x0E1A, 0x0E1B	—	(Disabled)	—	—
0x0E1C	BPDUR	TS beep duration setting register	R/W	0b00000000
0x0E1D	DIOR1	TS direct output control register 1	R/W	0b00000000
0x0E1E	DIOR2	TS direct output control register 2	R/W	0b00000000
0x0E1F	DIOR3	TS direct output control register 3	R/W	0b00000000
0x0E20	FTSEL	TS feature select register	R/W	0b00000100
0x0E21	AICWAT	TS AIC wait time setting register	R/W	0b00100111
0x0E22	CALITV	TS calibration interval setting register	R/W	0b00110000
0x0E23	ITGTM	TS integration time setting register	R/W	0b00001111
0x0E24	IDLETM	TS idle time setting register	R/W	0b00001111
0x0E25	CONTROL	TS control register	R/W	0b00000000
0x0E26	INTMR	TS interrupt mask register	R/W	0b00011000
0x0E27	INTCR	TS interrupt clear register	R/W	0b00000000
0x0E28	FLTP	TS filter period setting register	R/W	0b00000000
0x0E29	FLTTH	TS filter threshold setting register	R/W	0b00000000
0x0E2A	REFDLY	TS reference delay setting register	R/W	0b00000000
0x0E2B to 0x0E2F	—	(Disabled)	—	—
0x0E30	ALPH0	TS alpha value setting register ch. 0	R/W	0b00001000
0x0E31	ALPH1	TS alpha value setting register ch. 1	R/W	0b00001000
0x0E32	ALPH2	TS alpha value setting register ch. 2	R/W	0b00001000

Address	Register abbreviation	Register name	R/W	Initial value
0x0E33	ALPH3	TS alpha value setting register ch. 3	R/W	0b00001000
0x0E34	ALPH4	TS alpha value setting register ch. 4	R/W	0b00001000
0x0E35	ALPH5	TS alpha value setting register ch. 5	R/W	0b00001000
0x0E36	ALPH6	TS alpha value setting register ch. 6	R/W	0b00001000
0x0E37	ALPH7	TS alpha value setting register ch. 7	R/W	0b00001000
0x0E38 to 0x0E3F	—	(Disabled)	—	—
0x0E40	BETA	TS beta value setting register	R/W	0b00000100
0x0E41 to 0x0E4F	—	(Disabled)	—	—
0x0E50	STRTH0	TS touch strength threshold setting register ch. 0	R/W	0b00000001
0x0E51	STRTH1	TS touch strength threshold setting register ch. 1	R/W	0b00000001
0x0E52	STRTH2	TS touch strength threshold setting register ch. 2	R/W	0b00000001
0x0E53	STRTH3	TS touch strength threshold setting register ch. 3	R/W	0b00000001
0x0E54	STRTH4	TS touch strength threshold setting register ch. 4	R/W	0b00000001
0x0E55	STRTH5	TS touch strength threshold setting register ch. 5	R/W	0b00000001
0x0E56	STRTH6	TS touch strength threshold setting register ch. 6	R/W	0b00000001
0x0E57	STRTH7	TS touch strength threshold setting register ch. 7	R/W	0b00000001
0x0E58 to 0x0E5F	—	(Disabled)	—	—
0x0E60	STR0	TS touch strength register ch. 0	R	0bXXXXXXXX
0x0E61	STR1	TS touch strength register ch. 1	R	0bXXXXXXXX
0x0E62	STR2	TS touch strength register ch. 2	R	0bXXXXXXXX
0x0E63	STR3	TS touch strength register ch. 3	R	0bXXXXXXXX
0x0E64	STR4	TS touch strength register ch. 4	R	0bXXXXXXXX
0x0E65	STR5	TS touch strength register ch. 5	R	0bXXXXXXXX
0x0E66	STR6	TS touch strength register ch. 6	R	0bXXXXXXXX
0x0E67	STR7	TS touch strength register ch. 7	R	0bXXXXXXXX
0x0E68 to 0x0E6F	—	(Disabled)	—	—
0x0E70	CALIP0	TS calibrated impedance register ch. 0	R	0b0XXXXXXX
0x0E71	CALIP1	TS calibrated impedance register ch. 1	R	0b0XXXXXXX
0x0E72	CALIP2	TS calibrated impedance register ch. 2	R	0b0XXXXXXX
0x0E73	CALIP3	TS calibrated impedance register ch. 3	R	0b0XXXXXXX
0x0E74	CALIP4	TS calibrated impedance register ch. 4	R	0b0XXXXXXX
0x0E75	CALIP5	TS calibrated impedance register ch. 5	R	0b0XXXXXXX
0x0E76	CALIP6	TS calibrated impedance register ch. 6	R	0b0XXXXXXX
0x0E77	CALIP7	TS calibrated impedance register ch. 7	R	0b0XXXXXXX
0x0E78 to 0x0E7F	—	(Disabled)	—	—
0x0E80	IMPE0	TS impedance register ch. 0	R	0b0XXXXXXX
0x0E81	IMPE1	TS impedance register ch. 1	R	0b0XXXXXXX
0x0E82	IMPE2	TS impedance register ch. 2	R	0b0XXXXXXX
0x0F80	WRARH0	Wild register address setting register (upper) ch. 0	R/W	0b00000000
0x0F81	WRARL0	Wild register address setting register (lower) ch. 0	R/W	0b00000000

Address	Register abbreviation	Register name	R/W	Initial value
0x0F82	WRDR0	Wild register data setting register ch. 0	R/W	0b00000000
0x0F83	WRARH1	Wild register address setting register (upper) ch. 1	R/W	0b00000000
0x0F84	WRARL1	Wild register address setting register (lower) ch. 1	R/W	0b00000000
0x0F85	WRDR1	Wild register data setting register ch. 1	R/W	0b00000000
0x0F86	WRARH2	Wild register address setting register (upper) ch. 2	R/W	0b00000000
0x0F87	WRARL2	Wild register address setting register (lower) ch. 2	R/W	0b00000000
0x0F88	WRDR2	Wild register data setting register ch. 2	R/W	0b00000000
0x0F89 to 0x0F91	—	(Disabled)	—	—
0x0F92	T01CR0	8/16-bit composite timer 01 status control register 0	R/W	0b00000000
0x0F93	T00CR0	8/16-bit composite timer 00 status control register 0	R/W	0b00000000
0x0F94	T01DR	8/16-bit composite timer 01 data register	R/W	0b00000000
0x0F95	T00DR	8/16-bit composite timer 00 data register	R/W	0b00000000
0x0F96	TMCR0	8/16-bit composite timer 00/01 timer mode control register	R/W	0b00000000
0x0F97	T11CR0	8/16-bit composite timer 11 status control register 0	R/W	0b00000000
0x0F98	T10CR0	8/16-bit composite timer 10 status control register 0	R/W	0b00000000
0x0F99	T11DR	8/16-bit composite timer 11 data register	R/W	0b00000000
0x0F9A	T10DR	8/16-bit composite timer 10 data register	R/W	0b00000000
0x0F9B	TMCR1	8/16-bit composite timer 10/11 timer mode control register	R/W	0b00000000
0x0F9C	PPS01	8/16-bit PPG01 cycle setting buffer register	R/W	0b11111111
0x0F9D	PPS00	8/16-bit PPG00 cycle setting buffer register	R/W	0b11111111
0x0F9E	PDS01	8/16-bit PPG01 duty setting buffer register	R/W	0b11111111
0x0F9F	PDS00	8/16-bit PPG00 duty setting buffer register	R/W	0b11111111
0x0FA0	PPS11	8/16-bit PPG11 cycle setting buffer register	R/W	0b11111111
0x0FA1	PPS10	8/16-bit PPG10 cycle setting buffer register	R/W	0b11111111
0x0FA2	PDS11	8/16-bit PPG11 duty setting buffer register	R/W	0b11111111
0x0FA3	PDS10	8/16-bit PPG10 duty setting buffer register	R/W	0b11111111
0x0FA4	PPGS	8/16-bit PPG start register	R/W	0b00000000
0x0FA5	REVC	8/16-bit PPG output inversion register	R/W	0b00000000
0x0FA6 to 0x0FBD	—	(Disabled)	—	—
0x0FBE	PSSR0	UART/SIO dedicated baud rate generator prescaler select register ch. 0	R/W	0b00000000
0x0FBF	BRSR0	UART/SIO dedicated baud rate generator baud rate setting register ch. 0	R/W	0b00000000
0x0FC0	TIDR0	Touch input disable register 0	R/W	0b00000000
0x0FC1	TIDR1	Touch input disable register 1	R/W	0b00000000
0x0FC2	—	(Disabled)	—	—
0x0FC3	AIDRL	A/D input disable register (lower)	R/W	0b00000000
0x0FC4	LVDPW	LVD reset circuit password register	R/W	0b00000000
0x0FC5 to 0x0FE2	—	(Disabled)	—	—
0x0FE3	WCDR	Watch counter data register	R/W	0b00111111
0x0FE4	CRTH	Main CR clock trimming register (upper)	R/W	0b000XXXXX

Address	Register abbreviation	Register name	R/W	Initial value
0x0FE5	CRTL	Main CR clock trimming register (lower)	R/W	0b000XXXXX
0x0FE6	—	(Disabled)	—	—
0x0FE7	CRTDA	Main CR clock temperature dependent adjustment register	R/W	0b000XXXXX
0x0FE8	SYSC	System configuration register	R/W	0b11000011
0x0FE9	CMCR	Clock monitoring control register	R/W	0b00000000
0x0FEA	CMDR	Clock monitoring data register	R	0b00000000
0x0FEB	WDTH	Watchdog timer selection ID register (upper)	R	0bXXXXXXXX
0x0FEC	WDTL	Watchdog timer selection ID register (lower)	R	0bXXXXXXXX
0x0FED, 0x0FEE	—	(Disabled)	—	—
0x0FEF	WICR	Interrupt pin selection circuit control register	R/W	0b01000000
0x0FF0 to 0x0FFF	—	(Disabled)	—	—

■ R/W access symbols
R/W : Readable/Writable
R : Read only

■ Initial value symbols
0 : The initial value of this bit is “0”.
1 : The initial value of this bit is “1”.
X : The initial value of this bit is undefined.

Note: Do not write to an address that is “(Disabled)”. If a “(Disabled)” address is read, an indeterminate value is returned.

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Address	Register abbreviation	Register name	R/W	Initial value
0x0000	PDR0	Port 0 data register	R/W	0b00000000
0x0001	DDR0	Port 0 direction register	R/W	0b00000000
0x0002	PDR1	Port 1 data register	R/W	0b00000000
0x0003	DDR1	Port 1 direction register	R/W	0b00000000
0x0004	—	(Disabled)	—	—
0x0005	WATR	Oscillation stabilization wait time setting register	R/W	0b11111111
0x0006	PLLC	PLL control register	R/W	0b000X0000
0x0007	SYCC	System clock control register	R/W	0bXXX11011
0x0008	STBC	Standby control register	R/W	0b00000000
0x0009	RSRR	Reset source register	R/W	0b000XXXXX
0x000A	TBTC	Time-base timer control register	R/W	0b00000000
0x000B	WPCR	Watch prescaler control register	R/W	0b00000000
0x000C	WDTC	Watchdog timer control register	R/W	0b00XX0000
0x000D	SYCC2	System clock control register 2	R/W	0bXXXX0011
0x000E to 0x0011	—	(Disabled)	—	—
0x0012	PDR4	Port 4 data register	R/W	0b00000000
0x0013	DDR4	Port 4 direction register	R/W	0b00000000
0x0014, 0x0015	—	(Disabled)	—	—
0x0016	PDR6	Port 6 data register	R/W	0b00000000
0x0017	DDR6	Port 6 direction register	R/W	0b00000000
0x0018	PDR7	Port 7 data register	R/W	0b00000000
0x0019	DDR7	Port 7 direction register	R/W	0b00000000
0x001A, 0x001B	—	(Disabled)	—	—
0x001C	STBC2	Standby control register 2	R/W	0b00000000
0x001D to 0x0027	—	(Disabled)	—	—
0x0028	PDRF	Port F data register	R/W	0b00000000
0x0029	DDRF	Port F direction register	R/W	0b00000000
0x002A	PDRG	Port G data register	R/W	0b00000000
0x002B	DDRG	Port G direction register	R/W	0b00000000
0x002C	PUL0	Port 0 pull-up register	R/W	0b00000000
0x002D	PUL1	Port 1 pull-up register	R/W	0b00000000
0x002E, 0x002F	—	(Disabled)	—	—
0x0030	PUL4	Port 4 pull-up register	R/W	0b00000000
0x0031	—	(Disabled)	—	—
0x0032	PUL7	Port 7 pull-up register	R/W	0b00000000
0x0033	PUL6	Port 6 pull-up register	R/W	0b00000000
0x0034	—	(Disabled)	—	—
0x0035	PULG	Port G pull-up register	R/W	0b00000000
0x0036	T01CR1	8/16-bit composite timer 01 status control register 1	R/W	0b00000000

Address	Register abbreviation	Register name	R/W	Initial value
0x0037	T00CR1	8/16-bit composite timer 00 status control register 1	R/W	0b00000000
0x0038	T11CR1	8/16-bit composite timer 11 status control register 1	R/W	0b00000000
0x0039	T10CR1	8/16-bit composite timer 10 status control register 1	R/W	0b00000000
0x003A	PC01	8/16-bit PPG timer 01 control register	R/W	0b00000000
0x003B	PC00	8/16-bit PPG timer 00 control register	R/W	0b00000000
0x003C	PC11	8/16-bit PPG timer 11 control register	R/W	0b00000000
0x003D	PC10	8/16-bit PPG timer 10 control register	R/W	0b00000000
0x003E	PC21	8/16-bit PPG timer 21 control register	R/W	0b00000000
0x003F	PC20	8/16-bit PPG timer 20 control register	R/W	0b00000000
0x0040 to 0x0047	—	(Disabled)	—	—
0x0048	EIC00	External interrupt circuit control register ch. 0/ch. 1	R/W	0b00000000
0x0049	EIC10	External interrupt circuit control register ch. 2/ch. 3	R/W	0b00000000
0x004A	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	0b00000000
0x004B	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	0b00000000
0x004C	EIC01	External interrupt circuit control register ch. 8/ch. 9	R/W	0b00000000
0x004D	—	(Disabled)	—	—
0x004E	LVDR	LVD reset voltage selection ID register	R/W	0b00000000
0x004F	LVDCC	LVD reset circuit control register	R/W	0b00000001
0x0050 to 0x0055	—	(Disabled)	—	—
0x0056	SMC10	UART/SIO serial mode control register 1 ch. 0	R/W	0b00000000
0x0057	SMC20	UART/SIO serial mode control register 2 ch. 0	R/W	0b00100000
0x0058	SSR0	UART/SIO serial status and data register ch. 0	R/W	0b00000001
0x0059	TDR0	UART/SIO serial output data register ch. 0	R/W	0b00000000
0x005A	RDR0	UART/SIO serial input data register ch. 0	R	0b00000000
0x005B	CMR0	Comparator control register ch. 0	R/W	0b11000101
0x005C to 0x005F	—	(Disabled)	—	—
0x0060	IBCR00	I^2C bus control register 0 ch. 0	R/W	0b00000000
0x0061	IBCR10	I^2C bus control register 1 ch. 0	R/W	0b00000000
0x0062	IBSR0	I^2C bus status register ch. 0	R/W	0b00000000
0x0063	IDDR0	I^2C data register ch. 0	R/W	0b00000000
0x0064	IAAR0	I^2C address register ch. 0	R/W	0b00000000
0x0065	ICCR0	I^2C clock control register ch. 0	R/W	0b00000000
0x0066 to 0x006B	—	(Disabled)	—	—
0x006C	ADC1	8/10-bit A/D converter control register 1	R/W	0b00000000
0x006D	ADC2	8/10-bit A/D converter control register 2	R/W	0b00000000
0x006E	ADDH	8/10-bit A/D converter data register (upper)	R/W	0b00000000
0x006F	ADDL	8/10-bit A/D converter data register (lower)	R/W	0b00000000
0x0070	WCSR	Watch counter control register	R/W	0b00000000
0x0071	FSR2	Flash memory status register 2	R/W	0b00000000
0x0072	FSR	Flash memory status register	R/W	0b000X0000

Address	Register abbreviation	Register name	R/W	Initial value
0x0073	SWRE0	Flash memory sector write control register 0	R/W	0b00000000
0x0074	FSR3	Flash memory status register 3	R	0b000XXXXX
0x0075	FSR4	Flash memory status register 4	R/W	0b00000000
0x0076	WREN	Wild register address compare enable register	R/W	0b00000000
0x0077	WROR	Wild register data test setting register	R/W	0b00000000
0x0078	—	Mirror of register bank pointer (RP) and direct bank pointer (DP)	—	—
0x0079	ILR0	Interrupt level setting register 0	R/W	0b11111111
0x007A	ILR1	Interrupt level setting register 1	R/W	0b11111111
0x007B	ILR2	Interrupt level setting register 2	R/W	0b11111111
0x007C	ILR3	Interrupt level setting register 3	R/W	0b11111111
0x007D	ILR4	Interrupt level setting register 4	R/W	0b11111111
0x007E	ILR5	Interrupt level setting register 5	R/W	0b11111111
0x007F	—	(Disabled)	—	—
0x0E10	BPFREQ	Beep output frequency register	R/W	0b00000000
0x0E11	TER0	TS touch channel enable register 0	R/W	0b00000000
0x0E12	TER1	TS touch channel enable register 1	R/W	0b00000000
0x0E13	PSC	TS prescaler control register	R/W	0b00100000
0x0E14	WRESET	TS warm reset register	R/W	0b00000000
0x0E15	RSEL0	TS sensitivity select register 0	R/W	0b00000010
0x0E16	RSEL1	TS sensitivity select register 1	R/W	0b00010010
0x0E17	RSEL2	TS sensitivity select register 2	R/W	0b00010010
0x0E18	RSEL3	TS sensitivity select register 3	R/W	0b00010010
0x0E19	RSEL4	TS sensitivity select register 4	R/W	0b00010010
0x0E1A	RSEL5	TS sensitivity select register 5	R/W	0b00010010
0x0E1B	RSEL6	TS sensitivity select register 6	R/W	0b00010010
0x0E1C	BPDUR	TS beep duration setting register	R/W	0b00000000
0x0E1D	DIOR1	TS direct output control register 1	R/W	0b00000000
0x0E1E	DIOR2	TS direct output control register 2	R/W	0b00000000
0x0E1F	DIOR3	TS direct output control register 3	R/W	0b00000000
0x0E20	FTSEL	TS feature select register	R/W	0b00000100
0x0E21	AICWAT	TS AIC wait time setting register	R/W	0b00100111
0x0E22	CALITV	TS calibration interval setting register	R/W	0b00110000
0x0E23	ITGTM	TS integration time setting register	R/W	0b00001111
0x0E24	IDLETM	TS idle time setting register	R/W	0b00001111
0x0E25	CONTROL	TS control register	R/W	0b00000000
0x0E26	INTMR	TS interrupt mask register	R/W	0b00011000
0x0E27	INTCR	TS interrupt clear register	R/W	0b00000000
0x0E28	FLTP	TS filter period setting register	R/W	0b00000000
0x0E29	FLTTH	TS filter threshold setting register	R/W	0b00000000

Address	Register abbreviation	Register name	R/W	Initial value
0x0E2A	REFDLY	TS reference delay setting register	R/W	0b00000000
0x0E2B to 0x0E2F	—	(Disabled)	—	—
0x0E30	ALPH0	TS alpha value setting register ch. 0	R/W	0b00001000
0x0E31	ALPH1	TS alpha value setting register ch. 1	R/W	0b00001000
0x0E32	ALPH2	TS alpha value setting register ch. 2	R/W	0b00001000
0x0E33	ALPH3	TS alpha value setting register ch. 3	R/W	0b00001000
0x0E34	ALPH4	TS alpha value setting register ch. 4	R/W	0b00001000
0x0E35	ALPH5	TS alpha value setting register ch. 5	R/W	0b00001000
0x0E36	ALPH6	TS alpha value setting register ch. 6	R/W	0b00001000
0x0E37	ALPH7	TS alpha value setting register ch. 7	R/W	0b00001000
0x0E38	ALPH8	TS alpha value setting register ch. 8	R/W	0b00001000
0x0E39	ALPH9	TS alpha value setting register ch. 9	R/W	0b00001000
0x0E3A	ALPH10	TS alpha value setting register ch. 10	R/W	0b00001000
0x0E3B	ALPH11	TS alpha value setting register ch. 11	R/W	0b00001000
0x0E3C to 0x0E3F	—	(Disabled)	—	—
0x0E40	BETA	TS beta value setting register	R/W	0b00000100
0x0E41 to 0x0E4F	—	(Disabled)	—	—
0x0E50	STRTH0	TS touch strength threshold setting register ch. 0	R/W	0b00000001
0x0E51	STRTH1	TS touch strength threshold setting register ch. 1	R/W	0b00000001
0x0E52	STRTH2	TS touch strength threshold setting register ch. 2	R/W	0b00000001
0x0E53	STRTH3	TS touch strength threshold setting register ch. 3	R/W	0b00000001
0x0E54	STRTH4	TS touch strength threshold setting register ch. 4	R/W	0b00000001
0x0E55	STRTH5	TS touch strength threshold setting register ch. 5	R/W	0b00000001
0x0E56	STRTH6	TS touch strength threshold setting register ch. 6	R/W	0b00000001
0x0E57	STRTH7	TS touch strength threshold setting register ch. 7	R/W	0b00000001
0x0E58	STRTH8	TS touch strength threshold setting register ch. 8	R/W	0b00000001
0x0E59	STRTH9	TS touch strength threshold setting register ch. 9	R/W	0b00000001
0x0E5A	STRTH10	TS touch strength threshold setting register ch. 10	R/W	0b00000001
0x0E5B	STRTH11	TS touch strength threshold setting register ch. 11	R/W	0b00000001
0x0E5C to 0x0E5F	—	(Disabled)	—	—
0x0E60	STR0	TS touch strength register ch. 0	R	0bXXXXXXXX
0x0E61	STR1	TS touch strength register ch. 1	R	0bXXXXXXXX
0x0E62	STR2	TS touch strength register ch. 2	R	0bXXXXXXXX
0x0E63	STR3	TS touch strength register ch. 3	R	0bXXXXXXXX
0x0E64	STR4	TS touch strength register ch. 4	R	0bXXXXXXXX
0x0E65	STR5	TS touch strength register ch. 5	R	0bXXXXXXXX
0x0E66	STR6	TS touch strength register ch. 6	R	0bXXXXXXXX
0x0E67	STR7	TS touch strength register ch. 7	R	0bXXXXXXXX
0x0E68	STR8	TS touch strength register ch. 8	R	0bXXXXXXXX
0x0E69	STR9	TS touch strength register ch. 9	R	0bXXXXXXXX

Address	Register abbreviation	Register name	R/W	Initial value
0x0E6A	STR10	TS touch strength register ch. 10	R	0bXXXXXXXX
0x0E6B	STR11	TS touch strength register ch. 11	R	0bXXXXXXXX
0x0E6C to 0x0E6F	—	(Disabled)	—	—
0x0E70	CALIP0	TS calibrated impedance register ch. 0	R	0b0XXXXXXX
0x0E71	CALIP1	TS calibrated impedance register ch. 1	R	0b0XXXXXXX
0x0E72	CALIP2	TS calibrated impedance register ch. 2	R	0b0XXXXXXX
0x0E73	CALIP3	TS calibrated impedance register ch. 3	R	0b0XXXXXXX
0x0E74	CALIP4	TS calibrated impedance register ch. 4	R	0b0XXXXXXX
0x0E75	CALIP5	TS calibrated impedance register ch. 5	R	0b0XXXXXXX
0x0E76	CALIP6	TS calibrated impedance register ch. 6	R	0b0XXXXXXX
0x0E77	CALIP7	TS calibrated impedance register ch. 7	R	0b0XXXXXXX
0x0E78	CALIP8	TS calibrated impedance register ch. 8	R	0b0XXXXXXX
0x0E79	CALIP9	TS calibrated impedance register ch. 9	R	0b0XXXXXXX
0x0E7A	CALIP10	TS calibrated impedance register ch. 10	R	0b0XXXXXXX
0x0E7B	CALIP11	TS calibrated impedance register ch. 11	R	0b0XXXXXXX
0x0E7C to 0x0E7F	—	(Disabled)	—	—
0x0E80	IMPE0	TS impedance register ch. 0	R	0b0XXXXXXX
0x0E81	IMPE1	TS impedance register ch. 1	R	0b0XXXXXXX
0x0E82	IMPE2	TS impedance register ch. 2	R	0b0XXXXXXX
0x0E83	IMPE3	TS impedance register ch. 3	R	0b0XXXXXXX
0x0E84	IMPE4	TS impedance register ch. 4	R	0b0XXXXXXX
0x0E85	IMPE5	TS impedance register ch. 5	R	0b0XXXXXXX
0x0E86	IMPE6	TS impedance register ch. 6	R	0b0XXXXXXX
0x0E87	IMPE7	TS impedance register ch. 7	R	0b0XXXXXXX
0x0E88	IMPE8	TS impedance register ch. 8	R	0b0XXXXXXX
0x0E89	IMPE9	TS impedance register ch. 9	R	0b0XXXXXXX
0x0E8A	IMPE10	TS impedance register ch. 10	R	0b0XXXXXXX
0x0E8B	IMPE11	TS impedance register ch. 11	R	0b0XXXXXXX
0x0E8C to 0x0E8F	—	(Disabled)	—	—
0x0E90	TOUCHL	TS touch data register (lower)	R	0bXXXXXXXX
0x0E91	TOUCHH	TS touch data register (upper)	R	0b0000XXXX
0x0E92	INTPR	TS interrupt pending register	R	0b000XXXXX
0x0E93 to 0x0F7F	—	(Disabled)	—	—
0x0F80	WRARH0	Wild register address setting register (upper) ch. 0	R/W	0b00000000
0x0F81	WRARL0	Wild register address setting register (lower) ch. 0	R/W	0b00000000
0x0F82	WRDR0	Wild register data setting register ch. 0	R/W	0b00000000
0x0F83	WRARH1	Wild register address setting register (upper) ch. 1	R/W	0b00000000
0x0F84	WRARL1	Wild register address setting register (lower) ch. 1	R/W	0b00000000
0x0F85	WRDR1	Wild register data setting register ch. 1	R/W	0b00000000
0x0F86	WRARH2	Wild register address setting register (upper) ch. 2	R/W	0b00000000

Address	Register abbreviation	Register name	R/W	Initial value
0x0F87	WRARL2	Wild register address setting register (lower) ch. 2	R/W	0b00000000
0x0F88	WRDR2	Wild register data setting register ch. 2	R/W	0b00000000
0x0F89 to 0x0F91	—	(Disabled)	—	—
0x0F92	T01CR0	8/16-bit composite timer 01 status control register 0	R/W	0b00000000
0x0F93	T00CR0	8/16-bit composite timer 00 status control register 0	R/W	0b00000000
0x0F94	T01DR	8/16-bit composite timer 01 data register	R/W	0b00000000
0x0F95	T00DR	8/16-bit composite timer 00 data register	R/W	0b00000000
0x0F96	TMCR0	8/16-bit composite timer 00/01 timer mode control register	R/W	0b00000000
0x0F97	T11CR0	8/16-bit composite timer 11 status control register 0	R/W	0b00000000
0x0F98	T10CR0	8/16-bit composite timer 10 status control register 0	R/W	0b00000000
0x0F99	T11DR	8/16-bit composite timer 11 data register	R/W	0b00000000
0x0F9A	T10DR	8/16-bit composite timer 10 data register	R/W	0b00000000
0x0F9B	TMCR1	8/16-bit composite timer 10/11 timer mode control register	R/W	0b00000000
0x0F9C	PPS01	8/16-bit PPG01 cycle setting buffer register	R/W	0b11111111
0x0F9D	PPS00	8/16-bit PPG00 cycle setting buffer register	R/W	0b11111111
0x0F9E	PDS01	8/16-bit PPG01 duty setting buffer register	R/W	0b11111111
0x0F9F	PDS00	8/16-bit PPG00 duty setting buffer register	R/W	0b11111111
0x0FA0	PPS11	8/16-bit PPG11 cycle setting buffer register	R/W	0b11111111
0x0FA1	PPS10	8/16-bit PPG10 cycle setting buffer register	R/W	0b11111111
0x0FA2	PDS11	8/16-bit PPG11 duty setting buffer register	R/W	0b11111111
0x0FA3	PDS10	8/16-bit PPG10 duty setting buffer register	R/W	0b11111111
0x0FA4	PPGS	8/16-bit PPG start register	R/W	0b00000000
0x0FA5	REVC	8/16-bit PPG output inversion register	R/W	0b00000000
0x0FA6	PPS21	8/16-bit PPG21 cycle setting buffer register	R/W	0b11111111
0x0FA7	PPS20	8/16-bit PPG20 cycle setting buffer register	R/W	0b11111111
0x0FA8, 0x0FA9	—	(Disabled)	—	—
0x0FAA	PDS21	8/16-bit PPG21 duty setting buffer register	R/W	0b11111111
0x0FAB	PDS20	8/16-bit PPG20 duty setting buffer register	R/W	0b11111111
0x0FAC to 0x0FBD	—	(Disabled)	—	—
0x0FBE	PSSR0	UART/SIO dedicated baud rate generator prescaler select register ch. 0	R/W	0b00000000
0x0FBF	BRSR0	UART/SIO dedicated baud rate generator baud rate setting register ch. 0	R/W	0b00000000
0x0FC0	TIDR0	Touch input disable register 0	R/W	0b00000000
0x0FC1	TIDR1	Touch input disable register 1	R/W	0b00000000
0x0FC2	—	(Disabled)	—	—
0x0FC3	AIDRL	A/D input disable register (lower)	R/W	0b00000000
0x0FC4	LVDPW	LVD reset circuit password register	R/W	0b00000000
0x0FC5 to 0x0FE2	—	(Disabled)	—	—
0x0FE3	WCDR	Watch counter data register	R/W	0b00111111
0x0FE4	CRTH	Main CR clock trimming register (upper)	R/W	0b000XXXXX

Address	Register abbreviation	Register name	R/W	Initial value
0x0FE5	CRTL	Main CR clock trimming register (lower)	R/W	0b000XXXXX
0x0FE6	—	(Disabled)	—	—
0x0FE7	CRTDA	Main CR clock temperature dependent adjustment register	R/W	0b000XXXXX
0x0FE8	SYSC	System configuration register	R/W	0b11000011
0x0FE9	CMCR	Clock monitoring control register	R/W	0b00000000
0x0FEA	CMDR	Clock monitoring data register	R	0b00000000
0x0FEB	WDTH	Watchdog timer selection ID register (upper)	R	0bXXXXXXXX
0x0FEC	WDTL	Watchdog timer selection ID register (lower)	R	0bXXXXXXXX
0x0FED, 0x0FEE	—	(Disabled)	—	—
0x0FEF	WICR	Interrupt pin selection circuit control register	R/W	0b01000000
0x0FF0 to 0x0FFF	—	(Disabled)	—	—

■ R/W access symbols
R/W : Readable/Writable
R : Read only

■ Initial value symbols
0 : The initial value of this bit is “0”.
1 : The initial value of this bit is “1”.
X : The initial value of this bit is undefined.

Note: Do not write to an address that is “(Disabled)”. If a “(Disabled)” address is read, an indeterminate value is returned.

14. I/O Ports

14.1 MB95850K Series

■ List of port registers

Register name		Read/Write	Initial value
Port 0 data register	PDR0	R, RM/W	0b00000000
Port 0 direction register	DDR0	R/W	0b00000000
Port 1 data register	PDR1	R, RM/W	0b00000000
Port 1 direction register	DDR1	R/W	0b00000000
Port 4 data register	PDR4	R, RM/W	0b00000000
Port 4 direction register	DDR4	R/W	0b00000000
Port 6 data register	PDR6	R, RM/W	0b00000000
Port 6 direction register	DDR6	R/W	0b00000000
Port 7 data register	PDR7	R, RM/W	0b00000000
Port 7 direction register	DDR7	R/W	0b00000000
Port F data register	PDRF	R, RM/W	0b00000000
Port F direction register	DDRF	R/W	0b00000000
Port G data register	PDRG	R, RM/W	0b00000000
Port G direction register	DDRG	R/W	0b00000000
Port 0 pull-up register	PUL0	R/W	0b00000000
Port 1 pull-up register	PUL1	R/W	0b00000000
Port 6 pull-up register	PUL6	R/W	0b00000000
Port 7 pull-up register	PUL7	R/W	0b00000000
Port G pull-up register	PULG	R/W	0b00000000
A/D input disable register (lower)	AIDRL	R/W	0b00000000
Touch input disable register 0	TIDR0	R/W	0b00000000
Touch input disable register 1	TIDR1	R/W	0b00000000

R/W : Readable/writable (The read value is the same as the write value.)

R, RM/W : Readable/writable (The read value is different from the write value. The write value is read by the read-modify-write (RMW) type of instruction.)

14.1.1 Port 0

Port 0 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

1. Port 0 configuration

■ Port 0 is made up of the following elements.
- ❒ General-purpose I/O pins/peripheral function I/O pins
- ❒ Port 0 data register (PDR0)
- ❒ Port 0 direction register (DDR0)
- ❒ Port 0 pull-up register (PUL0)
- ❒ A/D input disable register (lower) (AIDRL)

2. Block diagrams of port 0

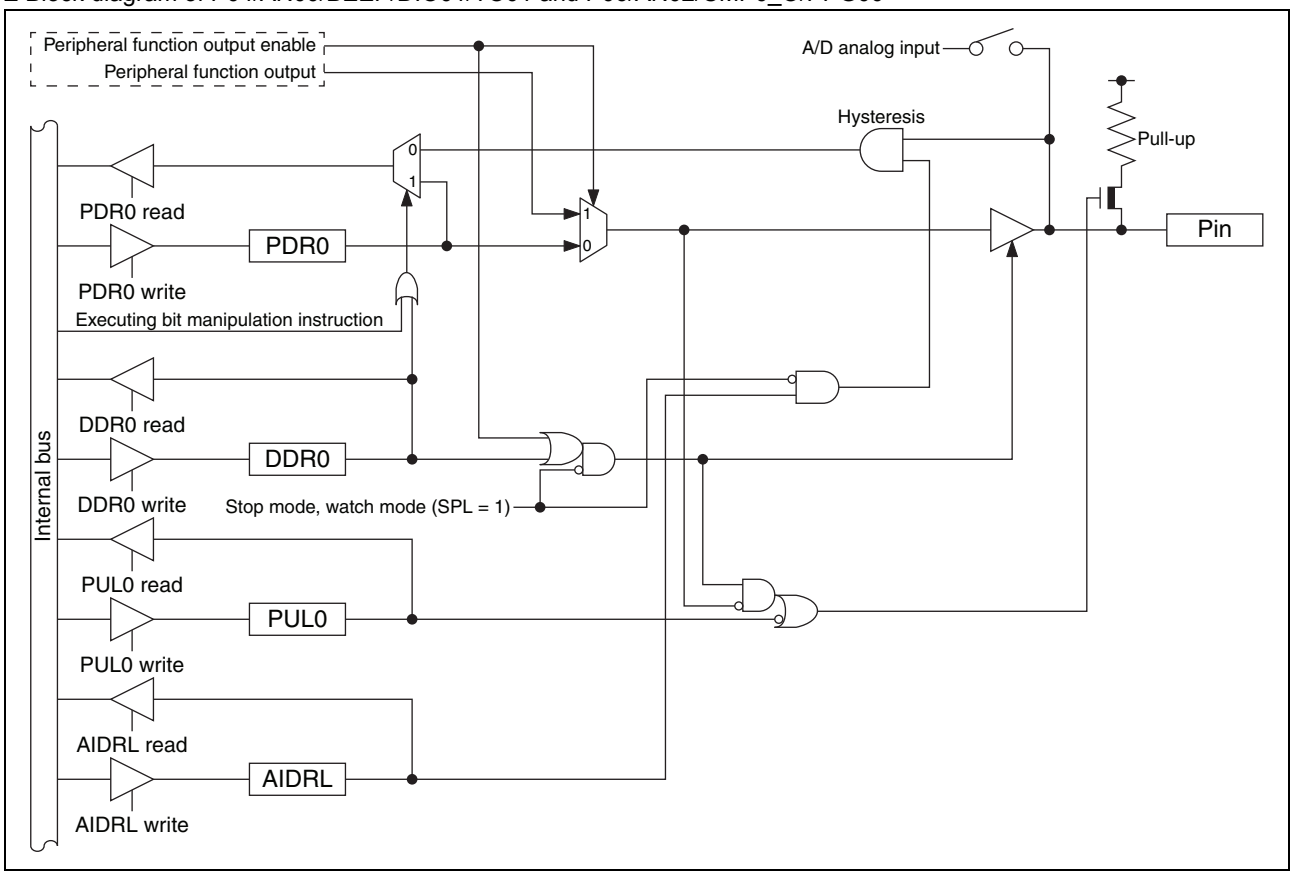
■ P04/AN00/BEEP/DIO01/TO01 pin

This pin has the following peripheral functions:
- ❒ 8/10-bit A/D converter analog input pin (AN00)
- ❒ Beep output pin (BEEP)
- ❒ TS direct output ch. 1 pin (DIO01)
- ❒ 8/16-bit composite timer ch. 0 output pin (TO01)

■ P06/AN02/CMP0_O/PPG00 pin

This pin has the following peripheral functions:
- ❒ 8/10-bit A/D converter analog input pin (AN02)
- ❒ Comparator ch. 0 digital output pin (CMP0_O)
- ❒ 816-bit PPG ch. 0 output pin (PPG00)

■ Block diagram of P04/AN00/BEEP/DIO01/TO01 and P06/AN02/CMP0_O/PPG00

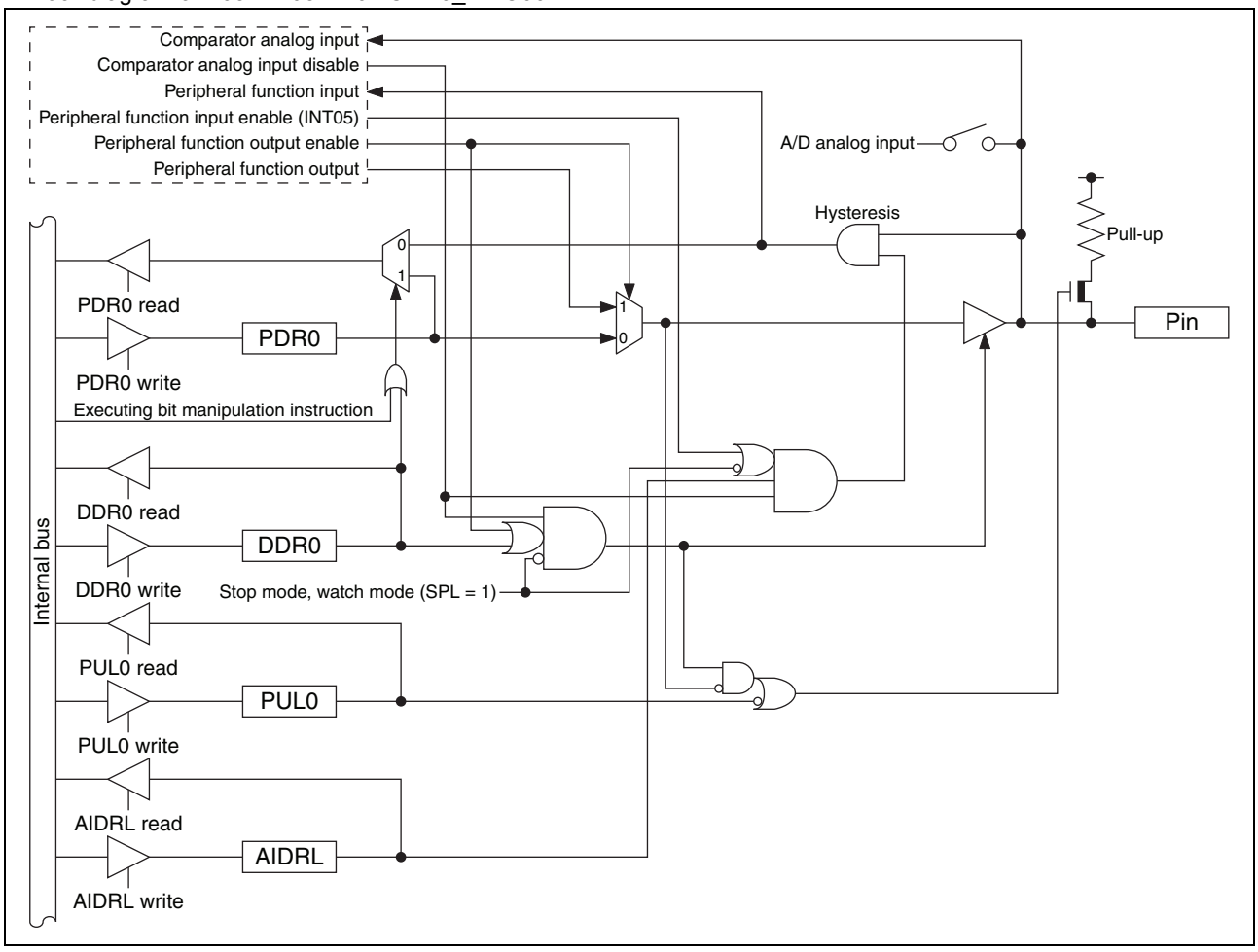


■ P05/INT05/AN01/CMP0_N/TO00 pin

This pin has the following peripheral functions:

- ❒ External interrupt input pin (INT05)
- ❒ 8/10-bit A/D converter analog input pin (AN01)
- ❒ Comparator ch. 0 inverting analog input (negative input) pin (CMP0_N)
- ❒ 8/16-bit composite timer ch. 0 output pin (TO00)

■ Block diagram of P05/INT05/AN01/CMP0_N/TO00

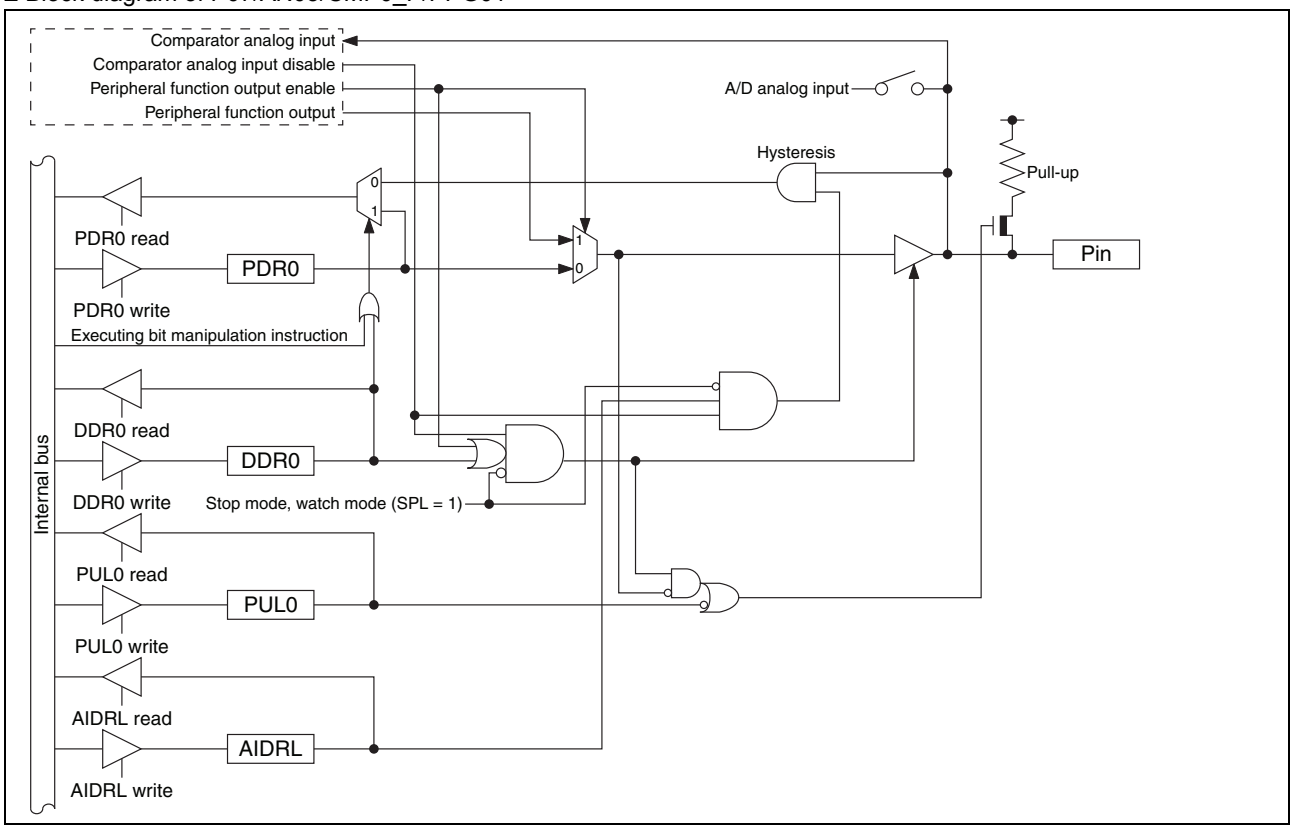


■ P07/AN03/CMP0_P/PPG01 pin

This pin has the following peripheral functions:

- ❒ 8/10-bit A/D converter analog input pin (AN03)
- ❒ Comparator ch. 0 non-inverting analog input (positive input) pin (CMP0_P)
- ❒ 8/16-bit PPG ch. 0 output pin (PPG01)

■ Block diagram of P07/AN03/CMP0_P/PPG01



3. Port 0 registers

■ Port 0 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR0	0	Pin state is “L” level.	PDR0 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR0 value is “1”.	As output port, outputs “H” level.
DDR0	0	Port input enabled		
	1	Port output enabled		
PUL0	0	Pull-up disabled		
	1	Pull-up enabled		
AIDRL	0	Analog input enabled		
	1	Port input enabled		

■ Correspondence between registers and pins for port 0

Pin name	Correspondence between related register bits and pins							
	P07	P06	P05	P04	-	-	-	-
PDR0	bit7	bit6	bit5	bit4	-	-	-	-
DDR0								
PUL0								
AIDRL	bit5	bit4	bit1	bit0				

4. Port 0 operations

■ Operation as an output port
- ❒ A pin becomes an output port if the bit in the DDR0 register corresponding to that pin is set to “1”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ When a pin is used as an output port, it outputs the value of the PDR0 register to external pins.
- ❒ If data is written to the PDR0 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
- ❒ Reading the PDR0 register returns the PDR0 register value.

■ Operation as an input port
- ❒ A pin becomes an input port if the bit in the DDR0 register corresponding to that pin is set to “0”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ When using a pin shared with the analog input function as an input port, set the bit in the A/D input disable register (lower) (AIDRL) corresponding to that pin to “1”.
- ❒ If data is written to the PDR0 register, the value is stored in the output latch but is not output to the pin set as an input port.
- ❒ Reading the PDR0 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR0 register, the PDR0 register value is returned.

■ Operation as a peripheral function output pin
- ❒ A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
- ❒ The pin value can be read from the PDR0 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR0 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR0 register, the PDR0 register value is returned.

■ Operation as a peripheral function input pin
- ❒ To set a pin as an input port, set the bit in the DDR0 register corresponding to the input pin of a peripheral function to “0”.
- ❒ When using a pin shared with the analog input function as another peripheral function input pin, configure it as an input port by setting the bit in the AIDRL register corresponding to that pin to “1”.
- ❒ Reading the PDR0 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR0 register, the PDR0 register value is returned.

■ Operation at reset

If the CPU is reset, all bits in the DDR0 register are initialized to “0” and port input is enabled. As for a pin shared with the analog input function, its port input is disabled because the AIDRL register is initialized to “0”.

■ Operation in stop mode and watch mode
- ❒ If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR0 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open. However, if the interrupt input is enabled for the external interrupt (INT05), the input is enabled and not blocked.
- ❒ If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

■ Operation as an analog input pin
- ❒ Set the DDR0 register bit corresponding to analog input pin to “0” and the bit corresponding to that pin in the AIDRL register to “0”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions. In addition, set the corresponding bit in the PUL0 register to “0”.

■ Operation as an external interrupt input pin
- ❒ Set the bit in the DDR0 register corresponding to the external interrupt input pin to “0”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ The pin value is always input to the external interrupt circuit. When using a pin for a function other than the interrupt, disable the external interrupt function corresponding to that pin.

■ Operation of the pull-up register

Setting the bit in the PUL0 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL0 register.

■ Operation as a comparator input pin
- ❒ Set the bit in the AIDRL register corresponding to the comparator input pin to “0”.
- ❒ Regardless of the value of the PDR0 register and that of the DDR0 register, if the comparator analog input enable bit in the comparator control register ch. 0 (CMR0:VCID) is set to “0”, the comparator input function is enabled.
- ❒ To disable the comparator input function, set the VCID bit to “1”.
- ❒ For details of the comparator, see “CHAPTER 25 COMPARATOR” in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

14.1.2 Port 1

Port 1 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

1. Port 1 configuration

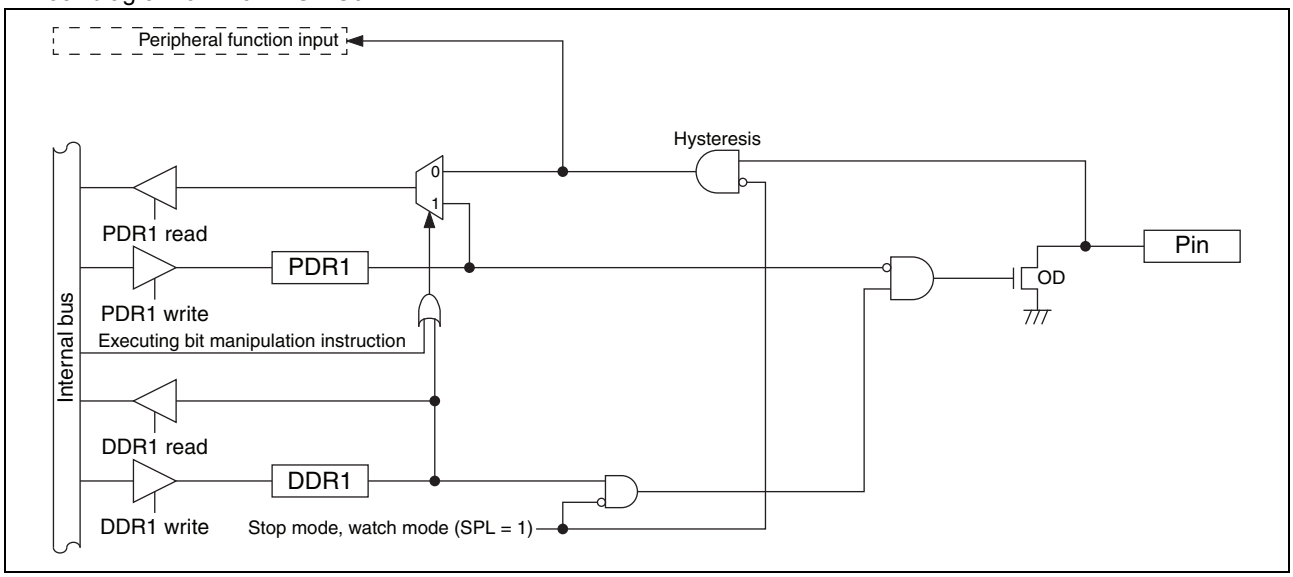
■ Port 1 is made up of the following elements.
- ❒ General-purpose I/O pins/peripheral function I/O pins
- ❒ Port 1 data register (PDR1)
- ❒ Port 1 direction register (DDR1)
- ❒ Port 1 pull-up register (PUL1)

2. Block diagrams of port 1

■ P10/DBG/EC0 pin

This pin has the following peripheral functions:
- ❒ DBG input pin (DBG)
- ❒ 8/16-bit composite timer ch. 0 clock input pin (EC0)

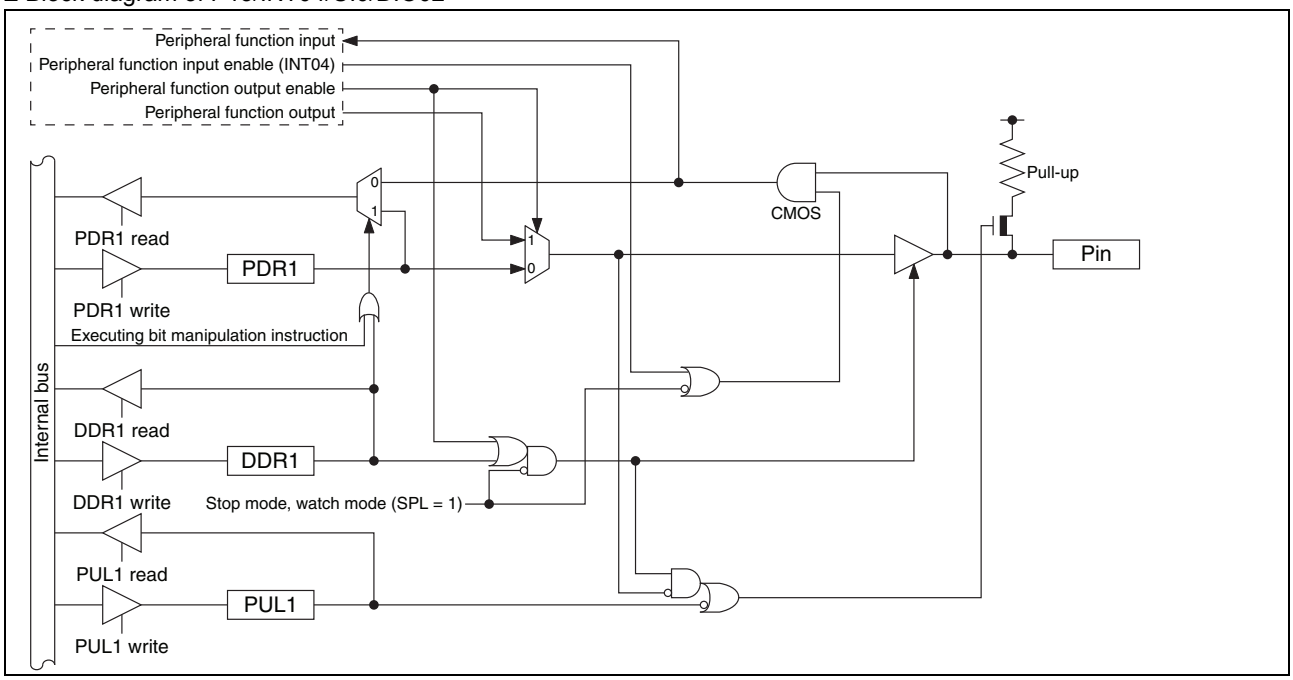
■ Block diagram of P10/DBG/EC0



■ P13/INT04/UI0/DIO02 pin

This pin has the following peripheral functions:
- ❒ External interrupt input pin (INT04)
- ❒ UART/SIO ch. 0 data input pin (UI0)
- ❒ TS direct output ch. 2 pin (DIO02)

■ Block diagram of P13/INT04/UI0/DIO02



■ P14/INT01/UO0/DIO00 pin

This pin has the following peripheral functions:

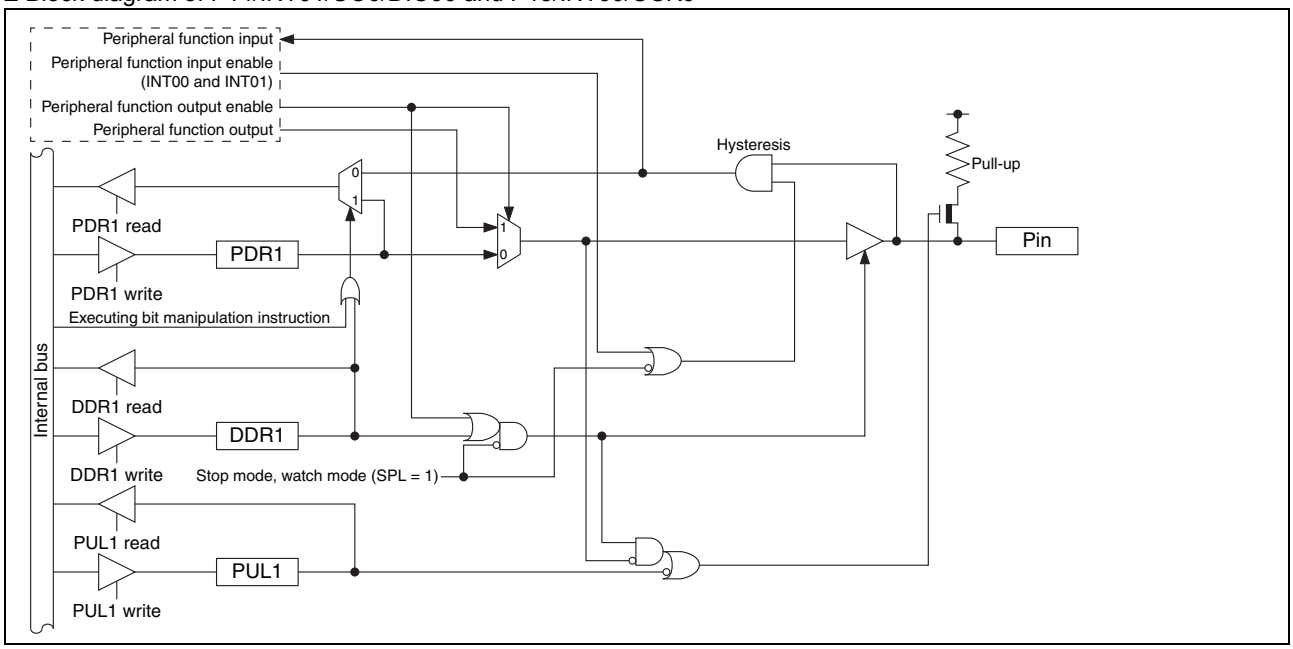
- ❒ External interrupt input pin (INT01)
- ❒ UART/SIO ch. 0 data output pin (UO0)
- ❒ TS direct output ch. 0 pin (DIO00)

■ P15/INT00/UCK0 pin

This pin has the following peripheral functions:

- ❒ External interrupt input pin (INT00)
- ❒ UART/SIO ch. 0 clock I/O pin (UCK0)

■ Block diagram of P14/INT01/UO0/DIO00 and P15/INT00/UCK0



3. Port 1 registers

■ Port 1 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR1	0	Pin state is “L” level.	PDR1 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR1 value is “1”.	As output port, outputs “H” level.*
DDR1	0	Port input enabled		
	1	Port output enabled		
PUL1	0	Pull-up disabled		
	1	Pull-up enabled		

*: If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

■ Correspondence between registers and pins for port 1

Pin name	Correspondence between related register bits and pins							
	-	-	P15	P14	P13	-	-	P10
PDR1	-	-	bit5	bit4	bit3	-	-	bit0*
DDR1								
PUL1								

*: Though P10 has no pull-up function, bit0 in the PUL1 register can still be accessed. The operation of P10 is not affected by the setting of bit0 in the PUL1 register.

4. Port 1 operations

■ Operation as an output port
- ❒ A pin becomes an output port if the bit in the DDR1 register corresponding to that pin is set to “1”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ When a pin is used as an output port, it outputs the value of the PDR1 register to external pins.
- ❒ If data is written to the PDR1 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
- ❒ Reading the PDR1 register returns the PDR1 register value.

■ Operation as an input port
- ❒ A pin becomes an input port if the bit in the DDR1 register corresponding to that pin is set to “0”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ If data is written to the PDR1 register, the value is stored in the output latch but is not output to the pin set as an input port.
- ❒ Reading the PDR1 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR1 register, the PDR1 register value is returned.

■ Operation as a peripheral function output pin
- ❒ A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
- ❒ The pin value can be read from the PDR1 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR1 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR1 register, the PDR1 register value is returned.

■ Operation as a peripheral function input pin
- ❒ To set a pin as an input port, set the bit in the DDR1 register corresponding to the input pin of a peripheral function to “0”.
- ❒ Reading the PDR1 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR1 register, the PDR1 register value is returned.

■ Operation at reset

If the CPU is reset, all bits in the DDR1 register are initialized to “0” and port input is enabled.

■ Operation in stop mode and watch mode

- If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR1 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open. However, if the interrupt input from the external interrupt (INT00, INT01 and INT04) is enabled, or if the interrupt input of P10/DBG/EC0 is enabled by the external interrupt control register ch. 0 (EIC00) of the external interrupt circuit and the interrupt pin selection circuit control register (WICR) of the interrupt pin selection circuit, the input is enabled and is not blocked.
- If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

■ Operation as an external interrupt input pin

- Set the bit in the DDR1 register corresponding to the external interrupt input pin to “0”.
- For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- The pin value is always input to the external interrupt circuit. When using a pin for a function other than the interrupt, disable the external interrupt function corresponding to that pin.

■ Operation of the pull-up register

Setting the bit in the PUL1 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL1 register.

14.1.3 Port 4

Port 4 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

1. Port 4 configuration

■ Port 4 is made up of the following elements.
- ❒ General-purpose I/O pins/peripheral function I/O pins
- ❒ Port 4 data register (PDR4)
- ❒ Port 4 direction register (DDR4)

2. Block diagrams of port 4

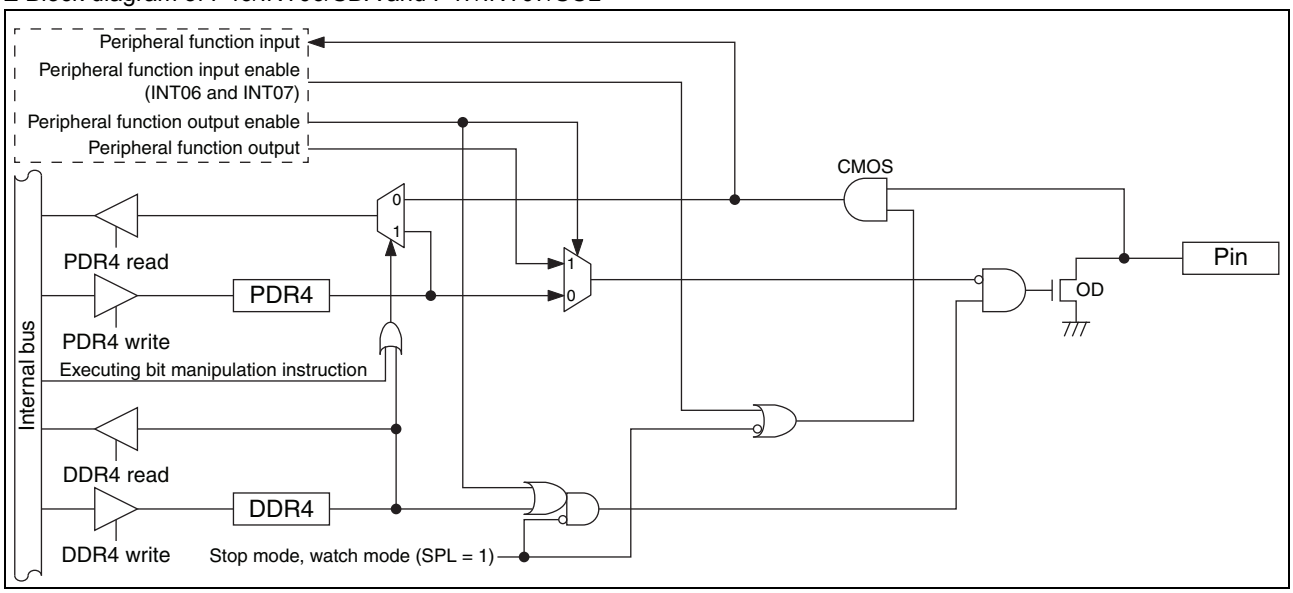
■ P46/INT06/SDA pin

This pin has the following peripheral functions:
- ❒ External interrupt input pin (INT06)
- ❒ I^2C bus interface ch. 0 data I/O pin (SDA)

■ P47/INT07/SCL pin

This pin has the following peripheral functions:
- ❒ External interrupt input pin (INT07)
- ❒ I^2C bus interface ch. 0 clock I/O pin (SCL)

■ Block diagram of P46/INT06/SDA and P47/INT07/SCL



3. Port 4 registers

■ Port 4 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR4	0	Pin state is “L” level.	PDR4 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR4 value is “1”.	As output port, outputs “H” level.*
DDR4	0	Port input enabled		
	1	Port output enabled		

*: If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

■ Correspondence between registers and pins for port 4

Pin name	Correspondence between related register bits and pins							
	P47	P46	-	-	-	-	-	-
PDR4	bit7	bit6	-	-	-	-	-	-
DDR4								

4. Port 4 operations

■ Operation as an output port
- ❒ A pin becomes an output port if the bit in the DDR4 register corresponding to that pin is set to “1”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ When a pin is used as an output port, it outputs the value of the PDR4 register to external pins.
- ❒ If data is written to the PDR4 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
- ❒ Reading the PDR4 register returns the PDR4 register value.

■ Operation as an input port
- ❒ A pin becomes an input port if the bit in the DDR4 register corresponding to that pin is set to “0”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ If data is written to the PDR4 register, the value is stored in the output latch but is not output to the pin set as an input port.
- ❒ Reading the PDR4 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR4 register, the PDR4 register value is returned.

■ Operation as a peripheral function output pin
- ❒ A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
- ❒ The pin value can be read from the PDR4 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR4 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR4 register, the PDR4 register value is returned.

■ Operation as a peripheral function input pin
- ❒ To set a pin as an input port, set the bit in the DDR4 register corresponding to the input pin of a peripheral function to “0”.
- ❒ Reading the PDR4 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR4 register, the PDR4 register value is returned.

■ Operation at reset

If the CPU is reset, all bits in the DDR4 register are initialized to “0” and port input is enabled.

■ Operation in stop mode and watch mode
- ❒ If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR4 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open. However, if the interrupt input is enabled for the external interrupt (INT06 and INT07), the input is enabled and not blocked.
- ❒ If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

■ Operation as an external interrupt input pin
- ❒ Set the bit in the DDR4 register corresponding to the external interrupt input pin to “0”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ The pin value is always input to the external interrupt circuit. When using a pin for a function other than the interrupt, disable the external interrupt function corresponding to that pin.

14.1.4 Port 6

Port 6 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

1. Port 6 configuration

■ Port 6 is made up of the following elements.
- ❒ General-purpose I/O pins/peripheral function I/O pins
- ❒ Port 6 data register (PDR6)
- ❒ Port 6 direction register (DDR6)
- ❒ Port 6 pull-up register (PUL6)
- ❒ Touch input disable register 0 (TIDR0)

2. Block diagrams of port 6

■ P63/AREF pin

This pin has the following peripheral function:
- ❒ TS reference input pin (AREF)

■ P65/S01 pin

This pin has the following peripheral function:
- ❒ TS touch ch. 1 input pin (S01)

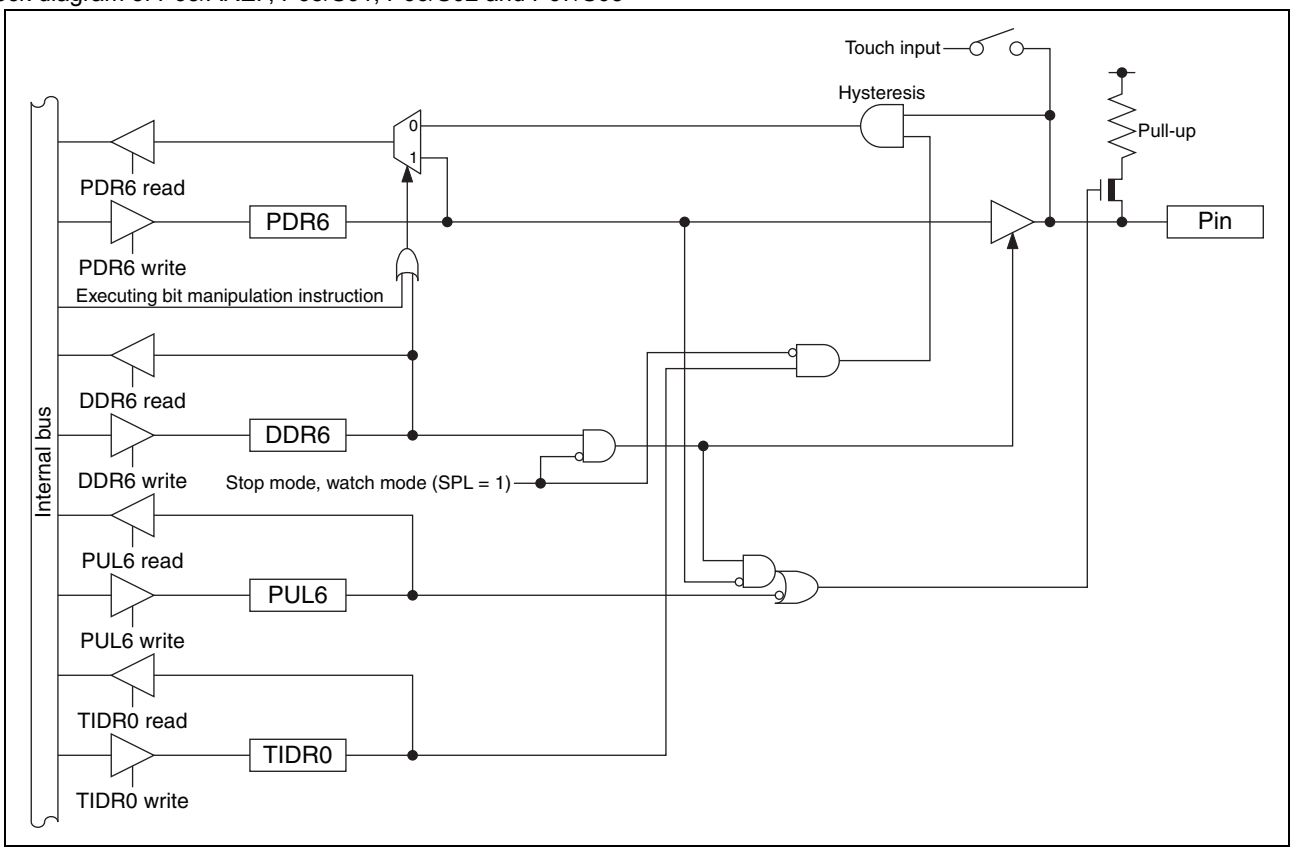
■ P66/S02 pin

This pin has the following peripheral function:
- ❒ TS touch ch. 2 input pin (S02)

■ P67/S03 pin

This pin has the following peripheral function:
- ❒ TS touch ch. 3 input pin (S03)

■ Block diagram of P63/AREF, P65/S01, P66/S02 and P67/S03



3. Port 6 registers

■ Port 6 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR6	0	Pin state is “L” level.	PDR6 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR6 value is “1”.	As output port, outputs “H” level.
DDR6	0	Port input enabled		
	1	Port output enabled		
PUL6	0	Pull-up disabled		
	1	Pull-up enabled		
TIDR0	0	Touch input or reference input enabled		
	1	Port input enabled		

■ Correspondence between registers and pins for port 6

Pin name	Correspondence between related register bits and pins							
	P67	P66	P65	-	P63	-	-	-
PDR6	bit7	bit6	bit5	-	bit3	-	-	-
DDR6								
PUL6								
TIDR0	bit7	bit6	bit5		bit3			

4. Port 6 operations

■ Operation as an output port

- ❒ A pin becomes an output port if the bit in the DDR6 register corresponding to that pin is set to “1”.
- ❒ When a pin is used as an output port, it outputs the value of the PDR6 register to external pins.
- ❒ If data is written to the PDR6 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
- ❒ Reading the PDR6 register returns the PDR6 register value.

■ Operation as an input port

- ❒ A pin becomes an input port if the bit in the DDR6 register corresponding to that pin is set to “0”.
- ❒ When using a pin shared with the touch input function as an input port, set the bit in the touch input disable register 0 (TIDR0) corresponding to that pin to “1”.
- ❒ If data is written to the PDR6 register, the value is stored in the output latch but is not output to the pin set as an input port.
- ❒ Reading the PDR6 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR6 register, the PDR6 register value is returned.

■ Operation at reset

If the CPU is reset, all bits in the DDR6 register are initialized to “0” and port input is enabled. As for a pin shared with the touch input function, its port input is disabled because the TIDR0 register is initialized to “0”.

■ Operation in stop mode and watch mode

- ❒ If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR6 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
- ❒ When the stop enable bit in the TS prescaler control register (PSC:STPE) is set to “1”, the TS can operate in stop mode or watch mode, the touch input is enabled and is not blocked. The TS wakes up in stop mode or watch mode provided that the TINT (touch interrupt) and the GINT (general interrupt) are set to enable the TS to wake up in stop mode or watch mode.
- ❒ If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

■ Operation as a touch input pin

Set the bit in the DDR6 register corresponding to the touch input pin to “0”, the bit in the TIDR0 register corresponding to the same pin to “0”, and the bit in the PUL6 register corresponding to the same pin to “0”.

■ Operation of the pull-up register

Setting the bit in the PUL6 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL6 register.

14.1.5 Port 7

Port 7 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

1. Port 7 configuration

■ Port 7 is made up of the following elements.
- ❒ General-purpose I/O pins/peripheral function I/O pins
- ❒ Port 7 data register (PDR7)
- ❒ Port 7 direction register (DDR7)
- ❒ Port 7 pull-up register (PUL7)
- ❒ Touch input disable register 1 (TIDR1)

2. Block diagrams of port 7

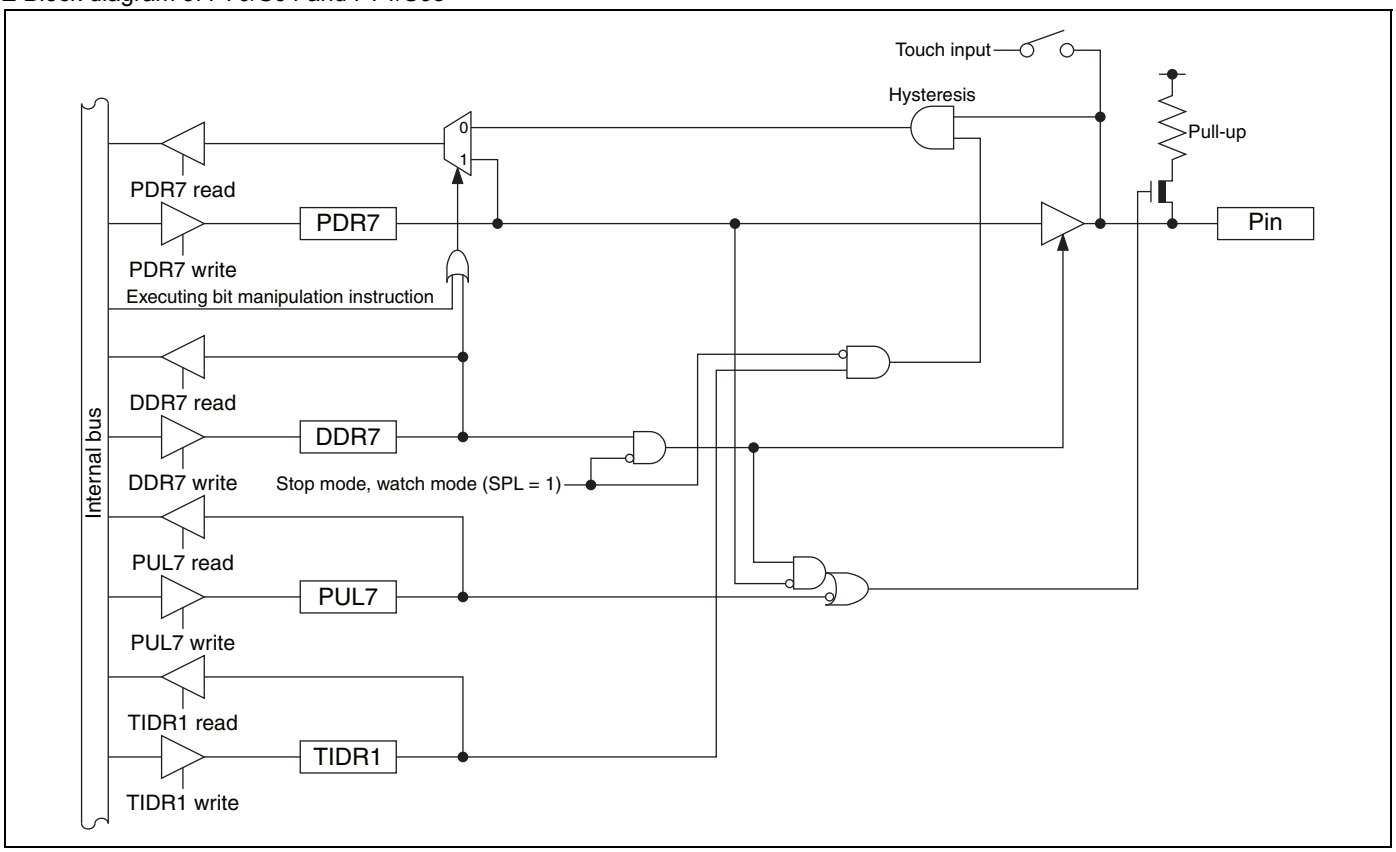
■ P70/S04 pin

This pin has the following peripheral function:
- ❒ TS touch ch. 4 input pin (S04)

■ P71/S05 pin

This pin has the following peripheral function:
- ❒ TS touch ch. 5 input pin (S05)

■ Block diagram of P70/S04 and P71/S05



3. Port 7 registers

■ Port 7 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR7	0	Pin state is “L” level.	PDR7 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR7 value is “1”.	As output port, outputs “H” level.
DDR7	0	Port input enabled		
	1	Port output enabled		
PUL7	0	Pull-up disabled		
	1	Pull-up enabled		
TIDR1	0	Touch input enabled		
	1	Port input enabled		

■ Correspondence between registers and pins for port 7

Pin name	Correspondence between related register bits and pins							
	-	-	-	-	-	-	P71	P70
PDR7	-	-	-	-	-	-	bit1	bit0
DDR7								
PUL7								
TIDR1								

4. Port 7 operations

■ Operation as an output port

- ❒ A pin becomes an output port if the bit in the DDR7 register corresponding to that pin is set to “1”.
- ❒ When a pin is used as an output port, it outputs the value of the PDR7 register to external pins.
- ❒ If data is written to the PDR7 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
- ❒ Reading the PDR7 register returns the PDR7 register value.

■ Operation as an input port

- ❒ A pin becomes an input port if the bit in the DDR7 register corresponding to that pin is set to “0”.
- ❒ When using a pin shared with the touch input function as an input port, set the bit in the touch input disable register 1 (TIDR1) corresponding to that pin to “1”.
- ❒ If data is written to the PDR7 register, the value is stored in the output latch but is not output to the pin set as an input port.
- ❒ Reading the PDR7 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR7 register, the PDR7 register value is returned.

■ Operation at reset

If the CPU is reset, all bits in the DDR7 register are initialized to “0” and port input is enabled. As for a pin shared with the touch input function, its port input is disabled because the TIDR1 register is initialized to “0”.

■ Operation in stop mode and watch mode

- ❒ If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR7 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
- ❒ When the stop enable bit in the TS prescaler control register (PSC:STPE) is set to “1”, the TS can operate in stop mode or watch mode, the touch input is enabled and is not blocked. The TS wakes up in stop mode or watch mode provided that the TINT (touch interrupt) and the GINT (general interrupt) are set to enable the TS to wake up in stop mode or watch mode.
- ❒ If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

■ Operation as a touch input pin

Set the bit in the DDR7 register corresponding to the touch input pin to “0”, the bit in the TIDR1 register corresponding to the same pin to “0”, and the bit in the PUL7 register corresponding to the same pin to “0”.

■ Operation of the pull-up register

Setting the bit in the PUL7 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL7 register.

14.1.6 Port F

Port F is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

1. Port F configuration

■ Port F is made up of the following elements.
- ❒ General-purpose I/O pins/peripheral function I/O pins
- ❒ Port F data register (PDRF)
- ❒ Port F direction register (DDRF)

2. Block diagrams of port F

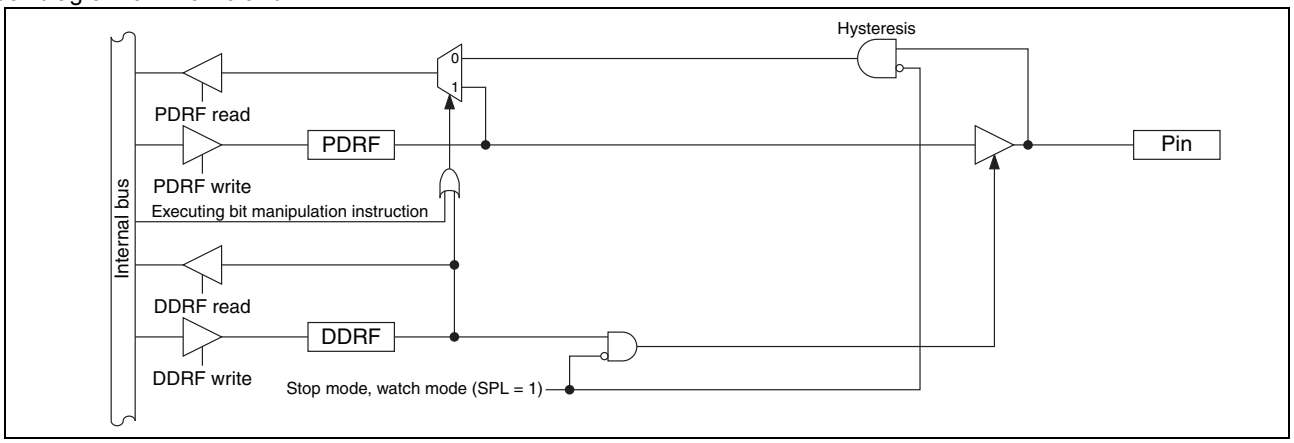
■ PF0/X0 pin

This pin has the following peripheral function:
- ❒ Main clock input oscillation pin (X0)

■ PF1/X1 pin

This pin has the following peripheral function:
- ❒ Main clock I/O oscillation pin (X1)

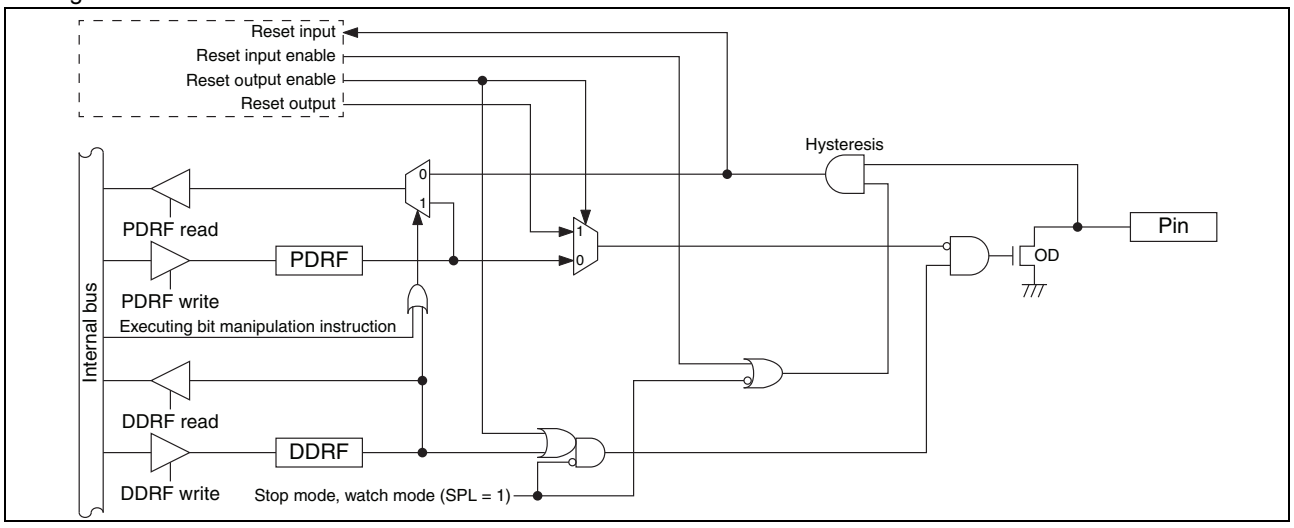
■ Block diagram of PF0/X0 and PF1/X1



■ PF2/$\overline{\text{RST}}$ pin

This pin has the following peripheral function:
- ❒ Reset pin ($\overline{\text{RST}}$)

■ Block diagram of PF2/$\overline{\text{RST}}$



3. Port F registers

■ Port F register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDRF	0	Pin state is “L” level.	PDRF value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDRF value is “1”.	As output port, outputs “H” level.*
DDRF	0	Port input enabled		
	1	Port output enabled		

*: If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

■ Correspondence between registers and pins for port F

Pin name	Correspondence between related register bits and pins							
	-	-	-	-	-	PF2	PF1	PF0
PDRF	-	-	-	-	-	bit2	bit1	bit0
DDRF								

4. Port F operations

■ Operation as an output port
- ❒ A pin becomes an output port if the bit in the DDRF register corresponding to that pin is set to “1”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ When a pin is used as an output port, it outputs the value of the PDRF register to external pins.
- ❒ If data is written to the PDRF register, the value is stored in the output latch and is output to the pin set as an output port as it is.
- ❒ Reading the PDRF register returns the PDRF register value.

■ Operation as an input port
- ❒ A pin becomes an input port if the bit in the DDRF register corresponding to that pin is set to “0”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ If data is written to the PDRF register, the value is stored in the output latch but is not output to the pin set as an input port.
- ❒ Reading the PDRF register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDRF register, the PDRF register value is returned.

■ Operation at reset

If the CPU is reset, all bits in the DDRF register are initialized to “0” and port input is enabled.

■ Operation in stop mode and watch mode
- ❒ If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRF register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
- ❒ If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

14.1.7 Port G

Port G is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

1. Port G configuration

■ Port G is made up of the following elements.
- ❒ General-purpose I/O pins/peripheral function I/O pins
- ❒ Port G data register (PDRG)
- ❒ Port G direction register (DDRG)
- ❒ Port G pull-up register (PULG)

2. Block diagram of port G

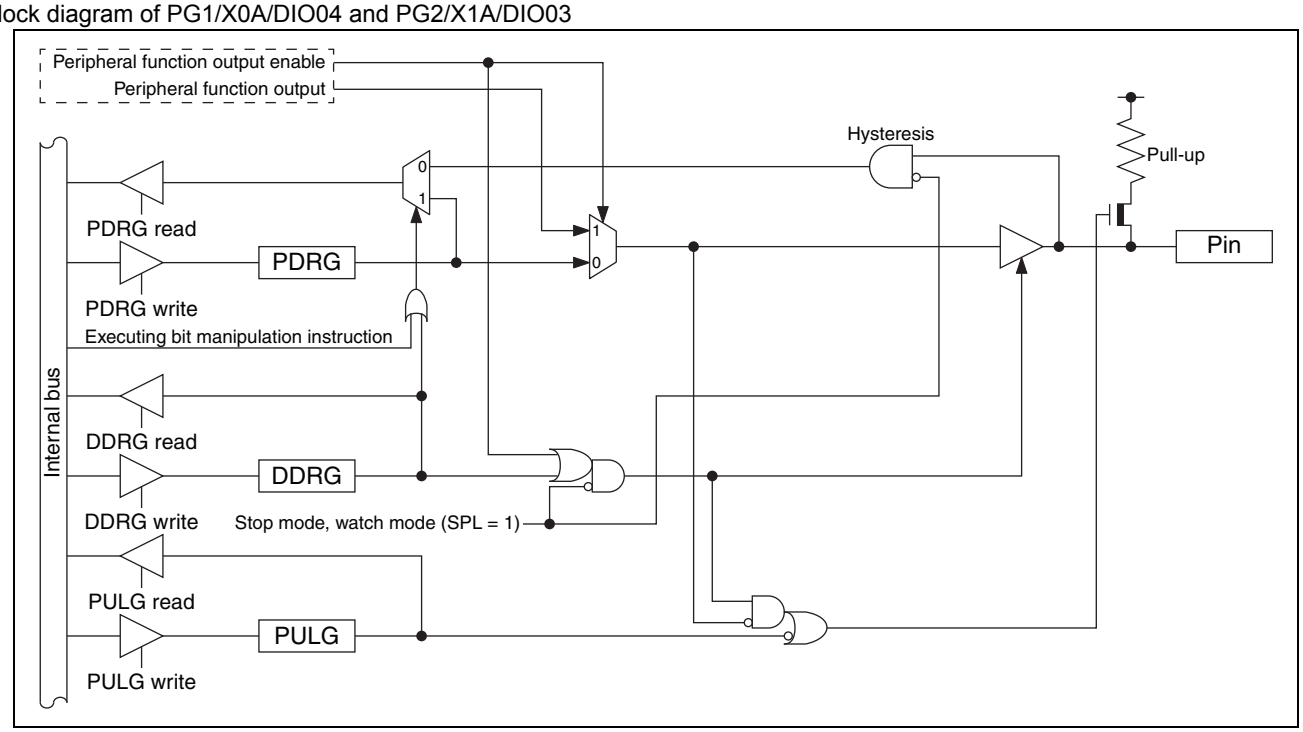
■ PG1/X0A/DIO04 pin

This pin has the following peripheral functions:
- ❒ Subclock input oscillation pin (X0A)
- ❒ TS direct output ch. 4 pin (DIO04)

■ PG2/X1A/DIO03 pin

This pin has the following peripheral functions:
- ❒ Subclock I/O oscillation pin (X1A)
- ❒ TS direct output ch. 3 pin (DIO03)

■ Block diagram of PG1/X0A/DIO04 and PG2/X1A/DIO03



3. Port G registers

■ Port G register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDRG	0	Pin state is “L” level.	PDRG value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDRG value is “1”.	As output port, outputs “H” level.
DDRG	0	Port input enabled		
	1	Port output enabled		
PULG	0	Pull-up disabled		
	1	Pull-up enabled		

■ Correspondence between registers and pins for port G

Pin name	Correspondence between related register bits and pins							
	-	-	-	-	-	PG2	PG1	-
PDRG	-	-	-	-	-	bit2	bit1	-
DDRG								
PULG								

4. Port G operations

■ Operation as an output port
- ❒ A pin becomes an output port if the bit in the DDRG register corresponding to that pin is set to “1”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ When a pin is used as an output port, it outputs the value of the PDRG register to external pins.
- ❒ If data is written to the PDRG register, the value is stored in the output latch and is output to the pin set as an output port as it is.
- ❒ Reading the PDRG register returns the PDRG register value.

■ Operation as an input port
- ❒ A pin becomes an input port if the bit in the DDRG register corresponding to that pin is set to “0”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ If data is written to the PDRG register, the value is stored in the output latch but is not output to the pin set as an input port.
- ❒ Reading the PDRG register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDRG register, the PDRG register value is returned.

■ Operation as a peripheral function output pin
- ❒ A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
- ❒ The pin value can be read from the PDRG register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDRG register. However, if the read-modify-write (RMW) type of instruction is used to read the PDRG register, the PDRG register value is returned.

■ Operation at reset

If the CPU is reset, all bits in the DDRG register are initialized to “0” and port input is enabled.

■ Operation in stop mode and watch mode
- ❒ If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRG register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
- ❒ If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

■ Operation of the pull-up register

Setting the bit in the PULG register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PULG register.

14.2 MB95860K Series

■ List of port registers

Register name		Read/Write	Initial value
Port 0 data register	PDR0	R, RM/W	0b00000000
Port 0 direction register	DDR0	R/W	0b00000000
Port 1 data register	PDR1	R, RM/W	0b00000000
Port 1 direction register	DDR1	R/W	0b00000000
Port 4 data register	PDR4	R, RM/W	0b00000000
Port 4 direction register	DDR4	R/W	0b00000000
Port 6 data register	PDR6	R, RM/W	0b00000000
Port 6 direction register	DDR6	R/W	0b00000000
Port 7 data register	PDR7	R, RM/W	0b00000000
Port 7 direction register	DDR7	R/W	0b00000000
Port F data register	PDRF	R, RM/W	0b00000000
Port F direction register	DDRF	R/W	0b00000000
Port G data register	PDRG	R, RM/W	0b00000000
Port G direction register	DDRG	R/W	0b00000000
Port 0 pull-up register	PUL0	R/W	0b00000000
Port 1 pull-up register	PUL1	R/W	0b00000000
Port 4 pull-up register	PUL4	R/W	0b00000000
Port 6 pull-up register	PUL6	R/W	0b00000000
Port 7 pull-up register	PUL7	R/W	0b00000000
Port G pull-up register	PULG	R/W	0b00000000
A/D input disable register (lower)	AIDRL	R/W	0b00000000
Touch input disable register 0	TIDR0	R/W	0b00000000
Touch input disable register 1	TIDR1	R/W	0b00000000

R/W : Readable/writable (The read value is the same as the write value.)

R, RM/W : Readable/writable (The read value is different from the write value. The write value is read by the read-modify-write (RMW) type of instruction.)

14.2.1 Port 0

Port 0 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

1. Port 0 configuration

■ Port 0 is made up of the following elements.
- ❒ General-purpose I/O pins/peripheral function I/O pins
- ❒ Port 0 data register (PDR0)
- ❒ Port 0 direction register (DDR0)
- ❒ Port 0 pull-up register (PUL0)
- ❒ A/D input disable register (lower) (AIDRL)

2. Block diagrams of port 0

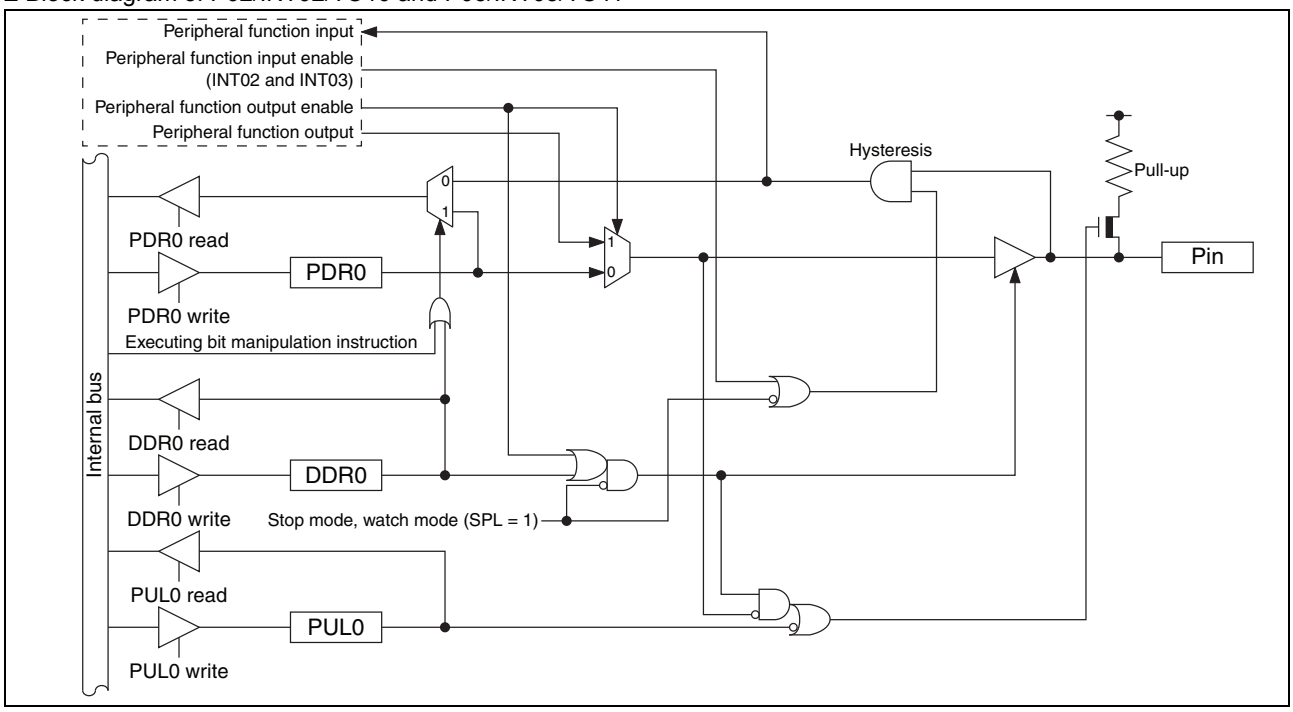
■ P02/INT02/TO10 pin

This pin has the following peripheral functions:
- ❒ External interrupt input pin (INT02)
- ❒ 8/16-bit composite timer ch. 1 output pin (TO10)

■ P03/INT03/TO11 pin

This pin has the following peripheral functions:
- ❒ External interrupt input pin (INT03)
- ❒ 8/16-bit composite timer ch. 1 output pin (TO11)

■ Block diagram of P02/INT02/TO10 and P03/INT03/TO11



■ P04/AN00/BEEP/DIO01 pin

This pin has the following peripheral functions:

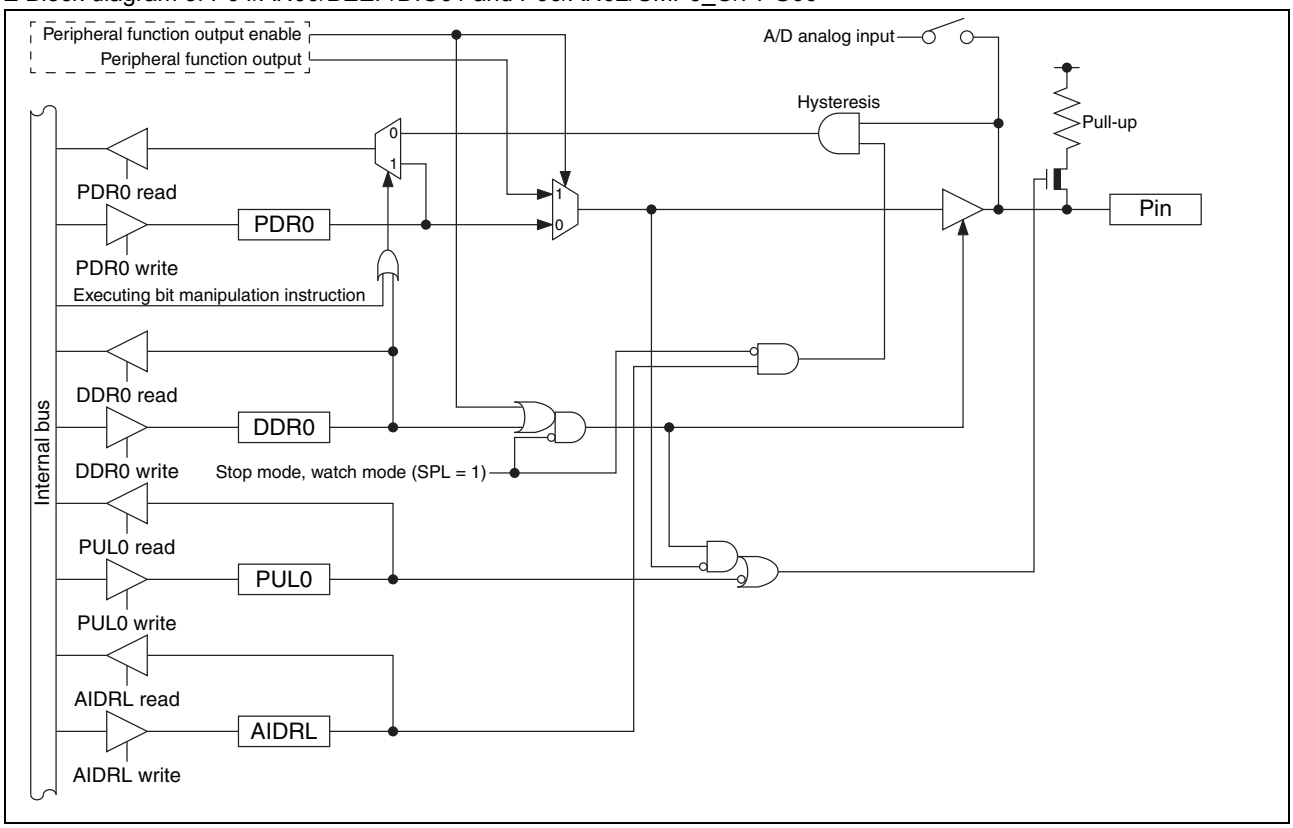
- ❒ 8/10-bit A/D converter analog input pin (AN00)
- ❒ Beep output pin (BEEP)
- ❒ TS direct output ch. 1 pin (DIO01)

■ P06/AN02/CMP0_O/PPG00 pin

This pin has the following peripheral functions:

- ❒ 8/10-bit A/D converter analog input pin (AN02)
- ❒ Comparator ch. 0 digital output pin (CMP0_O)
- ❒ 8/16-bit PPG ch. 0 output pin (PPG00)

■ Block diagram of P04/AN00/BEEP/DIO01 and P06/AN02/CMP0_O/PPG00

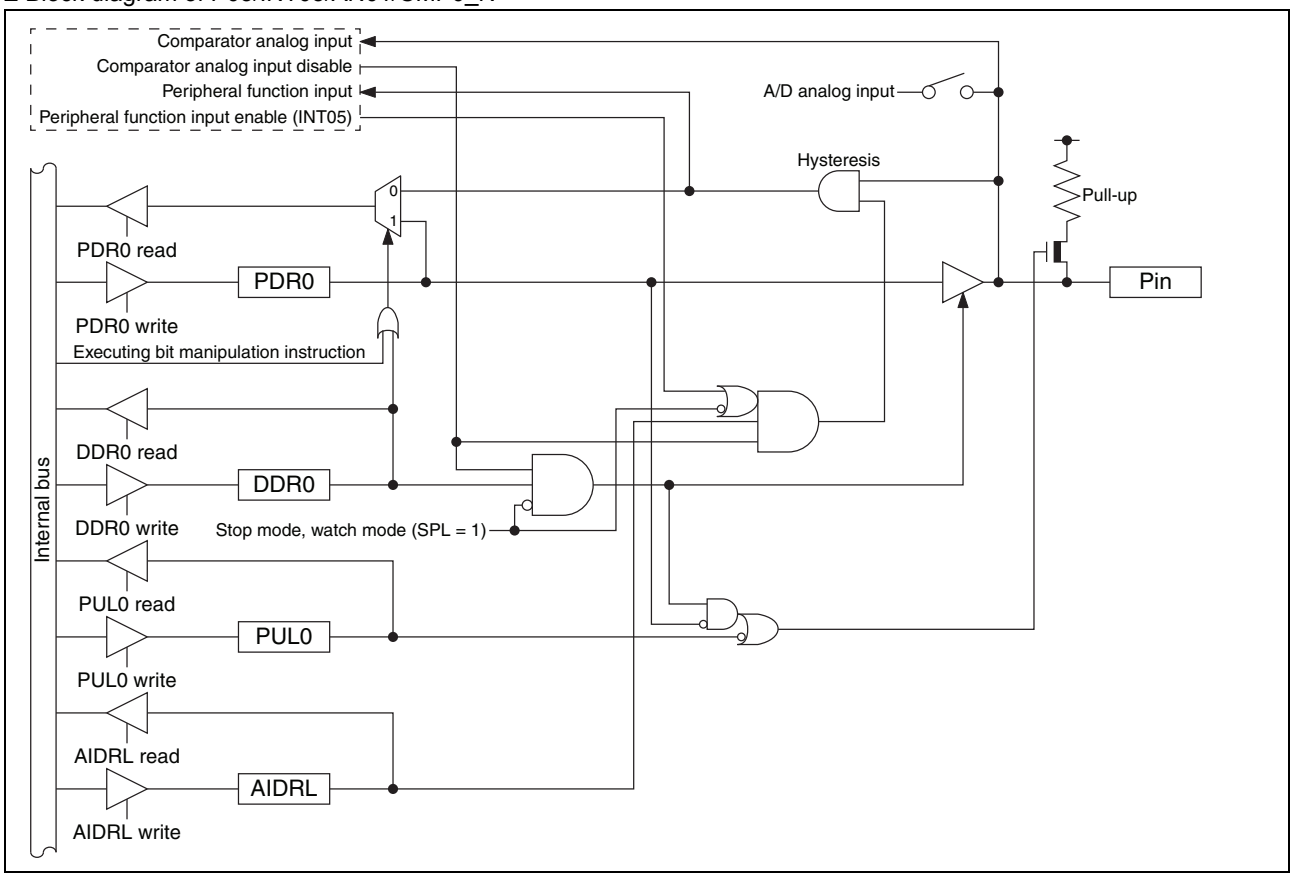


■ P05/INT05/AN01/CMP0_N pin

This pin has the following peripheral functions:

- ❒ External interrupt input pin (INT05)
- ❒ 8/10-bit A/D converter analog input pin (AN01)
- ❒ Comparator ch. 0 inverting analog input (negative input) pin (CMP0_N)

■ Block diagram of P05/INT05/AN01/CMP0_N

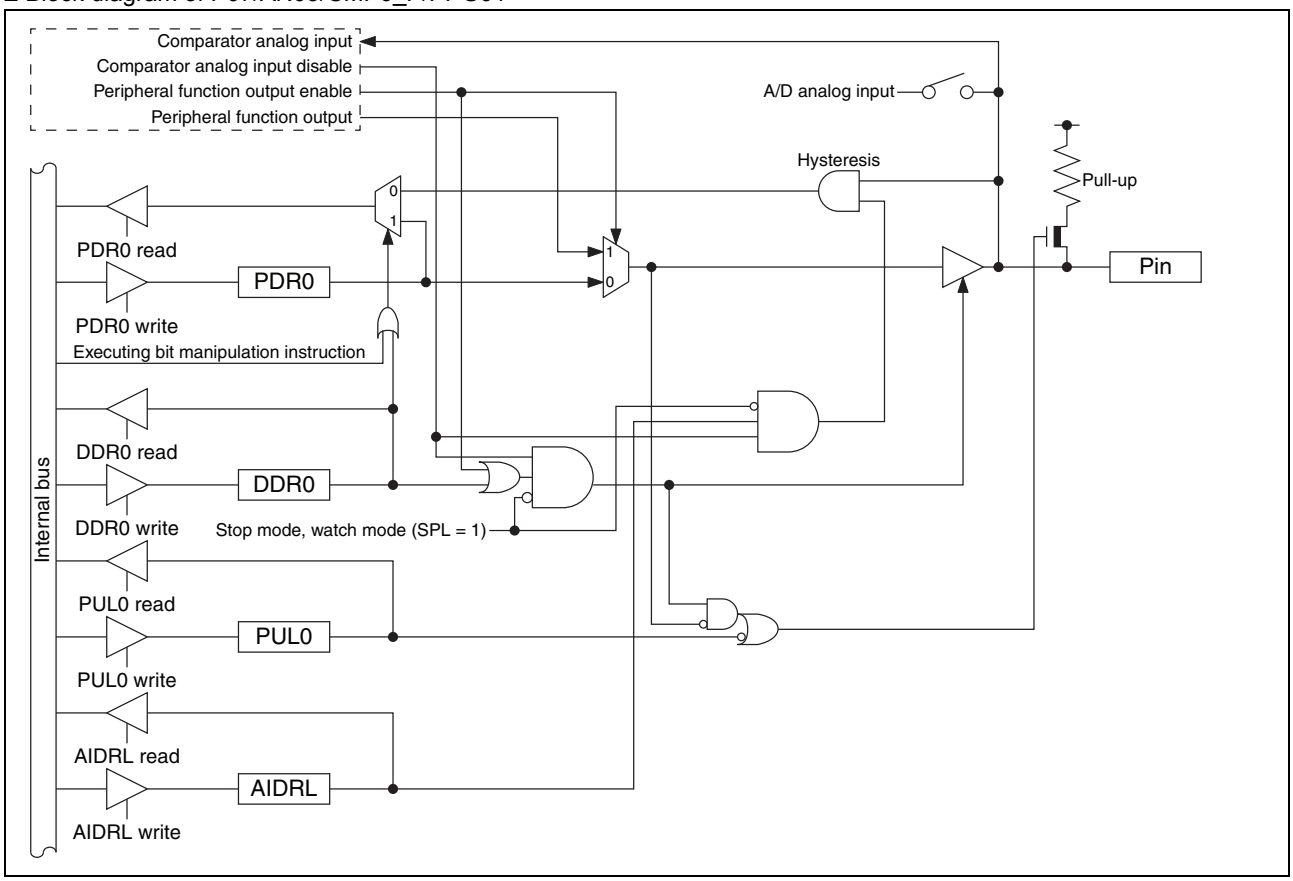


■ P07/AN03/CMP0_P/PPG01 pin

This pin has the following peripheral functions:

- ❒ 8/10-bit A/D converter analog input pin (AN03)
- ❒ Comparator ch. 0 non-inverting analog input (positive input) pin (CMP0_P)
- ❒ 8/16-bit PPG ch. 0 output pin (PPG01)

■ Block diagram of P07/AN03/CMP0_P/PPG01



3. Port 0 registers

■ Port 0 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR0	0	Pin state is “L” level.	PDR0 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR0 value is “1”.	As output port, outputs “H” level.
DDR0	0	Port input enabled		
	1	Port output enabled		
PUL0	0	Pull-up disabled		
	1	Pull-up enabled		
AIDRL	0	Analog input enabled		
	1	Port input enabled		

■ Correspondence between registers and pins for port 0

Pin name	Correspondence between related register bits and pins							
	P07	P06	P05	P04	P03	P02	-	-
PDR0	bit7	bit6	bit5	bit4	bit3	bit2	-	-
DDR0								
PUL0								
AIDRL	bit5	bit4	bit1	bit0	-	-		

4. Port 0 operations

■ Operation as an output port
- ❒ A pin becomes an output port if the bit in the DDR0 register corresponding to that pin is set to “1”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ When a pin is used as an output port, it outputs the value of the PDR0 register to external pins.
- ❒ If data is written to the PDR0 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
- ❒ Reading the PDR0 register returns the PDR0 register value.

■ Operation as an input port
- ❒ A pin becomes an input port if the bit in the DDR0 register corresponding to that pin is set to “0”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ When using a pin shared with the analog input function as an input port, set the bit in the A/D input disable register (lower) (AIDRL) corresponding to that pin to “1”.
- ❒ If data is written to the PDR0 register, the value is stored in the output latch but is not output to the pin set as an input port.
- ❒ Reading the PDR0 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR0 register, the PDR0 register value is returned.

■ Operation as a peripheral function output pin
- ❒ A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
- ❒ The pin value can be read from the PDR0 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR0 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR0 register, the PDR0 register value is returned.

■ Operation as a peripheral function input pin
- ❒ To set a pin as an input port, set the bit in the DDR0 register corresponding to the input pin of a peripheral function to “0”.
- ❒ When using a pin shared with the analog input function as another peripheral function input pin, configure it as an input port by setting the bit in the AIDRL register corresponding to that pin to “1”.
- ❒ Reading the PDR0 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR0 register, the PDR0 register value is returned.

■ Operation at reset

If the CPU is reset, all bits in the DDR0 register are initialized to “0” and port input is enabled. As for a pin shared with the analog input function, its port input is disabled because the AIDRL register is initialized to “0”.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR0 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open. However, if the interrupt input is enabled for the external interrupt (INT02, INT03 and INT05), the input is enabled and not blocked.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.
- Operation as an analog input pin
  - Set the bit in the DDR0 register bit corresponding to the analog input pin to “0” and the bit corresponding to that pin in the AIDRL register to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions. In addition, set the corresponding bit in the PUL0 register to “0”.
- Operation as an external interrupt input pin
  - Set the bit in the DDR0 register corresponding to the external interrupt input pin to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - The pin value is always input to the external interrupt circuit. When using a pin for a function other than the interrupt, disable the external interrupt function corresponding to that pin.
- Operation of the pull-up register

Setting the bit in the PUL0 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL0 register.

- Operation as a comparator input pin
  - Set the bit in the AIDRL register corresponding to the comparator input pin to “0”.
  - Regardless of the value of the PDR0 register and that of the DDR0 register, if the comparator analog input enable bit in the comparator control register ch. 0 (CMR0:VCID) is set to “0”, the comparator input function is enabled.
  - To disable the comparator input function, set the VCID bit to “1”.
  - For details of the comparator, refer to “CHAPTER 25 COMPARATOR” in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

14.2.2 Port 1

Port 1 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

1. Port 1 configuration

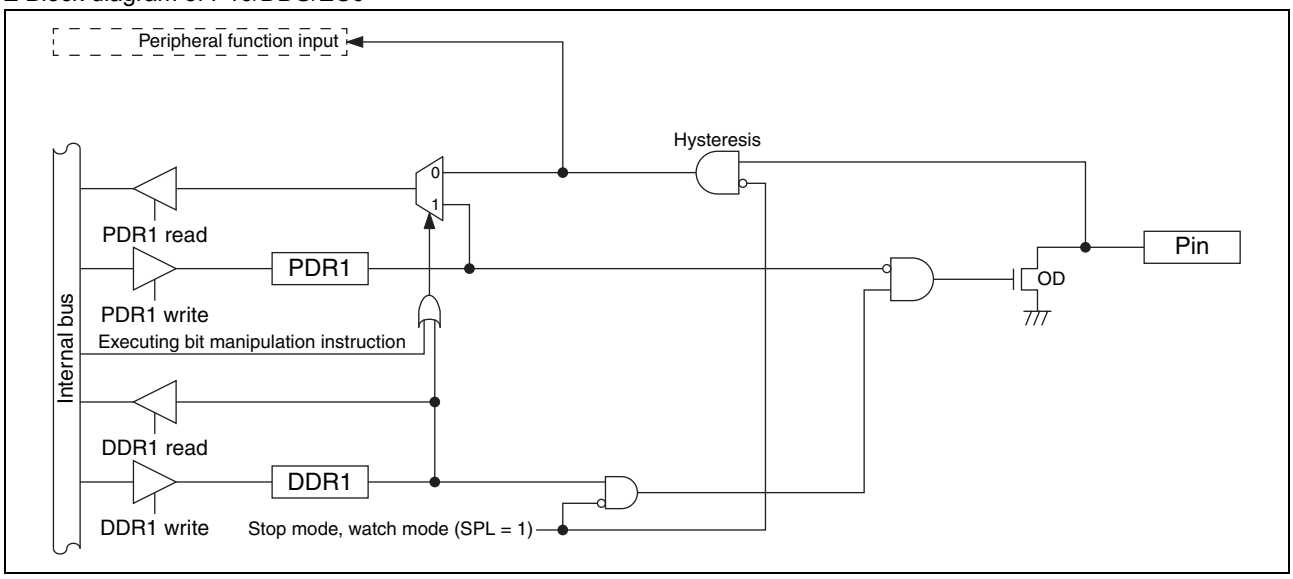
■ Port 1 is made up of the following elements.
- ❒ General-purpose I/O pins/peripheral function I/O pins
- ❒ Port 1 data register (PDR1)
- ❒ Port 1 direction register (DDR1)
- ❒ Port 1 pull-up register (PUL1)

2. Block diagrams of port 1

■ P10/DBG/EC0 pin

This pin has the following peripheral functions:
- ❒ DBG input pin (DBG)
- ❒ 8/16-bit composite timer ch. 0 clock input pin (EC0)

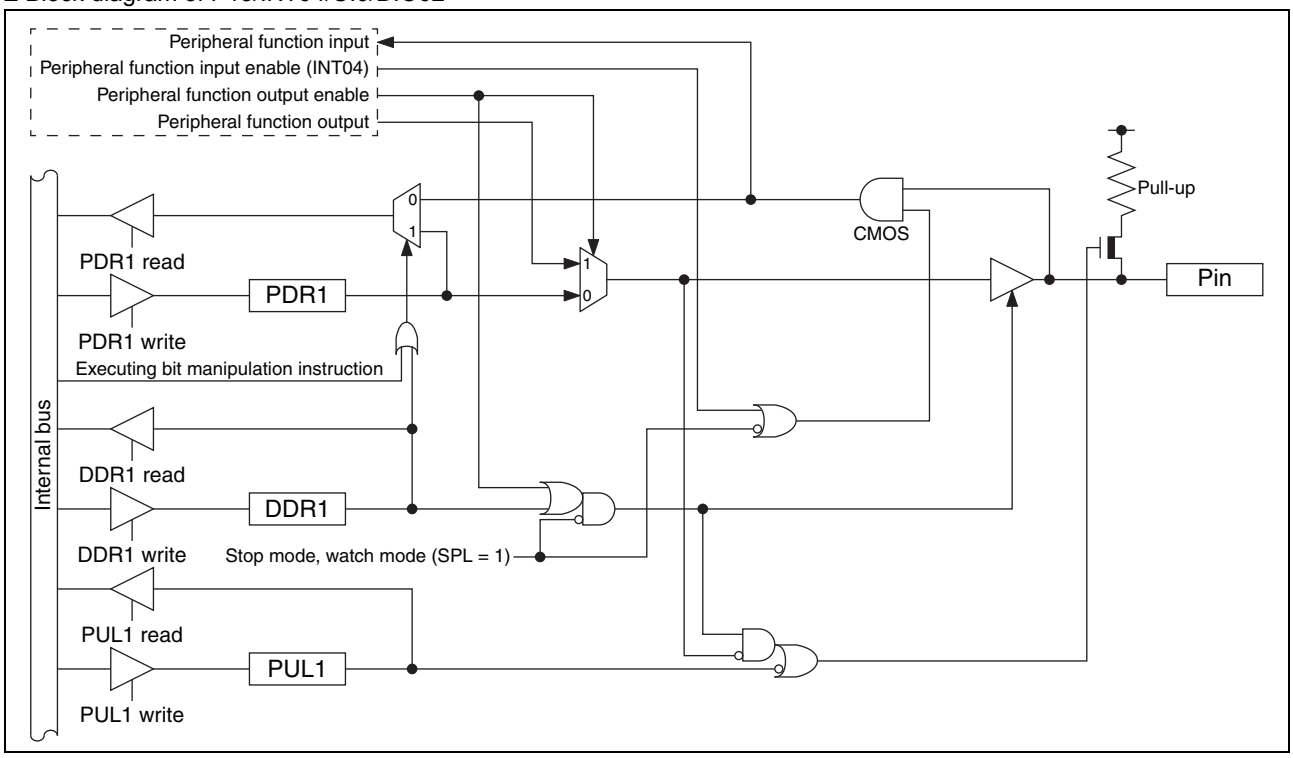
■ Block diagram of P10/DBG/EC0



■ P13/INT04/UI0/DIO02 pin

This pin has the following peripheral functions:
- ❒ External interrupt input pin (INT04)
- ❒ UART/SIO ch. 0 data input pin (UI0)
- ❒ TS direct output ch. 2 pin (DIO02)

■ Block diagram of P13/INT04/UI0/DIO02



■ P14/INT01/UO0 pin

This pin has the following peripheral functions:

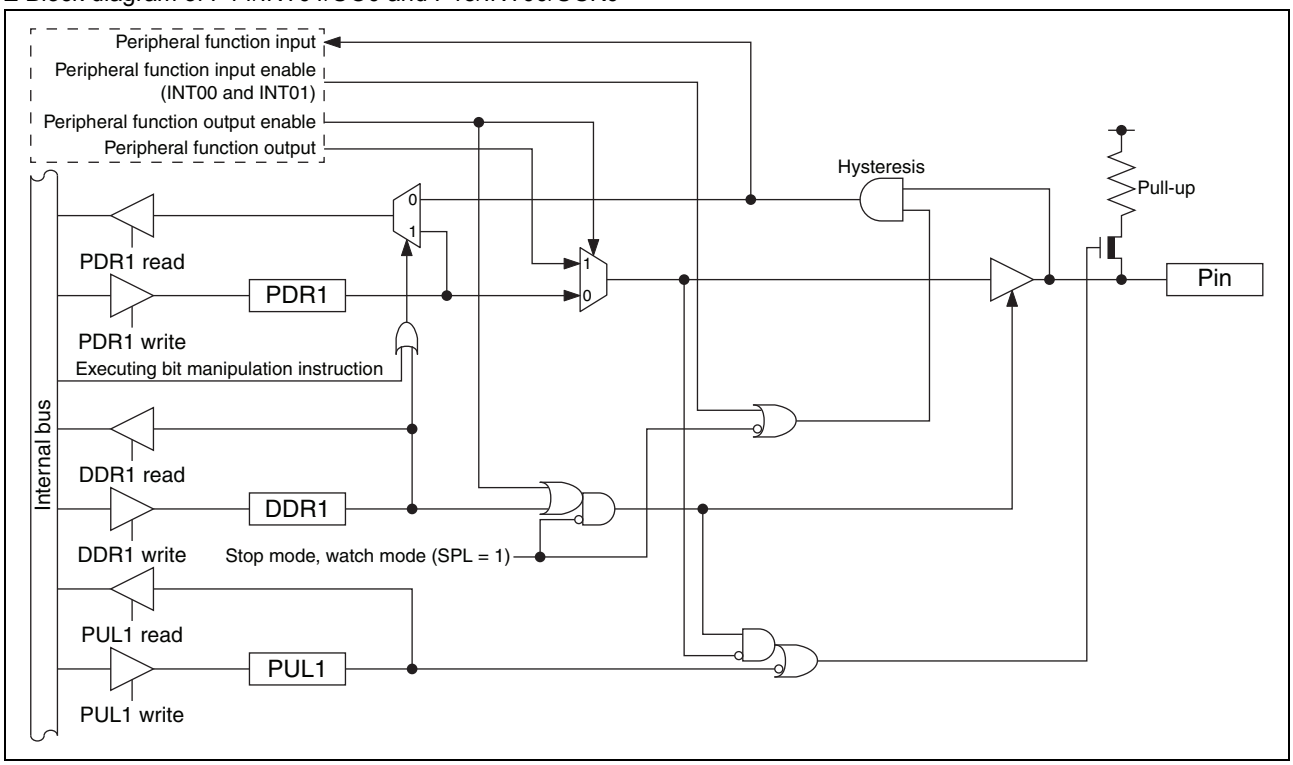
- ❒ External interrupt input pin (INT01)
- ❒ UART/SIO ch. 0 data output pin (UO0)

■ P15/INT00/UCK0 pin

This pin has the following peripheral functions:

- ❒ External interrupt input pin (INT00)
- ❒ UART/SIO ch. 0 clock I/O pin (UCK0)

■ Block diagram of P14/INT01/UO0 and P15/INT00/UCK0



3. Port 1 registers

■ Port 1 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR1	0	Pin state is “L” level.	PDR1 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR1 value is “1”.	As output port, outputs “H” level.*
DDR1	0	Port input enabled		
	1	Port output enabled		
PUL1	0	Pull-up disabled		
	1	Pull-up enabled		

*: If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

■ Correspondence between registers and pins for port 1

Pin name	Correspondence between related register bits and pins							
	-	-	P15	P14	P13	-	-	P10
PDR1	-	-	bit5	bit4	bit3	-	-	bit0*
DDR1								
PUL1								

*: Though P10 has no pull-up function, bit0 in the PUL1 register can still be accessed. The operation of P10 is not affected by the setting of bit0 in the PUL1 register.

4. Port 1 operations

■ Operation as an output port
- ❒ A pin becomes an output port if the bit in the DDR1 register corresponding to that pin is set to “1”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ When a pin is used as an output port, it outputs the value of the PDR1 register to external pins.
- ❒ If data is written to the PDR1 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
- ❒ Reading the PDR1 register returns the PDR1 register value.

■ Operation as an input port
- ❒ A pin becomes an input port if the bit in the DDR1 register corresponding to that pin is set to “0”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ If data is written to the PDR1 register, the value is stored in the output latch but is not output to the pin set as an input port.
- ❒ Reading the PDR1 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR1 register, the PDR1 register value is returned.

■ Operation as a peripheral function output pin
- ❒ A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
- ❒ The pin value can be read from the PDR1 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR1 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR1 register, the PDR1 register value is returned.

■ Operation as a peripheral function input pin
- ❒ To set a pin as an input port, set the bit in the DDR1 register corresponding to the input pin of a peripheral function to “0”.
- ❒ Reading the PDR1 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR1 register, the PDR1 register value is returned.

■ Operation at reset

If the CPU is reset, all bits in the DDR1 register are initialized to “0” and port input is enabled.

■ Operation in stop mode and watch mode
- ❒ If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR1 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open. However, if the interrupt input from the external interrupt (INT00, INT01 and INT04) is enabled, or if the interrupt input of P10/DBG/EC0 is enabled by the external interrupt control register ch. 0 (EIC00) of the external interrupt circuit and the interrupt pin selection circuit control register (WICR) of the interrupt pin selection circuit, the input is enabled and is not blocked.
- ❒ If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

■ Operation as an external interrupt input pin
- ❒ Set the bit in the DDR1 register corresponding to the external interrupt input pin to “0”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ The pin value is always input to the external interrupt circuit. When using a pin for a function other than the interrupt, disable the external interrupt function corresponding to that pin.

■ Operation of the pull-up register

Setting the bit in the PUL1 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL1 register.

14.2.3 Port 4

Port 4 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

1. Port 4 configuration

■ Port 4 is made up of the following elements.
- ❒ General-purpose I/O pins/peripheral function I/O pins
- ❒ Port 4 data register (PDR4)
- ❒ Port 4 direction register (DDR4)
- ❒ Port 4 pull-up register (PUL4)
- ❒ A/D input disable register (lower) (AIDRL)

2. Block diagrams of port 4

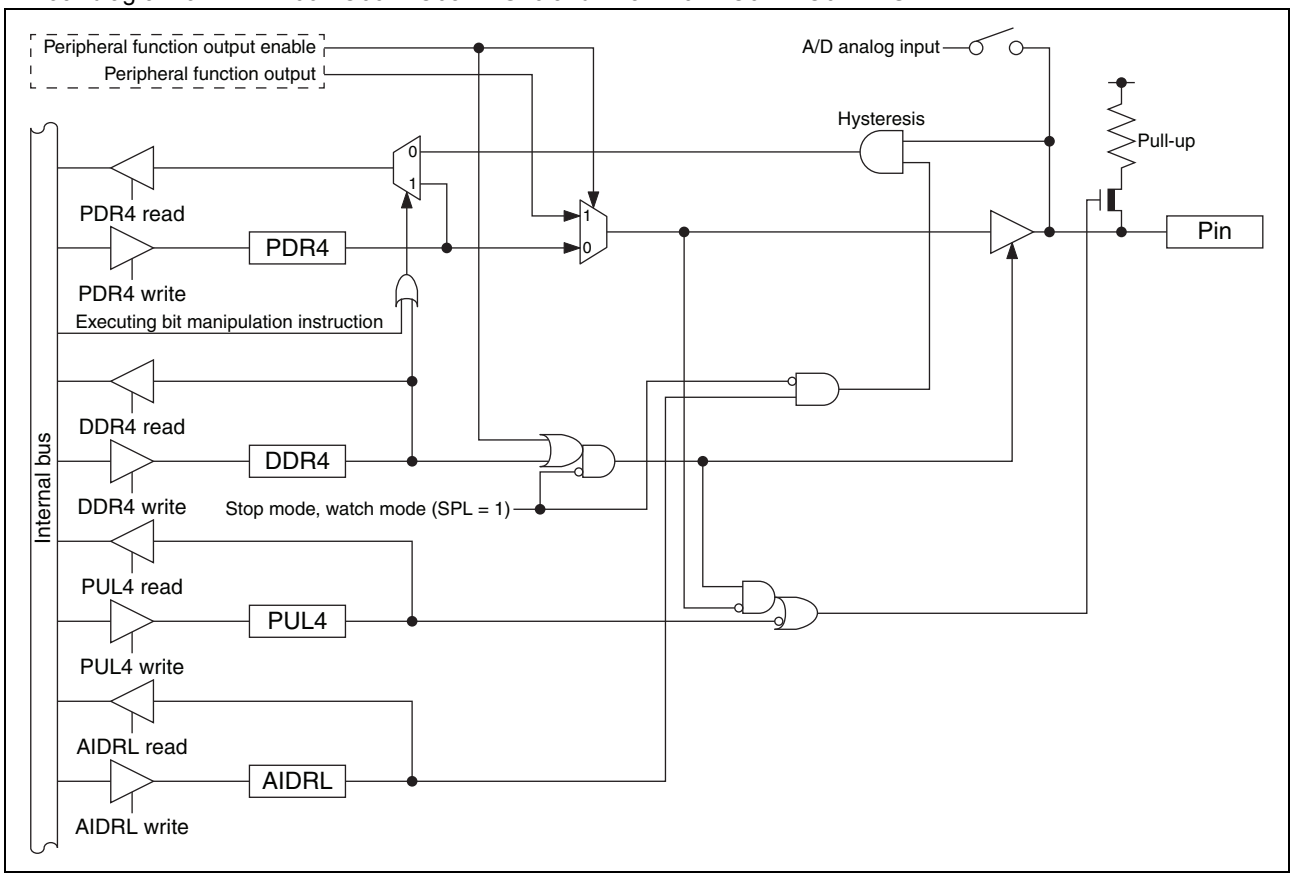
■ P44/AN06/TO00/DIO03/PPG10 pin

This pin has the following peripheral functions:
- ❒ 8/10-bit A/D converter analog input pin (AN06)
- ❒ 8/16-bit composite timer ch. 0 output pin (TO00)
- ❒ TS direct output ch. 3 pin (DIO03)
- ❒ 8/16-bit PPG ch. 1 output pin (PPG10)

■ P45/AN07/TO01/DIO04/PPG11 pin

This pin has the following peripheral functions:
- ❒ 8/10-bit A/D converter analog input pin (AN07)
- ❒ 8/16-bit composite timer ch. 0 output pin (TO01)
- ❒ TS direct output ch. 4 pin (DIO04)
- ❒ 8/16-bit PPG ch. 1 output pin (PPG11)

■ Block diagram of P44/AN06/TO00/DIO03/PPG10 and P45/AN07/TO01/DIO04/PPG11



■ P46/INT06/SDA pin

This pin has the following peripheral functions:

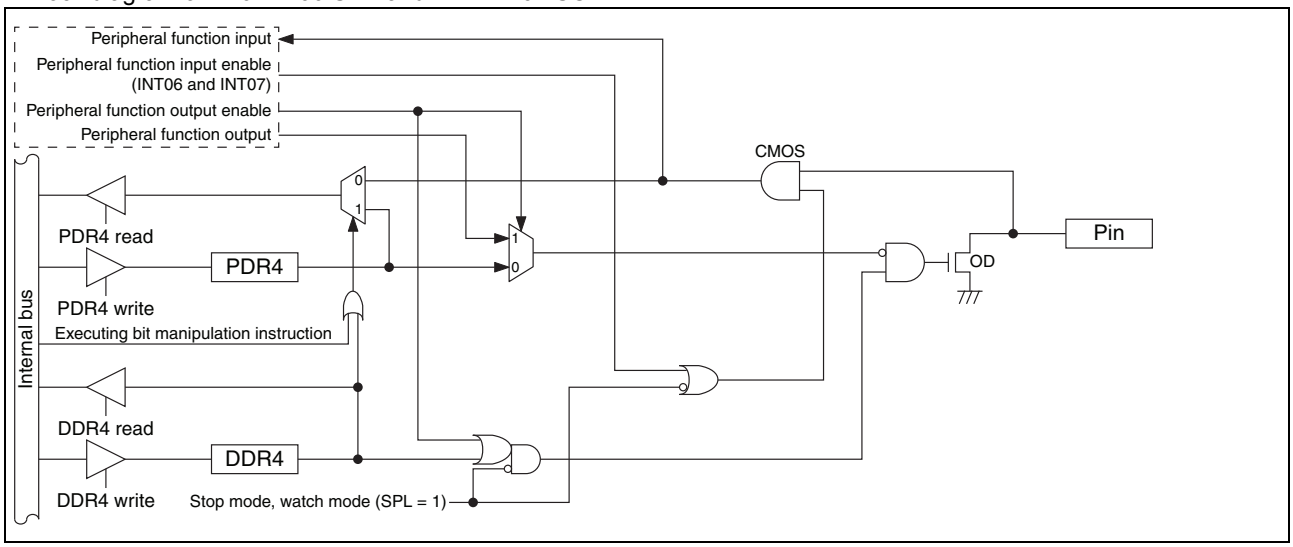
- ❒ External interrupt input pin (INT06)
- ❒ I^2C bus interface ch. 0 data I/O pin (SDA)

■ P47/INT07/SCL pin

This pin has the following peripheral functions:

- ❒ External interrupt input pin (INT07)
- ❒ I^2C bus interface ch. 0 clock I/O pin (SCL)

■ Block diagram of P46/INT06/SDA and P47/INT07/SCL



3. Port 4 registers

■ Port 4 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR4	0	Pin state is “L” level.	PDR4 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR4 value is “1”.	As output port, outputs “H” level.*
DDR4	0	Port input enabled		
	1	Port output enabled		
PUL4	0	Pull-up disabled		
	1	Pull-up enabled		
AIDRL	0	Analog input enabled		
	1	Port input enabled		

*: If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

■ Correspondence between registers and pins for port 4

Pin name	Correspondence between related register bits and pins							
	P47	P46	P45	P44	-	-	-	-
PDR4	bit7	bit6	bit5	bit4	-	-	-	-
DDR4								
PUL4	-	-						
AIDRL			bit7	bit6				

4. Port 4 operations

■ Operation as an output port
- ❒ A pin becomes an output port if the bit in the DDR4 register corresponding to that pin is set to “1”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ When a pin is used as an output port, it outputs the value of the PDR4 register to external pins.
- ❒ If data is written to the PDR4 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
- ❒ Reading the PDR4 register returns the PDR4 register value.

■ Operation as an input port
- ❒ A pin becomes an input port if the bit in the DDR4 register corresponding to that pin is set to “0”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ When using a pin shared with the analog input function as an input port, set the bit in the A/D input disable register (lower) (AIDRL) corresponding to that pin to “1”.
- ❒ If data is written to the PDR4 register, the value is stored in the output latch but is not output to the pin set as an input port.
- ❒ Reading the PDR4 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR4 register, the PDR4 register value is returned.

■ Operation as a peripheral function output pin
- ❒ A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
- ❒ The pin value can be read from the PDR4 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR4 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR4 register, the PDR4 register value is returned.

■ Operation as a peripheral function input pin
- ❒ To set a pin as an input port, set the bit in the DDR4 register corresponding to the input pin of a peripheral function to “0”.
- ❒ When using a pin shared with the analog input function as another peripheral function input pin, configure it as an input port by setting the bit in the AIDRL register corresponding to that pin to “1”.
- ❒ Reading the PDR4 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR4 register, the PDR4 register value is returned.

■ Operation at reset

If the CPU is reset, all bits in the DDR4 register are initialized to “0” and port input is enabled. As for a pin shared with the analog input function, its port input is disabled because the AIDRL register is initialized to “0”.

■ Operation in stop mode and watch mode
- ❒ If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR4 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open. However, if the interrupt input is enabled for the external interrupt (INT06 and INT07), the input is enabled and not blocked.
- ❒ If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

■ Operation as an analog input pin
- ❒ Set the bit in the DDR4 register bit corresponding to the analog input pin to “0” and the bit corresponding to that pin in the AIDRL register to “0”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions. In addition, set the corresponding bit in the PUL4 register to “0”.

■ Operation as an external interrupt input pin
- ❒ Set the bit in the DDR4 register corresponding to the external interrupt input pin to “0”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ The pin value is always input to the external interrupt circuit. When using a pin for a function other than the interrupt, disable the external interrupt function corresponding to that pin.

■ Operation of the pull-up register

Setting the bit in the PUL4 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL4 register.

14.2.4 Port 6

Port 6 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

1. Port 6 configuration

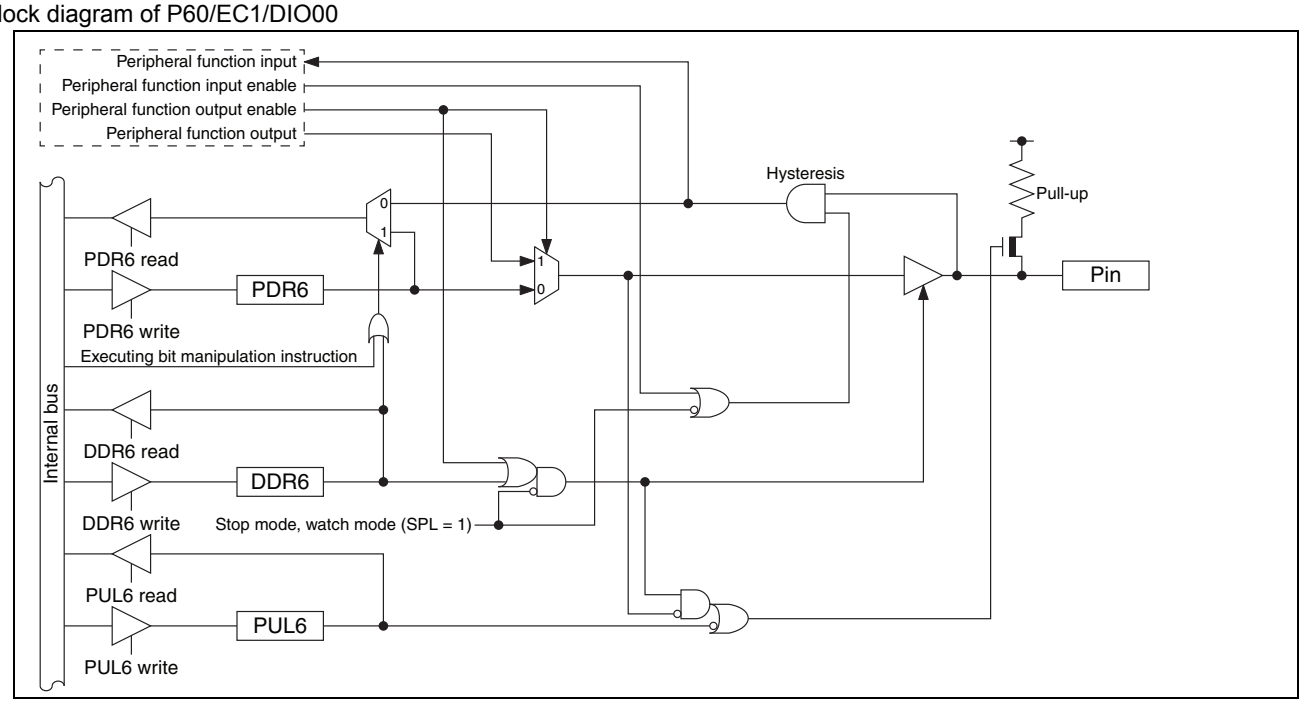
■ Port 6 is made up of the following elements.
- ❒ General-purpose I/O pins/peripheral function I/O pins
- ❒ Port 6 data register (PDR6)
- ❒ Port 6 direction register (DDR6)
- ❒ Port 6 pull-up register (PUL6)
- ❒ Touch input disable register 0 (TIDR0)

2. Block diagrams of port 6

■ P60/EC1/DIO00 pin

This pin has the following peripheral functions:
- ❒ 8/16-bit composite timer ch. 1 clock input pin (EC1)
- ❒ TS direct output ch. 0 pin (DIO00)

■ Block diagram of P60/EC1/DIO00



■ P63/AREF pin

This pin has the following peripheral function:
- ❒ TS reference input pin (AREF)

■ P64/S00 pin

This pin has the following peripheral function:
- ❒ TS touch ch. 0 input pin (S00)

■ P65/S01 pin

This pin has the following peripheral function:
- ❒ TS touch ch. 1 input pin (S01)

■ P66/S02 pin

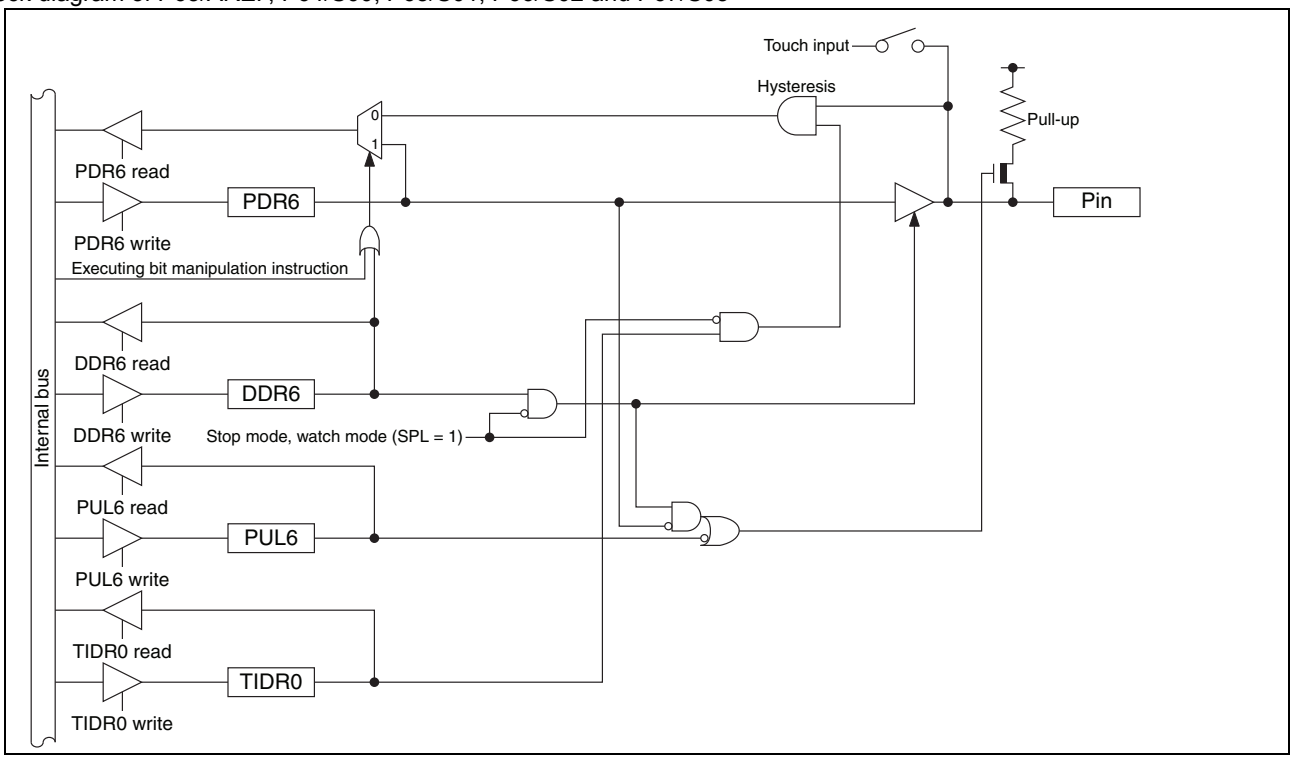
This pin has the following peripheral function:
- ❒ TS touch ch. 2 input pin (S02)

■ P67/S03 pin

This pin has the following peripheral function:

❒ TS touch ch. 3 input pin (S03)

■ Block diagram of P63/AREF, P64/S00, P65/S01, P66/S02 and P67/S03



3. Port 6 registers

■ Port 6 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR6	0	Pin state is “L” level.	PDR6 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR6 value is “1”.	As output port, outputs “H” level.
DDR6	0	Port input enabled		
	1	Port output enabled		
PUL6	0	Pull-up disabled		
	1	Pull-up enabled		
TIDR0	0	Touch input or reference input enabled		
	1	Port input enabled		

■ Correspondence between registers and pins for port 6

Pin name	Correspondence between related register bits and pins							
	P67	P66	P65	P64	P63	-	-	P60
PDR6	bit7	bit6	bit5	bit4	bit3	-	-	bit0
DDR6								
PUL6								
TIDR0	bit7	bit6	bit5	bit4	bit3			-

4. Port 6 operations

■ Operation as an output port
- ❒ A pin becomes an output port if the bit in the DDR6 register corresponding to that pin is set to “1”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ When a pin is used as an output port, it outputs the value of the PDR6 register to external pins.
- ❒ If data is written to the PDR6 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
- ❒ Reading the PDR6 register returns the PDR6 register value.

■ Operation as an input port
- ❒ A pin becomes an input port if the bit in the DDR6 register corresponding to that pin is set to “0”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ When using a pin shared with the touch input function as an input port, set the bit in the touch input disable register 0 (TIDR0) corresponding to that pin to “1”.
- ❒ If data is written to the PDR6 register, the value is stored in the output latch but is not output to the pin set as an input port.
- ❒ Reading the PDR6 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR6 register, the PDR6 register value is returned.

■ Operation as a peripheral function output pin
- ❒ A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
- ❒ The pin value can be read from the PDR6 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR6 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR6 register, the PDR6 register value is returned.

■ Operation as a peripheral function input pin
- ❒ To set a pin as an input port, set the bit in the DDR6 register corresponding to the input pin of a peripheral function to “0”.
- ❒ Reading the PDR6 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR6 register, the PDR6 register value is returned.

■ Operation at reset

If the CPU is reset, all bits in the DDR6 register are initialized to “0” and port input is enabled. As for a pin shared with the touch input function, its port input is disabled because the TIDR0 register is initialized to “0”.

■ Operation in stop mode and watch mode
- ❒ If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR6 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open. However, if the interrupt input of P60/EC1/DIO00 is enabled by the external interrupt control register ch. 0 (EIC00) of the external interrupt circuit and the interrupt pin selection circuit control register (WICR) of the interrupt pin selection circuit, the input is enabled and is not blocked.
- ❒ When the stop enable bit in the TS prescaler control register (PSC:STPE) is set to “1”, the TS can operate in stop mode or watch mode, the touch input is enabled and is not blocked. The TS wakes up in stop mode or watch mode provided that the TINT (touch interrupt) and the GINT (general interrupt) are set to enable the TS to wake up in stop mode or watch mode.
- ❒ If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

■ Operation as a touch input pin

Set the bit in the DDR6 register corresponding to the touch input pin to “0”, the bit in the TIDR0 register corresponding to the same pin to “0”, and the bit in the PUL6 register corresponding to the same pin to “0”.

■ Operation of the pull-up register

Setting the bit in the PUL6 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL6 register.

14.2.5 Port 7

Port 7 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

1. Port 7 configuration

■ Port 7 is made up of the following elements.
- ❒ General-purpose I/O pins/peripheral function I/O pins
- ❒ Port 7 data register (PDR7)
- ❒ Port 7 direction register (DDR7)
- ❒ Port 7 pull-up register (PUL7)
- ❒ Touch input disable register 1 (TIDR1)

2. Block diagrams of port 7

■ P70/S04 pin

This pin has the following peripheral function:
- ❒ TS touch ch. 4 input pin (S04)

■ P71/S05 pin

This pin has the following peripheral function:
- ❒ TS touch ch. 5 input pin (S05)

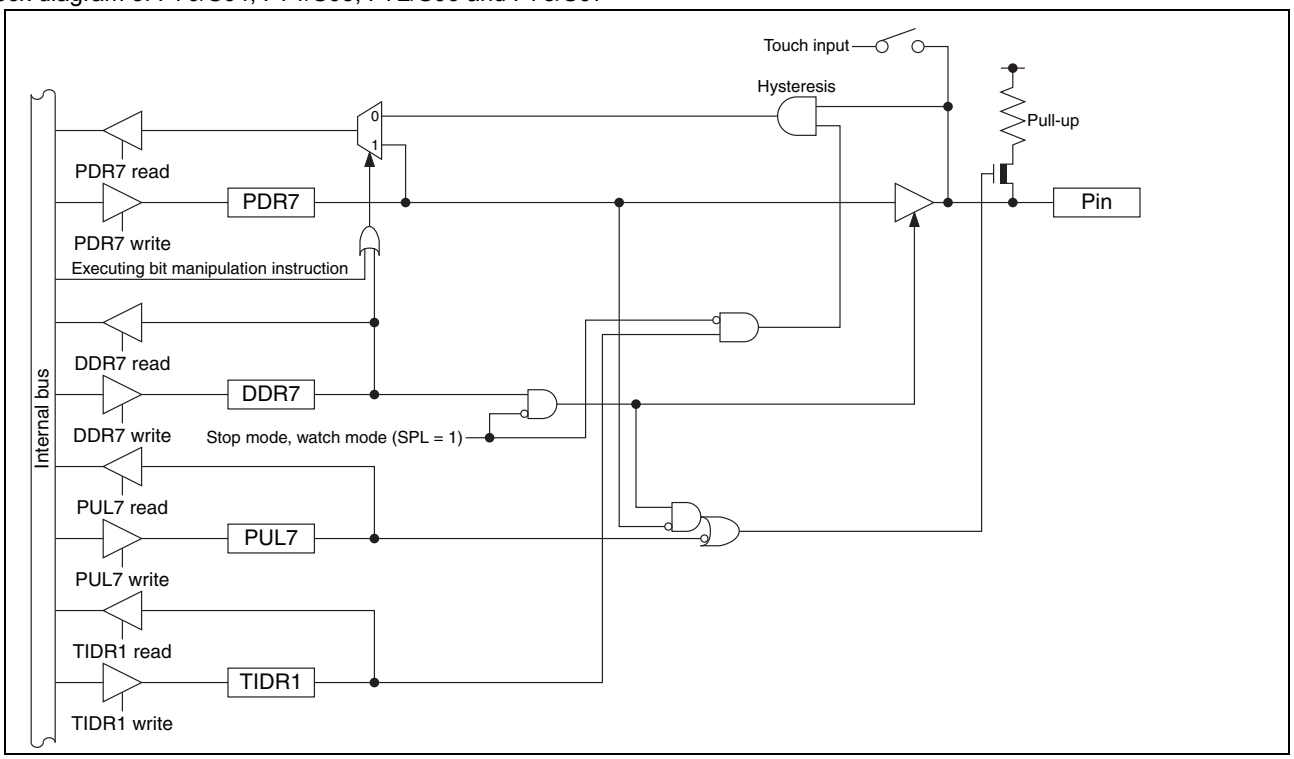
■ P72/S06 pin

This pin has the following peripheral function:
- ❒ TS touch ch. 6 input pin (S06)

■ P73/S07 pin

This pin has the following peripheral function:
- ❒ TS touch ch. 7 input pin (S07)

■ Block diagram of P70/S04, P71/S05, P72/S06 and P73/S07



3. Port 7 registers

■ Port 7 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR7	0	Pin state is “L” level.	PDR7 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR7 value is “1”.	As output port, outputs “H” level.
DDR7	0	Port input enabled		
	1	Port output enabled		
PUL7	0	Pull-up disabled		
	1	Pull-up enabled		
TIDR1	0	Touch input enabled		
	1	Port input enabled		

■ Correspondence between registers and pins for port 7

Pin name	Correspondence between related register bits and pins							
	-	-	-	-	P73	P72	P71	P70
PDR7	-	-	-	-	bit3	bit2	bit1	bit0
DDR7								
PUL7								
TIDR1								

4. Port 7 operations

■ Operation as an output port
- ❒ A pin becomes an output port if the bit in the DDR7 register corresponding to that pin is set to “1”.
- ❒ When a pin is used as an output port, it outputs the value of the PDR7 register to external pins.
- ❒ If data is written to the PDR7 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
- ❒ Reading the PDR7 register returns the PDR7 register value.

■ Operation as an input port
- ❒ A pin becomes an input port if the bit in the DDR7 register corresponding to that pin is set to “0”.
- ❒ When using a pin shared with the touch input function as an input port, set the bit in the touch input disable register 1 (TIDR1) corresponding to that pin to “1”.
- ❒ If data is written to the PDR7 register, the value is stored in the output latch but is not output to the pin set as an input port.
- ❒ Reading the PDR7 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR7 register, the PDR7 register value is returned.

■ Operation at reset

If the CPU is reset, all bits in the DDR7 register are initialized to “0” and port input is enabled. As for a pin shared with the touch input function, its port input is disabled because the TIDR1 register is initialized to “0”.

■ Operation in stop mode and watch mode
- ❒ If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR7 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
- ❒ When the stop enable bit in the TS prescaler control register (PSC:STPE) is set to “1”, the TS can operate in stop mode or watch mode, the touch input is enabled and is not blocked. The TS wakes up in stop mode or watch mode provided that the TINT (touch interrupt) and the GINT (general interrupt) are set to enable the TS to wake up in stop mode or watch mode.
- ❒ If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

■ Operation as a touch input pin

Set the bit in the DDR7 register corresponding to the touch input pin to “0”, the bit in the TIDR1 register corresponding to the same pin to “0”, and the bit in the PUL7 register corresponding to the same pin to “0”.

■ Operation of the pull-up register

Setting the bit in the PUL7 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL7 register.

14.2.6 Port F

Port F is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

1. Port F configuration

■ Port F is made up of the following elements.
- ❒ General-purpose I/O pins/peripheral function I/O pins
- ❒ Port F data register (PDRF)
- ❒ Port F direction register (DDRF)

2. Block diagrams of port F

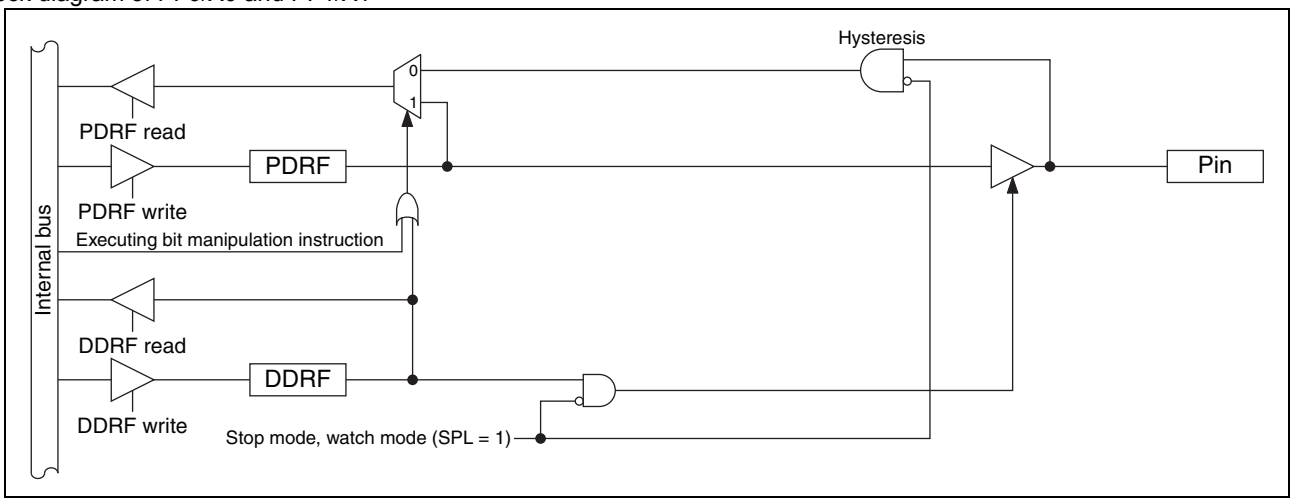
■ PF0/X0 pin

This pin has the following peripheral function:
- ❒ Main clock input oscillation pin (X0)

■ PF1/X1 pin

This pin has the following peripheral function:
- ❒ Main clock I/O oscillation pin (X1)

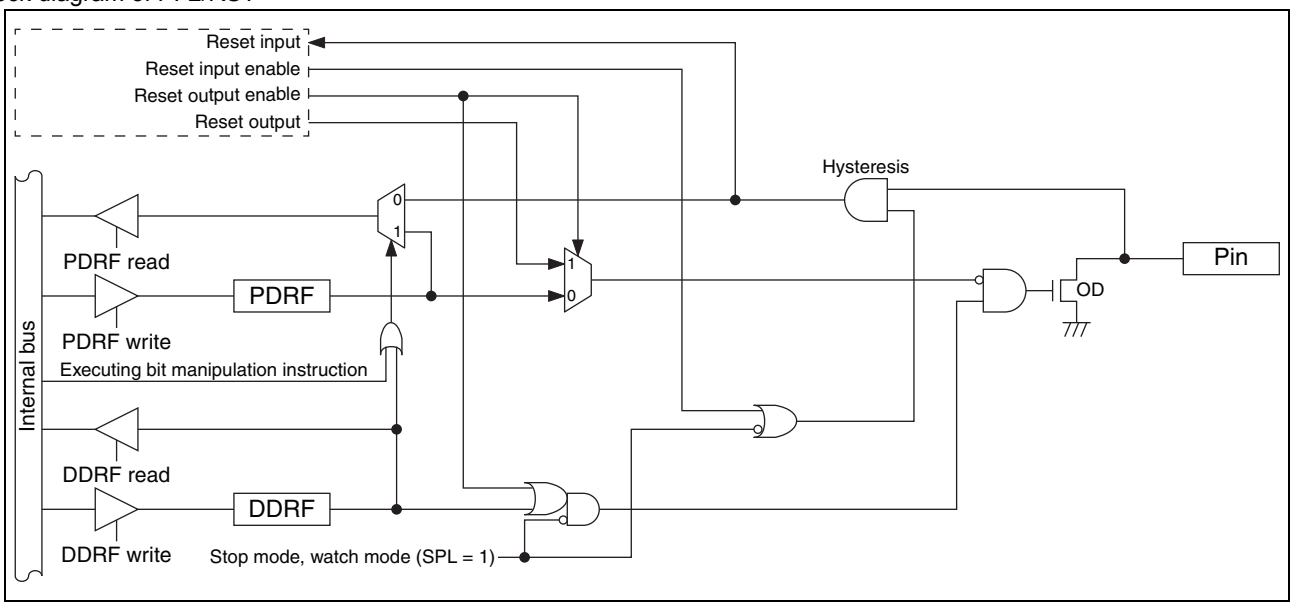
■ Block diagram of PF0/X0 and PF1/X1



■ PF2/$\overline{\text{RST}}$ pin

This pin has the following peripheral function:
- ❒ Reset pin ($\overline{\text{RST}}$)

■ Block diagram of PF2/$\overline{\text{RST}}$



3. Port F registers

■ Port F register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDRF	0	Pin state is “L” level.	PDRF value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDRF value is “1”.	As output port, outputs “H” level.*
DDRF	0	Port input enabled		
	1	Port output enabled		

*: If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

■ Correspondence between registers and pins for port F

Pin name	Correspondence between related register bits and pins							
	-	-	-	-	-	PF2	PF1	PF0
PDRF	-	-	-	-	-	bit2	bit1	bit0
DDRF								

4. Port F operations

■ Operation as an output port
- ❒ A pin becomes an output port if the bit in the DDRF register corresponding to that pin is set to “1”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ When a pin is used as an output port, it outputs the value of the PDRF register to external pins.
- ❒ If data is written to the PDRF register, the value is stored in the output latch and is output to the pin set as an output port as it is.
- ❒ Reading the PDRF register returns the PDRF register value.

■ Operation as an input port
- ❒ A pin becomes an input port if the bit in the DDRF register corresponding to that pin is set to “0”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ If data is written to the PDRF register, the value is stored in the output latch but is not output to the pin set as an input port.
- ❒ Reading the PDRF register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDRF register, the PDRF register value is returned.

■ Operation at reset

If the CPU is reset, all bits in the DDRF register are initialized to “0” and port input is enabled.

■ Operation in stop mode and watch mode
- ❒ If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRF register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
- ❒ If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

14.2.7 Port G

Port G is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

1. Port G configuration

■ Port G is made up of the following elements.
- ❒ General-purpose I/O pins/peripheral function I/O pins
- ❒ Port G data register (PDRG)
- ❒ Port G direction register (DDRG)
- ❒ Port G pull-up register (PULG)

2. Block diagram of port G

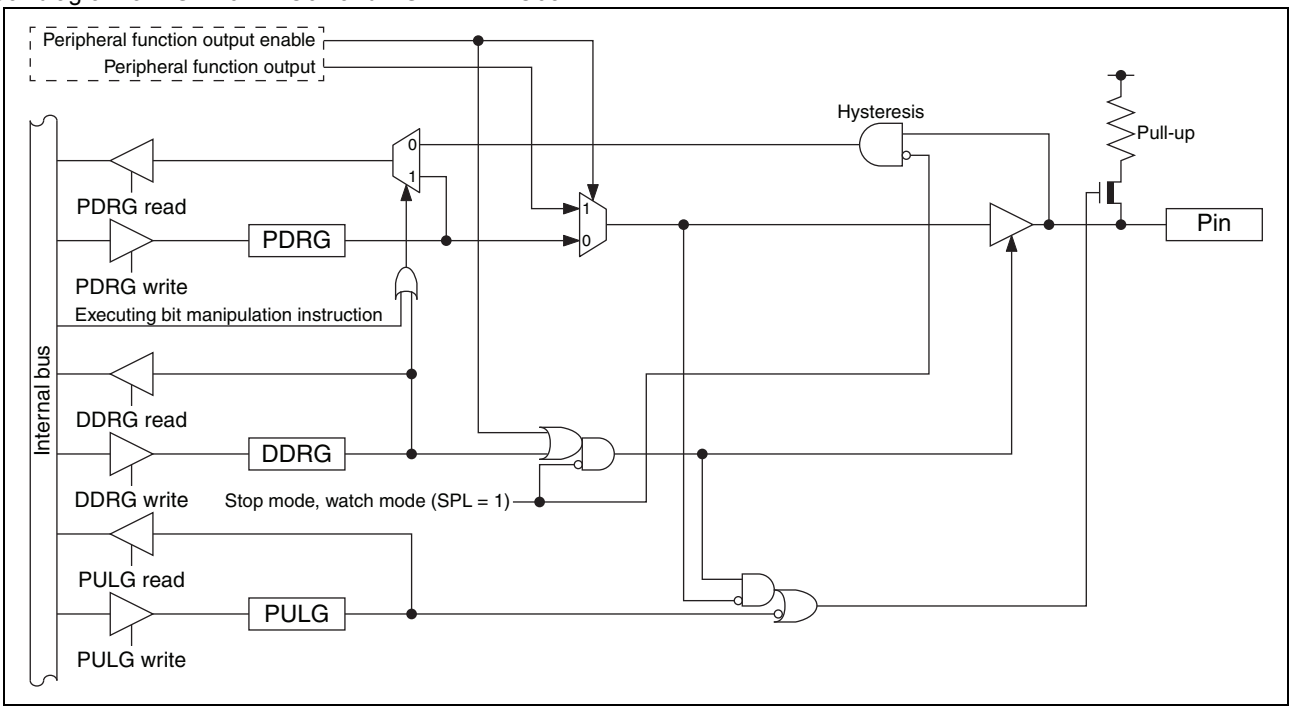
■ PG1/X0A/DIO04 pin

This pin has the following peripheral functions:
- ❒ Subclock input oscillation pin (X0A)
- ❒ TS direct output ch. 4 pin (DIO04)

■ PG2/X1A/DIO03 pin

This pin has the following peripheral functions:
- ❒ Subclock I/O oscillation pin (X1A)
- ❒ TS direct output ch. 3 pin (DIO03)

■ Block diagram of PG1/X0A/DIO04 and PG2/X1A/DIO03



3. Port G registers

■ Port G register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDRG	0	Pin state is “L” level.	PDRG value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDRG value is “1”.	As output port, outputs “H” level.
DDRG	0	Port input enabled		
	1	Port output enabled		
PULG	0	Pull-up disabled		
	1	Pull-up enabled		

■ Correspondence between registers and pins for port G

Pin name	Correspondence between related register bits and pins							
	-	-	-	-	-	PG2	PG1	-
PDRG	-	-	-	-	-	bit2	bit1	-
DDRG								
PULG								

4. Port G operations

■ Operation as an output port
- ❒ A pin becomes an output port if the bit in the DDRG register corresponding to that pin is set to “1”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ When a pin is used as an output port, it outputs the value of the PDRG register to external pins.
- ❒ If data is written to the PDRG register, the value is stored in the output latch and is output to the pin set as an output port as it is.
- ❒ Reading the PDRG register returns the PDRG register value.

■ Operation as an input port
- ❒ A pin becomes an input port if the bit in the DDRG register corresponding to that pin is set to “0”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ If data is written to the PDRG register, the value is stored in the output latch but is not output to the pin set as an input port.
- ❒ Reading the PDRG register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDRG register, the PDRG register value is returned.

■ Operation as a peripheral function output pin
- ❒ A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
- ❒ The pin value can be read from the PDRG register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDRG register. However, if the read-modify-write (RMW) type of instruction is used to read the PDRG register, the PDRG register value is returned.

■ Operation at reset

If the CPU is reset, all bits in the DDRG register are initialized to “0” and port input is enabled.

■ Operation in stop mode and watch mode
- ❒ If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRG register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
- ❒ If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

■ Operation of the pull-up register

Setting the bit in the PULG register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PULG register.

14.3 MB95870K Series

■ List of port registers

Register name		Read/Write	Initial value
Port 0 data register	PDR0	R, RM/W	0b00000000
Port 0 direction register	DDR0	R/W	0b00000000
Port 1 data register	PDR1	R, RM/W	0b00000000
Port 1 direction register	DDR1	R/W	0b00000000
Port 4 data register	PDR4	R, RM/W	0b00000000
Port 4 direction register	DDR4	R/W	0b00000000
Port 6 data register	PDR6	R, RM/W	0b00000000
Port 6 direction register	DDR6	R/W	0b00000000
Port 7 data register	PDR7	R, RM/W	0b00000000
Port 7 direction register	DDR7	R/W	0b00000000
Port F data register	PDRF	R, RM/W	0b00000000
Port F direction register	DDRF	R/W	0b00000000
Port G data register	PDRG	R, RM/W	0b00000000
Port G direction register	DDRG	R/W	0b00000000
Port 0 pull-up register	PUL0	R/W	0b00000000
Port 1 pull-up register	PUL1	R/W	0b00000000
Port 4 pull-up register	PUL4	R/W	0b00000000
Port 6 pull-up register	PUL6	R/W	0b00000000
Port 7 pull-up register	PUL7	R/W	0b00000000
Port G pull-up register	PULG	R/W	0b00000000
A/D input disable register (lower)	AIDRL	R/W	0b00000000
Touch input disable register 0	TIDR0	R/W	0b00000000
Touch input disable register 1	TIDR1	R/W	0b00000000

R/W : Readable/writable (The read value is the same as the write value.)

R, RM/W : Readable/writable (The read value is different from the write value. The write value is read by the read-modify-write (RMW) type of instruction.)

14.3.1 Port 0

Port 0 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

1. Port 0 configuration

■ Port 0 is made up of the following elements.
- ❒ General-purpose I/O pins/peripheral function I/O pins
- ❒ Port 0 data register (PDR0)
- ❒ Port 0 direction register (DDR0)
- ❒ Port 0 pull-up register (PUL0)
- ❒ A/D input disable register (lower) (AIDRL)

2. Block diagrams of port 0

■ P00/INT00 pin

This pin has the following peripheral function:
- ❒ External interrupt input pin (INT00)

■ P01/INT01 pin

This pin has the following peripheral function:
- ❒ External interrupt input pin (INT01)

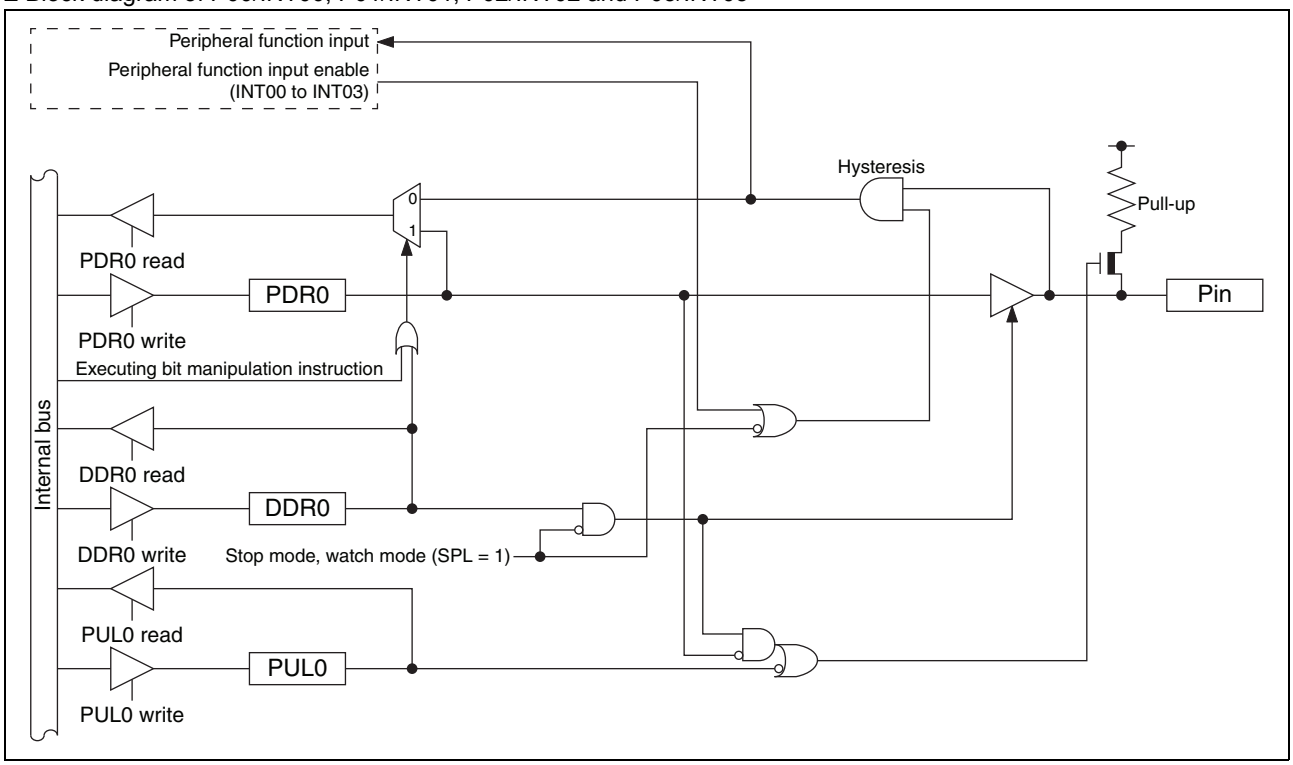
■ P02/INT02 pin

This pin has the following peripheral function:
- ❒ External interrupt input pin (INT02)

■ P03/INT03 pin

This pin has the following peripheral function:
- ❒ External interrupt input pin (INT03)

■ Block diagram of P00/INT00, P01/INT01, P02/INT02 and P03/INT03

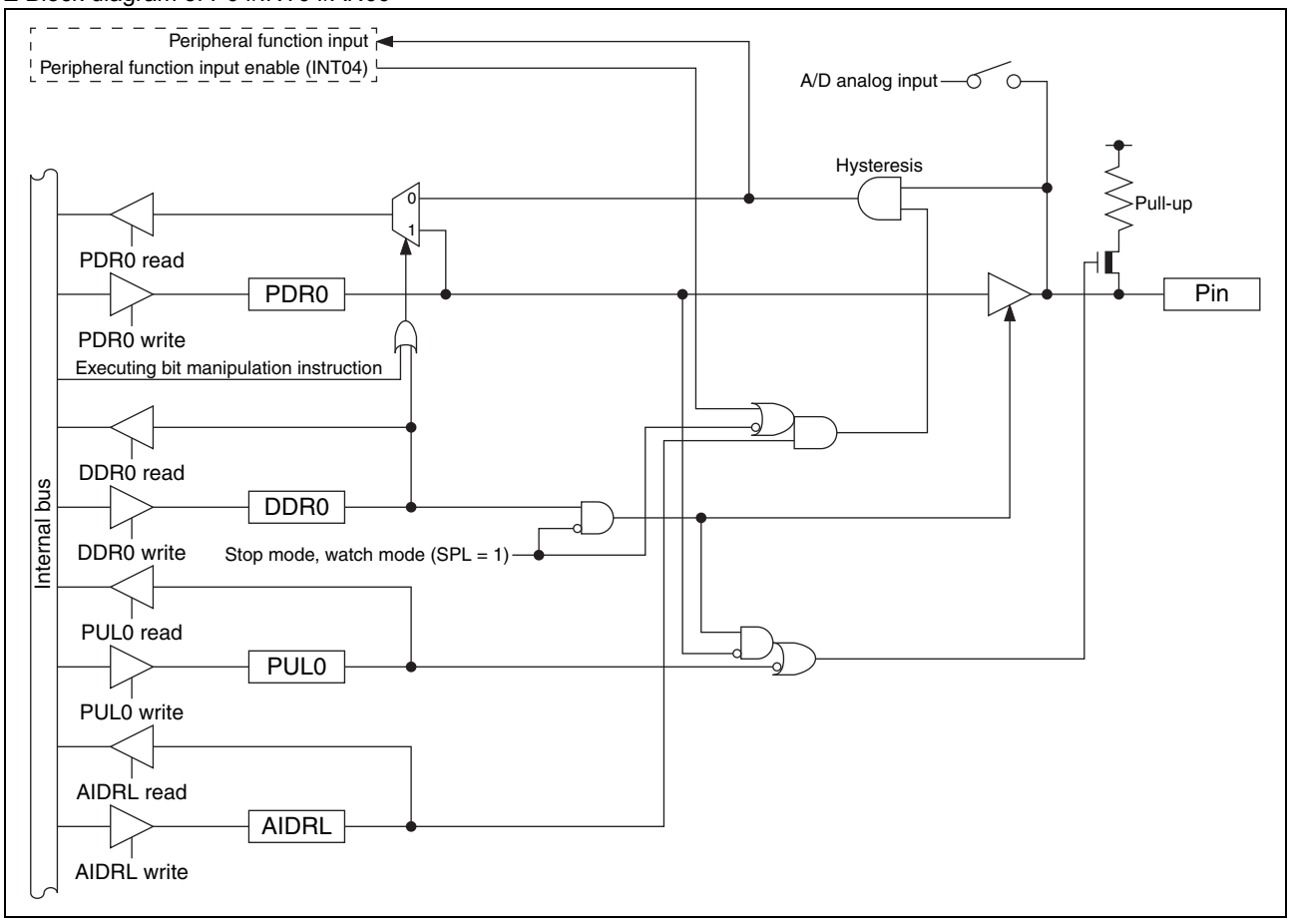


■ P04/INT04/AN00 pin

This pin has the following peripheral functions:

- ❒ External interrupt input pin (INT04)
- ❒ 8/10-bit A/D converter analog input pin (AN00)

■ Block diagram of P04/INT04/AN00

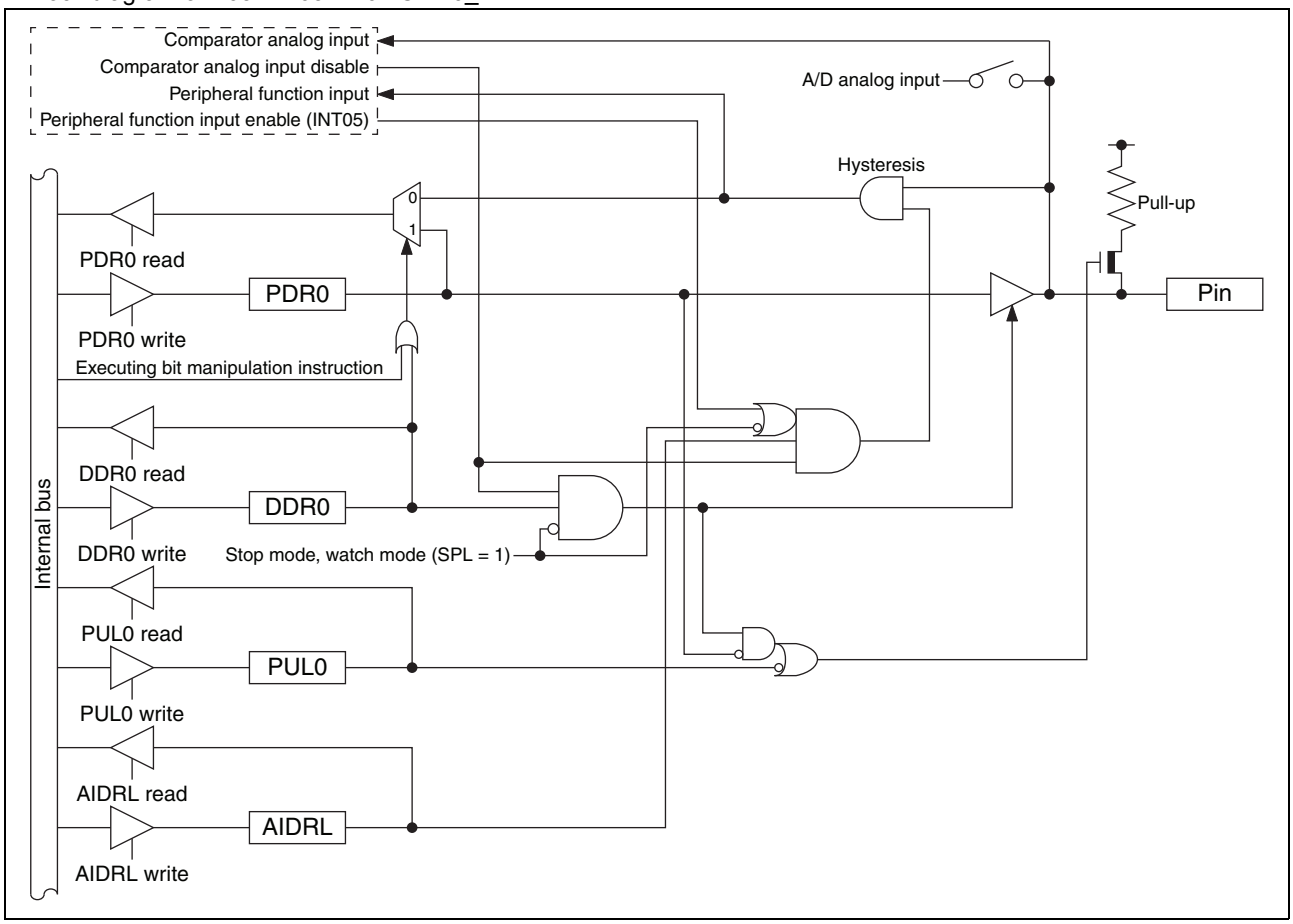


■ P05/INT05/AN01/CMP0_N pin

This pin has the following peripheral functions:

- ❒ External interrupt input pin (INT05)
- ❒ 8/10-bit A/D converter analog input pin (AN01)
- ❒ Comparator ch. 0 inverting analog input (negative input) pin (CMP0_N)

■ Block diagram of P05/INT05/AN01/CMP0_N

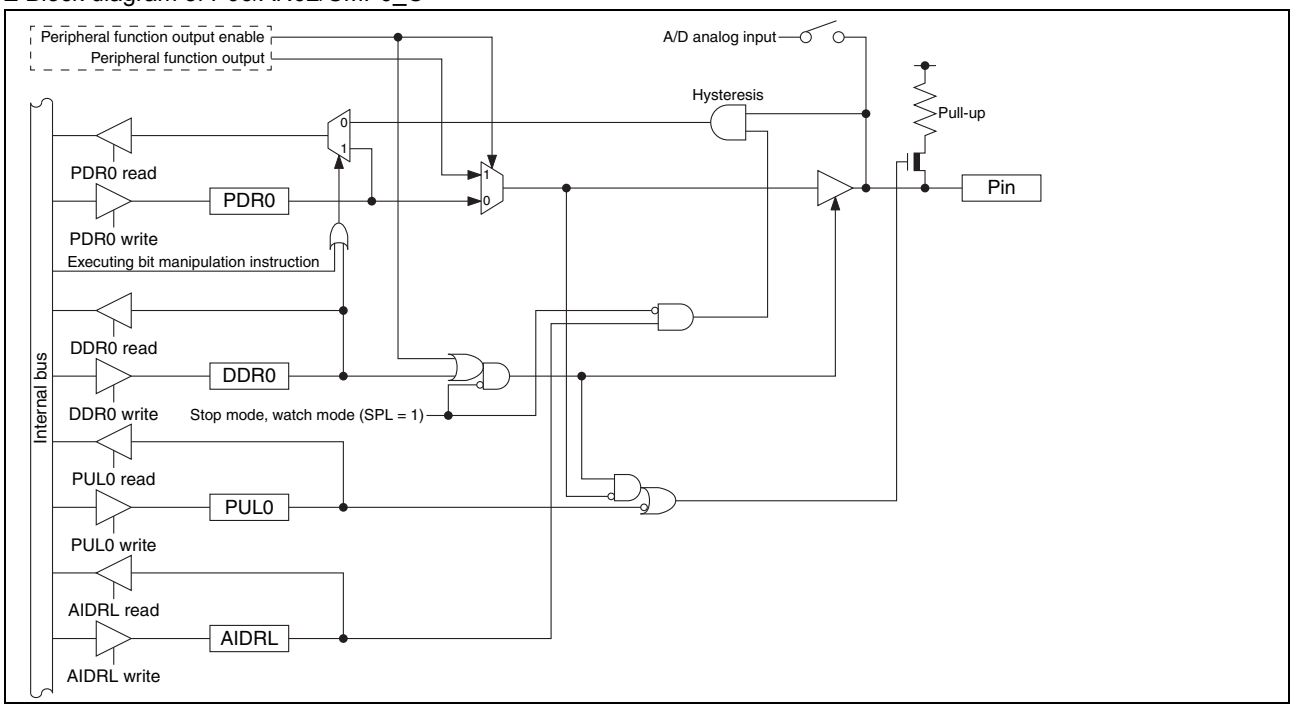


■ P06/AN02/CMP0_O pin

This pin has the following peripheral functions:

- ❒ 8/10-bit A/D converter analog input pin (AN02)
- ❒ Comparator ch. 0 digital output pin (CMP0_O)

■ Block diagram of P06/AN02/CMP0_O

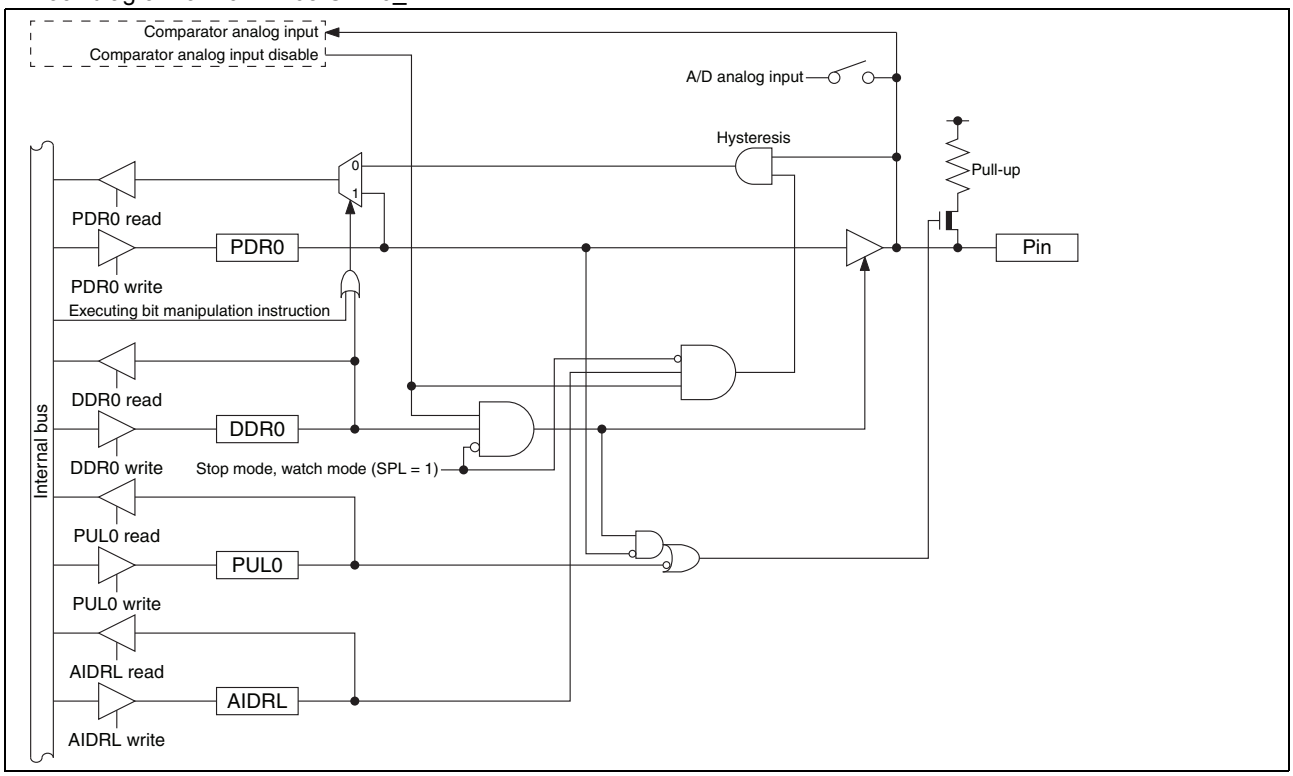


■ P07/AN03/CMP0_P pin

This pin has the following peripheral functions:

- 8/10-bit A/D converter analog input pin (AN03)
- Comparator ch. 0 non-inverting analog input (positive input) pin (CMP0_P)

■ Block diagram of P07/AN03/CMP0_P



3. Port 0 registers

■ Port 0 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR0	0	Pin state is “L” level.	PDR0 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR0 value is “1”.	As output port, outputs “H” level.
DDR0	0	Port input enabled		
	1	Port output enabled		
PUL0	0	Pull-up disabled		
	1	Pull-up enabled		
AIDRL	0	Analog input enabled		
	1	Port input enabled		

■ Correspondence between registers and pins for port 0

Pin name	Correspondence between related register bits and pins							
	P07	P06	P05	P04	P03	P02	P01	P00
PDR0	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DDR0								
PUL0								
AIDRL	bit5	bit4	bit1	bit0	-	-	-	-

4. Port 0 operations

■ Operation as an output port
- ❒ A pin becomes an output port if the bit in the DDR0 register corresponding to that pin is set to “1”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ When a pin is used as an output port, it outputs the value of the PDR0 register to external pins.
- ❒ If data is written to the PDR0 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
- ❒ Reading the PDR0 register returns the PDR0 register value.

■ Operation as an input port
- ❒ A pin becomes an input port if the bit in the DDR0 register corresponding to that pin is set to “0”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ When using a pin shared with the analog input function as an input port, set the bit in the A/D input disable register (lower) (AIDRL) corresponding to that pin to “1”.
- ❒ If data is written to the PDR0 register, the value is stored in the output latch but is not output to the pin set as an input port.
- ❒ Reading the PDR0 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR0 register, the PDR0 register value is returned.

■ Operation as a peripheral function output pin
- ❒ A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
- ❒ The pin value can be read from the PDR0 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR0 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR0 register, the PDR0 register value is returned.

■ Operation as a peripheral function input pin
- ❒ To set a pin as an input port, set the bit in the DDR0 register corresponding to the input pin of a peripheral function to “0”.
- ❒ When using a pin shared with the analog input function as another peripheral function input pin, configure it as an input port by setting the bit in the AIDRL register corresponding to that pin to “1”.
- ❒ Reading the PDR0 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR0 register, the PDR0 register value is returned.

■ Operation at reset

If the CPU is reset, all bits in the DDR0 register are initialized to “0” and port input is enabled. As for a pin shared with the analog input function, its port input is disabled because the AIDRL register is initialized to “0”.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR0 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open. However, if the interrupt input is enabled for the external interrupt (INT00 to INT05), the input is enabled and not blocked.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.
- Operation as an analog input pin
  - Set the bit in the DDR0 register bit corresponding to the analog input pin to “0” and the bit corresponding to that pin in the AIDRL register to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions. In addition, set the corresponding bit in the PUL0 register to “0”.
- Operation as an external interrupt input pin
  - Set the bit in the DDR0 register corresponding to the external interrupt input pin to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - The pin value is always input to the external interrupt circuit. When using a pin for a function other than the interrupt, disable the external interrupt function corresponding to that pin.
- Operation of the pull-up register

Setting the bit in the PUL0 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL0 register.

- Operation as a comparator input pin
  - Set the bit in the AIDRL register corresponding to the comparator input pin to “0”.
  - Regardless of the value of the PDR0 register and that of the DDR0 register, if the comparator analog input enable bit in the comparator control register ch. 0 (CMR0:VCID) is set to “0”, the comparator input function is enabled.
  - To disable the comparator input function, set the VCID bit to “1”.
  - For details of the comparator, refer to “CHAPTER 25 COMPARATOR” in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

14.3.2 Port 1

Port 1 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

1. Port 1 configuration

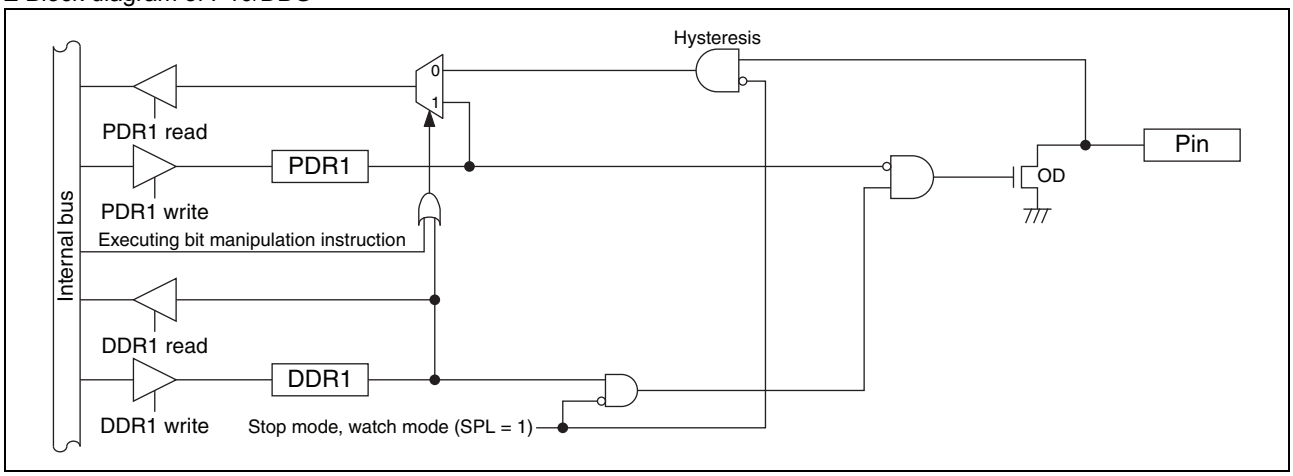
■ Port 1 is made up of the following elements.
- ❒ General-purpose I/O pins/peripheral function I/O pins
- ❒ Port 1 data register (PDR1)
- ❒ Port 1 direction register (DDR1)
- ❒ Port 1 pull-up register (PUL1)

2. Block diagrams of port 1

■ P10/DBG pin

This pin has the following peripheral function:
- ❒ DBG input pin (DBG)

■ Block diagram of P10/DBG



■ P11/EC0/DIO01 pin

This pin has the following peripheral functions:
- ❒ 8/16-bit composite timer ch. 0 clock input pin (EC0)
- ❒ TS direct output ch. 1 pin (DIO01)

■ P15/UCK0 pin

This pin has the following peripheral function:
- ❒ UART/SIO ch. 0 clock I/O pin (UCK0)

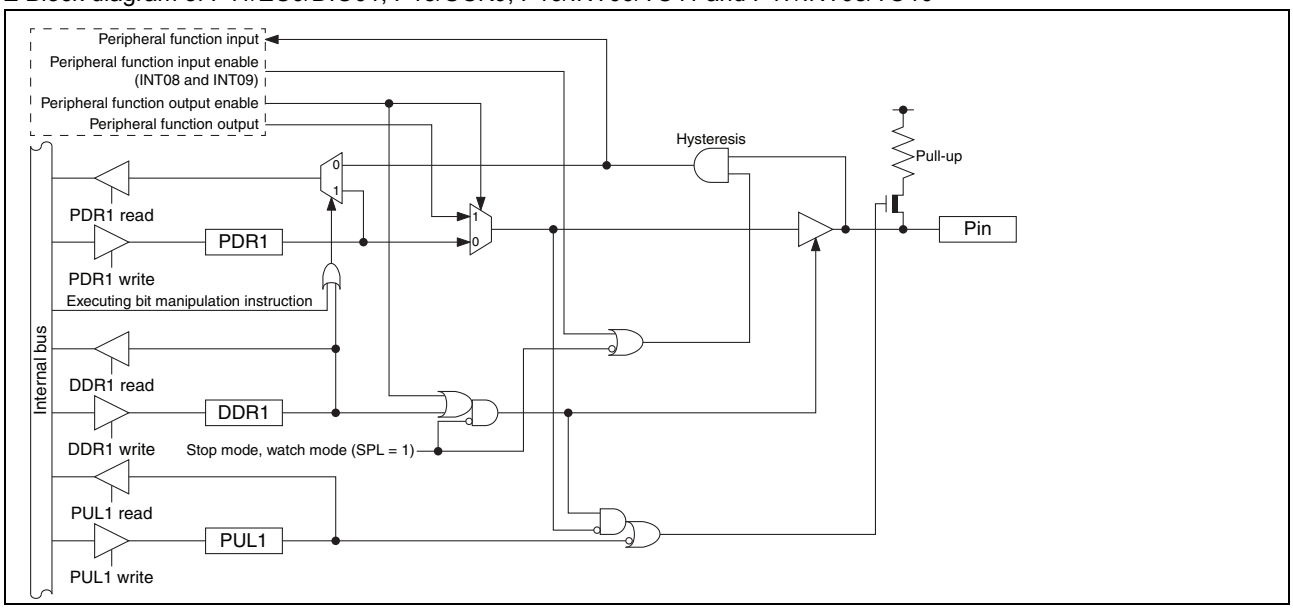
■ P16/INT09/TO11 pin

This pin has the following peripheral functions:
- ❒ External interrupt input pin (INT09)
- ❒ 8/16-bit composite timer ch. 1 output pin (TO11)

■ P17/INT08/TO10 pin

This pin has the following peripheral functions:
- ❒ External interrupt input pin (INT08)
- ❒ 8/16-bit composite timer ch. 1 output pin (TO10)

■ Block diagram of P11/EC0/DIO01, P15/UCK0, P16/INT09/TO11 and P17/INT08/TO10



■ P12/BEEP pin

This pin has the following peripheral function:

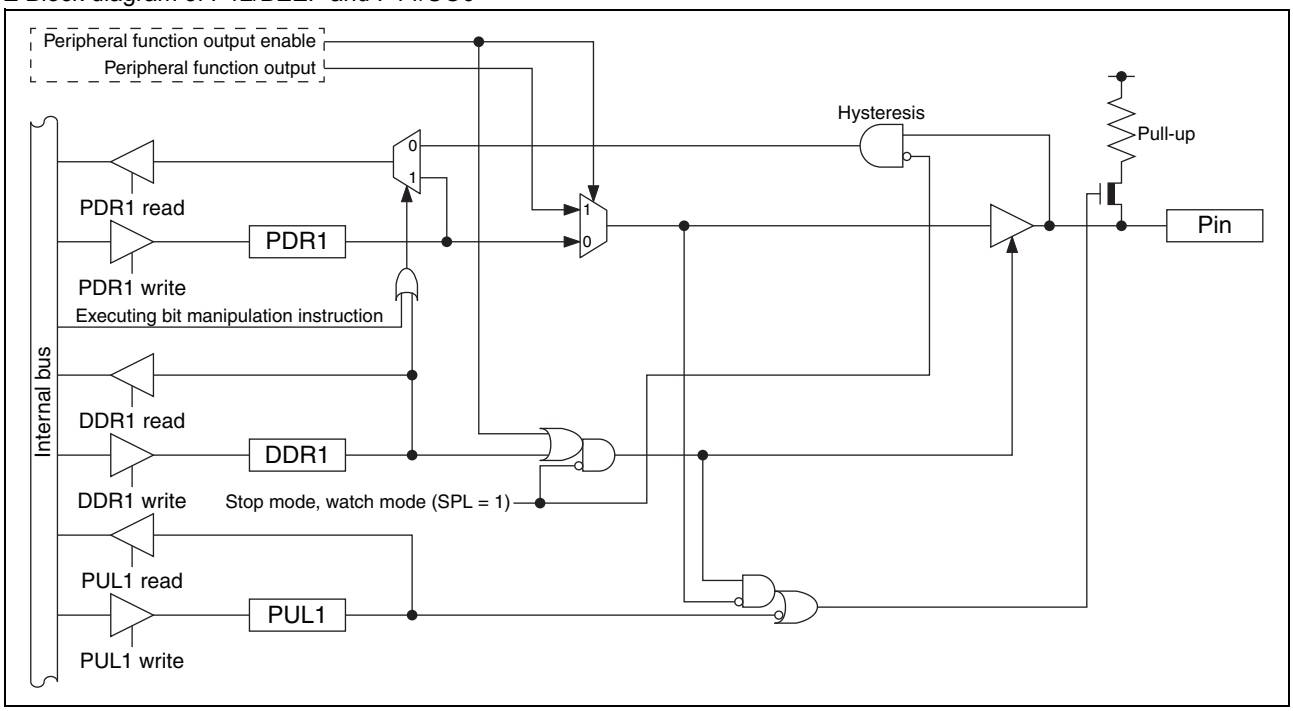
❒ Beep output pin (BEEP)

■ P14/UO0 pin

This pin has the following peripheral function:

❒ UART/SIO ch. 0 data output pin (UO0)

■ Block diagram of P12/BEEP and P14/UO0

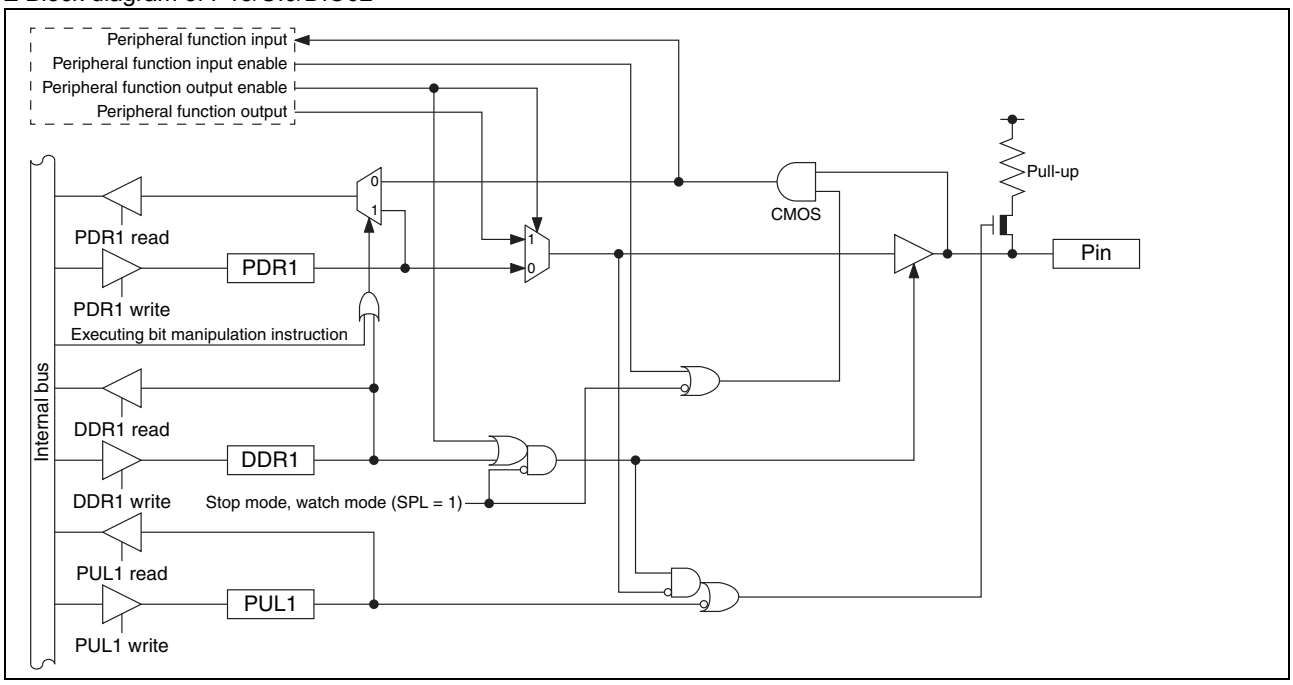


■ P13/UI0/DIO02 pin

This pin has the following peripheral functions:

- ❒ UART/SIO ch. 0 data input pin (UI0)
- ❒ TS direct output ch. 2 pin (DIO02)

■ Block diagram of P13/UI0/DIO02



3. Port 1 registers

■ Port 1 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR1	0	Pin state is “L” level.	PDR1 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR1 value is “1”.	As output port, outputs “H” level.*
DDR1	0	Port input enabled		
	1	Port output enabled		
PUL1	0	Pull-up disabled		
	1	Pull-up enabled		

*: If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

■ Correspondence between registers and pins for port 1

Pin name	Correspondence between related register bits and pins							
	P17	P16	P15	P14	P13	P12	P11	P10
PDR1	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0*
DDR1								
PUL1								

*: Though P10 has no pull-up function, bit0 in the PUL1 register can still be accessed. The operation of P10 is not affected by the setting of bit0 in the PUL1 register.

4. Port 1 operations

■ Operation as an output port
- ❒ A pin becomes an output port if the bit in the DDR1 register corresponding to that pin is set to “1”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ When a pin is used as an output port, it outputs the value of the PDR1 register to external pins.
- ❒ If data is written to the PDR1 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
- ❒ Reading the PDR1 register returns the PDR1 register value.

■ Operation as an input port
- ❒ A pin becomes an input port if the bit in the DDR1 register corresponding to that pin is set to “0”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ If data is written to the PDR1 register, the value is stored in the output latch but is not output to the pin set as an input port.
- ❒ Reading the PDR1 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR1 register, the PDR1 register value is returned.

■ Operation as a peripheral function output pin
- ❒ A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
- ❒ The pin value can be read from the PDR1 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR1 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR1 register, the PDR1 register value is returned.

■ Operation as a peripheral function input pin
- ❒ To set a pin as an input port, set the bit in the DDR1 register corresponding to the input pin of a peripheral function to “0”.
- ❒ Reading the PDR1 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR1 register, the PDR1 register value is returned.

■ Operation at reset

If the CPU is reset, all bits in the DDR1 register are initialized to “0” and port input is enabled.

■ Operation in stop mode and watch mode
- ❒ If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR1 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open. However, if the interrupt input from the external interrupt (INT08 and INT09) is enabled, or if the interrupt input of P11/EC0, P13/UI0 and P15/UCK0 is enabled by the external interrupt control register ch. 0 (EIC00) of the external interrupt circuit and the interrupt pin selection circuit control register (WICR) of the interrupt pin selection circuit, the input is enabled and is not blocked.
- ❒ If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

■ Operation as an external interrupt input pin
- ❒ Set the bit in the DDR1 register corresponding to the external interrupt input pin to “0”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ The pin value is always input to the external interrupt circuit. When using a pin for a function other than the interrupt, disable the external interrupt function corresponding to that pin.

■ Operation of the pull-up register

Setting the bit in the PUL1 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL1 register.

14.3.3 Port 4

Port 4 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

1. Port 4 configuration

■ Port 4 is made up of the following elements.
- ❒ General-purpose I/O pins/peripheral function I/O pins
- ❒ Port 4 data register (PDR4)
- ❒ Port 4 direction register (DDR4)
- ❒ Port 4 pull-up register (PUL4)
- ❒ A/D input disable register (lower) (AIDRL)

2. Block diagrams of port 4

■ P40/AN04/PPG00 pin

This pin has the following peripheral functions:
- ❒ 8/10-bit A/D converter analog input pin (AN04)
- ❒ 8/16-bit PPG ch. 0 output pin (PPG00)

■ P41/AN05/PPG01 pin

This pin has the following peripheral functions:
- ❒ 8/10-bit A/D converter analog input pin (AN05)
- ❒ 8/16-bit PPG ch. 0 output pin (PPG01)

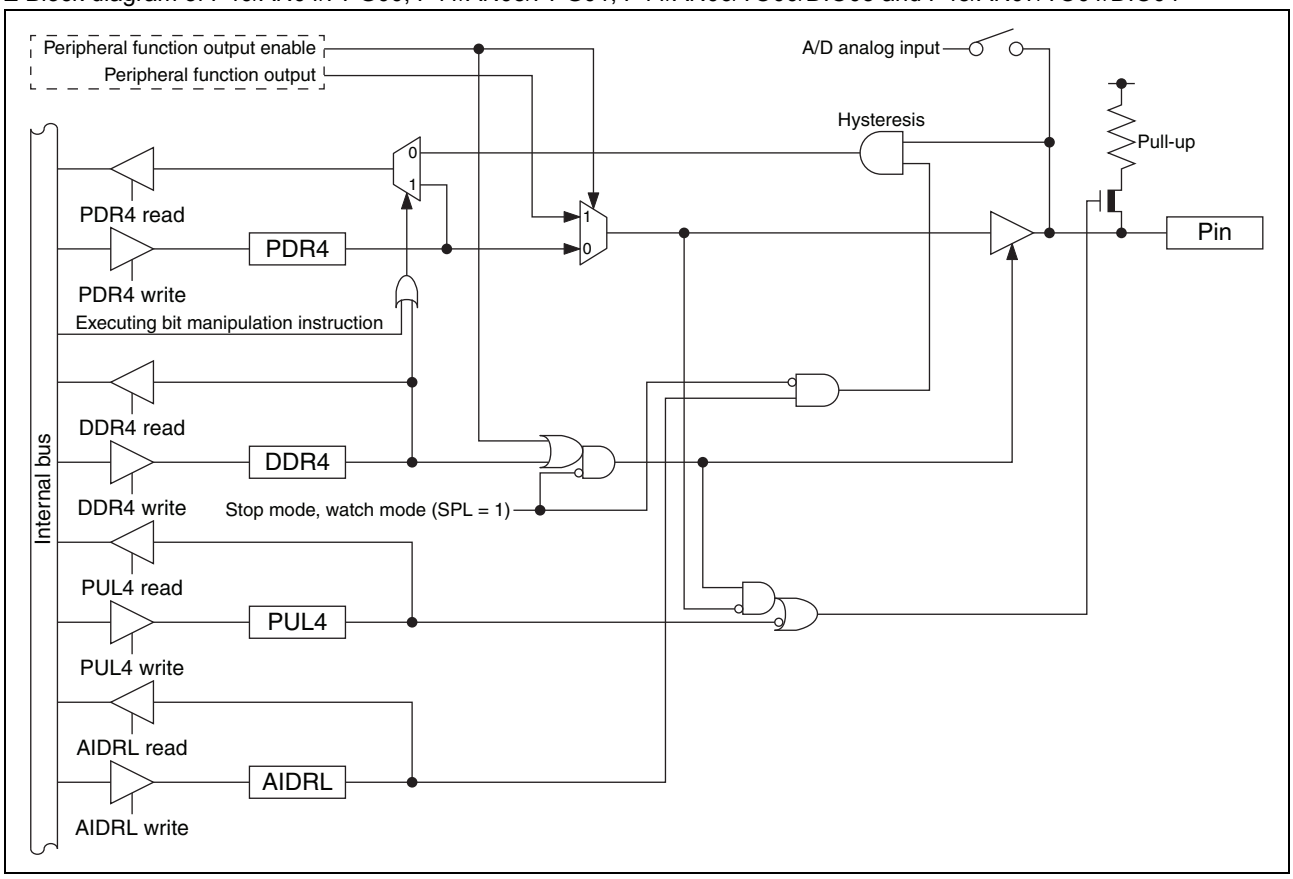
■ P44/AN06/TO00/DIO03 pin

This pin has the following peripheral functions:
- ❒ 8/10-bit A/D converter analog input pin (AN06)
- ❒ 8/16-bit composite timer ch. 0 output pin (TO00)
- ❒ TS direct output ch. 3 pin (DIO03)

■ P45/AN07/TO01/DIO04 pin

This pin has the following peripheral functions:
- ❒ 8/10-bit A/D converter analog input pin (AN07)
- ❒ 8/16-bit composite timer ch. 0 output pin (TO01)
- ❒ TS direct output ch. 4 pin (DIO04)

■ Block diagram of P40/AN04/PPG00, P41/AN05/PPG01, P44/AN06/TO00/DIO03 and P45/AN07/TO01/DIO04



■ P42/INT06/PPG10 pin

This pin has the following peripheral functions:

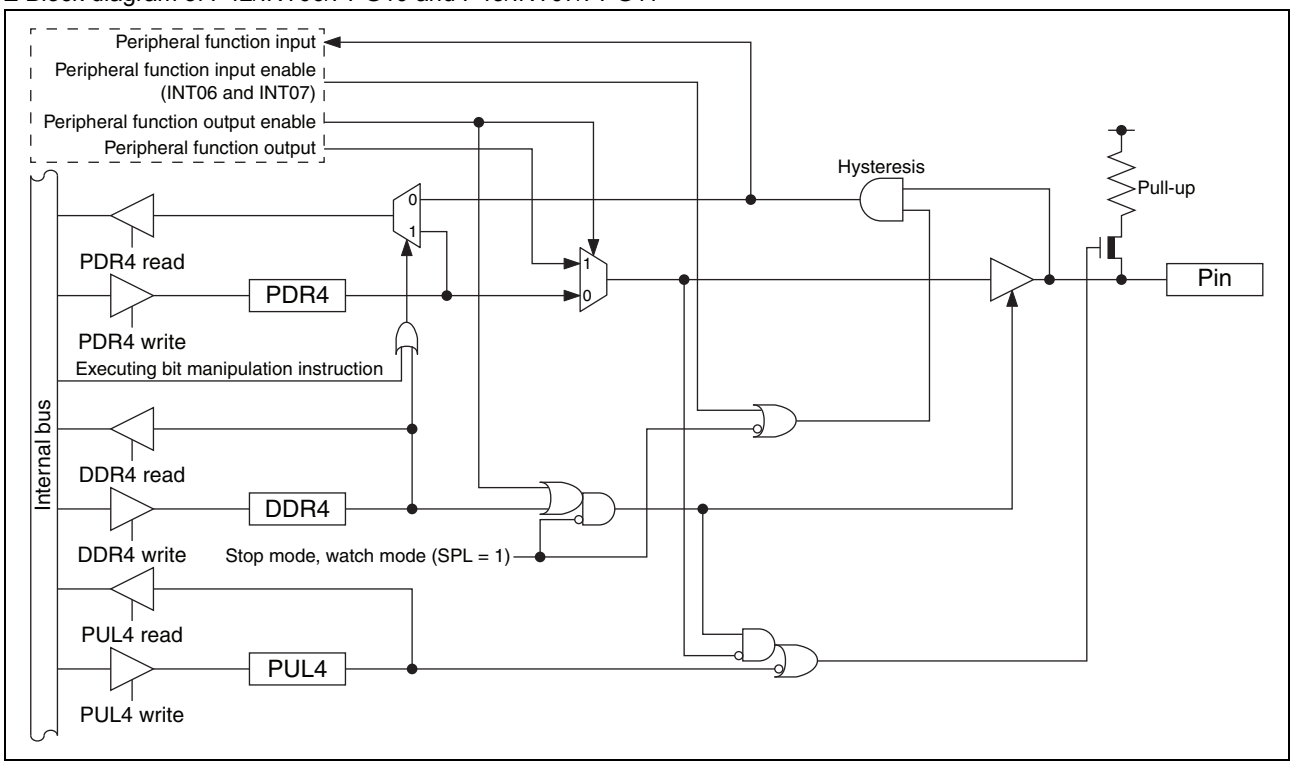
- ❒ External interrupt input pin (INT06)
- ❒ 8/16-bit PPG ch. 1 output pin (PPG10)

■ P43/INT07/PPG11 pin

This pin has the following peripheral functions:

- ❒ External interrupt input pin (INT07)
- ❒ 8/16-bit PPG ch. 1 output pin (PPG11)

■ Block diagram of P42/INT06/PPG10 and P43/INT07/PPG11



■ P46/SDA pin

This pin has the following peripheral function:

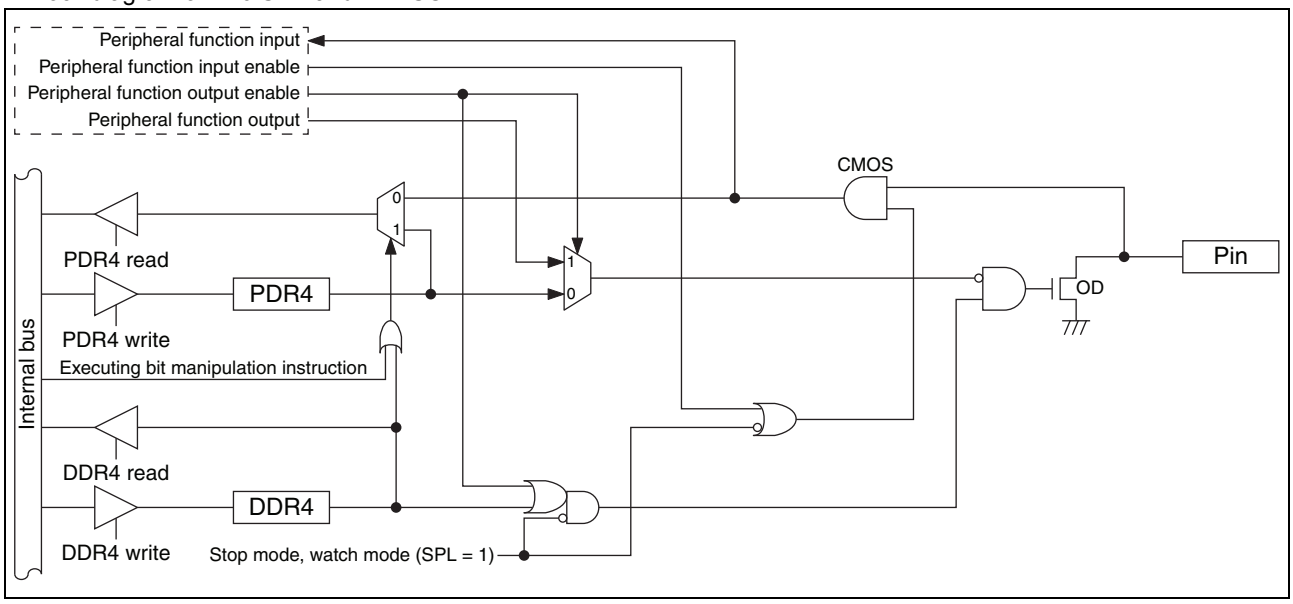
❒ I^2C bus interface ch. 0 data I/O pin (SDA)

■ P47/SCL pin

This pin has the following peripheral function:

❒ I^2C bus interface ch. 0 clock I/O pin (SCL)

■ Block diagram of P46/SDA and P47/SCL



3. Port 4 registers

■ Port 4 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR4	0	Pin state is “L” level.	PDR4 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR4 value is “1”.	As output port, outputs “H” level.*
DDR4	0	Port input enabled		
	1	Port output enabled		
PUL4	0	Pull-up disabled		
	1	Pull-up enabled		
AIDRL	0	Analog input enabled		
	1	Port input enabled		

*: If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

■ Correspondence between registers and pins for port 4

Pin name	Correspondence between related register bits and pins							
	P47	P46	P45	P44	P43	P42	P41	P40
PDR4	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DDR4								
PUL4	-	-						
AIDRL			bit7	bit6	-	-	bit3	bit2

4. Port 4 operations

■ Operation as an output port
- ❒ A pin becomes an output port if the bit in the DDR4 register corresponding to that pin is set to “1”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ When a pin is used as an output port, it outputs the value of the PDR4 register to external pins.
- ❒ If data is written to the PDR4 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
- ❒ Reading the PDR4 register returns the PDR4 register value.

■ Operation as an input port
- ❒ A pin becomes an input port if the bit in the DDR4 register corresponding to that pin is set to “0”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ When using a pin shared with the analog input function as an input port, set the bit in the A/D input disable register (lower) (AIDRL) corresponding to that pin to “1”.
- ❒ If data is written to the PDR4 register, the value is stored in the output latch but is not output to the pin set as an input port.
- ❒ Reading the PDR4 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR4 register, the PDR4 register value is returned.

■ Operation as a peripheral function output pin
- ❒ A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
- ❒ The pin value can be read from the PDR4 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR4 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR4 register, the PDR4 register value is returned.

■ Operation as a peripheral function input pin
- ❒ To set a pin as an input port, set the bit in the DDR4 register corresponding to the input pin of a peripheral function to “0”.
- ❒ When using a pin shared with the analog input function as another peripheral function input pin, configure it as an input port by setting the bit in the AIDRL register corresponding to that pin to “1”.
- ❒ Reading the PDR4 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR4 register, the PDR4 register value is returned.

■ Operation at reset

If the CPU is reset, all bits in the DDR4 register are initialized to “0” and port input is enabled. As for a pin shared with the analog input function, its port input is disabled because the AIDRL register is initialized to “0”.

■ Operation in stop mode and watch mode
- ❒ If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR4 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open. However, if the interrupt input is enabled for the external interrupt (INT06 and INT07), the input is enabled and not blocked.
- ❒ If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

■ Operation as an analog input pin
- ❒ Set the bit in the DDR4 register bit corresponding to the analog input pin to “0” and the bit corresponding to that pin in the AIDRL register to “0”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions. In addition, set the corresponding bit in the PUL4 register to “0”.

■ Operation as an external interrupt input pin
- ❒ Set the bit in the DDR4 register corresponding to the external interrupt input pin to “0”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ The pin value is always input to the external interrupt circuit. When using a pin for a function other than the interrupt, disable the external interrupt function corresponding to that pin.

■ Operation of the pull-up register

Setting the bit in the PUL4 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL4 register.

14.3.4 Port 6

Port 6 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

1. Port 6 configuration

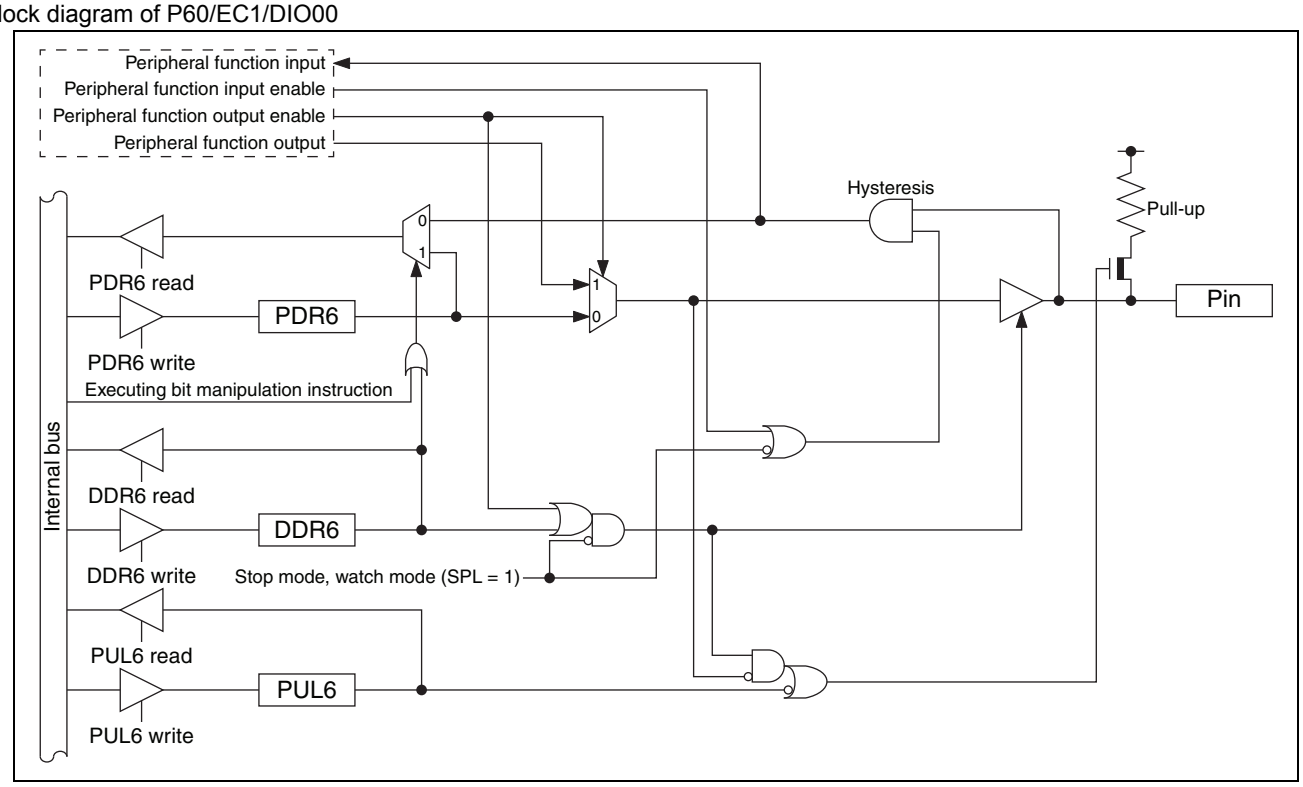
■ Port 6 is made up of the following elements.
- ❒ General-purpose I/O pins/peripheral function I/O pins
- ❒ Port 6 data register (PDR6)
- ❒ Port 6 direction register (DDR6)
- ❒ Port 6 pull-up register (PUL6)
- ❒ Touch input disable register 0 (TIDR0)

2. Block diagrams of port 6

■ P60/EC1/DIO00 pin

This pin has the following peripheral functions:
- ❒ 8/16-bit composite timer ch. 1 clock input pin (EC1)
- ❒ TS direct output ch. 0 pin (DIO00)

■ Block diagram of P60/EC1/DIO00



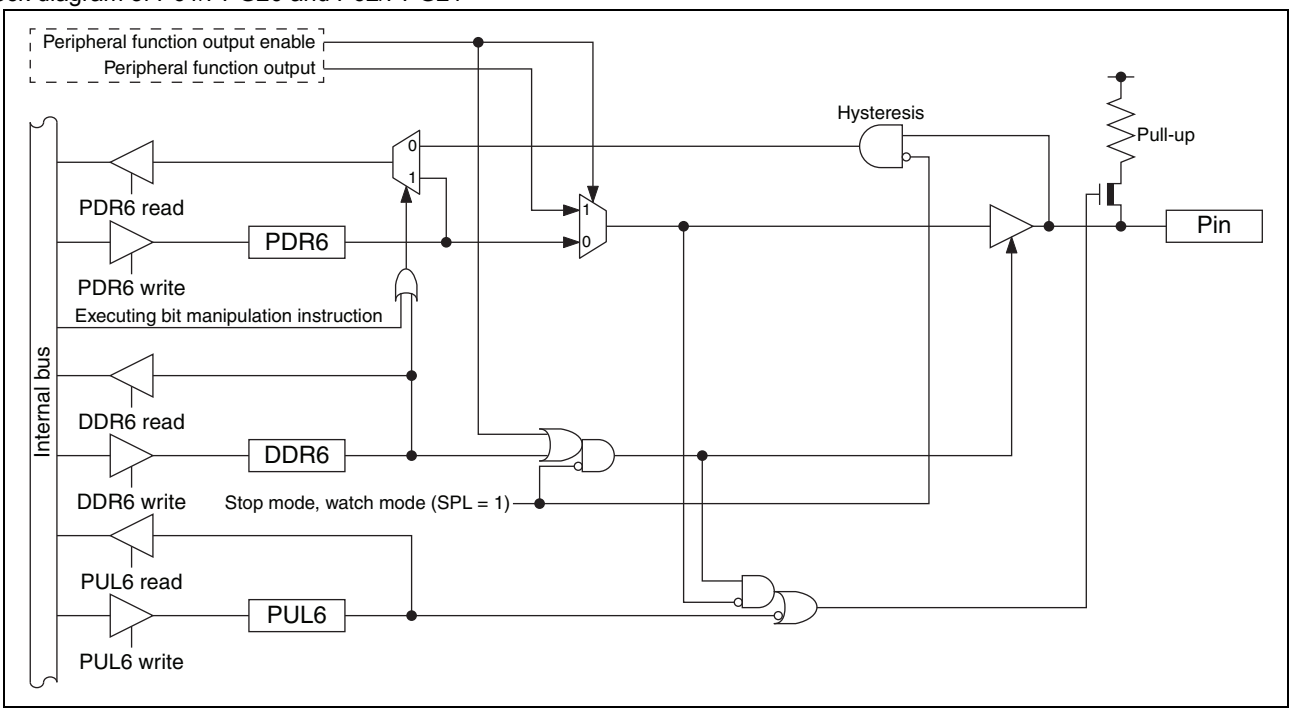
■ P61/PPG20 pin

This pin has the following peripheral function:
- ❒ 8/16-bit PPG ch. 2 output pin (PPG20)

■ P62/PPG21 pin

This pin has the following peripheral function:
- ❒ 8/16-bit PPG ch. 2 output pin (PPG21)

■ Block diagram of P61/PPG20 and P62/PPG21



■ P63/AREF pin

This pin has the following peripheral function:

❒ TS reference input pin (AREF)

■ P64/S00 pin

This pin has the following peripheral function:

❒ TS touch ch. 0 input pin (S00)

■ P65/S01 pin

This pin has the following peripheral function:

❒ TS touch ch. 1 input pin (S01)

■ P66/S02 pin

This pin has the following peripheral function:

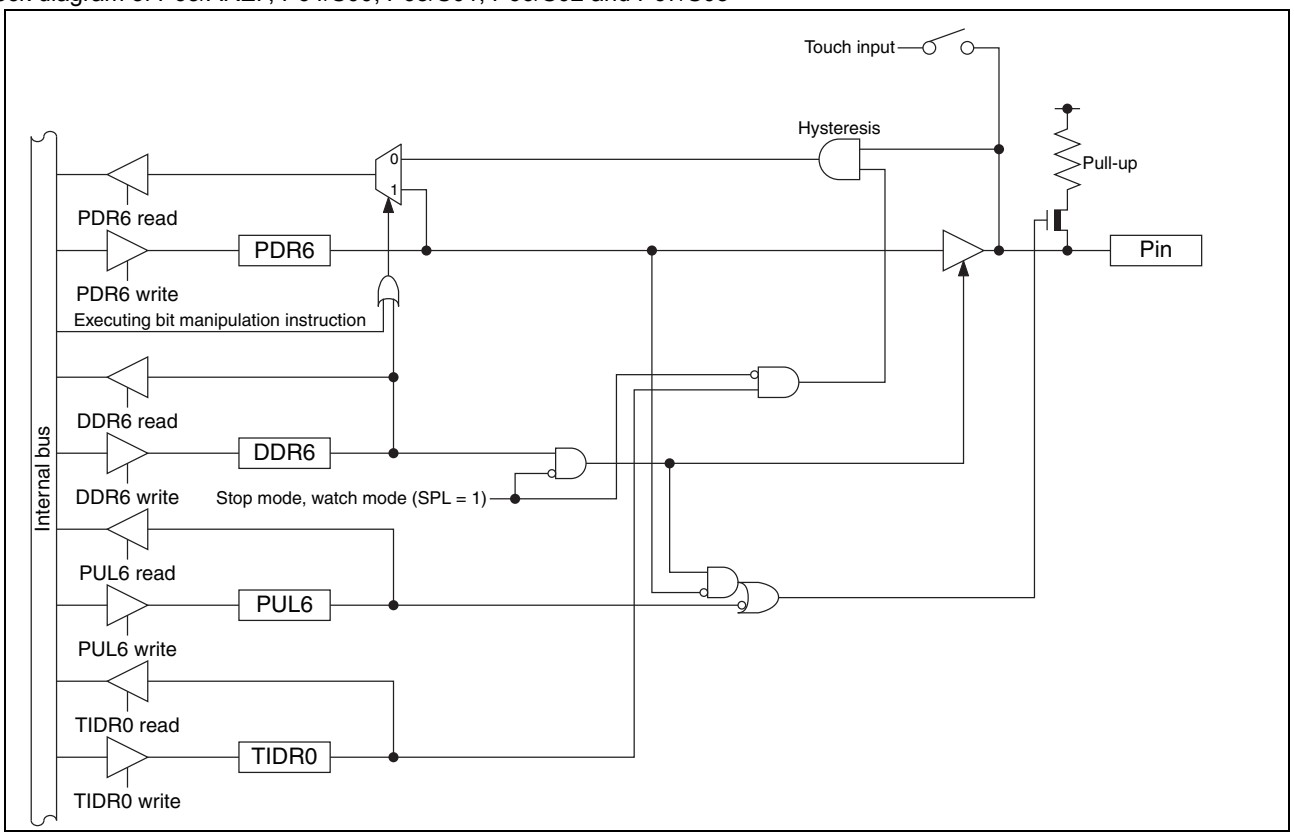
❒ TS touch ch. 2 input pin (S02)

■ P67/S03 pin

This pin has the following peripheral function:

❒ TS touch ch. 3 input pin (S03)

■ Block diagram of P63/AREF, P64/S00, P65/S01, P66/S02 and P67/S03



3. Port 6 registers

■ Port 6 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR6	0	Pin state is “L” level.	PDR6 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR6 value is “1”.	As output port, outputs “H” level.
DDR6	0	Port input enabled		
	1	Port output enabled		
PUL6	0	Pull-up disabled		
	1	Pull-up enabled		
TIDR0	0	Touch input or reference input enabled		
	1	Port input enabled		

■ Correspondence between registers and pins for port 6

Pin name	Correspondence between related register bits and pins							
	P67	P66	P65	P64	P63	P62	P61	P60
PDR6	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DDR6								
PUL6								
TIDR0	bit7	bit6	bit5	bit4	bit3	-	-	-

4. Port 6 operations

■ Operation as an output port
- ❒ A pin becomes an output port if the bit in the DDR6 register corresponding to that pin is set to “1”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ When a pin is used as an output port, it outputs the value of the PDR6 register to external pins.
- ❒ If data is written to the PDR6 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
- ❒ Reading the PDR6 register returns the PDR6 register value.

■ Operation as an input port
- ❒ A pin becomes an input port if the bit in the DDR6 register corresponding to that pin is set to “0”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ When using a pin shared with the touch input function as an input port, set the bit in the touch input disable register 0 (TIDR0) corresponding to that pin to “1”.
- ❒ If data is written to the PDR6 register, the value is stored in the output latch but is not output to the pin set as an input port.
- ❒ Reading the PDR6 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR6 register, the PDR6 register value is returned.

■ Operation as a peripheral function output pin
- ❒ A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
- ❒ The pin value can be read from the PDR6 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR6 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR6 register, the PDR6 register value is returned.

■ Operation as a peripheral function input pin
- ❒ To set a pin as an input port, set the bit in the DDR6 register corresponding to the input pin of a peripheral function to “0”.
- ❒ Reading the PDR6 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR6 register, the PDR6 register value is returned.

■ Operation at reset

If the CPU is reset, all bits in the DDR6 register are initialized to “0” and port input is enabled. As for a pin shared with the touch input function, its port input is disabled because the TIDR0 register is initialized to “0”.

■ Operation in stop mode and watch mode
- ❒ If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR6 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open. However, if the interrupt input of P60/EC1/DIO00 is enabled by the external interrupt control register ch. 0 (EIC00) of the external interrupt circuit and the interrupt pin selection circuit control register (WICR) of the interrupt pin selection circuit, the input is enabled and is not blocked.
- ❒ When the stop enable bit in the TS prescaler control register (PSC:STPE) is set to “1”, the TS can operate in stop mode or watch mode, the touch input is enabled and is not blocked. The TS wakes up in stop mode or watch mode provided that the TINT (touch interrupt) and the GINT (general interrupt) are set to enable the TS to wake up in stop mode or watch mode.
- ❒ If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

■ Operation as a touch input pin

Set the bit in the DDR6 register corresponding to the touch input pin to “0”, the bit in the TIDR0 register corresponding to the same pin to “0”, and the bit in the PUL6 register corresponding to the same pin to “0”.

■ Operation of the pull-up register

Setting the bit in the PUL6 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL6 register.

14.3.5 Port 7

Port 7 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

1. Port 7 configuration

- Port 7 is made up of the following elements.
  - General-purpose I/O pins/peripheral function I/O pins
  - Port 7 data register (PDR7)
  - Port 7 direction register (DDR7)
  - Port 7 pull-up register (PUL7)
  - Touch input disable register 1 (TIDR1)

2. Block diagrams of port 7

- P70/S04 pin

This pin has the following peripheral function:
  - TS touch ch. 4 input pin (S04)

- P71/S05 pin

This pin has the following peripheral function:
  - TS touch ch. 5 input pin (S05)

- P72/S06 pin

This pin has the following peripheral function:
  - TS touch ch. 6 input pin (S06)

- P73/S07 pin

This pin has the following peripheral function:
  - TS touch ch. 7 input pin (S07)

- P74/S08 pin

This pin has the following peripheral function:
  - TS touch ch. 8 input pin (S08)

- P75/S09 pin

This pin has the following peripheral function:
  - TS touch ch. 9 input pin (S09)

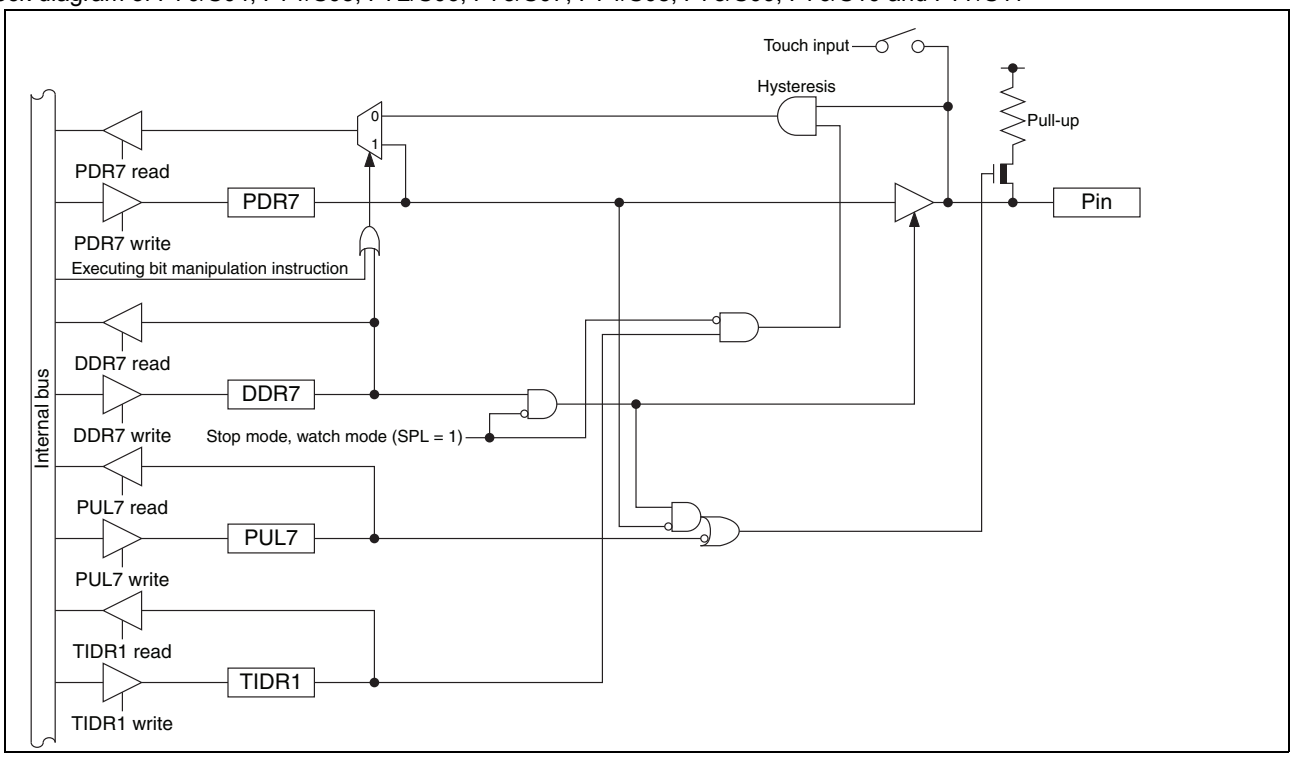
- P76/S10 pin

This pin has the following peripheral function:
  - TS touch ch. 10 input pin (S10)

- P77/S11 pin

This pin has the following peripheral function:
  - TS touch ch. 11 input pin (S11)

■ Block diagram of P70/S04, P71/S05, P72/S06, P73/S07, P74/S08, P75/S09, P76/S10 and P77/S11



3. Port 7 registers

■ Port 7 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR7	0	Pin state is “L” level.	PDR7 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR7 value is “1”.	As output port, outputs “H” level.
DDR7	0	Port input enabled		
	1	Port output enabled		
PUL7	0	Pull-up disabled		
	1	Pull-up enabled		
TIDR1	0	Touch input enabled		
	1	Port input enabled		

■ Correspondence between registers and pins for port 7

Pin name	Correspondence between related register bits and pins							
	P77	P76	P75	P74	P73	P72	P71	P70
PDR7	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DDR7								
PUL7								
TIDR1								

4. Port 7 operations

■ Operation as an output port
- ❒ A pin becomes an output port if the bit in the DDR7 register corresponding to that pin is set to “1”.
- ❒ When a pin is used as an output port, it outputs the value of the PDR7 register to external pins.
- ❒ If data is written to the PDR7 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
- ❒ Reading the PDR7 register returns the PDR7 register value.

■ Operation as an input port
- ❒ A pin becomes an input port if the bit in the DDR7 register corresponding to that pin is set to “0”.
- ❒ When using a pin shared with the touch input function as an input port, set the bit in the touch input disable register 1 (TIDR1) corresponding to that pin to “1”.
- ❒ If data is written to the PDR7 register, the value is stored in the output latch but is not output to the pin set as an input port.
- ❒ Reading the PDR7 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR7 register, the PDR7 register value is returned.

■ Operation at reset

If the CPU is reset, all bits in the DDR7 register are initialized to “0” and port input is enabled. As for a pin shared with the touch input function, its port input is disabled because the TIDR1 register is initialized to “0”.

■ Operation in stop mode and watch mode
- ❒ If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR7 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
- ❒ When the stop enable bit in the TS prescaler control register (PSC:STPE) is set to “1”, the TS can operate in stop mode or watch mode, the touch input is enabled and is not blocked. The TS wakes up in stop mode or watch mode provided that the TINT (touch interrupt) and the GINT (general interrupt) are set to enable the TS to wake up in stop mode or watch mode.
- ❒ If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

■ Operation as a touch input pin

Set the bit in the DDR7 register corresponding to the touch input pin to “0”, the bit in the TIDR1 register corresponding to the same pin to “0”, and the bit in the PUL7 register corresponding to the same pin to “0”.

■ Operation of the pull-up register

Setting the bit in the PUL7 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL7 register.

14.3.6 Port F

Port F is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

1. Port F configuration

■ Port F is made up of the following elements.
- ❒ General-purpose I/O pins/peripheral function I/O pins
- ❒ Port F data register (PDRF)
- ❒ Port F direction register (DDRF)

2. Block diagrams of port F

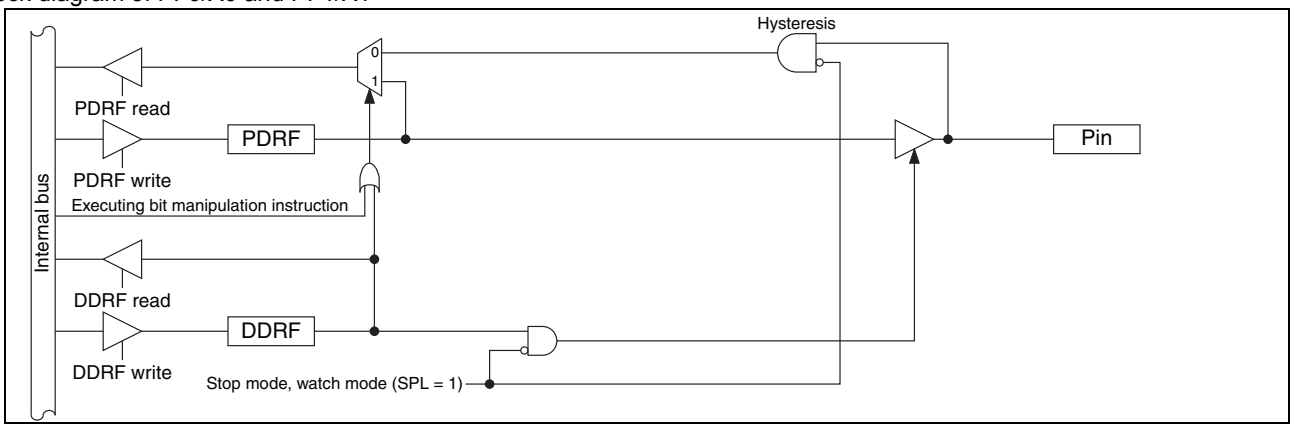
■ PF0/X0 pin

This pin has the following peripheral function:
- ❒ Main clock input oscillation pin (X0)

■ PF1/X1 pin

This pin has the following peripheral function:
- ❒ Main clock I/O oscillation pin (X1)

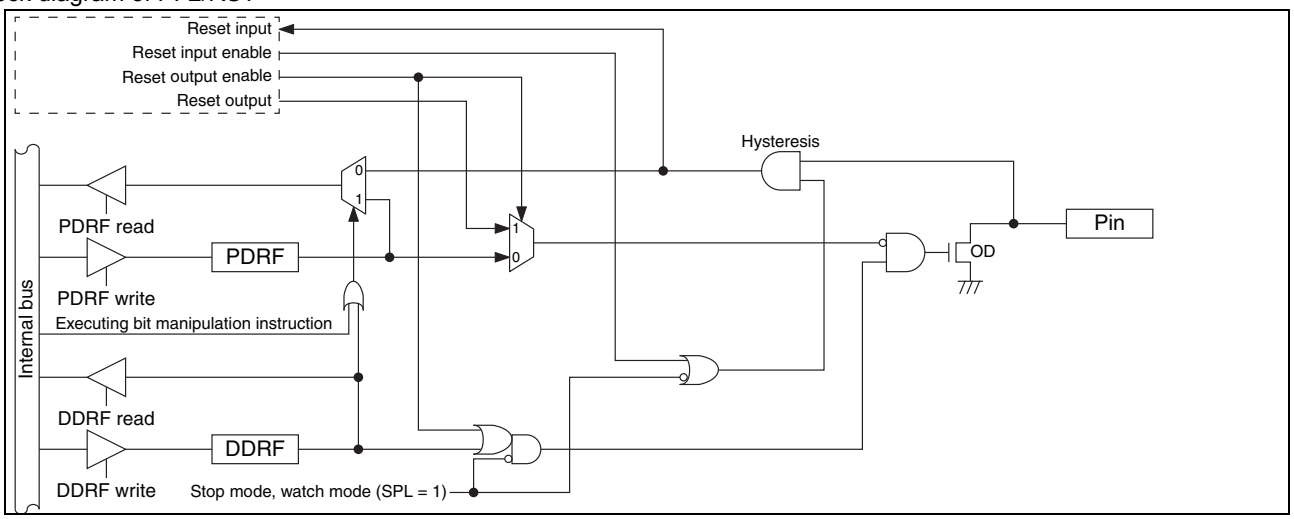
■ Block diagram of PF0/X0 and PF1/X1



■ PF2/$\overline{\text{RST}}$ pin

This pin has the following peripheral function:
- ❒ Reset pin ($\overline{\text{RST}}$)

■ Block diagram of PF2/$\overline{\text{RST}}$



3. Port F registers

■ Port F register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDRF	0	Pin state is “L” level.	PDRF value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDRF value is “1”.	As output port, outputs “H” level.*
DDRF	0	Port input enabled		
	1	Port output enabled		

*: If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

■ Correspondence between registers and pins for port F

Pin name	Correspondence between related register bits and pins							
	-	-	-	-	-	PF2	PF1	PF0
PDRF	-	-	-	-	-	bit2	bit1	bit0
DDRF								

4. Port F operations

■ Operation as an output port
- ❒ A pin becomes an output port if the bit in the DDRF register corresponding to that pin is set to “1”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ When a pin is used as an output port, it outputs the value of the PDRF register to external pins.
- ❒ If data is written to the PDRF register, the value is stored in the output latch and is output to the pin set as an output port as it is.
- ❒ Reading the PDRF register returns the PDRF register value.

■ Operation as an input port
- ❒ A pin becomes an input port if the bit in the DDRF register corresponding to that pin is set to “0”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ If data is written to the PDRF register, the value is stored in the output latch but is not output to the pin set as an input port.
- ❒ Reading the PDRF register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDRF register, the PDRF register value is returned.

■ Operation at reset

If the CPU is reset, all bits in the DDRF register are initialized to “0” and port input is enabled.

■ Operation in stop mode and watch mode
- ❒ If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRF register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
- ❒ If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

14.3.7 Port G

Port G is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

1. Port G configuration

■ Port G is made up of the following elements.
- ❒ General-purpose I/O pins/peripheral function I/O pins
- ❒ Port G data register (PDRG)
- ❒ Port G direction register (DDRG)
- ❒ Port G pull-up register (PULG)

2. Block diagram of port G

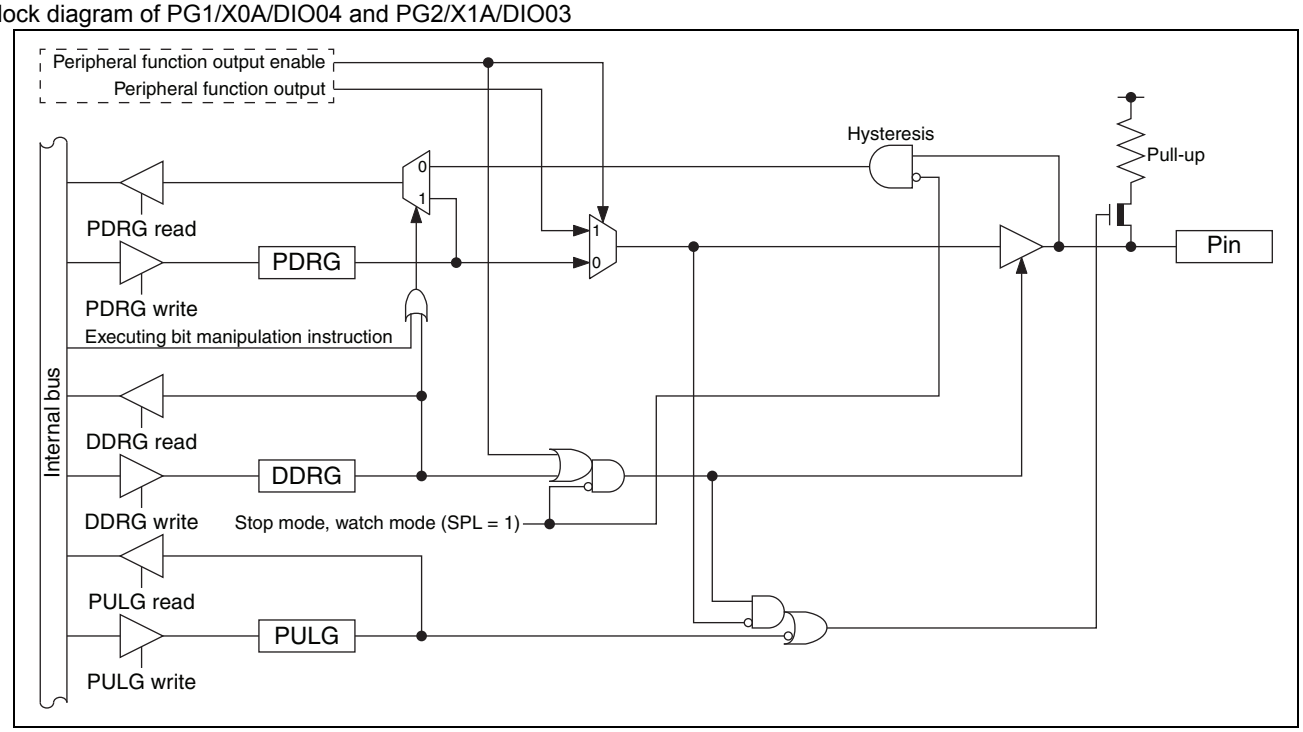
■ PG1/X0A/DIO04 pin

This pin has the following peripheral functions:
- ❒ Subclock input oscillation pin (X0A)
- ❒ TS direct output ch. 4 pin (DIO04)

■ PG2/X1A/DIO03 pin

This pin has the following peripheral functions:
- ❒ Subclock I/O oscillation pin (X1A)
- ❒ TS direct output ch. 3 pin (DIO03)

■ Block diagram of PG1/X0A/DIO04 and PG2/X1A/DIO03



3. Port G registers

■ Port G register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDRG	0	Pin state is “L” level.	PDRG value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDRG value is “1”.	As output port, outputs “H” level.
DDRG	0	Port input enabled		
	1	Port output enabled		
PULG	0	Pull-up disabled		
	1	Pull-up enabled		

■ Correspondence between registers and pins for port G

Pin name	Correspondence between related register bits and pins							
	-	-	-	-	-	PG2	PG1	-
PDRG	-	-	-	-	-	bit2	bit1	-
DDRG								
PULG								

4. Port G operations

■ Operation as an output port
- ❒ A pin becomes an output port if the bit in the DDRG register corresponding to that pin is set to “1”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ When a pin is used as an output port, it outputs the value of the PDRG register to external pins.
- ❒ If data is written to the PDRG register, the value is stored in the output latch and is output to the pin set as an output port as it is.
- ❒ Reading the PDRG register returns the PDRG register value.

■ Operation as an input port
- ❒ A pin becomes an input port if the bit in the DDRG register corresponding to that pin is set to “0”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ If data is written to the PDRG register, the value is stored in the output latch but is not output to the pin set as an input port.
- ❒ Reading the PDRG register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDRG register, the PDRG register value is returned.

■ Operation as a peripheral function output pin
- ❒ A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
- ❒ The pin value can be read from the PDRG register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDRG register. However, if the read-modify-write (RMW) type of instruction is used to read the PDRG register, the PDRG register value is returned.

■ Operation at reset

If the CPU is reset, all bits in the DDRG register are initialized to “0” and port input is enabled.

■ Operation in stop mode and watch mode
- ❒ If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRG register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
- ❒ If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

■ Operation of the pull-up register

Setting the bit in the PULG register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PULG register.

15. Interrupt Source Tables

15.1 MB95850K Series

Interrupt source	Interrupt request number	Vector table address		Interrupt level setting register		Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower	Register	Bit	
External interrupt ch. 0	IRQ00	0xFFFA	0xFFFB	ILR0	L00 [1:0]	High ↓ Low
External interrupt ch. 4						
External interrupt ch. 1	IRQ01	0xFFF8	0xFFF9	ILR0	L01 [1:0]	
External interrupt ch. 5						
External interrupt ch. 6	IRQ02	0xFFF6	0xFFF7	ILR0	L02 [1:0]	
External interrupt ch. 7	IRQ03	0xFFF4	0xFFF5	ILR0	L03 [1:0]	
UART/SIO ch. 0	IRQ04	0xFFF2	0xFFF3	ILR1	L04 [1:0]	
8/16-bit composite timer ch. 0 (lower)	IRQ05	0xFFF0	0xFFF1	ILR1	L05 [1:0]	
8/16-bit composite timer ch. 0 (upper)	IRQ06	0xFFEE	0xFFEF	ILR1	L06 [1:0]	
Touch interrupt (TINT)	IRQ07	0xFFEC	0xFFED	ILR1	L07 [1:0]	
General interrupt (GINT)	IRQ08	0xFFEA	0xFFEB	ILR2	L08 [1:0]	
—	IRQ09	0xFFE8	0xFFE9	ILR2	L09 [1:0]	
—	IRQ10	0xFFE6	0xFFE7	ILR2	L10 [1:0]	
—	IRQ11	0xFFE4	0xFFE5	ILR2	L11 [1:0]	
8/16-bit PPG ch. 0 (upper)	IRQ12	0xFFE2	0xFFE3	ILR3	L12 [1:0]	
8/16-bit PPG ch. 0 (lower)	IRQ13	0xFFE0	0xFFE1	ILR3	L13 [1:0]	
—	IRQ14	0xFFDE	0xFFDF	ILR3	L14 [1:0]	
—	IRQ15	0xFFDC	0xFFDD	ILR3	L15 [1:0]	
I^2C bus interface ch. 0	IRQ16	0xFFDA	0xFFDB	ILR4	L16 [1:0]	
—	IRQ17	0xFFD8	0xFFD9	ILR4	L17 [1:0]	
8/10-bit A/D converter	IRQ18	0xFFD6	0xFFD7	ILR4	L18 [1:0]	
Time-base timer	IRQ19	0xFFD4	0xFFD5	ILR4	L19 [1:0]	
Watch prescaler	IRQ20	0xFFD2	0xFFD3	ILR5	L20 [1:0]	
Watch counter						
Comparator ch. 0	IRQ21	0xFFD0	0xFFD1	ILR5	L21 [1:0]	
—	IRQ22	0xFFCE	0xFFCF	ILR5	L22 [1:0]	
Flash memory	IRQ23	0xFFCC	0xFFCD	ILR5	L23 [1:0]	

15.2 MB95860K Series

Interrupt source	Interrupt request number	Vector table address		Interrupt level setting register		Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower	Register	Bit	
External interrupt ch. 0	IRQ00	0xFFFA	0xFFFB	ILR0	L00 [1:0]	High ↓ Low
External interrupt ch. 4						
External interrupt ch. 1	IRQ01	0xFFF8	0xFFF9	ILR0	L01 [1:0]	
External interrupt ch. 5						
External interrupt ch. 2	IRQ02	0xFFF6	0xFFF7	ILR0	L02 [1:0]	
External interrupt ch. 6						
External interrupt ch. 3	IRQ03	0xFFF4	0xFFF5	ILR0	L03 [1:0]	
External interrupt ch. 7						
UART/SIO ch. 0	IRQ04	0xFFF2	0xFFF3	ILR1	L04 [1:0]	
8/16-bit composite timer ch. 0 (lower)	IRQ05	0xFFF0	0xFFF1	ILR1	L05 [1:0]	
8/16-bit composite timer ch. 0 (upper)	IRQ06	0xFFEE	0xFFEF	ILR1	L06 [1:0]	
Touch interrupt (TINT)	IRQ07	0xFFEC	0xFFED	ILR1	L07 [1:0]	
General interrupt (GINT)	IRQ08	0xFFEA	0xFFEB	ILR2	L08 [1:0]	
8/16-bit PPG ch. 1 (lower)	IRQ09	0xFFE8	0xFFE9	ILR2	L09 [1:0]	
8/16-bit PPG ch. 1 (upper)	IRQ10	0xFFE6	0xFFE7	ILR2	L10 [1:0]	
—	IRQ11	0xFFE4	0xFFE5	ILR2	L11 [1:0]	
8/16-bit PPG ch. 0 (upper)	IRQ12	0xFFE2	0xFFE3	ILR3	L12 [1:0]	
8/16-bit PPG ch. 0 (lower)	IRQ13	0xFFE0	0xFFE1	ILR3	L13 [1:0]	
8/16-bit composite timer ch. 1 (upper)	IRQ14	0xFFDE	0xFFDF	ILR3	L14 [1:0]	
—	IRQ15	0xFFDC	0xFFDD	ILR3	L15 [1:0]	
I^2C bus interface ch. 0	IRQ16	0xFFDA	0xFFDB	ILR4	L16 [1:0]	
—	IRQ17	0xFFD8	0xFFD9	ILR4	L17 [1:0]	
8/10-bit A/D converter	IRQ18	0xFFD6	0xFFD7	ILR4	L18 [1:0]	
Time-base timer	IRQ19	0xFFD4	0xFFD5	ILR4	L19 [1:0]	
Watch prescaler	IRQ20	0xFFD2	0xFFD3	ILR5	L20 [1:0]	
Watch counter						
Comparator ch. 0	IRQ21	0xFFD0	0xFFD1	ILR5	L21 [1:0]	
8/16-bit composite timer ch. 1 (lower)	IRQ22	0xFFCE	0xFFCF	ILR5	L22 [1:0]	
Flash memory	IRQ23	0xFFCC	0xFFCD	ILR5	L23 [1:0]	

15.3 MB95870K Series

Interrupt source	Interrupt request number	Vector table address		Interrupt level setting register		Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower	Register	Bit	
External interrupt ch. 0	IRQ00	0xFFFA	0xFFFB	ILR0	L00 [1:0]	High ↑
External interrupt ch. 4						
External interrupt ch. 1	IRQ01	0xFFF8	0xFFF9	ILR0	L01 [1:0]	
External interrupt ch. 5						
External interrupt ch. 2	IRQ02	0xFFF6	0xFFF7	ILR0	L02 [1:0]	
External interrupt ch. 6						
External interrupt ch. 3	IRQ03	0xFFF4	0xFFF5	ILR0	L03 [1:0]	
External interrupt ch. 7						
UART/SIO ch. 0	IRQ04	0xFFF2	0xFFF3	ILR1	L04 [1:0]	
8/16-bit composite timer ch. 0 (lower)	IRQ05	0xFFF0	0xFFF1	ILR1	L05 [1:0]	
8/16-bit composite timer ch. 0 (upper)	IRQ06	0xFFEE	0xFFEF	ILR1	L06 [1:0]	
Touch interrupt (TINT)	IRQ07	0xFFEC	0xFFED	ILR1	L07 [1:0]	
General interrupt (GINT)	IRQ08	0xFFEA	0xFFEB	ILR2	L08 [1:0]	
8/16-bit PPG ch. 1 (lower)	IRQ09	0xFFE8	0xFFE9	ILR2	L09 [1:0]	
8/16-bit PPG ch. 1 (upper)	IRQ10	0xFFE6	0xFFE7	ILR2	L10 [1:0]	
8/16-bit PPG ch. 2 (upper)	IRQ11	0xFFE4	0xFFE5	ILR2	L11 [1:0]	
8/16-bit PPG ch. 0 (upper)	IRQ12	0xFFE2	0xFFE3	ILR3	L12 [1:0]	
8/16-bit PPG ch. 0 (lower)	IRQ13	0xFFE0	0xFFE1	ILR3	L13 [1:0]	
8/16-bit composite timer ch. 1 (upper)	IRQ14	0xFFDE	0xFFDF	ILR3	L14 [1:0]	
8/16-bit PPG ch. 2 (lower)	IRQ15	0xFFDC	0xFFDD	ILR3	L15 [1:0]	
I^2C bus interface ch. 0	IRQ16	0xFFDA	0xFFDB	ILR4	L16 [1:0]	
External interrupt ch. 8	IRQ17	0xFFD8	0xFFD9	ILR4	L17 [1:0]	
External interrupt ch. 9						
8/10-bit A/D converter	IRQ18	0xFFD6	0xFFD7	ILR4	L18 [1:0]	
Time-base timer	IRQ19	0xFFD4	0xFFD5	ILR4	L19 [1:0]	
Watch prescaler	IRQ20	0xFFD2	0xFFD3	ILR5	L20 [1:0]	
Watch counter						
Comparator ch. 0	IRQ21	0xFFD0	0xFFD1	ILR5	L21 [1:0]	
8/16-bit composite timer ch. 1 (lower)	IRQ22	0xFFCE	0xFFCF	ILR5	L22 [1:0]	
Flash memory	IRQ23	0xFFCC	0xFFCD	ILR5	L23 [1:0]	↓ Low

16. Pin States in Each Mode

16.1 MB95850K Series

Pin name	Normal operation	Sleep mode	Stop mode		Watch mode		On reset
			SPL=0	SPL=1	SPL=0	SPL=1	
PF0/X0	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	—
	I/O port*1	I/O port*1	Previous state kept Input blocked*1, *2	Hi-Z Input blocked*1, *2	Previous state kept Input blocked*1, *2	Hi-Z Input blocked*1, *2	Hi-Z Input enabled*3 (However, it does not function.)
PF1/X1	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	—
	I/O port*1	I/O port*1	Previous state kept Input blocked*1, *2	Hi-Z Input blocked*1, *2	Previous state kept Input blocked*1, *2	Hi-Z Input blocked*1, *2	Hi-Z Input enabled*3 (However, it does not function.)
PF2/$\overline{\text{RST}}$	Reset input*4	Reset input*4	Reset input	Reset input	Reset input	Reset input	Reset input*4
	I/O port	I/O port	Previous state kept Input blocked*1, *2	Hi-Z Input blocked*1, *2	Previous state kept Input blocked*1, *2	Hi-Z Input blocked*1, *2	Hi-Z Input enabled*3 (However, it does not function.)
PG1/X0A/ DIO04	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	—
	I/O port*1/ peripheral function I/O	I/O port*1/ peripheral function I/O	Previous state kept*5 Input blocked*1, *2	Hi-Z*6 Input blocked*1, *2	Previous state kept*5 Input blocked*1, *2	Hi-Z*6 Input blocked*1, *2	Hi-Z Input enabled*3 (However, it does not function.)
PG2/X1A/ DIO03	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	—
	I/O port*1/ peripheral function I/O	I/O port*1/ peripheral function I/O	Previous state kept*5 Input blocked*1, *2	Hi-Z*6 Input blocked*1, *2	Previous state kept*5 Input blocked*1, *2	Hi-Z*6 Input blocked*1, *2	Hi-Z Input enabled*3 (However, it does not function.)
P04/AN00/ BEEP/ DIO01/TO01	I/O port/ peripheral function I/O/ analog input	I/O port/ peripheral function I/O/ analog input	Previous state kept*5, *10 Input blocked*2	Hi-Z*6 Input blocked*2	Previous state kept*5, *10 Input blocked*2	Hi-Z*6 Input blocked*2	Hi-Z Input blocked*2
P05/INT05/ AN01/ CMP0_N/ TO00	I/O port/ peripheral function I/O/ analog input	I/O port/ peripheral function I/O/ analog input	Previous state kept Input blocked*2, *7, *8	Hi-Z*6 Input blocked*2, *7, *8	Previous state kept Input blocked*2, *7, *8	Hi-Z*6 Input blocked*2, *7, *8	Hi-Z Input blocked*2
P06/AN02/ CMP0_O/ PPG00	I/O port/ peripheral function I/O/ analog input	I/O port/ peripheral function I/O/ analog input	Previous state kept*9 Input blocked*2	Hi-Z*6 Input blocked*2	Previous state kept*9 Input blocked*2	Hi-Z*6 Input blocked*2	Hi-Z Input blocked*2
P07/AN03/ CMP0_P/ PPG01	I/O port/ peripheral function I/O/ analog input	I/O port/ peripheral function I/O/ analog input	Previous state kept Input blocked*2, *8	Hi-Z*6 Input blocked*2, *8	Previous state kept Input blocked*2, *8	Hi-Z*6 Input blocked*2, *8	Hi-Z Input blocked*2
P10/DBG/ EC0	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	Previous state kept Input blocked*2, *7	Hi-Z Input blocked*2, *7	Previous state kept Input blocked*2, *7	Hi-Z Input blocked*2, *7	Hi-Z Input enabled*3 (However, it does not function.)
P13/INT04/UI0/DI O02	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	Previous state kept*5 Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Previous state kept*5 Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Hi-Z Input enabled*3 (However, it does not function.)
P14/INT01/UO0/D IO00	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	Previous state kept*5 Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Previous state kept*5 Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Hi-Z Input enabled*3 (However, it does not function.)
P15/INT00/UCK0	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	Previous state kept Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Previous state kept Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Hi-Z Input enabled*3 (However, it does not function.)

Pin name	Normal operation	Sleep mode	Stop mode		Watch mode		On reset
			SPL=0	SPL=1	SPL=0	SPL=1	
P46/INT06/ SDA	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	Previous state kept Input blocked*2, *7, *11	Hi-Z Input blocked*2, *7, *11	Previous state kept Input blocked*2, *7, *11	Hi-Z Input blocked*2, *7, *11	Hi-Z Input enabled*3 (However, it does not function.)
P47/INT07/ SCL							
P63/AREF	I/O port/ touch input	I/O port/ touch input	Previous state kept*12 Input blocked*2, *13	Hi-Z*12 Input blocked*2, *13	Previous state kept*12 Input blocked*2, *13	Hi-Z*12 Input blocked*2, *13	Hi-Z Input blocked*2
P65/S01							
P66/S02							
P67/S03							
P70/S04							
P71/S05							

SPL: Pin state setting bit in the standby control register (STBC:SPL)
Hi-Z: High impedance
*1: The pin stays at the state shown when configured as a general-purpose I/O port.
*2: “Input blocked” means direct input gate operation from the pin is disabled.
*3: “Input enabled” means that the input function is enabled. While the input function is enabled, a pull-up or pull-down operation has to be performed in order to prevent leaks due to external input. If a pin is used as an output port, its pin state is the same as that of other ports.
*4: The PF2/$\overline{\text{RST}}$ pin stays at the state shown when configured as a reset pin.
*5: In stop mode and watch mode, the pin functions as a TS direct output pin only when the SPL bit is set to “0” and the TS direct output function is enabled.
*6: The pull-up control setting is still effective.
*7: Though input is blocked, an external interrupt can be input when the external interrupt request is enabled.
*8: Though input is blocked, an analog signal can be input to generate a comparator interrupt when the comparator interrupt is enabled.
*9: In stop mode and watch mode, comparator input varies according to the register settings of the comparator, and the pin functions as a comparator output pin only when the SPL bit is set to “0” and the comparator output function is enabled.
*10: In stop mode and watch mode, the pin functions as a beep output pin only when the SPL bit is set to “0” and the beep output function is enabled.
*11: The I^2C bus interface can wake up the MCU in stop mode or watch mode when its MCU standby mode wakeup function is enabled. For details of the MCU standby mode wakeup function, refer to “CHAPTER 21 I^2C BUS INTERFACE” in “New 8FX MB95850K/860K/870K Series Hardware Manual”.
*12: In stop mode and watch mode, the pin outputs SNCLK only when it is used as a TS touch input pin and the TS is in operation.
*13: Though input is blocked, a touch signal can be input to generate a touch interrupt (TINT) when the TINT is enabled.

16.2 MB95860K Series

Pin name	Normal operation	Sleep mode	Stop mode		Watch mode		On reset
			SPL=0	SPL=1	SPL=0	SPL=1	
PF0/X0	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	—
	I/O port*1	I/O port*1	Previous state kept Input blocked*1, *2	Hi-Z Input blocked*1, *2	Previous state kept Input blocked*1, *2	Hi-Z Input blocked*1, *2	Hi-Z Input enabled*3 (However, it does not function.)
PF1/X1	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	—
	I/O port*1	I/O port*1	Previous state kept Input blocked*1, *2	Hi-Z Input blocked*1, *2	Previous state kept Input blocked*1, *2	Hi-Z Input blocked*1, *2	Hi-Z Input enabled*3 (However, it does not function.)
PF2/$\overline{\text{RST}}$	Reset input*4	Reset input*4	Reset input	Reset input	Reset input	Reset input	Reset input*4
	I/O port	I/O port	Previous state kept Input blocked*1, *2	Hi-Z Input blocked*1, *2	Previous state kept Input blocked*1, *2	Hi-Z Input blocked*1, *2	Hi-Z Input enabled*3 (However, it does not function.)
PG1/X0A/ DIO04	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	—
	I/O port*1/ peripheral function I/O	I/O port*1/ peripheral function I/O	Previous state kept*5 Input blocked*1, *2	Hi-Z*6 Input blocked*1, *2	Previous state kept*5 Input blocked*1, *2	Hi-Z*6 Input blocked*1, *2	Hi-Z Input enabled*3 (However, it does not function.)
PG2/X1A/ DIO03	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	—
	I/O port*1/ peripheral function I/O	I/O port*1/ peripheral function I/O	Previous state kept*5 Input blocked*1, *2	Hi-Z*6 Input blocked*1, *2	Previous state kept*5 Input blocked*1, *2	Hi-Z*6 Input blocked*1, *2	Hi-Z Input enabled*3 (However, it does not function.)
P02/INT02/ TO10	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	Previous state kept Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Previous state kept Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Hi-Z Input enabled*3 (However, it does not function.)
P03/INT03/ TO11							
P04/AN00/ BEEP/ DIO01	I/O port/ peripheral function I/O/ analog input	I/O port/ peripheral function I/O/ analog input	Previous state kept*5, *10 Input blocked*2	Hi-Z*6 Input blocked*2	Previous state kept*5, *10 Input blocked*2	Hi-Z*6 Input blocked*2	Hi-Z Input blocked*2
P05/INT05/ AN01/ CMP0_N	I/O port/ peripheral function I/O/ analog input	I/O port/ peripheral function I/O/ analog input	Previous state kept Input blocked*2, *7, *8	Hi-Z*6 Input blocked*2, *7, *8	Previous state kept Input blocked*2, *7, *8	Hi-Z*6 Input blocked*2, *7, *8	Hi-Z Input blocked*2
P06/AN02/ CMP0_O/ PPG00	I/O port/ peripheral function I/O/ analog input	I/O port/ peripheral function I/O/ analog input	Previous state kept*9 Input blocked*2	Hi-Z*6 Input blocked*2	Previous state kept*9 Input blocked*2	Hi-Z*6 Input blocked*2	Hi-Z Input blocked*2
P07/AN03/ CMP0_P/ PPG01	I/O port/ peripheral function I/O/ analog input	I/O port/ peripheral function I/O/ analog input	Previous state kept Input blocked*2, *8	Hi-Z*6 Input blocked*2, *8	Previous state kept Input blocked*2, *8	Hi-Z*6 Input blocked*2, *8	Hi-Z Input blocked*2
P10/DBG/ EC0	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	Previous state kept Input blocked*2, *7	Hi-Z Input blocked*2, *7	Previous state kept Input blocked*2, *7	Hi-Z Input blocked*2, *7	Hi-Z Input enabled*3 (However, it does not function.)
P13/INT04/UI0/DI O02	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	Previous state kept*5 Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Previous state kept*5 Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Hi-Z Input enabled*3 (However, it does not function.)
P14/INT01/UO0	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	Previous state kept Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Previous state kept Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Hi-Z Input enabled*3 (However, it does not function.)

Pin name	Normal operation	Sleep mode	Stop mode		Watch mode		On reset
			SPL=0	SPL=1	SPL=0	SPL=1	
P15/INT00/UCK0	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	Previous state kept Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Previous state kept Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Hi-Z Input enabled*3 (However, it does not function.)
P44/AN06/ TO00/ DIO03/ PPG10	I/O port/ peripheral function I/O/ analog input	I/O port/ peripheral function I/O/ analog input	Previous state kept*5 Input blocked*2	Hi-Z*6 Input blocked*2	Previous state kept*5 Input blocked*2	Hi-Z*6 Input blocked*2	Hi-Z Input blocked*2
P45/AN07/ TO01/ DIO04/ PPG11							
P46/INT06/ SDA	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	Previous state kept Input blocked*2, *7, *11	Hi-Z Input blocked*2, *7, *11	Previous state kept Input blocked*2, *7, *11	Hi-Z Input blocked*2, *7, *11	Hi-Z Input enabled*3 (However, it does not function.)
P47/INT07/ SCL							
P60/EC1/ DIO00	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	Previous state kept*5 Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Previous state kept*5 Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Hi-Z Input enabled*3 (However, it does not function.)
P63/AREF	I/O port/ touch input	I/O port/ touch input	Previous state kept*12 Input blocked*2, *13	Hi-Z*12 Input blocked*2, *13	Previous state kept*12 Input blocked*2, *13	Hi-Z*12 Input blocked*2, *13	Hi-Z Input blocked*2
P64/S00							
P65/S01							
P66/S02							
P67/S03							
P70/S04							
P71/S05							
P72/S06							
P73/S07							

SPL: Pin state setting bit in the standby control register (STBC:SPL)
Hi-Z: High impedance

*1: The pin stays at the state shown when configured as a general-purpose I/O port.
*2: “Input blocked” means direct input gate operation from the pin is disabled.
*3: “Input enabled” means that the input function is enabled. While the input function is enabled, a pull-up or pull-down operation has to be performed in order to prevent leaks due to external input. If a pin is used as an output port, its pin state is the same as that of other ports.
*4: The PF2/$\overline{\text{RST}}$ pin stays at the state shown when configured as a reset pin.
*5: In stop mode and watch mode, the pin functions as a TS direct output pin only when the SPL bit is set to “0” and the TS direct output function is enabled.
*6: The pull-up control setting is still effective.
*7: Though input is blocked, an external interrupt can be input when the external interrupt request is enabled.
*8: Though input is blocked, an analog signal can be input to generate a comparator interrupt when the comparator interrupt is enabled.
*9: In stop mode and watch mode, comparator input varies according to the register settings of the comparator, and the pin functions as a comparator output pin only when the SPL bit is set to “0” and the comparator output function is enabled.
*10: In stop mode and watch mode, the pin functions as a beep output pin only when the SPL bit is set to “0” and the beep output function is enabled.
*11: The I^2C bus interface can wake up the MCU in stop mode or watch mode when its MCU standby mode wakeup function is enabled. For details of the MCU standby mode wakeup function, refer to “CHAPTER 21 I^2C BUS INTERFACE” in “New 8FX MB95850K/860K/870K Series Hardware Manual”.
*12: In stop mode and watch mode, the pin outputs SNCLK only when it is used as a TS touch input pin and the TS is in operation.
*13: Though input is blocked, a touch signal can be input to generate a touch interrupt (TINT) when the TINT is enabled.

16.3 MB95870K Series

Pin name	Normal operation	Sleep mode	Stop mode		Watch mode		On reset
			SPL=0	SPL=1	SPL=0	SPL=1	
PF0/X0	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	—
	I/O port*1	I/O port*1	Previous state kept Input blocked*1, *2	Hi-Z Input blocked*1, *2	Previous state kept Input blocked*1, *2	Hi-Z Input blocked*1, *2	Hi-Z Input enabled*3 (However, it does not function.)
PF1/X1	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	—
	I/O port*1	I/O port*1	Previous state kept Input blocked*1, *2	Hi-Z Input blocked*1, *2	Previous state kept Input blocked*1, *2	Hi-Z Input blocked*1, *2	Hi-Z Input enabled*3 (However, it does not function.)
PF2/$\overline{\text{RST}}$	Reset input*4	Reset input*4	Reset input	Reset input	Reset input	Reset input	Reset input*4
	I/O port	I/O port	Previous state kept Input blocked*1, *2	Hi-Z Input blocked*1, *2	Previous state kept Input blocked*1, *2	Hi-Z Input blocked*1, *2	Hi-Z Input enabled*3 (However, it does not function.)
PG1/X0A/ DIO04	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	—
	I/O port*1/ peripheral function I/O	I/O port*1/ peripheral function I/O	Previous state kept*5 Input blocked*1, *2	Hi-Z*6 Input blocked*1, *2	Previous state kept*5 Input blocked*1, *2	Hi-Z*6 Input blocked*1, *2	Hi-Z Input enabled*3 (However, it does not function.)
PG2/X1A/ DIO03	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	—
	I/O port*1/ peripheral function I/O	I/O port*1/ peripheral function I/O	Previous state kept*5 Input blocked*1, *2	Hi-Z*6 Input blocked*1, *2	Previous state kept*5 Input blocked*1, *2	Hi-Z*6 Input blocked*1, *2	Hi-Z Input enabled*3 (However, it does not function.)
P00/INT00	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	Previous state kept Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Previous state kept Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Hi-Z Input enabled*3 (However, it does not function.)
P01/INT01							
P02/INT02							
P03/INT03							
P04/INT04/ AN00	I/O port/ peripheral function I/O/ analog input	I/O port/ peripheral function I/O/ analog input	Previous state kept Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Previous state kept Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Hi-Z Input blocked*2
P05/INT05/ AN01/ CMP0_N	I/O port/ peripheral function I/O/ analog input	I/O port/ peripheral function I/O/ analog input	Previous state kept Input blocked*2, *7, *8	Hi-Z*6 Input blocked*2, *7, *8	Previous state kept Input blocked*2, *7, *8	Hi-Z*6 Input blocked*2, *7, *8	Hi-Z Input blocked*2
P06/AN02/ CMP0_O	I/O port/ peripheral function I/O/ analog input	I/O port/ peripheral function I/O/ analog input	Previous state kept*9 Input blocked*2	Hi-Z*6 Input blocked*2	Previous state kept*9 Input blocked*2	Hi-Z*6 Input blocked*2	Hi-Z Input blocked*2
P07/AN03/ CMP0_P	I/O port/ analog input	I/O port/ analog input	Previous state kept Input blocked*2, *8	Hi-Z*6 Input blocked*2, *8	Previous state kept Input blocked*2, *8	Hi-Z*6 Input blocked*2, *8	Hi-Z Input blocked*2
P10/DBG	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	Previous state kept Input blocked*2	Hi-Z Input blocked*2	Previous state kept Input blocked*2	Hi-Z Input blocked*2	Hi-Z Input enabled*3 (However, it does not function.)
P11/EC0/ DIO01	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	Previous state kept*5 Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Previous state kept*5 Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Hi-Z Input enabled*3 (However, it does not function.)

Pin name	Normal operation	Sleep mode	Stop mode		Watch mode		On reset
			SPL=0	SPL=1	SPL=0	SPL=1	
P12/BEEP	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	Previous state kept*10 Input blocked*2	Hi-Z*6 Input blocked*2	Previous state kept*10 Input blocked*2	Hi-Z*6 Input blocked*2	Hi-Z Input enabled*3 (However, it does not function.)
P13/UI0/ DIO02	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	Previous state kept*5 Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Previous state kept*5 Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Hi-Z Input enabled*3 (However, it does not function.)
P14/UO0	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	Previous state kept Input blocked*2	Hi-Z*6 Input blocked*2	Previous state kept Input blocked*2	Hi-Z*6 Input blocked*2	Hi-Z Input enabled*3 (However, it does not function.)
P15/UCK0	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	Previous state kept Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Previous state kept Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Hi-Z Input enabled*3 (However, it does not function.)
P16/INT09/ TO11	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	Previous state kept Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Previous state kept Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Hi-Z Input enabled*3 (However, it does not function.)
P17/INT08/ TO10							
P40/AN04/ PPG00	I/O port/ peripheral function I/O/ analog input	I/O port/ peripheral function I/O/ analog input	Previous state kept Input blocked*2	Hi-Z*6 Input blocked*2	Previous state kept Input blocked*2	Hi-Z*6 Input blocked*2	Hi-Z Input blocked*2
P41/AN05/ PPG01							
P42/INT06/ PPG10	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	Previous state kept Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Previous state kept Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Hi-Z Input enabled*3 (However, it does not function.)
P43/INT07/ PPG11							
P44/AN06/ TO00/DIO03	I/O port/ peripheral function I/O/ analog input	I/O port/ peripheral function I/O/ analog input	Previous state kept*5 Input blocked*2	Hi-Z*6 Input blocked*2	Previous state kept*5 Input blocked*2	Hi-Z*6 Input blocked*2	Hi-Z Input blocked*2
P45/AN07/ TO01/DIO04							
P46/SDA	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	Previous state kept Input blocked*2, *11	Hi-Z Input blocked*2, *11	Previous state kept Input blocked*2, *11	Hi-Z Input blocked*2, *11	Hi-Z Input enabled*3 (However, it does not function.)
P47/SCL							
P60/EC1/ DIO00	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	Previous state kept*5 Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Previous state kept*5 Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Hi-Z Input enabled*3 (However, it does not function.)
P61/PPG20	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	Previous state kept Input blocked*2	Hi-Z*6 Input blocked*2	Previous state kept Input blocked*2	Hi-Z*6 Input blocked*2	Hi-Z Input enabled*3 (However, it does not function.)
P62/PPG21							

Pin name	Normal operation	Sleep mode	Stop mode		Watch mode		On reset
			SPL=0	SPL=1	SPL=0	SPL=1	
P63/AREF	I/O port/ touch input	I/O port/ touch input	Previous state kept*12 Input blocked*2, *13	Hi-Z*12 Input blocked*2, *13	Previous state kept*12 Input blocked*2, *13	Hi-Z*12 Input blocked*2, *13	Hi-Z Input blocked*2
P64/S00							
P65/S01							
P66/S02							
P67/S03							
P70/S04							
P71/S05							
P72/S06							
P73/S07							
P74/S08							
P75/S09							
P76/S10							
P77/S11							

SPL: Pin state setting bit in the standby control register (STBC:SPL)
Hi-Z: High impedance

*1: The pin stays at the state shown when configured as a general-purpose I/O port.
*2: “Input blocked” means direct input gate operation from the pin is disabled.
*3: “Input enabled” means that the input function is enabled. While the input function is enabled, a pull-up or pull-down operation has to be performed in order to prevent leaks due to external input. If a pin is used as an output port, its pin state is the same as that of other ports.
*4: The PF2/$\overline{\text{RST}}$ pin stays at the state shown when configured as a reset pin.
*5: In stop mode and watch mode, the pin functions as a TS direct output pin only when the SPL bit is set to “0” and the TS direct output function is enabled.
*6: The pull-up control setting is still effective.
*7: Though input is blocked, an external interrupt can be input when the external interrupt request is enabled.
*8: Though input is blocked, an analog signal can be input to generate a comparator interrupt when the comparator interrupt is enabled.
*9: In stop mode and watch mode, comparator input varies according to the register settings of the comparator, and the pin functions as a comparator output pin only when the SPL bit is set to “0” and the comparator output function is enabled.
*10: In stop mode and watch mode, the pin functions as a beep output pin only when the SPL bit is set to “0” and the beep output function is enabled.
*11: The I^2C bus interface can wake up the MCU in stop mode or watch mode when its MCU standby mode wakeup function is enabled. For details of the MCU standby mode wakeup function, refer to “CHAPTER 21 I^2C BUS INTERFACE” in “New 8FX MB95850K/860K/870K Series Hardware Manual”.
*12: In stop mode and watch mode, the pin outputs SNCLK only when it is used as a TS touch input pin and the TS is in operation.
*13: Though input is blocked, a touch signal can be input to generate a touch interrupt (TINT) when the TINT is enabled.

17. Electrical Characteristics

17.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} − 0.3	V_{SS} + 6	V	
Input voltage*1	V_I	V_{SS} − 0.3	V_{SS} + 6	V	*2
Output voltage*1	V_O	V_{SS} − 0.3	V_{SS} + 6	V	*2
Maximum clamp current	I_{CLAMP}	−2	+2	mA	Applicable to specific pins*3
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	—	20	mA	Applicable to specific pins*3
“L” level maximum output current	I_{OL}	—	15	mA	
“L” level average current	I_{OLAV1}	—	4	mA	For pins other than P06, P07, P40 to P45 Average output current = operating current × operating ratio (1 pin)
	I_{OLAV2}		12		For P06, P07, P40 to P45 Average output current = operating current × operating ratio (1 pin)
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	37	mA	Total average output current = operating current × operating ratio (Total number of pins)
“H” level maximum output current	I_{OH}	—	−15	mA	
“H” level average current	I_{OHAV1}	—	−4	mA	For pins other than P06, P07, P40 to P45 Average output current = operating current × operating ratio (1 pin)
	I_{OHAV2}		−8		For P06, P07, P40 to P45 Average output current = operating current × operating ratio (1 pin)
“H” level total maximum output current	ΣI_{OH}	—	−100	mA	
“H” level total average output current	ΣI_{OHAV}	—	−47	mA	Total average output current = operating current × operating ratio (Total number of pins)
Power consumption	P_d	—	320	mW	
Operating temperature	T_A	−40	+85	°C	
Storage temperature	T_{stg}	−55	+150	°C	
Operating humidity	H_{opr}	5	95	%	
Electrostatic discharge (human-body model)	HBM	—	8000	V	For the TS touch input pins: S00 to S11

*1: These parameters are based on the condition that V_{SS} is 0.0 V.

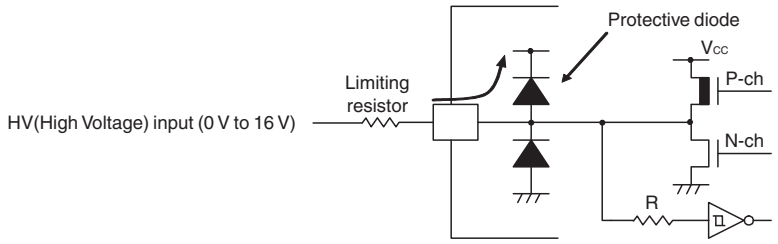
*2: V_1 and V_0 must not exceed V_{CC} + 0.3 V. V_1 must not exceed the rated voltage. However, if the maximum current to/from an input is limited by means of an external component, the I_{CLAMP} rating is used instead of the V_I rating.

*3: Specific pins: P00 to P07, P11 to P17, P40 to P45, P60 to P67, P70 to P77, PF0, PF1, PG1, PG2

- Use under recommended operating conditions.
- Use with DC voltage (current).
- The HV (High Voltage) signal is an input signal exceeding the V_{CC} voltage. Always connect a limiting resistor between the HV (High Voltage) signal and the microcontroller before applying the HV (High Voltage) signal.
- The value of the limiting resistor should be set to a value at which the current to be input to the microcontroller pin when the HV (High Voltage) signal is input is below the standard value, irrespective of whether the current is transient current or stationary current.

- When the microcontroller drive current is low, such as in low power consumption modes, the HV (High Voltage) input potential may pass through the protective diode to increase the potential of the V_{CC} pin, affecting other devices.
- If the HV (High Voltage) signal is input when the microcontroller power supply is off (not fixed at 0 V), since power is supplied from the pins, incomplete operations may be executed.
- If the HV (High Voltage) input is input after power-on, since power is supplied from the pins, the voltage of power supply may not be sufficient to enable a power-on reset.
- Do not leave the HV (High Voltage) input pin unconnected.
- Example of a recommended circuit:

Input/Output equivalent circuit



Warning: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

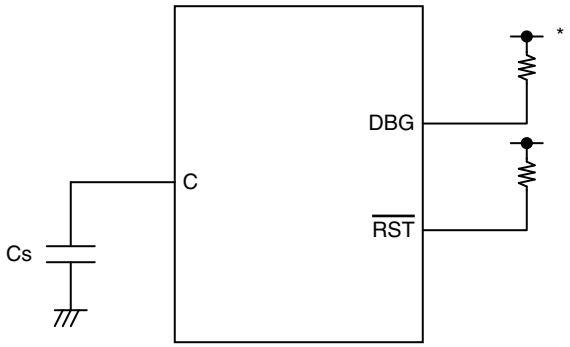
17.2 Recommended Operating Conditions

(V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	2.88	5.5	V	When the device is powered on or in on-chip debug mode, or when the LVD reset circuit is enabled
		2.4	5.5		When the LVD reset circuit is disabled
		2.3	5.5		Hold condition in stop mode
Decoupling capacitor	C_S	0.022	1	µF	*
Operating temperature	T_A	−40	+85	°C	Other than on-chip debug mode
		+5	+35		On-chip debug mode

*: Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The bypass capacitor for the V_{CC} pin must have a capacitance larger than C_S. For the connection to a decoupling capacitor C_S, see the diagram below. To prevent the device from unintentionally entering an unknown mode due to noise, minimize the distance between the C pin and C_S and the distance between C_S and the V_{SS} pin when designing the layout of a printed circuit board.

■ DBG / $\overline{\text{RST}}$ / C pins connection diagram



*: Connect the DBG pin to an external pull-up resistor of 2 kΩ or above. After power-on, ensure that the DBG pin does not stay at “L” level until the reset output is released. The DBG pin becomes a communication pin in debug mode. Since the actual pull-up resistance depends on the tool used and the interconnection length, refer to the tool document when selecting a pull-up resistor.

Warning:

- The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.
- Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.
- No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

17.3 DC Characteristics

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IHI}	P13, P46, P47	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	CMOS input level
	V_{IHS}	Other than P13, P46, P47, PF2	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
	V_{IHM}	PF2	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
"L" level input voltage	V_{ILI}	P13, P46, P47	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	CMOS input level
	V_{ILS}	Other than P13, P46, P47, PF2	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	Hysteresis input
	V_{ILM}	PF2	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	Hysteresis input
Open-drain output application voltage	V_D	P10, P46, P47, PF2	—	V_{SS} – 0.3	—	Vss + 5.5	V	
"H" level output voltage	V_{OH1}	Output pins other than P06, P07, P10, P40 to P45, PF2	I_{OH} = –4 mA	V_{CC} – 0.5	—	—	V	
	V_{OH2}	P06, P07, P40 to P45	I_{OH} = –8 mA	V_{CC} – 0.5	—	—	V	
"L" level output voltage	V_{OL1}	Output pins other than P06, P07, P40 to P45	I_{OL} = 4 mA	—	—	0.4	V	
	V_{OL2}	P06, P07, P40 to P45	I_{OL} = 12 mA	—	—	0.4	V	
Input leak current (Hi-Z output leak current)	I_{LI}	All input pins	0.0 V < V_I < V_{CC}	–5	—	+5	µA	When the internal pull-up resistor is disabled
Internal pull-up resistor	R_{PULL}	Other than P10, P46, P47, PF0, PF1, PF2	V_I = 0 V	25	50	100	kΩ	When the internal pull-up resistor is enabled
Input capacitance	C_{IN}	Other than V_{CC} and V_{SS}	f = 1 MHz	—	5	15	pF	

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*3	I_{CC}	V_{CC} (External clock operation)	F_{CH} = 32 MHz F_{MP} = 16 MHz Main clock mode (divided by 2)	—	4.7	5.8	mA	Except during Flash memory programming and erasing
				—	8.6	13.8	mA	During Flash memory programming and erasing
				—	6.1	9.1	mA	At A/D conversion
	I_{CCS}		F_{CH} = 32 MHz F_{MP} = 16 MHz Main sleep mode (divided by 2)	—	2.2	3	mA	
	I_{CCL}		F_{CL} = 32 kHz F_{MPL} = 16 kHz Subclock mode (divided by 2) T_A = +25 °C	—	63	145	µA	
	I_{CCLS}		F_{CL} = 32 kHz F_{MPL} = 16 kHz Subsleep mode (divided by 2) T_A = +25 °C	—	11	16	µA	In deep standby mode
	I_{CCT}		F_{CL} = 32 kHz Watch mode Main stop mode T_A = +25 °C	—	8	13	µA	In deep standby mode
	I_{CCMPLL}	V_{CC}	F_{MCRPLL} = 16 MHz F_{MP} = 16 MHz Main CR PLL clock mode (multiplied by 4) T_A = +25 °C	—	5.1	6.8	mA	
	I_{CCMCR}		F_{CRH} = 4 MHz F_{MP} = 4 MHz Main CR clock mode	—	1.4	4.6	mA	
	I_{CCSCR}		Sub-CR clock mode (divided by 2) T_A = +25 °C	—	58.1	230	µA	
	I_{CCTS}	V_{CC} (External clock operation)	F_{CH} = 32 MHz Time-base timer mode T_A = +25 °C	—	590	660	µA	In deep standby mode
	I_{CCH}		Substop mode T_A = +25 °C	—	8	13	µA	In deep standby mode

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*3	I_V	V_{CC}	Current consumption of the comparator	—	60	160	µA	
	I_{LVD}		Current consumption of the low-voltage detection reset circuit	—	4	7	µA	
	I_{CRH}		Current consumption of the main CR oscillator	—	240	320	µA	
	I_{CRL}		Current consumption of the sub-CR oscillator oscillating at 100 kHz	—	7	20	µA	
	I_{NSTBY}		Current consumption difference between normal standby mode and deep standby mode T_A = +25 °C	—	20	30	µA	
	I_{TSC}		Current consumption difference between standby mode with the TS in operation and standby mode with the TS not in operation	—	37	60	µA	

*1: V_{CC} = 5.0 V, T_A = +25 °C
*2: V_{CC} = 5.5 V, T_A = +85 °C (unless otherwise specified)
*3:
- The power supply current is determined by the external clock. When the low-voltage detection reset circuit is selected, the power supply current is the sum of adding the current consumption of the low-voltage detection reset circuit (I_{LVD}) to one of the values from I_{CC} to I_{CCH}. In addition, when both the low-voltage detection reset circuit and a CR oscillator are selected, the power supply current is the sum of adding up the current consumption of the low-voltage detection circuit, the current consumption of the CR oscillators (I_{CRH} or I_{CRL}) and one of the values from I_{CC} to I_{CCH}. In on-chip debug mode, the main CR oscillator (I_{CRH}) and the low-voltage detection resket circuit are always in operation, and current consumption therefore increases accordingly.
- See “4. AC Characteristics Clock Timing on page 141” for F_{CH}, F_{CL}, F_{CRH} and F_{MCRPLL}.
- See “4. AC Characteristics Source Clock/Machine Clock on page 145” for F_{MP} and F_{MPL}.
- The power supply current value in standby mode is measured in deep standby mode. The current consumption in normal standby is higher than that in deep standby mode. The power supply current value in normal standby can be found by adding the current consumption difference between normal standby mode and deep standby mode (I_{NSTBY}) to the power supply current value in deep standby mode. For details of normal standby and deep standby mode, refer to “CHAPTER 3 CLOCK CONTROLLER” in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

17.4 AC Characteristics

17.4.1 Clock Timing

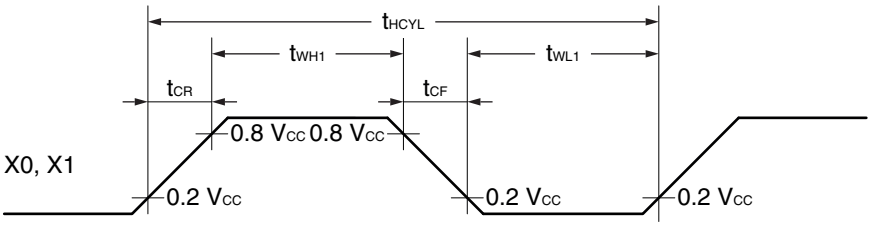
(V_{CC} = 2.4 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_{CH}	X0, X1	—	1	—	16.25	MHz	When the main oscillation circuit is used
		X0	X1: open	1	—	12	MHz	When the main external clock is used
		X0, X1	*	1	—	32.5	MHz	
	F_{CRH}	—	—	3.92	4	4.08	MHz	Operating conditions • The main CR clock is used. • 0 °C ≤ T_A ≤ +70 °C
				3.8	4	4.2	MHz	Operating conditions • The main CR clock is used. • – 40 °C ≤ T_A < 0 °C, + 70 °C < T_A ≤ + 85 °C
	F_{MCRPLL}	—	—	7.84	8	8.16	MHz	Operating conditions • PLL multiplication rate: 2 • 0 °C ≤ T_A ≤ +70 °C
				7.6	8	8.4	MHz	Operating conditions • PLL multiplication rate: 2 • – 40 °C ≤ T_A < 0 °C, + 70 °C < T_A ≤ + 85 °C
				9.8	10	10.2	MHz	Operating conditions • PLL multiplication rate: 2.5 • 0 °C ≤ T_A ≤ +70 °C
				9.5	10	10.5	MHz	Operating conditions • PLL multiplication rate: 2.5 • – 40 °C ≤ T_A < 0 °C, + 70 °C < T_A ≤ + 85 °C
				11.76	12	12.24	MHz	Operating conditions • PLL multiplication rate: 3 • 0 °C ≤ T_A ≤ +70 °C
				11.4	12	12.6	MHz	Operating conditions • PLL multiplication rate: 3 • – 40 °C ≤ T_A < 0 °C, + 70 °C < T_A ≤ + 85 °C
				15.68	16	16.32	MHz	Operating conditions • PLL multiplication rate: 4 • 0 °C ≤ T_A ≤ +70 °C
				15.2	16	16.8	MHz	Operating conditions • PLL multiplication rate: 4 • – 40 °C ≤ T_A < 0 °C, + 70 °C < T_A ≤ + 85 °C
	F_{CL}	X0A, X1A	—	—	32.768	—	kHz	When the sub-oscillation circuit is used
				—	32.768	—	kHz	When the sub-external clock is used
	F_{CRL}	—	—	50	100	150	kHz	When the sub-CR clock is used
Clock cycle time	t_{HCYL}	X0, X1	—	61.5	—	1000	ns	When the main oscillation circuit is used
		X0	X1: open	83.4	—	1000	ns	When an external clock is used
		X0, X1	*	30.8	—	1000	ns	
	t_{LCYL}	X0A, X1A	—	—	30.5	—	µs	When the subclock is used

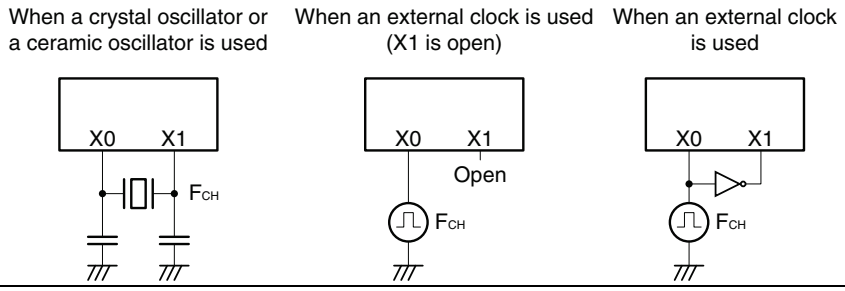
Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input clock pulse width	t_{WH1}, t_{WL1}	X0	X1: open	33.4	—	—	ns	When an external clock is used, the duty ratio should range between 40% and 60%.
		X0, X1	*	12.4	—	—	ns	
	t_{WH2}, t_{WL2}	X0A	—	—	15.2	—	µs	
Input clock rising time and falling time	t_{CR}, t_{CF}	X0	X1: open	—	—	5	ns	When an external clock is used
		X0, X1	*	—	—	5	ns	
CR oscillation start time	t_{CRHWK}	—	—	—	—	50	µs	When the main CR clock is used
	t_{CRLWK}	—	—	—	—	30	µs	When the sub-CR clock is used
PLL oscillation start time	$t_{MCRPLLWK}$	—	—	—	—	100	µs	When the main CR PLL clock is used

*: The external clock signal is input to X0 and the inverted external clock signal to X1.

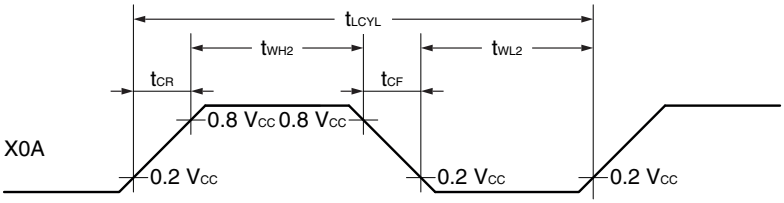
■ Input waveform generated when an external clock (main clock) is used



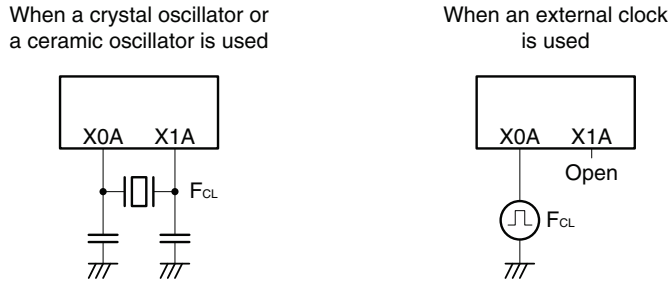
■ Figure of main clock input port external connection



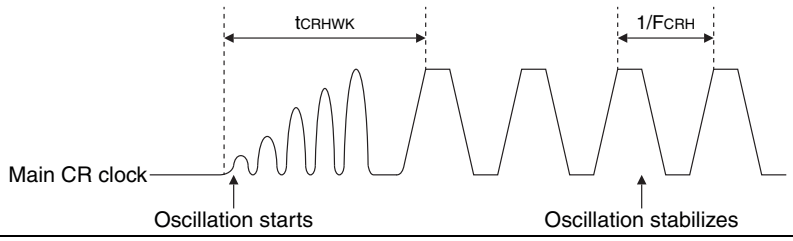
■ Input waveform generated when an external clock (subclock) is used



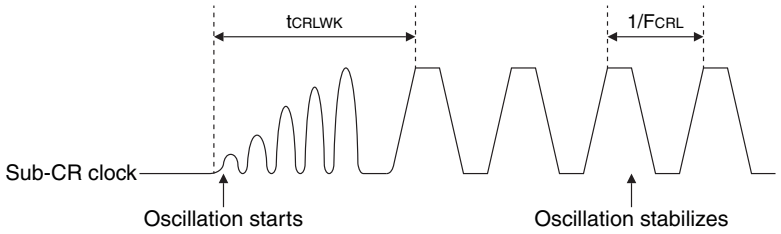
■ Figure of subclock input port external connection



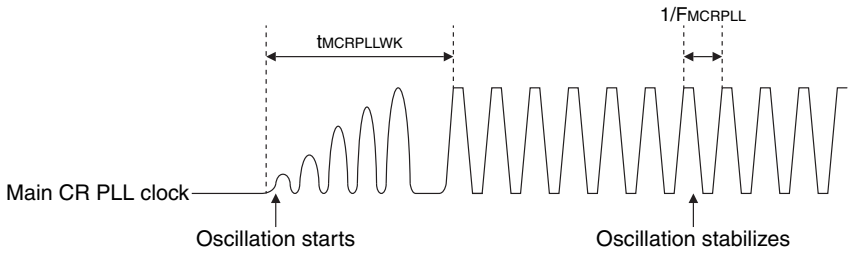
■ Input waveform generated when an internal clock (main CR clock) is used



■ Input waveform generated when an internal clock (sub-CR clock) is used



■ Input waveform generated when an internal clock (main CR PLL clock) is used



17.4.2 Source Clock/Machine Clock

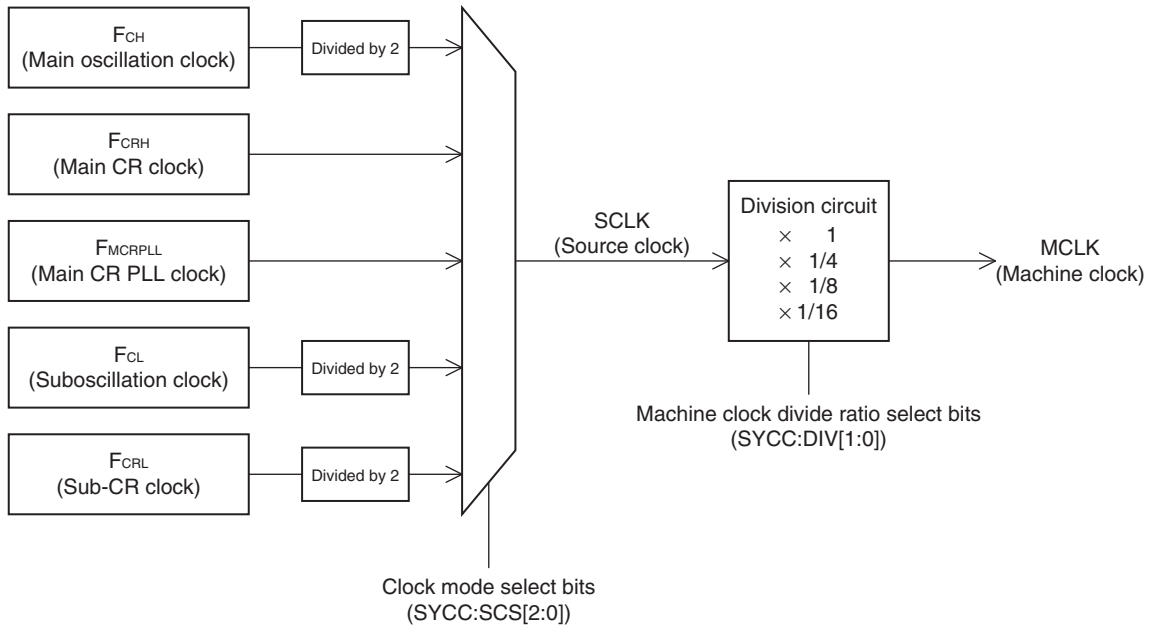
(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Source clock cycle time*1	t_{SCLK}	—	61.5	—	2000	ns	When the main external clock is used Min: F_{CH} = 32.5 MHz, divided by 2 Max: F_{CH} = 1 MHz, divided by 2
			62.5	—	1000	ns	When the main CR clock is used Min: F_{CRH} = 4 MHz, multiplied by 4 Max: F_{CRH} = 4 MHz, divided by 4
			—	61	—	µs	When the sub-oscillation clock is used F_{CL} = 32.768 kHz, divided by 2
			—	20	—	µs	When the sub-CR clock is used F_{CRL} = 100 kHz, divided by 2
Source clock frequency	F_{SP}	—	0.5	—	16.25	MHz	When the main oscillation clock is used
			—	4	12.5	MHz	When the main CR clock is used
	F_{SPL}		—	16.384	—	kHz	When the sub-oscillation clock is used
			—	50	—	kHz	When the sub-CR clock is used F_{CRL} = 100 kHz, divided by 2
Machine clock cycle time*2 (minimum instruction execution time)	t_{MCLK}	—	61.5	—	32000	ns	When the main oscillation clock is used Min: F_{SP} = 16.25 MHz, no division Max: F_{SP} = 0.5 MHz, divided by 16
			250	—	4000	ns	When the main CR clock is used Min: F_{SP} = 4 MHz, no division Max: F_{SP} = 4 MHz, divided by 16
			61	—	976.5	µs	When the sub-oscillation clock is used Min: F_{SPL} = 16.384 kHz, no division Max: F_{SPL} = 16.384 kHz, divided by 16
			20	—	320	µs	When the sub-CR clock is used Min: F_{SPL} = 50 kHz, no division Max: F_{SPL} = 50 kHz, divided by 16
Machine clock frequency	F_{MP}	—	0.031	—	16.25	MHz	When the main oscillation clock is used
			0.25	—	16	MHz	When the main CR clock is used
	F_{MPL}		1.024	—	16.384	kHz	When the sub-oscillation clock is used
			3.125	—	50	kHz	When the sub-CR clock is used F_{CRL} = 100 kHz

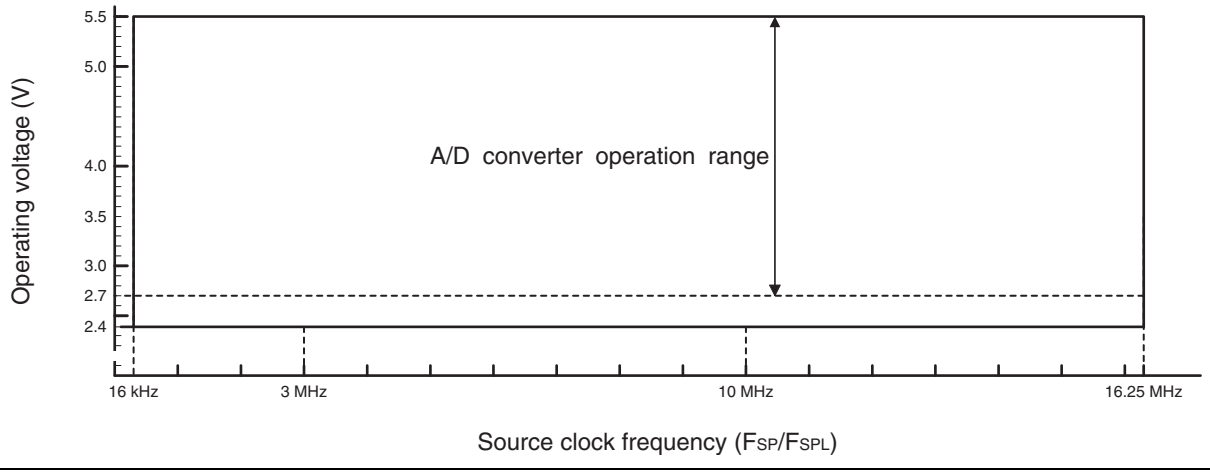
*1: This is the clock before it is divided according to the division ratio set by the machine clock division ratio select bits (SYCC:DIV[1:0]). This source clock is divided to become a machine clock according to the division ratio set by the machine clock division ratio select bits (SYCC:DIV[1:0]). In addition, a source clock can be selected from the following.
- Main clock divided by 2
- Main CR clock
- PLL multiplication of main CR clock (Select a multiplication rate from 2, 2.5, 3 and 4.)
- Subclock divided by 2
- Sub-CR clock divided by 2

*2: This is the operating clock of the microcontroller. A machine clock can be selected from the following.
- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

■ Schematic diagram of the clock generation block



■ Operating voltage - Operating frequency (T_A = –40°C to +85°C)

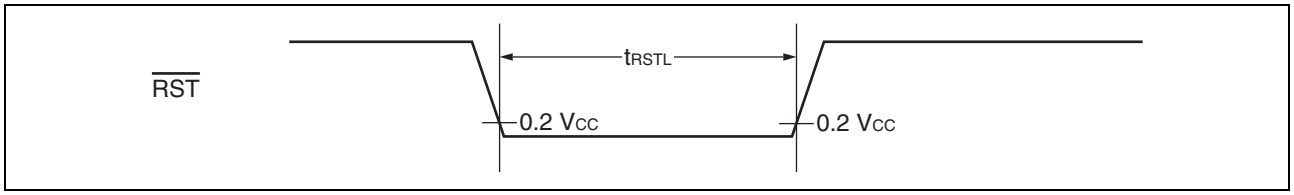


17.4.3 External Reset

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
$\overline{RST}$ "L" level pulse width	t_{RSTL}	2 t_{MCLK}*	—	ns	

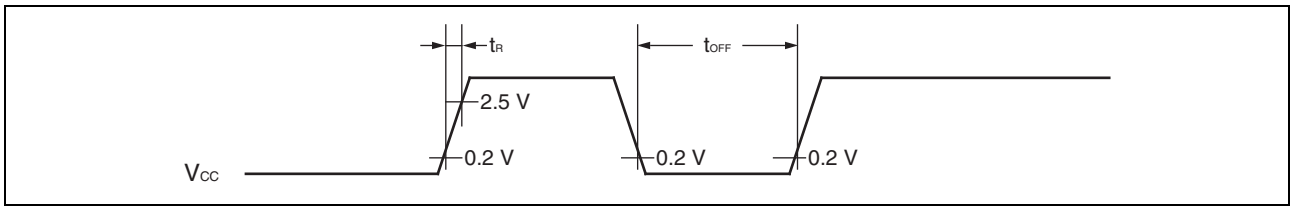
*: See "Source Clock/Machine Clock" for t_{MCLK}.



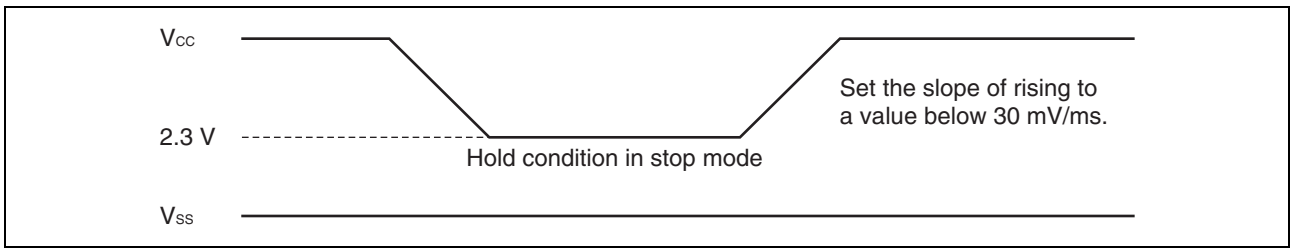
17.4.4 Power-on Reset

(V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_R	—	—	50	ms	
Power supply cutoff time	t_{OFF}	—	1	—	ms	Wait time until power-on



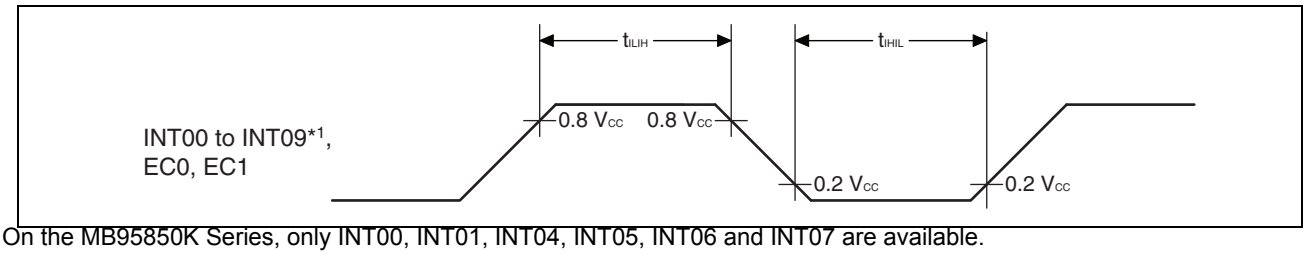
Note: A sudden change of power supply voltage may activate the power-on reset function. When changing the power supply voltage during the operation, set the slope of rising to a value below within 30 mV/ms as shown below.



17.4.5 Peripheral Input Timing

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Peripheral input “H” pulse width	t_{ILIH}	INT00 to INT09*1, EC0, EC1	2 t_{MCLK}*2	—	ns
Peripheral input “L” pulse width	t_{IHIL}		2 t_{MCLK}*2	—	ns



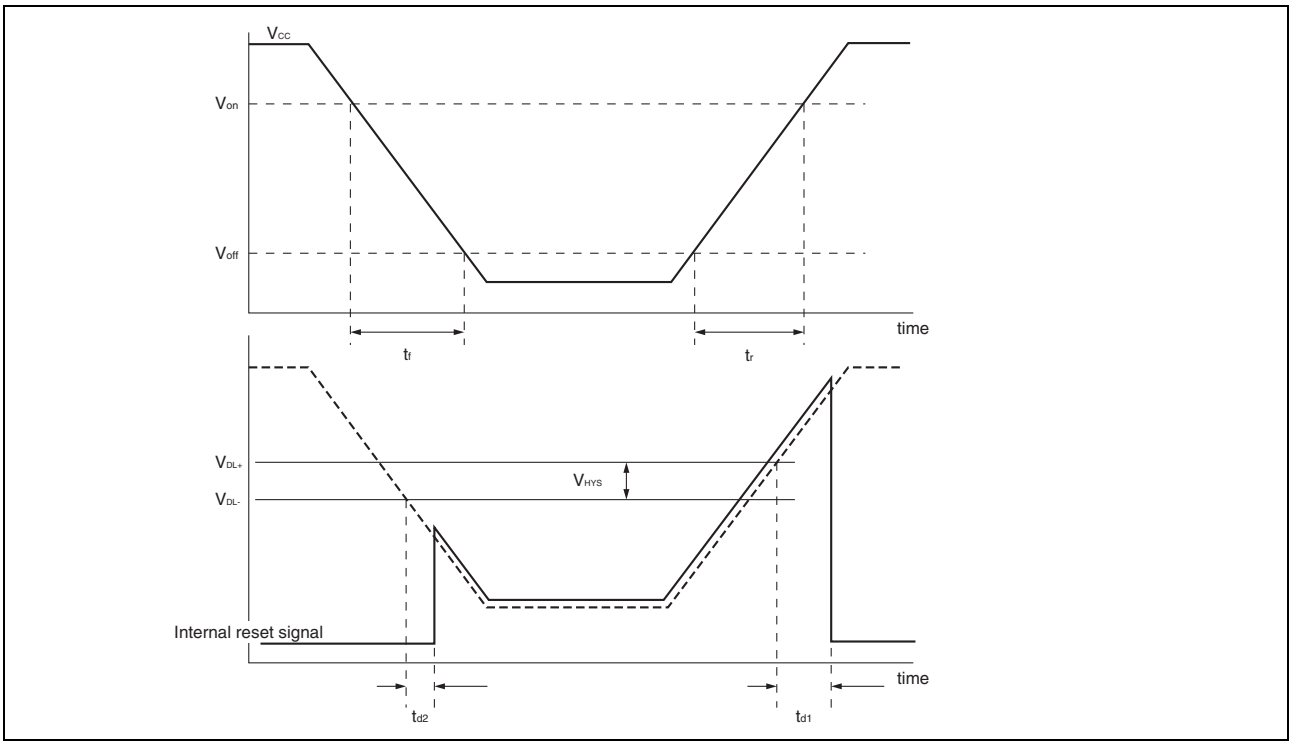
*1: On the MB95850K Series, only INT00, INT01, INT04, INT05, INT06 and INT07 are available.
On the MB95860K Series, only INT00 to INT07 are available.
On the MB95870K Series, INT00 to INT09 are available.
*2: See “Source Clock/Machine Clock” for t_{MCLK}.

17.4.6 Low-voltage Detection

(V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Release voltage*	V_{DL+}	2.52	2.7	2.88	V	At power supply rise
		2.61	2.8	2.99	V	
		2.89	3.1	3.31	V	
		3.08	3.3	3.52	V	
Detection voltage*	V_{DL-}	2.43	2.6	2.77	V	At power supply fall
		2.52	2.7	2.88	V	
		2.80	3	3.20	V	
		2.99	3.2	3.41	V	
Hysteresis width	V_{HYS}	—	—	100	mV	
Power supply start voltage	V_{off}	—	—	2.3	V	
Power supply end voltage	V_{on}	4.9	—	—	V	
Power supply voltage change time (at power supply rise)	t_r	650	—	—	µs	Slope of power supply that the reset release signal generates within the rating (V_{DL+})
Power supply voltage change time (at power supply fall)	t_f	650	—	—	µs	Slope of power supply that the reset detection signal generates within the rating (V_{DL-})
Reset release delay time	t_{d1}	—	—	30	µs	
Reset detection delay time	t_{d2}	—	—	30	µs	
LVD reset threshold voltage transition stabilization time	t_{stb}	10	—	—	µs	

*: After the LVD reset is enabled by the LVD reset circuit control register (LVDCC), the release voltage and the detection voltage can be selected by using the LVD reset voltage selection ID register (LVDR) in the low-voltage detection reset circuit. For details of the LVDCC register and the LVDR register, refer to “CHAPTER 16 LOW-VOLTAGE DETECTION RESET CIRCUIT” in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

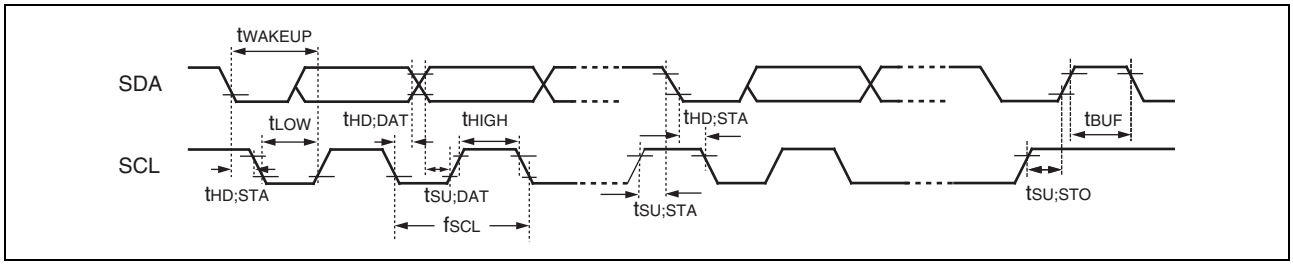

V_{CC}
V_{on}
V_{off}
time
t_f
t_r
V_{DL+}
V_{DL-}
V_{HYS}
Internal reset signal
time
t_{d2}
t_{d1}

17.4.7 I^2C Bus Interface Timing

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value				Unit
				Standard-mode		Fast-mode		
				Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	SCL	R = 1.7 kΩ, C = 50 pF*1	0	100	0	400	kHz
(Repeated) START condition hold time SDA ↓ → SCL ↓	$t_{HD;STA}$	SCL, SDA		4.0	—	0.6	—	µs
SCL clock “L” width	t_{LOW}	SCL		4.7	—	1.3	—	µs
SCL clock “H” width	t_{HIGH}	SCL		4.0	—	0.6	—	µs
(Repeated) START condition setup time SCL ↑ → SDA ↓	$t_{SU;STA}$	SCL, SDA		4.7	—	0.6	—	µs
Data hold time SCL ↓ → SDA ↓↑	$t_{HD;DAT}$	SCL, SDA		0	3.45*2	0	0.9*3	µs
Data setup time SDA ↓↑ → SCL ↑	$t_{SU;DAT}$	SCL, SDA		0.25	—	0.1	—	µs
STOP condition setup time SCL ↑ → SDA ↑	$t_{SU;STO}$	SCL, SDA		4	—	0.6	—	µs
Bus free time between STOP condition and START condition	t_{BUF}	SCL, SDA		4.7	—	1.3	—	µs

*1: R represents the pull-up resistor of the SCL and SDA lines, and C the load capacitor of the SCL and SDA lines.
*2: The maximum $t_{HD;DAT}$ in the Standard-mode is applicable only when the time during which the device is holding the SCL signal at “L” (t_{LOW}) does not extend.
*3: A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system, provided that the condition of $t_{SU;DAT} \geq 250$ ns is fulfilled.



(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value*2		Unit	Remarks
				Min	Max		
SCL clock “L” width	t_{LOW}	SCL	R = 1.7 kΩ, C = 50 pF*1	$(2 + nm/2)t_{MCLK} - 20$	—	ns	Master mode
SCL clock “H” width	t_{HIGH}	SCL		$(nm/2)t_{MCLK} - 20$	$(nm/2)t_{MCLK} + 20$	ns	Master mode
START condition hold time	$t_{HD;STA}$	SCL, SDA		$(-1 + nm/2)t_{MCLK} - 20$	$(-1 + nm)t_{MCLK} + 20$	ns	Master mode Maximum value is applied when m, n = 1, 8. Otherwise, the minimum value is applied.
STOP condition setup time	$t_{SU;STO}$	SCL, SDA		$(1 + nm/2)t_{MCLK} - 20$	$(1 + nm/2)t_{MCLK} + 20$	ns	Master mode
START condition setup time	$t_{SU;STA}$	SCL, SDA		$(1 + nm/2)t_{MCLK} - 20$	$(1 + nm/2)t_{MCLK} + 20$	ns	Master mode
Bus free time between STOP condition and START condition	t_{BUF}	SCL, SDA		$(2\ nm + 4)\ t_{MCLK} - 20$	—	ns	
Data hold time	$t_{HD;DAT}$	SCL, SDA		$3\ t_{MCLK} - 20$	—	ns	Master mode
Data setup time	$t_{SU;DAT}$	SCL, SDA		$(-2 + nm/2)\ t_{MCLK} - 20$	$(-1 + nm/2)\ t_{MCLK} + 20$	ns	Master mode It is assumed that “L” of SCL is not extended. The minimum value is applied to the first bit of continuous data. Otherwise, the maximum value is applied.
Setup time between clearing interrupt and SCL rising	$t_{SU;INT}$	SCL		$(nm/2)\ t_{MCLK} - 20$	$(1 + nm/2)\ t_{MCLK} + 20$	ns	The minimum value is applied to the interrupt at the ninth SCL↓. The maximum value is applied to the interrupt at the eighth SCL↓.
SCL clock “L” width	t_{LOW}	SCL		$4\ t_{MCLK} - 20$	—	ns	At reception
SCL clock “H” width	t_{HIGH}	SCL		$4\ t_{MCLK} - 20$	—	ns	At reception

Parameter	Symbol	Pin name	Condition	Value*2		Unit	Remarks
				Min	Max		
START condition detection	$t_{HD;STA}$	SCL, SDA	R = 1.7 kΩ, C = 50 pF*1	2 t_{MCLK} − 20	—	ns	No START condition is detected when 1 t_{MCLK} is used at reception.
STOP condition detection	$t_{SU;STO}$	SCL, SDA		2 t_{MCLK} − 20	—	ns	No STOP condition is detected when 1 t_{MCLK} is used at reception.
RESTART condition detection condition	$t_{SU;STA}$	SCL, SDA		2 t_{MCLK} − 20	—	ns	No RESTART condition is detected when 1 t_{MCLK} is used at reception.
Bus free time	t_{BUF}	SCL, SDA		2 t_{MCLK} − 20	—	ns	At reception
Data hold time	$t_{HD;DAT}$	SCL, SDA		2 t_{MCLK} − 20	—	ns	At slave transmission mode
Data setup time	$t_{SU;DAT}$	SCL, SDA		t_{LOW} − 3 t_{MCLK} − 20	—	ns	At slave transmission mode
Data hold time	$t_{HD;DAT}$	SCL, SDA		0	—	ns	At reception
Data setup time	$t_{SU;DAT}$	SCL, SDA		t_{MCLK} − 20	—	ns	At reception
SDA↓ → SCL↑ (with wakeup function in use)	t_{WAKEUP}	SCL, SDA		Oscillation stabilization wait time +2 t_{MCLK} − 20	—	ns	

*1: R represents the pull-up resistor of the SCL and SDA lines, and C the load capacitor of the SCL and SDA lines.

*2: • See "Source Clock/Machine Clock" for t_{MCLK}.

- m represents the CS[4:3] bits in the I^2C clock control register (ICCR0).
- n represents the CS[2:0] bits in the I^2C clock control register (ICCR0).
- The actual timing of the I^2C bus interface is determined by the values of m and n set by the machine clock (t_{MCLK}) and the CS[4:0] bits in the ICCR0 register.
- Standard-mode:
  m and n can be set to values in the following range: 0.9 MHz < t_{MCLK} (machine clock) < 16.25 MHz.
  The usable frequencies of the machine clock are determined by the settings of m and n as shown below.
  (m, n) = (1, 8) : 0.9 MHz < t_{MCLK} ≤ 1 MHz
  (m, n) = (1, 22), (5, 4), (6, 4), (7, 4), (8, 4) : 0.9 MHz < t_{MCLK} ≤ 2 MHz
  (m, n) = (1, 38), (5, 8), (6, 8), (7, 8), (8, 8) : 0.9 MHz < t_{MCLK} ≤ 4 MHz
  (m, n) = (1, 98), (5, 22), (6, 22), (7, 22) : 0.9 MHz < t_{MCLK} ≤ 10 MHz
  (m, n) = (8, 22) : 0.9 MHz < t_{MCLK} ≤ 16.25 MHz
- Fast-mode:
  m and n can be set to values in the following range: 3.3 MHz < t_{MCLK} (machine clock) < 16.25 MHz.
  The usable frequencies of the machine clock are determined by the settings of m and n as shown below.
  (m, n) = (1, 8) : 3.3 MHz < t_{MCLK} ≤ 4 MHz
  (m, n) = (1, 22), (5, 4) : 3.3 MHz < t_{MCLK} ≤ 8 MHz
  (m, n) = (1, 38), (6, 4), (7, 4), (8, 4) : 3.3 MHz < t_{MCLK} ≤ 10 MHz
  (m, n) = (5, 8) : 3.3 MHz < t_{MCLK} ≤ 16.25 MHz

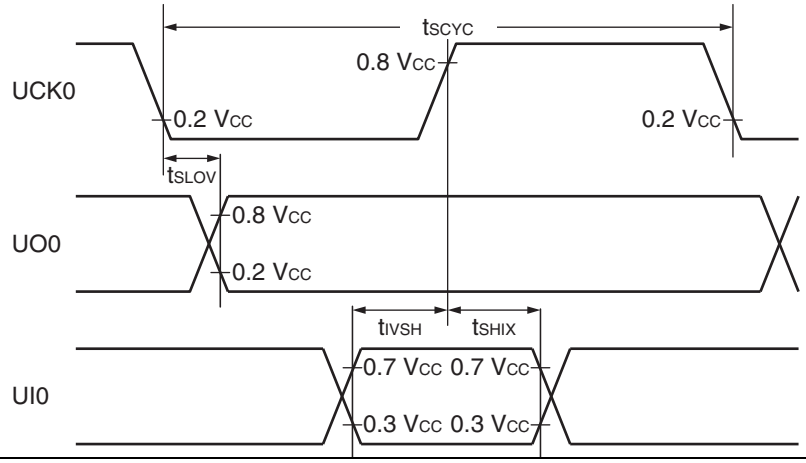
17.4.8 UART/SIO, Serial I/O Timing

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

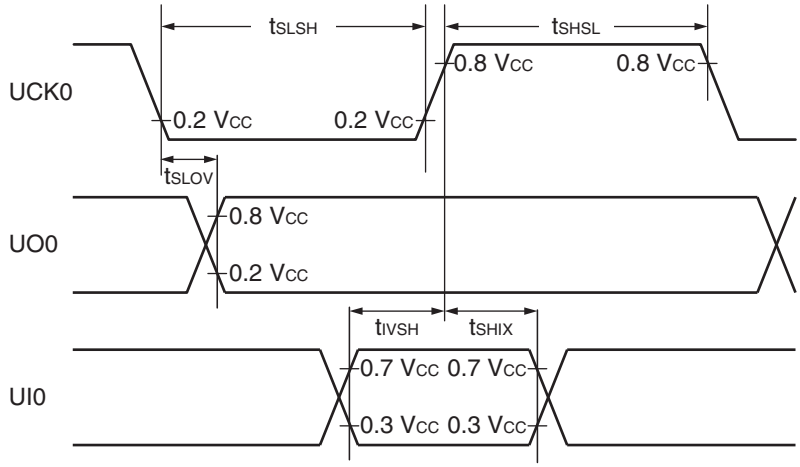
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	UCK0	Internal clock operation	4 t_{MCLK}*	—	ns
UCK ↓ → UO time	t_{SLOV}	UCK0, UO0		–190	+190	ns
Valid UI → UCK ↑	t_{IVSH}	UCK0, UI0		2 t_{MCLK}*	—	ns
UCK ↑ → valid UI hold time	t_{SHIX}	UCK0, UI0		2 t_{MCLK}*	—	ns
Serial clock “H” pulse width	t_{SHSL}	UCK0	External clock operation	4 t_{MCLK}*	—	ns
Serial clock “L” pulse width	t_{SLSH}	UCK0		4 t_{MCLK}*	—	ns
UCK ↓ → UO time	t_{SLOV}	UCK0, UO0		—	190	ns
Valid UI → UCK ↑	t_{IVSH}	UCK0, UI0		2 t_{MCLK}*	—	ns
UCK ↑ → valid UI hold time	t_{SHIX}	UCK0, UI0		2 t_{MCLK}*	—	ns

*: See “Source Clock/Machine Clock” for t_{MCLK}.

■ Internal shift clock mode



■ External shift clock mode



17.4.9 Comparator Timing

(V_{CC} = 2.4 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Pin name	Value			Unit	Remarks
		Min	Typ	Max		
Voltage range	CMP0_P, CMP0_N	0	—	V_{CC} – 1.3	V	
Offset voltage	CMP0_P, CMP0_N	–15	—	+15	mV	
Delay time	CMP0_O	—	650	1200	ns	Overdrive 5 mV
		—	140	420	ns	Overdrive 50 mV
Power down delay	CMP0_O	—	—	1200	ns	Power down recovery PD: 1 → 0
Power up stabilization wait time	CMP0_O	—	—	1200	ns	Output stabilization time at power up

17.4.10 BGR for Comparator

(V_{CC} = 2.4 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power up stabilization wait time	—	—	—	150	µs	Load: 10 pF
Output voltage	VBGR	1.1495	1.21	1.2705	V	

17.4.11 TS

(V_{CC} = 2.4 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Touch sensitivity	Stch	0.068	0.149	—	pF	The sensitivity of touch ch. n bits in a TS sensitivity select register x (RSELx:SnB[2:0])*1 have been set to “0b000”.
		0.054	0.086	—	pF	The sensitivity of touch ch. n bits in a TS sensitivity select register x (RSELx:SnB[2:0])*1 have been set to “0b001”.
		0.040	0.063	—	pF	The sensitivity of touch ch. n bits in a TS sensitivity select register x (RSELx:SnB[2:0])*1 have been set to “0b010”.
		0.032	0.047	—	pF	The sensitivity of touch ch. n bits in a TS sensitivity select register x (RSELx:SnB[2:0])*1 have been set to “0b011”.
		0.025	0.040	—	pF	The sensitivity of touch ch. n bits in a TS sensitivity select register x (RSELx:SnB[2:0])*1 have been set to “0b100”.
		0.022	0.033	—	pF	The sensitivity of touch ch. n bits in a TS sensitivity select register x (RSELx:SnB[2:0])*1 have been set to “0b101”.
		0.019	0.030	—	pF	The sensitivity of touch ch. n bits in a TS sensitivity select register x (RSELx:SnB[2:0])*1 have been set to “0b110”.
		0.017	0.027	—	pF	The sensitivity of touch ch. n bits in a TS sensitivity select register x (RSELx:SnB[2:0])*1 have been set to “0b111”.
Tuning capacitor in AREF and sensor pad	C_{si}	0	—	15	pF	
Sensor clock*2 (sensing phase)	F_{SNCLKS}	5	—	20	kHz	Frequency of the sensor clock in the sensing phase

*1: “n” represents the touch channel number and “x” a number from one to six. For details of the RSELx register, refer to “CHAPTER 26 TOUCH SENSOR” in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

*2: For details of the sensor clock, refer to “CHAPTER 26 TOUCH SENSOR” in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

17.5 A/D Converter

17.5.1 A/D Converter Electrical Characteristics

(V_{CC} = 2.7 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

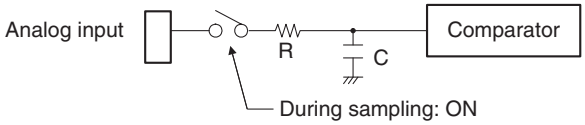
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	
Total error		–3	—	+3	LSB	
Linearity error		–2.5	—	+2.5	LSB	
Differential linearity error		–1.9	—	+1.9	LSB	
Zero transition voltage	V_{0T}	V_{SS} – 7.2 LSB	V_{SS} + 0.5 LSB	V_{SS} + 8.2 LSB	V	
Full-scale transition voltage	V_{FST}	V_{CC} – 6.2 LSB	V_{CC} – 1.5 LSB	V_{CC} + 9.2 LSB	V	
Compare time	—	3	—	10	µs	2.7 V ≤ V_{CC} ≤ 5.5 V
Sampling time	—	0.941	—	¥	µs	2.7 V ≤ V_{CC} ≤ 5.5 V, with external impedance < 3.3 kΩ and external capacitance = 10 pF
Analog input current	I_{AIN}	–0.3	—	+0.3	µA	
Analog input voltage	V_{AIN}	V_{SS}	—	V_{CC}	V	

17.5.2 Notes on Using A/D Converter

■ External impedance of analog input and its sampling time

The A/D converter of the MB95850K/860K/870K Series has a sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the capacitor of the internal sample and hold circuit is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, considering the relationship between the external impedance and minimum sampling time, either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. In addition, if sufficient sampling time cannot be secured, connect a capacitor of about 0.1 µF to the analog input pin.

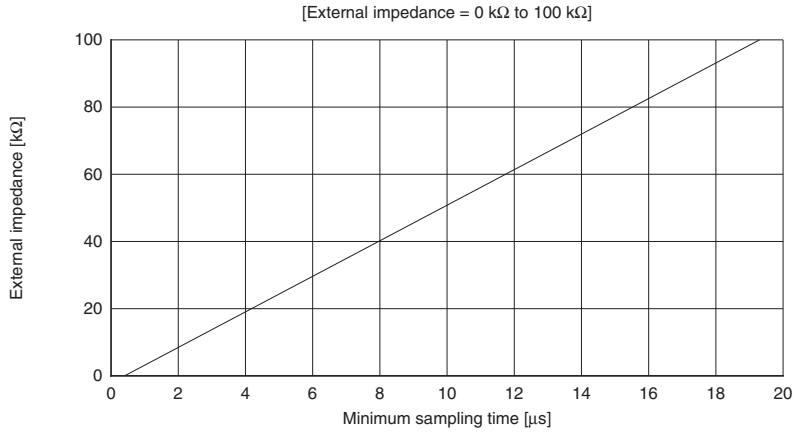
■ Analog input equivalent circuit

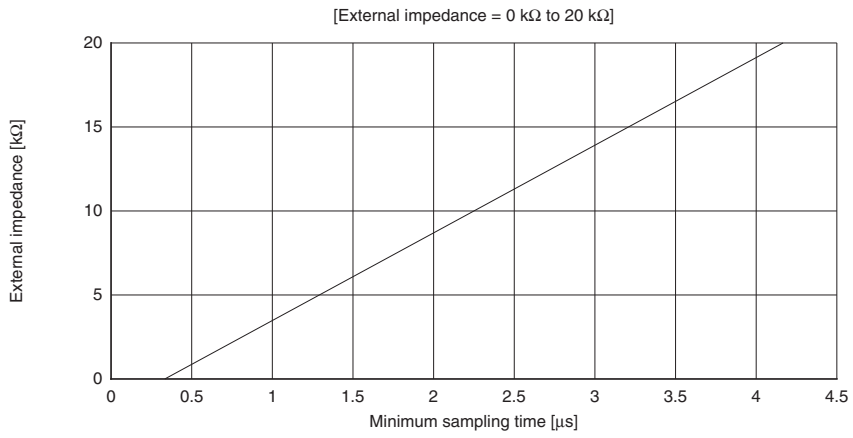


V_{CC}	R	C
4.5 V ≤ V_{CC} ≤ 5.5 V	1.45 kΩ (Max)	14.89 pF (Max)
2.7 V ≤ V_{CC} < 4.5 V	2.7 kΩ (Max)	14.89 pF (Max)

Note: The values are reference values.

■ Relationship between external impedance and minimum sampling time





Note: External capacitance = 10 pF

■ A/D conversion error

As $|V_{CC} - V_{SS}|$ decreases, the A/D conversion error increases proportionately.

17.5.3 Definitions of A/D Converter Terms

■ Resolution

It indicates the level of analog variation that can be distinguished by the A/D converter.

When the number of bits is 10, analog voltage can be divided into 2^{10} = 1024.

■ Linearity error (unit: LSB)

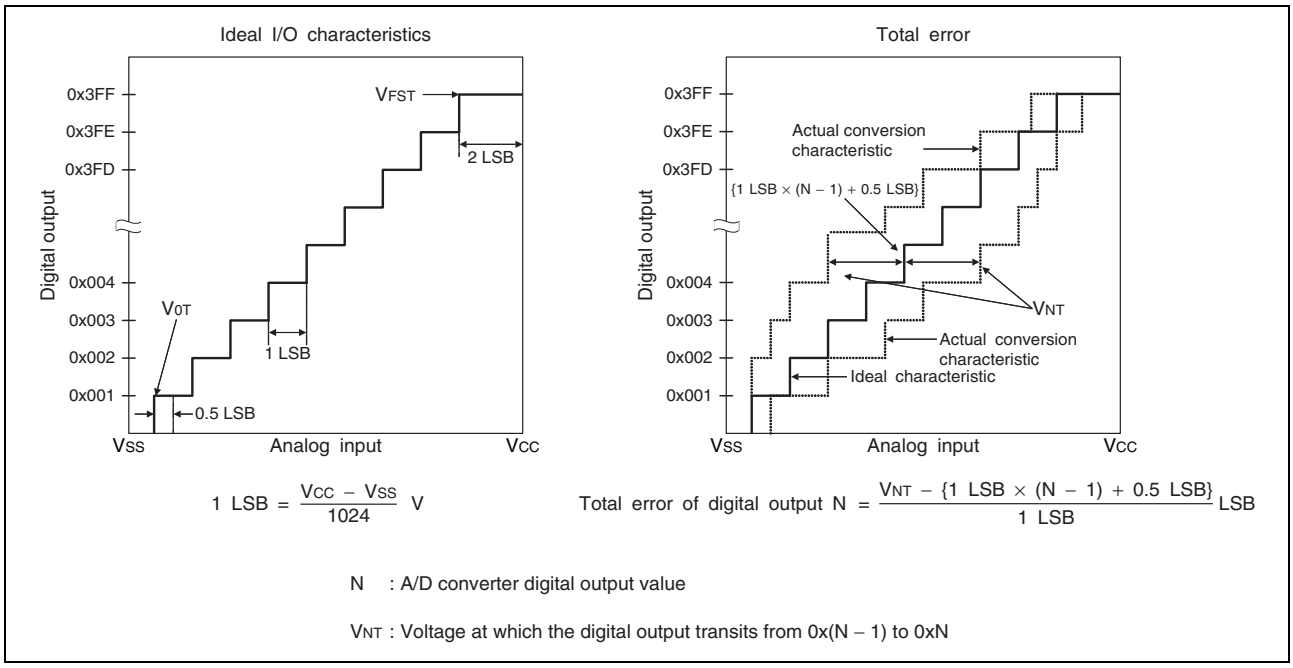
It indicates how much an actual conversion value deviates from the straight line connecting the zero transition point (“0000000000” ← → “0000000001”) of a device to the full-scale transition point (“1111111111” ← → “1111111110”) of the same device.

■ Differential linear error (unit: LSB)

It indicates how much the input voltage required to change the output code by 1 LSB deviates from an ideal value.

■ Total error (unit: LSB)

It indicates the difference between an actual value and a theoretical value. The error can be caused by a zero transition error, a full-scale transition errors, a linearity error, a quantum error, or noise.



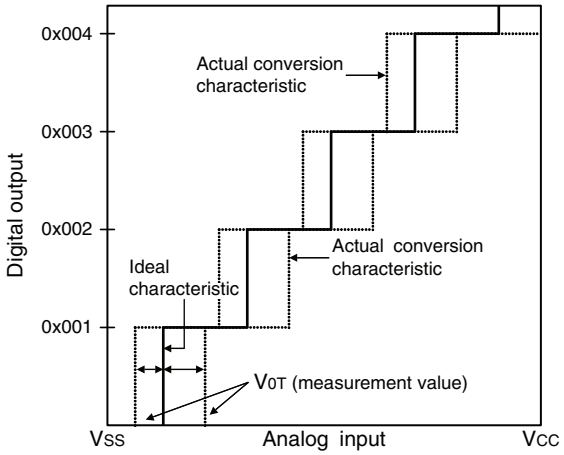
$$1\ \text{LSB} = \frac{V_{CC} - V_{SS}}{1024}\ \text{V}$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ \text{LSB}$$

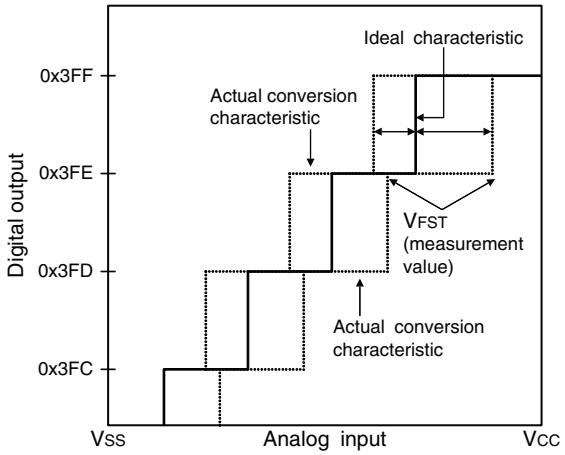
N : A/D converter digital output value

V_{NT} : Voltage at which the digital output transits from 0x(N – 1) to 0xN

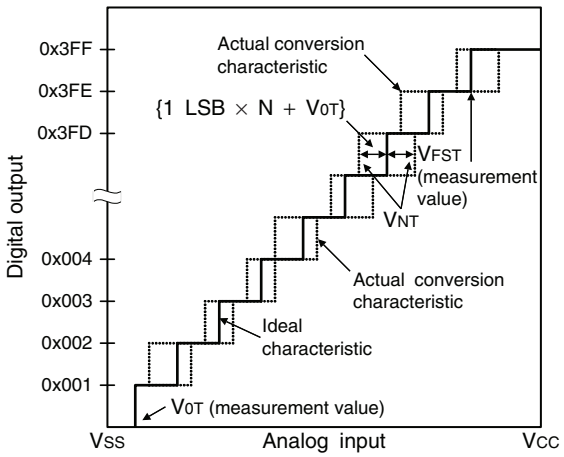
Zero transition error



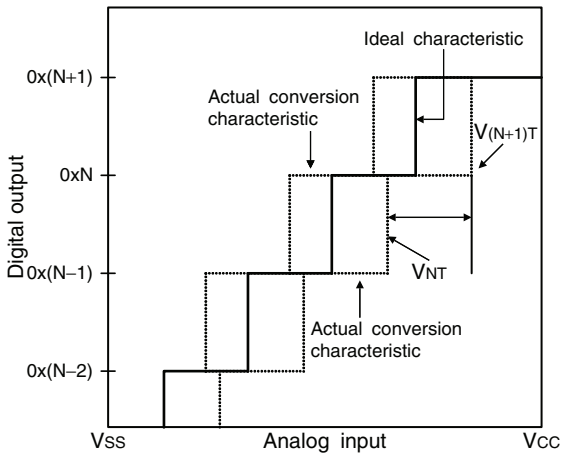
Full-scale transition error



Linearity error



Differential linearity error



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times N + V_{OT}\}}{1\ \text{LSB}}$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

N : A/D converter digital output value

V_{NT} : Voltage at which the digital output transits from 0x(N – 1) to 0xN

V_{OT} (ideal value) = V_{SS} + 0.5 LSB [V]

V_{FST} (ideal value) = V_{CC} – 2 LSB [V]

17.6 Flash Memory Program/Erase Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time (2 Kbyte sector)	—	0.3*1	1.6*2	s	The time of writing “0x00” prior to erasure is excluded.
Sector erase time (32 Kbyte sector)	—	0.6*1	3.1*2	s	The time of writing “0x00” prior to erasure is excluded.
Byte writing time	—	17	272	µs	System-level overhead is excluded.
Program/erase cycle	100000	—	—	cycle	
Power supply voltage at program/erase	2.4	—	5.5	V	
Flash memory data retention time	20*3	—	—	year	Average T_A = +85 °C Number of program/erase cycles: 1000 or below
	10*3	—	—		Average T_A = +85 °C Number of program/erase cycles: 1001 to 10000 inclusive
	5*3	—	—		Average T_A = +85 °C Number of program/erase cycles: 10001 or above

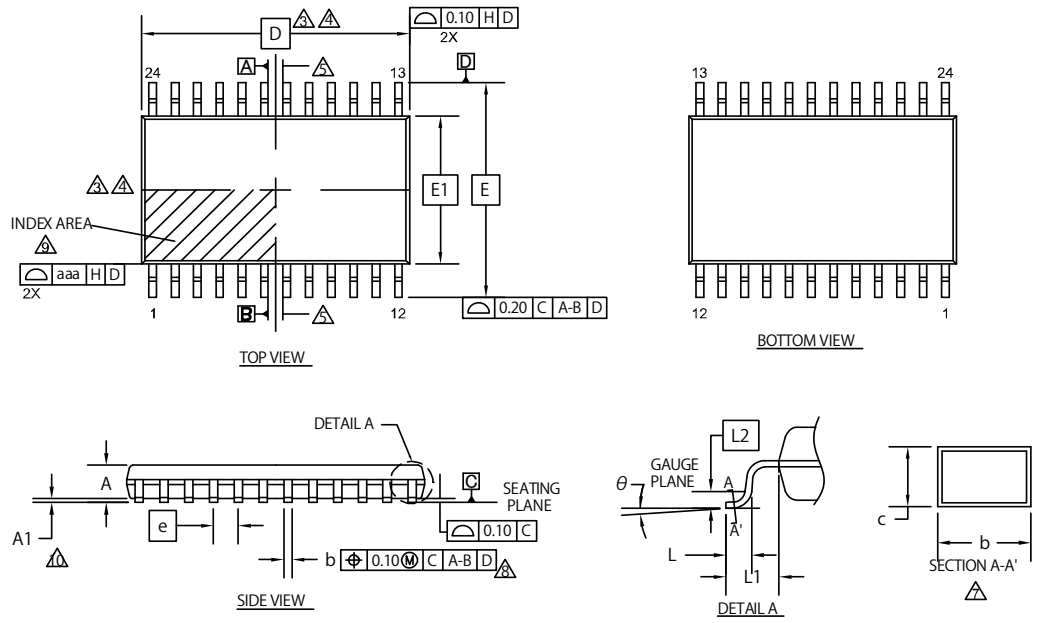
*1: V_{CC} = 5.5 V, T_A = +25 °C, 0 cycle
*2: V_{CC} = 2.4 V, T_A = +85 °C, 100000 cycles
*3: These values were converted from the result of a technology reliability assessment. (These values were converted from the result of a high temperature accelerated test using the Arrhenius equation with the average temperature being +85 °C.)

18. Ordering Information

Part number	Package
MB95F856KPFT-G-SNE2	24-pin plastic TSSOP (STI024)
MB95F856KPF-G-SNE2	24-pin plastic SOP (SOL024)
MB95F866KPMC-G-SNE2	32-pin plastic LQFP (LQB032)
MB95F876KPMC-G-SNE2	48-pin plastic LQFP (LQA048)
MB95F876KPMC1-G-SNE2	52-pin plastic LQFP (LQC052)

19. Package Dimension

Package Type	Package Code
TSSOP 24	STI024



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	——	——	1.20
A1	0.05	——	0.15
D	7.80 BSC		
E	6.40 BSC		
E1	4.40 BSC		
θ	0°	——	8°
c	0.10	——	0.19
b	0.20	0.22	0.29
L	0.45	0.60	0.75
L 1	1.00 REF		
L 2	0.25 BSC		
e	0.65 BSC		

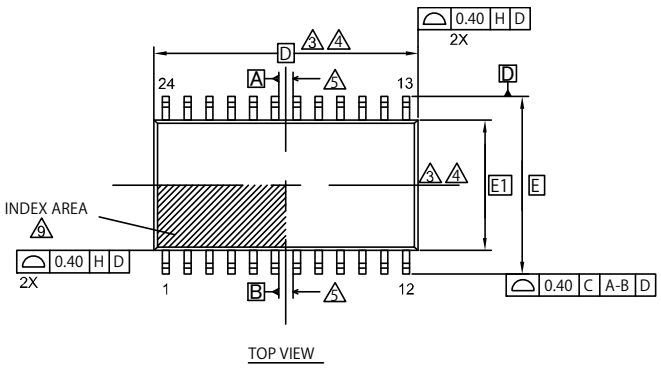
NOTES

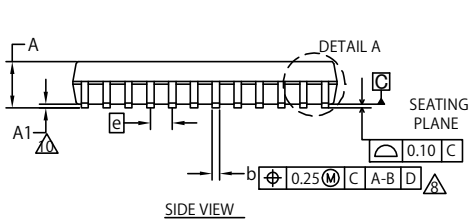
1. ALL DIMENSIONS ARE IN MILLIMETER.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DIMENSIONING D INCLUDE MOLD FLASH, DIMENSIONING E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.025 mm PER SIDE. D and E1 DIMENSION ARE DETERMINED AT DATUM H
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONING D and E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, THE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A & B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSION APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm TO 0.25mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE THE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR MAY NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. LF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED
10. "A1" IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY EXCLUDING THE LID AND OR THERMAL ENHANCEMENT ON CAVITY DOWN PACKAGE CONFIGURATIONS.

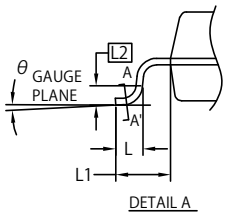
002-14046 **

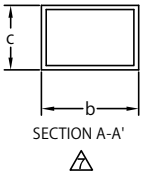
PACKAGE OUTLINE, 24 LEAD TSSOP
4.4X7.8X1.2 MM STI024 REV**

Package Type	Package Code
SOP 24	SOL024









SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	——	——	2.80
A1	0.05	——	0.30
D	15.34 BSC		
E	10.20 BSC		
E1	7.50 BSC		
θ	0°	——	8°
c	0.20	——	0.34
b	0.35	0.42	0.49
L	0.40	0.60	0.80
L 1	1.35 REF		
L 2	0.25 BSC		
e	1.27 BSC		

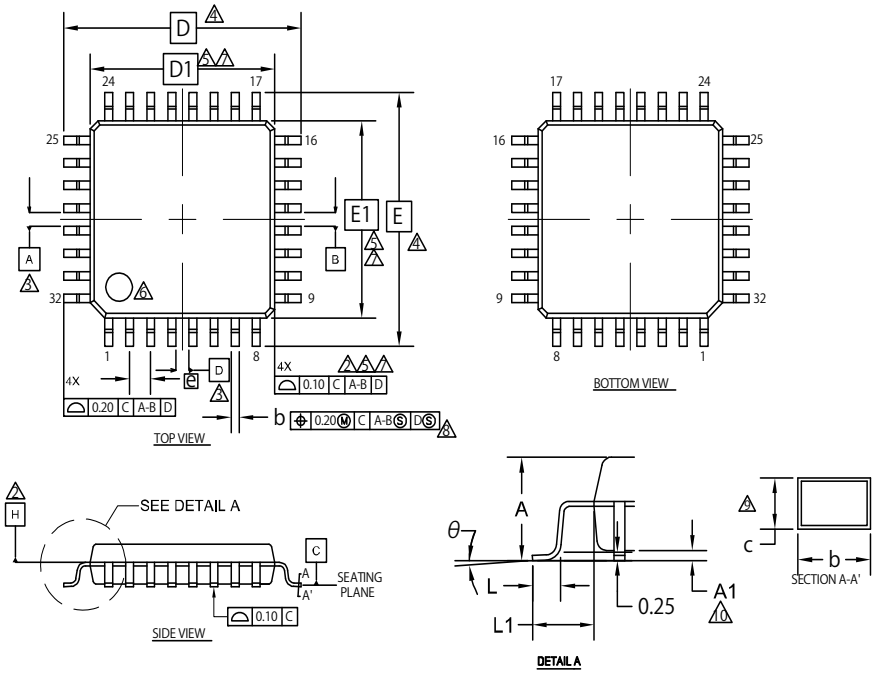
NOTES

1. ALL DIMENSIONS ARE IN MILLIMETER.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DIMENSIONING D INCLUDE MOLD FLASH. DIMENSIONING E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.025 mm PER SIDE. D and E1 DIMENSION ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONING D and E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, THE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A & B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSION APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm TO 0.25mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE THE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR MAY NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. LF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED
10. "A1" IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY EXCLUDING THE LID AND OR THERMAL ENHANCEMENT ON CAVITY DOWN PACKAGE CONFIGURATIONS.
11. JEDEC SPECIFICATON NO. REF : N/A

002-16904 **

PACKAGE OUTLINE, 24 LEAD SOP
15.34X7.50X2.80 MM SOL024 REV**

Package Type	Package Code
LQFP 32	LQB032



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
b	0.32	0.35	0.43
c	0.13	—	0.18
D	9.00 BSC		
D1	7.00 BSC		
e	0.80 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

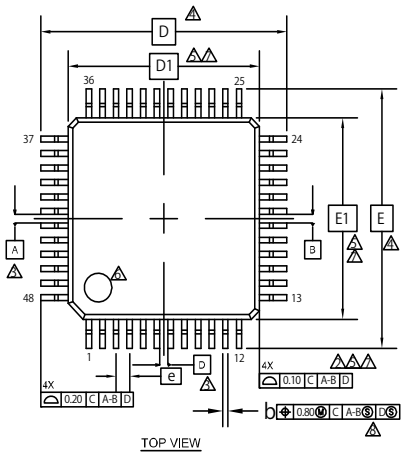
NOTES

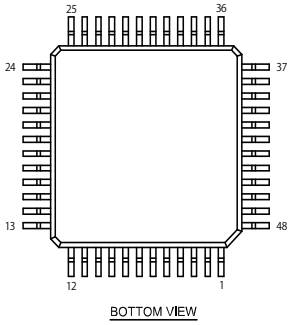
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

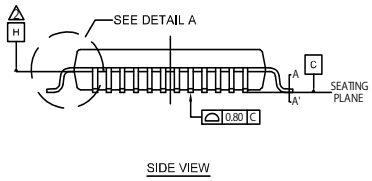
002-13879 **

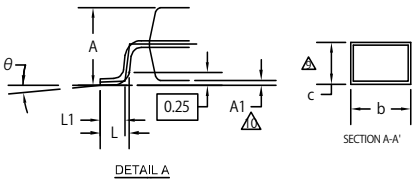
PACKAGE OUTLINE, 32 LEAD LQFP
7.0X7.0X1.6 MM LQB032 REV*.*

Package Type	Package Code
LQFP 48	LQA048









SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.15	—	0.27
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.50 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

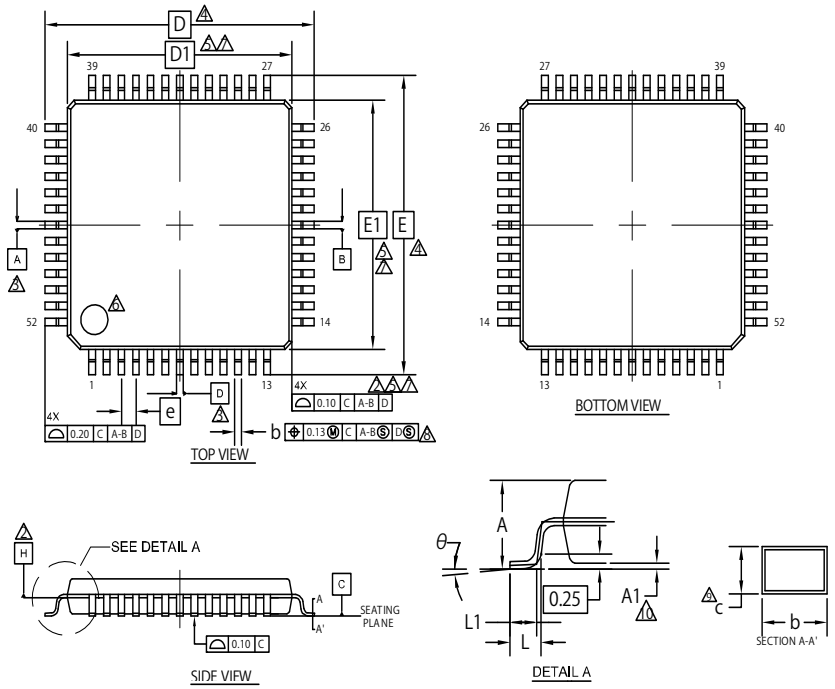
NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13731 **

PACKAGE OUTLINE, 48 LEAD LQFP
7.0X7.0X1.7 MM LQA048 REV**

Package Type	Package Code
LQFP 52	LQC052



SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.265	0.30	0.365
c	0.09	—	0.20
D	12.00 BSC		
D1	10.00 BSC		
e	0.65 BSC		
E	12.00 BSC		
E1	10.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13880 **

PACKAGE OUTLINE, 52 LEAD LQFP
10.0X10.0X1.7 MM LQC052 REV**

20. Major Changes in This Edition

Spansion Document Code: DS702-00013-0v02-E.

Page	Section	Details
11	Pin Functions MB95850K Series	Revised the function of the AREF pin. TS reference input pin ® TS reference impedance input pin
13	Pin Functions MB95860K Series	Revised the function of the AREF pin. TS reference input pin ® TS reference impedance input pin
17	Pin Functions MB95870K Series	Revised the function of the AREF pin. TS reference input pin ® TS reference impedance input pin
29	Pin Connection DBG pin	Revised details of "• DBG pin".
	$\overline{\text{RST}}$ pin	Revised details of "• $\overline{\text{RST}}$ pin".
40	I/O Map MB95850K Series	Revised the register name of the RSEL0 register. TS resistance select register 0 → TS sensitivity select register 0
		Revised the register name of the RSEL1 register. TS resistance select register 1 → TS sensitivity select register 1
		Revised the register name of the RSEL2 register. TS resistance select register 2 → TS sensitivity select register 2
		Revised the register name of the RSEL3 register. TS resistance select register 3 → TS sensitivity select register 3
42		Corrected the initial value of the TOUCHH register. 0b00000XXX → 0b0000XXXX

Page	Section	Details
47	I/O Map MB95860K Series	Revised the register name of the RSEL0 register. TS resistance select register 0 → TS sensitivity select register 0
		Revised the register name of the RSEL1 register. TS resistance select register 1 → TS sensitivity select register 1
		Revised the register name of the RSEL2 register. TS resistance select register 2 → TS sensitivity select register 2
		Revised the register name of the RSEL3 register. TS resistance select register 3 → TS sensitivity select register 3
		Revised the register name of the RSEL4 register. TS resistance select register 4 → TS sensitivity select register 4
49		Corrected the initial value of the TOUCHH register. 0b00000XXX → 0b0000XXXX
54	I/O Map MB95870K Series	Revised the register name of the RSEL0 register. TS resistance select register 0 → TS sensitivity select register 0
		Revised the register name of the RSEL1 register. TS resistance select register 1 → TS sensitivity select register 1
		Revised the register name of the RSEL2 register. TS resistance select register 2 → TS sensitivity select register 2
		Revised the register name of the RSEL3 register. TS resistance select register 3 → TS sensitivity select register 3
		Revised the register name of the RSEL4 register. TS resistance select register 4 → TS sensitivity select register 4
		Revised the register name of the RSEL5 register. TS resistance select register 5 → TS sensitivity select register 5
		Revised the register name of the RSEL6 register. TS resistance select register 6 → TS sensitivity select register 6
57	I/O MAP MB95870K Series	Corrected the initial value of the TOUCHH register. 0b00000XXX → 0b0000XXXX

Page	Section	Details
84	I/O Ports MB95850K Series 6.Port F (4)Port F operations •Operation as an input port	Added the following statement. For a pin shared with other peripheral functions, disable the output of such peripheral functions.
118	I/O Ports MB95860K Series 6.Port F (4)Port F operations •Operation as an input port	Added the following statement. For a pin shared with other peripheral functions, disable the output of such peripheral functions.
153	I/O Ports MB95850K Series 5.Port 7 (4)Port 7 operations •Operation as an output port	Deleted the following statement. For a pin shared with other peripheral functions, disable the output of such peripheral functions.
157	6.Port F (4)Port F operations •Operation as an input port	Added the following statement. For a pin shared with other peripheral functions, disable the output of such peripheral functions.
175	Electrical Characteristics Recommended Operating Conditions	Revised the remark in "• DBG/$\overline{\text{RST}}$/C pins connection diagram".
176	DC Characteristics	Revised the remark of the parameter "Input leak current (Hi-Z output leak current)". When pull-up resistance is disabled ® When the internal pull-up resistor is disabled
		Rename the parameter "Pull-up resistance" to "Internal pull-up resistor".
		Revised the remark of the parameter "Internal pull-up resistor". When pull-up resistance is enabled ® When the internal pull-up resistor is enabled
183	AC Characteristics (2)Source Clock/Machine Clock	Added the maximum value of F_{SP} of the parameter "Source clock frequency". 12.5
196	AC Characteristics (11)TS	Revised the minimum values and typical values of the parameter "Touch sensitivity".
		Deleted the parameter "Sensor clock".
		Added the parameter "Sensor clock" to "Sensor clock (sensing phase)".
		Added remark *2.
197	A/D Converter (1)A/D Converter Electrical Characteristics	Corrected the symbol of the parameter "Zero transition voltage". $V_{OT} \rightarrow V_{0T}$
199, 200	A/D Converter (3)Definitions of A/D Converter Terms	Corrected the symbol of the zero transition voltage. $V_{OT} \rightarrow V_{0T}$

Document History Page

Document Title: MB95F856K, MB95F866K, MB95F876K New 8FX MB95850K/860K/870K Series Datasheet Document Number: 002-09305				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	YSKA	08/02/2012	Migrated to Cypress and assigned document number 002-09305. No change to document contents or format.
*A	5560459	YSKA	12/20/2016	Migrated to Cypress datasheet template
*B	5844036	YSAT	08/04/2017	Adapted new Cypress logo
*C	6038234	YSAT	01/22/2018	Corrected the package codes as bellow FPT-24P-M10 → STI024 FPT-24P-M34 → SOL024 FPT-32P-M30 → LQB032 FPT-48P-M49 → LQA048 FPT-52P-M02 → LQC052 Updated “19. Package Dimension” Updated Arm trademark and the last page

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