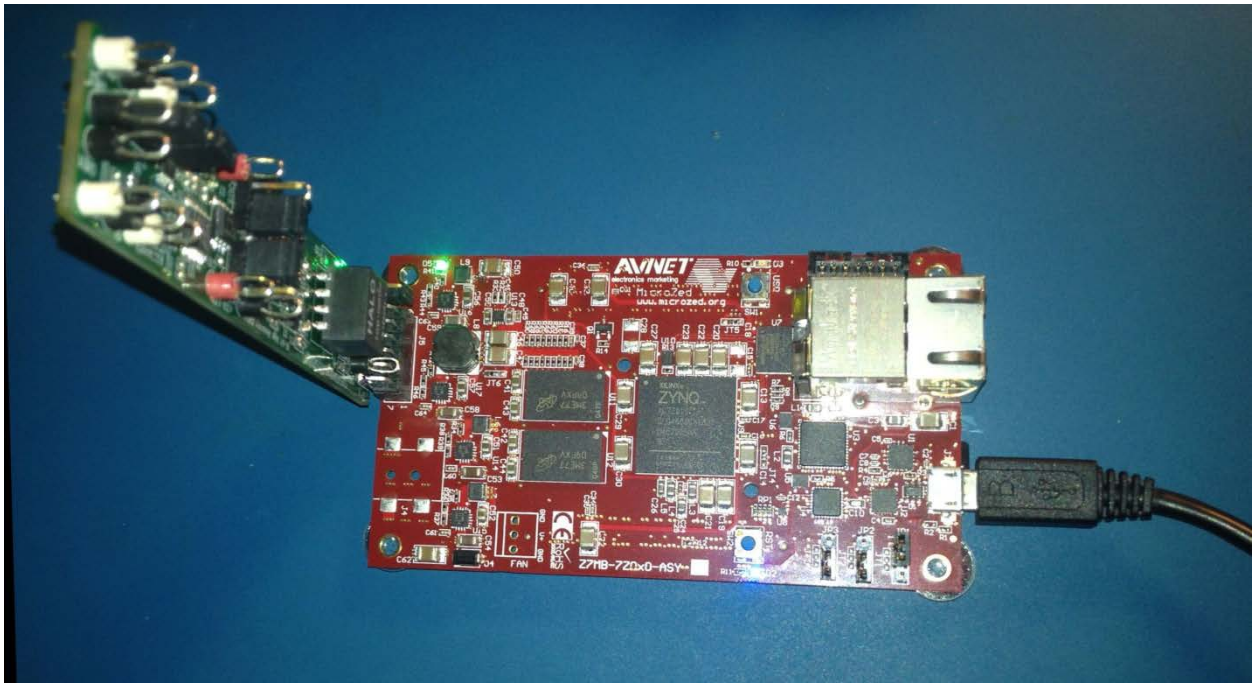
Santa Fe (MAXREFDES5#) MicroZed Quick Start Guide

Rev 0; 5/14



Maxim Integrated 160 Rio Robles, San Jose, CA 95134 USA 1-408-601-1000

Table of Contents

1. Required Equipment

- Santa Fe (MAXREFDES5#) board
- MicroZed™ development kit
- Industrial sensor or signal source
- To run the binary from SD card:
  - Host PC with Windows® OS with Terminal Software installed (HyperTerminal) and one USB port
  - CP2104 device drivers (Silicon Labs USB-UART)
  - 4GB FAT32 formatted SD card
- To run the software from the Xilinx® SDK:
  - PC with Windows® OS with Xilinx Vivado®/SDK version 13.4 or later and two USB ports
  - License for Xilinx EDK/SDK (free WebPACK™ license is OK)
  - Xilinx Platform Cable USB II-compatible JTAG device

2. Overview

The Santa Fe MicroZed software can be downloaded to the MicroZed board via two methods:

- (Easiest) Boot from an SD card containing a binary file that loads the necessary CPU bootloader, FPGA bitstream, and MAXREFDES5# executable file. This approach is explained in detail in Section 3 of this document.
- (Flexible) Use the Xilinx SDK to download the board bitstream and executable file. This approach allows the source code to be modified. This approach is explained in detail of Section 4 of this document.

3. Boot from an SD Card

The steps below describe how to download the binary image (BOOT.BIN), install on an SD card, and begin using the MAXREFDES5 system.

1) Download the latest BOOT.BIN file from the MAXREFDES5# page.
2) Obtain a FAT32 formatted 4GB SD card such as the one provided with the MicroZed board.
3) Copy the BOOT.BIN file onto the SD card. A USB-to-SD adapter and Micro-SD-to-SD adapter are normally required to do this on a PC with Windows OS (Figure 1).
4) Ensure the only file on the Micro-SD card is the BOOT.BIN file. **Note that if using the Avnet-supplied SD card, it comes pre-installed with a Linux test image. This image needs to be removed.**
5) Remove the SD card from the host PC. Make sure the MicroZed board is powered off, and insert the SD card in the MicroZed (Figure 2).
6) Configure the MicroZed boot source jumpers to boot from SD (Figure 3).

7) Insert the MAXREFDES5# reference board in the J5 connector (Figure 4). Note the orientation so that the component side of the MAXREFDES5# board faces the component side of the MicroZed board.
8) Connect a Micro-USB cable to MicroZed USB connector J2. This will power the MicroZed board. If the BOOT.BIN file has loaded successfully, the red LED (D3) should begin blinking, indicating the MAXREFDES5 software is running.

   Note: The USB UART on the MicroZed board uses a Silicon Labs CP2104 USB-UART device. Drivers are normally installed with the Xilinx SDK release, but if needed, they can be downloaded from the Silicon Labs website.
9) Open HyperTerminal or similar Terminal program on the PC. Find the appropriate COM port, usually a higher number port, such as COM4, or COM6, and configure the connection for 115200, n, 8, 1, none (flow control).
10) The MAXREFDES5 software will display a message to **Press a key to continue.** (Figure 5).
11) Press any key, and the demo will begin (Figure 6). Use the **Menu** selections to choose an analog sample channel.

Figure 1. USB-SD, SD-Micro-SD, and Micro-SD Card

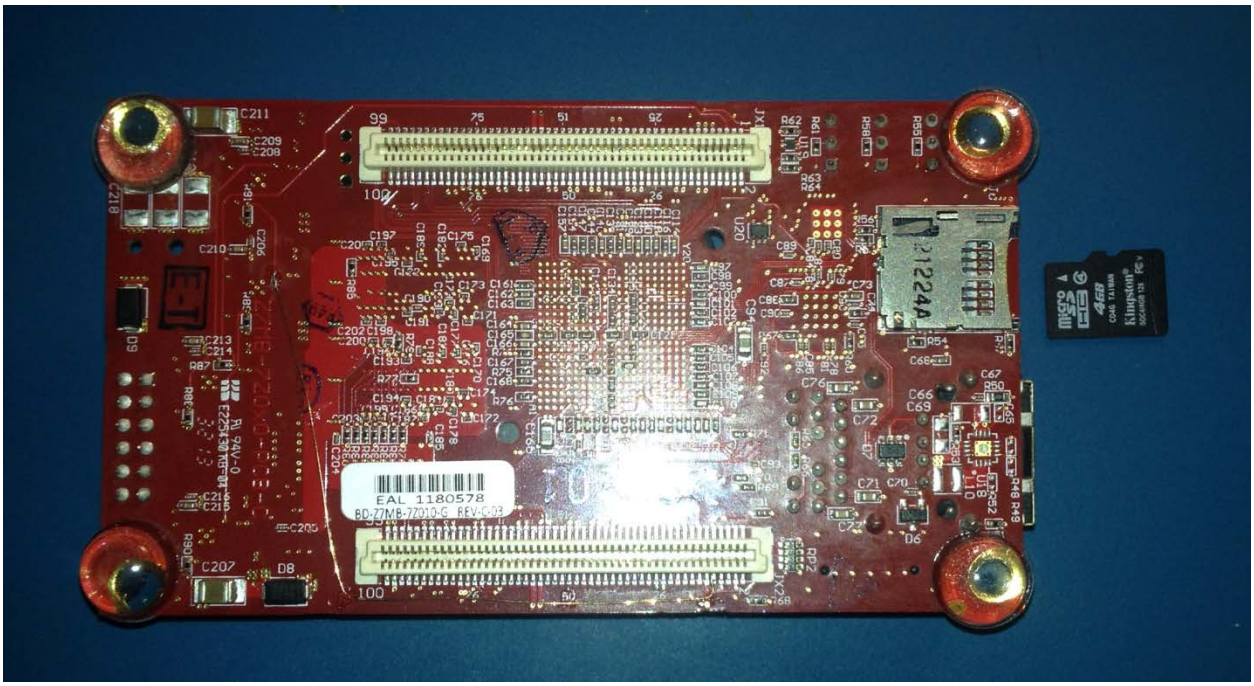


Figure 2. MicroZed SD Card Slot and Micro-SD Card

Figure 3. MicroZed Board Boot from SD Jumper Settings

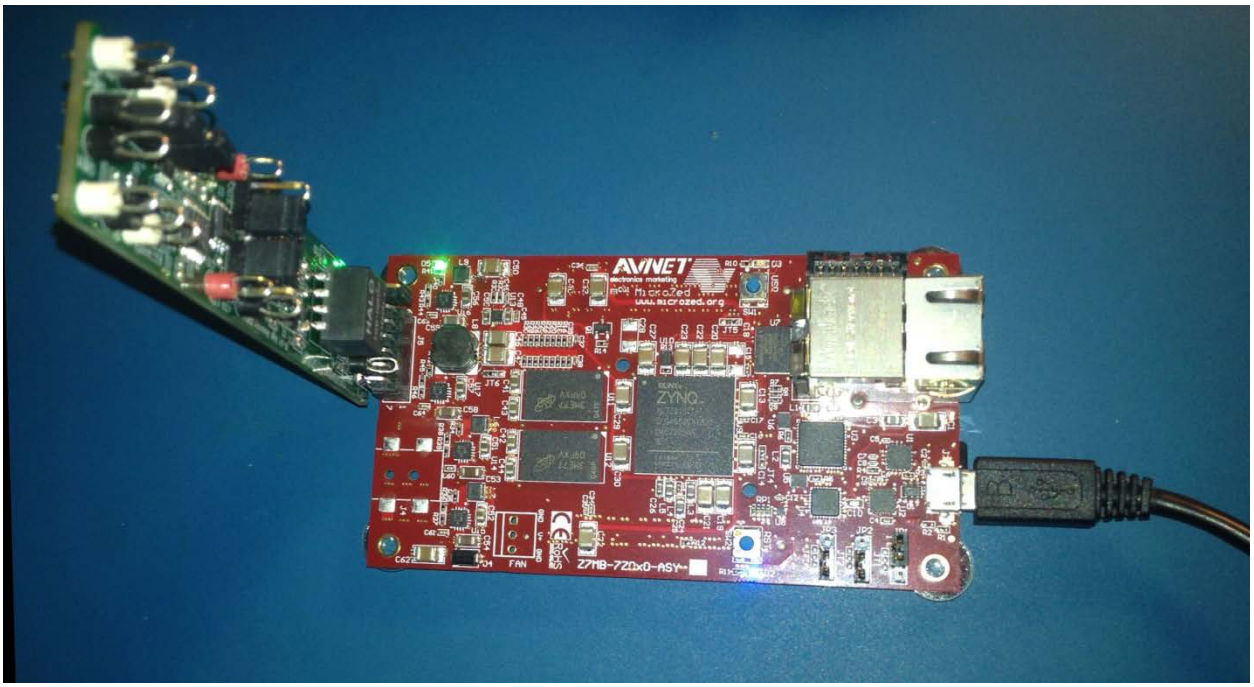


Figure 4. MAXREFDES5# Installed in J5 Connector

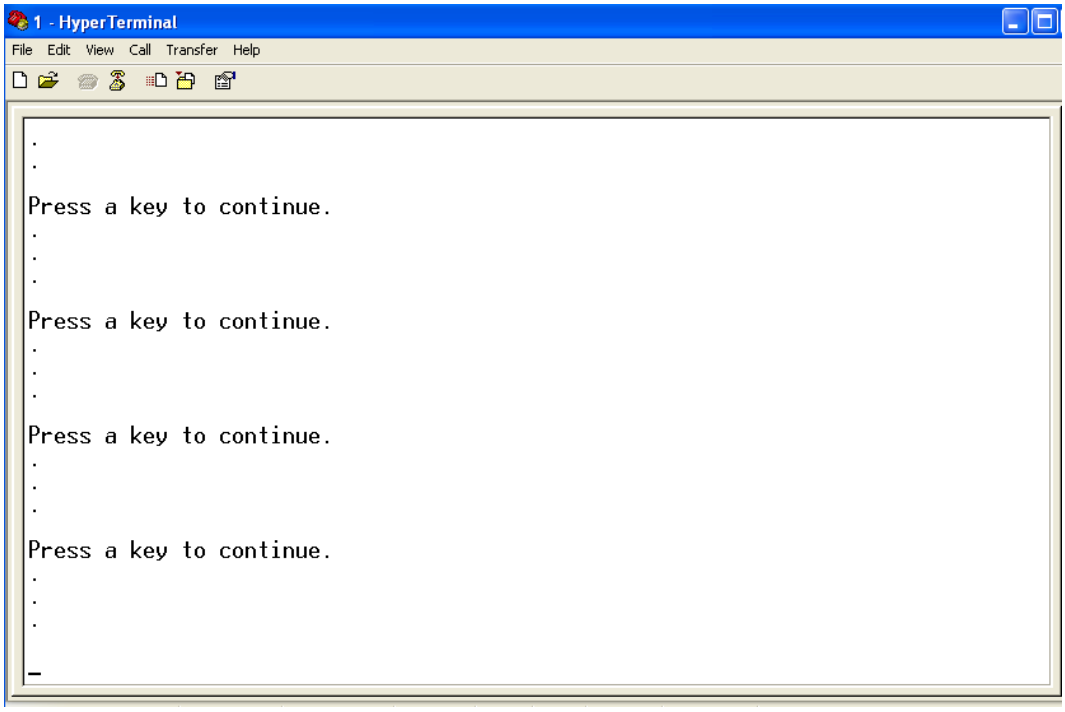


Figure 5. MAXREFDES5# Opening Screen

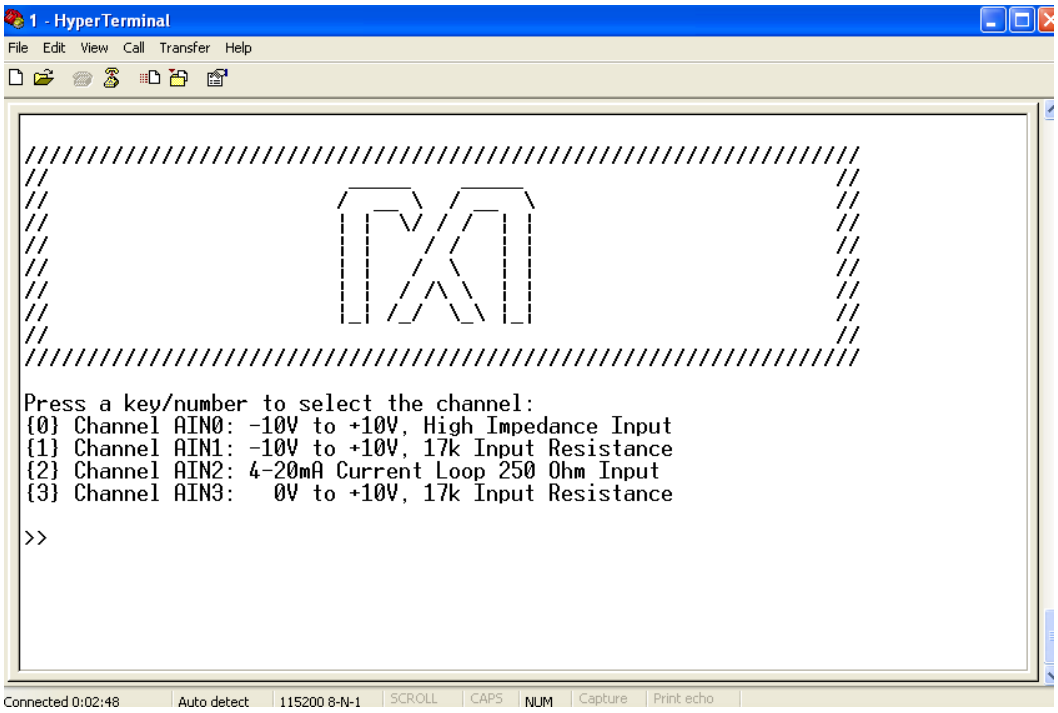


Figure 6. MAXREFDES5# Main Demo Menu

4. Download Demonstration from Xilinx SDK

The steps below provide a high-level description of how to download and use the MAXREFDES5 demonstration from within the Xilinx SDK. This method allows the user to access and modify the source code for the reference design demonstration.

1) Connect the Santa Fe board to the J5 port of a MicroZed board as shown in Figure 4. Ensure the connector is aligned so that the component side of the MAXREFDES5# board points towards the component side of the MicroZed board.
2) Download the latest “all design files” **RD5V04_00.ZIP** file located at the Santa Fe page.
3) Extract the **RD5V04_00.ZIP** file to a directory on your PC.
4) Open the Xilinx SDK.
5) Download the bitstream (.BIT) file to the board. This bitstream contains the FPGA hardware design and software bootloader.
6) Use Xilinx SDK to download and run the executable file (.ELF) on one of the two ARM® Cortex™ -A9 processors.

Detailed instructions for this process can be found in Section 6 of this document.

5. Included Files

The top level of the hardware design is a Xilinx Vivado Project (.xpr) for Xilinx Vivado version 13.4. The Verilog-based arm_system_wrapper.v module provides FPGA/board net connectivity and instantiates both the Zynq® Processing System as well as the Zynq SPI peripheral that interfaces directly to the Pmod™ port. A Xilinx software development kit (SDK) project is supplied and includes an example c program to evaluate the Santa Fe subsystem reference design. The c-code driver routines are portable to the user's own software project.

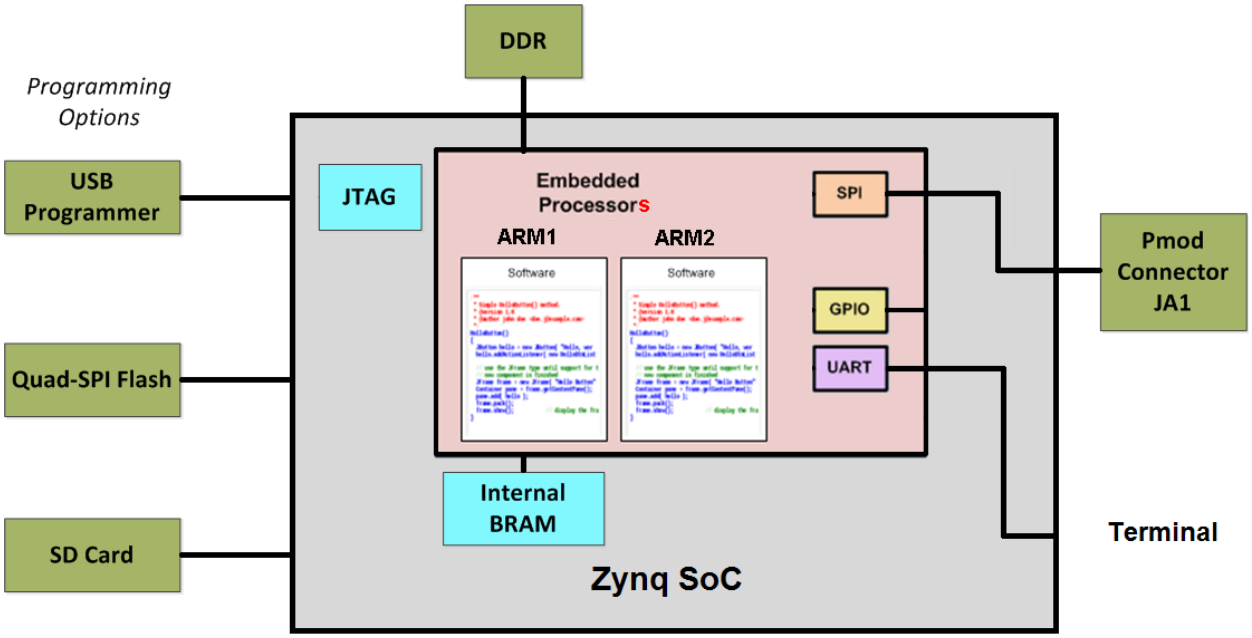


Figure 7. Block Diagram of FPGA Hardware Design

6. Procedure

1. Connect the Santa Fe board to the J5 port of a MicroZed board as shown in Figure 4.

2. Power up the ZedBoard by connecting a Micro-USB cable to the USB UART port J2.

3. Connect a Xilinx-compatible JTAG debugger to the J3 JTAG port on the MicroZed.

4. Download the latest "all design files" **RD5V04_00.ZIP** file at **www.maximintegrated.com/AN5561**. All files available for download are available at the bottom of the page.

5. Extract the **RD5V04_00.ZIP** file to a directory on your PC. The location is arbitrary but the maximum path length limitation in Windows (260 characters) should not be exceeded.

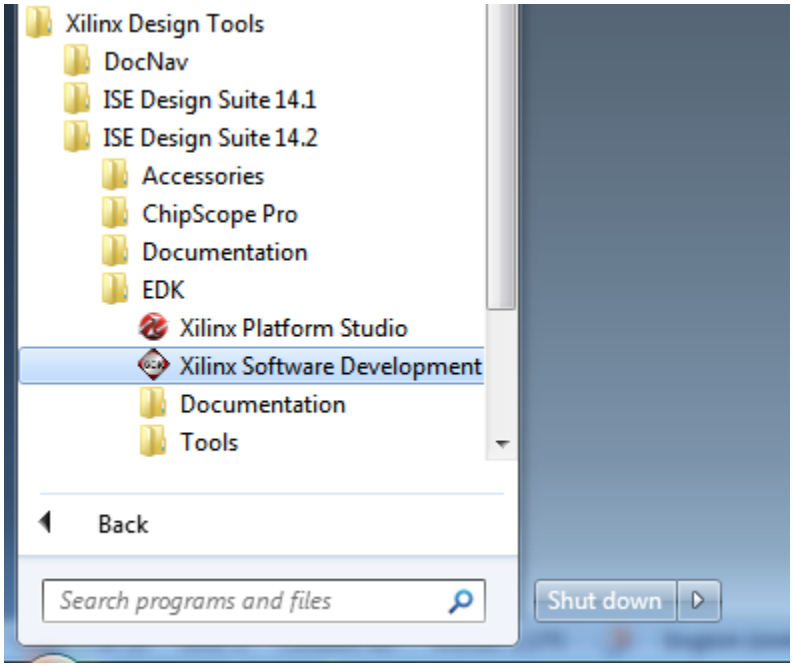
   In addition, the Xilinx tools require the path to not contain any spaces.

   C:\Do Not Use Spaces In The Path\RD5V04_00.ZIP (This path has spaces.)

   For the purposes of this document, it will be **C:\designs\maxim\RD5V04_00\RD5_uZED_V01_00**

   See **Appendix A: Project Structure and Key Filenames** in this document for the project structure and key filenames.

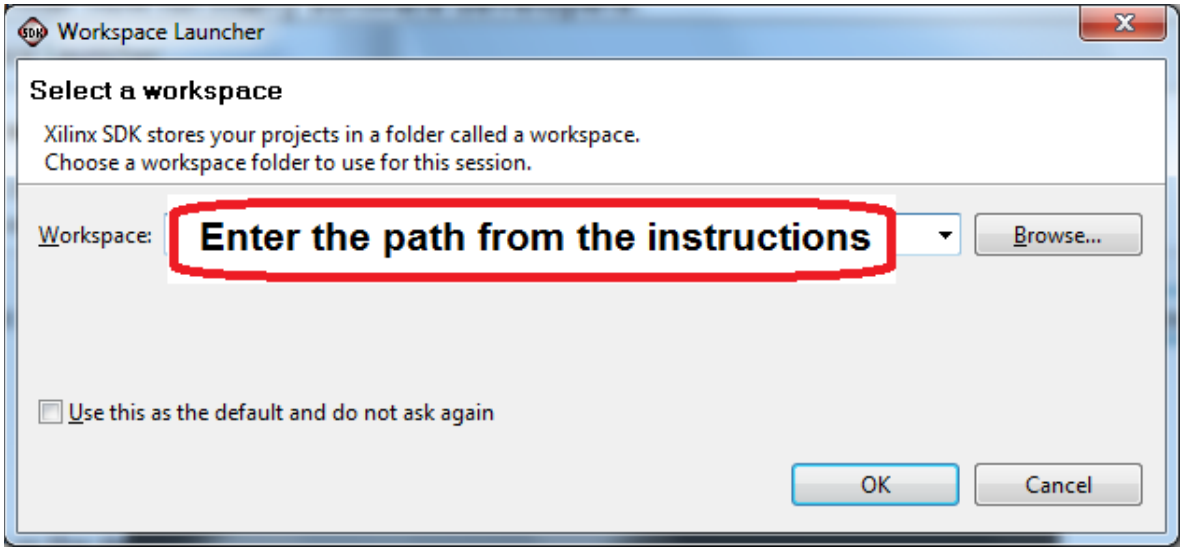
6. Open the **Xilinx Software Development Kit (SDK)** from the Windows **Start** menu.



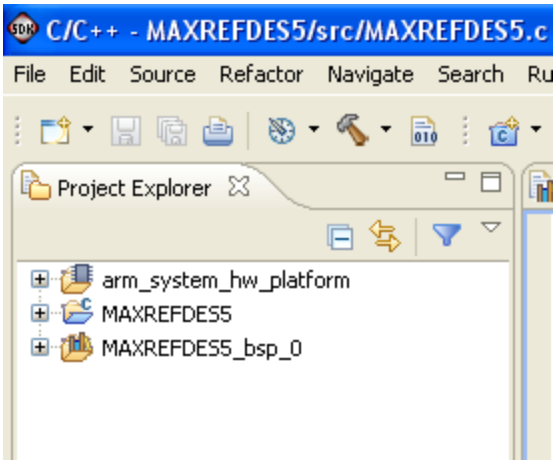
7. SDK will prompt for a workspace directory, which is the location where the software project is located. For this example, it is:

C:\designs\maxim\RD5V04_00\RD5_uZED_V01_00\Design_Files\top.sdk\SDK\SDK_Export

Click **OK** and SDK will open. The Xilinx SDK is based on an Eclipse™-based IDE, so it will be a familiar flow for many software developers.



8. Review the SDK IDE. The **Project Explorer** in the upper left tab should have three components as shown in the image below. If all three subfolders are present, you can skip the next step.

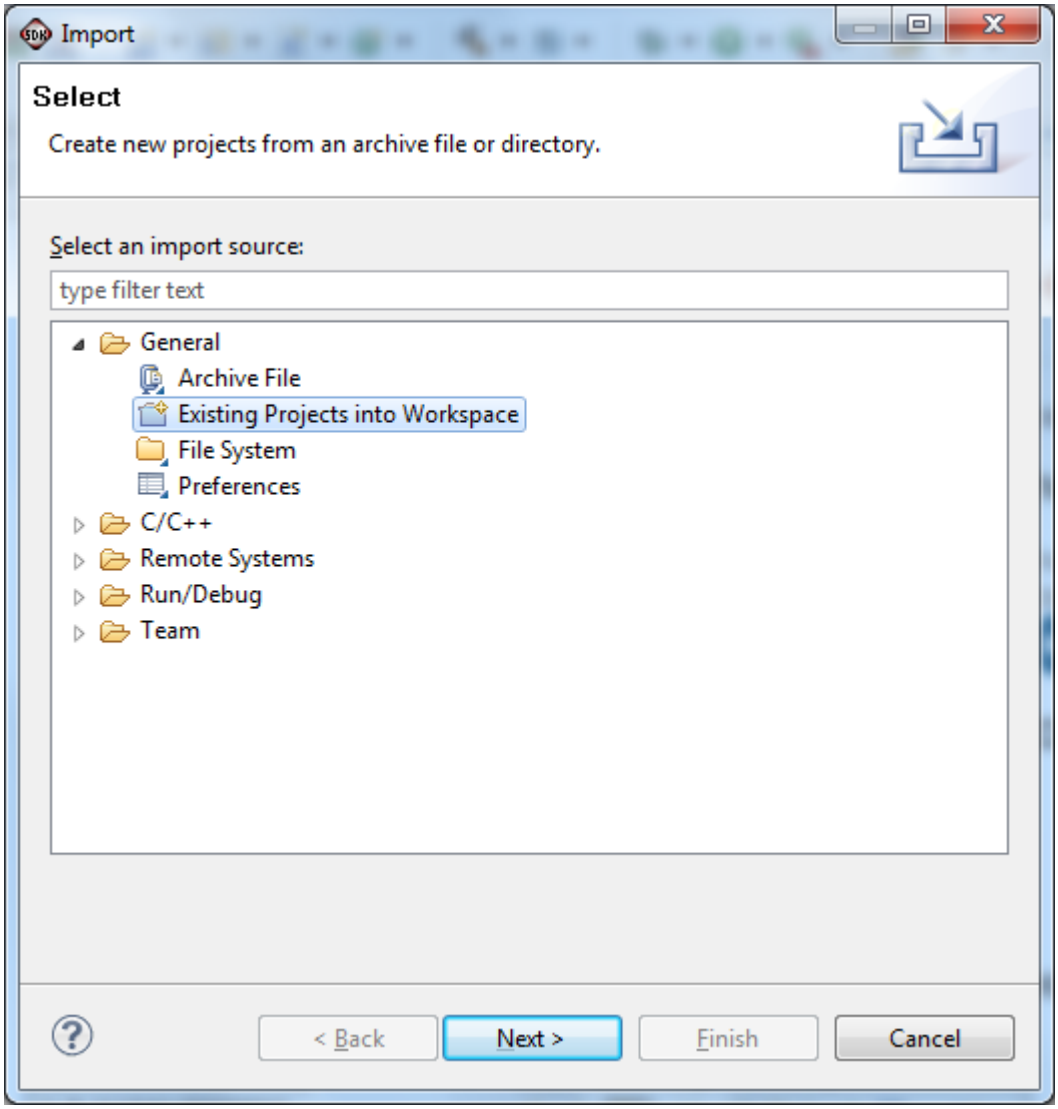


9. If the **Project Explorer** does not contain these five subfolders, launch the **File | Import** menu, expand the **General** folder, and select **Existing Projects into Workspace**. Click **Next**. Set the root directory to:

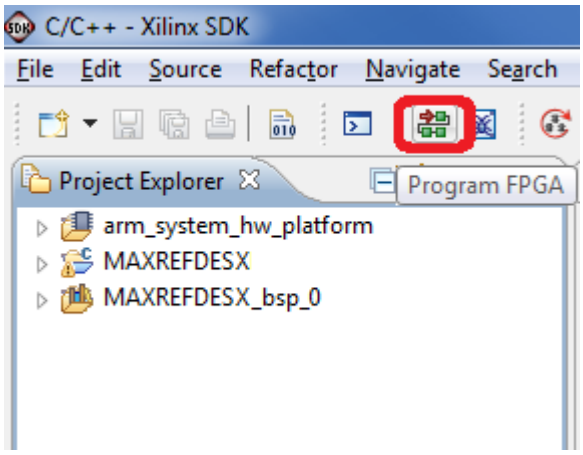
   C:\designs\maxim\RD5V04_00\RD5_uZED_V01_00\Design_Files\top.sdk\SDK\SDK_Export

   and the missing projects should appear in SDK **Project Explorer** with their checkboxes checked.

   Click **Finish** to import the projects.



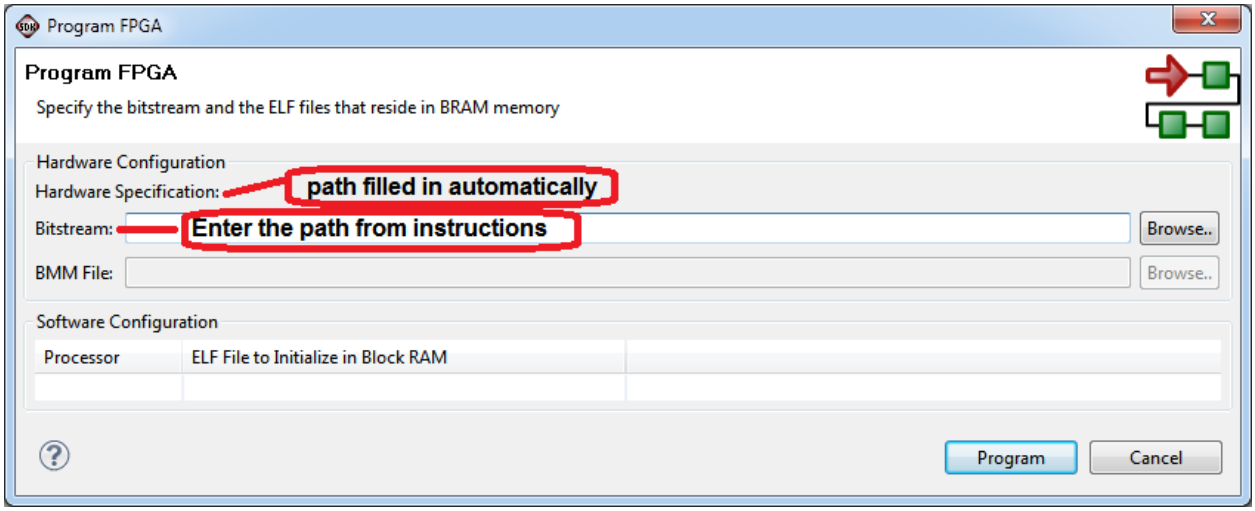
10. To download the bitstream (.BIT) file to the board, click on the **Program FPGA** icon (which looks like a green chain of devices).



The **Program FPGA** dialog box appears. From here, an FPGA bitstream (.BIT) file is selected. Be sure to select the .BIT file by using the path below.

Bitstream:
C:\Designs\maxim\RD5V04_00\RD5_uZED_V01_00\Design_Files\top.runs\impl_1\arm_system_wrapper.bit

Press **Program**.



It takes approximately 10 seconds to download the FPGA, then a message box indicating **FPGA configuration complete** appears. If programming fails, try unplugging and reconnecting the USB programmer cable or restarting Xilinx SDK.

11. Set up the terminal program to run on the PC using the following steps. Before loading the executable firmware file on the FPGA, the terminal program on the PC should be running. The example firmware running on the FPGA communicates with the PC via a USB port set up to emulate a serial port (UART). To establish this communication link, the PC must be configured with the appropriate Windows drivers. A suitable terminal program such as Tera Term or HyperTerminal should be invoked.

    The MicroZed board utilizes a Silicon Labs CP2104 USB-UART bridge IC for serial communications. If the Windows cannot automatically install the driver for the USB-UART bridge IC, the driver is available for download from www.silabs.com.

    Once installed, Windows will assign a previously unused COM port. Use the Windows **Control Panel | System | Device Manager** to determine the COM port number. (It will be named Cypress Serial.) Make a note of which COM port this is. That information is needed in the next step.

    Next, a terminal emulation program needs to be installed and launched. For Windows XP® and earlier systems, the HyperTerminal program is the usual choice. However, since HyperTerminal was eliminated from Windows 7, it may be necessary to locate an alternative. Several are available; one good choice is called Tera Term (http://ttssh2.sourceforge.jp/). Whatever terminal program you choose, the communication should be set up by opening the COM port number previously described above and the port configured as :

    bits per second: **115200**

    data bits: **8**;

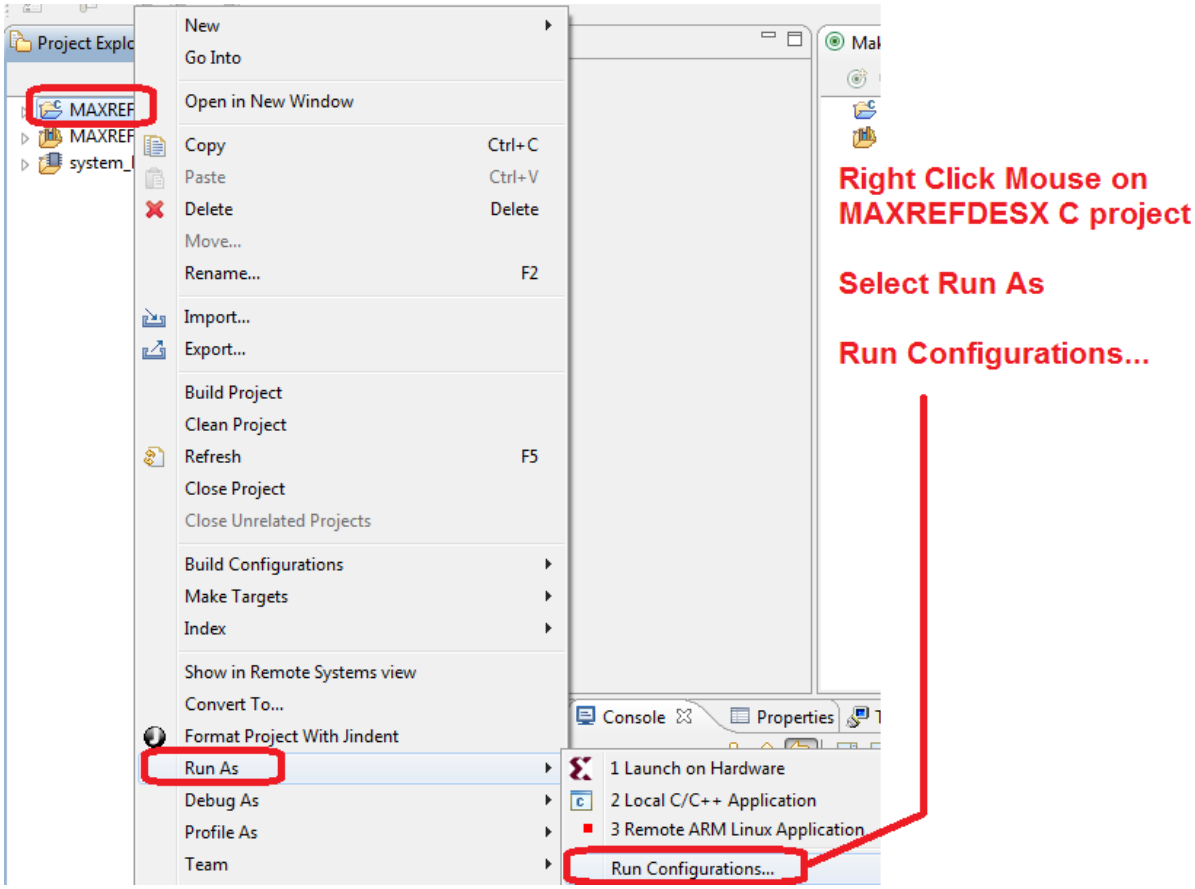
    parity: **none**;

    stop bits: **1**;

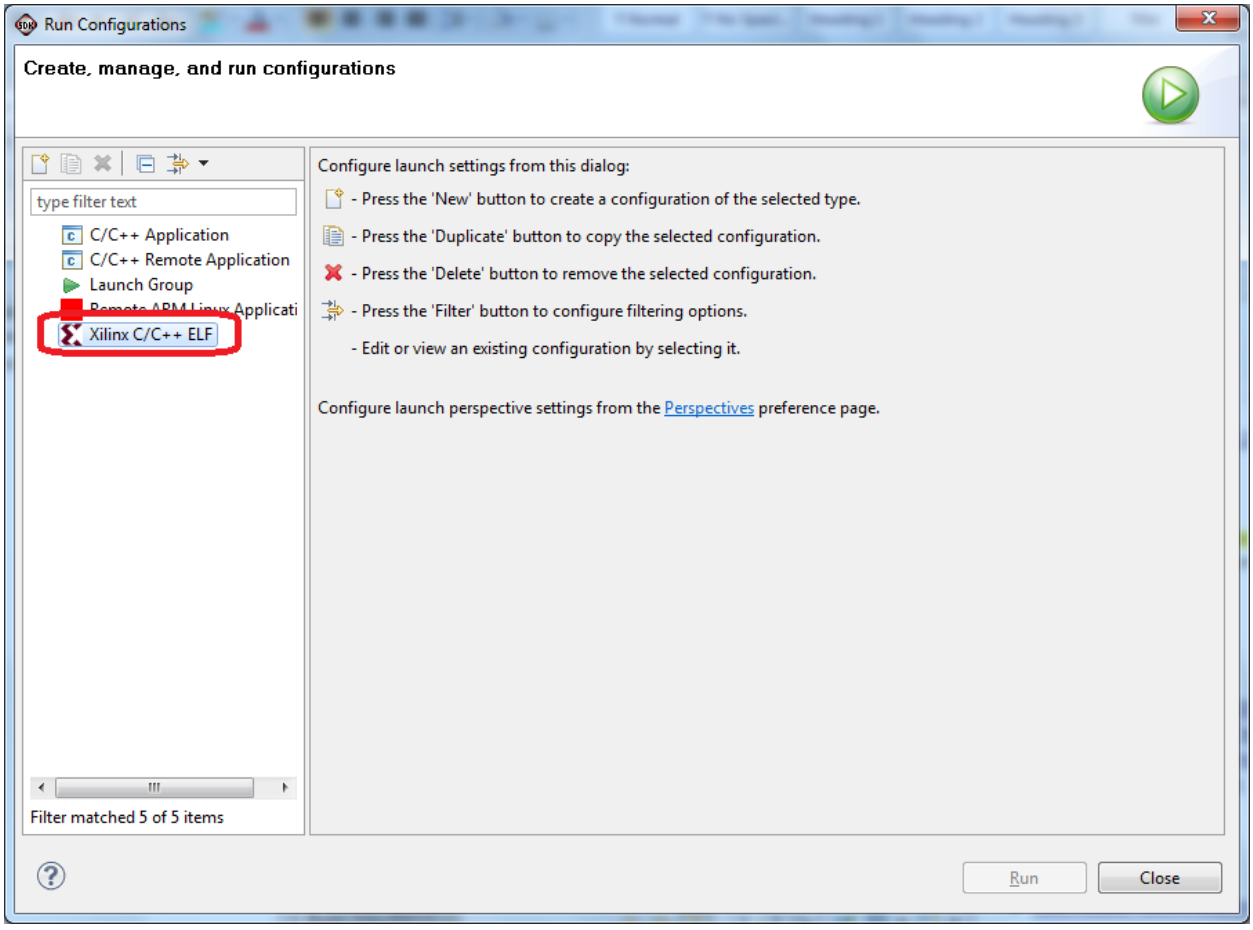
    flow control: **none**.

12. Use the Xilinx SDK to download and run the executable ELF (.ELF) file on the ARM Cortex-A9 processor using the following steps.

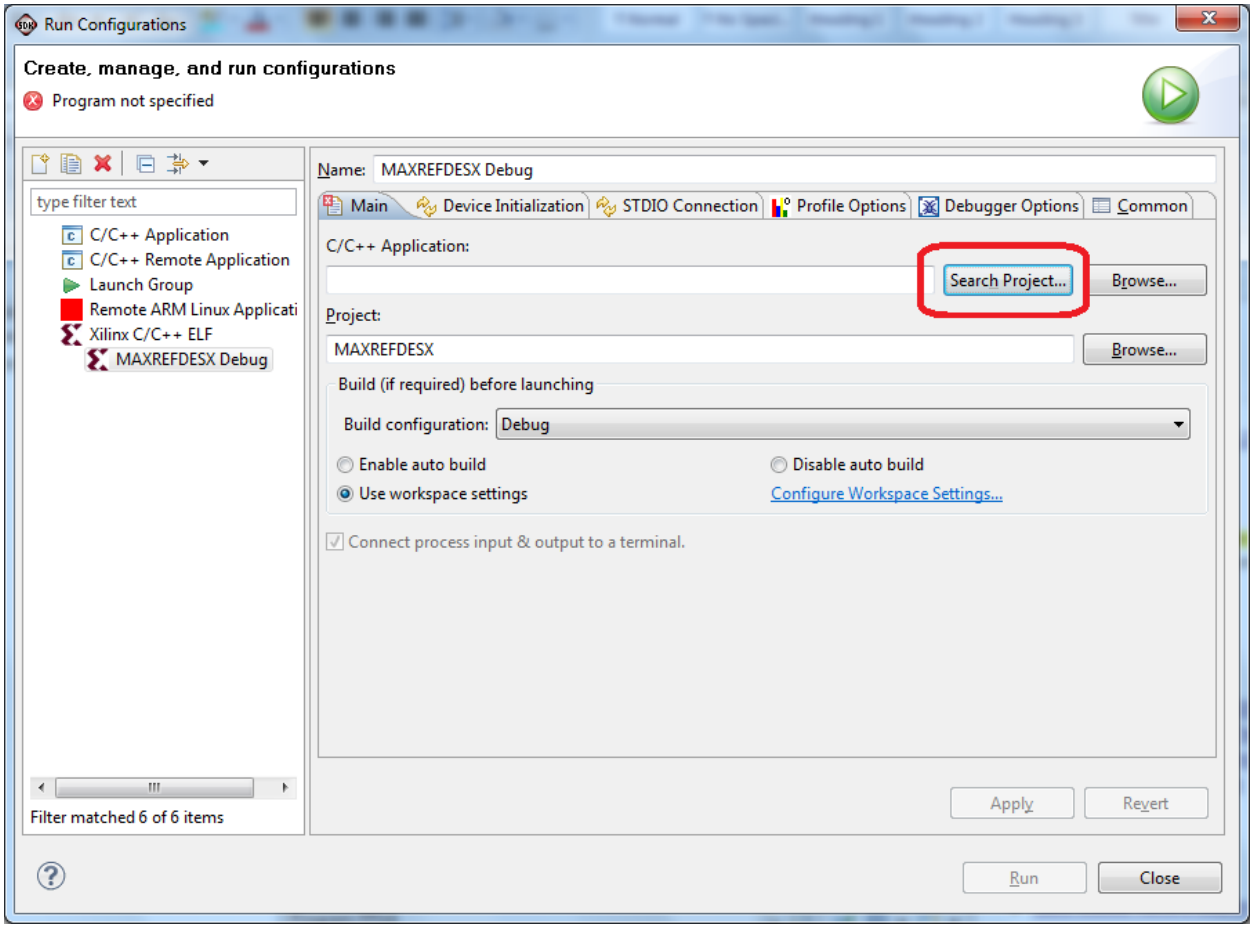
    Right-click the mouse while the **MAXREFDES5 C** project is selected, choose the **Run As** menu, and then **Run Configurations…** menu as shown below.



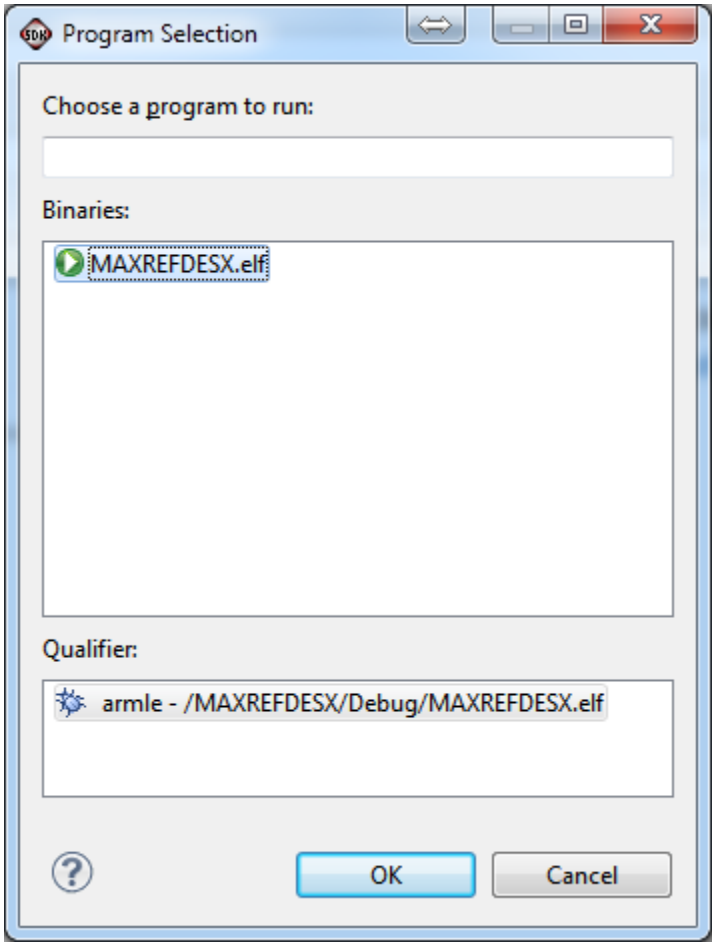
Next, double-click the mouse on the **Xilinx C/C++ ELF** menu.



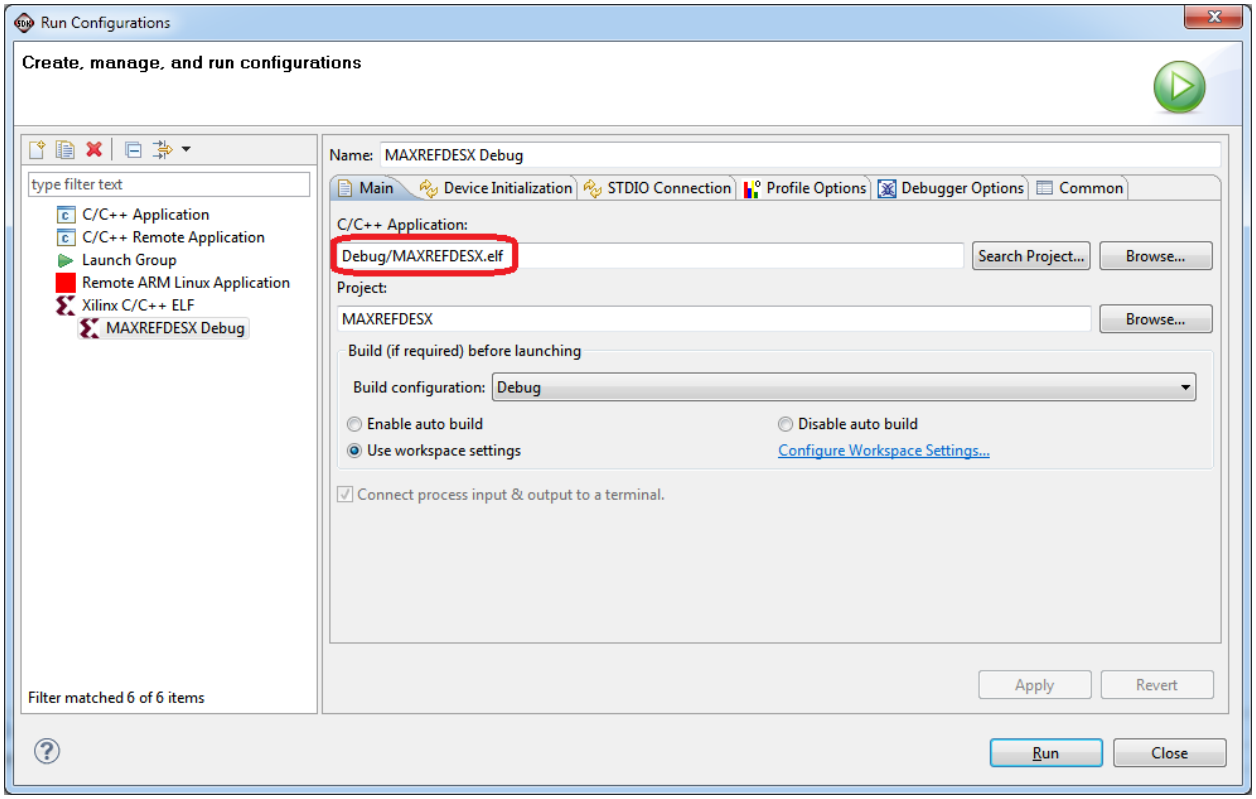
Next, press the **Search Project** button.



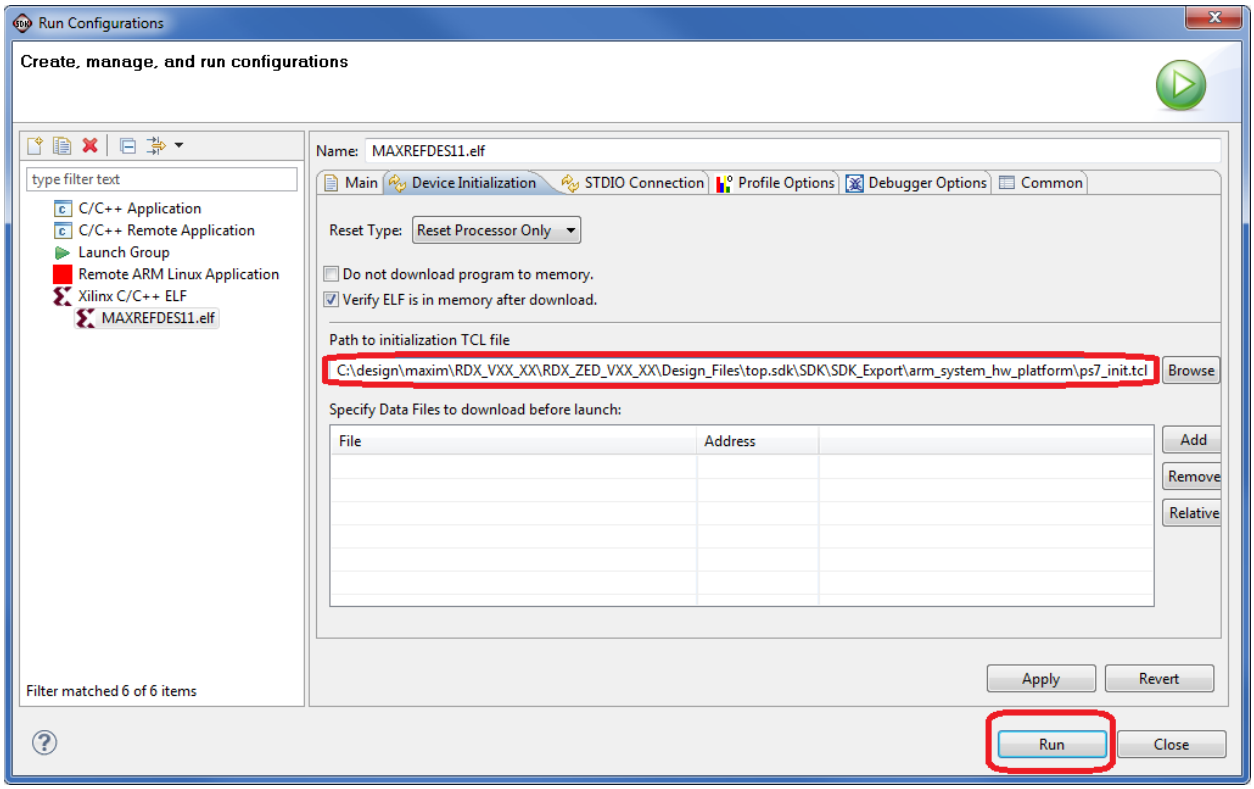
Double-click on the **MAXREFDES5.elf** binary.



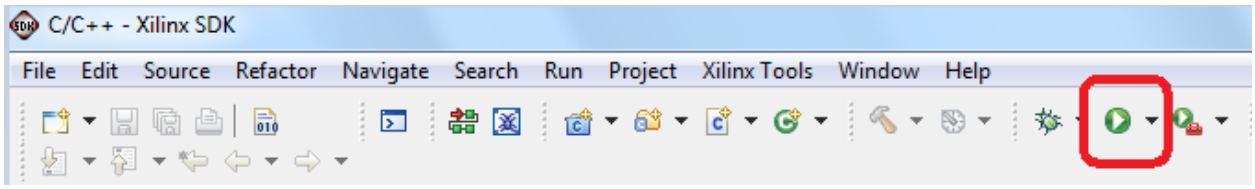
Verify the application is selected on the **Main** tab.



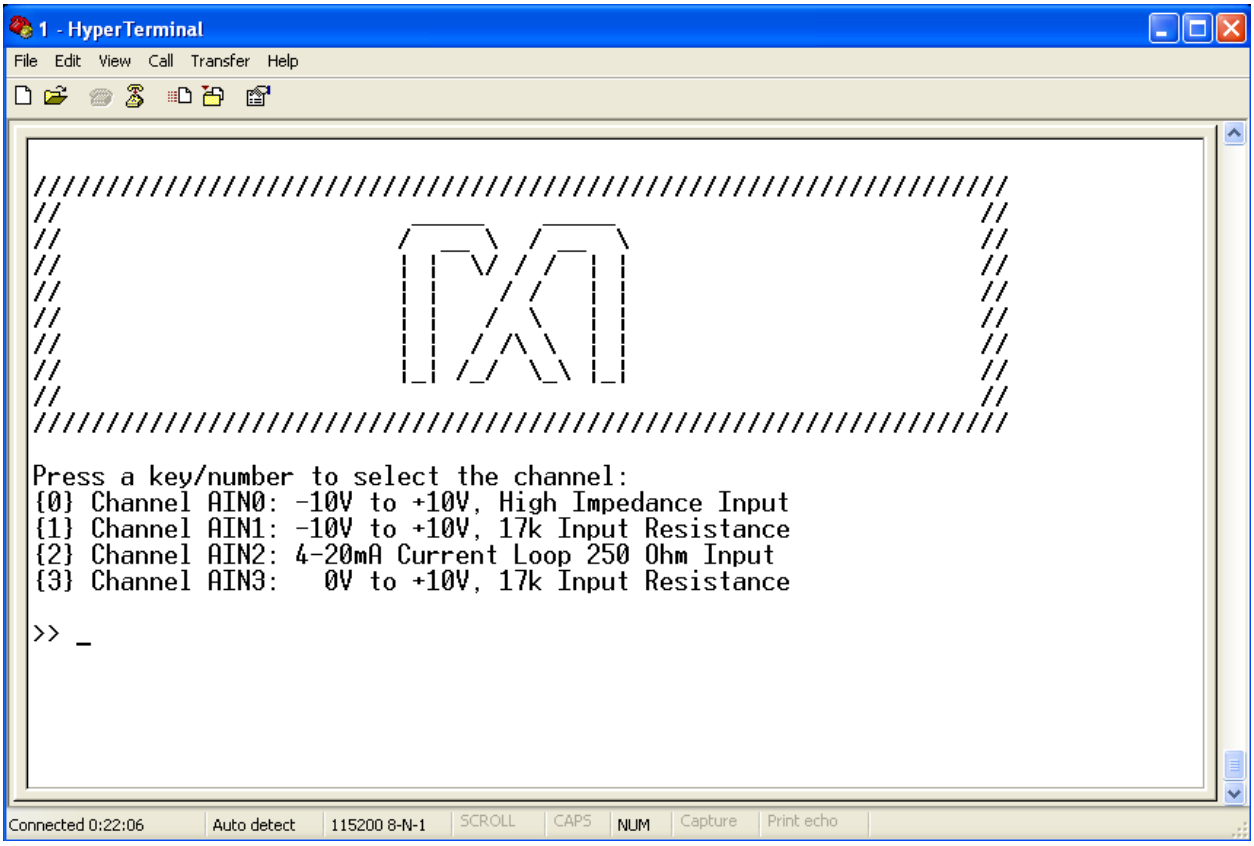
On the **Device Initialization** tab, click **Browse…** button to select the "**ps7_init.tcl**" initialization TCL file and press the **Run** button.



Once the Debug/MAXREFDES5 configuration is set up once, you just need to press the **Run** button if you ever want to run the program again.

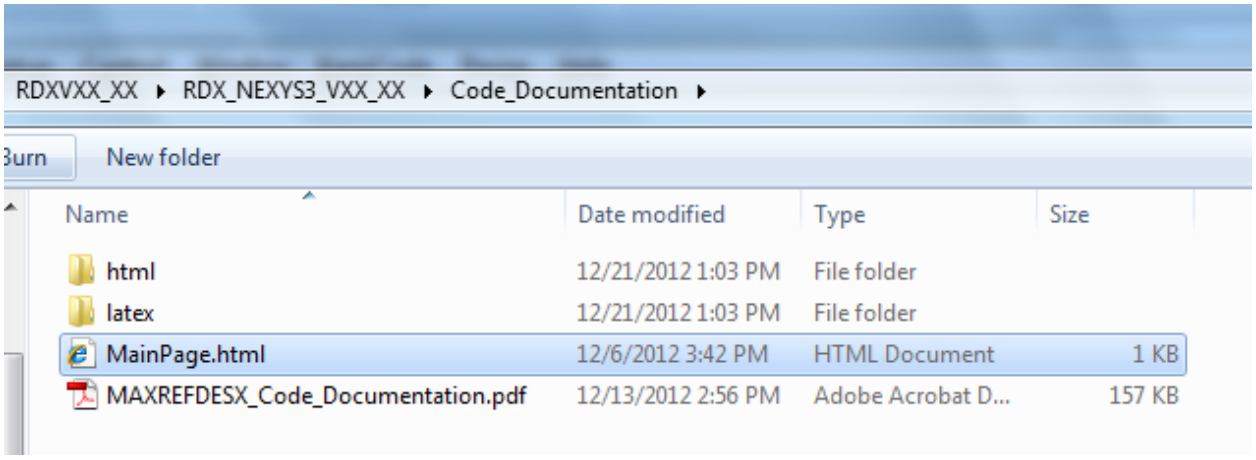


At this point, the application will be running on the Cortex-A9 and the terminal program will show the menu below. Make the desired selections by pressing the appropriate keys on the keyboard. For example, to select channel AIN0, press **0**.



7. Code Documentation

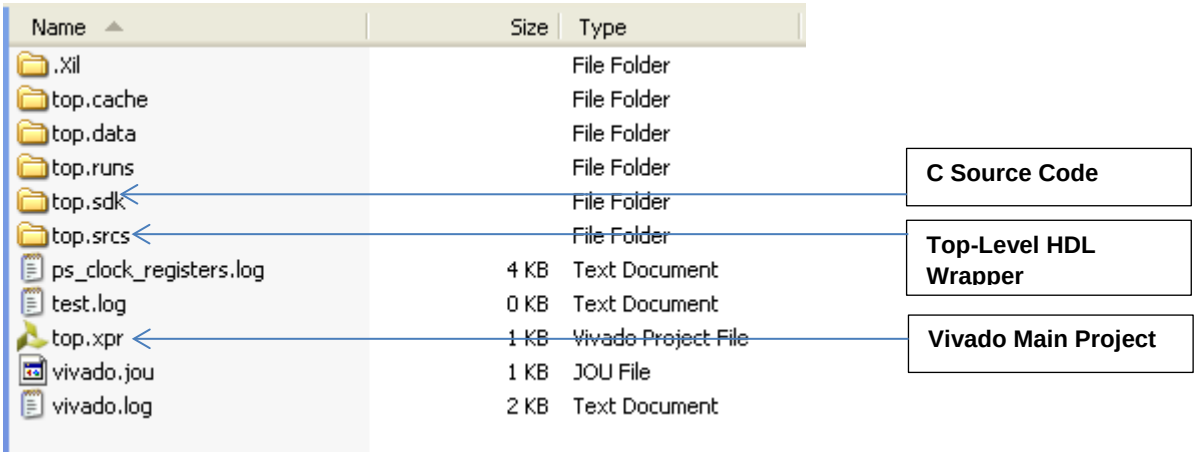
Code documentation can be found at:
C:\Designs\maxim\RD5V04_00\RD5_uZED_V01_00\Code_Documentation



To view the code documentation in HTML format with a browser, open the **MainPage.html** file.

To view the code documentation in .PDF format with a PDF reader, open the **MAXREFDES5_Code_Documentation.pdf** file.

8. Appendix A: Project Structure and Key Filenames



9. Trademarks

ARM is a registered trademark of ARM Ltd.
Cortex is a trademark of ARM Ltd.
Eclipse is a trademark of Eclipse Foundation, Inc.
MicroBlaze is a trademark of Xilinx, Inc.
MicroZed is a trademark of ZedBoard.org.
Pmod is a trademark of Digilent Inc.
Vivado is a registered trademark of Xilinx, Inc.
WebPACK is a trademark of Xilinx, Inc.
Windows is a registered trademark and registered service mark and Windows XP is a registered trademark of Microsoft Corporation.
Xilinx is a registered trademark and registered service mark of Xilinx, Inc.
ZedBoard is a trademark of ZedBoard.org.
Zynq is a registered trademark of Xilinx, Inc.

10. Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/14	Initial release	—