ATA5577C – Read/Write LF RFID IDIC 100 kHz to 150 kHz

Introduction

The ATA5577C is a contactless read/write Identification Integrated Chip (IDIC®) for applications in the 125 kHz or 134 kHz frequency band. A single coil connected to the chip serves as the IC's power supply and bidirectional communication interface. The antenna and chip together form a transponder or tag. The on-chip 363-bit EEPROM (11 blocks with 33 bits each) is read and written blockwise from a base station (reader). Data are transmitted from the IDIC (uplink) using load modulation. This is achieved by damping the RF field with a resistive load between the two terminals, "Coil 1 and Coil 2". The IC receives and decodes serial base station commands (downlink), which are encoded as 100% amplitude modulated On-Off Keying (OOK) Pulse Interval Encoded (PIE) bit streams.

Features

These are the following features of read/write LF RFID IDIC 100 kHz to 150 kHz:

- Contactless Power Supply
- Contactless Read/Write Data Transmission
- Radio Frequency f_{RF} from 100 kHz to 150 kHz
- Basic mode or Extended mode
- Compatible with T5557, ATA5567
- Replacement for e5551/T5551 in Most Common Operation modes
- Configurable for ISO/IEC 11784/785 Compatibility
- Total 363 Bits EEPROM Memory: 11 Blocks (32 bits + 1 lock bit):
  - 7 × 32 bits EEPROM user memory, including 32-bit password memory
  - 2 × 32 bits for unique ID
  - 1 × 32-bit Option register in EEPROM to set up the analog front end:
    - Clock and gap detection level
    - Improved downlink timing
    - Clamp and modulation voltage
    - Soft modulation switching
    - Write damping like the T5557/ATA5567 or with resistor
    - Downlink protocol
  - 1 × 32-bit Configuration register in EEPROM to set up:
    - Data rate
      - RF/2 to RF/128, binary-selectable or
      - Fixed Basic mode rates
    - Modulation/coding
      - Bi-phase, Manchester, Frequency Shift Keying (FSK), Phase-Shift Keying (PSK), Non-Return-to-Zero (NRZ)
    - Other options:
      - Password mode
      - Max block feature
      - Direct Access mode
      - Sequence terminator(s)

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  - Blockwise write protection (lock bit)
  - Answer-On-Request (AOR) mode
  - Inverse data output
  - Disable Test mode access
  - Fast downlink (~6 kbps versus ~3 kbps)
  - OTP functionality
  - Init delay (~67 ms)

- High Q-Antenna Tolerance due to Build In Options
- Adaptable to Different Applications:
  - Access control
  - Animal ID
  - Waste management
- On-Chip Trimmed Antenna Capacitor:
  - 250 pF/330 pF (±3%)
- Pad Options:
  - ATA5577M1C
    - 100 µm × 100 µm for wire bonding or flip chip
  - ATA5577M2C
    - 200 µm × 400 µm for direct coil bonding

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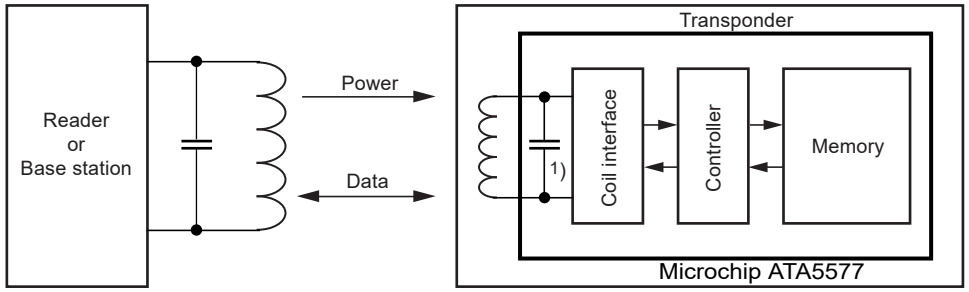
1. Compatibility

The ATA5577C is designed to be compatible with the T5557/ATA5567. The structure of the Configuration register is identical. The two modes, Basic mode and Extended mode, are also available. The ATA5577C is able to replace the e5551/T5551 in most common operation modes. In all applications, the correct functionality of the replacements must be evaluated and proved. For more details, refer to product-relevant application notes on the Microchip website.

2. System Block Diagram

The following figure illustrates the system block diagram of the RFID system.

Figure 2-1. RFID System Using ATA5577C Tag

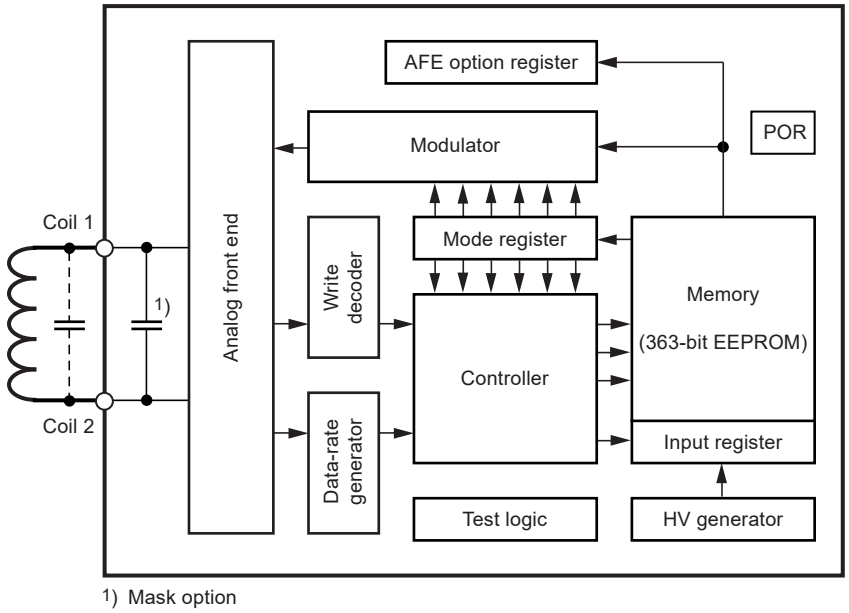


1) Mask option

3. ATA5577C – Functional Blocks

The following figure illustrates the functional block of ATA5577C.

Figure 3-1. Block Diagram



1) Mask option

3.1 Analog Front End (AFE)

The AFE includes all circuits that are directly connected to the coil terminals. It generates the IC's power supply and handles the bidirectional data communication with the reader.

The AFE consists of the following blocks:

- Rectifier to generate a DC supply voltage from the AC coil voltage
- Clock extractor
- Switchable load between "Coil 1 and Coil 2" for data transmission from the tag to the reader
- Field gap detector for data transmission from the base station to the tag
- Electrostatic Discharge (ESD) protection circuitry

3.2 AFE Option Register

The Option register maintains a readable shadow copy of the data held in the EEPROM page 1, block 3 (refer to Figure 3-2). This contains the AFE level and threshold settings, with enhanced downlink protocol selection with which the device is fine-tuned for perfect operation and all application environments. It is continually refreshed during Read mode operation and reloaded after every Power-on Reset event or Reset command. By default, the Option register is preprogrammed according to Table 8-3.

3.3 Data-Rate Generator

The data rate is binary programmable to operate at any even numbered data rate between RF/2 and RF/128, or to any of the fixed Basic mode data rates (RF/8, RF/16, RF/32, RF/40, RF/50, RF/64, RF/100 and RF/128).

3.4 Write Decoder

The write decoder detects the write gaps and verifies the validity of the data stream according to the e555x downlink protocol (pulse interval encoding).

3.5 HV Generator

This on-chip charge pump circuit generates the high voltage required to program the EEPROM.

3.6 DC Supply

Power is supplied to the IDIC externally via the two coil connections. The IC rectifies and regulates this RF source, and uses it to generate its supply voltage.

3.7 Power-on Reset (POR)

The POR circuit blocks the voltage supply to the IDIC until an acceptable voltage threshold is reached.

3.8 Clock Extraction

The clock extraction circuit uses the external RF signal as its internal clock source.

3.9 Controller

The control logic module executes the following functions:

- Loads Mode register with configuration data from EEPROM block 0 after power-on and during reading
- Loads Option register with the settings for the analog front end stored in EEPROM page 1, block 3 (refer to Figure 3-2) after power-on and during reading
- Controls all EEPROM memory read/write access and data protection
- Handles the downlink command decoding detecting protocol violations and error conditions

3.10 Mode Register

The Mode register maintains a readable shadow copy of the configuration data held in block 0 of the EEPROM. It is continually refreshed during Read mode and reloaded after every POR event or Reset command. On delivery, the Mode register is preprogrammed according to Table 8-3.

3.11 Modulator

The modulator encodes the serialized EEPROM data for transmission to a tag reader or base station.

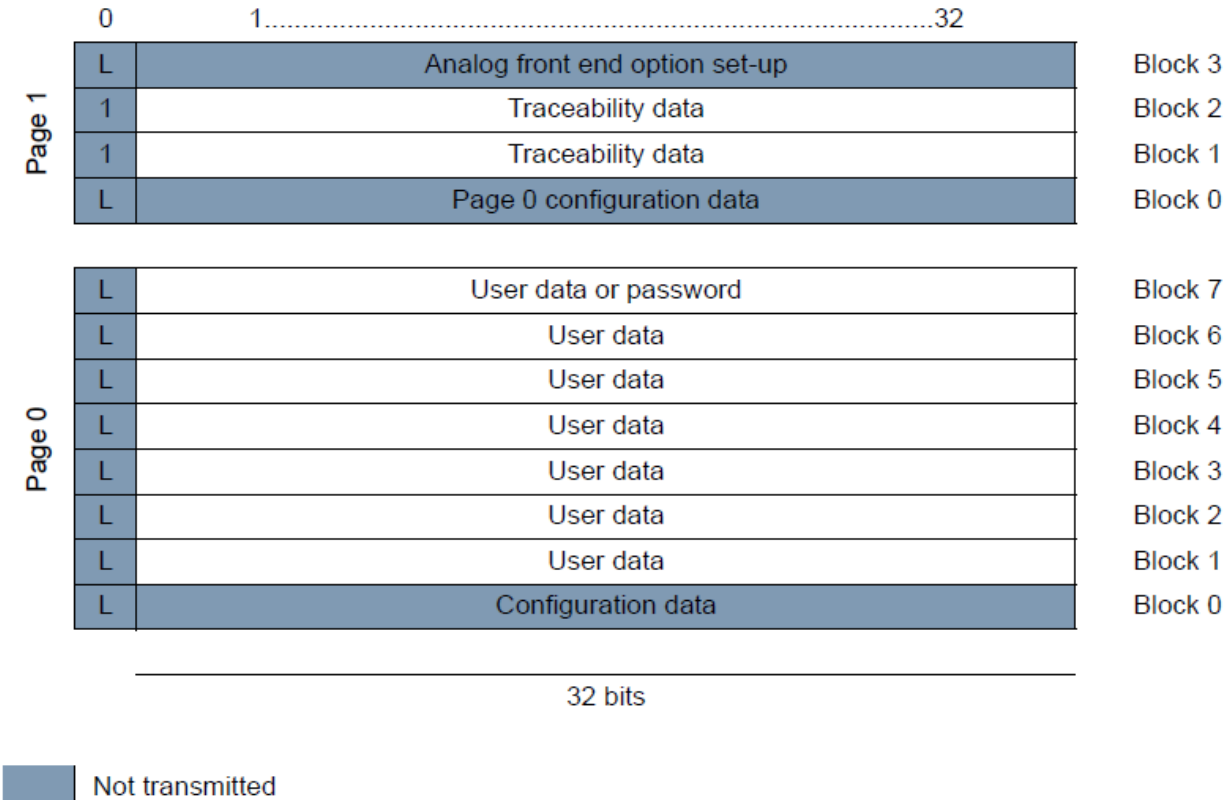
Several types of modulation are available:

- Manchester
- Bi-phase
- FSK
- PSK
- NRZ

3.12 Memory

The following figure shows the memory map of ATA5577C.

Figure 3-2. Memory Map



The memory is a 363-bit EEPROM, which is arranged in 11 blocks of 33 bits each. Each block includes a single lock bit, which is responsible for write-protecting the associated block. Programming takes place on a block basis, so a complete block (including lock bit) is programmed with a single command.

The memory is subdivided into two page areas:

- Page 0 contains eight blocks
- Page 1 contains three blocks

All 33 bits of a block, including the lock bit, are programmed simultaneously. Block 0 of page 0 (refer to Figure 3-2) contains the mode/configuration data, which are not transmitted during Regular-Read mode operations.

Addressing block 0 always affects block 0 of page 0 (refer to Figure 3-2) regardless of the page selector. Block 7 of page 0 (refer to Figure 3-2) may be used as a protection password. Block 3 of page 1 (refer to Figure 3-2) contains the AFE Option register, which is also not transmitted during Regular-Read mode operation. Bit '0' of every block is the lock bit for that block.

Once locked, the block (including the lock bit itself) is not reprogrammable via the RF field. Blocks 1 and 2 of page 1 (refer to Figure 3-2) contain traceability data and are transmitted with the modulation parameters defined in the Configuration register after the opcode '11' is issued by the reader (see Figure 4-15 and Figure 4-16). The traceability data blocks are programmed and locked by ATA5577C.

3.13 Traceability Data Structure/Unique ID

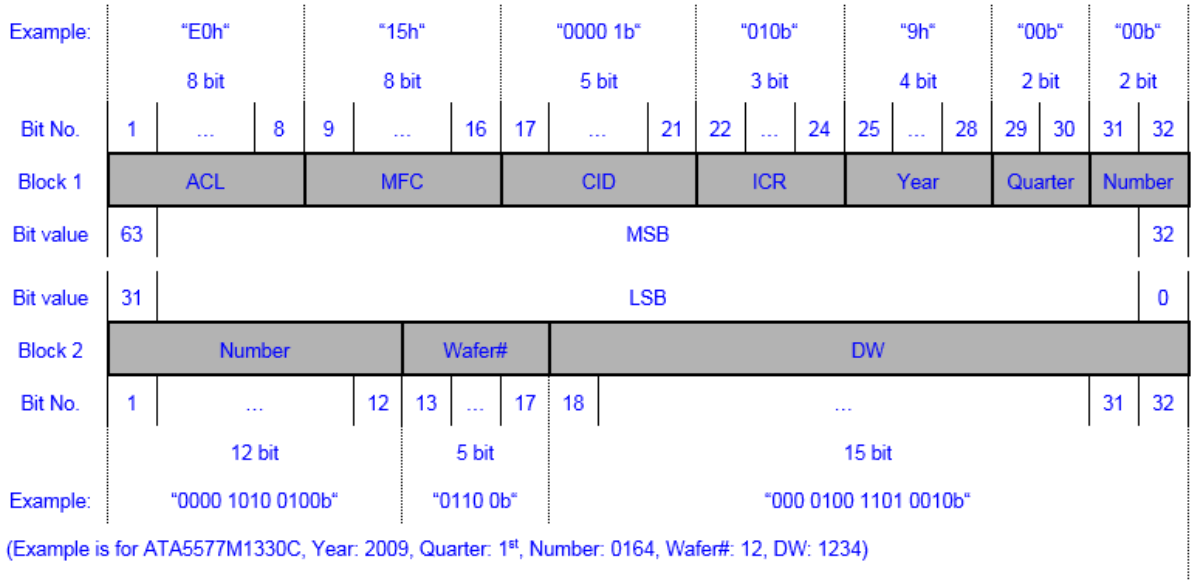
Blocks 1 and 2 of page 1 (refer to Figure 3-2) contain the traceability data and are programmed and locked by ATA5577C during production testing [(1)]. The Most Significant Byte (MSB) of block 1 is fixed to E0h, the Allocation Class (ACL), as defined in ISO/IEC 15963-1. The second byte is, therefore, defined in ISO/IEC 7816-6 as the

manufacturer ID (15h). The following five bits indicate chip ID (CID – '00001b' for ATA5577M1 and '00010b' for ATA5577M2), and the next bits (IC revision, ICR) are used by Microchip for the IC and/or foundry version of the ATA5577C. The lower 40 bits of data encode Microchip's traceability information and conform to a unique numbering system (unique ID). These 40 data bits contain the lot ID (year, quarter, number), wafer number (Wafer#) and die number of the wafer (DW).

Note:

1. This is only valid for sawn wafer on foil delivery.

Figure 3-3. ATA5577C Traceability Data Structure



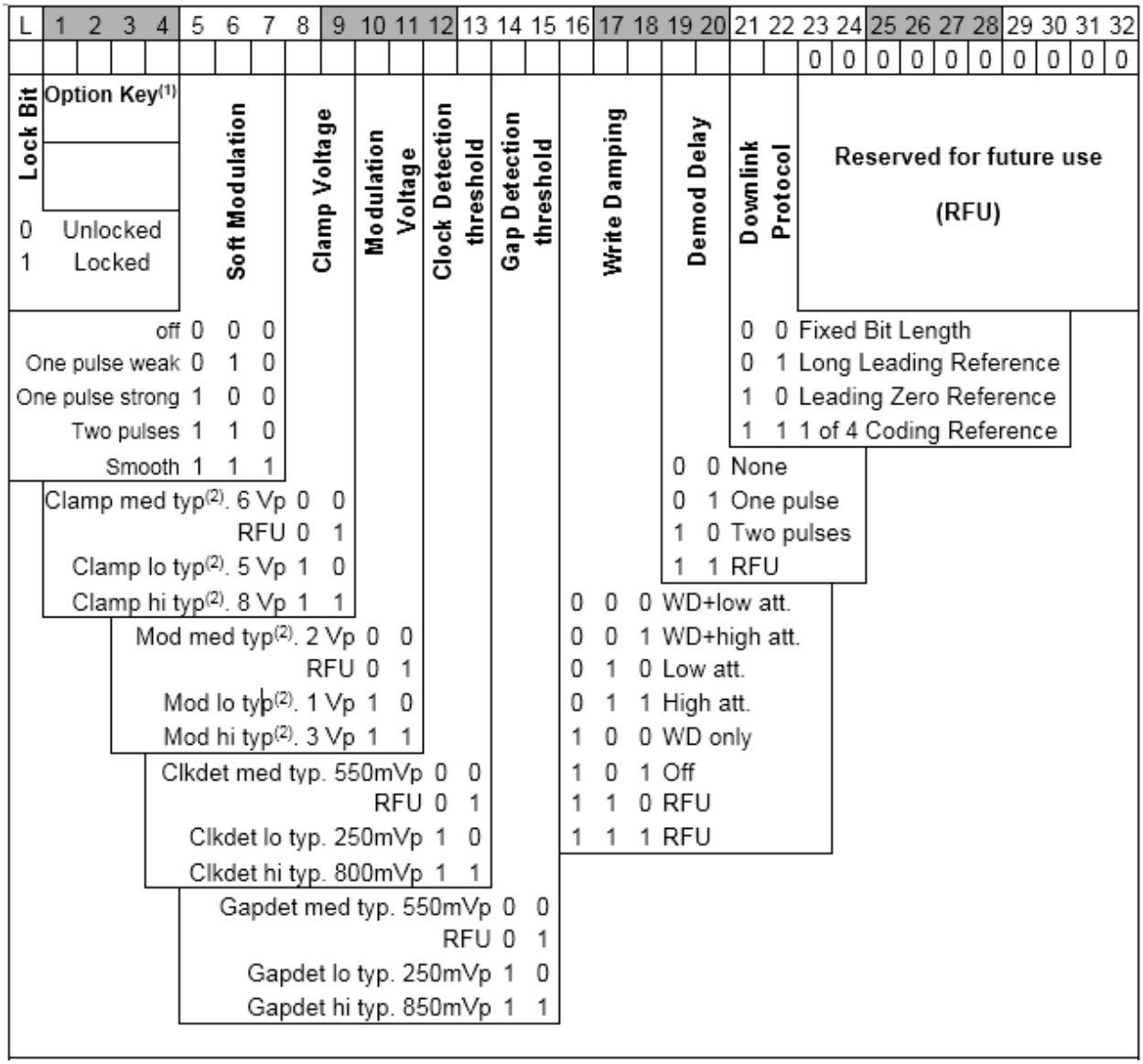
- ACL – Allocation Class as defined in ISO/IEC 15963-1 = E0h
- MFC – Atmel Corporation Manufacturer Code as defined in ISO/IEC 7816-6 = 15h
- CID – 5-bit Chip ID for identification of the different products: '00001b' for ATA5577M1 and '00010b' for ATA5577M2
- ICR – 3-bit IC Revision to identify foundry and/or revision of IC
- Year – 1-digit BCD encoded year of manufacturing
- Quarter – 2 bits for quarter of manufacturing
- Number – 14 bits of consecutive number
- Wafer# – 5 bits for wafer number
- DW – 15 bits designating sequential die number on wafer

4. Operating the ATA5577C

4.1 Configuring the ATA5577C

The following figures illustrates the configuration of the ATA5577C.

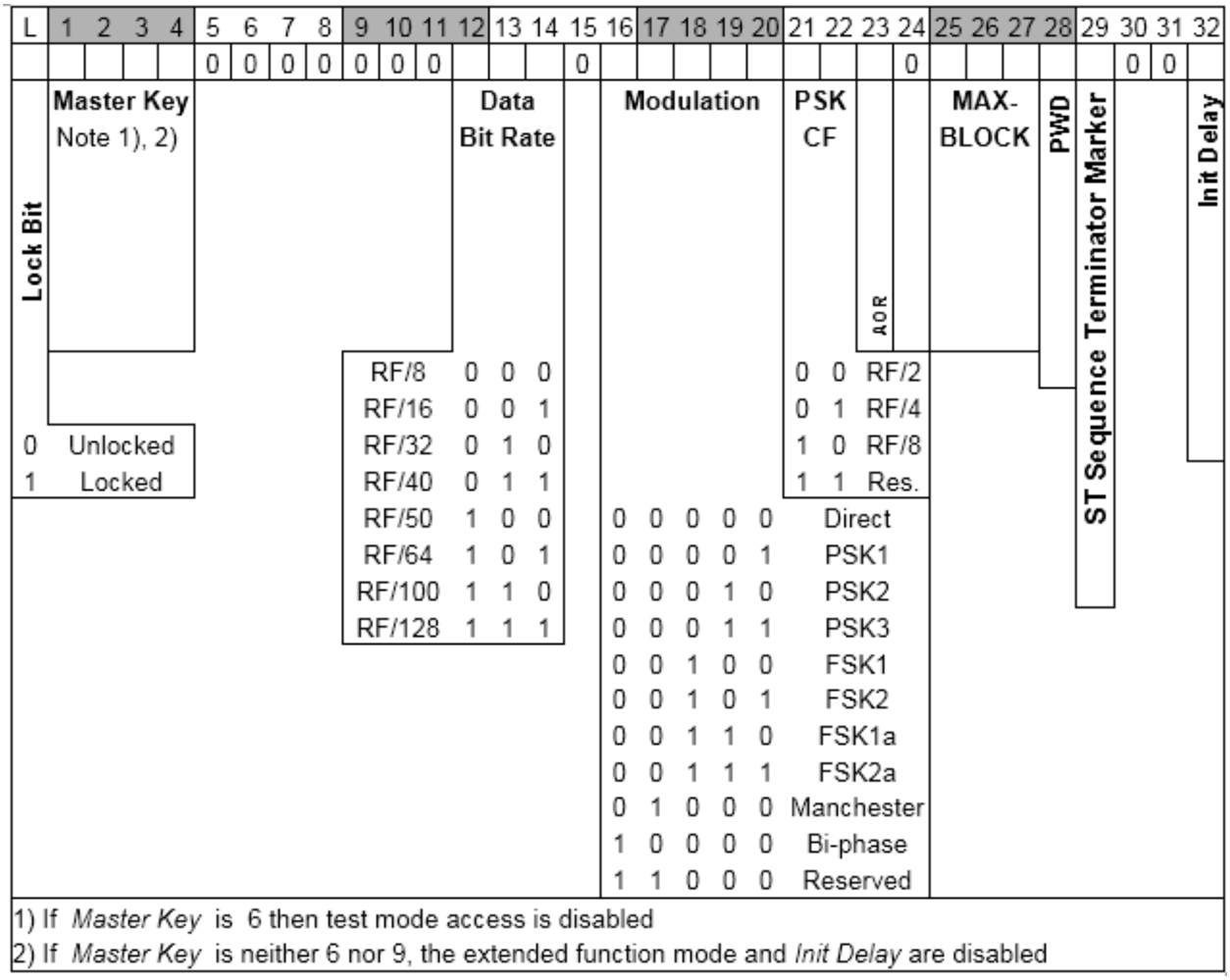
Figure 4-1. Block 3 Page 1 – Analog Front-End Option Setup 1



Note:

1. If the option key is 6 or 9, the front-end options are activated. For all other values, they take on the default state (all '0's). If the option key is 6, then the complete page 1 (that is, Option register and traceability data) cannot be overwritten by any test write command. This means that if the lock bits of the three blocks of page 1 are set and the option key is 6, then all of page 1's blocks (refer to Figure 3-2) are locked against change.
2. Weak field condition.

Figure 4-2. Block 0 Page 0 – Configuration Mapping in Basic Mode



1) If *Master Key* is 6 then test mode access is disabled
2) If *Master Key* is neither 6 nor 9, the extended function mode and *Init Delay* are disabled

Figure 4-3. Block 0 Page 0 – Configuration Mapping in Extended Mode (X-mode)

L	1 2 3 4	5 6 7 8	9 10 11 12	13 14 15 16	17 18 19 20	21 22 23 24	25 26 27 28	29 30 31 32
		0 0 0 0		1				
Lock Bit	Master Key Note 1, 2		n5 n4 n3 n2 n1 n0 Data Bit Rate RF/(2n+2)	X-Mode	Modulation	PSK-CF; AOR; OTP	MAX-BLOCK	PWD	Seq. Start; Fast Downlink; Inverse Data; Init-Delay

Lock Bit: 0 Unlocked; 1 Locked

Modulation					
direct	0	0	0	0	0
PSK1	0	0	0	0	1
PSK2	0	0	0	1	0
PSK3	0	0	0	1	1
FSK1	0	0	1	0	0
FSK2	0	0	1	0	1
Manchester	0	1	0	0	0
Biphase	1	0	0	0	0
Differential Biphase	1	1	0	0	0

PSK-CF		AOR
0	0	RF/2
0	1	RF/4
1	0	RF/8
1	1	Res.

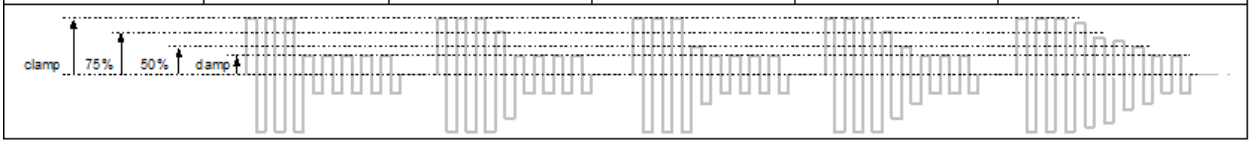
1) If Master Key is 6 and bit 15 is set, then test mode access is disabled and extended mode is active
2) If Master Key is 9 and bit 15 is set, then extended mode is enabled

4.2 Soft Modulation Switching

Modulation switching results in abrupt rise of the modulation signal at the beginning of each modulation. This could lead to clock losses, and therefore, timing violations, especially in applications with high-quality antennas. To prevent this, several soft modulation settings can be chosen for a soft transition into the modulation state. Soft modulation must be used in combination with modulation schemes and data rates which do not involve high-frequency modulation changes.

Figure 4-4. Soft Modulation Switching Scheme

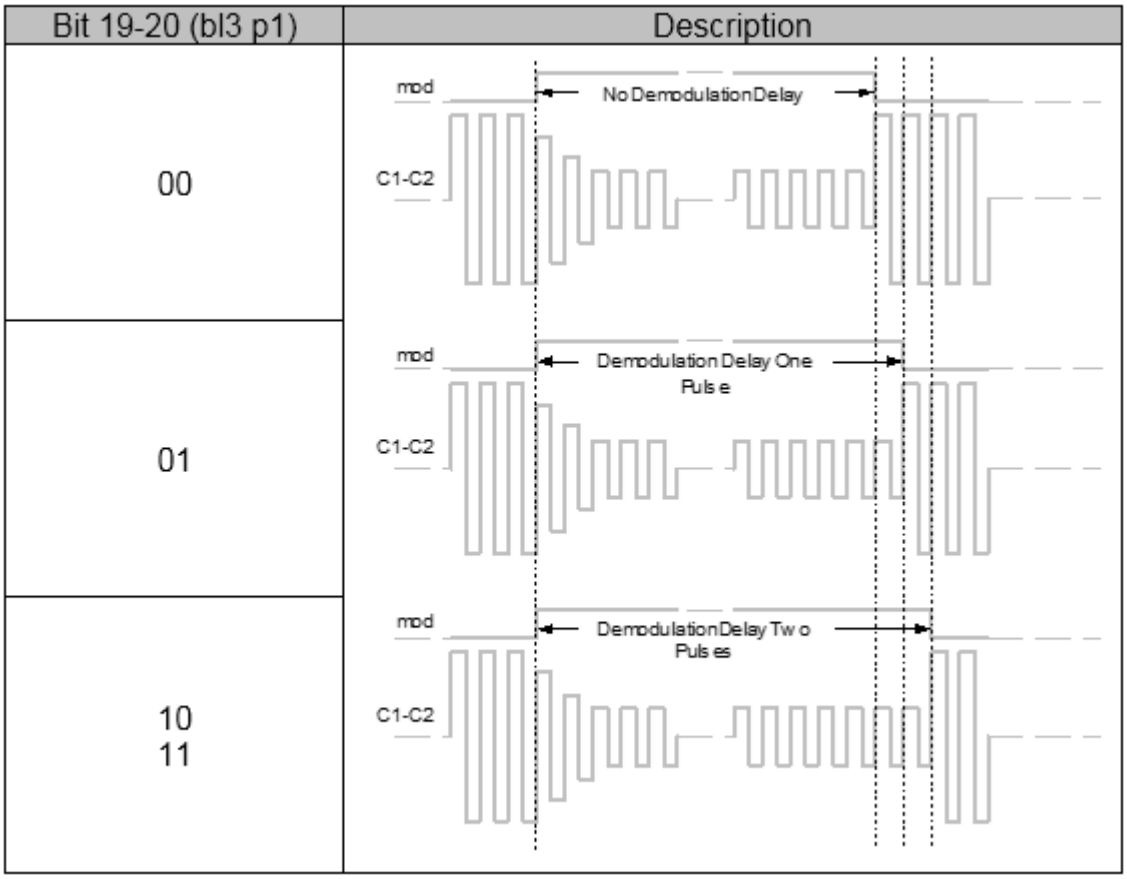
Bit 5-7 (bl3 p1)	000	010	100	110	111
Description	No soft modulation	One pulse weak	One pulse strong	Two pulses	Smooth



4.3 Demodulation Delay

Soft modulation causes imbalance in modulated and unmodulated phases. Depending on the soft modulation setting, the unmodulated phase is longer than the modulated phase. To balance out this mismatch, the switch point from the modulated to the unmodulated phase is delayed for one or two pulses. These delays and soft modulation switching must be used in combination with modulation schemes and data rates which do not involve high-frequency modulation changes.

Figure 4-5. Demodulation Delay Scheme



4.4 Write Damping

Reader-to-tag communication is initialized by sending a start gap from the reader station. To ease gap detection with respect to detecting subsequent field gaps reliably, receive damping and low attenuation are activated by default. A higher attenuation factor is switched on to fasten the relaxation time, especially in combination with high-quality coils. Using antenna coils with a low Q-factor might make it feasible to switch off the write damping. This results in better energy balance, and therefore, improved write distance.

4.5 Initialization and Init Delay

The POR circuit remains active until an adequate voltage threshold is reached. This, in turn, triggers the default initialization delay sequence. During this configuration period, for 192 field clocks, the ATA5577C is initialized with the configuration data stored in EEPROM block 0 (refer to Figure 3-2) and with the options stored in block 3, page 1 (refer to Figure 3-2).

Tag modulation in Regular-Read mode is observed for 3 ms after entering the RF field. If the init delay bit is set, the ATA5577C variant with damping during initialization remains in a permanent damping state for t ~ 69 ms at f = 125 kHz.

The ATA5577C variant without damping starts modulation after t ~ 69 ms without damping:

- Init delay = 0: $T_{INIT} = 192 \times T_C + T_{POR} \sim 3$ ms; $T_C = 8$ µs at f = 125 kHz (T_{POR} denotes delay for POR and depends on environmental conditions)
- Init delay = 1: $T_{INIT} = (192 + 8192) \times T_C + T_{POR} \sim 69$ ms

Any field gap occurring during this initialization phase, restarts the complete sequence. After this initialization time, the ATA5577C enters Regular-Read mode, and modulation starts automatically using the parameters defined in the Configuration register.

4.6 Modulator in Basic Mode

The modulator consists of data encoders for the following types of modulation in Basic mode:

Table 4-1. Types of Modulation in Basic Mode

Mode	Direct Data Output		
FSK1a(1)	FSK/8 – FSK/5	0 = RF/8	1 = RF/5
FSK2a(1)	FSK/8 – FSK/10	0 = RF/8	1 = RF/10
FSK1(1)	FSK/5 – FSK/8	0 = RF/5	1 = RF/8
FSK2(1)	FSK/10 – FSK/8	0 = RF/10	1 = RF/8
PSK1(2)	Phase change when input changes		
PSK2(2)	Phase change on bit clock if input high		
PSK3(2)	Phase change on rising edge of input		
Manchester	0 = falling edge, 1 = rising edge		
Bi-phase	1 = creates an additional mid-bit change		
NRZ	1 = damping on, 0 = damping off		

Note:

1. A common multiple of bit rate and FSK frequencies is recommended.
2. In PSK mode, the selected data rate must be an integer multiple of the PSK sub-carrier frequency.

4.7 Maxblock Setting

After entering Regular-Read mode, the ATA5577C transmits the data content starting with block 1. The MAXBLK setting defines how many data blocks are transmitted.

4.8 Password Mode

When Password mode is active (PWD = 1), the first 32 bits after the opcode are regarded as the password. They are compared bit-by-bit with the contents of block 7, starting at bit 1. If the comparison fails, the ATA5577C must not program the memory. Instead, it restarts in Regular-Read mode once the command transmission is finished.

Note: In Password mode, MAXBLK must be set to a value lower than seven to prevent the password from being transmitted by the ATA5577C.

Each transmission of the direct access command (2 opcode bits, 32-bit password, '0' bit plus 3 address bits = 38 bits) needs about 18 ms. Testing all possible combinations (about 4.3 billion) can take about two years.

4.9 Answer-On-Request (AOR) Mode

When the AOR bit in the Configuration register is set, the ATA5577C does not start modulation in the Regular-Read mode after loading configuration block 0. The tag waits for a valid AOR data stream (wake-up command) from the reader before modulation is enabled. The wake-up command consists of the opcode ('10' or '11') followed by a valid password. The selected tag remains active until the RF field is turned off or a new command with a different password is transmitted, which may address another tag in the RF field.

Table 4-2. ATA5577C – Modes of Operation

PWD	AOR	Behavior of Tag after Reset Command or POR	Deactivate Function
1	1	AOR mode: • Modulation starts after wake-up with a matching password • Programming needs valid password	Command with non-matching password deactivates the selected tag
1	0	Password mode: • Modulation in Regular-Read mode starts after Reset • Programming and direct access needs valid password	—
0	—	Normal mode: • Modulation in Regular-Read mode starts after Reset • Programming and direct access without password	—

Figure 4-6. AOR Mode, Fixed Bit Length Protocol Example

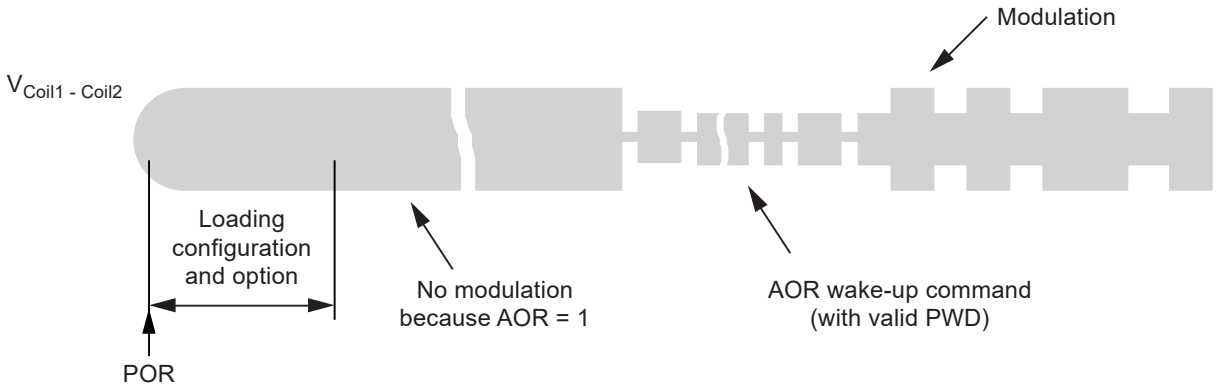
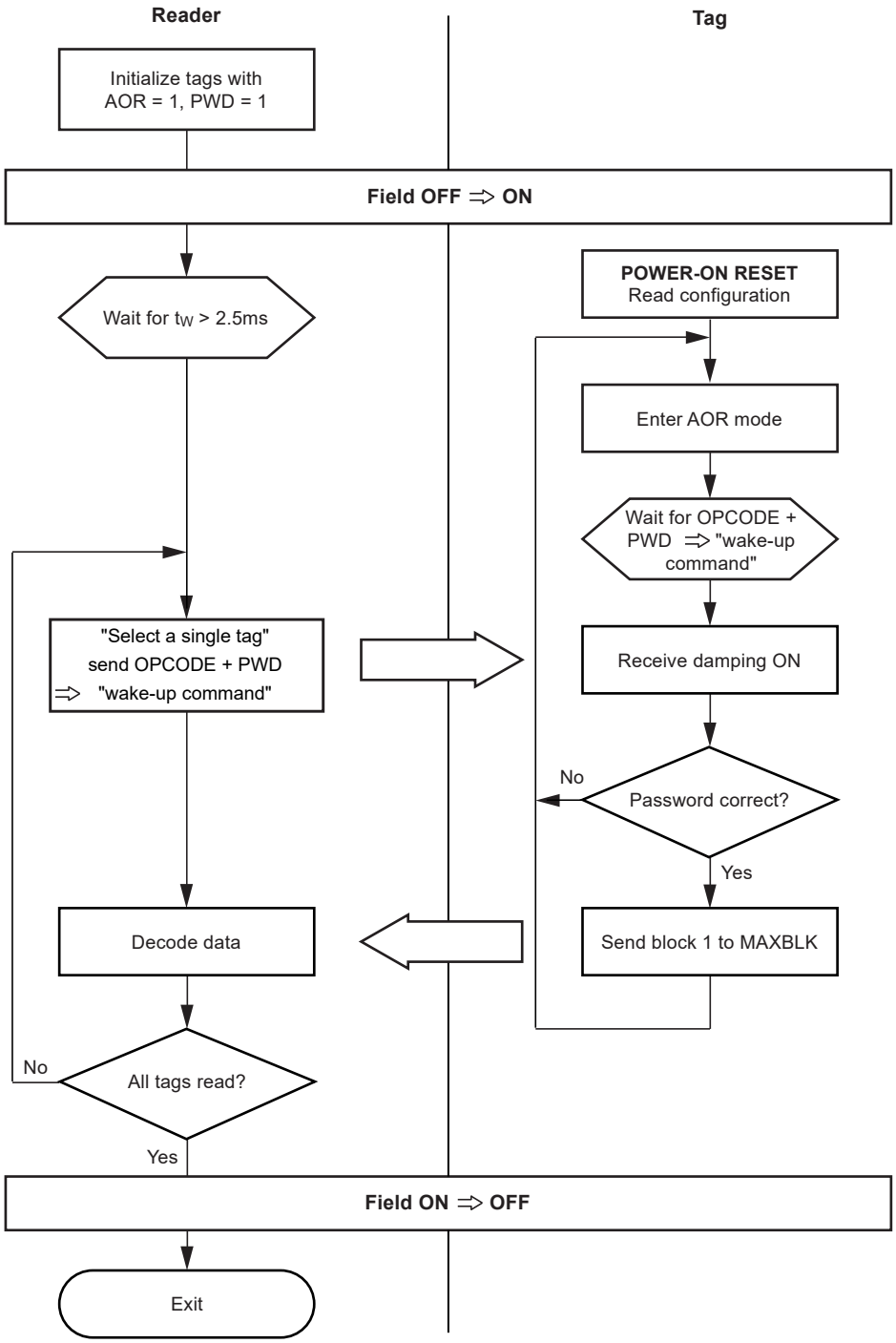


Figure 4-7. Anti-Collision Procedure Using AOR Mode



4.10 ATA5577C in Extended Mode (X-mode)

In general, setting of the master key (bits 1 to 4) of block 0 to the value 6 or 9, together with the X-mode bit, enables the Extended mode functions, such as the binary bit rate generator, OTP functionality, fast downlink, inverse data output and sequence start marker.

- Master key = 9:
  - Test mode access and Extended mode are both enabled

- Master key = 6:
  - Any Test mode access is denied but the Extended mode is still enabled

Any other master key setting prevents activation of the ATA5577C Extended mode options, even when the X-mode bit is set.

4.10.1 Modulator in Extended Mode (X-mode)

The following table provides the details of the modulator in Extended mode (X-mode).

Table 4-3. ATA5577C Types of Modulation in Extended Mode (X-mode)

Mode	Direct Data Output Encoding		Inverse Data Output Encoding		
FSK1[1]	FSK/5 – FSK/8	0 = RF/5; 1 = RF/8	FSK/8 – FSK/5	0 = RF/8; 1 = RF/5	(= FSK1a)
FSK2[1]	FSK/10 – FSK/8	0 = RF/10; 1 = RF/8	FSK/8 – FSK/10	0 = RF/8; 1 = RF/10	(= FSK2a)
PSK1[2]	Phase change when input changes		Phase change when input changes		
PSK2[2]	Phase change on bit clock if input high		Phase change on bit clock if input low		
PSK3[2]	Phase change on rising edge of input		Phase change on falling edge of input		
Manchester	0 = falling edge, 1 = rising edge mid-bit		1 = falling edge, 0 = rising edge mid-bit		
Bi-phase	1 creates an additional mid-bit change		0 creates an additional mid-bit change		
Differential bi-phase	0 creates an additional mid-bit change		1 creates an additional mid-bit change		
NRZ	1 = damping on, 0 = damping off		0 = damping on, 1 = damping off		

Note:

1. A common multiple of bit rate and FSK frequencies is recommended.
2. In PSK mode, the selected data rate must be an integer multiple of the PSK sub-carrier frequency.

4.10.2 Binary Bit Rate Generator

In Extended mode, the data rate is binary-programmable to operate at any even numbered data rate between RF/2 and RF/128 as given in the formula: *Data Rate = RF/(2n + 2)*.

4.10.3 OTP Functionality

If the OTP bit is set to '1', all memory blocks are write-protected and behave as if all lock bits are set to '1'. If, in addition, the master key is set to 6, the ATA5577C mode of operation is locked forever (One-Time-Programmable functionality). If the master key is set to 9, Test mode access allows reconfiguration of the tag.

4.10.4 Fast Downlink

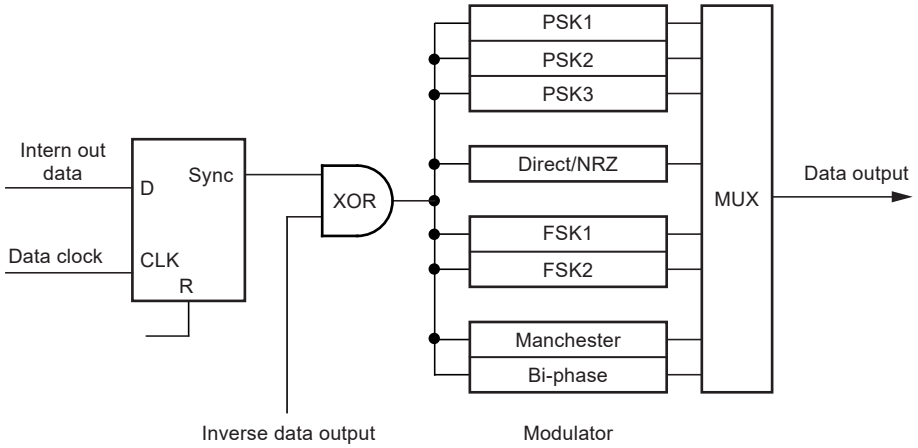
In the optional Fast Downlink mode, the time between two gaps is reduced. In the Fixed Bit Length Protocol mode, there are nominally 12 field clocks for a '0' and 28 field clocks for a '1'. When there is no gap for more than 32 field clocks after a previous gap, the ATA5577C in the Fixed Bit Length Protocol mode will exit the Downlink mode (refer to Table 4-5).

The Fast Downlink mode timings for the long leading reference protocol are shown in Table 4-6, for the leading zero reference protocol in Table 4-7 and for the 1-of-4 coding protocol in Table 4-8.

4.10.5 Inverse Data Output

In Extended mode (X-mode), the ATA5577C supports an inverse data output option. If inverse data are enabled, the modulator shown in the following figure works on inverted data (see Table 4-3). This function is supported for all basic types of encoding.

Figure 4-8. Data Encoder for Inverse Data Output



4.11 Tag-to-Reader Communication

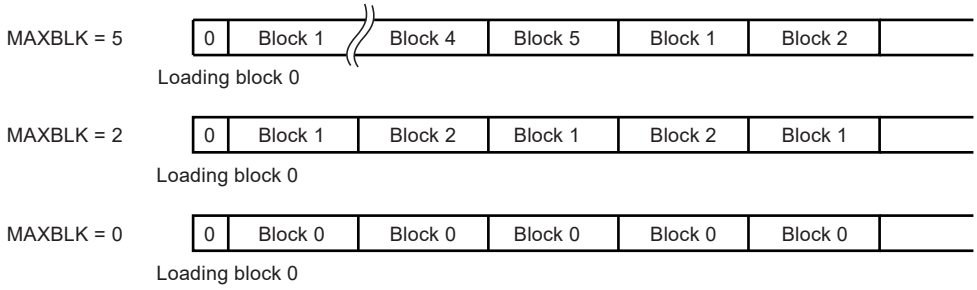
During read operation (Uplink mode), the data stored within the EEPROM are cycled, and the “Coil 1 and Coil 2” terminals are load modulated. This resistive load modulation is detected at the reader device.

4.11.1 Regular-Read Mode

In Regular-Read mode, data from the memory are transmitted serially, starting with block 1, bit 1, up to the last block (for example, 7), bit 32. The last block to be read is defined by the mode parameter field MAXBLK in EEPROM block 0. When the data block addressed by MAXBLK is read, data transmission restarts with block 1, bit 1.

The user may limit the cyclic data stream in Regular-Read mode by setting MAXBLK between 0 and 7 (representing each of the eight data blocks). If set to 7, blocks 1 through 7 are read. If set to 1, only block 1 is transmitted continuously. If set to 0, the contents of the configuration block (normally not transmitted) are read. In the case of MAXBLK = 0 or 1, Regular-Read mode cannot be distinguished from Block-Read mode.

Figure 4-9. Examples of Different MAXBLK Settings



Every time the ATA5577C enters Regular or Block-Read mode, the first bit transmitted is a logical ‘0’. The data stream starts with block 1, bit 1, continues through MAXBLK bit 32, and if in Regular-Read mode, cycles continuously.

Note: This behavior is different from that of the original e555x and helps to decode PSK-modulated data.

4.11.2 Block-Read Mode

With the direct access command, only the addressed block is read repetitively. This mode is called Block-Read mode. Direct access is entered by transmitting the page access opcode (‘10’ or ‘11’), a single 0 and the requested 3-bit block address when the tag is in Normal mode.

In Password mode (PWD bit set), direct access to a single block needs the valid 32-bit password to be transmitted after the page access opcode, followed by a 0 and the 3-bit block address. If the transmitted password does not match the contents of block 7, the ATA5577C tag returns to Regular-Read mode.

Note:

- A direct access to block 0 of page 1 reads the configuration data of block 0, page 0
- A direct access to block 4 to 7 of page 1 reads all data bits as zero

4.11.3 Sequence Terminator (Basic Mode)

The Sequence Terminator (ST) is a special damping pattern, which is inserted in front of the first block and can be used to synchronize the reader. This sequence terminator is recommended only for FSK and Manchester coding. This Basic mode sequence terminator consists of four bit periods. During the first and third bit period, the data value is 1. During the second and fourth bit periods, modulation is switched off (using Manchester encoding, switched on).

Biphase modulated data blocks need fixed leading and trailing bits, in combination with the sequence terminator, to be reliably identified. The sequence terminator may be individually enabled by setting mode bit 29 (ST = `1`) in Basic mode (X-mode = `0`).

In the Regular-Read mode, the sequence terminator is inserted at the start of each MAXBLK-limited read data stream.

In Block-Read mode, after any block write or direct access command, or if MAXBLK was set to '`1`', the sequence terminator is inserted before the transmission of the selected block.

This behavior is different from that of previous ICs (e5551/T5551, T5554). For further details, refer to the relevant application notes.

Figure 4-10. Read Data Stream with Sequence Terminator

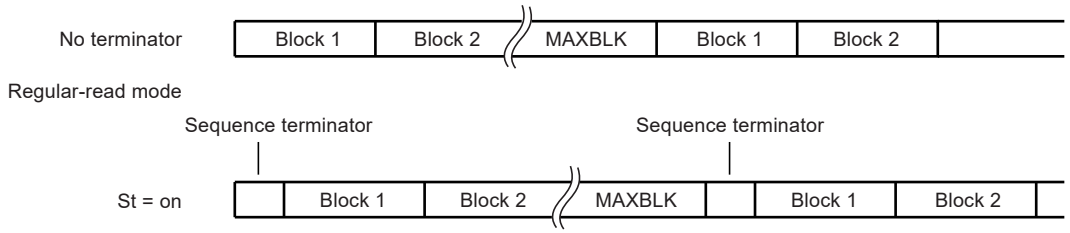
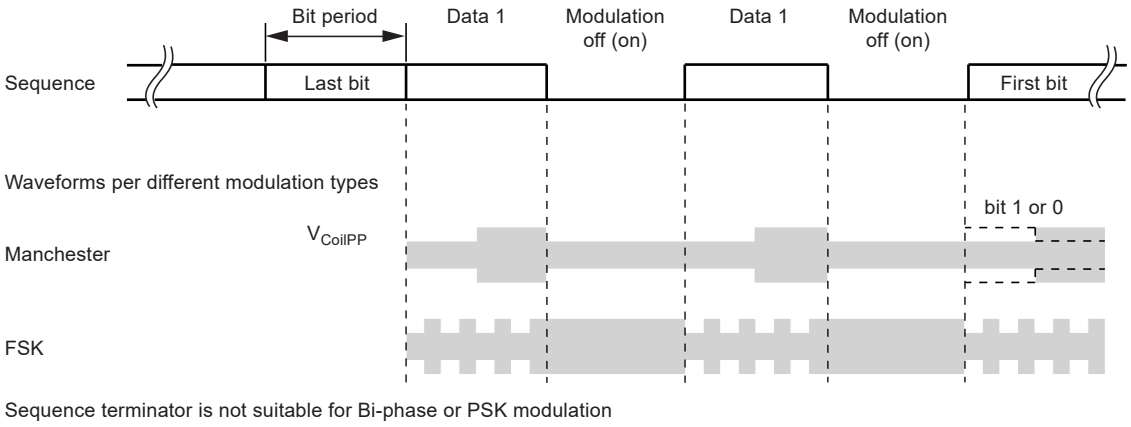


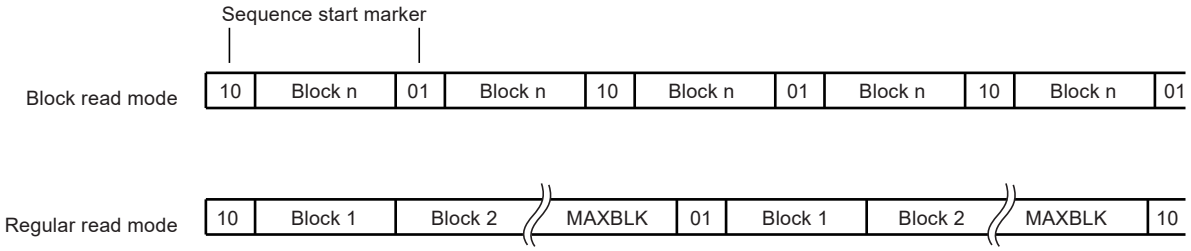
Figure 4-11. Basic Mode Sequence Terminator Waveforms



4.11.4 Sequence Start Marker (X-mode)

The ATA5577C sequence start marker is a special damping pattern in Extended mode which may be used to synchronize the reader. The sequence start marker consists of two bits ('`01`' or '`10`'), which are inserted as a header before the first block to be transmitted, if in Extended mode, bit 29 is set. At the start of a new block sequence, the value of the two bits is inverted.

Figure 4-12. ATA5577C Sequence Start Marker in Extended Mode



4.12 Reader to Tag Communication

Data are transmitted to the tag by interrupting the RF field with short field gaps (On-Off Keying) in accordance with the T5557/ATA5567 write method (Downlink mode). The duration of these field gaps is, for example, 100 µs. The time between two gaps encodes the 0/1 information to be transmitted (pulse interval encoding). There are four different downlink protocols available, which are selectable via bit 21 and bit 22 in the Option register block 3, page 1 (see Figure 4-1).

Choosing the default downlink protocol (fixed bit length protocol), the time between two gaps is nominally 24 field clocks for a 0 and 56 field clocks for a 1. When there is no gap for more than 64 field clocks after a previous gap, the ATA5577C exits the Downlink mode. The tag starts with the command execution if the correct number of bits were received. If a failure is detected, the ATA5577C does not continue and enters Regular-Read mode.

Improved downlink performance could be achieved by choosing self-calibrating downlink protocols.

The ATA5577C offers three different possibilities to achieve better performance using self-calibrating downlink protocols:

- Long leading reference:
  - Fully forward and backward compatible with former tags and readers.
- Leading zero:
  - A reader sends a leading zero in front of the downlink bit stream. This leading zero serves as a reference for the following zero and one bits.
- 1-of-4 coding:
  - Compact downlink protocol with optimized energy balance.

4.12.1 Start Gap

The initial gap is referred to as the start gap. This triggers the reader-to-tag communication. In the Option register (block 3, page 1), several settings are chosen to ease gap detection during this mode of operation; for example, the receive damping is activated (see Figure 4-1). The start gap may need to be longer than subsequent gaps, so-called write gaps, in order to be detected reliably.

A start gap is accepted at any time after the Mode register is loaded (≥ 3 ms). A single gap does not change the previously selected page (by a previous opcode '10' or '11').

Figure 4-13. Start of Reader-to-Tag Communication

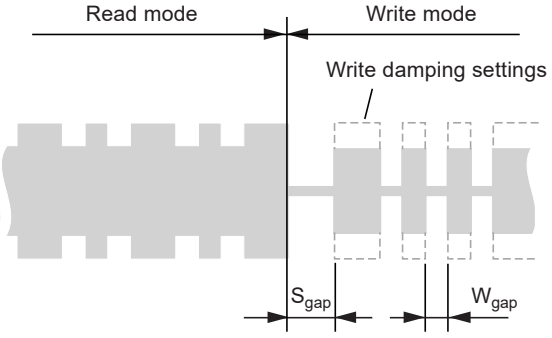


Table 4-4. Gap Scheme

Parameters	Remark	Symbol	Min.	Max.	Unit
Start gap	—	S_{gap}	8	50	T_C
Write gap	Normal Downlink mode	W_{gap}	8	20	T_C

Note: All absolute times assume $T_C = 1/f_C = 8$ µs ($f_C = 125$ kHz).

4.12.2 Downlink Data Protocols

The ATA5577C expects to receive a dual bit opcode as a part of a reader command sequence.

There are three valid opcodes:

1. The opcode '10' precedes all downlink operations for page 0.
2. The opcode '11' precedes all downlink operations for page 1. Performing a direct access command on block 0 always provides block 0, page 0 independently of the page selector (see Figure 3-2).
3. The Reset opcode '00' initiates an initialization cycle.

The fourth opcode '01' precedes all Test mode write operations. Any Test mode access is ignored after master key (bits 1 to 4) in block 0 is set to 6. Any further modifications of the master key are prohibited by setting the lock bit of block 0 or the OTP bit.

Rules to follow for the downlink:

- Standard write needs the opcode, the lock bit, 32 data bits and the 3-bit address (38 bits total)
- Protected write (PWD bit set) requires a valid 32-bit password between the opcode, and the data and address bits. Protected write (PWD bit set), in conjunction with the leading-zero-reference protocol or with the 1-of-4 coding protocol, requires two padding zero bits between the opcode and the password (see Figure 4-22). This ensures the uniqueness of the direct access with the password and the standard write command (see Table 5-1)
- For the AOR wake-up command, an opcode and a valid password are necessary to select and activate a specific tag

Note: The data bits are read in the same order as written.

If the transmitted command sequence is invalid, the ATA5577C enters Regular-Read mode with the previously selected page (by previous opcode '10' or '11').

Figure 4-14. Complete Writing Sequence with Fixed Bit Length Protocol

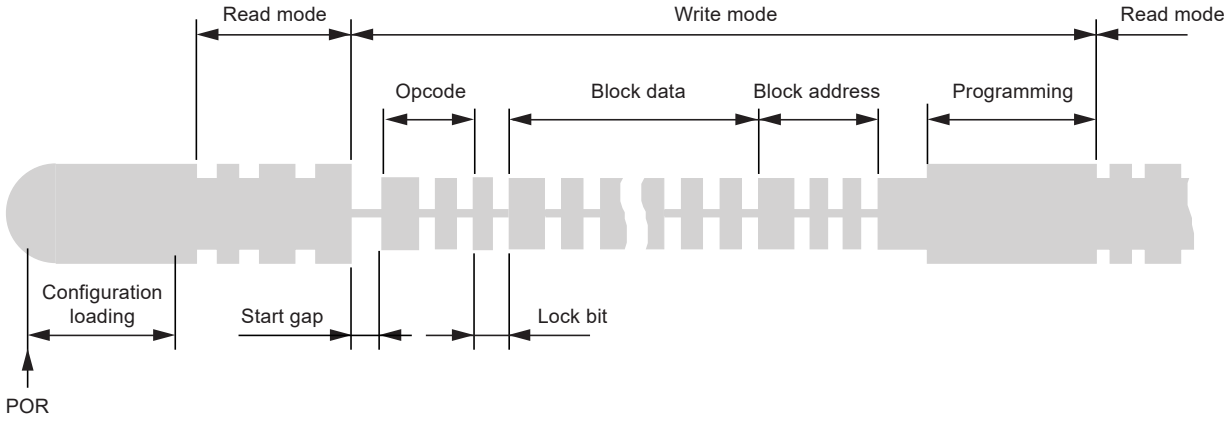


Figure 4-15. ATA5577C Command Formats Fixed Bit Length Protocol and Long Leading Reference Protocol

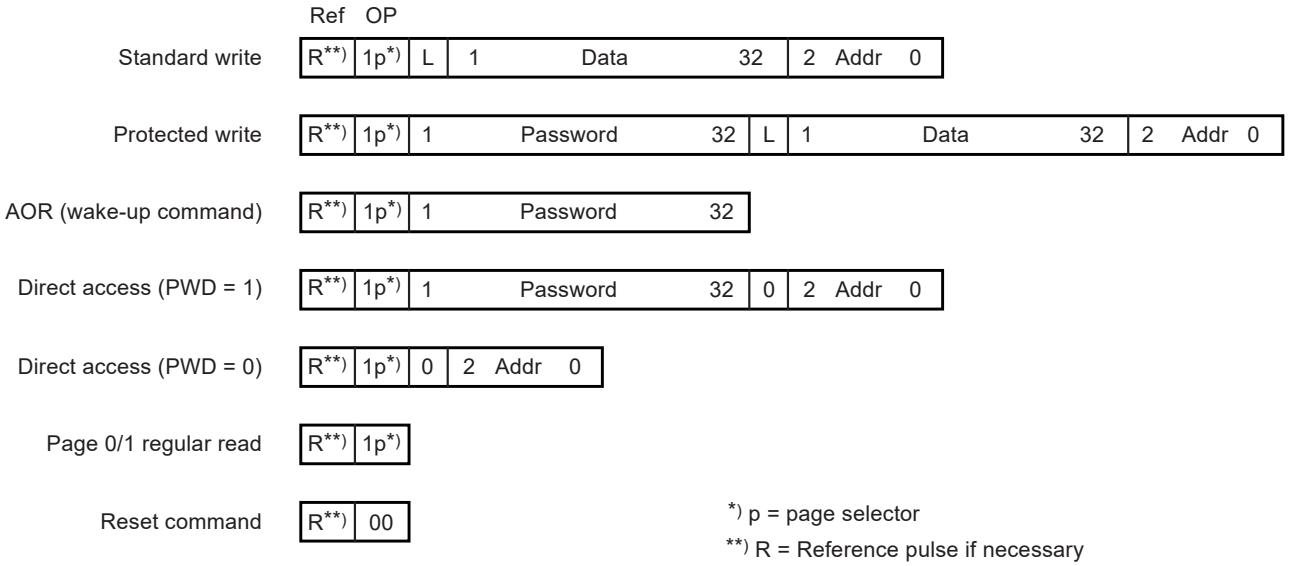
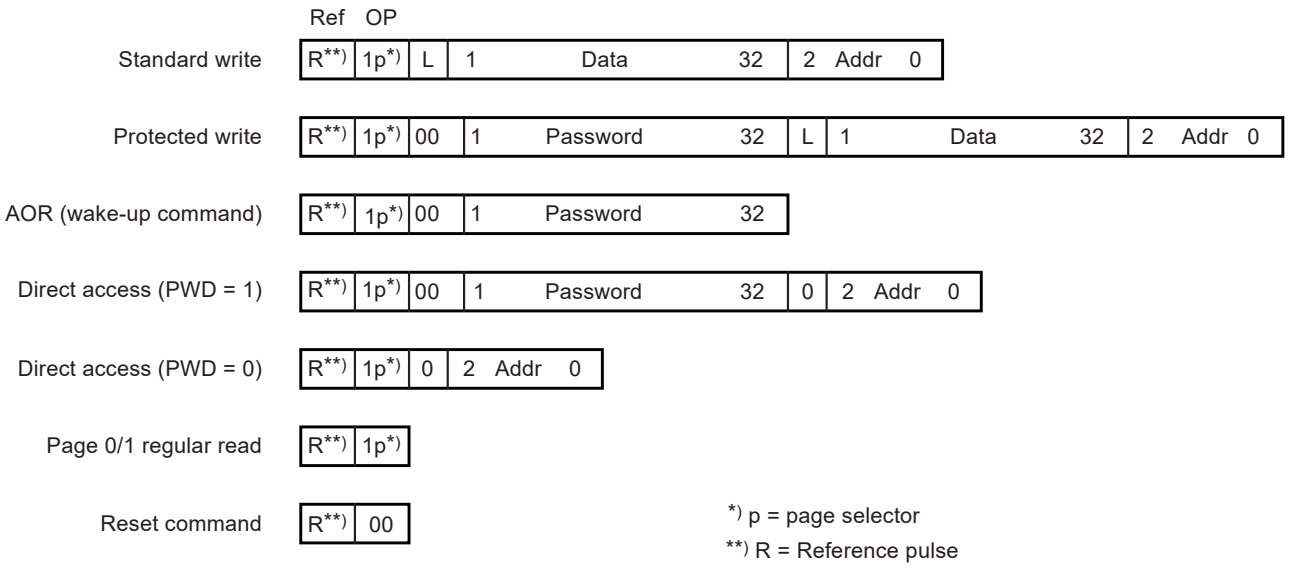


Figure 4-16. ATA5577C Command Formats Leading Zero Reference Protocol and 1-of-4 Coding Protocol



4.12.3 Fixed Bit Length Protocol

In the fixed bit length protocol, the time between two gaps is nominally 24 field clocks for a 0 and 56 field clocks for a 1. When there is no gap for more than 64 field clocks after a previous gap, the ATA5577C exits the Downlink mode. This protocol is compatible with the T5557/ATA5567 transponder.

Table 4-5. Downlink Data Coding Scheme with Fixed Bit Length Protocol

Parameter	Remark	Symbol	Normal Downlink			Fast Downlink			
			Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
Start gap	—	S_{gap}	8	15	50	8	15	50	T_C
Write gap	—	W_{gap}	8	10	20	8	10	20	T_C

.....continued

Parameter	Remark	Symbol	Normal Downlink			Fast Downlink			
			Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
Write data coding (gap separation)	0 data	d0	16	24	32	8	12	16	T_C
	1 data	d1	48	56	64	24	28	32	T_C

Note: All absolute times assume: $T_C = 1/f_C = 8\ \mu s$ ($f_C = 125$ kHz).

Figure 4-17. Fixed Bit Length Protocol

4.12.4 Long Leading Reference Protocol

To achieve better downlink performance, an enhanced ATA5577C reader places a reference pulse in front of the opcode. This reference pulse is used as a timing reference for all following data, thus providing an auto-adjustment for varying environmental conditions. The long leading reference protocol allows full compatibility and coexistence of both T5557/ATA5567 and ATA5577C devices with both T5557/ATA5567 compatible readers and advanced ATA5577C readers. However, only the ATA5577C devices can profit from the self-calibration and the resultant increase in write distance (see Figure 4-1 for Option register settings).

In this mode, the reference pulse in front of the command is monitored. Depending on the pulse length, the remainder of the command is either evaluated using the fixed bit length protocol or is used as a measurement reference to evaluate the following command bits. Otherwise, the following bits are considered as an invalid command.

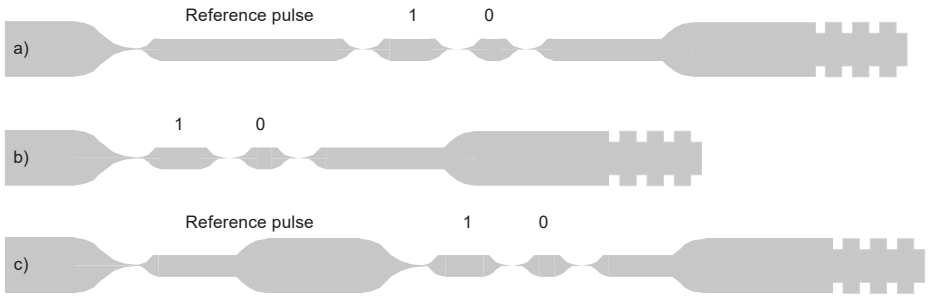
1. For a reference-based command, the reference pulse (dref) has a length of 16 to 32 + 136 = 152 to 168 field clocks (zero bit + timing bias = reference pulse). Hence, the expected length lies between 152 and 168 field clocks. The equivalent expected zero bit length is then extracted and used as a reference for all following bits. The long leading reference pulse, in this case, is used as a timing reference only and does not contribute to the command data itself (see part ‘a’ on Figure 4-18).
2. The first bit must lie within the fixed bit length frame (for example, in Normal mode: 0: 16 to 32 clocks; 1: 48 to 64 clocks), the device switches automatically to the fixed bit length protocol (see 4.12.3 Fixed Bit Length Protocol) and this first pulse is evaluated as the first command bit. This allows compatibility with long leading reference programmed ATA5577C devices, interacting with T5557/ATA5567 readers, which do not send any reference pulses (see part ‘b’ on Figure 4-18).
3. If an T5557/ATA5567 device interacts with an enhanced ATA5577C reader, the reference pulse (152 to 168 field clocks) is ignored by the T5557/ATA5567 and the following data bits are evaluated correctly. Therefore, a T5557/ATA5567 device is compatible with an enhanced ATA5577C reader (see part ‘b’ on Figure 4-18).
4. The first bit corresponds to neither (1) nor (2), then it is rejected as an invalid command.

Table 4-6. Downlink Data Coding Scheme with Long Leading Reference

Parameter	Remark	Symbol	Normal Downlink			Fast Downlink			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Start gap	—	S_{gap}	8	15	50	8	15	50	T_C
Write gap	—	W_{gap}	8	10	20	8	10	20	T_C
Write data coding (gap separation)	Reference Pulse	dref	152	160	168	140	144	148	T_C
			136 clocks + 0 data bit			132 clocks + 0 data bit			T_C
	0 data	d0	dref – 143	dref – 136	dref – 128	dref – 135	dref – 132	dref – 124	T_C
	1 data	d1	dref – 111	dref – 104	dref – 96	dref – 119	dref – 116	dref – 112	T_C

Note: All absolute times assume: $T_C = 1/f_C = 8\ \mu s$ ($f_C = 125$ kHz).

Figure 4-18. Long Leading Reference Protocol



4.12.5 Leading Zero Reference Protocol

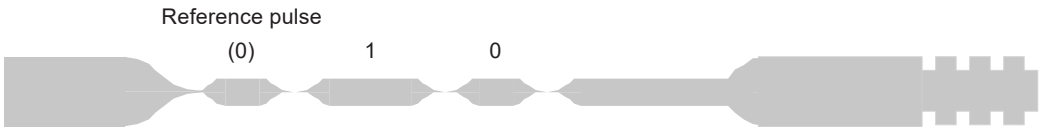
If the device is programmed in this mode, it always expects a reference pulse before the command data itself. This pulse length must correspond exactly to the length of the zero bits in the following command. All further lengths of the zero and one bits of the command are derived from the reference pulse. Therefore, downlink performance is optimal in different environmental conditions.

Table 4-7. Downlink Data Coding Scheme with Leading Zero Reference

Parameter	Remark	Symbol	Normal Downlink			Fast Downlink			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Start gap	—	S_{gap}	8	15	50	8	15	50	T_C
Write gap	—	W_{gap}	8	10	20	8	10	20	T_C
Write data coding (gap separation)	Reference Pulse	dref	12	—	72	8	—	68	T_C
	0 data	d0	dref – 7	dref	dref + 8	dref – 3	dref	dref + 4	T_C
	1 data	d1	dref + 9	dref + 16	dref + 24	dref + 5	dref + 8	dref + 12	T_C

Note: All absolute times assume: $T_C = 1/f_C = 8\ \mu s$ ($f_C = 125$ kHz).

Figure 4-19. Leading Zero Reference Protocol



4.12.6 1-of-4 Coding Protocol

This protocol codes the data in bit pairs so that the length of each packet can have one of four discrete lengths. This protocol is extremely compact and exhibits the least number of field gaps, which in turn, improves the device's ability to extract power from the field. Additionally, a leading reference pulse, '00', is placed in front of the downlink command. This serves as a reference pulse for all following data bits, thus providing an auto-adjustment for varying environmental conditions.

Table 4-8. Downlink Data Coding Scheme with 1-of-4 Coding

Parameter	Remark	Symbol	Normal Downlink			Fast Downlink			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Start gap		S_{gap}	8	15	50	8	15	50	T_C
Write gap		W_{gap}	8	10	20	8	10	20	T_C

.....continued

Parameter	Remark	Symbol	Normal Downlink			Fast Downlink			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Write data coding (gap separation)	Reference pulse '00'	dref	12	—	72	8	—	68	T_C
	'00' data	d00	dref – 7	dref	dref + 8	dref – 3	dref	dref + 4	T_C
	'01' data	d01	dref + 9	dref + 16	dref + 24	dref + 5	dref + 8	dref + 12	T_C
	'10' data	d10	dref + 25	dref + 32	dref + 40	dref + 13	dref + 16	dref + 20	T_C
	'11' data	d11	dref + 41	dref + 48	dref + 56	dref + 21	dref + 24	dref + 28	T_C

Note: All absolute times assume: $T_C = 1/f_C = 8\ \mu s$ ($f_C = 125$ kHz).

Figure 4-20. 1-of-4 Coding Protocol

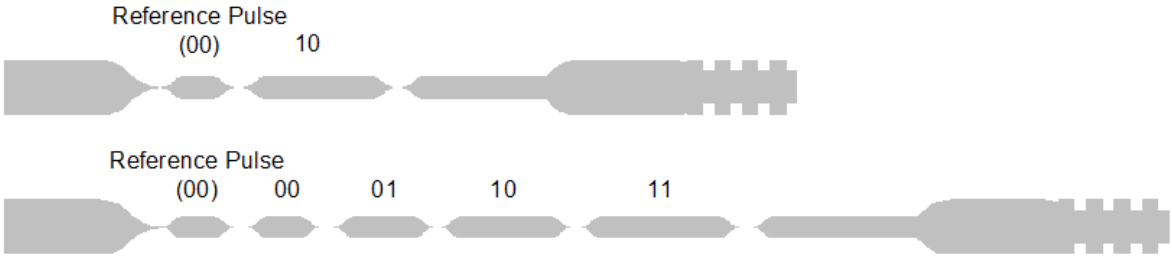
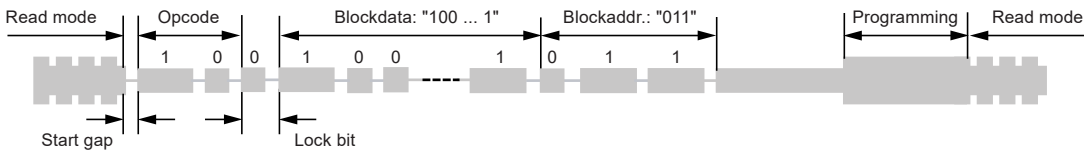
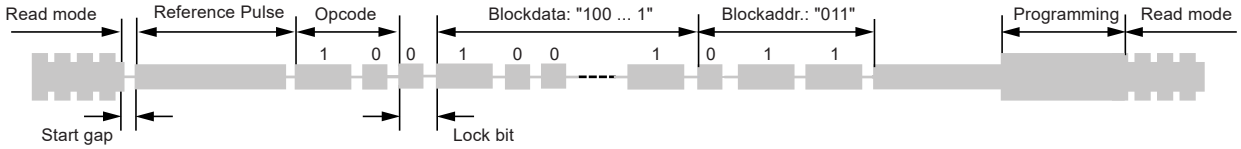


Figure 4-21. Standard Write Sequence Example

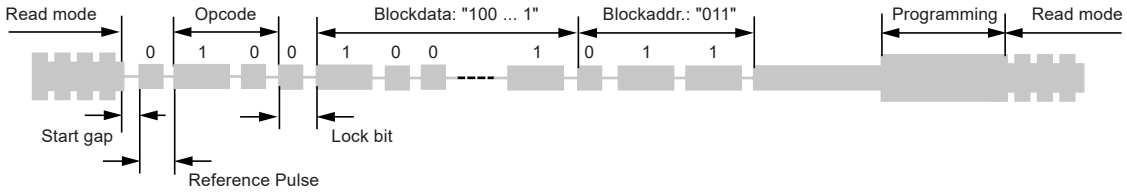
a) Fixed-bit-length Protocol



b) Long-leading-reference Protocol



c) Leading-zero-reference Protocol



d) 1-of-4-coding Protocol

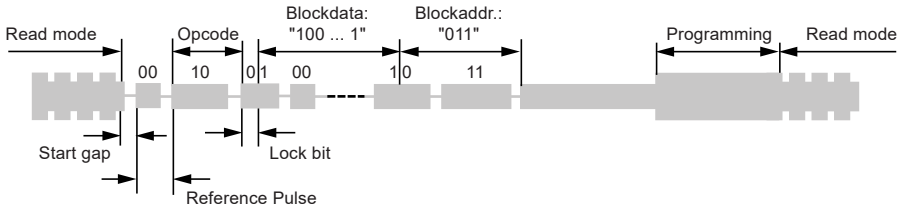
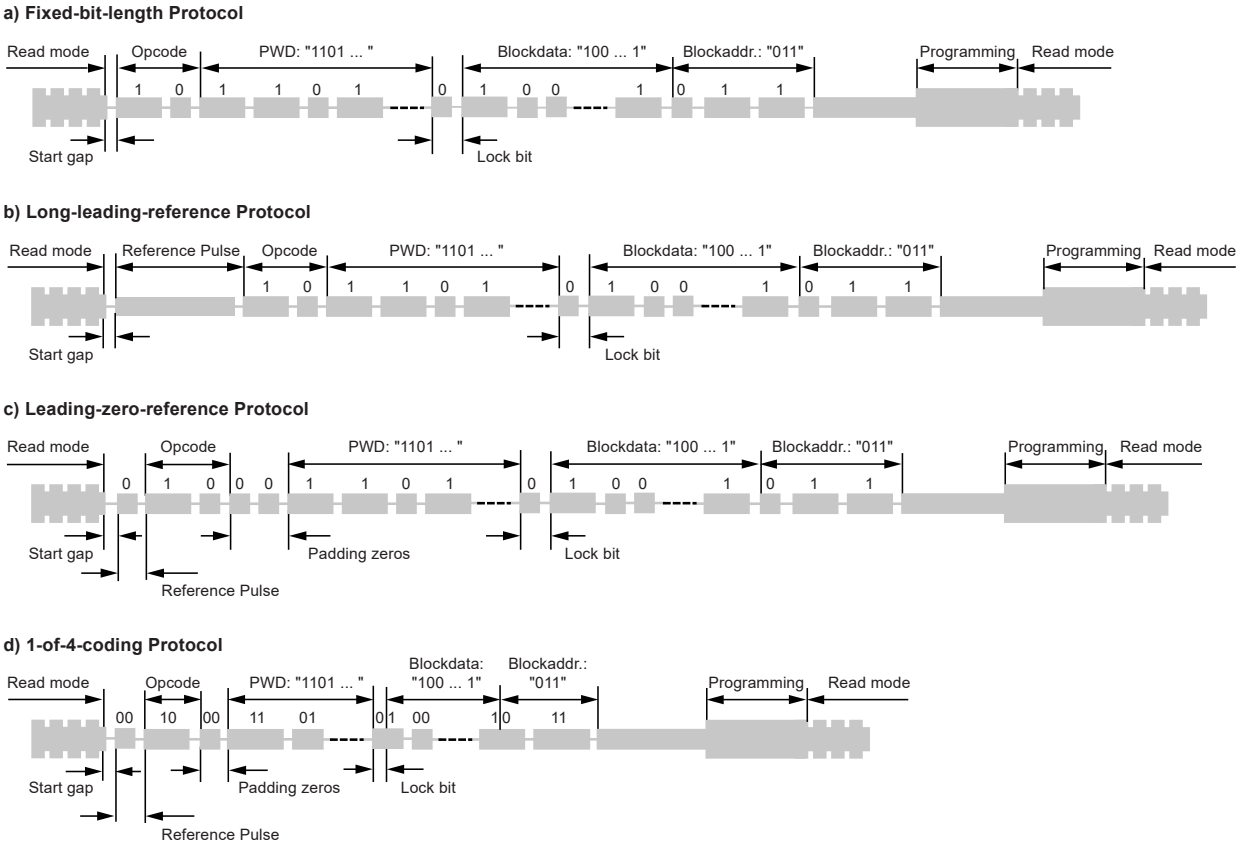


Figure 4-22. Protected Write Sequence Example



4.13 Programming

The ATA5577C can be programmed when all the required information is received. There is a clock delay between the end of the writing sequence and the start of programming.

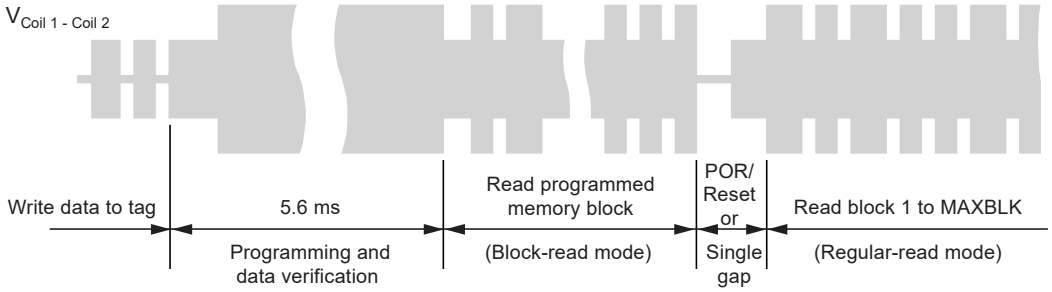
Typical programming time is 5.6 ms. This cycle includes a data verification read to grant secure and correct programming. After programming is successfully executed, the ATA5577C enters Block-Read mode, transmitting the block just programmed as shown in the following figure.

Note: This timing and behavior are different from that of the e555x family predecessors. For more details, refer to relevant application notes.

If the command sequence is validated and the addressed block is not write-protected, then the new data are programmed into the EEPROM memory. The new state of the block write protection bit (lock bit) is programmed at the same time accordingly.

Each programming cycle consists of four consecutive steps: erase block, erase verification (data = `0`), programming and write verification (corresponding data bits = `1`).

Figure 4-23. Coil Voltage after Programming a Memory Block



Note: Programming of page 1 with following single gap leads to a page 1 read. To enter Regular-Read mode, a POR or Reset command must be performed.

5. Error Handling

Several error conditions are detected to ensure that only valid bits are programmed into the EEPROM. There are two error types, which lead to two different actions.

5.1 Errors During Command Sequence

The following detectable errors occur while sending a command sequence to the ATA5577C:

- Wrong number of field clocks between two gaps (that is, not a valid 1 or 0 pulse stream)
- Password mode is activated and the password does not match the contents of block 7
- The number of bits received in the command sequence is incorrect

Valid bit counts accepted by the ATA5577C are listed in the following table.

Table 5-1. Bit Counts of Command Sequences

Command	Protect	Fixed Bit Length Protocol	Long Leading Reference Protocol	Leading Zero Reference Protocol	1-of-4 Coding Protocol
Standard write	(PWD = 0)	38 bits	38 bits	38 bits	38 bits
Direct access	(PWD = 0)	6 bits	6 bits	6 bits	6 bits
Password write	(PWD = 1)	70 bits	70 bits	72 bits	72 bits
Direct access with PWD	(PWD = 1)	38 bits	38 bits	40 bits	40 bits
AOR wake-up	(PWD = 1)	34 bits	34 bits	36 bits	36 bits
Reset command	—	2 bits	2 bits	2 bits	2 bits
Page 0/1 regular read	—	2 bits	2 bits	2 bits	2 bits

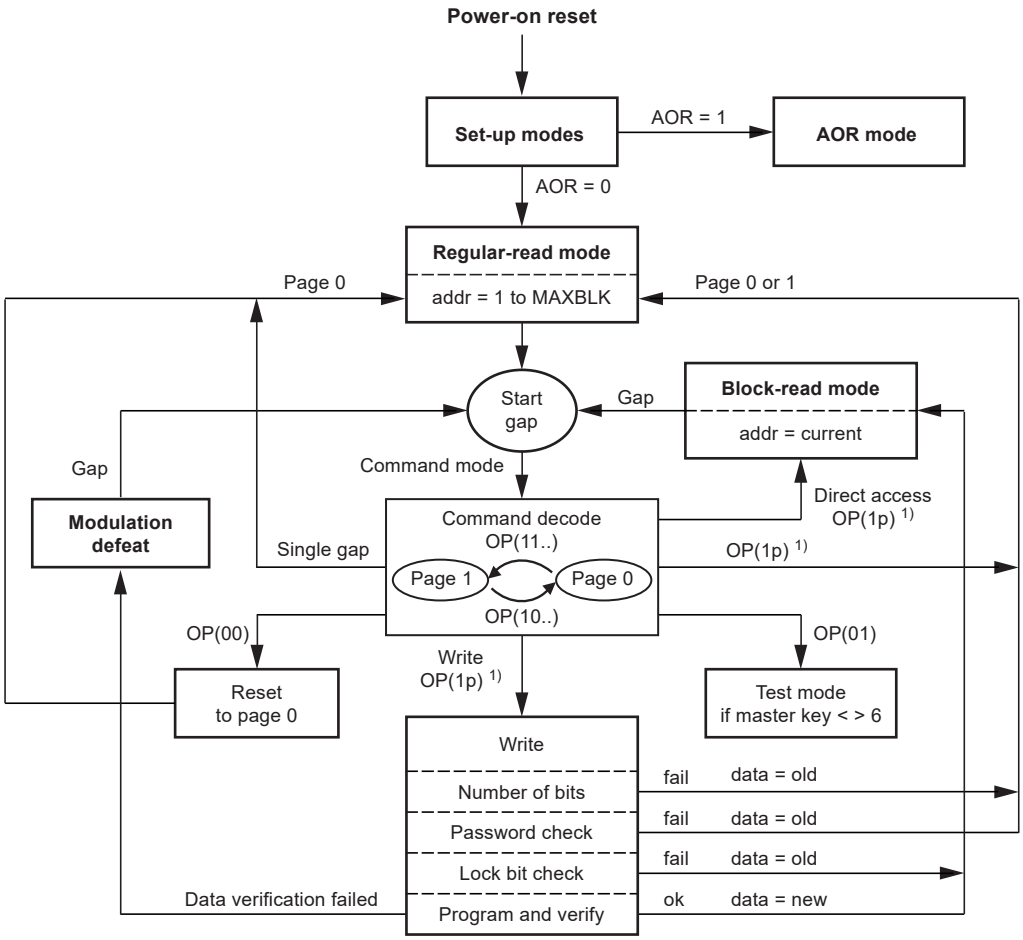
If any of these erroneous conditions (except AOR mode) are detected, the ATA5577C enters Regular-Read mode, starting with block 1 of the page defined in the command sequence. An erroneous AOR wake-up command stops modulation (modulation defeat).

5.2 Errors Before/During Programming the EEPROM

If the command sequence is received successfully, the following errors prevent programming:

- The lock bit of the addressed block is already set.
- If it is a locked block, Programming mode is not entered. The ATA5577C reverts to Block-Read mode, continuously transmitting the currently addressed block.
- If a data verification error is detected after an executed data block programming, the tag stops modulation (modulation defeat) until a new command is transmitted.

Figure 5-1. ATA5577C Functional Diagram



1) p = page selector

Figure 5-2. Example with Manchester Coding with Data Rate RF/16

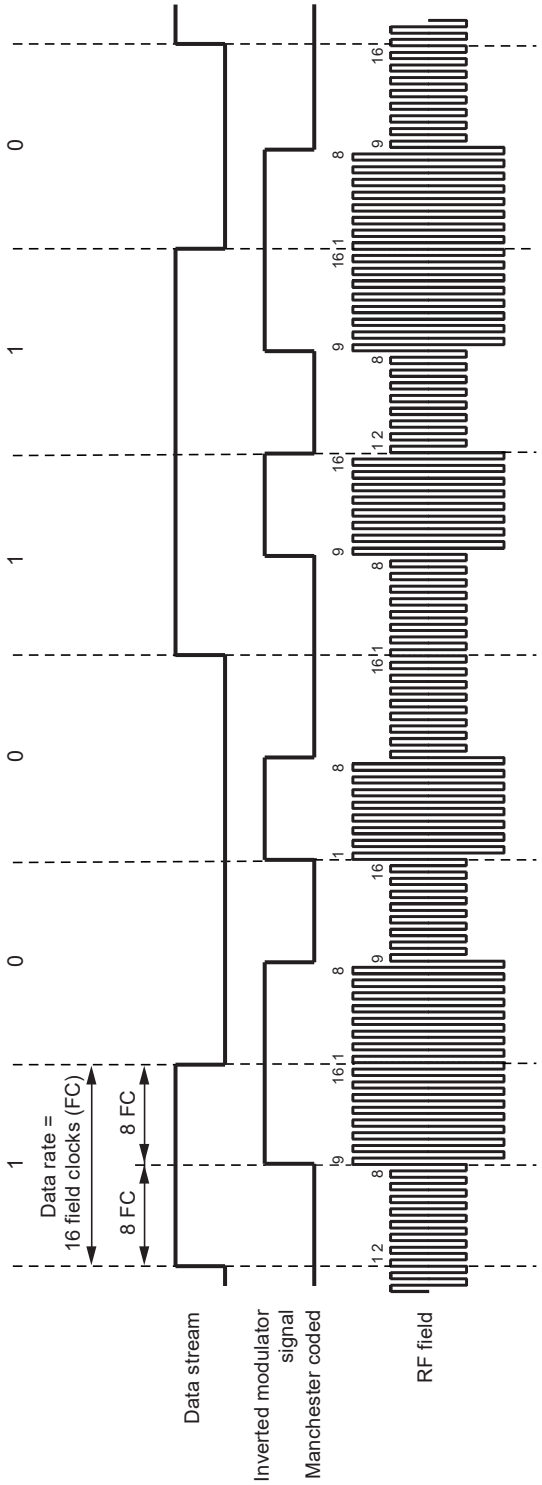


Figure 5-3. Example of Bi-Phase Coding with Data Rate RF/16

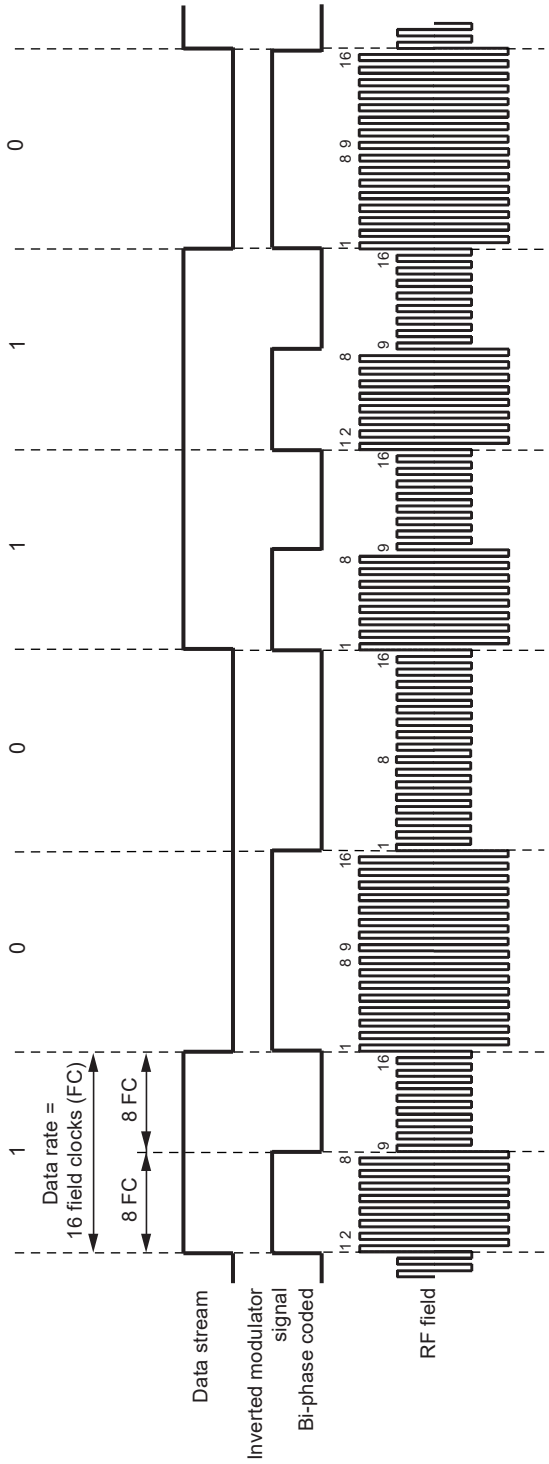


Figure 5-4. Example: FSK1a Coding with Data Rate RF/40, Sub-Carrier f0 = RF/8, f1 = RF/5

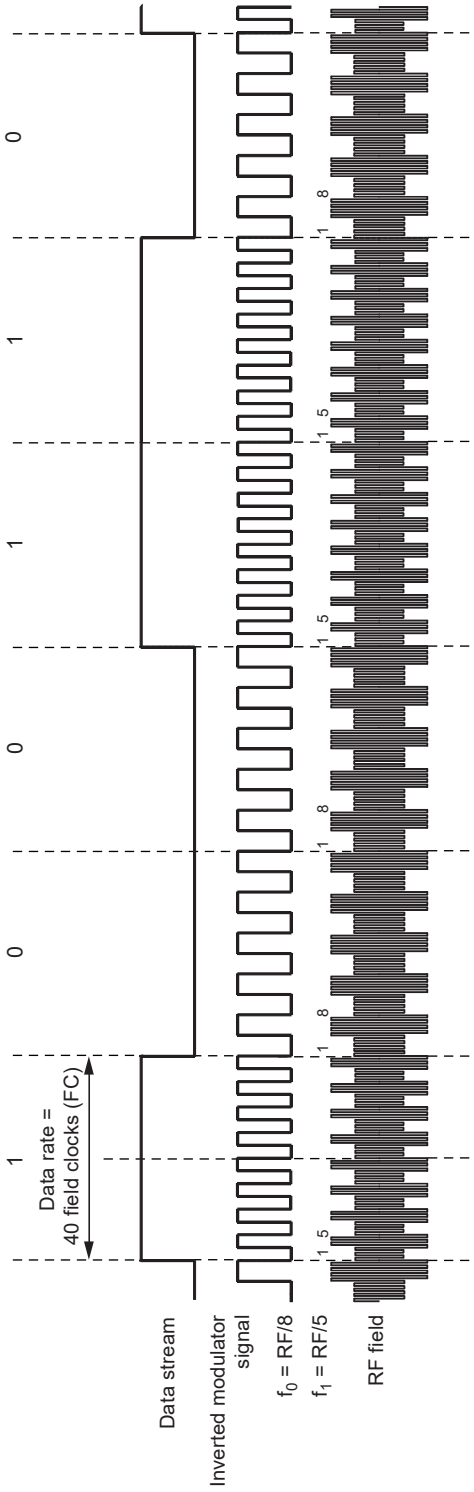


Figure 5-5. Example of PSK1 Coding with Data Rate RF/16

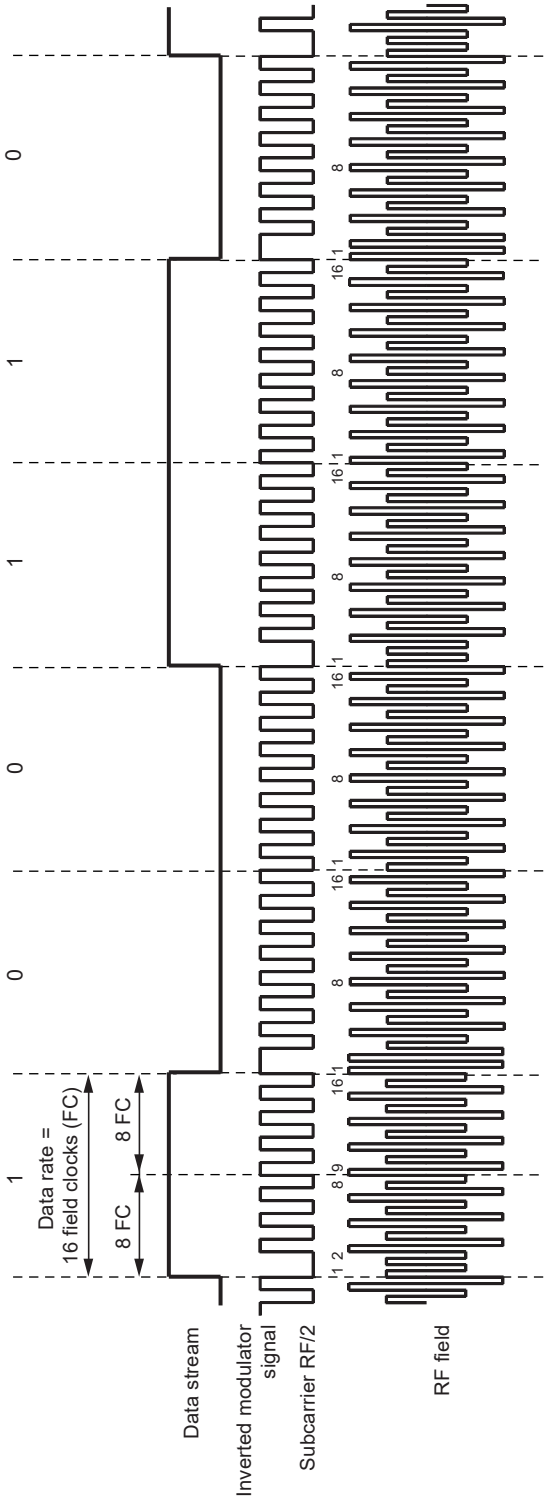


Figure 5-6. Example of PSK2 Coding with Data Rate RF/16

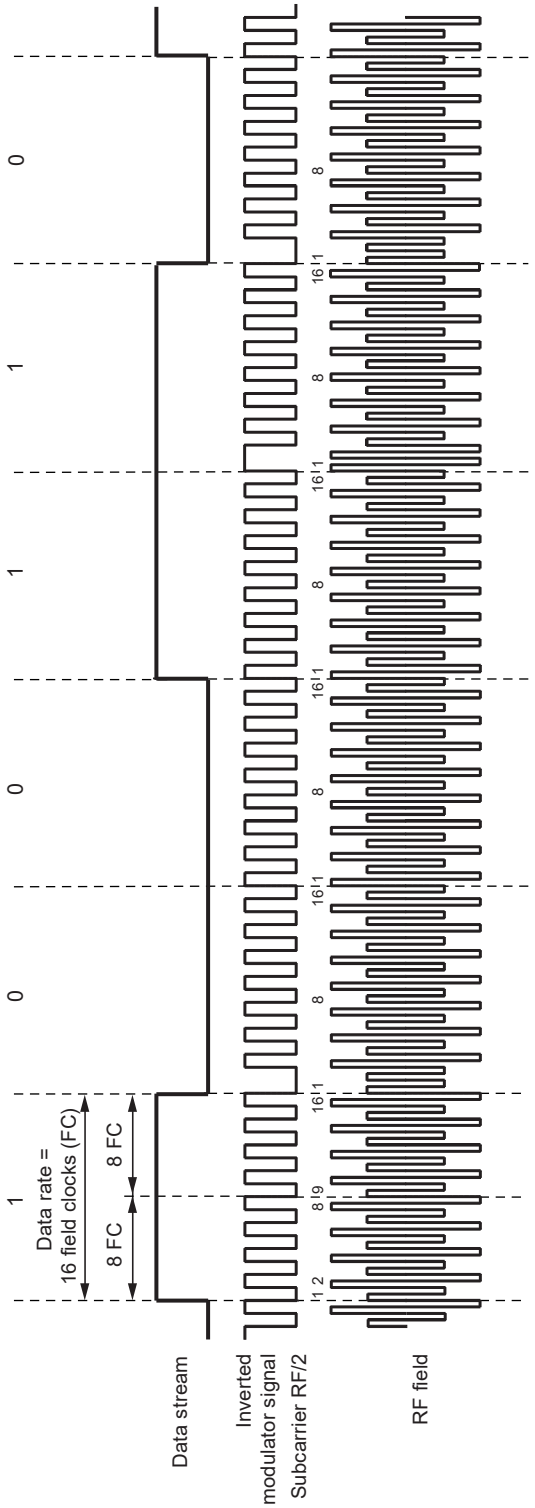
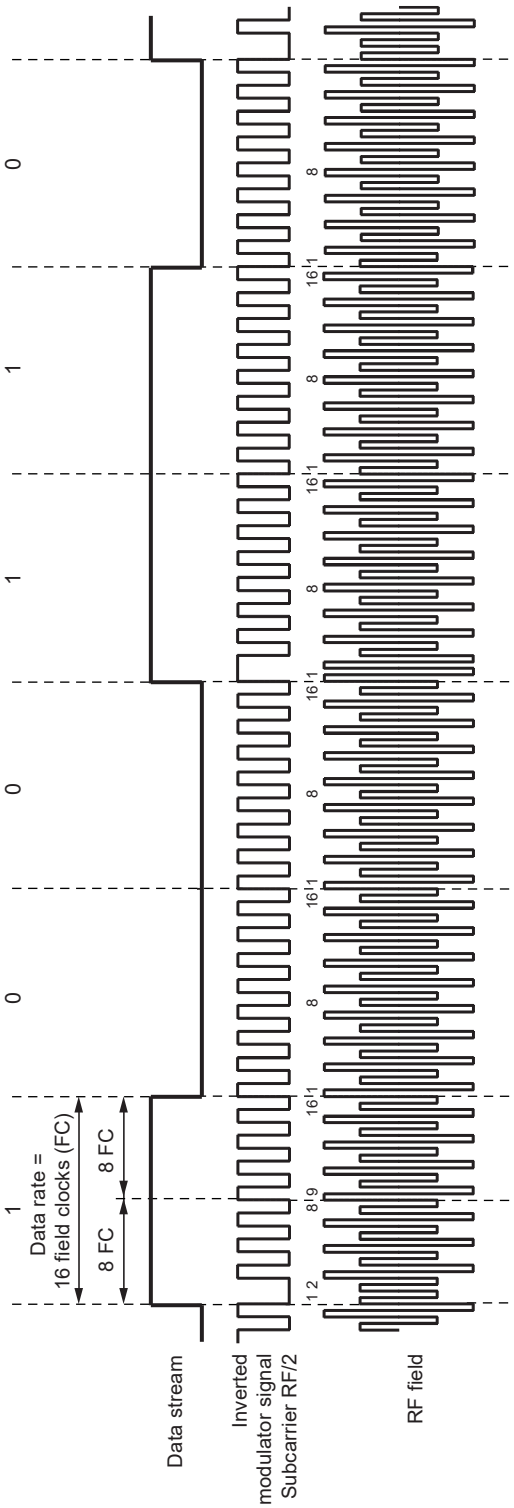


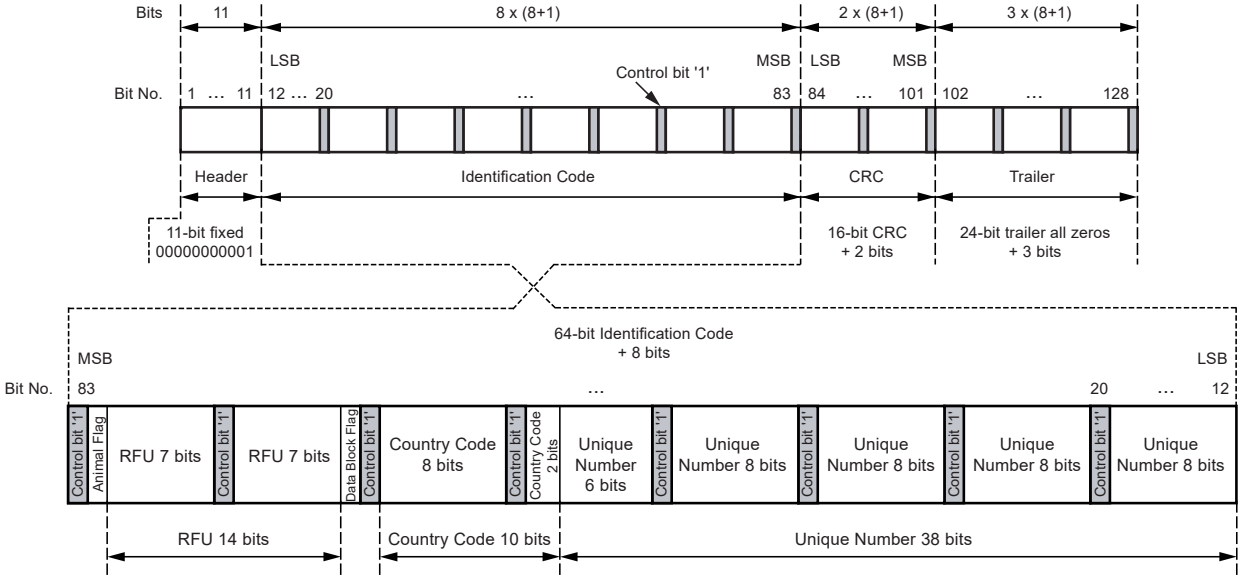
Figure 5-7. Example of PSK3 Coding with Data Rate RF/16



6. Animal ID

In ISO 11784/11785, the code structure of a 128-bit FDX-B telegram is defined. Following is an example of how to program the ATA5577C for ISO 11785 FDX-B.

Figure 6-1. Structure of the ISO 11785 FDX-B Telegram



1. Except for the header, every eight bits are followed by one control bit (‘1’) to prevent the header from recurring.
2. All data are transmitted LSB first.
3. Country codes are defined in ISO 3166.
4. The bits reserved for future use (RFU) are all set to ‘0’.
5. If the data block flag is not set, the trailer bits are all set to ‘0’.
6. CRC is performed on the 64-bit identification code without the control bits. The generator polynomial is $P(x) = x^{16} + x^{12} + x^5 + 1$. Reverse CRC-CCITT (0x8408) is used. Data stream is LSB first.

Table 6-1. Example Data for Animal ID

Code	Dec. Value	Hex. Value	Comment
Animal flag	1	1	Use for animal ID
RFU	0	0	Reserved for future use
Data block flag	0	0	No data in trailer
Country code	999	3E7	Country code for demo tags
Unique number	78187493530	123456789A	Any demo number
CRC	36255	8D9F	CRC for the identification code

Programming of the ATA5577C for animal ID:

- Encoding of the data is differential bi-phase RF/32
- 128 bits have to be transmitted in Regular-Read mode (Maxblock = 4)

Table 6-2. Programming the ATA5577C with Example Data

Block	Address	Value	Comment
Option register	Block 3, page 1	0x 6DD0 0000[1]	Soft modulation, two pulses recommended

.....continued

Block	Address	Value	Comment
Configuration register	Block 0, page 0	0x 603F 8080	RF/32, differential bi-phase, Maxblock = 4
User data block 1	Block 1, page 0	0x 002B 31EB	Header, unique number
User data block 2	Block 2, page 0	0x 54B2 979F	Unique number (cont.), country code
User data block 3	Block 3, page 0	0x 8040 7F3B	Data block flag, RFU, animal flag, CRC
User data block 4	Block 4, page 0	0x 1804 0201	CRC (cont.), trailer bits

Note:

1. Depending on application, settings may vary.

7. Electrical Characteristics

The electrical characteristics of ATA5577C are described in the following table.

T_{amb} = +25°C; f_{coil} = 125 kHz; unless otherwise specified.

Table 7-1. Electrical Characteristics

No.	Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit	Type*
1	RF Frequency Range		f_{RF}	100	125	150	kHz	
2.1	Supply Current (without current consumed by the external LC tank circuit)	T_{amb} = 25°C(1)	I_{DD}		1.5	3	µA	T
2.2		Read – full temperature range			2	5	µA	Q
2.3		Programming full – temperature range			25		µA	Q
3.1	Coil Voltage (AC supply)	POR threshold (50 mV hysteresis)	$V_{coil\ pp}$		3.6		V	Q
3.2		Read mode and write command(2)		6		V_{clamp}	V	Q
3.3		Program EEPROM(2)		8		V_{clamp}	V	Q
4	Start-up Time	$V_{coil\ pp}$ = 6V	$t_{startup}$		2.5		ms	Q
5.1	Clamp Voltage (depends on settings in Option register)	3 mA current into Coil 1/ Coil 2	$V_{PP\ clamp\ lo}$		11		V	Q
5.2			$V_{PP\ clamp\ med}$		13		V	Q
5.3			$V_{PP\ clamp\ hi}$	14	17	21	V	T
5.4		20 mA current into Coil 1/ Coil 2	$V_{PP\ clamp\ med}$	13	15	18	V	T
6.1	Modulation Parameters (depends on settings in Option register)	3 mA current into Coil 1/ Coil 2 and modulation on	$V_{PP\ mod\ lo}$	2	3	4	V	T
6.2			$V_{PP\ mod\ med}$		5		V	Q
6.3			$V_{PP\ mod\ hi}$		7		V	Q
6.4		20 mA current into Coil 1/ Coil 2 and modulation on	$V_{PP\ mod\ med}$	6	7.5	9	V	T
6.5	Thermal Stability		$V_{mod\ lo}/T_{amb}$		-1		mV/°C	Q
7.1	Clock Detection Level (depends on settings in Option register)	$V_{coil\ pp}$ = 8V	$V_{clkdet\ lo}$		250		mV	Q
7.2			$V_{clkdet\ med}$	400	550	730	mV	T
7.3			$V_{clkdet\ hi}$		800		mV	Q
7.4	Gap Detection Level (depends on settings in Option register)	$V_{coil\ pp}$ = 8V	$V_{gapdet\ lo}$		250		mV	Q
7.5			$V_{gapdet\ med}$	400	550	730	mV	T
7.6			$V_{gapdet\ hi}$		850		mV	Q
8	Programming Time	From last command gap to re-enter Read mode (64 + 648 internal clocks)	T_{prog}	5	5.7	6	ms	T
9	Endurance	Erase all/write all(3)	n_{cycle}	100000			Cycles	Q

.....continued

No.	Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit	Type*
10.1	Data Retention	Top = 55°C[3]	$t_{retention}$	10	20	50	Years	Q
10.2		Top = 150°C[3]	$t_{retention}$	96			hrs	T
10.3		Top = 250°C[3]	$t_{retention}$	24			hrs	Q
11.1	Resonance Capacitor	Mask option[4]	C_r	320	330	340	pF	T
11.2				242	250	258		
11.3					130			
11.4					75			
11.5					10			Q
12.1	Micromodule Capacitor Parameters[4]	Capacitance tolerance T_{amb}	C_r	320	330	340	pF	T

* Type means:

- T: Directly or indirectly tested during production
- Q: Ensured based on initial product qualification data

Note:

1. I_{DD} measurement setup: EEPROM programmed to 00 ... 000 (erase all); chip in modulation defeat.
2. Current into Coil 1/Coil 2 is limited to 10 mA.
3. Since EEPROM performance is influenced by assembly processes, cannot confirm the parameters for -DDW (tested die on unsawn wafer) delivery.
4. For more details, refer to 8. Ordering Information.

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 7-2. Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Maximum DC Current into Coil 1/Coil 2	I_{coil}	20	mA
Maximum AC Current into Coil 1/Coil 2, f = 125 kHz	$I_{coil\ p}$	20	mA
Power Dissipation (die) (free air condition, time of application: 1s)	P_{tot}	100	mW
Electrostatic Discharge Maximum to ANSI/ESD-STM5.1-2001 Standard (HBM)	V_{max}	3000	V
Operating Ambient Temperature Range	T_{amb}	-40 to +85	°C
Storage Temperature Range (data retention reduced)	T_{stg}	-40 to +150	°C

8. Ordering Information

The following figures illustrate the part number of ATA5577M devices.

Figure 8-1. ATA5577M Die Type 1

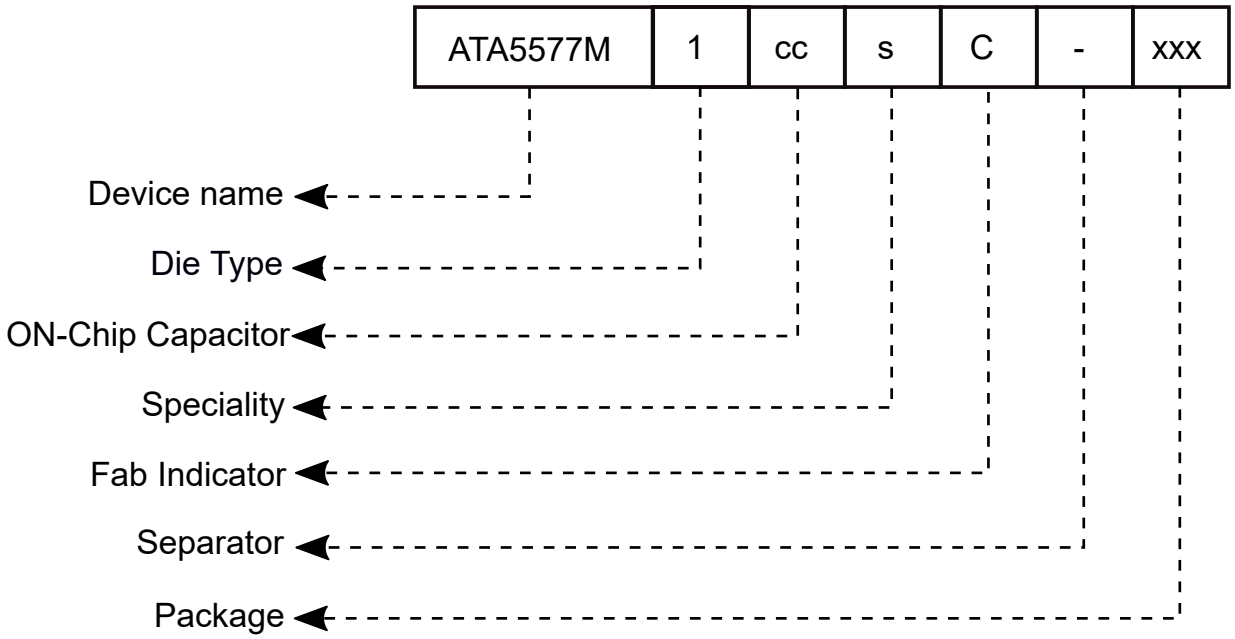
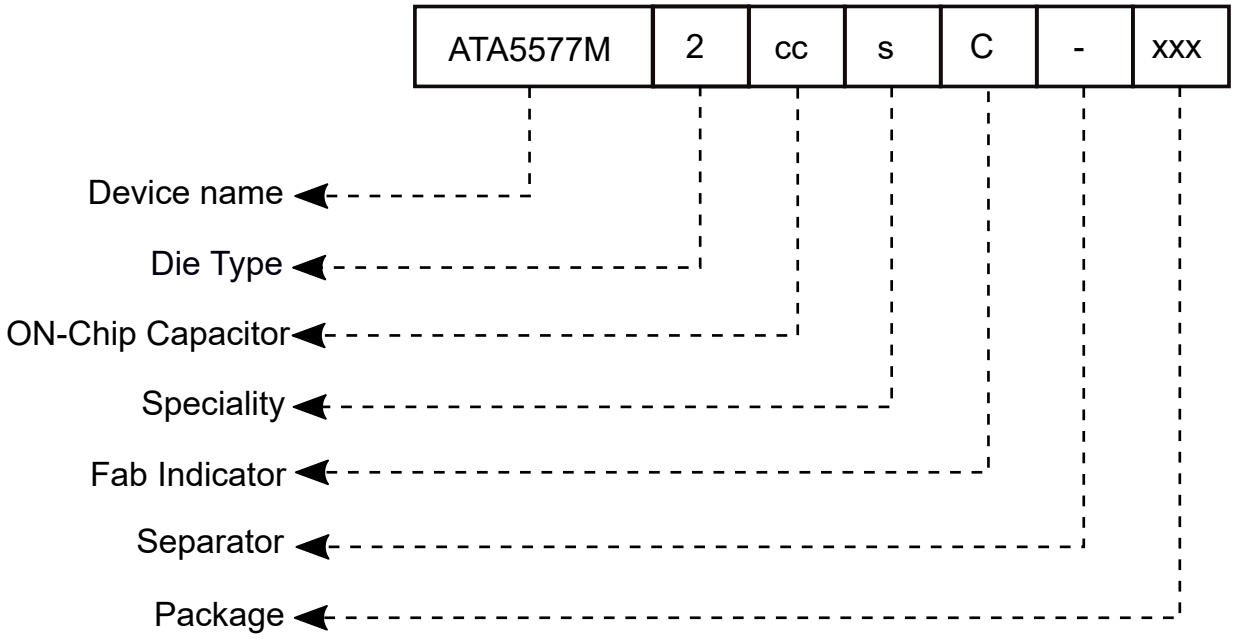


Figure 8-2. ATA5577M Die Type 2



8.1 Ordering Details for Pad Type 1

The following table provides the ordering details of ATA5577M devices for pad type 1.

Table 8-1. Ordering Details for Pad Type 1

Model Number	Die Description	Ordering Code	Description
ATA5577M	Type 1 – Standard pads	ATA5577M1330C-DDB ATA5577M133SC-DDB	• On-chip capacity value in pF – 330 • Package: – 6" sawn wafer on foil with ring – Thickness 150 µm (approx. 6 mil) • Fab indicator – C • Speciality: – 0: Nothing special – S: Preprogrammed in unique format • Refer to Figure 9-1
		ATA5577M1330C-DDW	• On-chip capacity value in pF – 330 • Package – 6" wafer, thickness 680 µm (approx. 27 mil) • Fab indicator – C • Refer to Figure 9-1
		ATA5577M1330C-PAE	• On-chip capacity value in pF – 330 • Package – NOA3 micromodule (lead-free) • Fab indicator – C • Refer to: – Figure 9-5 – Figure 9-6
		ATA5577M1330C-UFQW	• On-chip capacity value in pF – 330 • Package – XDFN package 1.5 mm by 2 mm, thickness 0.37 mm • Fab indicator – C • Refer to Figure 9-7
		ATA5577M1330C-PPMY	• On-chip capacity value in pF – 330 • Package – Transponder Brick package • Fab indicator – C • See *"ATA5577M1330C-PPMY Data Sheet"*

8.2 Ordering Details for Pad Type 2

The following table provides the ordering details of ATA5577M devices for pad type 2.

Table 8-2. Ordering Details for Pad Type 2

Model Number	Die Description	Ordering Code	Description
ATA5577M	Type 2 – Mega pads, 200 µm by 400 µm	ATA5577M2330C-DBB ATA5577M233SC-DBB ATA5577M233AC-DBB	• On-chip capacity value in pF = 330 • Package: – 6" sawn wafer on foil with ring – Thickness 150 µm (approx. 6 mil) with gold bumps 25 µm • Fab indicator – C • Speciality: – 0: Nothing special – S: Preprogrammed in unique format – A: Thickness 280 µm (approx. 11 mil) with gold bumps 25 µm (for DBB) • Refer to Figure 9-2
		ATA5577M2330C-DBQ ATA5577M233SC-DBQ	• On-chip capacity value in pF = 330 • Package – Die in blister tape, thickness 280 µm (approx. 11 mil), plus gold bumps 25 µm • Fab indicator – C • Speciality: – 0: Nothing special – S: Preprogrammed in unique format • Refer to Figure 9-4
		ATA5577M233TC-DBB	• On-chip capacity value in pF = 330 • Package: – 6" sawn wafer on foil with 8" ring – Thickness 150 µm (approx. 6 mil) with gold bumps 25 µm • Fab indicator: C • Speciality: – T: Preprogrammed in unique format • Refer to Figure 9-3

8.3 Configuration on Delivery

The following table describes the configuration on delivery of ATA5577C.

Table 8-3. Configuration on Delivery

Block	Address	Value	Comment
AFE option setup	Block 3, page 1	0x 0000 0000	All options take on the default state
Configuration register	Block 0, page 0	0x 0008 8040	RF/32, Manchester, Maxblock = 2
User data block 1	Block 1, page 0	0x 0000 0000	All ‘0’s
User data block 2	Block 2, page 0	0x 0000 0000	All ‘0’s

9. Package Information

The following figures illustrate the package information of ATA5577C.

Figure 9-1. Sawn Wafer on Foil with Ring (Type 1, Standard Pads)

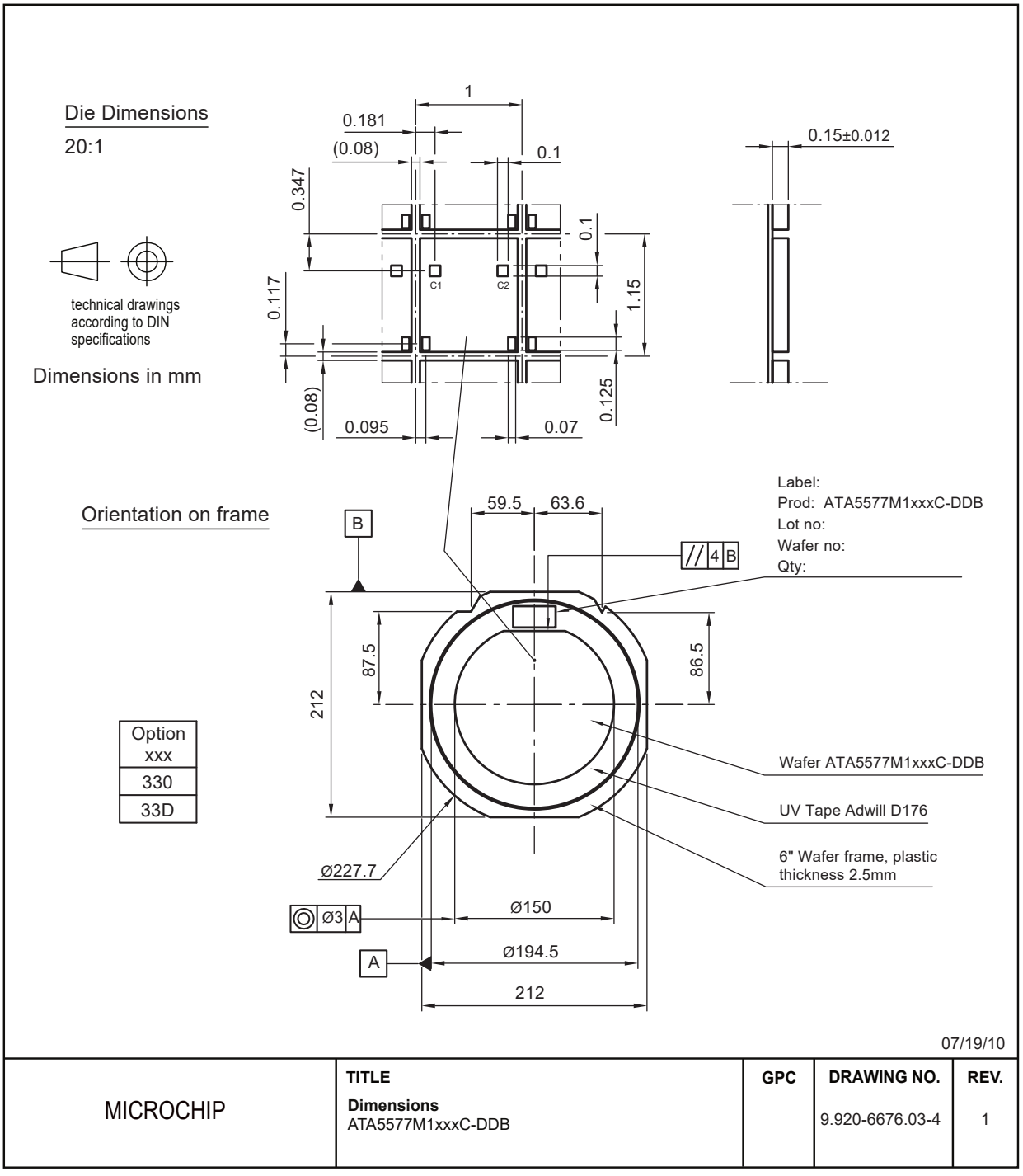


Figure 9-2. Sawn Wafer on Foil with Ring (Type 2, Mega Pads and Au Bumps)

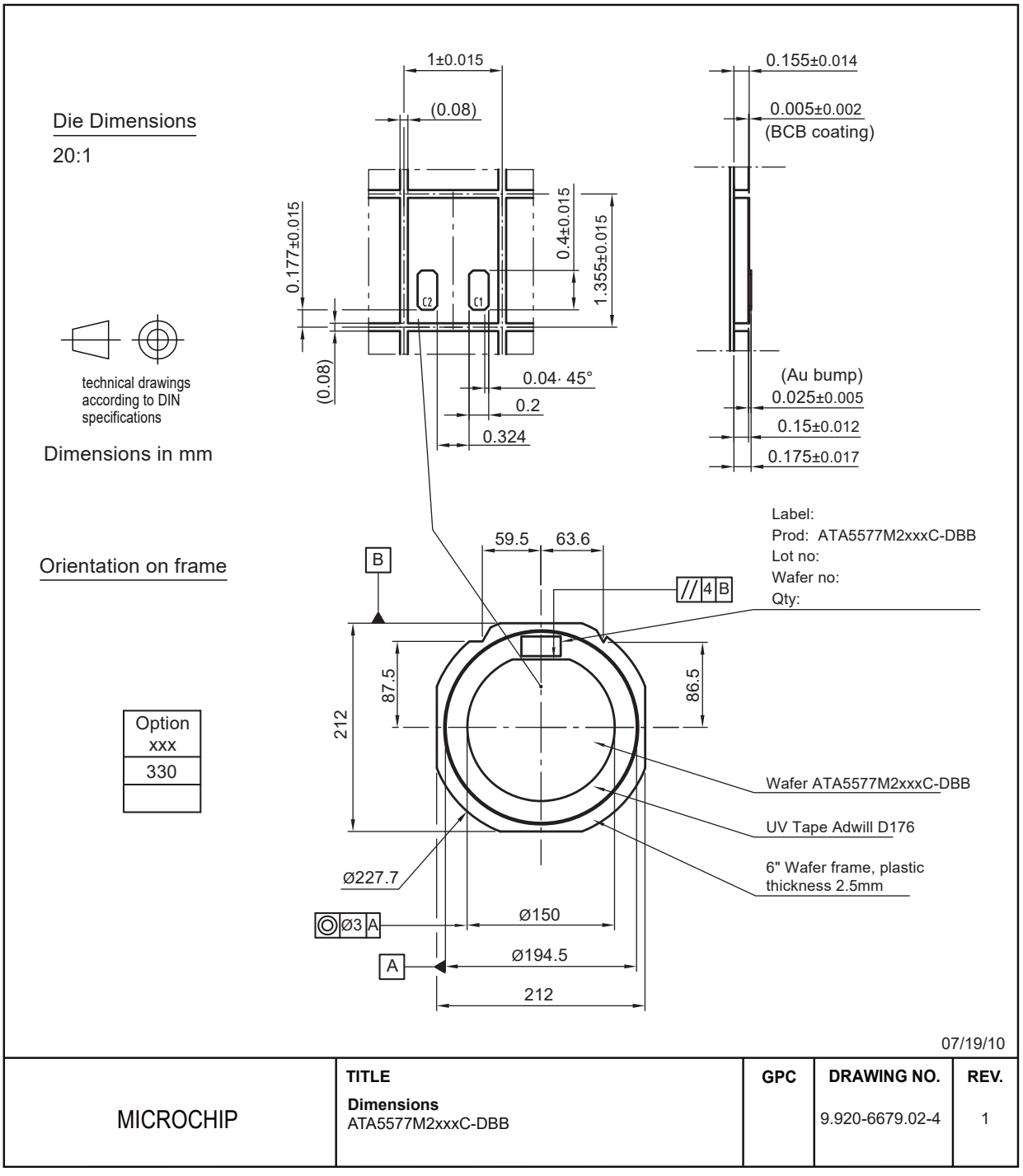


Figure 9-3. Sawn Wafer on Foil with Ring (Gold Bumps)

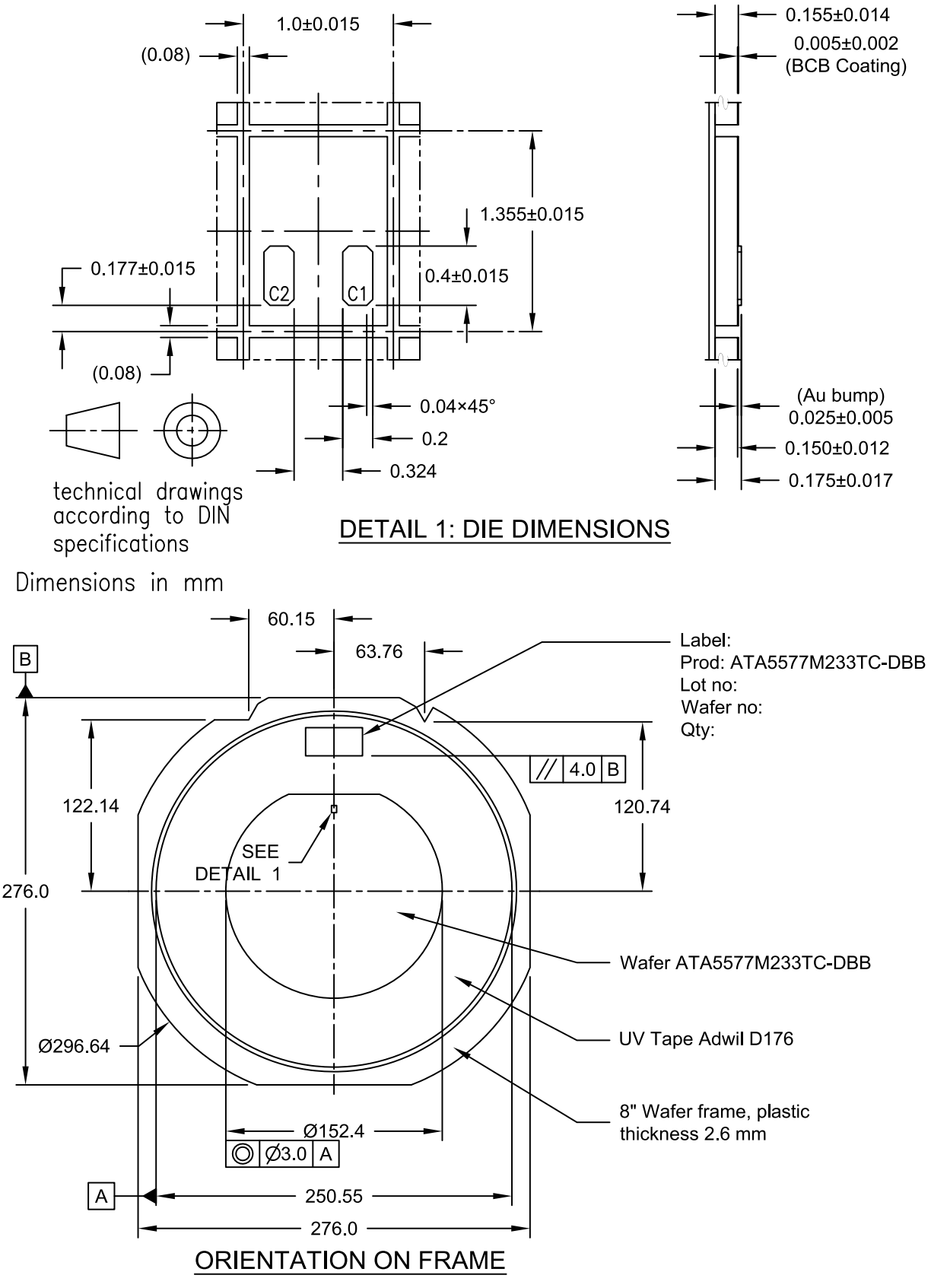
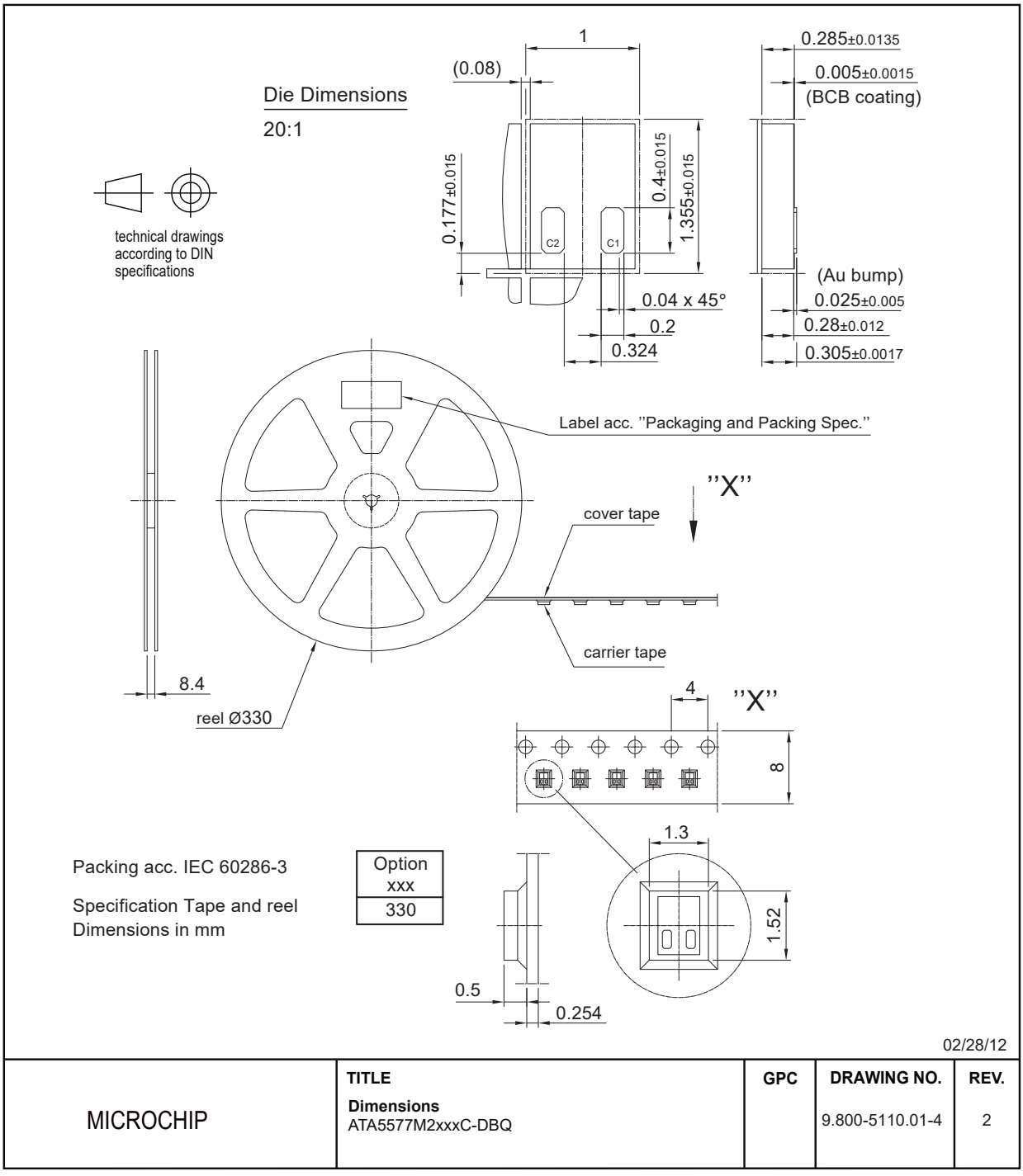
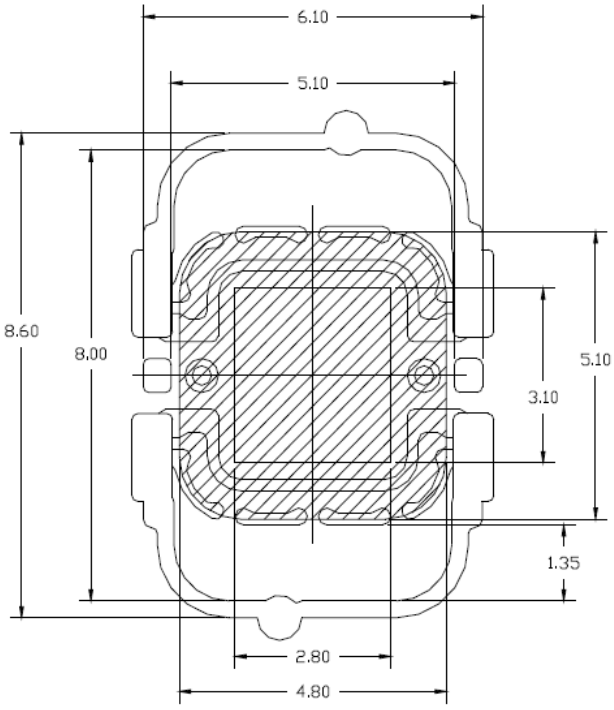


Figure 9-4. Die in Blister Tape



	TITLE	GPC	DRAWING NO.	REV.
MICROCHIP	**Dimensions** ATA5577M2xxxC-DBQ		9.800-5110.01-4	2

Figure 9-5. NOA3S Micromodule



NOA3S Module
(all dimensions in mm)

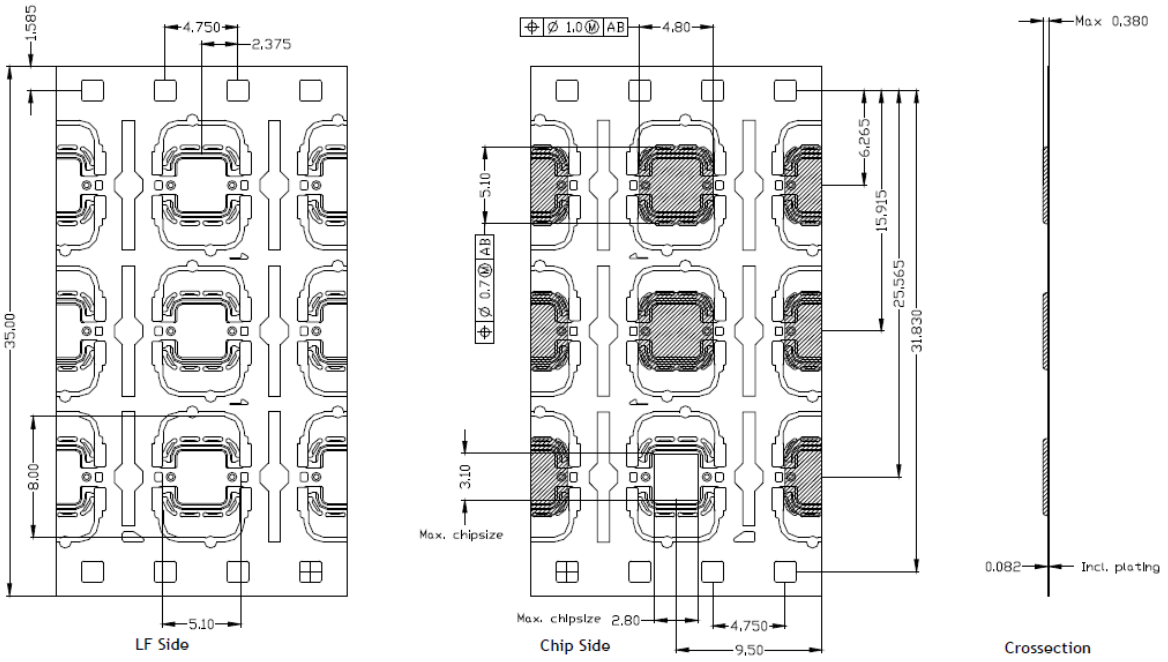
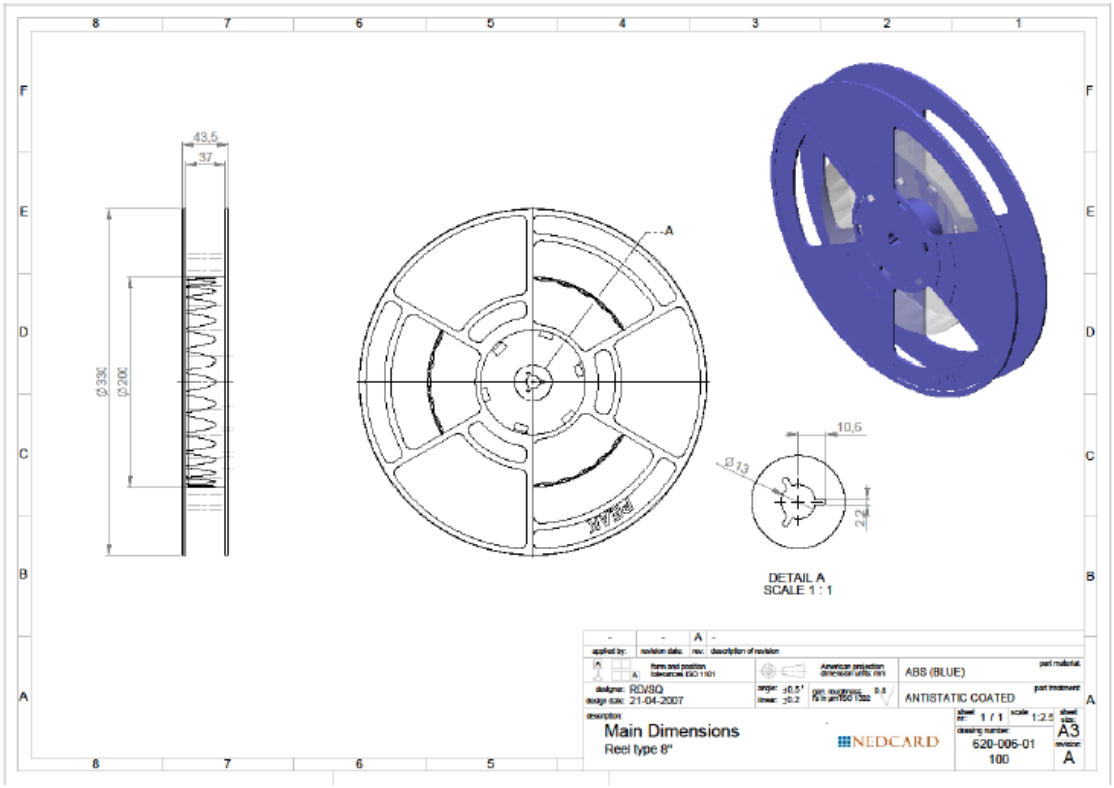
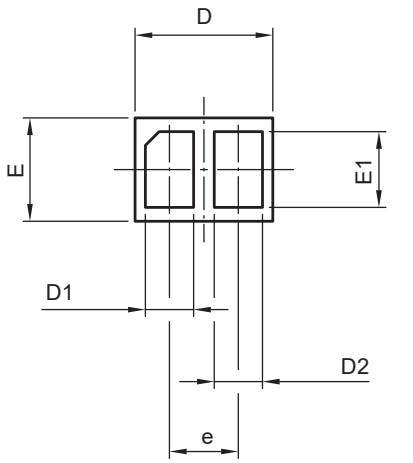


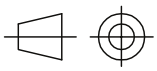
Figure 9-6. Shipping Reel for NOA3 Micromodule



Reel type: TX36-08-A2.
ESD Surface resistivity: 10^8 - 10^{11} Ohms/SQ
Outer diameter: 330 m +0.3/-0.4 mm
Total thickness of reel: 45.2 max.

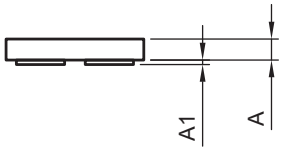
Figure 9-7. XDFN Package

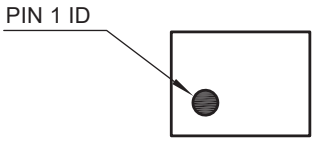




technical drawings
according to DIN
specifications

Dimensions in mm





COMMON DIMENSIONS (Unit of Measure = mm)			
Symbol	**MIN**	**NOM**	**MAX**
A	0.32	0.37	0.4
A1		0.1 nom.	
D	1.95	2	2.05
D1	0.6	0.7	0.8
D2	0.6	0.7	0.8
E	1.45	1.5	1.55
E1	1	1.1	1.2
e		1 BSC	

04/06/11

	TITLE	GPC	DRAWING NO.	REV.
MICROCHIP	**Package: XDFN_1.5x2_2L**		6.543-5159.01-4	1

10. Document Revision History

Revision	Date	Section	Description
B	02/20	Document	• 8.2 Ordering Details for Pad Type 2 was updated • Added new delivery option, “ATA5577M233TC-DBB” (Figure 9-3)
A	04/18	Document	• Updated from Atmel to Microchip template • Assigned a new Microchip document number. Previous version is Atmel 9187 revision H. • ISBN number added.

10.1 Atmel Revision History

Revision No.	History
9187H-RFID-07/14	• Section 10 “Ordering Information” on pages 38 to 39 updated • Section 11 “Package Information” on pages 40 to 45 updated
9187G-RFID-04/13	• Section 10 “Ordering Information” on pages 37 to 38 updated
9187F-RFID-01/13	• Section 5.5 “Initialization and Init Delay” on page 11 updated • Figure 5-1 “Answer-on-request (AOR) Mode ...” on page 12 updated • Figure 5-9 “Complete Writing Sequence ...” on page 19 updated • Ordering Information for ATA5577M1cccC-DDW on pages 37 and 38 added
9187E-RFID-07/12	• Section 10 “Ordering Information” on pages 37 to 38: Ordering codes added
9187D-RFID-04/12	• Figure 11-4 “Die in Blister Tape” on page 42 added • Figure 11-5 “Die on Sticky Tape” on page 43 updated
9187C-RFID-04/11	• Figure 11-1 “Pad Layout (Type 1, Standard Pads)” on page 41 removed • Figure 11-2 “Pad Layout (Type 2, Mega Pads)” on page 42 removed
9187BX-RFID-03/11	• Section 10 “Ordering Information” on page 39 changed • Section 10.1 “Available Order Codes” on page 40 changed • Figure 11-4 “Die in Waffle Pack” on page 44 added

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