MCP48CXBX4/8

8/10/12-Bit Digital-to-Analog Converters, 1 LSb INL, Quad/Octal Voltage Output with SPI Interface

Features

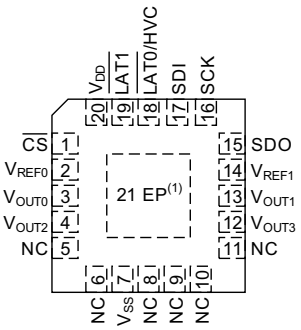
- Memory Options:
  - Volatile memory: MCP48CVBXX
  - Nonvolatile memory: MCP48CMBXX
- Operating Voltage Range:
  - 2.7V to 5.5V – full specifications
  - 1.8V to 2.7V – reduced device specifications
- Output Voltage Resolutions:
  - 8-bit: MCP48CXB0X (256 steps)
  - 10-bit: MCP48CXB1X (1024 steps)
  - 12-bit: MCP48CXB2X (4096 steps)
- Nonvolatile Memory (MTP) Size: 32 Locations
- 1 LSb Integral Nonlinearity (INL) Specification
- DAC Voltage Reference Source Options:
  - Device V_{DD}
  - External V_{REF} pin (buffered or unbuffered)
  - Internal band gap (1.214V typical)
- Output Gain Options:
  - 1x (unity)
  - 2x (available when not using internal V_{DD} as voltage source)
- Power-on/Brown-out Reset (POR/BOR) Protection
- Power-Down Modes:
  - Disconnects output buffer (high-impedance)
  - Selection of V_{OUT} pull-down resistors (100 kΩ or 1 kΩ)
- SPI Interface:
  - Supports '00' and '11' modes
  - Write speed: up to 50 MHz
  - Read speed: up to 25 MHz
- Package Types:
  - 20-lead 4 mm x 4 mm QFN, 20-lead TSSOP
- Extended Temperature Range: -40°C to +125°C

Applications

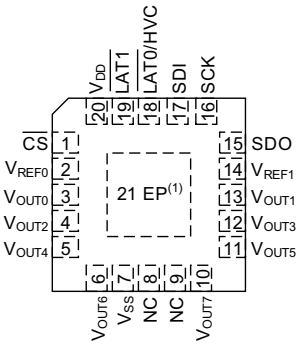
- Set Point or Offset Trimming
- Sensor Calibration
- Low-Power Portable Instrumentation
- Data Acquisition Systems
- Motor Control

Package Types

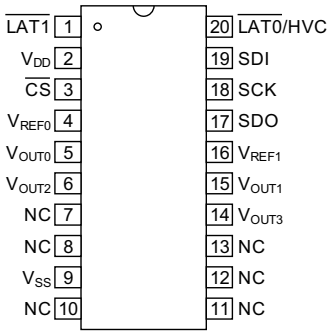
MCP48CXBX4 (Quad)
20-Lead QFN (4 x 4)



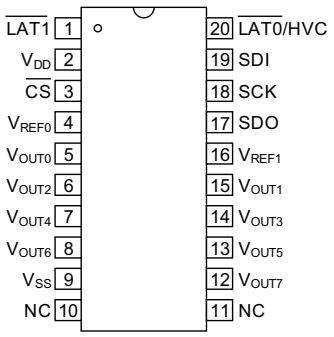
MCP48CXBX8 (Octal)
20-Lead QFN (4 x 4)



MCP48CXBX4 (Quad)
20-Lead TSSOP



MCP48CXBX8 (Octal)
20-Lead TSSOP



Note 1: Includes Exposed Thermal Pad (EP); see Table 3-1 and Table 3-2.

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General Description

The MCP48CXBX4/8 devices are quad and octal channel 8-bit, 10-bit and 12-bit buffered voltage output Digital-to-Analog Converters (DAC) with volatile or MTP memory and an SPI serial interface.

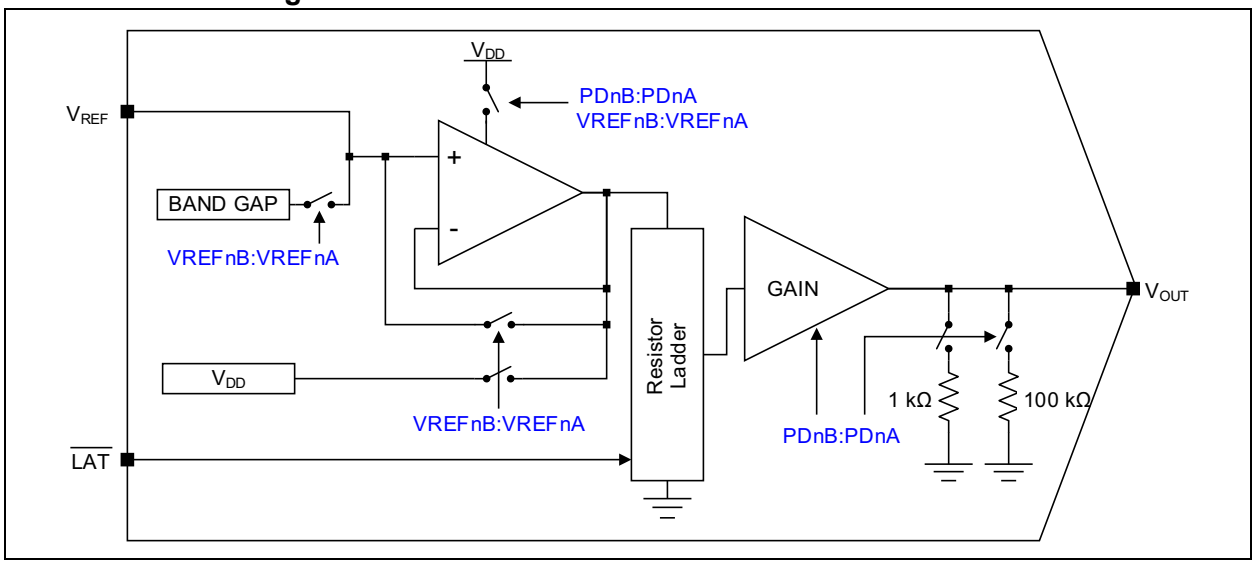
The MTP memory can be written by the user up to 32 times for each specific register. It requires a high-voltage level on the HVC pin, typically 7.5V, in order to successfully program the desired memory location. The nonvolatile memory consists of power-up output values, configuration registers and general purpose locations.

The V_{REF} pin, the device V_{DD} or the internal band gap voltage can be selected as the DAC's reference voltage. When V_{DD} is selected, V_{DD} is internally connected to the DAC reference circuit.

When the V_{REF} pin is used with an external voltage reference, the user can select between a gain of 1 or 2 and can have the reference buffer enabled or disabled. When the gain is 2, the V_{REF} pin voltage must be limited to a maximum of $V_{DD}/2$.

These devices have a four-wire SPI-compatible serial interface with speeds up to 50 MHz for write and 25 MHz for read operations.

DAC Core Block Diagram



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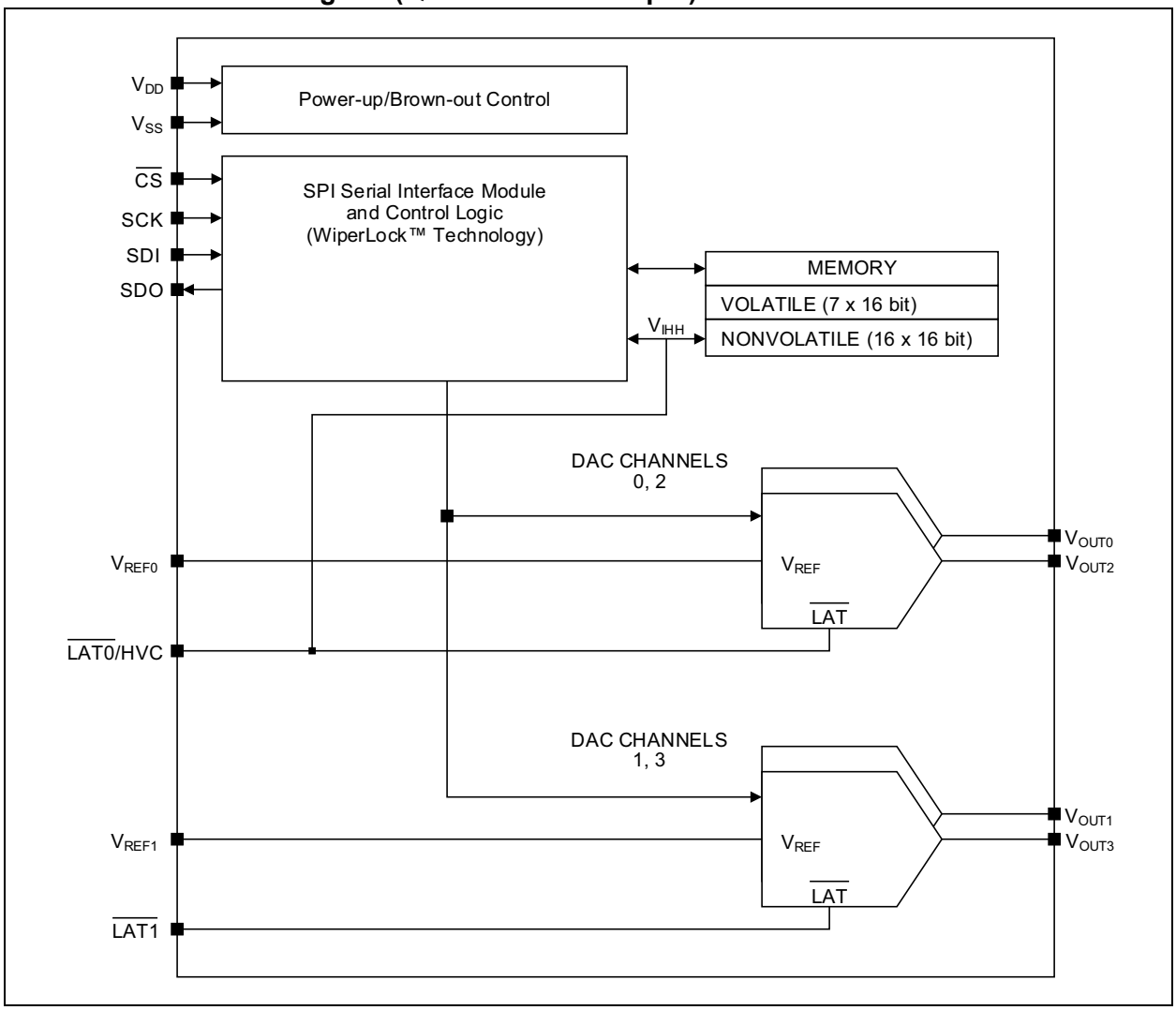
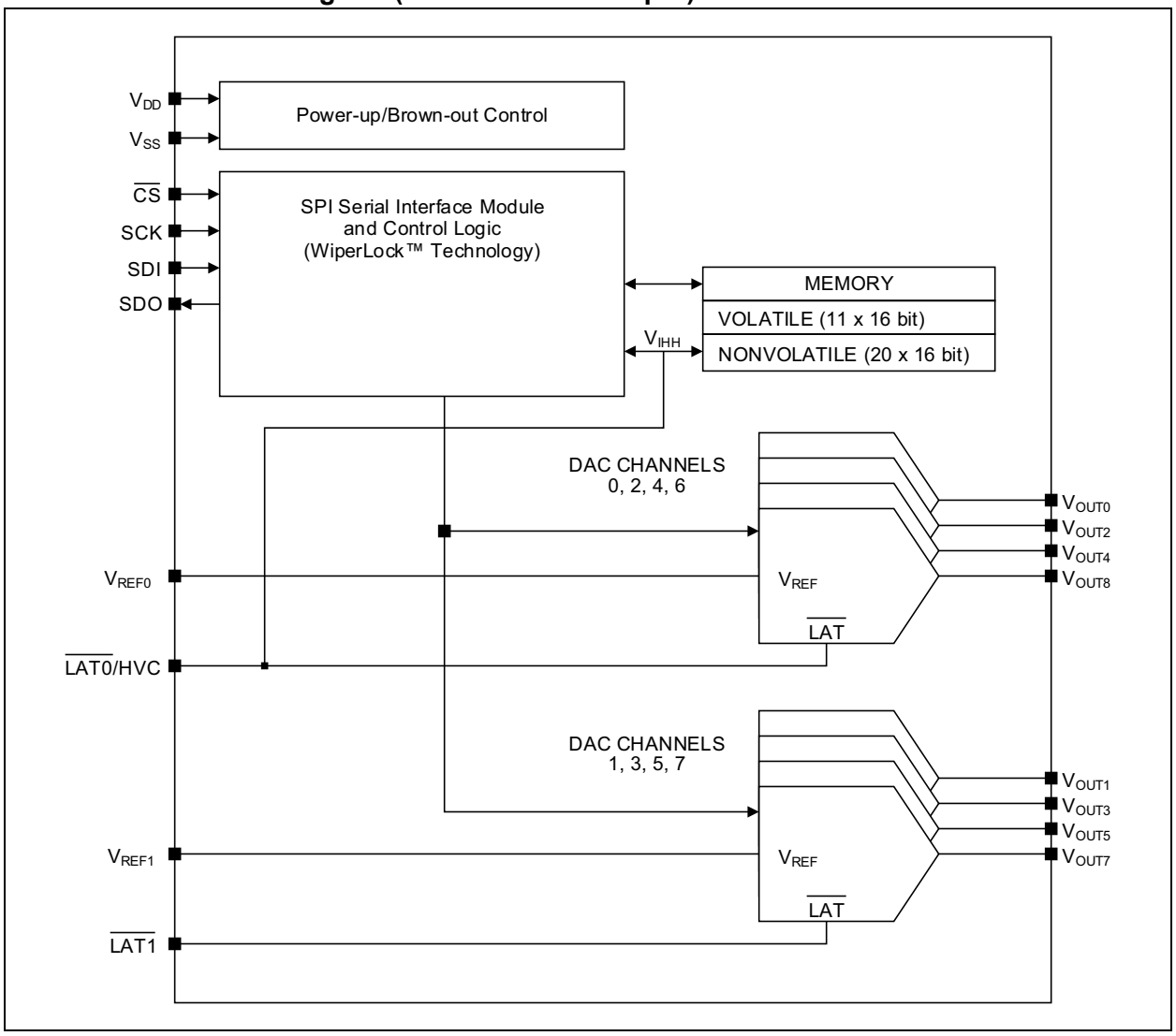
MCP48CXBX4 Block Diagram (Quad-Channel Output)



MCP48CXBX8 Block Diagram (Octal-Channel Output)



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Family Device Features

Device	Package Type	# of Channels	Resolution (bits)	DAC Output POR/BOR Setting(1)	# of V_{REF} Inputs	# of $\overline{LAT}$ Inputs	Memory(2)	GP MTP Locations
MCP48CVB04	TSSOP, QFN	4	8	7Fh	2	2	RAM	—
MCP48CVB14	TSSOP, QFN	4	10	1FFh	2	2	RAM	—
MCP48CVB24	TSSOP, QFN	4	12	7FFh	2	2	RAM	—
MCP48CVB08	TSSOP, QFN	8	8	7Fh	2	2	RAM	—
MCP48CVB18	TSSOP, QFN	8	10	1FFh	2	2	RAM	—
MCP48CVB28	TSSOP, QFN	8	12	7FFh	2	2	RAM	—
MCP48CMB04	TSSOP, QFN	4	8	7Fh	2	2	MTP	8
MCP48CMB14	TSSOP, QFN	4	10	1FFh	2	2	MTP	8
MCP48CMB24	TSSOP, QFN	4	12	7FFh	2	2	MTP	8
MCP48CMB08	TSSOP, QFN	8	8	7Fh	2	2	MTP	8
MCP48CMB18	TSSOP, QFN	8	10	1FFh	2	2	MTP	8
MCP48CMB28	TSSOP, QFN	8	12	7FFh	2	2	MTP	8

Note 1: The factory default value.

2: Each nonvolatile memory location can be written 32 times. For subsequent writes to the MTP, the device will ignore the commands and the memory will not be modified.

NOTES:

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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

Voltage on V_{DD} with Respect to V_{SS} ..... -0.6V to +6.5V
Voltage on all Pins with Respect to V_{SS} ..... -0.6V to V_{DD} + 0.3V
Input Clamp Current, I_{IK} ($V_I < 0$, $V_I > V_{DD}$, $V_I > V_{PP}$ on HV Pins) .....±20 mA
Output Clamp Current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$) .....±20 mA
Maximum Current out of the V_{SS} Pin (Quad) .....50 mA
(Octal) .....100 mA
Maximum Current into the V_{DD} Pin (Quad) .....50 mA
(Octal) .....100 mA
Maximum Current Sourced by the V_{OUT} Pin .....20 mA
Maximum Current Sunk by the V_{OUT} Pin .....20 mA
Maximum Current Sourced/Sunk by the $V_{REF(0)}$ Pin (in Band Gap mode) .....20 mA
Maximum Current Sunk by the V_{REFX} Pin (when V_{REF} is in Unbuffered mode) .....350 µA
Maximum Current Sourced by the V_{REFX} Pin .....20 µA
Maximum Current Sunk by the V_{REF} Pin .....125 µA
Maximum Output Current Sourced/Sunk by the SDO Output Pin .....25 mA
Total Power Dissipation(1) .....400 mW
ESD Protection on all Pins .....≥ ±8 kV (HBM)
.....≥ ±400V (MM)
.....≥ ±2 kV (CDM)
Latch-Up (per JEDEC® JESD78A) at +125°C .....±100 mA
Storage Temperature .....-65°C to +150°C
Ambient Temperature with Power Applied .....-55°C to +125°C
Soldering Temperature of Leads (10 seconds) ..... +300°C
Maximum Junction Temperature (T_J) ..... +150°C

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Power dissipation is calculated as follows:
$P_{DIS} = V_{DD} \times \{I_{DD} - \Sigma I_{OH}\} + \Sigma \{(V_{DD} - V_{OH}) \times I_{OH}\} + \Sigma(V_{OL} \times I_{OL})$

DC CHARACTERISTICS

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended)
All parameters apply across the specified operating ranges, unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF} = +1.000V to V_{DD}, V_{SS} = 0V, R_L = 2 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	V_{DD}	2.7	—	5.5	V	
		1.8	—	2.7	V	DAC operation (reduced analog specifications) and serial interface
V_{DD} Voltage (Rising) to Ensure Device Power-on Reset	V_{POR}	—	—	1.75	V	RAM retention voltage: (V_{RAM}) < V_{POR}, V_{DD} voltages greater than the V_{POR} limit ensure that the device is out of reset
V_{DD} Voltage (Falling) to Ensure Device Brown-out Reset	V_{BOR}	V_{RAM}	—	1.61	V	RAM retention voltage: (V_{RAM}) < V_{BOR}
V_{DD} Rise Rate to Ensure POR	V_{DDRR}	**Note 3**			V/ms	
POR to Output-Driven Delay(1)	T_{POR2OD}	—	—	175	µs	V_{DD} rising, V_{DD} > V_{POR}, quad output
		—	—	265	µs	V_{DD} rising, V_{DD} > V_{POR}, octal output

Note 1 This parameter is ensured by design.

Note 3 POR/BOR voltage trip point is not slope-dependent. Hysteresis is implemented with time delay.

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DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended)
All parameters apply across the specified operating ranges, unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF} = +1.000V to V_{DD}, V_{SS} = 0V, R_L = 2 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions		
Supply Current	I_{DD}	—	—	550	µA	Quad	1 MHz	Serial interface active, VRnB:VRnA = 10[4], V_{OUT} is unloaded, V_{REF} = V_{DD} = 5.5V, Volatile DAC register = Mid-Scale
		—	—	940			10 MHz[2]	
		—	—	2030			50 MHz[2]	
		—	—	890		Octal	1 MHz	
		—	—	1270			10 MHz[2]	
		—	—	2400			50 MHz[2]	
		—	—	410		Quad	Serial interface inactive, VRnB:VRnA = 10, V_{OUT} is unloaded, V_{REF} = V_{DD} = 5.5V, Volatile DAC register = Mid-Scale	
		—	—	720		Octal		
$\overline{LAT}$/HVC Pin Write Current[1]	$I_{DD(MTP\_WR)}$	—	—	6.40	mA	—	Serial interface inactive (MTP write active), VRnB:VRnA = 10 (valid for all modes), V_{DD} = 5.5V, $\overline{LAT}$/HVC = V_{IHH}, write all '1's to nonvolatile DAC0, V_{OUT} pins are unloaded	
Power-Down Current	I_{DDP}	—	0.54	2.40	µA	—	PDnB:PDnA = 01[5], VRnB:VRnA = 10, V_{OUT} not connected	

Note 2 This parameter is ensured by characterization.

Note 4 Supply current is independent of current through the resistor ladder in mode VRnB:VRnA = 10.

Note 5 The PDnB:PDnA = 01, 10 and 11 configurations must have the same current.

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DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended)
All parameters apply across the specified operating ranges, unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF} = +1.000V to V_{DD}, V_{SS} = 0V, R_L = 2 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions	
Resistor Ladder Resistance[6]	R_L	62.475	73.5	84.525	kΩ	VRnB:VRnA = 10, V_{REF} = V_{DD}	
Resolution (# of resistors and # of taps), (see **B.1, "Resolution"**)	N	256			Taps	8-bit	No missing codes
		1024			Taps	10-bit	No missing codes
		4096			Taps	12-bit	No missing codes
Nominal V_{OUT} Match[10]	$\lvert V_{OUT} - V_{OUTMEAN}\rvert / V_{OUTMEAN}$	—	0.026	0.300	%	1.8V ≤ V_{DD} ≤ 5.5V[2]	
V_{OUT} Temperature Coefficient[2] (see **B.19, "V_{OUT} Temperature Coefficient"**)	$\Delta V_{OUT}/\Delta T$	—	3	—	ppm/°C	Code = Mid-Scale, VRnB:VRnA = 00, 10 and 11	
V_{REF} Pin Input Voltage Range[1]	V_{REF}	V_{SS}	—	V_{DD}	V	1.8V ≤ V_{DD} ≤ 5.5V	

Note 1 This parameter is ensured by design.

Note 2 This parameter is ensured by characterization.

Note 6 Resistance is defined as the resistance between the V_{REF} pin (mode VRnB:VRnA = 10) and the V_{SS} pin. This is the effective resistance of each resistor ladder. The resistance measurement is one of the resistor ladders measured in parallel.

Note 10 Variation of one output voltage to mean output voltage.

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DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended)
All parameters apply across the specified operating ranges, unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF} = +1.000V to V_{DD}, V_{SS} = 0V, R_L = 2 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions	
Zero-Scale Error (Code = 000h) (see **B.4, "Zero-Scale Error (E_{ZS})"**)	E_{ZS}	—	—	0.5	LSb	8-bit	VRnB:VRnA = 10, G = 0, V_{REF} = V_{DD}, no load
		—	—	2	LSb	10-bit	VRnB:VRnA = 10, G = 0, V_{REF} = V_{DD}, no load
		—	—	8	LSb	12-bit	VRnB:VRnA = 10, G = 0, V_{REF} = V_{DD}, no load
Offset Error (see **B.6, "Offset Error (E_{OS})"**)	E_{OS}	-9	±1.1	+9	mV	VRnB:VRnA = 10, Gn = 0, no load, 8-bit: Code = 4; 10-bit: Code = 16; 12-bit: Code = 64	
Offset Voltage Temperature Coefficient[2, 9]	V_{OSTC}	—	±9	—	µV/°C		
Full-Scale Error (see **B.5, "Full-Scale Error (E_{FS})"**)	E_{FS}	—	—	0.625	LSb	8-bit	VRnB:VRnA = 10, G = 0, V_{REF} = V_{DD}, no load
		—	—	2.5	LSb	10-bit	VRnB:VRnA = 10, G = 0, V_{REF} = V_{DD}, no load
		—	—	10	LSb	12-bit	VRnB:VRnA = 10, G = 0, V_{REF} = V_{DD}, no load
Gain Error (see **B.8, "Gain Error (E_G)"**)[7]	E_G	-0.6	±0.1	+0.6	% of FSR	8-bit	VRnB:VRnA = 10, G = 0, Code = 252, V_{REF} = V_{DD}, no load
		-0.6	±0.1	+0.6	% of FSR	10-bit	VRnB:VRnA = 10, G = 0, Code = 1008, V_{REF} = V_{DD}, no load
		-0.6	±0.1	+0.6	% of FSR	12-bit	VRnB:VRnA = 10, G = 0, Code = 4032, V_{REF} = V_{DD}, no load
Gain Error Drift[2, 9] (see **B.9, "Gain Error Drift (EG_D)"**)	ΔG/°C	—	-10	—	ppm/°C		

Note 2 This parameter is ensured by characterization.

Note 7 This gain error does not include the offset error.

Note 9 Code range dependent on resolution: 8-bit, codes 4 to 252; 10-bit, codes 16 to 1008; 12-bit, codes 64 to 4032.

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DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended)
All parameters apply across the specified operating ranges, unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF} = +1.000V to V_{DD}, V_{SS} = 0V, R_L = 2 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units		Conditions
Total Unadjusted Error[2, 9] (see **B.10, "Total Unadjusted Error (E_T)"**)	E_T	-1.375	—	0.625	LSb	8-bit	VRnB:VRnA = 10, G = 0, V_{REF} = V_{DD}, no load
		-5.5	—	2.5	LSb	10-bit	VRnB:VRnA = 10, G = 0, V_{REF} = V_{DD}, no load
		-22	—	10	LSb	12-bit	VRnB:VRnA = 10, G = 0, V_{REF} = V_{DD}, no load
		See **Section 2.0, "Typical Performance Curves"**			LSb		VRnB:VRnA = 10, G = 1, V_{REF} = 0.5 × V_{DD}, no load
		See **Section 2.0, "Typical Performance Curves"**			LSb		VRnB:VRnA = 01, G = 0, G = 1, V_{DD} = 1.8V-5.5V, no load
Integral Nonlinearity (see **B.11, "Integral Nonlinearity (INL)"**)[9]	INL	-0.1	—	+0.1	LSb	8-bit	VRnB:VRnA = 10, G = 0, V_{REF} = V_{DD}, no load
		-0.25	—	+0.25	LSb	10-bit	VRnB:VRnA = 10, G = 0, V_{REF} = V_{DD}, no load
		-1	—	+1	LSb	12-bit	VRnB:VRnA = 10, G = 0, V_{REF} = V_{DD}, no load
		See **Section 2.0, "Typical Performance Curves"**			LSb		VRnB:VRnA = 10, G = 1, V_{REF} = 0.5 × V_{DD}, no load
		See **Section 2.0, "Typical Performance Curves"**			LSb		VRnB:VRnA = 01, G = 0, G = 1, V_{DD} = 1.8V-5.5V, no load
Differential Nonlinearity (see **B.12, "Differential Nonlinearity (DNL)"**)[9]	DNL	-0.1	—	+0.1	LSb	8-bit	VRnB:VRnA = 10, G = 0, V_{REF} = V_{DD}, no load
		-0.25	—	+0.25	LSb	10-bit	VRnB:VRnA = 10, G = 0, V_{REF} = V_{DD}, no load
		-1.0	—	+1.0	LSb	12-bit	VRnB:VRnA = 10, G = 0, V_{REF} = V_{DD}, no load
		See **Section 2.0, "Typical Performance Curves"**			LSb		VRnB:VRnA = 10, G = 1, V_{REF} = 0.5 × V_{DD}, no load
		See **Section 2.0, "Typical Performance Curves"**			LSb		VRnB:VRnA = 01, G = 0, G = 1, V_{DD} = 1.8V-5.5V, no load

Note 2 This parameter is ensured by characterization.

Note 9 Code range dependent on resolution: 8-bit, codes 4 to 252; 10-bit, codes 16 to 1008; 12-bit, codes 64 to 4032.

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DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended)
All parameters apply across the specified operating ranges, unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF} = +1.000V to V_{DD}, V_{SS} = 0V, R_L = 2 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions	
-3 dB Bandwidth (see **B.16, "-3 dB Bandwidth"**)	BW	—	270	—	kHz	V_{REF} = 3.00V ± 2V, VRnB:VRnA = 10, Gn = 0	
		—	170	—		V_{REF} = 3.50V ± 1.5V, VRnB:VRnA = 10, Gn = 1	
Output Amplifier (Op Amp)							
Phase Margin(1)	PM	—	76	—	°C	R_L = ∞	
Slew Rate	SR	—	0.7	—	V/µs	R_L = 2 kΩ	
Load Regulation	—	—	147	—	µV/mA	1 mA ≤ I ≤ 6 mA	V_{DD} = 5.5V, DAC code = Mid-Scale
		—	176	—	µV/mA	-6 mA ≤ I ≤ -1 mA	
Short-Circuit Current	I_{SC_OA}	6	10	14	mA	Short to V_{SS}	DAC code = Full Scale
		6	10	14	mA	Short to V_{DD}	DAC code = Zero Scale
Settling Time(8)	$t_{SETTLING}$	—	4	—	µs	R_L = 2 kΩ	
Internal Band Gap							
Band Gap Voltage	V_{BG}	1.180	1.214	1.260	V	1.8V ≤ V_{DD} ≤ 5.5V	
Short-Circuit Current	I_{SC_BG}	6	10	14	mA	Short to V_{SS}	
		6	10	14	mA	Short to V_{DD}	
Band Gap Voltage Temperature Coefficient	V_{BGTC}	—	18	—	ppm/°C	1.8V ≤ V_{DD} ≤ 5.5V	
Band Gap Mode, V_{REF} Pin Load Regulation	I_{BG}	—	38	—	µV/mA	1 mA ≤ I ≤ 6 mA	V_{DD} = 5.5V
		—	363	—	µV/mA	-6 mA ≤ I ≤ -1 mA	

Note 1 This parameter is ensured by design.

Note 8 Within 1/2 LSb of the final value, when code changes from 1/4 to 3/4 of FSR (Example: 400h to C00h in a 12-bit device).

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DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended)
All parameters apply across the specified operating ranges, unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF} = +1.000V to V_{DD}, V_{SS} = 0V, R_L = 2 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
External Reference (V_{REF})						
Input Range(1)	V_{REF}	V_{SS}	—	V_{DD}	V	VRnB:VRnA = 10 (Unbuffered mode)
Input Capacitance	C_{REF}	—	29	—	pF	VRnB:VRnA = 10 (Unbuffered mode)
Input Impedance	R_L	See **Resistor Ladder Resistance(6)**			kΩ	2.7V ≤ V_{DD} ≤ 5.5V, VRnB:VRnA = 10, V_{REF} = V_{DD}
Current through V_{REF}(1)	I_{VREF}	—	—	353.1	µA	Mathematically from $R_{VREF(min)}$ spec (at 5.5V)
Total Harmonic Distortion(1)	THD	—	-76	—	dB	V_{REF} = 2.048V ± 0.1V, VRnB:VRnA = 10, Gn = 0, Frequency = 1 kHz
Dynamic Performance						
Major Code Transition Glitch (see **B.14, "Major Code Transition Glitch"**)	—	—	60	—	nV-s	1 LSb change around major carry (7FFh to 800h)
Digital Feedthrough (see **B.15, "Digital Feedthrough"**)	—	—	< 2	—	nV-s	

Note 1 This parameter is ensured by design.

Note 6 Resistance is defined as the resistance between the V_{REF} pin (mode VRnB:VRnA = 10) and the V_{SS} pin. This is the effective resistance of each resistor ladder. The resistance measurement is one of the resistor ladders measured in parallel.

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DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended)
All parameters apply across the specified operating ranges, unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF} = +1.000V to V_{DD}, V_{SS} = 0V, R_L = 2 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions	
Digital Inputs/Outputs ($\overline{CS}$, SDI, SDO, SCK, $\overline{LATn}$)							
Schmitt Trigger High-Input Threshold	V_{IH}	0.45 V_{DD}	—	—	V	1.8V ≤ V_{DD} ≤ 5.5V (Allows 2.7V Digital V_{DD} with 5.5V Analog V_{DD} or 1.8V Digital V_{DD} with 3.0V Analog V_{DD})	
Schmitt Trigger Low-Input Threshold	V_{IL}	—	—	0.2 V_{DD}	V		
Hysteresis of Schmitt Trigger Inputs	V_{HYS}	—	0.1 V_{DD}	—	V		
Output Low Voltage (SDO)	V_{OL}	V_{SS}	—	0.3 V_{DD}	V	I_{OL} = 200 µA	
Output High Voltage (SDO)	V_{OH}	0.7 V_{DD}	—	V_{DD}	V	I_{OH} = -200 µA	
Input Leakage Current	I_{IL}	-1	—	1	µA	V_{IN} = V_{DD} and V_{IN} = V_{SS}	
Pin Capacitance	C_{IN}, C_{OUT}	—	10	—	pF		
RAM Value							
Value Range	N	0h	—	FFh	Hex	8-bit	
			—	3FFh		10-bit	
			—	FFFh		12-bit	
DAC Register POR/BOR Value	N	See Table 4-2			Hex	8-bit	
						10-bit	
						12-bit	
PDCON Initial Factory Setting	—	See Table 4-2			Hex		
Power Requirements							
Power Supply Sensitivity	PSS	—	0.0010	0.0070	%/%	8-bit	Code = Mid-Scale
		—				10-bit	
		—				12-bit	

DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended)
All parameters apply across the specified operating ranges, unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF} = +1.000V to V_{DD}, V_{SS} = 0V, R_L = 2 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Multi-Time Programming Memory (MTP)						
MTP Programming Voltage(1)	V_{PG_MTP}	2.0	—	5.5	V	HVC = V_{IHH}, -20°C ≤ T_A ≤ +125°C
$\overline{LAT}$/HVC Pin Voltage for MTP Programming (high-voltage commands)	V_{IHH}	7.25	7.5	7.75V	V	The $\overline{LAT}$/HVC pin will be at one of the three input levels (V_{IL}, V_{IH} or V_{IHH})(1, 11) The $\overline{LAT}$/HVC pin must supply the required MTP programming current (up to 6.4 mA)
Writes Cycles	—	—	—	32(12)	Cycles	**Note 1**
Data Retention	DR_{MTP}	10	—	—	Years	At +125°C(1)
MTP Range	N	0h	—	FFh	Hex	8-bit
		0h	—	3FFh	Hex	10-bit
		0h	—	FFFh	Hex	12-bit
		0000h		7FFFh	Hex	All general purpose memory
Initial Factory Setting	N	See Table 4-2			—	
MTP Programming Write Cycle Time(1)	$t_{WC(MTP)}$	—	—	250	µs	V_{DD} = +2.0V to 5.5V, -20°C ≤ T_A ≤ +125°C

Note 1 This parameter is ensured by design.

Note 11 High-voltage on the LAT/HVC pin must be limited to the command plus programming time. After the programming cycle, the LAT/HVC pin voltage must be returned to 5.5V or lower.

Note 12 After 32 MTP write cycles, writes are inhibited and the 32nd write value is retained (not corrupted).

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DC Notes:

1. This parameter is ensured by design.
2. This parameter is ensured by characterization.
3. POR/BOR voltage trip point is not slope-dependent. Hysteresis is implemented with time delay.
4. Supply current is independent of current through the resistor ladder in mode VRnB:VRnA = `10`.
5. The PDnB:PDnA = `01`, `10` and `11` configurations must have the same current.
6. Resistance is defined as the resistance between the V_{REF} pin (mode VRnB:VRnA = `10`) and the V_{SS} pin. This is the effective resistance of each resistor ladder. The resistance measurement is one of the resistor ladders measured in parallel.
7. This gain error does not include the offset error.
8. Within 1/2 LSb of the final value, when code changes from 1/4 to 3/4 of FSR (Example: 400h to C00h in a 12-bit device).
9. Code range dependent on resolution: 8-bit, codes 4 to 252; 10-bit, codes 16 to 1008; 12-bit, codes 64 to 4032.
10. Variation of one output voltage to mean output voltage.
11. High-voltage on the $\overline{LAT}$/HVC pin must be limited to the command plus programming time. After the programming cycle, the $\overline{LAT}$/HVC pin voltage must be returned to 5.5V or lower.
12. After 32 MTP write cycles, writes are inhibited and the 32nd write value is retained (not corrupted).

1.1 Timing Waveforms and Requirements

1.1.1 WIPER SETTLING TIME

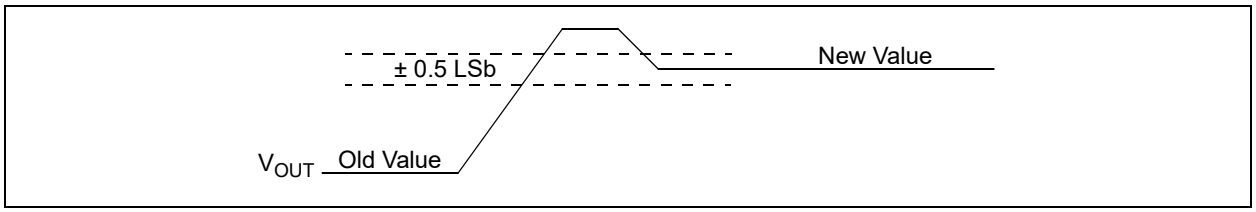

FIGURE 1-1: *V_{OUT} Settling Time Waveforms.*

TABLE 1-1: WIPER SETTLING TIMING

Timing Characteristics		**Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) All parameters apply across the specified operating ranges, unless noted. V_{DD} = +2.7V to 5.5V, V_{SS} = 0V, R_L = 2 kΩ from V_{OUT} to GND, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
V_{OUT} Settling Time (see **B.13, "Settling Time"**)	t_S	—	4	—	µs	12-bit	Code = 400h → C00h; C00h → 400h**(3)**

Note 3 Within 1/2 LSb of final value when the code changes from 1/4 to 3/4 of FSR.

1.1.2 LATCH PIN ($\overline{LAT}$) TIMING

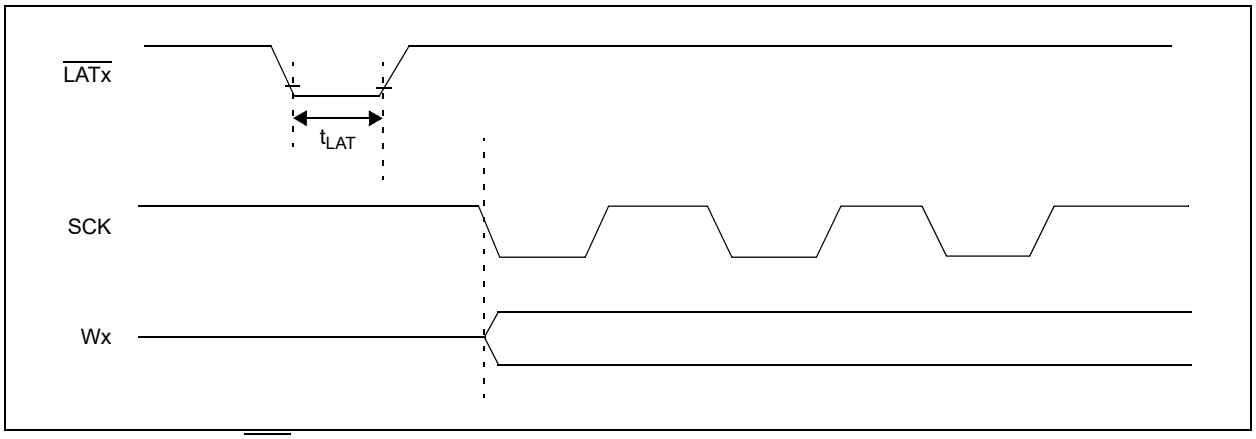

FIGURE 1-2: *$\overline{LAT}$ Pin Waveforms.*

TABLE 1-2: $\overline{LAT}$ PIN TIMING

Timing Characteristics		**Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) All parameters apply across the specified operating ranges, unless noted. V_{DD} = +2.7V to 5.5V, V_{SS} = 0V, RL = 2 kΩ from V_{OUT} to GND, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.				
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
$\overline{LATx}$ Pin Pulse Width	t_{LAT}	20	—	—	ns	

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1.2 SPI Mode Timing Waveforms and Requirements

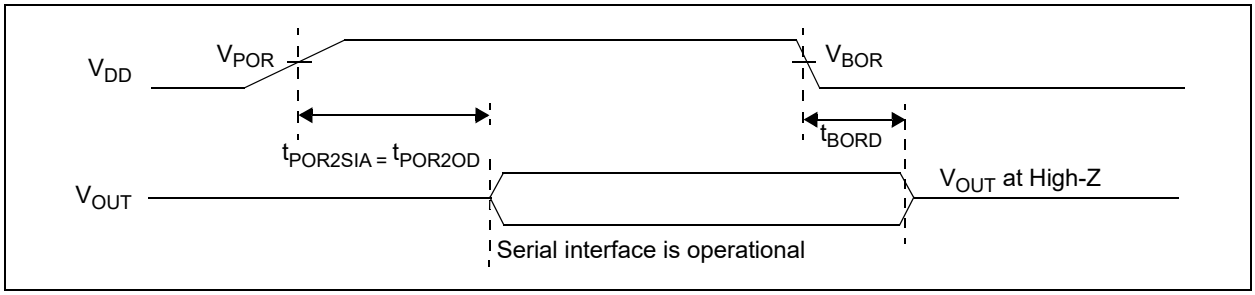

FIGURE 1-3: *Power-on and Brown-out Reset Waveforms.*

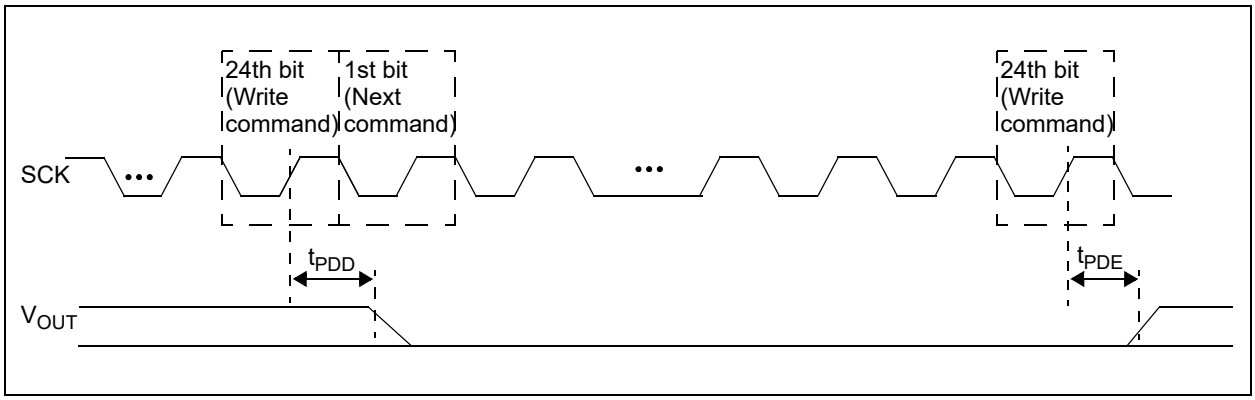

FIGURE 1-4: *SPI Power-Down Command Timing.*

TABLE 1-3: RESET TIMING

Timing Characteristics		**Standard Operating Conditions (unless otherwise specified)**: Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) All parameters apply across the specified operating ranges, unless noted. V_{DD} = +2.7V to 5.5V, V_{SS} = 0V, R_L = 2 kΩ from V_{OUT} to GND, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
Power-on Reset Delay(1)	$t_{POR2SIA}$	—	—	175	µs	Quad	V_{DD} transitions from $V_{DD(MIN)} \rightarrow > V_{POR}$; V_{OUT} disabled to V_{OUT} driven
		—	—	265		Octal	
Brown-out Reset Delay	t_{BORD}	—	30	—	µs	V_{DD} transitions from $V_{DD(MIN)} \rightarrow V_{DD} > V_{POR}$, V_{OUT} driven to V_{OUT} disabled	
Power-Down Output Disable Time Delay	T_{PDD}	—	0.02	—	µs	PDnB:PDnA = 00 → 11, 10 or 01 started from the rising edge of the 24th SCK clock cycle; V_{OUT} = V_{OUT} – 10 mV, V_{OUT} not connected	
Power-Down Output Enable Time Delay	T_{PDE}	—	7	—	µs	PDnB:PDnA = 11, 10, or 01 → 00 started from the rising edge of the 24th SCK clock cycle; Volatile DAC register = FFFh, V_{OUT} = 10 mV, V_{OUT} not connected	

Note 1 Not tested, ensured by design.

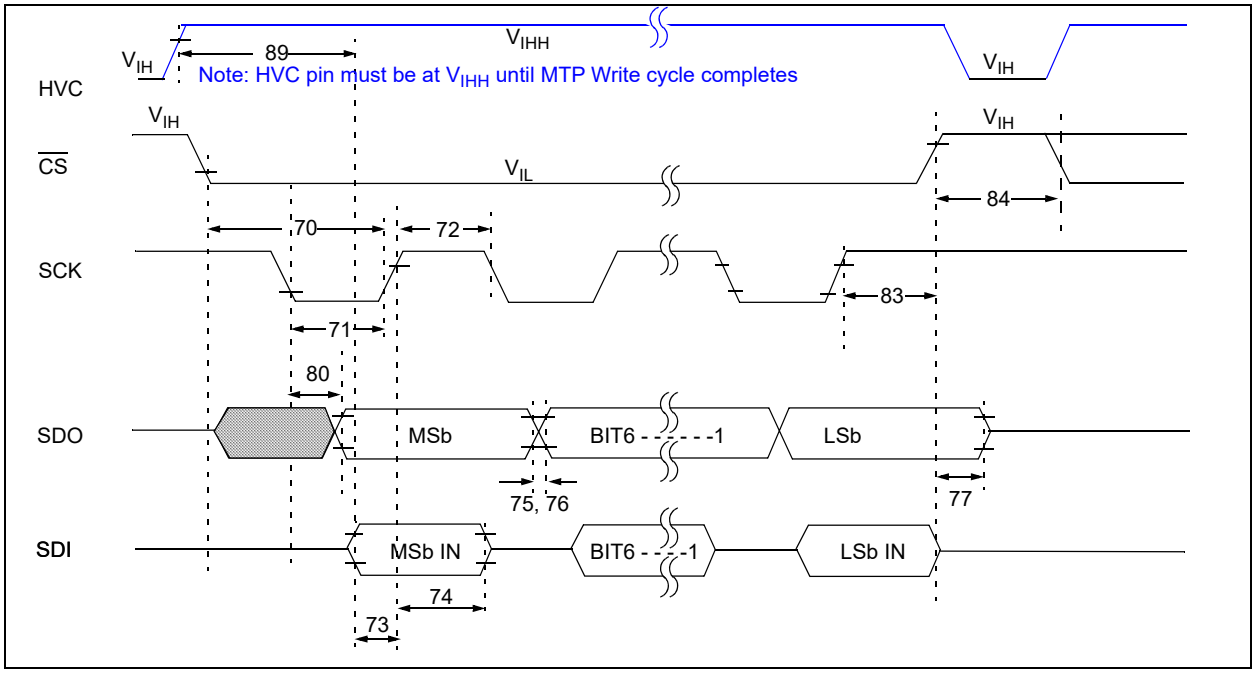

FIGURE 1-5: *SPI Timing Waveform (Mode = 11).*

TABLE 1-4: SPI REQUIREMENTS (MODE = 11)

#	Characteristic[2]	Sym.	Min.	Max.	Units	Conditions
—	SCK Input Frequency	F_{SCK}	—	25	MHz	V_{DD} = 2.7V to 5.5V Read command, C_L = 20 pF
			—	50	MHz	V_{DD} = 2.7V to 5.5V write command, C_L = 20 pF
			—	10	MHz	V_{DD} = 1.8V to 2.7V
70	$\overline{CS}$ Active (V_{IL}) to SCK↑ Input	$T_{CSA2SCH}$	15	—	ns	
71	SCK Input High Time	T_{SCH}	10	—	ns	V_{DD} = 2.7V to 5.5V
			20	—	ns	V_{DD} = 1.8V to 2.7V
72	SCK Input Low Time	T_{SCL}	10	—	ns	V_{DD} = 2.7V to 5.5V
			20	—	ns	V_{DD} = 1.8V to 2.7V
73	SDI Input Valid to SCK↑ Edge (Setup Time)	$T_{DIV2SCH}$	5	—	ns	
74	SCK↑ Edge to SDI Input Invalid (Hold Time)	$T_{SCH2DIL}$	10	—	ns	
77	$\overline{CS}$ Inactive (V_{IH}) to SDO Output High-Impedance	$T_{CSH2DOZ}$	—	20	ns	**Note 1**
80	SCK↓ Edge to SDO Data Output Valid	$T_{SCL2DOV}$	—	20	ns	V_{DD} = 2.7V to 5.5V
			—	35	ns	V_{DD} = 1.8V to 2.7V
83	SCK↑ Edge to $\overline{CS}$ Inactive (V_{IH}) (Hold Time)	$T_{SCH2CSI}$	15	—	ns	V_{DD} = 2.7V to 5.5V
			20	—	ns	V_{DD} = 1.8V to 2.7V
84	$\overline{CS}$ Input High Time	$T_{CSA2CSI}$	30	—	ns	
89	Delay from HVC V_{IHH} to First Command Byte[1]	—	0	—	ns	

Note 1 This specification is ensured by design.
Note 2 This parameter is ensured by characterization.

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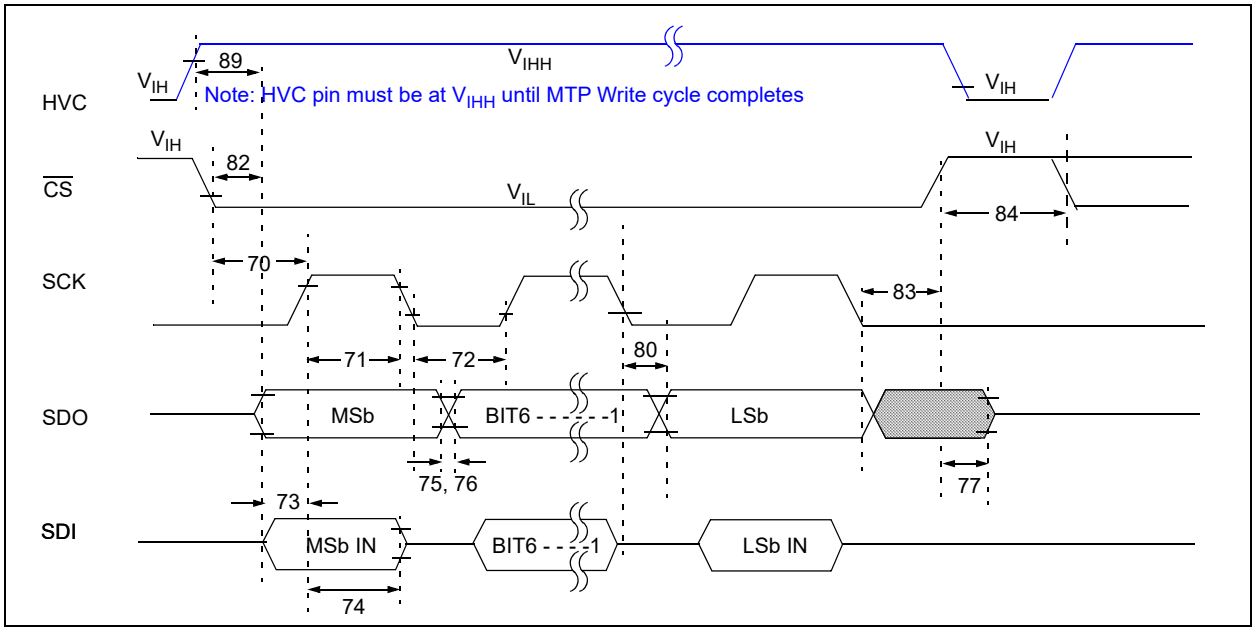

FIGURE 1-6: *SPI Timing Waveform (Mode = 00).*

TABLE 1-5: SPI REQUIREMENTS (MODE = 00)

#	Characteristic[2]	Sym.	Min.	Max.	Units	Conditions
—	SCK Input Frequency	F_{SCK}	—	25	MHz	V_{DD} = 2.7V to 5.5V Read command, C_L = 20 pF
			—	50	MHz	V_{DD} = 2.7V to 5.5V write command, C_L = 20 pF
			—	10	MHz	V_{DD} = 1.8V to 2.7V
70	$\overline{CS}$ Active (V_{IL} or V_{IHH}) to SCK↑ Input	$T_{CSA2SCH}$	15	—	ns	
71	SCK Input High Time	T_{SCH}	10	—	ns	V_{DD} = 2.7V to 5.5V
			20	—	ns	V_{DD} = 1.8V to 2.7V
72	SCK Input Low Time	T_{SCL}	10	—	ns	V_{DD} = 2.7V to 5.5V
			20	—	ns	V_{DD} = 1.8V to 2.7V
73	SDI Input Valid to SCK↑ Edge (Setup Time)	$T_{DIV2SCH}$	5	—	ns	
74	SCK↑ Edge to SDI Input Invalid (Hold Time)	$T_{SCH2DIL}$	10	—	ns	
77	$\overline{CS}$ Inactive (V_{IH}) to SDO Output High-Impedance	$T_{CSH2DOZ}$	—	20	ns	**Note 1**
80	SCK↓ Edge to SDO Data Output Valid	$T_{SCL2DOV}$	—	20	ns	V_{DD} = 2.7V to 5.5V
			—	35	ns	V_{DD} = 1.8V to 2.7V
82	$\overline{CS}$ Active (V_{IL}) to SDO Data Output Valid	$T_{CSL2DOV}$	—	20	ns	2.7V to 5.5V
			—	35	ns	1.8V to 2.7V
83	SCK↓ Edge to $\overline{CS}$ Inactive (V_{IH}) (Hold Time)	$T_{SCH2CSI}$	15	—	ns	V_{DD} = 2.7V to 5.5V
			20	—	ns	V_{DD} = 1.8V to 2.7V
84	$\overline{CS}$ Input High Time	$T_{CSA2CSI}$	30	—	ns	
89	Delay from HVC V_{IHH} to First Command Byte[1]	—	0	—	ns	

Note 1 This specification is ensured by design.
Note 2 This parameter is ensured by characterization.

Timing Notes:

1. Not tested, ensured by design.
2. Not tested, ensured by characterization.
3. Within 1/2 LSb of final value when the code changes from 1/4 to 3/4 of FSR.

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TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.7V to +5.5V, V_{SS} = GND.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 20L-TSSOP	θ_{JA}	—	90	—	°C/W	
Thermal Resistance, 20L-QFN (4 x 4)	θ_{JA}	—	30	—	°C/W	

NOTES:

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

2.1 Device Currents

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

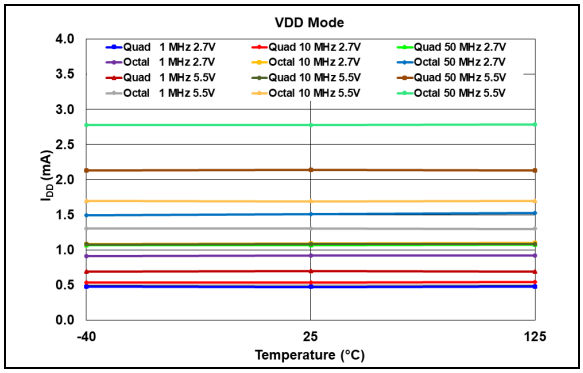

FIGURE 2-1: *Average Supply Current vs. F_{SCK} Frequency, Voltage and Temperature – Active Interface, VRnB:VRnA =* `00`.

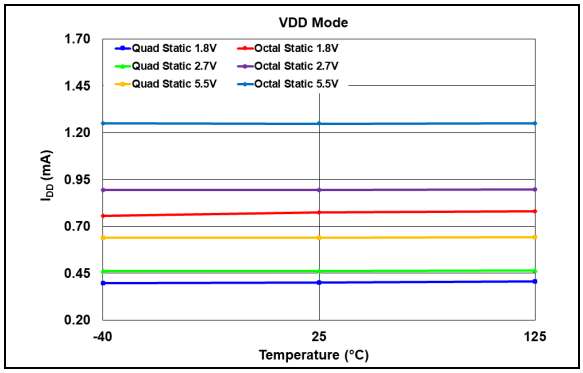

FIGURE 2-4: *Average Supply Current vs. Voltage and Temperature – Inactive Interface (SCK = V_{IH} or V_{IL}), VRnB:VRnA =* `00`.

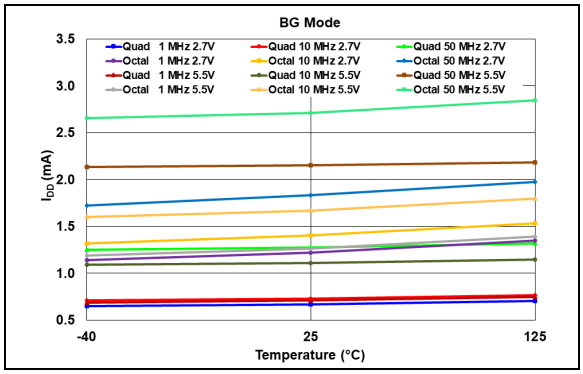

FIGURE 2-2: *Average Supply Current vs. F_{SCK} Frequency, Voltage and Temperature – Active Interface, VRnB:VRnA =* `01`.

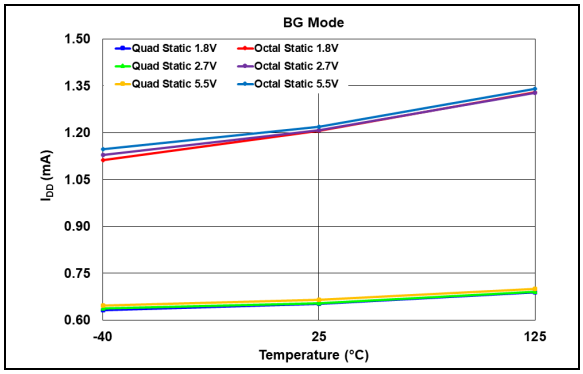

FIGURE 2-5: *Average Supply Current – Inactive Interface (SCK = V_{IH} or V_{IL}) vs. Voltage and Temperature, VRnB:VRnA =* `01`.

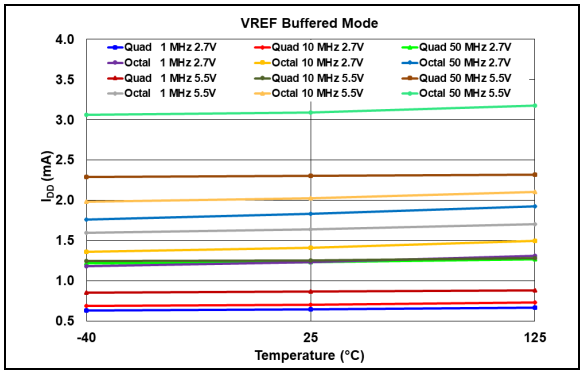

FIGURE 2-3: *Average Supply Current vs. F_{SCK} Frequency, Voltage and Temperature – Active Interface, VRnB:VRnA =* `11`.

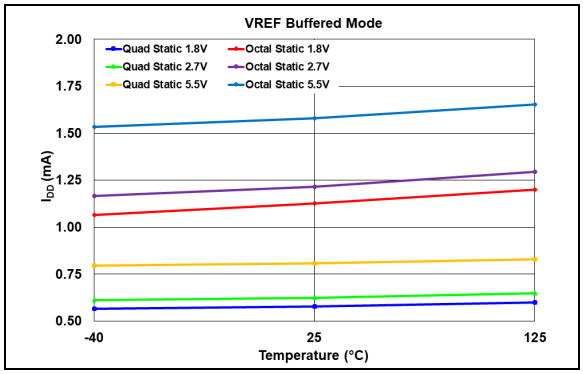

FIGURE 2-6: *Average Supply Current – Inactive Interface (SCK = V_{IH} or V_{IL}) vs. Voltage and Temperature, VRnB:VRnA =* `11`.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

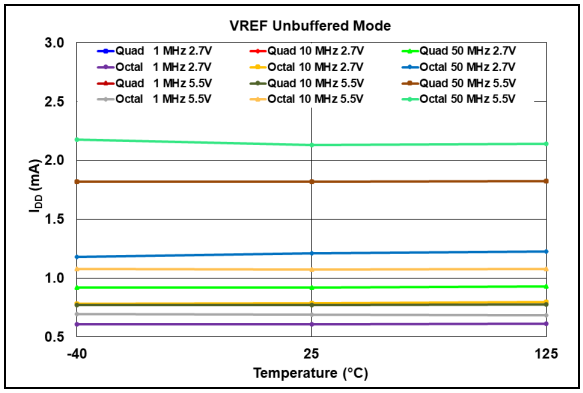

FIGURE 2-7: *Average Device Supply Current vs. F_{SCK} Frequency, Voltage and Temperature – Active Interface, VRnB:VRnA =* `10`*.*

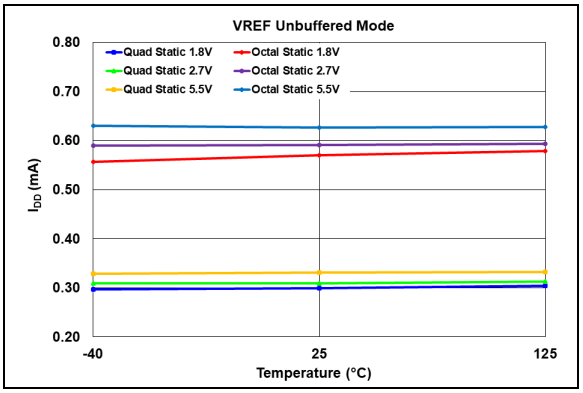

FIGURE 2-9: *Average Device Supply vs. Voltage and Temperature Current – Inactive Interface (SCK = V_{IH} or V_{IL}), VRnB:VRnA =* `10`*.*

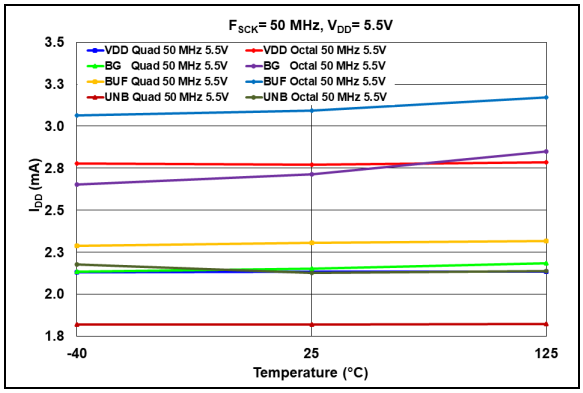

FIGURE 2-8: *Average Device Supply Active Current (I_{DDA}) vs. Temperature and DAC Reference Voltage Mode, V_{DD} = 5.5V and F_{SCK} = 50MHz.*

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2.2 Linearity Data

2.2.1 TOTAL UNADJUSTED ERROR (TUE) – MCP48CXB2X (12-BIT), VRnB:VRnA = 10, $V_{REF} = V_{DD}$, GAIN = 1x, CODE 64-4032

Note: Unless otherwise indicated: T_A = +25°C, V_{DD} = 5.5V.

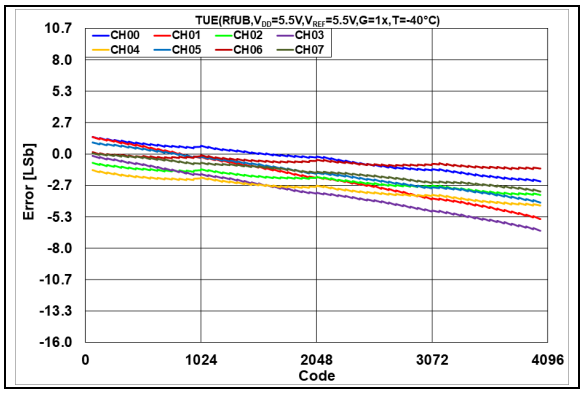

FIGURE 2-10: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 5.5V, T = -40°C.*

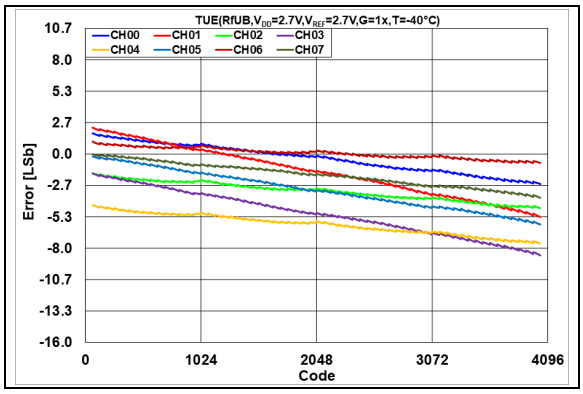

FIGURE 2-13: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 2.7V, T = -40°C.*

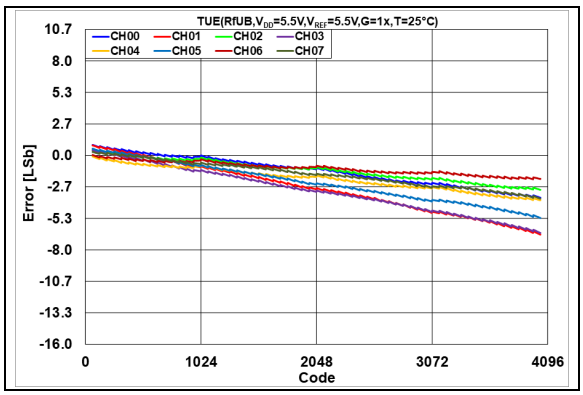

FIGURE 2-11: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 5.5V, T = +25°C.*

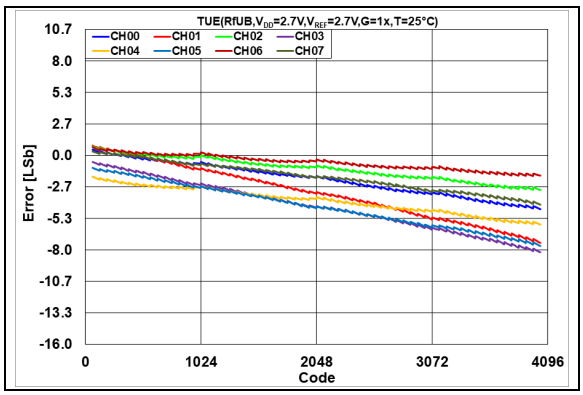

FIGURE 2-14: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 2.7V, T = +25°C.*

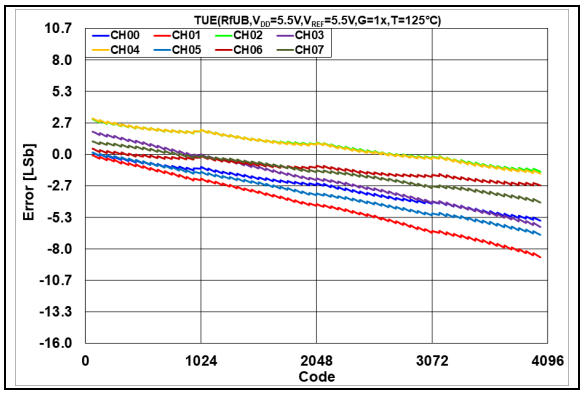

FIGURE 2-12: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 5.5V, T = +125°C.*

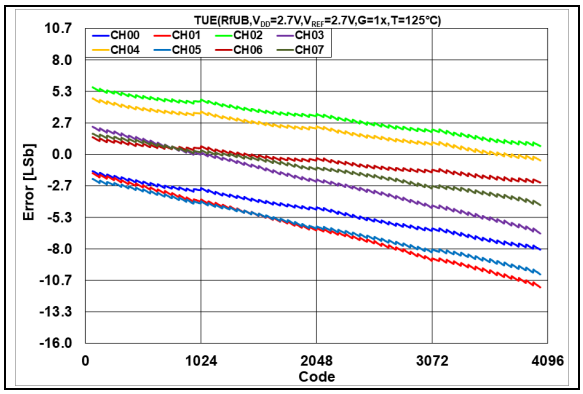

FIGURE 2-15: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 2.7V, T = +125°C.*

Note: Unless otherwise indicated: T_A = +25°C, V_{DD} = 5.5V.

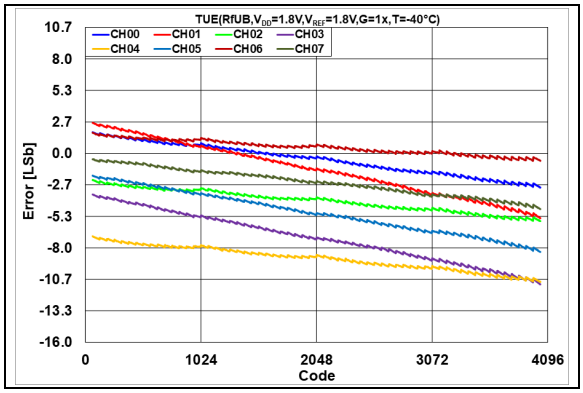

FIGURE 2-16: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 1.8V, T = -40°C.*

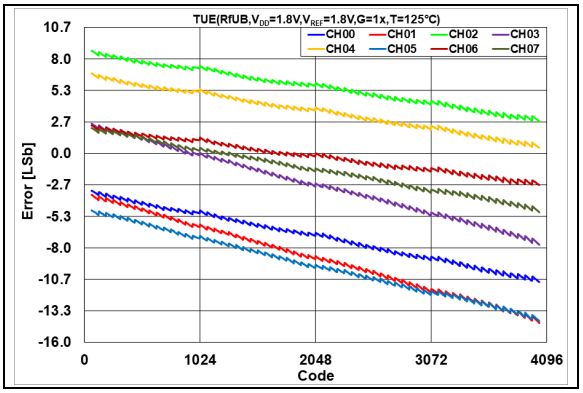

FIGURE 2-18: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 1.8V, T = +125°C.*

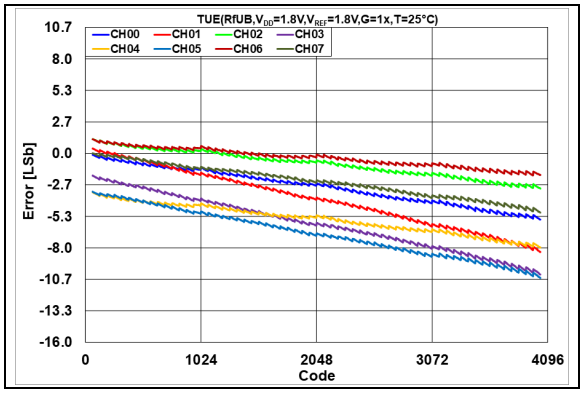

FIGURE 2-17: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 1.8V, T = +25°C.*

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2.2.2 INTEGRAL NONLINEARITY (INL) – MCP48CXB2X (12-BIT), VRnB:VRnA = 10, $V_{REF} = V_{DD}$, GAIN = 1x, CODE 64-4032

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

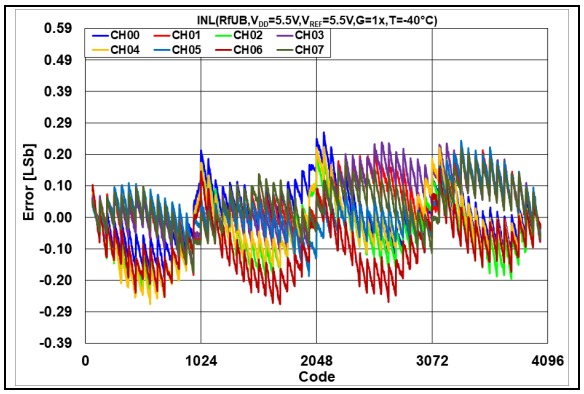

FIGURE 2-19: *INL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, T = -40°C.*

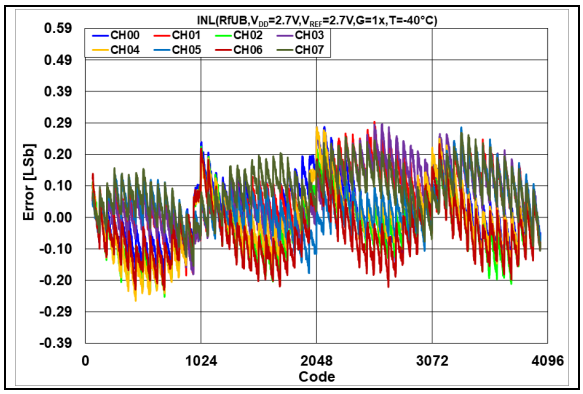

FIGURE 2-22: *INL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, T = -40°C.*

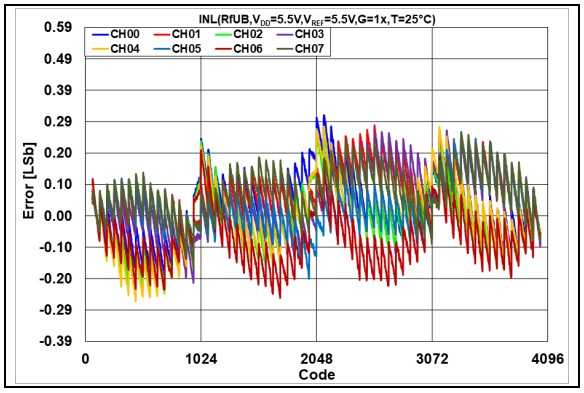

FIGURE 2-20: *INL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, T = +25°C.*

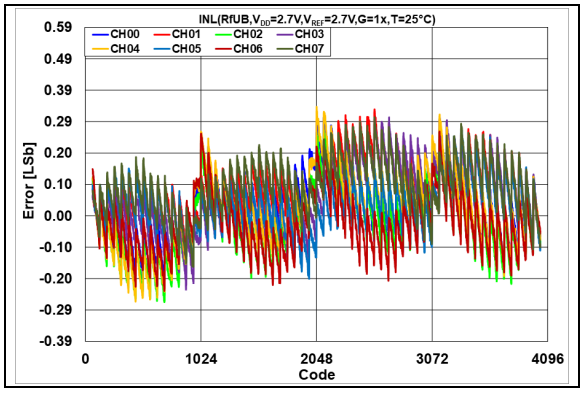

FIGURE 2-23: *INL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, T = +25°C.*

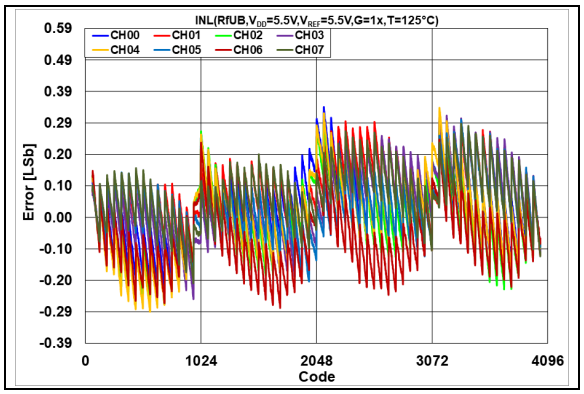

FIGURE 2-21: *INL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, T = +125°C.*

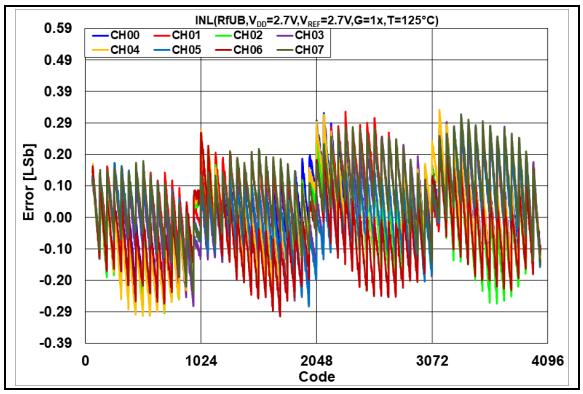

FIGURE 2-24: *INL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, T = +125°C.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

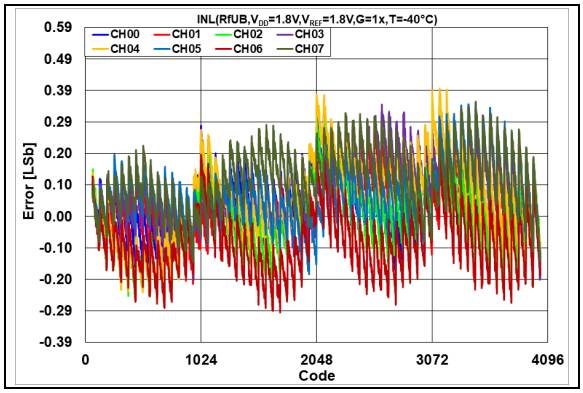

FIGURE 2-25: *INL Error vs. DAC Code and Temperature, V_{DD} = 1.8V, T = -40°C.*

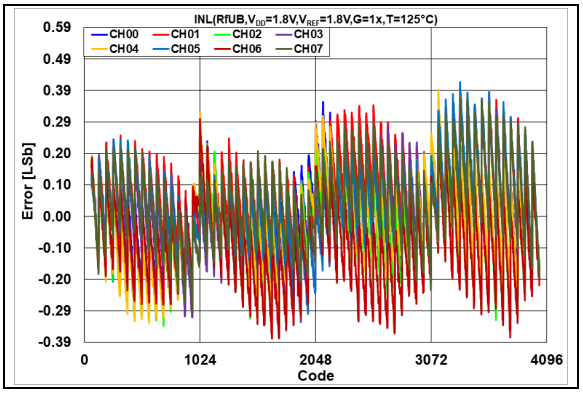

FIGURE 2-27: *INL Error vs. DAC Code and Temperature, V_{DD} = 1.8V, T = +125°C.*

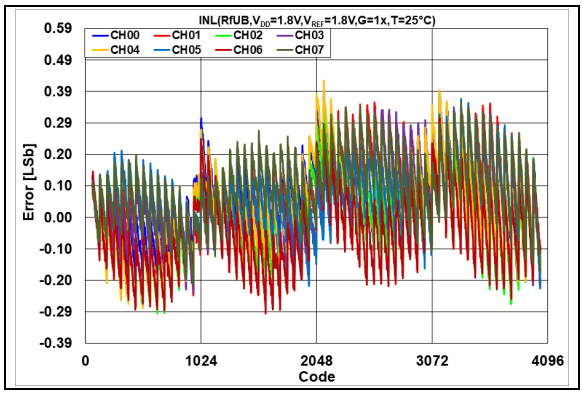

FIGURE 2-26: *INL Error vs. DAC Code and Temperature, V_{DD} = 1.8V, T = +25°C.*

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2.2.3 DIFFERENTIAL NONLINEARITY (DNL) – MCP48CXB2X (12-BIT), VRnB:VRnA = 10, $V_{REF} = V_{DD}$, GAIN = 1x, CODE 64-4032

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

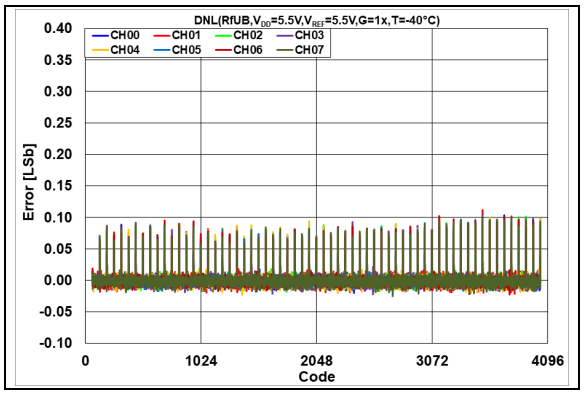

FIGURE 2-28: *DNL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, T = -40°C.*

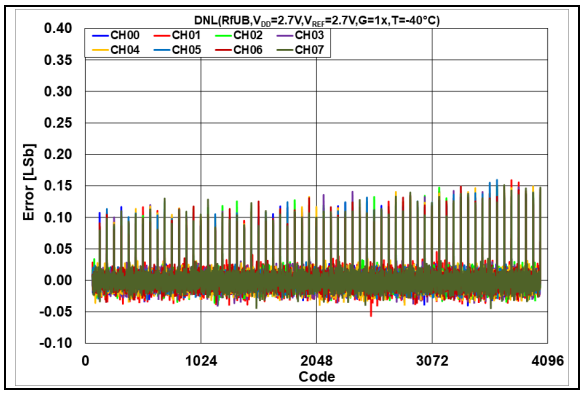

FIGURE 2-31: *DNL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, T = -40°C.*

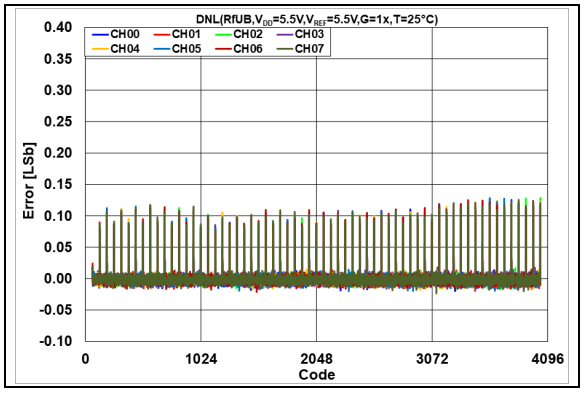

FIGURE 2-29: *DNL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, T = +25°C.*

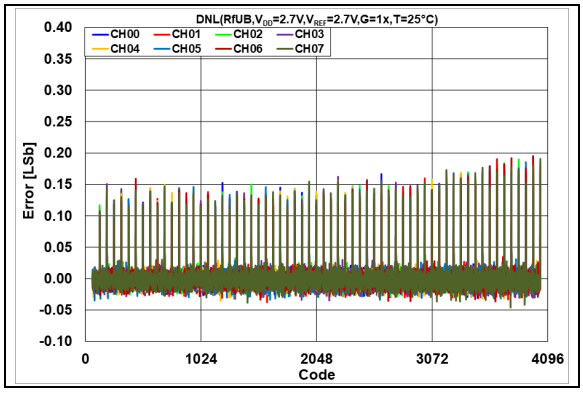

FIGURE 2-32: *DNL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, T = +25°C.*

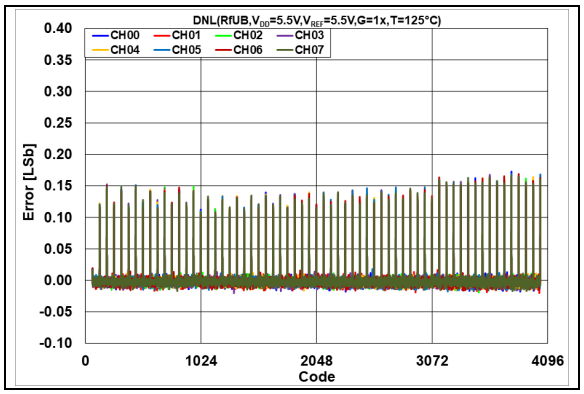

FIGURE 2-30: *DNL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, T = +125°C.*

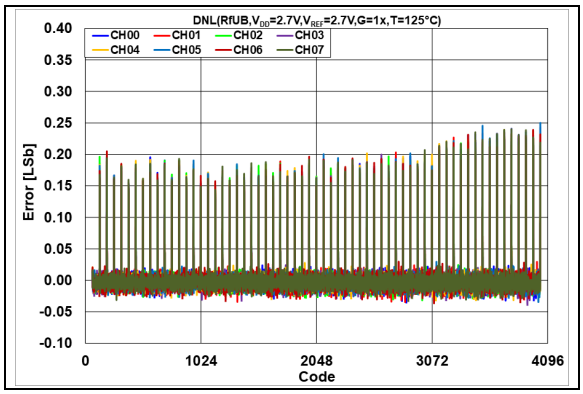

FIGURE 2-33: *DNL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, T = +125°C.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

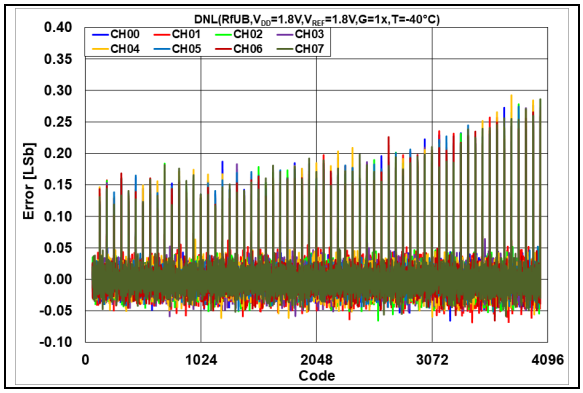

FIGURE 2-34: *DNL Error vs. DAC Code and Temperature, V_{DD} = 1.8V, T = -40°C.*

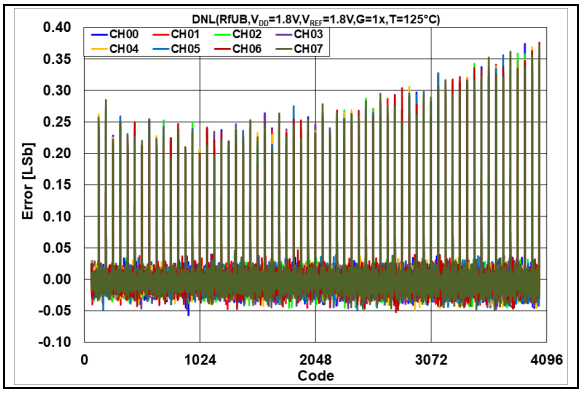

FIGURE 2-36: *DNL Error vs. DAC Code and Temperature, V_{DD} = 1.8V, T = +125°C.*

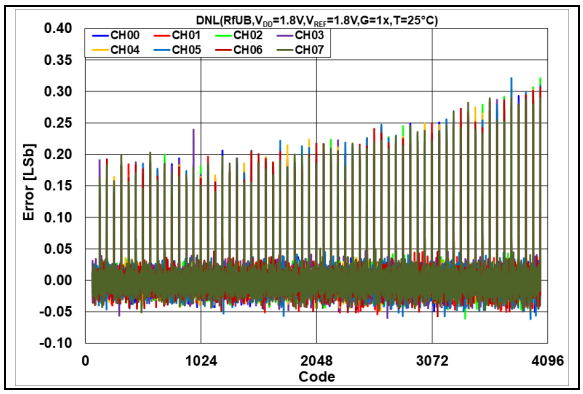

FIGURE 2-35: *DNL Error vs. DAC Code and Temperature, V_{DD} = 1.8V, T = +25°C.*

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2.2.4 TOTAL UNADJUSTED ERROR (TUE) – MCP48CXB2X (12-BIT), VRnB:VRnA = 10, V_{REF} = 0.5 x V_{DD}, GAIN = 2x, CODE 64-4032

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

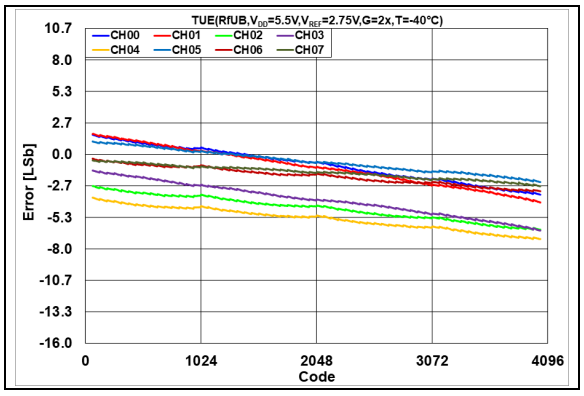

FIGURE 2-37: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 5.5V, V_{REF} = 2.75V, T = -40°C.*

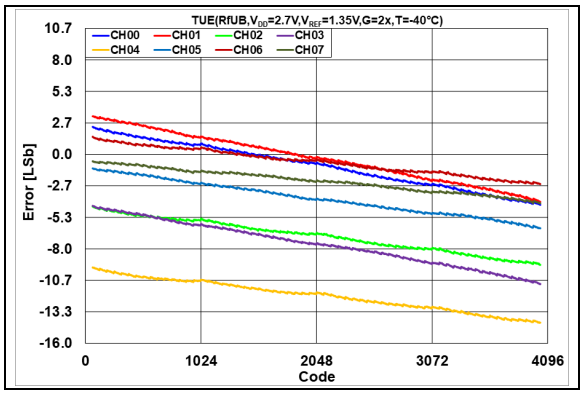

FIGURE 2-40: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 2.7V, V_{REF} = 1.35V, T = -40°C.*

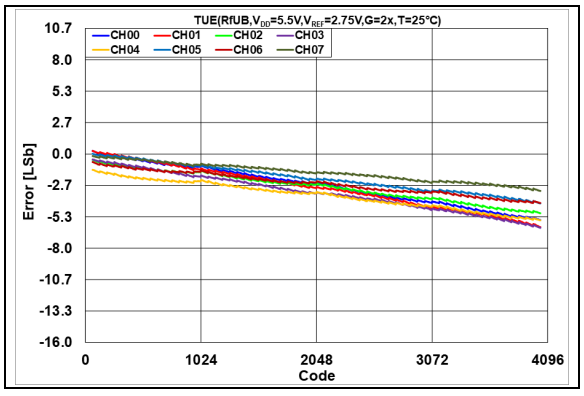

FIGURE 2-38: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 5.5V, V_{REF} = 2.75V, T = +25°C.*

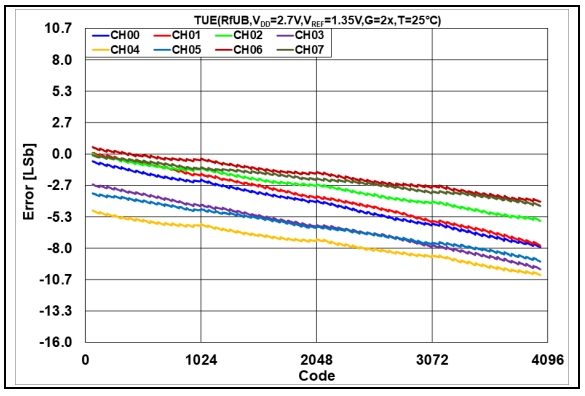

FIGURE 2-41: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 2.7V, V_{REF} = 1.35V, T = +25°C.*

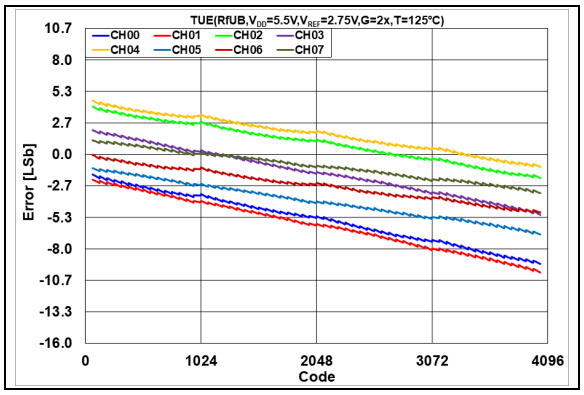

FIGURE 2-39: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 5.5V, V_{REF} = 2.75V, T = +125°C.*

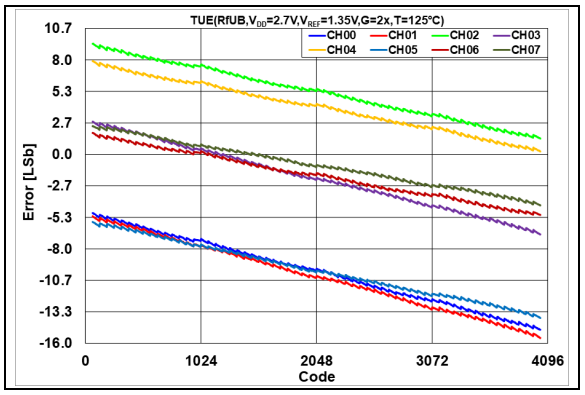

FIGURE 2-42: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 2.7V, V_{REF} = 1.35V, T = +125°C.*

2.2.5 INTEGRAL NONLINEARITY (INL) – MCP48CXB2X (12-BIT), VRnB:VRnA = 10, V_{REF} = 0.5 x V_{DD}, GAIN = 2x, CODE 64-4032

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

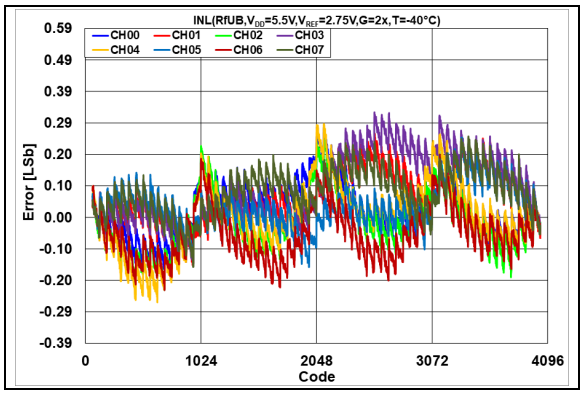

FIGURE 2-43: *INL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, V_{REF} = 2.75V, T = -40°C.*

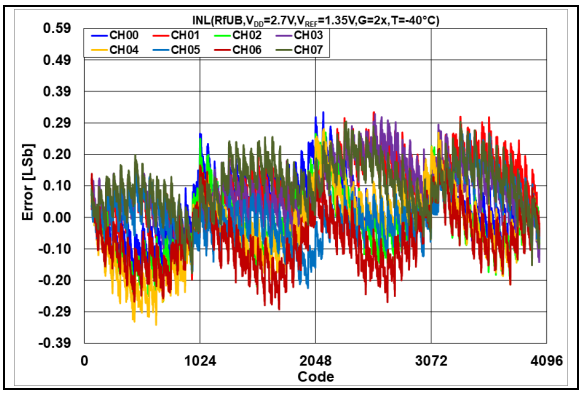

FIGURE 2-46: *INL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, V_{REF} = 1.35V, T = -40°C.*

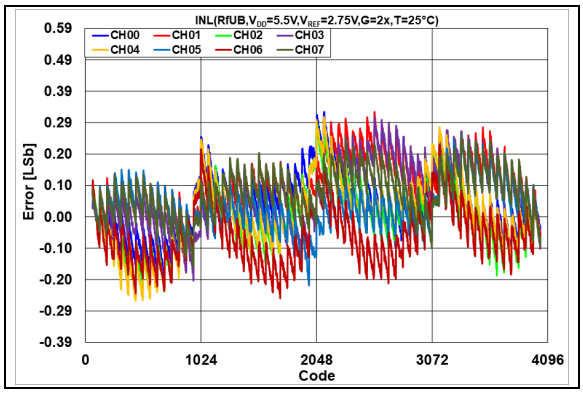

FIGURE 2-44: *INL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, V_{REF} = 2.75V, T = +25°C.*

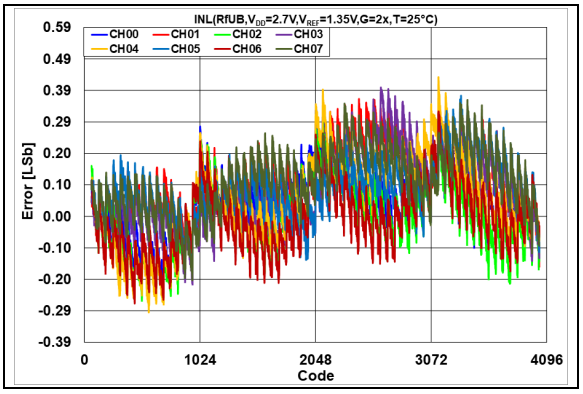

FIGURE 2-47: *INL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, V_{REF} = 1.35V, T = +25°C.*

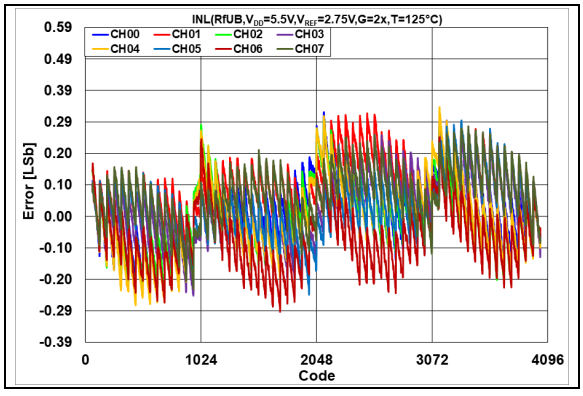

FIGURE 2-45: *INL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, V_{REF} = 2.75V, T = +125°C.*

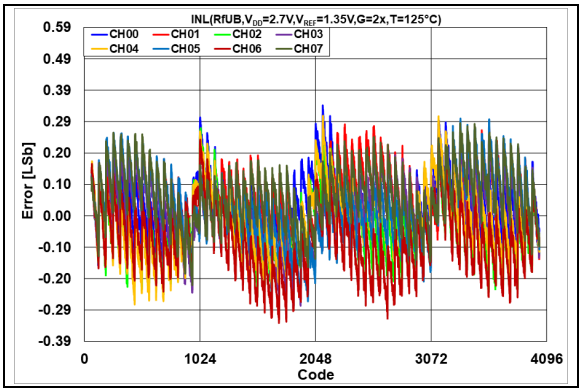

FIGURE 2-48: *INL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, V_{REF} = 1.35V, T = +125°C.*

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2.2.6 DIFFERENTIAL NONLINEARITY ERROR (DNL) – MCP48CXB2X (12-BIT), VRnB:VRnA = 10, V_{REF} = 0.5 x V_{DD}, GAIN = 2x, CODE 64-4032

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

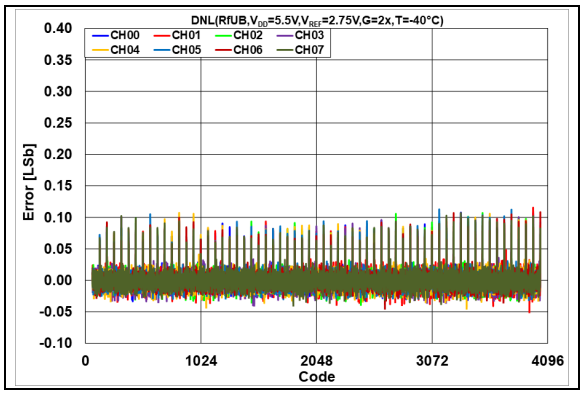

FIGURE 2-49: *DNL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, V_{REF} = 2.75V, T = -40°C.*

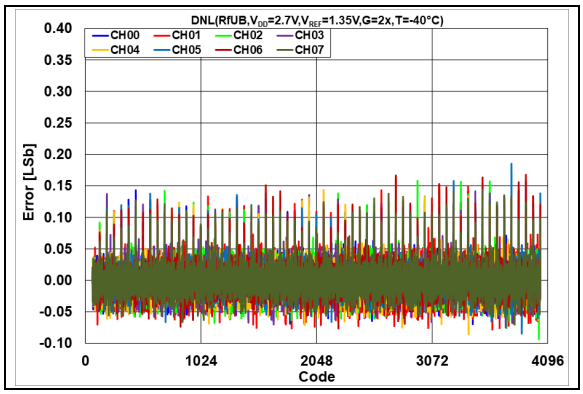

FIGURE 2-52: *DNL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, V_{REF} = 1.35V, T = +125°C.*

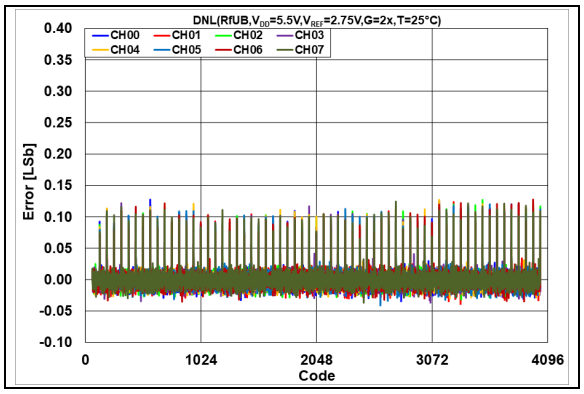

FIGURE 2-50: *DNL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, V_{REF} = 2.75V, T = +25°C.*

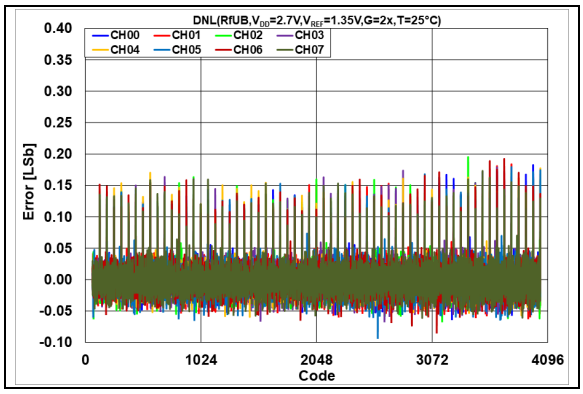

FIGURE 2-53: *DNL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, V_{REF} = 1.35V, T = +25°C.*

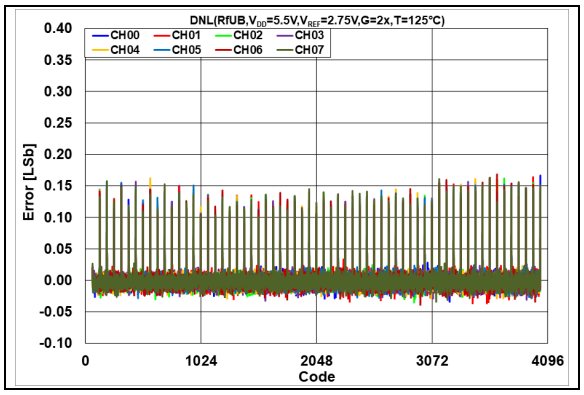

FIGURE 2-51: *DNL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, V_{REF} = 2.75V, T = +125°C.*

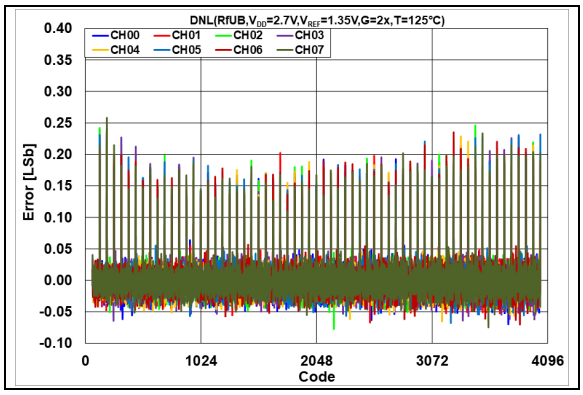

FIGURE 2-54: *DNL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, V_{REF} = 1.35V, T = +125°C.*

2.2.7 TOTAL UNADJUSTED ERROR (TUE) – MCP48CXB2X (12-BIT), VRnB:VRnA = 01, V_{REF} = INTERNAL BAND GAP, GAIN = 1x, CODE 64-4032

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

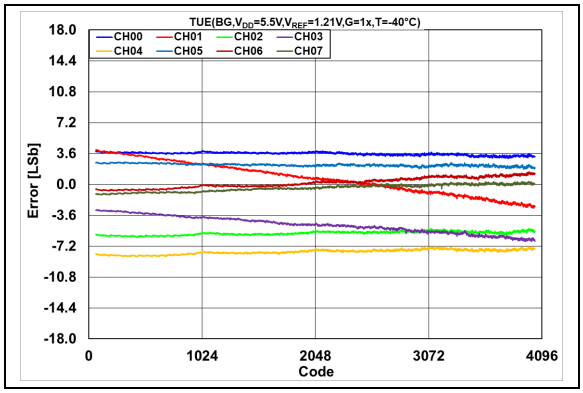

FIGURE 2-55: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 5.5V, T = -40°C.*

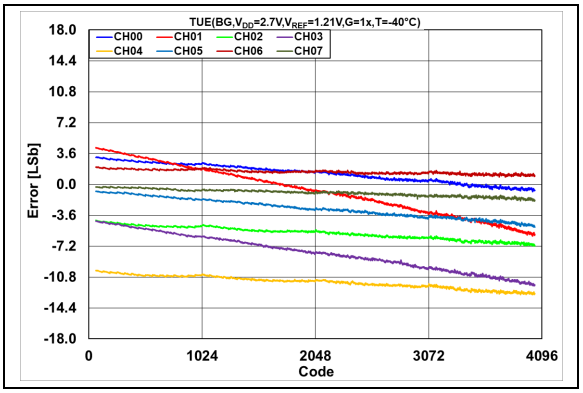

FIGURE 2-58: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 2.7V, T = -40°C.*

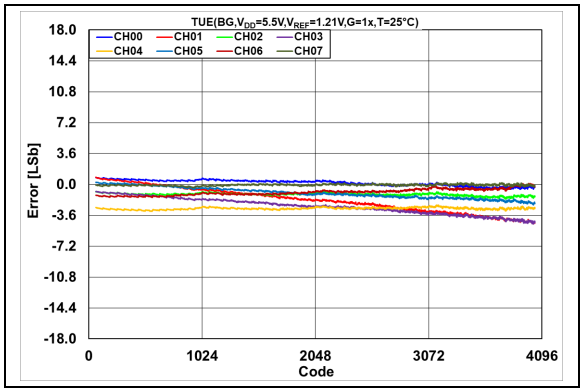

FIGURE 2-56: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 5.5V, T = +25°C.*

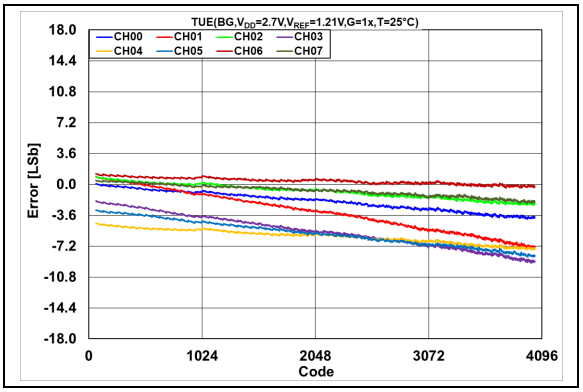

FIGURE 2-59: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 2.7V, T = +25°C.*

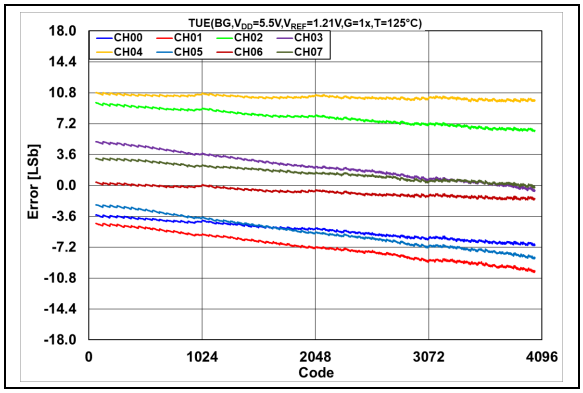

FIGURE 2-57: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 5.5V, T = +125°C.*

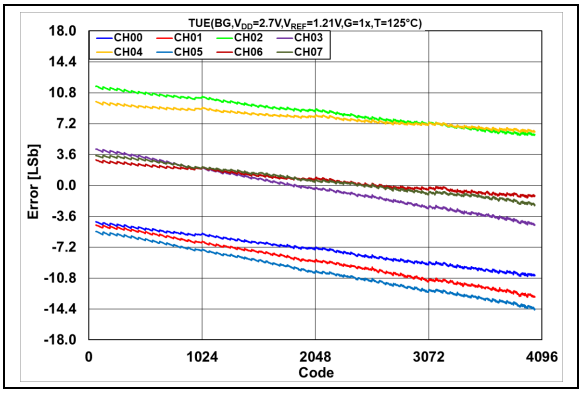

FIGURE 2-60: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 2.7V, T = +125°C.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

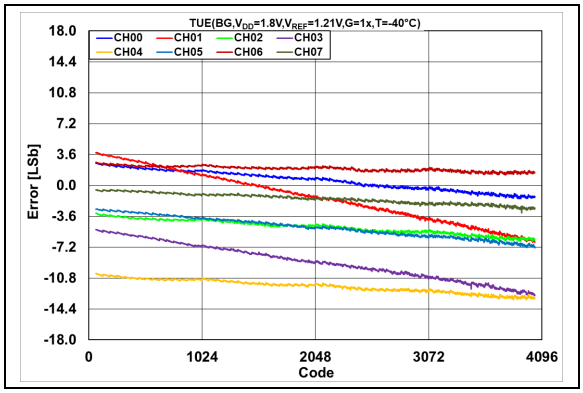

FIGURE 2-61: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 1.8V, T = -40°C.*

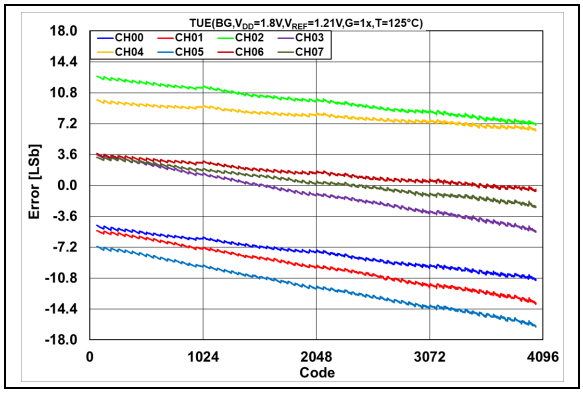

FIGURE 2-63: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 1.8V, T = +125°C.*

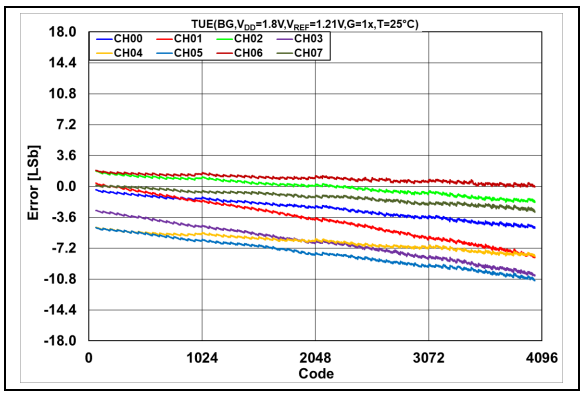

FIGURE 2-62: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 1.8V, T = +25°C.*

2.2.8 TOTAL UNADJUSTED ERROR (TUE) – MCP48CXB2X (12-BIT), VRnB:VRnA = 01, V_{REF} = INTERNAL BAND GAP, GAIN = 2x, CODE 64-4032

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

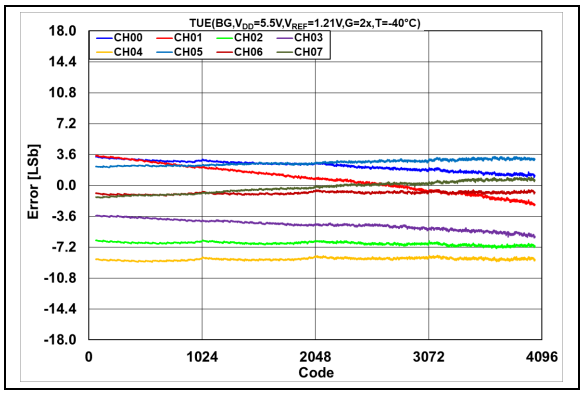

FIGURE 2-64: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 5.5V, T = -40°C.*

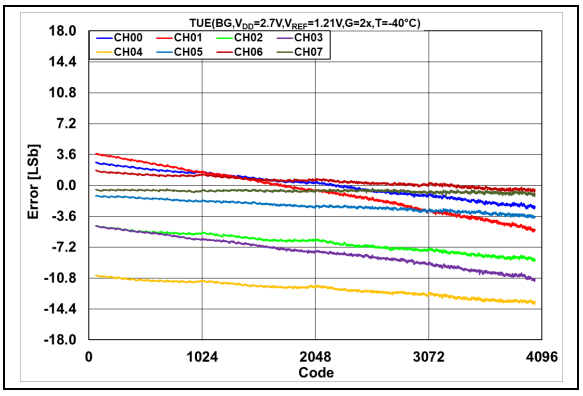

FIGURE 2-67: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 2.7V, T = -40°C.*

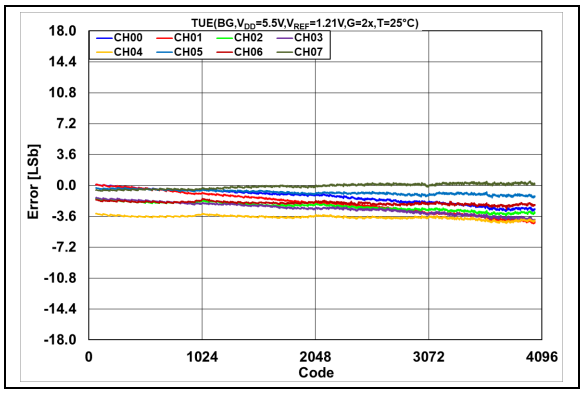

FIGURE 2-65: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 5.5V, T = +25°C.*

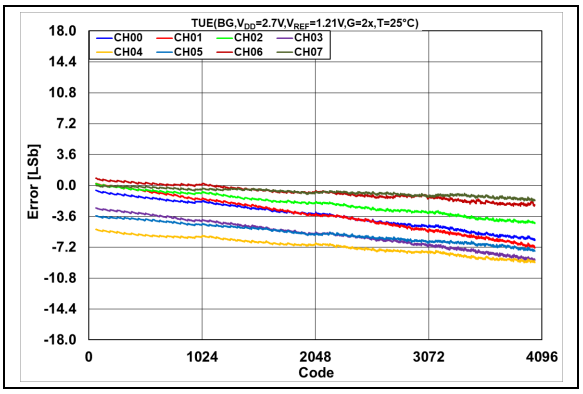

FIGURE 2-68: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 2.7V, T = +25°C.*

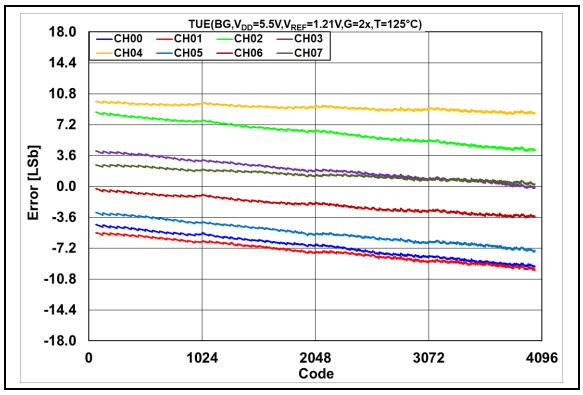

FIGURE 2-66: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 5.5V, T = +125°C.*

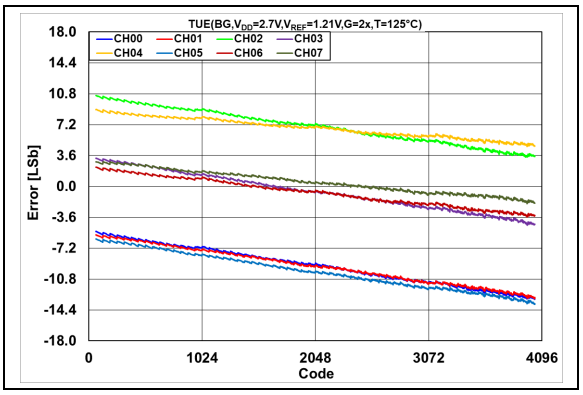

FIGURE 2-69: *Total Unadjusted Error (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 2.7V, T = +125°C.*

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2.2.9 INTEGRAL NONLINEARITY ERROR (INL) – MCP48CXB2X (12-BIT), VRnB:VRnA = 01, V_{REF} = INTERNAL BAND GAP, GAIN = 1x, CODE 64-4032

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

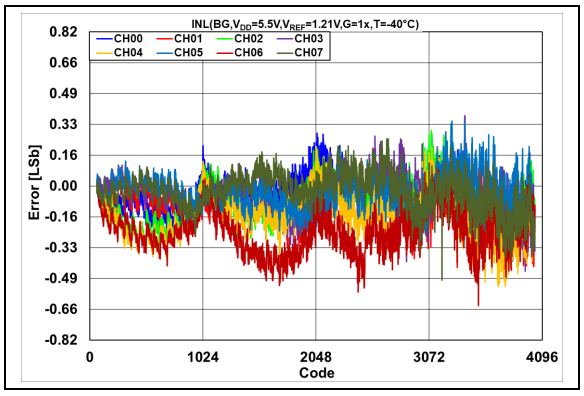

FIGURE 2-70: *INL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, T = -40°C.*

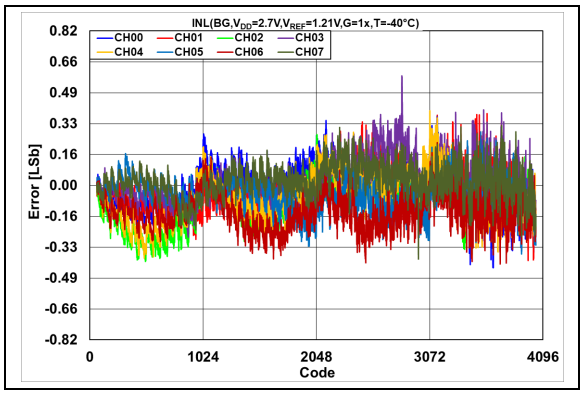

FIGURE 2-73: *INL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, T = -40°C.*

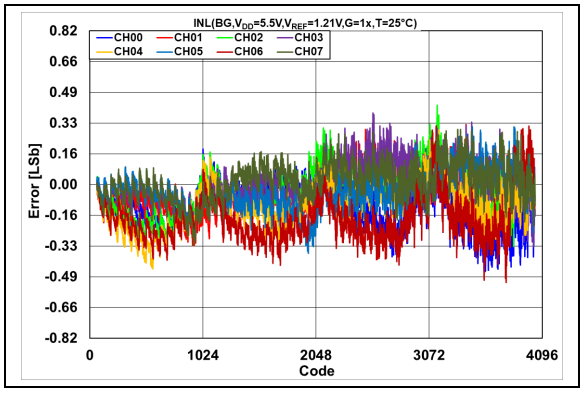

FIGURE 2-71: *INL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, T = +25°C.*

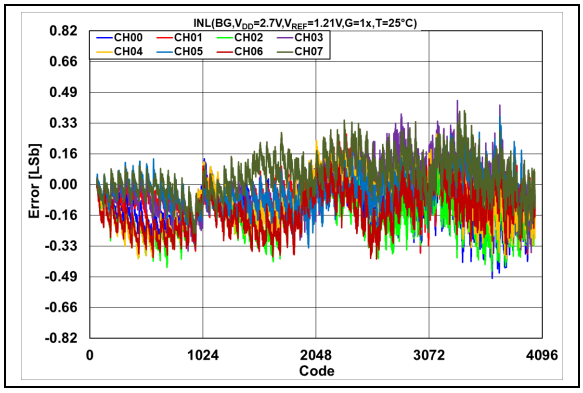

FIGURE 2-74: *INL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, T = +25°C.*

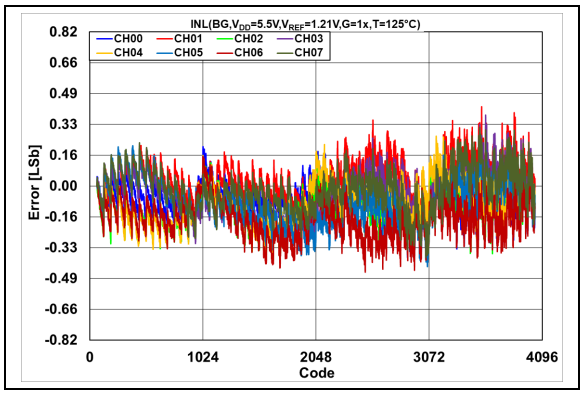

FIGURE 2-72: *INL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, T = +125°C.*

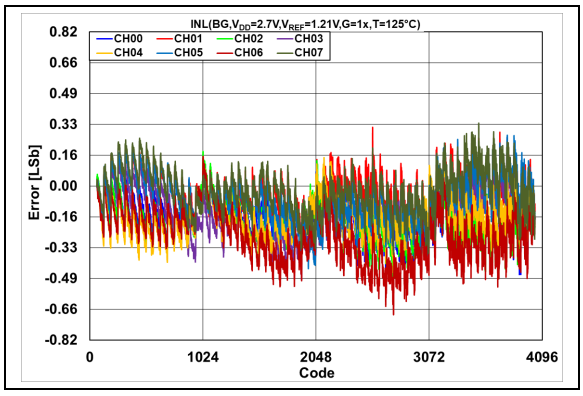

FIGURE 2-75: *INL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, T = +125°C.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

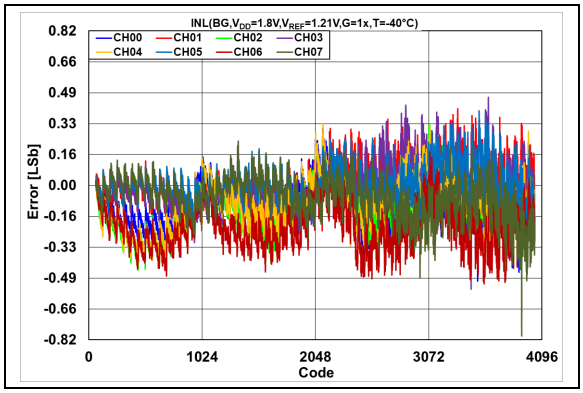

FIGURE 2-76: *INL Error vs. DAC Code and Temperature, V_{DD} = 1.8V, T = -40°C.*

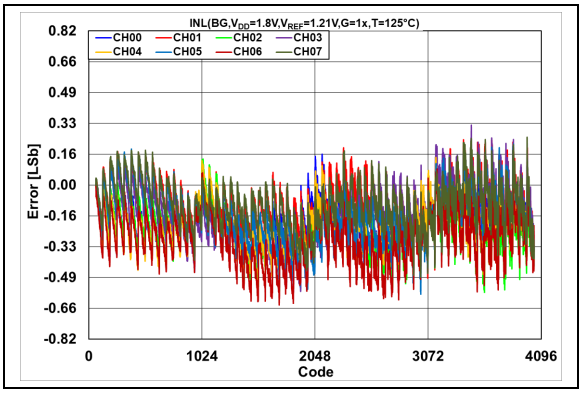

FIGURE 2-78: *INL Error vs. DAC Code and Temperature, V_{DD} = 1.8V, T = +125°C.*

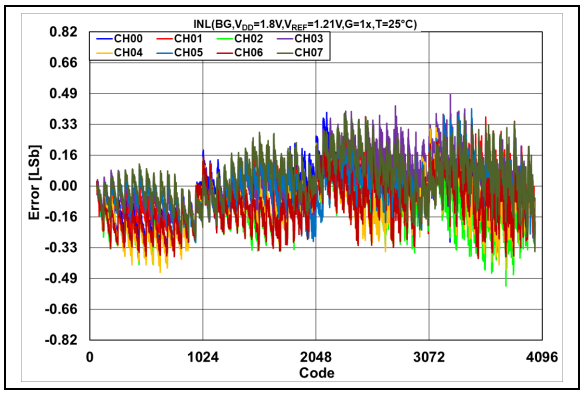

FIGURE 2-77: *INL Error vs. DAC Code and Temperature, V_{DD} = 1.8V, T = +25°C.*

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2.2.10 INTEGRAL NONLINEARITY ERROR (INL) – MCP48CXB2X (12-BIT), VRnB:VRnA = 01, V_{REF} = INTERNAL BAND GAP, GAIN = 2x, CODE 64-4032

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

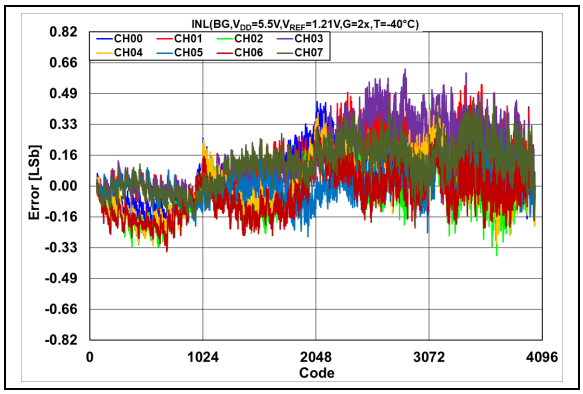

FIGURE 2-79: *INL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, T = -40°C.*

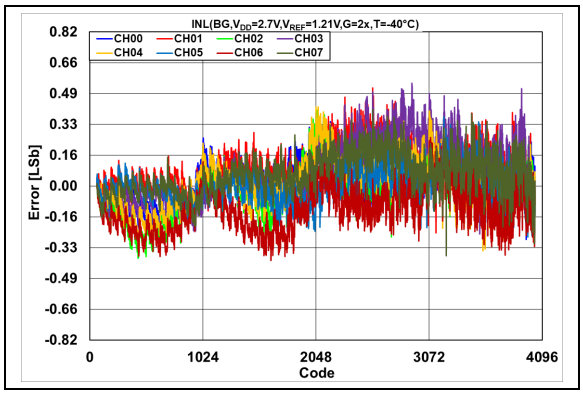

FIGURE 2-82: *INL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, T = -40°C.*

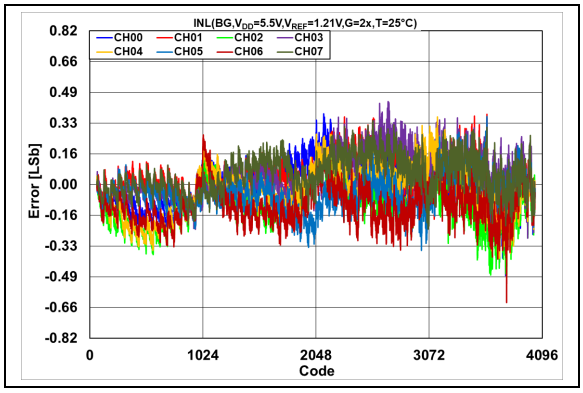

FIGURE 2-80: *INL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, T = +25°C.*

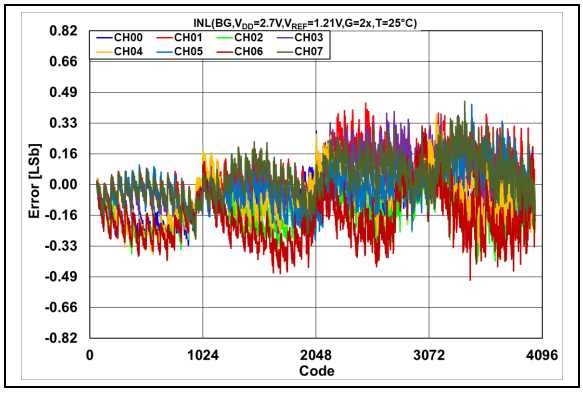

FIGURE 2-83: *INL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, T = +25°C.*

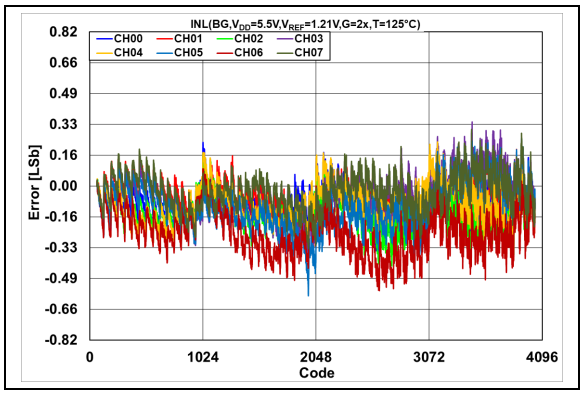

FIGURE 2-81: *INL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, T = +125°C.*

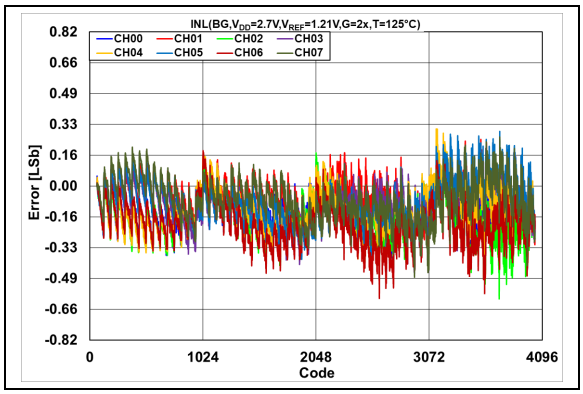

FIGURE 2-84: *INL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, T = +125°C.*

2.2.11 DIFFERENTIAL NONLINEARITY ERROR (DNL) – MCP48CXB2X (12-BIT), VRnB:VRnA = 01, V_{REF} = INTERNAL BAND GAP, GAIN = 1x, CODE 64-4032

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

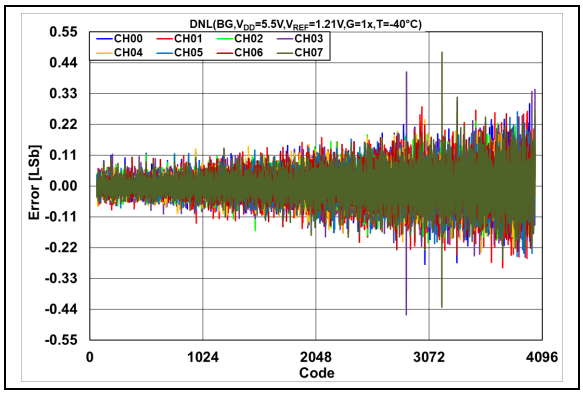

FIGURE 2-85: *DNL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, T = -40°C.*

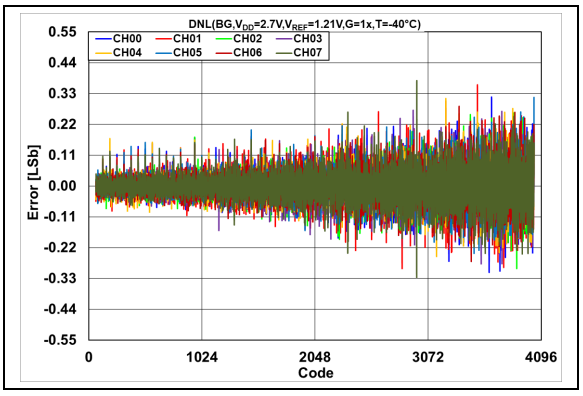

FIGURE 2-88: *DNL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, T = -40°C.*

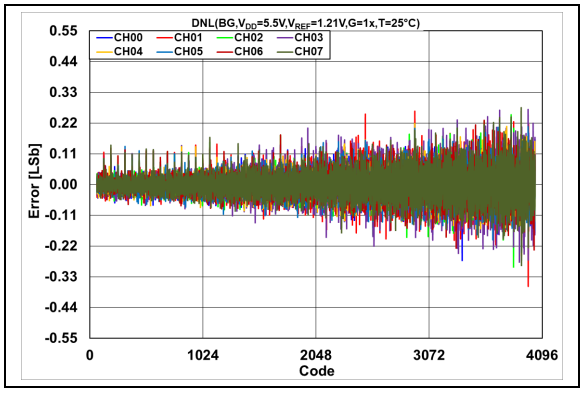

FIGURE 2-86: *DNL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, T = +25°C.*

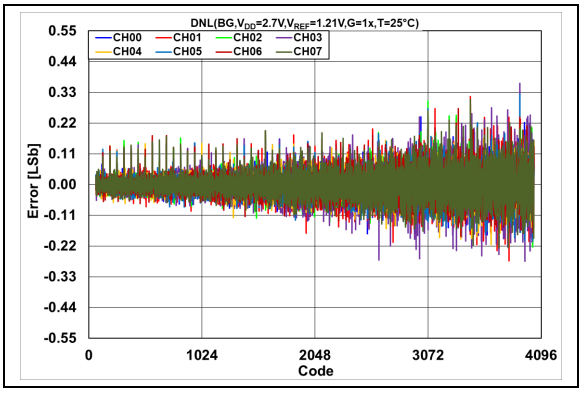

FIGURE 2-89: *DNL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, T = +25°C.*

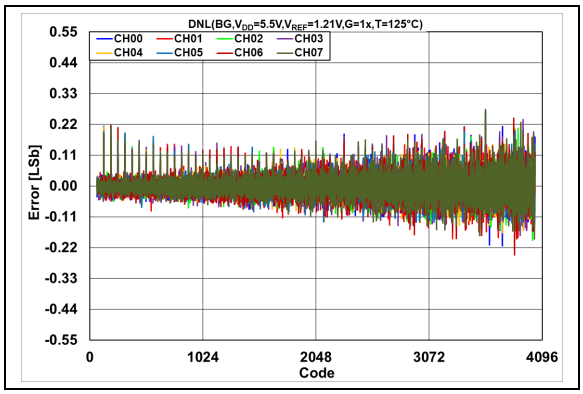

FIGURE 2-87: *DNL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, T = +125°C.*

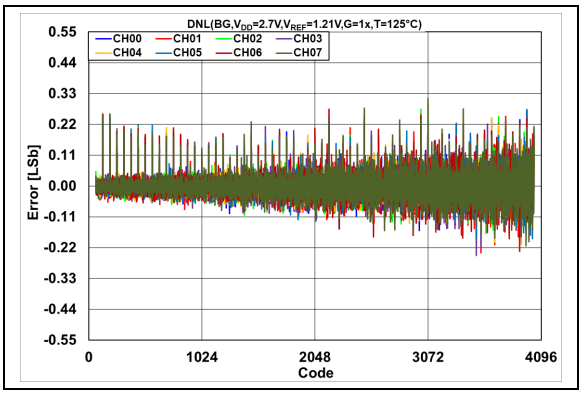

FIGURE 2-90: *DNL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, T = +125°C.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

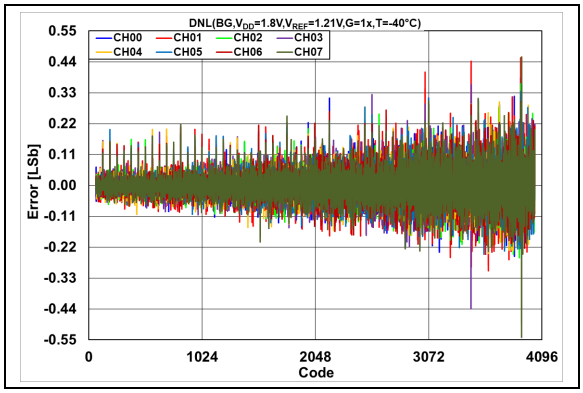

FIGURE 2-91: *DNL Error vs. DAC Code and Temperature, V_{DD} = 1.8V, T = -40°C.*

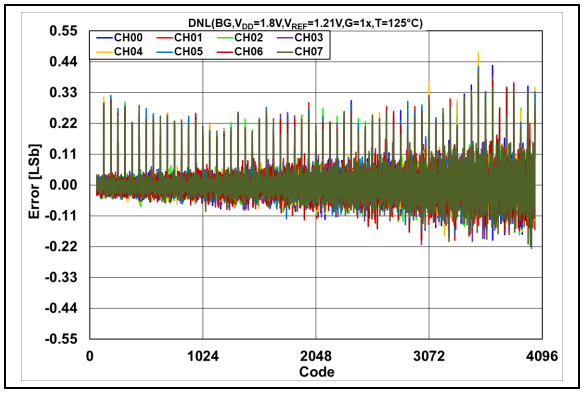

FIGURE 2-93: *DNL Error vs. DAC Code and Temperature, V_{DD} = 1.8V, T = +125°C.*

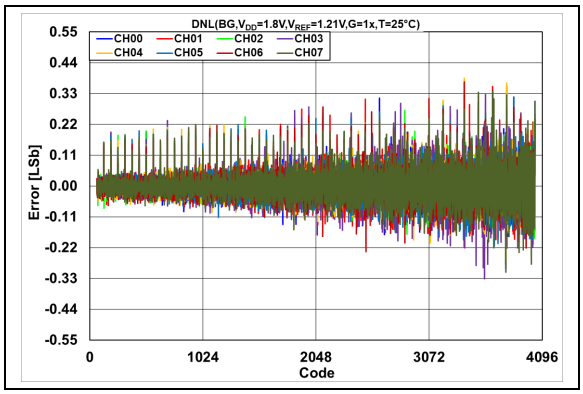

FIGURE 2-92: *DNL Error vs. DAC Code and Temperature, V_{DD} = 1.8V, T = +25°C.*

2.2.12 DIFFERENTIAL NONLINEARITY ERROR (DNL) – MCP48CXB2X (12-BIT), VRnB:VRnA = 01, V_{REF} = INTERNAL BAND GAP, GAIN = 2x, CODE 64-4032

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

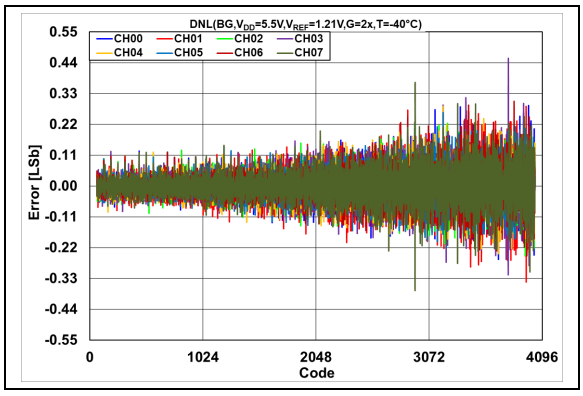

FIGURE 2-94: *DNL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, T = -40°C.*

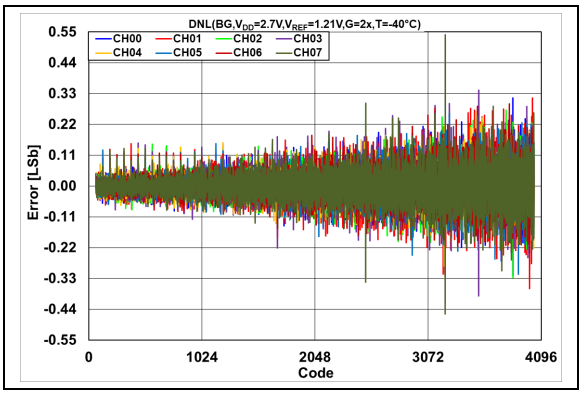

FIGURE 2-97: *DNL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, T = -40°C.*

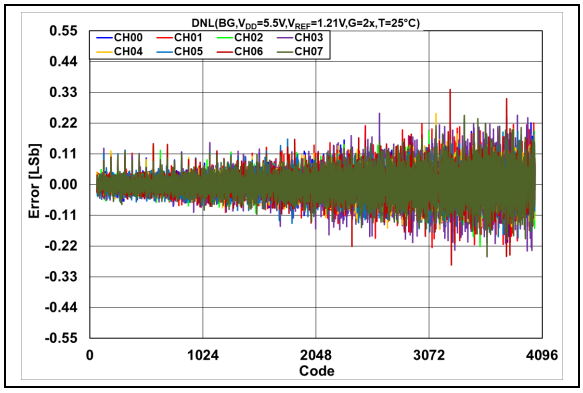

FIGURE 2-95: *DNL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, T = +25°C.*

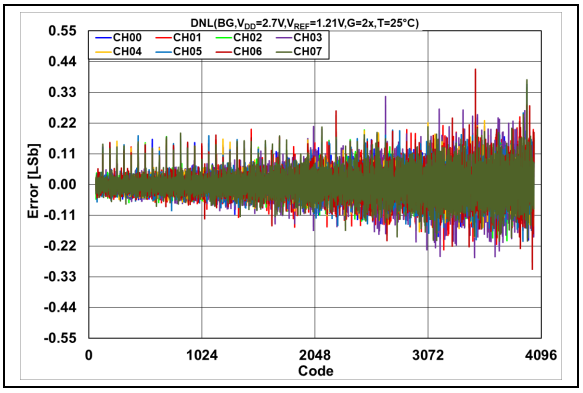

FIGURE 2-98: *DNL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, T = +25°C.*

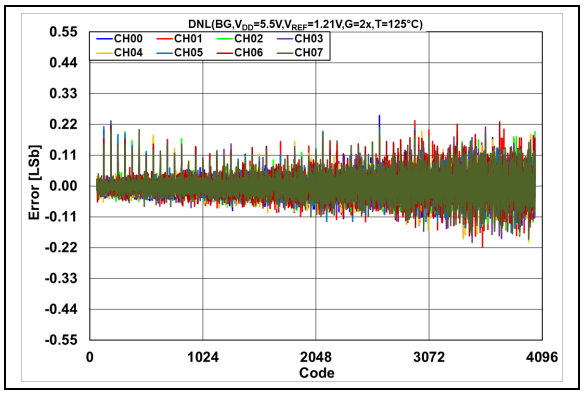

FIGURE 2-96: *DNL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, T = +125°C.*

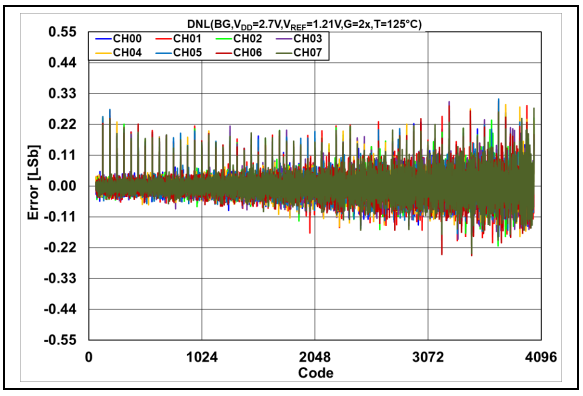

FIGURE 2-99: *DNL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, T = +125°C.*

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3.0 PIN DESCRIPTIONS

Overviews of the pin functions are provided in **Section 3.1, "Positive Power Supply Input (VDD)"** through **Section 3.10, "SPI – Serial Data Output Pin (SDO)"**.

The descriptions of the pins for the quad-DAC output devices are listed in Table 3-1 and descriptions for the octal-DAC output devices are listed in Table 3-2.

TABLE 3-1: MCP48CXBX4 (QUAD-DAC) PIN FUNCTION TABLE

Pin		Symbol	I/O	Buffer Type	Description
20-Lead TSSOP	20-Lead QFN				
1	19	$\overline{LAT1}$	I	ST	DAC Register Latch 1 Pin. The Latch 1 pin allows the values in the volatile DAC1/DAC3 registers to be transferred to the V_{OUT1}/ V_{OUT3} output pins.
2	20	V_{DD}	—	P	Supply Voltage Pin
3	1	$\overline{CS}$	I	ST	SPI Chip Select Pin
4	2	V_{REF0}	A	A	Voltage Reference Input 0 Pin
5	3	V_{OUT0}	A	A	Buffered Analog Voltage Output – Channel 0 Pin
6	4	V_{OUT2}	A	A	Buffered Analog Voltage Output – Channel 2 Pin
7, 8, 10, 11, 12, 13	5, 6, 8, 9, 10, 11	NC	—	—	Not Internally Connected
9	7	V_{SS}	—	P	Ground Reference Pin for all circuitries on the device
14	12	V_{OUT3}	A	A	Buffered Analog Voltage Output - Channel 3 Pin
15	13	V_{OUT1}	A	A	Buffered Analog Voltage Output - Channel 1 Pin
16	14	V_{REF1}	A	A	Voltage Reference Input 1 Pin
17	15	SDO	O	—	SPI Serial Data Output Pin
18	16	SCK	I	ST	SPI Serial Clock Pin
19	17	SDI	I	ST	SPI Serial Data Input Pin
20	18	$\overline{LAT0}$/HVC	I	ST	DAC Wiper Register Latch 0/High-Voltage Command Pin. The Latch 0 pin allows the values in the volatile DAC0/DAC2 registers to be transferred to the V_{OUT0}/V_{OUT2} output pins. High-voltage commands allow the MTP Configuration bits to be written.
—	21	EP	—	P	Exposed Thermal Pad – it must be connected to V_{SS}

Note 1: A = Analog, I = Input, ST = Schmitt Trigger, O = Output, I/O = Input/Output, P = Power

TABLE 3-2: MCP48CXBX8 (OCTAL-DAC) PIN FUNCTION TABLE

Pin		Symbol	I/O	Buffer Type	Description
20-Lead TSSOP	20-Lead QFN				
1	19	$\overline{LAT1}$	I	ST	DAC Register Latch 1 Pin. The Latch 1 pin allows the values in the volatile DAC1/DAC3/DAC5/DAC7 registers to be transferred to the $V_{OUT1}/V_{OUT3}/V_{OUT5}/V_{OUT7}$ output pins.
2	20	V_{DD}	—	P	Supply Voltage Pin
3	1	$\overline{CS}$	I	ST	SPI Chip Select Pin
4	2	V_{REF0}	A	A	Voltage Reference Input 0 Pin
5	3	V_{OUT0}	A	A	Buffered Analog Voltage Output – Channel 0 Pin
6	4	V_{OUT2}	A	A	Buffered Analog Voltage Output – Channel 2 Pin
7	5	V_{OUT4}	A	A	Buffered Analog Voltage Output – Channel 4 Pin
8	6	V_{OUT6}	A	A	Buffered Analog Voltage Output – Channel 6 Pin
9	7	V_{SS}	—	P	Ground Reference Pin for all circuitries on the device
10, 11	8, 9	NC	—	—	Not Internally Connected
12	10	V_{OUT7}	A	A	Buffered Analog Voltage Output – Channel 7 Pin
13	11	V_{OUT5}	A	A	Buffered Analog Voltage Output – Channel 5 Pin
14	12	V_{OUT3}	A	A	Buffered Analog Voltage Output – Channel 3 Pin
15	13	V_{OUT1}	A	A	Buffered Analog Voltage Output – Channel 1 Pin
16	14	V_{REF1}	A	A	Voltage Reference Input 1 Pin
17	15	SDO	O	—	SPI Serial Data Output Pin
18	16	SCK	I	ST	SPI Serial Clock Pin
19	17	SDI	I	ST	SPI Serial Data Input Pin
20	18	$\overline{LAT0}$/HVC	I	ST	DAC Wiper Register Latch 0/High-Voltage Command Pin. The Latch 0 pin allows the values in the volatile DAC0/DAC2/DAC4/DAC6 registers to be transferred to the $V_{OUT0}/V_{OUT2}/V_{OUT4}/V_{OUT6}$ output pins. High-voltage commands allow the MTP Configuration bits to be written.
—	21	EP	—	P	Exposed Thermal Pad – it must be connected to V_{SS}

Note 1: A = Analog, I = Input, ST = Schmitt Trigger, O = Output, I/O = Input/Output, P = Power

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3.1 Positive Power Supply Input (V_{DD})

V_{DD} is the positive supply voltage input pin. The input supply voltage is relative to V_{SS}.

The power supply at the V_{DD} pin must be as clean as possible for a good DAC performance. It is recommended to use an appropriate bypass capacitor of about 0.1 µF (ceramic) to ground as close as possible to the pin. An additional 10 µF capacitor in parallel can be added to further attenuate noise present in application boards.

3.2 Ground (V_{SS})

The V_{SS} pin is the device ground reference.

The user must connect the V_{SS} pin to a ground plane through a low-impedance connection. If an analog ground path is available in the application Printed Circuit Board (PCB), it is highly recommended that the V_{SS} pin be tied to the analog ground path or isolated within an analog ground plane of the circuit board.

3.3 Voltage Reference Pins (V_{REFn})

The V_{REFn} pins are either an input or an output. When the DAC's voltage reference is configured as the V_{REF} pin, the pin is an input. When the DAC's voltage reference is configured as the internal band gap, the pin is an output.

When the DAC's voltage reference is configured as the V_{REF} pin, there are two options for this voltage input: the V_{REF} pin voltage is buffered or unbuffered. The buffered option is offered in cases where the external reference voltage does not have sufficient current capability to not drop its voltage when connected to the internal resistor ladder circuit.

When the DAC's voltage reference is configured as the device V_{DD}, the V_{REF} pin is disconnected from the internal circuit.

When the DAC's voltage reference is configured as the internal band gap, the V_{REF} pin's drive capability is minimal, so the output signal must be buffered.

See **Section 4.4.2, "Voltage Reference Selection"** and Register 4-2 for more details on the Configuration bits.

3.4 No Connect (NC)

The NC pins are not internally connected to the device.

3.5 Analog Output Voltage Pins (V_{OUTn})

V_{OUTn} are the DAC analog voltage output pins. Each DAC output has an output amplifier. The DAC output range depends on the selection of the voltage reference source (and potential output gain selection):

- Device V_{DD} – The Full-Scale Range (FSR) of the DAC output is from V_{SS} to approximately V_{DD}.
- V_{REF} pin – The FSR of the DAC output is from V_{SS} to G × V_{RL}, where G is the gain selection option (1x or 2x).
- Internal Band Gap – The FSR of the DAC output is from V_{SS} to G × V_{BG}, where G is the gain selection option (1x or 2x).

In Normal mode, the DC impedance of the output pin is about 1Ω. In Power-Down mode, the output pin is internally connected to a known pull-down resistor of 1 kΩ, 100 kΩ or open. The power-down selection bits settings are shown in Register 4-3 (Table 4-7).

3.6 Latch Pins ($\overline{LATn}$)/High-Voltage Command Pin (HVC)

The DAC output value update event can be controlled and synchronized using the $\overline{LAT}$ pin, for individual channels, on single or multiple devices.

The $\overline{LAT}$ pin controls the effect of the Volatile Wiper registers, VRnB:VRnA, PDnB:PDnA and Gn bits on the DAC output. If the $\overline{LAT}$ pin is held at V_{IH}, the values sent to the Volatile Wiper registers and Configuration bits have no effect on the DAC outputs. After the Volatile Wiper registers and Configuration bits are loaded with the desired data, once the voltage on the pin transitions to V_{IL}, the values in the Volatile Wiper registers and Configuration bits are transferred to the DAC outputs. Pulling $\overline{LAT}$ low during writes to the output registers could lead to unpredictable DAC output voltage values and must be avoided. To clear such a situation, a low-to-high followed by a high-to-low transition on the $\overline{LAT}$ pin is required. The pin is level-sensitive, so writing to the Volatile Wiper registers and Configuration bits while it is being held at V_{IL} will trigger an immediate change in the outputs.

$\overline{LAT0}$ is multiplexed with an HVC pin functionality. The HVC pin allows the device's MTP memory to be programmed for the MCP48CMBXX devices. The programming voltage supply must provide 7.5V and at least 6.4 mA.

Note:	The HVC pin must have voltages greater than 5.5V present only during the MTP programming operation. Using voltages greater than 5.5V for an extended time on the pin may cause device reliability issues.

3.7 SPI – Chip Select Pin ($\overline{CS}$)

The $\overline{CS}$ pin enables/disables the serial interface (SDI, SDO and SCK). The serial interface must be enabled for the device to receive any serial commands.

See **Section 4.5 "Serial Communication Interface"** for more details regarding the SPI serial interface communication.

3.8 SPI – Serial Clock Pin (SCK)

The SCK pin is the serial clock pin of the SPI interface. The MCP48CXBX4/8 SPI interface only accepts external serial clocks.

3.9 SPI – Serial Data Input Pin (SDI)

The SDI pin is the serial data input pin of the SPI interface. The SDI pin is used to write the DAC wiper registers and configuration bits.

3.10 SPI – Serial Data Output Pin (SDO)

The SDO pin is the serial data output pin of the SPI interface. The SDO pin is used to read the DAC wiper registers and configuration bits.

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4.0 DEVICE OPERATION

4.1 General Description

The MCP48CXBX4 (MCP48CXB04, MCP48CXB14 and MCP48CXB24) are quad-channel voltage output devices.

The MCP48CXBX8 (MCP48CXB08, MCP48CXB18 and MCP48CXB28) are octal-channel voltage output devices.

These devices are offered with 8-bit (MCP48CXB0X), 10-bit (MCP48CXB1X) and 12-bit (MCP48CXB2X) resolutions.

The family offers two memory options: the MCP48CVBXX devices have volatile memory, while the MCP48CMBXX devices have 32-times programmable nonvolatile memory (MTP).

All devices include an SPI serial interface and write latch ($\overline{LAT}$) pins to control the update of the analog output voltage value from the value written in the volatile DAC output registers.

The devices use a resistor ladder architecture. The resistor ladder DAC is driven from a software-selectable voltage reference source. The source can be either the device's internal V_{DD}, an external V_{REF} pin voltage (buffered or unbuffered) or an internal band gap voltage source.

The DAC output is buffered with a low-power and precision output amplifier. This output amplifier provides a rail-to-rail output with low offset voltage and low noise. The gain (1x or 2x) of the output buffer is software configurable.

The devices operate from a single supply voltage. This voltage is specified from 2.7V to 5.5V for full specified operation and from 1.8V to 5.5V for digital operation. The device operates between 1.8V and 2.7V, but some device parameters are not specified.

The MCP48CMBXX devices also have user-programmable nonvolatile configuration memory (MTP). This allows the device's desired POR values to be saved. The device also has general purpose MTP memory locations for storing system-specific information (calibration data, serial numbers, system ID information). A high-voltage requirement for programming on the HVC pin ensures that these device settings are not accidentally modified during normal system operation.

The MCP48CXBX4/8 device architecture is composed of the following functional units:

- **Power-on Reset/Brown-out Reset Module**
- **Device Memory**
- **DAC Circuitry**
- **Serial Communication Interface**

4.2 Power-on Reset/Brown-out Reset Module

The internal POR/BOR circuit monitors the power supply voltage (V_{DD}) during operation. This circuit ensures correct device start-up at system power-up and power-down events.

The device's RAM retention voltage (V_{RAM}) is lower than the POR/BOR voltage trip point (V_{POR}/V_{BOR}). The maximum V_{POR}/V_{BOR} voltage is less than 1.8V.

The POR and BOR trip points are at the same voltage and the condition is determined by whether the V_{DD} voltage is rising or falling (see Figure 4-1). What occurs is different depending on whether the Reset is a POR or BOR.

POR occurs as the voltage rises (typically from 0V), while BOR occurs as the voltage falls (typically from $V_{DD(MIN)}$ or higher).

When $V_{POR}/V_{BOR} < V_{DD} < 2.7V$, the electrical performance may not meet the data sheet specifications. In this region, the device is capable of reading and writing to its volatile memory if the proper serial command is executed.

4.2.1 POWER-ON RESET

The POR is the case where the device's V_{DD} has power applied to it from the V_{SS} voltage level. As the device powers up, the V_{OUT} pin floats to an unknown value. When the device's V_{DD} is above the transistor threshold voltage of the device, the output starts to be pulled low.

After the V_{DD} is above the POR/BOR trip point (V_{BOR}/V_{POR}), the resistor network's wiper is loaded with the POR value. The POR value is either mid-scale (MCP48CVBXX) or the user's MTP programmed value (MCP48CMBXX).

Note:	In order to have the MCP48CMBXX devices load the values from nonvolatile memory locations at POR, they have to be programmed at least once by the user. Otherwise, the loaded values will be the default ones. After MTP programming, a POR event is required to load the written values from the nonvolatile memory.

The volatile memory determines the analog output (V_{OUT}) pin voltage. After the device is powered up, the user can update the device memory.

When the rising V_{DD} voltage crosses the V_{POR} trip point, the following occur:

- The default DAC POR value is latched into the volatile DAC register.
- The default DAC POR Configuration bit values are latched into the volatile Configuration bits.
- The POR status bit is set ('1').
- The Reset Delay Timer (t_{PORD}) starts; when the Reset Delay Timer (t_{PORD}) times out, the serial interface is operational. During this delay time, the SPI interface will not accept commands.
- The Device Memory Address Pointer is forced to 00h.

The Analog Output (V_{OUT}) state is determined by the state of the volatile Configuration bits and the DAC register. This is called a Power-on Reset (event).

Figure 4-1 illustrates the conditions for power-up and power-down events under typical conditions.

4.2.2 BROWN-OUT RESET

A BOR occurs when a device has power applied to it and that power (voltage) drops below the specified range. If the V_{DD} voltage decreases below the V_{RAM} voltage, all volatile memory may become corrupted. Serial commands not completed due to a Brown-out condition may cause the memory location to become corrupted.

When the falling V_{DD} voltage crosses the V_{POR} trip point (BOR event), the following occur:

- The serial interface is disabled.
- The MTP writes are disabled.
- The device is forced into a Power-Down state (PDnB:PDnA = 11). Analog circuitry is turned off.
- The volatile DAC register is forced to 000h.
- The volatile Configuration bits, VRnB:VRnA and Gn, are forced to '0'.

As the voltage recovers and crosses above the V_{POR}/V_{BOR} voltage threshold, see **Section 4.2.1, "Power-on Reset"** for further details.

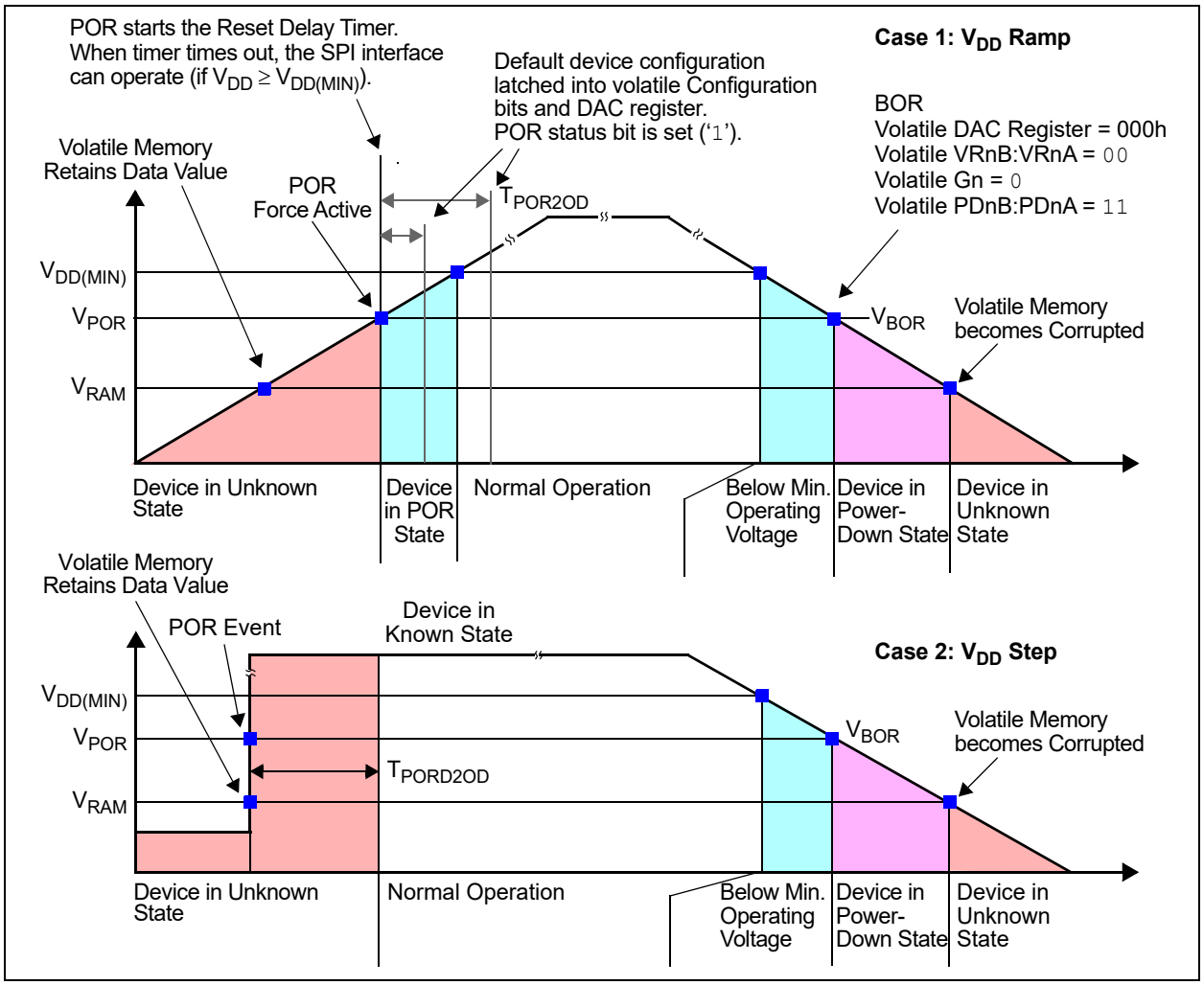

FIGURE 4-1: *Power-on/Brown-out Reset Operation.*

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4.3 Device Memory

The user memory includes the following types:

- **Volatile Register Memory (RAM)**
- **Nonvolatile Register Memory (MTP)**

MTP memory is only present for the MCP48CMBXX devices and has three groupings:

- NV DAC output values (loaded on POR event)
- Device configuration memory
- General purpose NV memory

Each memory location is up to 16 bits wide. The memory-mapped register space is shown in Table 4-1.

Memory reading and writing depends on the serial interface. Refer to **Section 4.5, "Serial Communication Interface"** and **Section 4.6, "Device Commands"** for more details on reading and writing the device's memory.

4.3.1 VOLATILE REGISTER MEMORY (RAM)

The MCP48CXBX4/8 devices have volatile memory to directly control the operation of the DACs. There are up to eleven volatile memory locations:

- DACn Output Value registers
- VREF Select register
- Power-Down Configuration register
- Gain and Status register

The volatile memory starts functioning when the device V_{DD} is at (or above) the RAM retention voltage (V_{RAM}). The volatile memory will be loaded with the default device values when the V_{DD} rises across the V_{POR}/V_{BOR} voltage trip point.

After the device is powered-up, the user can update the device memory. Table 4-2 shows the volatile memory locations and their interaction due to a POR event.

TABLE 4-1: MCP48CXBX4/8 MEMORY MAP (16-BIT)

Address	Function	Quad(1)	Octal(1)	Address	Function	Quad(1)	Octal(1)
00h	Volatile DAC Wiper Register 0	Y	Y	10h	Nonvolatile DAC Wiper Register 0	Y	Y
01h	Volatile DAC Wiper Register 1	Y	Y	11h	Nonvolatile DAC Wiper Register 1	Y	Y
02h	Volatile DAC Wiper Register 2	Y	Y	12h	Nonvolatile DAC Wiper Register 2	Y	Y
03h	Volatile DAC Wiper Register 3	Y	Y	13h	Nonvolatile DAC Wiper Register 3	Y	Y
04h	Volatile DAC Wiper Register 4	—	Y	14h	Nonvolatile DAC Wiper Register 4	—	Y
05h	Volatile DAC Wiper Register 5	—	Y	15h	Nonvolatile DAC Wiper Register 5	—	Y
06h	Volatile DAC Wiper Register 6	—	Y	16h	Nonvolatile DAC Wiper Register 6	—	Y
07h	Volatile DAC Wiper Register 7	—	Y	17h	Nonvolatile DAC Wiper Register 7	—	Y
08h	Volatile VREF Register	Y	Y	18h	Nonvolatile VREF Register	Y	Y
09h	Volatile Power-Down Register	Y	Y	19h	Nonvolatile Power-Down Register	Y	Y
0Ah	Volatile Gain and Status Register	Y	Y	1Ah	Nonvolatile Gain Register	Y	Y
0Bh	Reserved	—	—	1Bh	NV WiperLock™ Technology Register	Y	Y
0Ch	General Purpose MTP	**Note 1**		1Ch	General Purpose MTP	**Note 1**	
0Dh	General Purpose MTP	**Note 1**		1Dh	General Purpose MTP	**Note 1**	
0Eh	General Purpose MTP	**Note 1**		1Eh	General Purpose MTP	**Note 1**	
0Fh	General Purpose MTP	**Note 1**		1Fh	General Purpose MTP	**Note 1**	

Legend:

	Volatile Memory Addresses
	MTP Memory Addresses
	Memory Locations Not Implemented

Note 1: On nonvolatile memory devices only (MCP48CMBXX).

4.3.2 NONVOLATILE REGISTER MEMORY (MTP)

This memory option is available only for the MCP48CMBXX devices.

The MTP memory starts functioning below the device's V_{POR}/V_{BOR} trip point and, once the V_{POR} event occurs, the volatile memory registers are loaded with the corresponding MTP register memory values.

Memory addresses, 0Ch through 1Fh, are nonvolatile memory locations. These registers contain the DAC POR/BOR wiper values, the DAC POR/BOR Configuration bits and eight general purpose memory addresses for storing user-defined data as calibration constants or identification numbers. The nonvolatile DAC Wiper registers and Configuration bits contain the user's DAC output and configuration values for the POR event.

The Nonvolatile DAC Wiper registers contain the user's DAC output and configuration values for the POR event. These nonvolatile values will overwrite the factory default values. If these MTP addresses are unprogrammed, the factory default values define the output state.

The nonvolatile DAC registers enable the stand-alone operation of the device (without microcontroller control) after being programmed to the desired values.

To program nonvolatile memory locations, a high-voltage source on the $\overline{LAT}$/HVC pin is required. Each register/MTP location can be programmed 32 times. After 32 writes, a new write operation will not be possible and the last successful value written will remain associated with the memory location.

The device starts writing the MTP memory cells at the completion of the serial interface command at the rising edge of the last data bit. The high voltage must remain present on the $\overline{LAT}$/HVC pin until the write cycle is complete; otherwise, the write is unsuccessful and the location is compromised (cannot be used again and the number of available writes decreases by one).

To recover from an aborted MTP write operation, the following procedure must be used:

1. Write any valid value to the same address again.
2. Force a POR condition.
3. Write the desired value to the MTP location again.

It is recommended to keep high voltage on only during the MTP write command and programming cycle, otherwise the reliability of the device could be affected.

4.3.3 POR/BOR OPERATION WITH WIPERLOCK™ TECHNOLOGY ENABLED

Regardless of the WiperLock technology state, a POR event will load the volatile DACn Wiper register value with the nonvolatile DACn Wiper register value. See **Section 4.2, "Power-on Reset/Brown-out Reset Module"** for further information.

4.3.4 UNIMPLEMENTED LOCATIONS

4.3.4.1 Unimplemented Register Bits

When issuing read commands to a valid memory location with unimplemented bits, the unimplemented bits will be read as '0'.

4.3.4.2 Unimplemented (RESERVED) Registers

There are a number of unimplemented memory locations that are reserved for future use. Normal (voltage) commands (read or write) to any unimplemented memory address will result in a command error condition (CMDERR).

High-voltage commands to any unimplemented Configuration bit(s) will also result in a command error condition.

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TABLE 4-2: FACTORY DEFAULT POR/BOR VALUES (MTP MEMORY UNPROGRAMMED)

Address	Function	POR/BOR Value		
		8-Bit	10-Bit	12-Bit
00h	Volatile DAC0 Wiper Register	7Fh	1FFh	7FFh
01h	Volatile DAC1 Wiper Register	7Fh	1FFh	7FFh
02h	Volatile DAC2 Wiper Register	7Fh	1FFh	7FFh
03h	Volatile DAC3 Wiper Register	7Fh	1FFh	7FFh
04h	Volatile DAC4 Wiper Register	7Fh	1FFh	7FFh
05h	Volatile DAC5 Wiper Register	7Fh	1FFh	7FFh
06h	Volatile DAC6 Wiper Register	7Fh	1FFh	7FFh
07h	Volatile DAC7 Wiper Register	7Fh	1FFh	7FFh
08h	Volatile VREF Register	0000h	0000h	0000h
09h	Volatile Power-Down Register	0000h	0000h	0000h
0Ah	Volatile Gain and Status Register(3)	0080h	0080h	0080h
0Bh	Reserved(2)	0000h	0000h	0000h
0Ch	General Purpose MTP(1)	0000h	0000h	0000h
0Dh	General Purpose MTP(1)	0000h	0000h	0000h
0Eh	General Purpose MTP(1)	0000h	0000h	0000h
0Fh	General Purpose MTP(1)	0000h	0000h	0000h

Address	Function	POR/BOR Value		
		8-Bit	10-Bit	12-Bit
10h	Nonvolatile DAC0 Wiper Register(1)	7Fh	1FFh	7FFh
11h	Nonvolatile DAC1 Wiper Register(1)	7Fh	1FFh	7FFh
12h	Nonvolatile DAC2 Wiper Register(1)	7Fh	1FFh	7FFh
13h	Nonvolatile DAC3 Wiper Register(1)	7Fh	1FFh	7FFh
14h	Nonvolatile DAC4 Wiper Register(1)	7Fh	1FFh	7FFh
15h	Nonvolatile DAC5 Wiper Register(1)	7Fh	1FFh	7FFh
16h	Nonvolatile DAC6 Wiper Register(1)	7Fh	1FFh	7FFh
17h	Nonvolatile DAC7 Wiper Register(1)	7Fh	1FFh	7FFh
18h	Nonvolatile VREF Register(1)	0000h	0000h	0000h
19h	Nonvolatile Power-Down Register(1)	0000h	0000h	0000h
1Ah	NV Gain (1)	0060h	0060h	0060h
1Bh	NV WiperLock™ Technology Register(1)	0000h	0000h	0000h
1Ch	General Purpose MTP(1)	0000h	0000h	0000h
1Dh	General Purpose MTP(1)	0000h	0000h	0000h
1Eh	General Purpose MTP(1)	0000h	0000h	0000h
1Fh	General Purpose MTP(1)	0000h	0000h	0000h

Legend:

- Volatile Memory Address Range
- Nonvolatile Memory Address Range
- Not Implemented

Note 1: On nonvolatile devices only (MCP48CMBXX).

2: Reading a reserved memory location will result in a CMDERR condition on the SPI serial interface.

3: The '1' bit is the POR status bit, which is set after the POR event and cleared after address 0Ah is read.

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4.3.5 DEVICE REGISTERS

Register 4-1 shows the format of the DAC Output Value registers for the volatile memory locations. These registers are 8 bits, 10 bits or 12 bits wide. The values are right justified.

REGISTER 4-1: DAC0 TO DAC7 OUTPUT VALUE REGISTERS ADDRESSES 00H THROUGH 07H/10H THROUGH 17H (VOLATILE/NONVOLATILE)

	U-0	U-0	U-0	U-0	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n
12-bit	—	—	—	—	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
10-bit	—	—	—	—	—(1)	—(1)	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
8-bit	—	—	—	—	—(1)	—(1)	—(1)	—(1)	D07	D06	D05	D04	D03	D02	D01	D00
	bit 15															bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
= 12-bit device	= 10-bit device	= 8-bit device	

12-bit	**10-bit**	**8-bit**	
bit 15-12	bit 15-10	bit 15-8	**Unimplemented:** Read as '0'
bit 11-0	—	—	**D11:D00:** DAC Output Value bits – 12-bit devices FFFh = Full-Scale output value 7FFh = Mid-Scale output value 000h = Zero-Scale output value
—	bit 9-0	—	**D09:D00:** DAC Output Value bits – 10-bit devices 3FFh = Full-Scale output value 1FFh = Mid-Scale output value 000h = Zero-Scale output value
—	—	bit 7-0	**D07:D00:** DAC Output Value bits – 8-bit devices FFh = Full-Scale output value 7Fh = Mid-Scale output value 00h = Zero-Scale output value

Note 1: Unimplemented bit, read as '0'.

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Register 4-2 shows the format of the Voltage Reference Control register. Each DAC has two bits to control the source of the DAC's voltage reference. This register is for the volatile memory locations. The width of this register is two times the number of DACs for the device.

REGISTER 4-2: VOLTAGE REFERENCE (VREF) CONTROL REGISTER ADDRESSES 08H/18H (VOLATILE/NONVOLATILE)

	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n
Octal	VR7B	VR7A	VR6B	VR6A	VR5B	VR5A	VR4B	VR4A	VR3B	VR3A	VR2B	VR2A	VR1B	VR1A	VR0B	VR0A
Quad	—(1)	—(1)	—(1)	—(1)	—(1)	—(1)	—(1)	—(1)	VR3B	VR3A	VR2B	VR2A	VR1B	VR1A	VR0B	VR0A
	bit 15															bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
= Quad-channel device	= Octal-channel device		

Octal	**Quad**	
—	bit 15-8	**Unimplemented:** Read as '0'
bit 15-0	bit 7-0	**VRnB:VRnA:** DAC Voltage Reference Control bits 11 =V_{REF} pin (buffered); V_{REF} buffer enabled 10 =V_{REF} pin (unbuffered); V_{REF} buffer disabled 01 =Internal band gap; V_{REF} buffer enabled, V_{REF} voltage driven when powered down(2) 00 =V_{DD} (unbuffered); V_{REF} buffer disabled, use this state with power-down bits for lowest current

Note 1: Unimplemented bit, read as '0'.

2: When the internal band gap is selected, the band gap voltage source will continue to output the voltage on the V_{REF} pin in any of the Power-Down modes. To reduce the power consumption to its lowest level (band gap disabled), after selecting the desired Power-Down mode, the voltage reference must be changed to V_{DD} or the V_{REF} pin unbuffered ('00' or '10'), which turns off the internal band gap circuitry. After wake-up, the user needs to reselect the internal band gap ('01') for the voltage reference source.

Register 4-3 shows the format of the Power-Down Control register. Each DAC has two bits to control the Power-Down state of the DAC. This register is for both volatile and nonvolatile memory locations. The width of this register is two times the number of DACs for the device.

REGISTER 4-3: POWER-DOWN CONTROL REGISTER ADDRESSES 09H/19H (VOLATILE/NONVOLATILE)

	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n
Octal	PD7B	PD7A	PD6B	PD6A	PD5B	PD5A	PD4B	PD4A	PD3B	PD3A	PD2B	PD2A	PD1B	PD1A	PD0B	PD0A
Quad	—(1)	—(1)	—(1)	—(1)	—(1)	—(1)	—(1)	—(1)	PD3B	PD3A	PD2B	PD2A	PD1B	PD1A	PD0B	PD0A
	bit 15															bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
= Quad-channel device	= Octal-channel device		

Octal	Quad	
—	bit 15-8	**Unimplemented:** Read as '0'
bit 15-0	bit 7-0	**PDnB:PDnA:** DAC Power-Down Control bits(2) 11 =Powered down – V_{OUT} is open circuit 10 =Powered down – V_{OUT} is loaded with a 100 kΩ resistor to ground 01 =Powered down – V_{OUT} is loaded with a 1 kΩ resistor to ground 00 =Normal operation (not powered down)

Note 1: Unimplemented bit, read as '0'.

2: See Table 4-7 for more details.

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Register 4-4 shows the format of the Gain Control and System Status register. Each DAC has one bit to control the gain of the DAC and two Status bits.

REGISTER 4-4: GAIN CONTROL AND SYSTEM STATUS REGISTER ADDRESS 0AH (VOLATILE)

	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/C-1	R	U-0	U-0	U-0	U-0	U-0	U-0
Octal	G7	G6	G5	G4	G3	G2	G1	G0	POR	MTPMA	—	—	—	—	—	—
Quad	—(1)	—(1)	—(1)	—(1)	G3	G2	G1	G0	POR	MTPMA	—	—	—	—	—	—
	bit 15															bit 0

Legend:			
R = Readable bit	W = Writable bit	C = Clearable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
= Quad-channel device	= Octal-channel device		

Octal	**Quad**	
—	bit 15-12	**Unimplemented:** Read as '0'
bit 15-8	bit 11-8	**Gn:** DAC Channel n Output Driver Gain Control bit 1 = 2x gain; not applicable when V_{DD} is used as V_{RL}(2) 0 = 1x gain
bit 7	bit 7	**POR:** Power-on Reset (Brown-out Reset) Status bit This bit indicates if a POR or BOR event has occurred since the last read command of this register. Reading this register clears the state of the POR Status bit. 1 = A POR (BOR) event has occurred since the last read of this register; reading this register clears this bit. 0 = A POR (BOR) event has not occurred since the last read of this register.
bit 6	bit 6	**MTPMA:** MTP Memory Access Status bit(3) This bit indicates if the MTP memory access occurs. 1 = An MTP memory access is currently occurring (during the POR MTP read cycle or an MTP write cycle is occurring); only serial commands addressing the volatile memory are allowed. 0 = An MTP memory access is NOT currently occurring.
bit 5-0	bit 5-0	**Unimplemented:** Read as '0'

Note 1: Unimplemented bit, read as '0'.

2: The DAC's Gain bit is ignored and the gain is forced to 1x (Gn = 0) when the DAC voltage reference is selected as V_{DD} (VRnB:VRnA = 00).

3: For devices configured as volatile memory, this bit is read as '0'.

Register 4-5 shows the format of the Nonvolatile Gain Control register. Each DAC has one bit to control the gain of the DAC.

REGISTER 4-5: GAIN CONTROL REGISTER ADDRESS 1AH (NONVOLATILE)

	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
Octal	G7	G6	G5	G4	G3	G2	G1	G0	—	—	—	—	—	—	—	—
Quad	—(1)	—(1)	—(1)	—(1)	G3	G2	G1	G0	—	—	—	—	—	—	—	—
	bit 15															bit 0

Legend:			
R = Readable bit	W = Writable bit	C = Clearable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
= Quad-channel device	= Octal-channel device		

Octal	Quad	
—	bit 15-12	**Unimplemented:** Read as '0'
bit 15-8	bit 11-8	**Gn**: DAC Channel n Output Driver Gain Control bit(2) 1 = 2x gain 0 = 1x gain
bit 7-0	bit 7-0	**Unimplemented:** Read as '0'

Note 1: Unimplemented bit, read as '0'.

2: When the DAC voltage reference is selected as V_{DD} (VRnB:VRnA = 00), the DAC's Gain bit is ignored and the gain is forced to 1x (Gn = 0).

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Register 4-6 shows the format of the DAC WiperLock Technology Status register. The width of this register is two times the number of DACs for the device.

WiperLock technology bits only control access to volatile memory. Nonvolatile memory write access is controlled by the requirement of high voltage on the HVC pin, which is recommended to not be available during normal device operation.

REGISTER 4-6: WiperLock™ TECHNOLOGY CONTROL REGISTER ADDRESS 1Bh (NONVOLATILE)

	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n
Octal	WL7B	WL7A	WL6B	WL6B	WL5A	WL5B	WL4A	WL4B	WL3A	WL3B	WL2A	WL2B	WL1B	WL1A	WL0B	WL0A
Quad	—(1)	—(1)	—(1)	—(1)	—(1)	—(1)	—(1)	—(1)	WL3A	WL3B	WL2A	WL2B	WL1B	WL1A	WL0B	WL0A
	bit 15															bit 0

Legend:			
R = Readable bit	W = Writable bit	C = Clearable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
= Quad channel device	= Octal channel device		

Octal	**Quad**	
—	bit 15-8	**Unimplemented:** Read as '0'
bit 15-0	bit 7-0	**WLnB:WLnA:** WiperLock™ Technology Status bits(2) 11 = Volatile DAC Wiper register and volatile DAC Configuration bits are locked 10 = Volatile DAC Wiper register is locked and volatile DAC Configuration bits are unlocked 01 = Volatile DAC Wiper register is unlocked and volatile DAC Configuration bits are locked 00 = Volatile DAC Wiper register and volatile DAC Configuration bits are unlocked

Note 1: Unimplemented bit, read as '0'.

2: The volatile PDnB:PDnA bits are NOT locked due to the requirement of being able to exit Power-Down mode.

4.4 DAC Circuitry

The Digital-to-Analog Converter circuitry converts a digital value into its analog representation. This section describes the functional operation of the device.

The DAC architecture is based on a resistor ladder implementation. Devices have up to eight DACs. Figure 4-2 shows the functional block diagram for the MCP48CXBX4/8 DAC circuitry.

The functional blocks of the DAC circuitry include:

- **Resistor Ladder**
- **Voltage Reference Selection**
- **Output Driver**
- **Latch Pins (LATn)**
- **Power-Down Control**

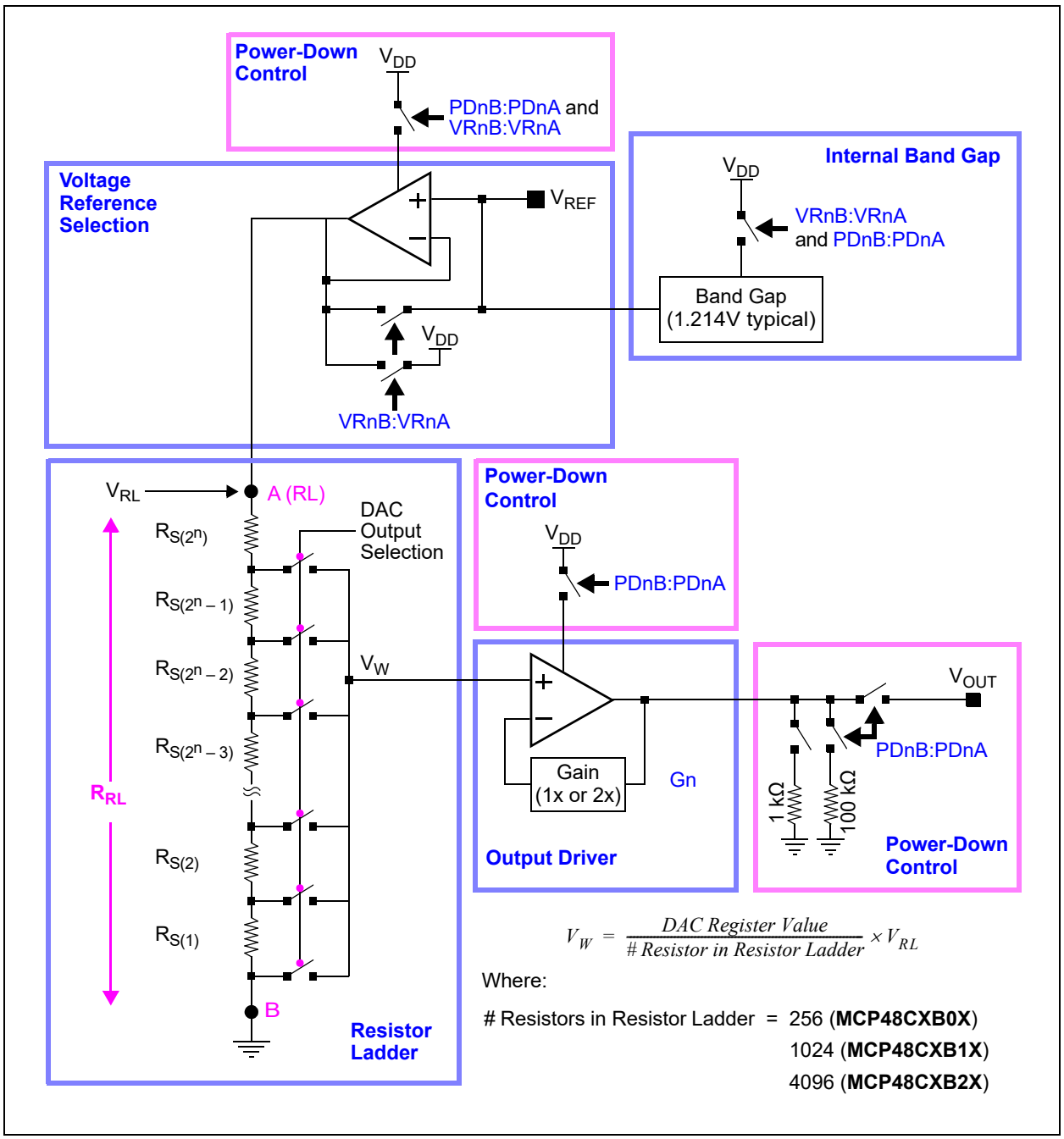

FIGURE 4-2: *MCP48CXBX4/8 DAC Circuitry Functional Block Diagram.*

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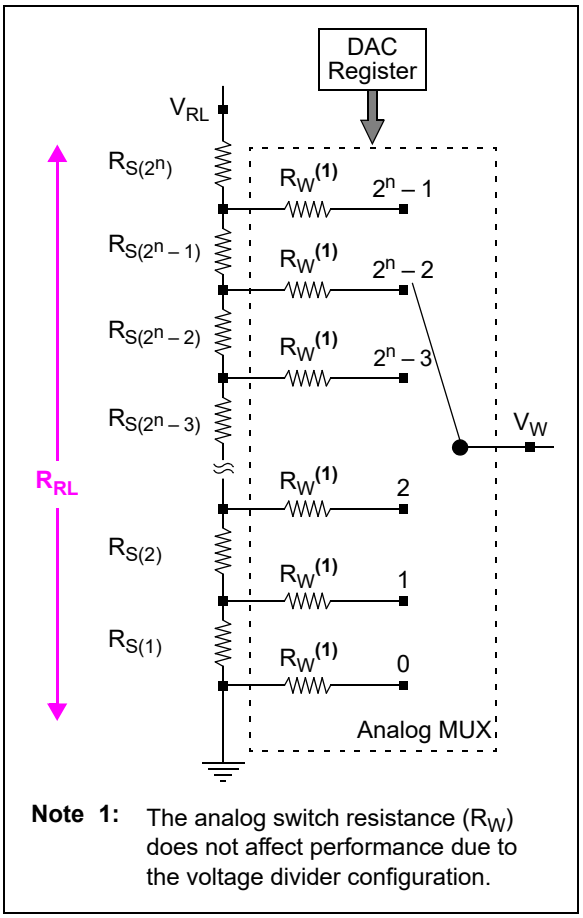
4.4.1 RESISTOR LADDER

The resistor ladder is a digital potentiometer with the A Terminal connected to the selected reference voltage and the B Terminal internally grounded (see Figure 4-3). The volatile DAC register controls the wiper position. The wiper voltage (V_W) is proportional to the DAC register value divided by the number of resistor elements (R_S) in the ladder (256, 1024 or 4096) related to the V_{RL} voltage.



Note 1: The analog switch resistance (R_W) does not affect performance due to the voltage divider configuration.

FIGURE 4-3: *Resistor Ladder Model Block Diagram.*

The output of the resistor network will drive the input of an output buffer.

The resistor network has three parts:

- Resistor ladder (string of R_S elements)
- Wiper switches
- DAC register decode

The resistor ladder has a typical impedance (R_{RL}) of approximately 73.5 kΩ. This resistor ladder resistance (R_{RL}) may vary from device to device, up to ±15%. Since this is a voltage divider configuration, the actual R_{RL} resistance does not affect the output, given a fixed voltage at V_{RL}.

Equation 4-1 shows the calculation for the step resistance.

EQUATION 4-1: R_S CALCULATION

$$R_S = \frac{R_{RL}}{(256)} \quad \textit{8-bit Device}$$

$$R_S = \frac{R_{RL}}{(1024)} \quad \textit{10-bit Device}$$

$$R_S = \frac{R_{RL}}{(4096)} \quad \textit{12-bit Device}$$

Note: The maximum wiper position is $2^n - 1$, while the number of resistors in the resistor ladder is 2^n. This means that when the DAC register is at full scale, there is one resistor element (R_S) between the wiper and the V_{RL} voltage.

If the unbuffered V_{REF} pin is used as the V_{RL} voltage source, the external voltage source must have a low output impedance.

When the DAC is powered down, the resistor ladder is disconnected from the selected reference voltage.

4.4.2 VOLTAGE REFERENCE SELECTION

The resistor ladder has up to four sources for the reference voltage. The selection of the voltage reference source is specified with the volatile VRnB:VRnA Configuration bits (see Register 4-2). The selected voltage source is connected to the V_{RL} node (see Figure 4-3 and Figure 4-4).

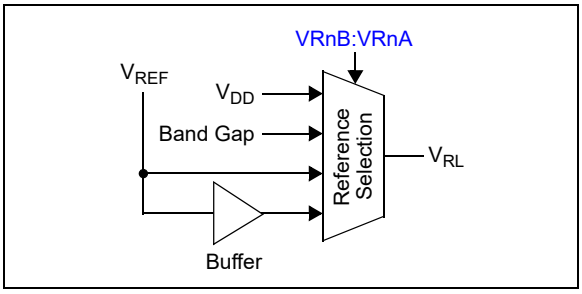


FIGURE 4-4: *Resistor Ladder Reference Voltage Selection Block Diagram.*

The four voltage source options for the resistor ladder are:

1. V_{DD} pin voltage
2. Internal band gap voltage reference (V_{BG})
3. V_{REF} pin voltage – unbuffered
4. V_{REF} pin voltage – internally buffered

On a POR/BOR event, the default configuration state or the value written in the nonvolatile register is latched into the volatile VRnB:VRnA Configuration bits.

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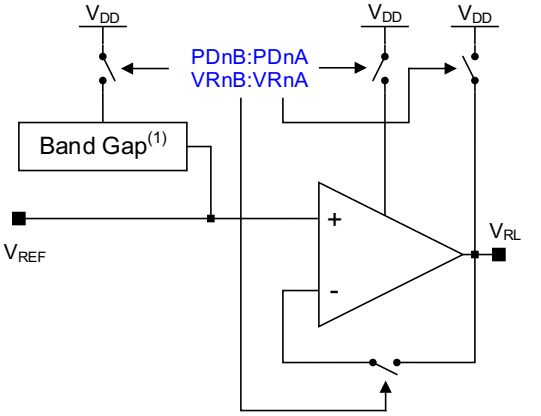

Note 1: The band gap voltage (V_{BG}) is 1.214V (typical). The band gap output goes through the buffer with a 2x gain to create the V_{RL} voltage. See Table 4-3 for additional information on the band gap circuit.

FIGURE 4-5: *Reference Voltage Selection Implementation Block Diagram.*

If the V_{REF} pin is used with an external voltage source, then the user must select between Buffered or Unbuffered mode.

4.4.2.1 Using V_{DD} as V_{REF}

When the user selects the V_{DD} as reference, the V_{REF} pin voltage is not connected to the resistor ladder. The V_{DD} voltage is internally connected to the resistor ladder.

4.4.2.2 Using an External V_{REF} Source in Unbuffered Mode

In this case, the V_{REF} pin voltage may vary from V_{SS} to V_{DD}. The voltage source must have a low output impedance. If the voltage source has a high output impedance, then the voltage on the V_{REF} pin could be lower than expected. The resistor ladder has a typical impedance of 73.5 kΩ and a typical capacitance of 29 pF.

If a single V_{REF} pin supplies multiple DACs, the V_{REF} pin source must have adequate current capability to support the number of DACs. It must be assumed that the resistor ladder resistance (R_{RL}) of each DAC is at the minimum specified resistance and these resistances are in parallel.

If the V_{REF} pin is tied to the V_{DD} voltage, selecting the V_{DD} Reference mode (VRnB:VRnA = 00) is recommended.

4.4.2.3 Using an External V_{REF} Source in Buffered Mode

The V_{REF} pin voltage may be from 0V to V_{DD}. The input buffer (amplifier) provides low offset voltage, low noise and a very high input impedance, with only minor limitations on the input range and frequency response.

Any variation or noises on the reference source can directly affect the DAC output. The reference voltage needs to be as clean as possible for accurate DAC performance.

4.4.2.4 Using the Internal Band Gap as Voltage Reference

The internal band gap is designed to drive the resistor ladder buffer.

If the internal band gap is selected, the band gap voltage source will drive the external V_{REF} pins. The V_{REF0} pin can source up to 1 mA of current without affecting the DAC output specifications. The V_{REF1} pin must be left unloaded in this mode. The voltage reference source can be independently selected, but restrictions apply:

- The V_{DD} mode can be used without issues on any channel.
- When the internal band gap is selected as the voltage source, all the V_{REF} pins are connected to its output. The use of the Unbuffered mode is only possible on V_{REF0}, because it's the only one that can be loaded.
- When using the Internal Band Gap mode on Channel 0, Channels 1, 3, 5 and 7 must be put in Buffered External V_{REF} mode or V_{DD} Reference mode and the V_{REF1} pin must be left unloaded.

The resistance of the resistor ladder (R_{RL}) is targeted to be 73.5 kΩ (±15%), which means a minimum resistance of 62.475 kΩ. The band gap selection can be used across the V_{DD} voltages while maximizing the V_{OUT} voltage ranges. For V_{DD} voltages below the Gain ∗ V_{BG} voltage, the output for the upper codes will be clipped to the V_{DD} voltage.

Table 4-3 shows the maximum DAC register code given device V_{DD} and Gain bit setting.

TABLE 4-3: V_{OUT} USING BAND GAP

V_{DD}	DAC Gain	Max DAC Code(1)			Comment
		12-Bit	10-Bit	8-Bit	
5.5	1	FFFh	3FFh	FFh	$V_{OUT(max)}$ = 1.214V(3)
	2	FFFh	3FFh	FFh	$V_{OUT(max)}$ = 2.428V(3)
2.7	1	FFFh	3FFh	FFh	$V_{OUT(max)}$ = 1.214V(3)
	2	FFFh	3FFh	FFh	$V_{OUT(max)}$ = 2.428V
1.8	1	FFFh	3FFh	FFh	$V_{OUT(max)}$ = 1.214V
	2(2)	BBCh	2EFh	BBh	1.8V

Note 1: Without the V_{OUT} pin voltage being clipped.
2: Recommended to use the Gain = 1 setting.
3: When V_{BG} = 1.214V typical.

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4.4.3 OUTPUT DRIVER

The output driver buffers the wiper voltage (V_W) of the resistor ladder. Figure 4-6 shows a block diagram of the output driver circuit.

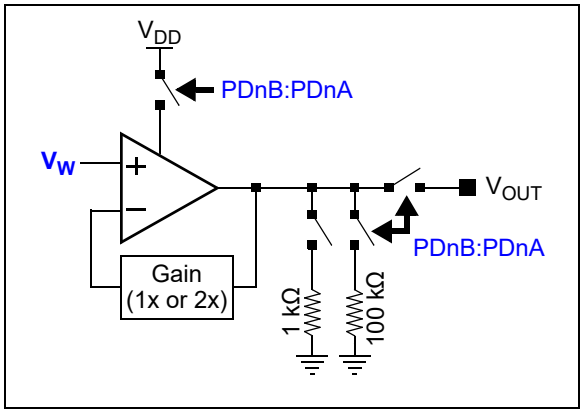

FIGURE 4-6: *Output Driver Block Diagram.*

The DAC output is buffered with a low-power, precision output amplifier with selectable gain. This amplifier provides a rail-to-rail output with low offset voltage and low noise. The amplifier's output can drive the resistive and high-capacitive loads without oscillation.

Note:	The load resistance must be kept higher than 2 kΩ to maintain stability of the analog output and have it meet electrical specifications.

The amplifier provides a maximum load current, which is enough for most programmable voltage reference applications. See **Section 1.0, "Electrical Characteristics"** for the specifications of the output amplifier. Power-down logic also controls the output buffer operation (see **Section 4.4.5, "Power-Down Control"** for additional information on power-down). In any of the three Power-Down modes, the output amplifier is powered down and its output becomes a high-impedance to the V_{OUT} pin.

4.4.3.1 Programmable Gain

The amplifier's gain is controlled by the Gain (Gn) Configuration bits (see Register 4-4) and the V_{RL} reference selection (see Register 4-2).

The gain options are:

a) Gain of 1, with either the V_{DD} or the V_{REF} pin used as the reference voltage.

b) Gain of 2, only when the V_{REF} pin or the internal band gap is used as the reference voltage. The V_{REF} pin voltage must be limited to $V_{DD}/2$. When the reference voltage selection (V_{RL}) is the device's V_{DD} voltage, the Gn bit is ignored and a gain of 1 is used.

Table 4-4 shows the gain bit operation.

TABLE 4-4: OUTPUT DRIVER GAIN

Gain Bit	Gain	Comment
0	1	
1	2	Limits V_{REF} pin voltages relative to device V_{DD} voltage.

The volatile G bit value can be modified by:

- POR event
- BOR event
- SPI write command (to volatile registers)

4.4.3.2 Output Voltage

The volatile DAC register values, along with the device's Configuration bits, control the analog V_{OUT} voltage. The volatile DAC register's value is unsigned binary. The formula for the output voltage is provided in Equation 4-2.

EQUATION 4-2: CALCULATING OUTPUT VOLTAGE (V_{OUT})

$$V_{OUT} = \frac{V_{RL} \times DAC\ Register\ Value}{\#\ Resistor\ in\ Resistor\ Ladder} \times Gain$$

Where:

 # Resistors in R Ladder = 4096 (MCP48CXB2X)
1024 (MCP48CXB1X)
256 (MCP48CXB0X)

Examples of volatile DAC register values and the corresponding theoretical V_{OUT} voltage for the MCP48CXBX4/8 devices are shown in Table 4-8.

When Gain = 2 (V_{RL} = V_{REF}), if $V_{REF} > V_{DD}/2$, the V_{OUT} voltage is limited to V_{DD}. So if $V_{REF} = V_{DD}$, the V_{OUT} voltage does not change for Volatile DAC register values mid-scale and greater, since the output amplifier is at full-scale output.

The following events update the DAC register value, and therefore, the analog voltage output (V_{OUT}):

- POR
- BOR
- SPI write command (to volatile registers)

Next, the V_{OUT} voltage starts driving to the new value after the event has occurred.

4.4.3.3 Output Slew Rate

Figure 4-7 shows an example of the slew rate of the V_{OUT} pin.

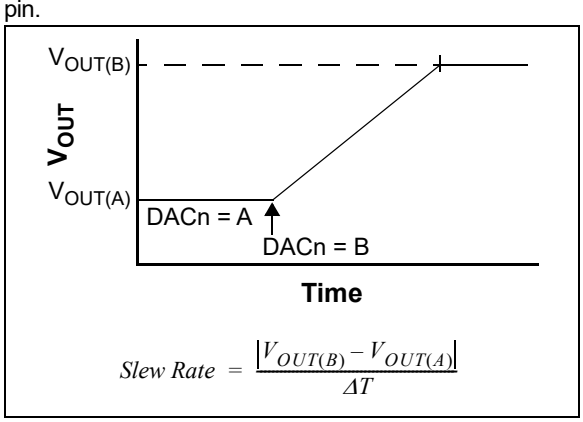

FIGURE 4-7: *V_{OUT} Pin Slew Rate.*

The slew rate can be affected by the characteristics of the circuit connected to the V_{OUT} pin.

4.4.3.4 Driving Small Capacitive Loads

With a small capacitive load, the output buffer's current is not affected by the capacitive load (C_L). But still, the V_{OUT} pin's voltage is not a step transition from one output value (DAC register value) to the next output value. The change of the V_{OUT} voltage is limited by the output buffer's characteristics, so the V_{OUT} pin voltage will have a slope from the old voltage to the new voltage. This slope is fixed for the output buffer and is referred to as the buffer slew rate (SR_{BUF}).

4.4.3.5 Driving Large Capacitive Loads

With a larger capacitive load, the slew rate is determined by two factors:

- The output buffer's short-circuit current (I_{SC})
- The V_{OUT} pin's external load

I_{OUT} cannot exceed the output buffer's short-circuit current (I_{SC}), which fixes the output buffer slew rate (SR_{BUF}). The voltage on the capacitive load (C_L), V_{CL}, changes at a rate proportional to I_{OUT}, which fixes a capacitive load slew rate (SR_{CL}).

The V_{CL} voltage slew rate is limited to the slower of the output buffer's internally set slew rate (SRBUF) and the capacitive load slew rate (SR_{CL}).

4.4.3.6 Step Voltage (V_S)

The step voltage can easily be calculated by using Equation 4-3 (the DAC register value is equal to '1').

EQUATION 4-3: V_S CALCULATION

$$V_S = \frac{V_{RL}}{\#\ Resistor\ in\ Resistor\ Ladder} \times Gain$$

Where:

 # Resistors in R Ladder = 4096 (12-bit)
1024 (10-bit)
256 (8-bit)

The step voltage depends on the device resolution and the calculated output voltage range. One LSb is defined as the ideal voltage difference between two successive codes. Theoretical step voltages are shown in Table 4-5 for several V_{REF} voltages.

TABLE 4-5: THEORETICAL STEP VOLTAGE (V_S)(1)

Step Voltage	V_{REF}					
	5.0	**2.7**	**1.8**	**1.5**	**1.0**	
V_S	1.22 mV	659 uV	439 uV	366 uV	244 uV	12-bit
	4.88 mV	2.64 mV	1.76 mV	1.46 mV	977 uV	10-bit
	19.5 mV	10.5 mV	7.03 mV	5.86 mV	3.91 mV	8-bit

Note 1: When Gain = 1x, $V_{FS} = V_{RL}$ and $V_{ZS} = 0V$.

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4.4.4 LATCH PINS ($\overline{LAT}$n)

The Latch pin controls when the volatile DAC register value is transferred to the DAC wiper. This is useful for applications that need to synchronize the wiper(s) updates to an external event, such as zero crossing or updates to the other wipers on the device. The $\overline{LAT}$ pin is asynchronous to the serial interface operation.

When the $\overline{LAT}$ pin is high, transfers from the volatile DAC register to the DAC wiper are inhibited. The volatile DAC register value(s) can continue to be updated.

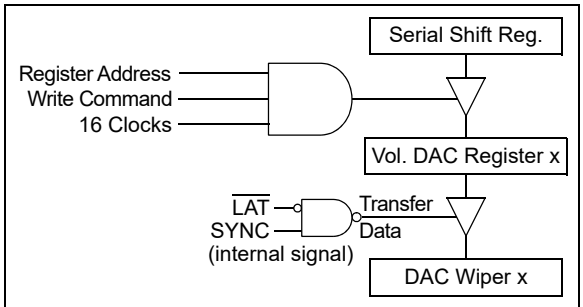
When the $\overline{LAT}$ pin is low, the volatile DAC register value is transferred to the DAC wiper.

This allows all the volatile wiper registers to be updated while the $\overline{LAT}$ pin is high and to have outputs synchronously updated as the $\overline{LAT}$ pin is driven low.

Figure 4-8 shows the interaction of the $\overline{LAT}$ pin and the loading of the DAC wiper x (from the volatile DAC register x). The transfers are level-driven. If the $\overline{LAT}$ pin is held low, the corresponding DAC wiper is updated as soon as the volatile DAC register value is updated.

The $\overline{LAT}$ pin allows the DAC wiper to be updated to an external event and to have multiple DAC channels/devices updated at a common event.

Since the DAC wiper x is updated from the volatile DAC register x, all DACs that are associated with a given $\overline{LAT}$ pin can be updated synchronously.



$\overline{LAT}$	SYNC	Transfer Data	Comment
1	1	0	No Transfer
1	0	0	No Transfer
0	1	1	Vol. DAC Register x → DAC Wiper x
0	0	0	No Transfer

FIGURE 4-8: *$\overline{LAT}$ and DAC Interaction.*

If the application does not require synchronization, this signal must be tied low.

Figure 4-9 shows two cases of using the $\overline{LAT}$ pin to control when the wiper register is updated, relative to the amplitude of a sine wave signal.

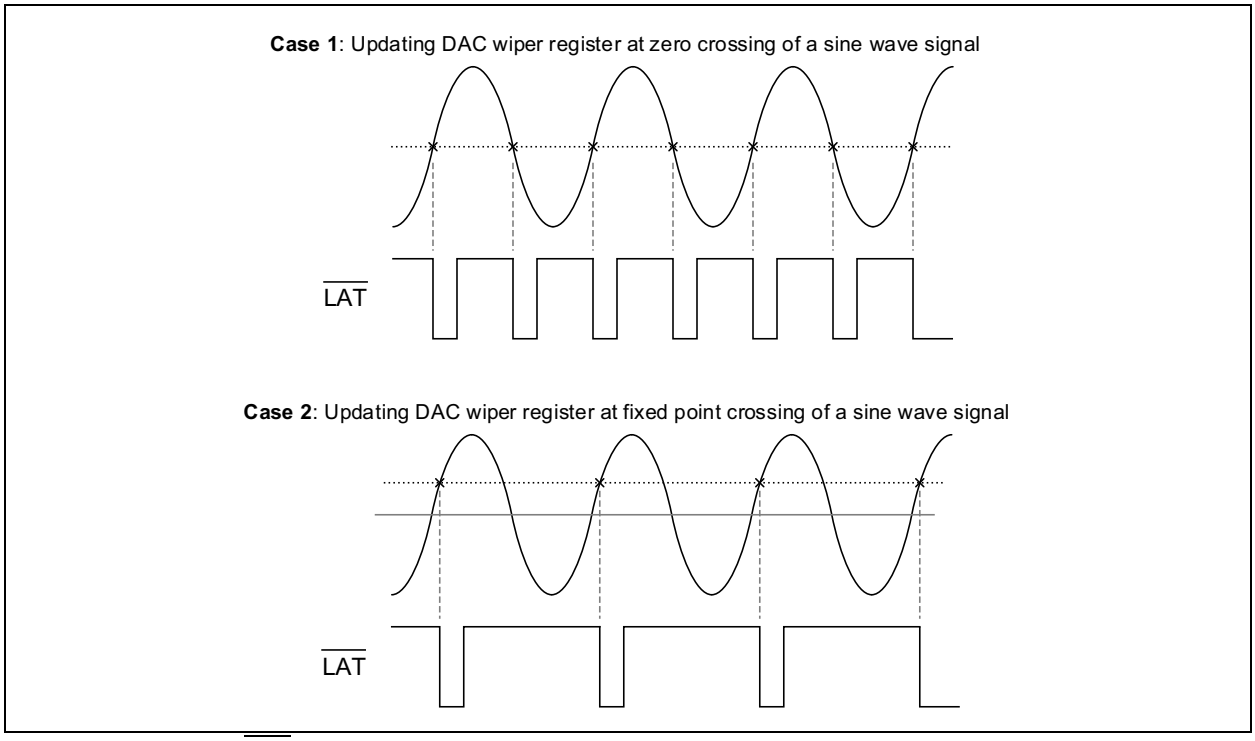


FIGURE 4-9: *$\overline{LAT}$ Pin Operation Example.*

4.4.5 POWER-DOWN CONTROL

To allow the application to conserve power when DAC operation is not required, three Power-Down modes are available. On devices with multiple DACs, each DAC's Power-Down mode is individually controllable.

All Power-Down modes do the following:

- Turn off most of the DAC module's internal circuits
- Op amp output becomes high-impedance to the V_{OUT} pin
- Retain the value of the volatile DAC register and Configuration bits

Depending on the selected Power-Down mode, the following will occur:

- V_{OUT} pin is switched to one of the two resistive pull-downs:
  - 100 kΩ (typical)
  - 1 kΩ (typical)
- Op amp is powered down and the V_{OUT} pin becomes high-impedance

The power-down Configuration bits (PDnB:PDnA) control the power-down operation (Table).

TABLE 4-6: POWER-DOWN BITS AND OUTPUT RESISTIVE LOAD

PDnB	PDnA	Function
0	0	Normal operation
0	1	1 kΩ resistor to ground
1	0	100 kΩ resistor to ground
1	1	Open circuit

There is a delay (T_{PDD}) between the PD1:PD0 bits changing from '00' to either '01', '10' or '11' and the op amp no longer driving the V_{OUT} output and the pull-down resistor's sinking current.

Table 4-7 shows the current sources for the DAC based on the selected source of the DAC's reference voltage and if the device is in normal operating mode or one of the Power-Down modes. In any of the Power-Down modes, where the V_{OUT} pin is not externally connected (sinking or sourcing current), as the number of DACs increases, the device's power-down current will also increase.

TABLE 4-7: DAC CURRENT SOURCES

Device V_{DD} Current Source	PDnB:nA = 00, VRnB:nA =				PDnB:nA ≠ 00, VRnB:nA =			
	00	01	10	11	00	01	10	11
Output Op Amp	Y	Y	Y	Y	N	N	N	N
Resistor Ladder	Y	Y	N(1)	Y	N	N	N(1)	N
V_{REF} Selection Buffer	N	Y	N	Y	N	N	N	N
Band Gap	N	Y	N	N	N(2)	Y(2)	N(2)	N(2)

Note 1: The current is sourced from the V_{REF} pin, not the device V_{DD}.
2: If any DAC channel is in one of the Power-Down modes, MTP write operations are not recommended.

The power-down bits are modified by using commands that write to the volatile power-down register or a POR event, which transfers the nonvolatile power-down register to the volatile power-down register.

Section 4.6, "Device Commands" describes the SPI commands for writing the power-down bits.

4.4.5.1 Exiting Power-Down

The following event changes the PDnB:PDnA bits to '00' and therefore exits the Power-Down mode: any SPI write command where the PDnB:PDnA bits are '00'.

When the device exits Power-Down mode, the following occur:

- Disabled internal circuits are turned on
- Resistor ladder is connected to the selected reference voltage (V_{RL})
- Selected pull-down resistor is disconnected
- The V_{OUT} output is driven to the voltage represented by the volatile DAC register's value and Configuration bits

The DAC wiper register and DAC wiper value may be different due to the DAC wiper register being modified while the $\overline{LAT}$ pin was driven to (and remaining at) V_{IH}.

The V_{OUT} output signal requires time as these circuits are powered up and the output voltage is driven to the specified value, as determined by the volatile DAC register and Configuration bits.

Note: Since the op amp and resistor ladder are powered off (0V), the op amp's input voltage (V_W) can be considered as 0V. There is a delay (T_{PDE}) between the PDnB:PDnA bits updating to '00' and the op amp driving the V_{OUT} output. The op amp's settling time (from 0V) needs to be taken into account to ensure the V_{OUT} voltage reflects the selected value.

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TABLE 4-8: DAC INPUT CODE VS. CALCULATED ANALOG OUTPUT (V_{OUT}) (V_{DD} = 5.0V)

Device	Volatile DAC Register Value	V_{RL}[1]	LSb		Gain Selection[2]	V_{OUT}[3]	
			Equation	µV		Equation	V
MCP48CVB2X (12-bit)	1111 1111 1111	5.0V	5.0V/4096	1,220.7	1x	$V_{RL} * (4095/4096) * 1$	4.998779
		2.5V	2.5V/4096	610.4	1x	$V_{RL} * (4095/4096) * 1$	2.499390
					2x[2]	$V_{RL} * (4095/4096) * 2$	4.998779
	0111 1111 1111	5.0V	5.0V/4096	1,220.7	1x	$V_{RL} * (2047/4096) * 1$	2.498779
		2.5V	2.5V/4096	610.4	1x	$V_{RL} * (2047/4096) * 1$	1.249390
					2x[2]	$V_{RL} * (2047/4096) * 2$	2.498779
	0011 1111 1111	5.0V	5.0V/4096	1,220.7	1x	$V_{RL} * (1023/4096) * 1$	1.248779
		2.5V	2.5V/4096	610.4	1x	$V_{RL} * (1023/4096) * 1$	0.624390
					2x[2]	$V_{RL} * (1023/4096) * 2$	1.248779
	0000 0000 0000	5.0V	5.0V/4096	1,220.7	1x	$V_{RL} * (0/4096) * 1$	0
		2.5V	2.5V/4096	610.4	1x	$V_{RL} * (0/4096) * 1$	0
					2x[2]	$V_{RL} * (0/4096) * 2$	0
MCP48CVB1X (10-bit)	11 1111 1111	5.0V	5.0V/1024	4,882.8	1x	$V_{RL} * (1023/1024) * 1$	4.995117
		2.5V	2.5V/1024	2,441.4	1x	$V_{RL} * (1023/1024) * 1$	2.497559
					2x[2]	$V_{RL} * (1023/1024) * 2$	4.995117
	01 1111 1111	5.0V	5.0V/1024	4,882.8	1x	$V_{RL} * (511/1024) * 1$	2.495117
		2.5V	2.5V/1024	2,441.4	1x	$V_{RL} * (511/1024) * 1$	1.247559
					2x[2]	$V_{RL} * (511/1024) * 2$	2.495117
	00 1111 1111	5.0V	5.0V/1024	4,882.8	1x	$V_{RL} * (255/1024) * 1$	1.245117
		2.5V	2.5V/1024	2,441.4	1x	$V_{RL} * (255/1024) * 1$	0.622559
					2x[2]	$V_{RL} * (255/1024) * 2$	1.245117
	00 0000 0000	5.0V	5.0V/1024	4,882.8	1x	$V_{RL} * (0/1024) * 1$	0
		2.5V	2.5V/1024	2,441.4	1x	$V_{RL} * (0/1024) * 1$	0
					2x[2]	$V_{RL} * (0/1024) * 1$	0
MCP48CVB0X (8-bit)	1111 1111	5.0V	5.0V/256	19,531.3	1x	$V_{RL} * (255/256) * 1$	4.980469
		2.5V	2.5V/256	9,765.6	1x	$V_{RL} * (255/256) * 1$	2.490234
					2x[2]	$V_{RL} * (255/256) * 2$	4.980469
	0111 1111	5.0V	5.0V/256	19,531.3	1x	$V_{RL} * (127/256) * 1$	2.480469
		2.5V	2.5V/256	9,765.6	1x	$V_{RL} * (127/256) * 1$	1.240234
					2x[2]	$V_{RL} * (127/256) * 2$	2.480469
	0011 1111	5.0V	5.0V/256	19,531.3	1x	$V_{RL} * (63/256) * 1$	1.230469
		2.5V	2.5V/256	9,765.6	1x	$V_{RL} * (63/256) * 1$	0.615234
					2x[2]	$V_{RL} * (63/256) * 2$	1.230469
	0000 0000	5.0V	5.0V/256	19,531.3	1x	$V_{RL} * (0/256) * 1$	0
		2.5V	2.5V/256	9,765.6	1x	$V_{RL} * (0/256) * 1$	0
					2x[2]	$V_{RL} * (0/256) * 2$	0

Note 1: V_{RL} is the resistor ladder's reference voltage. It is independent of the VRnB:VRnA selection.

2: Gain selection of 2x (Gn = 1) requires the voltage reference source to come from the V_{REF} pin (VRnB:VRnA = 10 or 11) and requires the V_{REF} pin voltage (or V_{RL}) ≤ $V_{DD}/2$ or from the internal band gap (VRnB:VRnA = 01).

3: These theoretical calculations do not take into account the offset, gain and nonlinearity errors.

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4.5 Serial Communication Interface

4.5.1 SPI SERIAL INTERFACE MODULE

The MCP48CXBX4/8's SPI serial interface module is a four-wire interface. The devices operate only as clients (do not generate the host clock). Figure 4-10 shows a typical SPI interface connection.

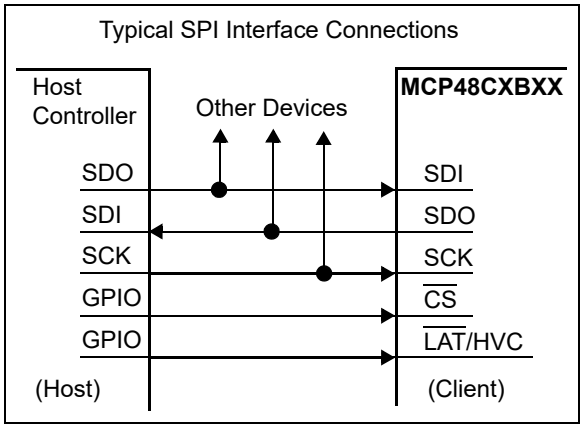

FIGURE 4-10: *Typical SPI Interface.*

The frame content (commands) for the MCP48CXBX4/8 is defined in **Section 4.6 "Device Commands"**.

4.5.1.1 Overview

This section discusses some of the specific characteristics of the MCP48CXBX4/8's SPI serial interface module. This is to assist in the development of your application.

The following sections discuss some of these device-specific characteristics:

- **Communication Data Rates**
- **POR/BOR**
- **Interface Pins (CS, SCK, SDI, SDO and LAT/HVC)**
- **Device Memory Address**
- **SPI Modes**

The MCP48CXBX4/8 devices support the SPI serial protocol. This SPI operates in Client mode (does not generate the serial clock).

The SPI interface uses four pins. These are:

- $\overline{CS}$ – Chip Select
- SCK – Serial Clock
- SDI – Serial Data In
- SDO – Serial Data Out

A fifth pin is used if a write is done in the MTP memory. This pin is HVC – High Voltage Command (customer manufacturing only, multiplexed with the $\overline{LAT0}$ functionality).

The HVC pin is used to program the MTP memory. This is intended to be used only during the customer's factory production flow. On volatile devices, the HVC pin is high-voltage tolerant. To enter a high voltage command, the HVC pin must be greater than the V_{IHH} voltage.

Typical SPI interfaces are shown in Figure 4-10. In the SPI interface, the Host's Output pin is connected to the Client's Input pin, and the Host's Input pin is connected to the Client's Output pin.

The MCP48CXBX4/8 SPI module supports two (of the four) standard SPI modes. These are modes `0,0` and `1,1`. The SPI mode is determined by the state of the SCK pin (V_{IH} or V_{IL}) when the $\overline{CS}$ pin transitions from inactive (V_{IH}) to active (V_{IL}).

4.5.1.2 Communication Data Rates

The MCP48CXBX4/8 supports clock rates (bit rates) of up to 25 MHz for read, and 50 MHz for write commands.

For most applications, the write time will be considered more important, since that is how the device operation is controlled.

4.5.1.3 POR/BOR

On a POR/BOR event, the SPI serial interface module state machine is reset, which includes forcing the device's Memory Address Pointer to 00h.

4.5.1.4 Interface Pins ($\overline{CS}$, SCK, SDI, SDO and $\overline{LAT}$/HVC)

The operation of the four interface pins and the HVC pin is discussed in this section. The serial interface works on 24-bit boundaries. The $\overline{CS}$ pin frames the SPI commands.

4.5.1.5 Serial Data In (SDI)

The Serial Data In (SDI) signal is the data signal in the device. The value on this pin is latched on the rising edge of the SCK signal.

4.5.1.6 Serial Data Out (SDO)

The Serial Data Out (SDO) signal is the data signal out of the device. The value on this pin is driven on the falling edge of the SCK signal.

Once the $\overline{CS}$ pin is forced to the active level (V_{IL}), the SDO pin is driven. The state of the SDO pin is determined by the serial bit's position in the command, the selected command and if there is a state of command error (CMDERR).

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4.5.1.7 Serial Clock (SCK) (SPI Frequency Of Operation)

The SPI interface is specified to operate up to 50 MHz for write commands and 25 MHz for read commands. The actual clock rate depends on the configuration of the system and the serial command used. Table 4-9 shows the SCK frequency for different configurations.

TABLE 4-9: SCK FREQUENCY

Memory Type Access		Command	
		Read	Write
Nonvolatile Memory	SDI, SDO	25 MHz	50 MHz(1)
Volatile Memory	SDI, SDO	25 MHz	50 MHz(1)

Note 1: After issuing a write command to the NV locations, the internal write cycle must be completed before the next SPI command addressing the NV locations is received (t_{WC}).

4.5.1.8 $\overline{CS}$ Signal

The $\overline{CS}$ signal is used to select the device and frame a command sequence. To start a command, or sequence of commands, the $\overline{CS}$ signal must transition from the Inactive state (V_{IH}) to an Active state (V_{IL}).

After the $\overline{CS}$ signal goes active, the SDO pin is driven and the clock bit counter is reset.

Note: There is a required delay after the $\overline{CS}$ pin goes active to the first edge of the SCK pin.

If an error condition occurs for an SPI command, the Command byte's Command Error (CMDERR) bit (on the SDO pin) will be driven low (V_{IL}). To exit the error condition, the user must take the $\overline{CS}$ pin to the V_{IH} level.

When the $\overline{CS}$ pin returns to the Inactive state (V_{IH}), the SPI module resets (including the Address Pointer). While the $\overline{CS}$ pin is in the Inactive state (V_{IH}), the serial interface is ignored. This allows the Host Controller to interface to other SPI devices using the same SDI, SDO and SCK signals.

4.5.1.9 HVC Signal

The high-voltage requirement of the HVC pin for programming MTP registers ensures that a device in normal operation does not corrupt the values.

4.5.1.10 Device Memory Address

The memory address is the 5-bit value that specifies the location in the device's memory that the specified command will operate on.

On a POR/BOR event, the device's Memory Address Pointer is forced to 00h.

4.5.1.11 SPI Modes

The SPI module supports two (of the four) standard SPI modes. These are modes `0,0` and `1,1`. The MCP48CXBX4/8's SPI mode is automatically determined based on the host's configured mode.

4.5.1.12 Operation in SPI Mode 0,0

In SPI **Mode 0,0**:

- SCK Idle state = Low (V_{IL})
- Data are clocked in on the SDI pin on the rising edge of SCK
- Data are clocked out on the SDO pin on the falling edge of SCK

4.5.1.13 Operation in SPI Mode 1,1

In SPI **Mode 1,1**:

- SCK Idle state = High (V_{IH})
- Data are clocked in on the SDI pin on the rising edge of SCK
- Data are clocked out on the SDO pin on the falling edge of SCK

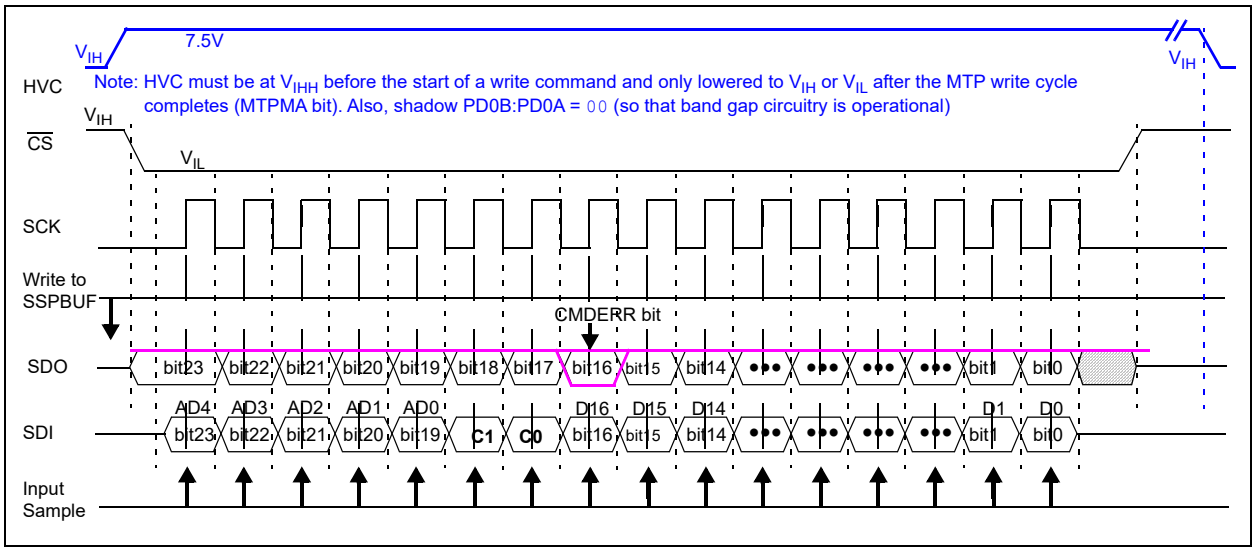

FIGURE 4-11: *24-Bit Commands (Write, Read) – SPI Waveform (Mode 0,0).*

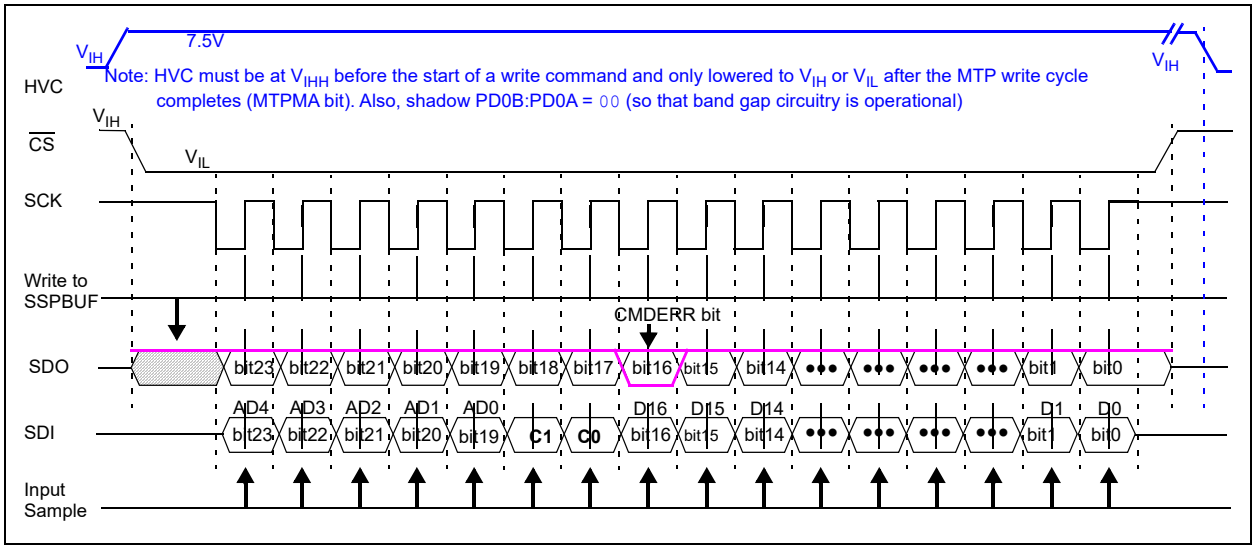

FIGURE 4-12: *24-Bit Commands (Write, Read) – SPI Waveform (Mode 1,1).*

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4.6 Device Commands

The MCP48CXBX4/8 devices' SPI command format supports 32 memory address locations and two commands. The command may have two modes. These are:

- Normal Serial Commands
- MTP Programming (HV) Serial Commands

Normal serial commands are those where the HVC pin is driven to either V_{IH} or V_{IL}. With high-voltage serial commands, the HVC pin is driven to 7.5V. These commands are shown in Table 4-10.

Table 4-10 shows an overview of all the SPI commands and their interaction with other device features.

The 24-bit commands (**Read Command** and **Write Command**) contain a command byte and a data word. The command byte contains one reserved bit (see Figure 4-13).

TABLE 4-10: COMMAND BITS OVERVIEW

Bit States C1:C0	Command	# of Bits	Normal or HV
11	Read Data	24 bits	Normal only(1)
00	Write Data	24 bits	Both
01	Reserved	—	—
10	Reserved	—	—

Note 1: Reading from the NV memory locations will return the shadow RAM value of the NV memory, not the NV memory contents. Once a write cycle starts, no other commands accessing NV memory locations are allowed.

4.6.1 COMMAND BYTE

The command byte has three fields, the Address (5 bits), the Command (2 bits) and one Reserved bit (see Figure 4-13).

The device memory is accessed when the host sends a proper command byte to select the desired operation. The memory location getting accessed is contained in the command byte's AD4:AD0 bits. The action desired is contained in the command byte's C1:C0 bits (see Figure 4-17). C1:C0 determines if the desired memory location will be read or written.

As the Command Byte is loaded into the device (on the SDI pin), the device's SDO pin drives. The SDO pin will output high bits for the first seven bits of that command. On the eighth bit, the SDO pin will output the CMDERR bit state.

4.6.2 DATA BYTES

The read and write commands use data bytes (see Figure 4-13). The D15:D12 bits are reserved, their value being ignored. Bits D11:D0 represent the data to be read or written, depending on the command and device resolution.

4.6.3 CONTINUOUS COMMANDS

The device supports the ability to execute commands continuously. While the $\overline{CS}$ pin is in Active state (V_{IL}), any sequence of valid commands may be received.

The following example is a valid sequence of events:

1. $\overline{CS}$ pin driven active (V_{IL})
2. Read command
3. Write command (volatile memory)
4. Write command (nonvolatile memory)
5. $\overline{CS}$ pin driven inactive (V_{IH})

Note 1: While the $\overline{CS}$ pin is active, only one type of command must be issued. When changing commands, it is recommended to take the $\overline{CS}$ pin inactive, then force it back to the Active state.

2: Long command strings must be broken down into shorter command strings. This reduces the probability of noise on the SCK pin corrupting the desired SPI command string.

4.6.4 ERROR CONDITION

The CMDERR bit indicates if the five address bits received (AD4:AD0) and the two command bits received (C1:C0) are a valid combination. The CMDERR bit is high if the combination is valid and low if the combination is invalid.

The command error bit will also be low if a write to a nonvolatile address is specified and another SPI command occurs before the $\overline{CS}$ pin is driven inactive (V_{IH}).

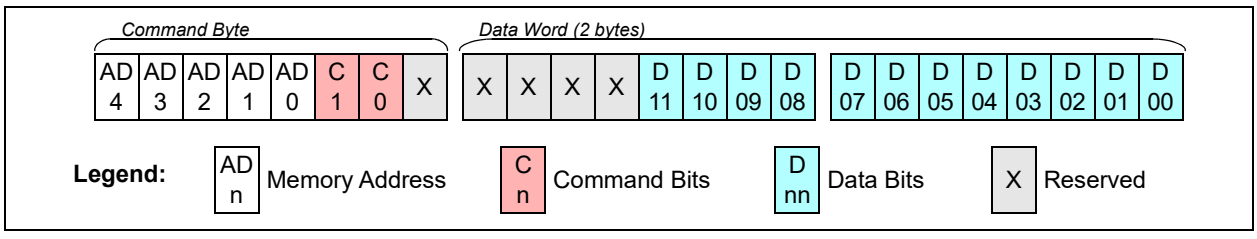

FIGURE 4-13: *24-Bit SPI Command Format.*

SPI commands that do not have a multiple of 24 clocks are ignored.

Once an error condition occurs, any following commands are ignored. All following SDO bits will be low until the CMDERR condition is cleared by forcing the $\overline{CS}$ pin to the Inactive state (V_{IH}) or doing a POR.

4.6.5 ABORTING A TRANSMISSION

All SPI transmissions must have the correct number of SCK pulses to be executed. The command is not executed until the complete number of clocks is received. Some commands also require the $\overline{CS}$ pin to be forced inactive (V_{IH}). If the $\overline{CS}$ pin is forced to the Inactive state (V_{IH}), the serial interface is reset. Partial commands are not executed.

SPI is more susceptible to noise than other bus protocols. The most likely case is that this noise corrupts the value of the data being clocked into the MCP48CXBX4/8 or the SCK pin is injected with extra clock pulses. This may cause data to be corrupted in the device or a command error to occur, since the address and command bits were not a valid combination. The extra SCK pulse will also cause the SPI data (SDI) and clock (SCK) to be out of sync. Forcing the $\overline{CS}$ pin to the Inactive state (V_{IH}) resets the serial interface. The SPI interface will ignore activity on the SDI and SCK pins until the $\overline{CS}$ pin transition to the Active state is detected (V_{IH} to V_{IL}).

Note 1: When the MCP48CXBX4/8 does not receive data, it is recommended that the $\overline{CS}$ pin be forced to the inactive level (V_{IL}).

4.6.6 WRITE COMMAND

The write command is a 24-bit command. The write command can be issued to both the volatile and nonvolatile memory locations. The format of the command is shown in Figure 4-14.

A write command to a volatile memory location changes that location after a properly formatted write command (24-clock) is received.

A write command to a nonvolatile memory location will only start a write cycle after a properly formatted write command (24-clock) is received and the $\overline{CS}$ pin transitions to the Inactive state (V_{IH}).

Note: Writes to volatile memory locations depend on the state of the WiperLock™ Technology bits.

4.6.6.1 Single Write to Volatile Memory

The write operation requires that the $\overline{CS}$ pin be in the Active state (V_{IL}). Typically, the $\overline{CS}$ pin is in the Inactive state (V_{IH}) and is driven to the Active state (V_{IL}). The 24-bit write command (command byte and data bytes) is then clocked in on the SCK and SDI pins. Once all 24 bits are received, the specified volatile address is updated. A write will not occur if the write command is not exactly 24 clocks pulses. This protects against system issues from corrupting the nonvolatile memory locations.

Figure 4-14 shows the waveform for a single write.

4.6.6.2 Single Write to Nonvolatile Memory

The sequence to write to a single nonvolatile memory location is the same as a single write to volatile memory with the exception that before the command, the HVC pin must be driven to V_{IHH}. After the command, the $\overline{CS}$ pin is driven inactive (V_{IH}), which then starts the MTP write cycle (t_{WC}). The HVC pin must remain at the V_{IHH} level until the completion of the MTP write cycle.

A write cycle will not start if the write command is not exactly 24 clocks pulses. This protects against system issues from corrupting the nonvolatile memory locations.

After the $\overline{CS}$ pin is driven inactive (V_{IH}), the serial interface may immediately be re-enabled by driving the $\overline{CS}$ pin to the Active state (V_{IL}).

During an MTP write cycle, only serial commands to volatile memory are accepted. All other serial commands are ignored until the MTP write cycle (t_{WC}) is completed. The MTPMA bit in the Status register indicates the status of an MTP write cycle.

Once a write command to a nonvolatile memory location is received, NO other SPI commands must be received before the $\overline{CS}$ pin transitions to the Inactive state (V_{IH}) or a Command Error (CMDERR) on the current SPI command occurs.

The write to a Nonvolatile Memory command has the same format as the write to a Volatile Memory command (see Figure 4-14).

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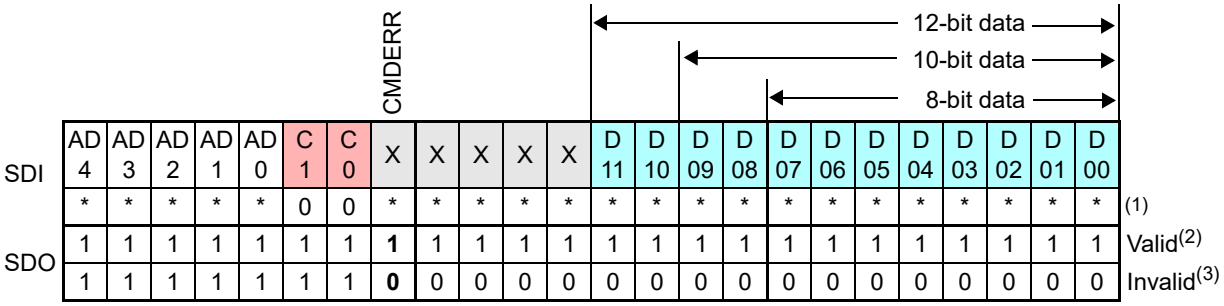


Note 1: For write commands addressing the DAC Wiper registers, the Data bits depend on the resolution of the device: 12-bit = D11:D00, 10-bit = D09:D00 and 8-bit = D07:D00.
Data are right justified for easy Host Controller operation (no data manipulation before transmitting the desired value). The unimplemented bits are ignored.

2: After a valid memory address and a write command byte are received (CMDERR = 1), all the following SDO bits will be output as '1'.

3: If an Error condition occurs (CMDERR = 0), all the following SDO bits will be output as '0' until the CMDERR condition is cleared (the $\overline{CS}$ pin is forced to the Inactive state).

FIGURE 4-14: *Write Single Memory Location Command – SDI and SDO States.*

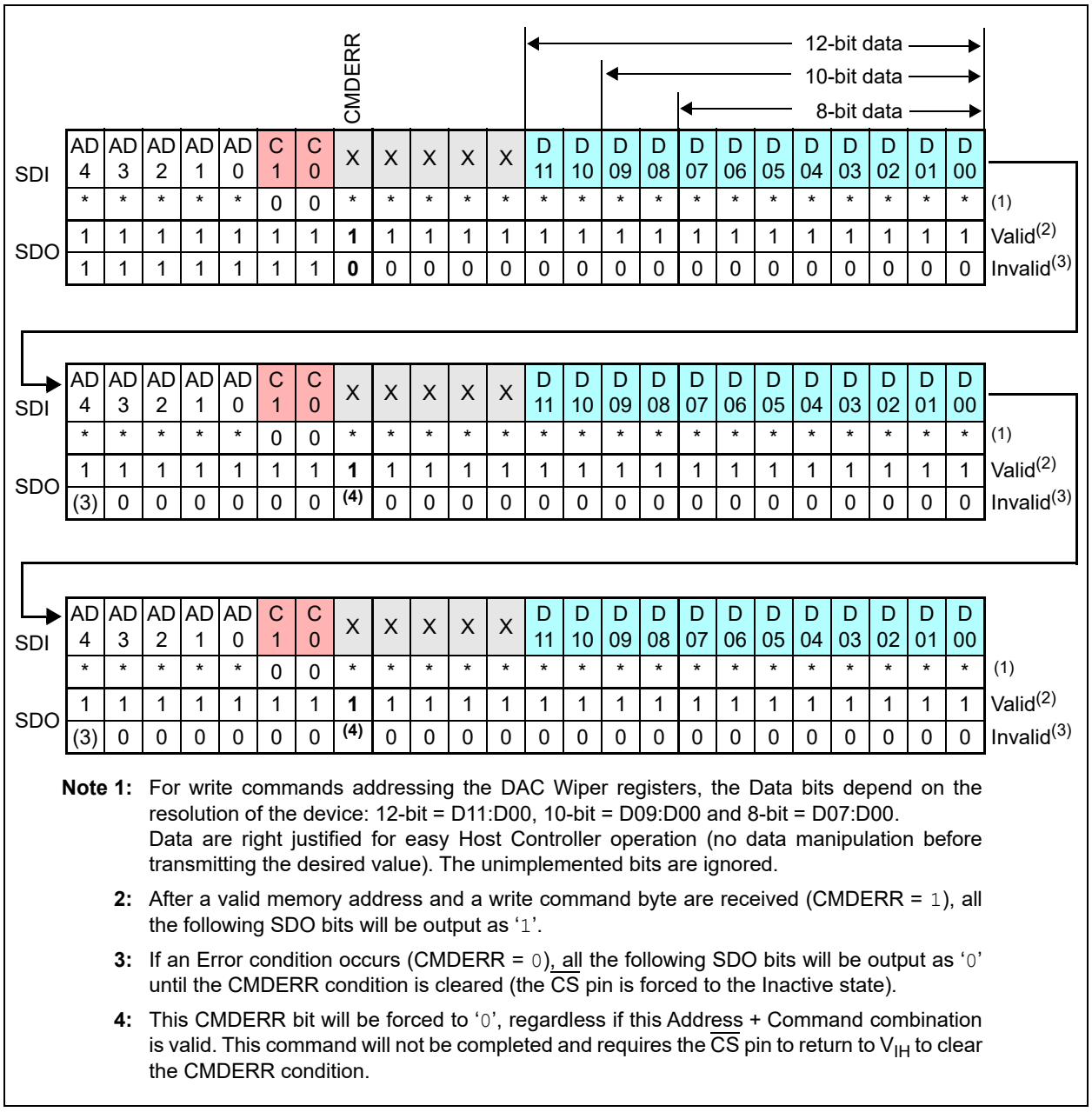
4.6.6.3 Continuous Writes to Volatile Memory

Continuous writes are possible only when writing to the volatile memory registers.

Figure 4-15 shows the sequence for three continuous writes. The writes do not need to be to the same volatile memory address.

4.6.6.4 Continuous Writes to Nonvolatile Memory

Continuous writes to nonvolatile memory are not allowed and attempts to do so will result in a CMDERR condition.



Note 1: For write commands addressing the DAC Wiper registers, the Data bits depend on the resolution of the device: 12-bit = D11:D00, 10-bit = D09:D00 and 8-bit = D07:D00. Data are right justified for easy Host Controller operation (no data manipulation before transmitting the desired value). The unimplemented bits are ignored.

2: After a valid memory address and a write command byte are received (CMDERR = 1), all the following SDO bits will be output as '1'.

3: If an Error condition occurs (CMDERR = 0), all the following SDO bits will be output as '0' until the CMDERR condition is cleared (the $\overline{CS}$ pin is forced to the Inactive state).

4: This CMDERR bit will be forced to '0', regardless if this Address + Command combination is valid. This command will not be completed and requires the $\overline{CS}$ pin to return to V_{IH} to clear the CMDERR condition.

FIGURE 4-15: *Continuous Write Sequence (Volatile Memory Only).*

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4.6.7 READ COMMAND

The read command is a 24-bit command. The read command can be issued to both the volatile and nonvolatile memory locations. The format of the command is shown in Figure 4-16.

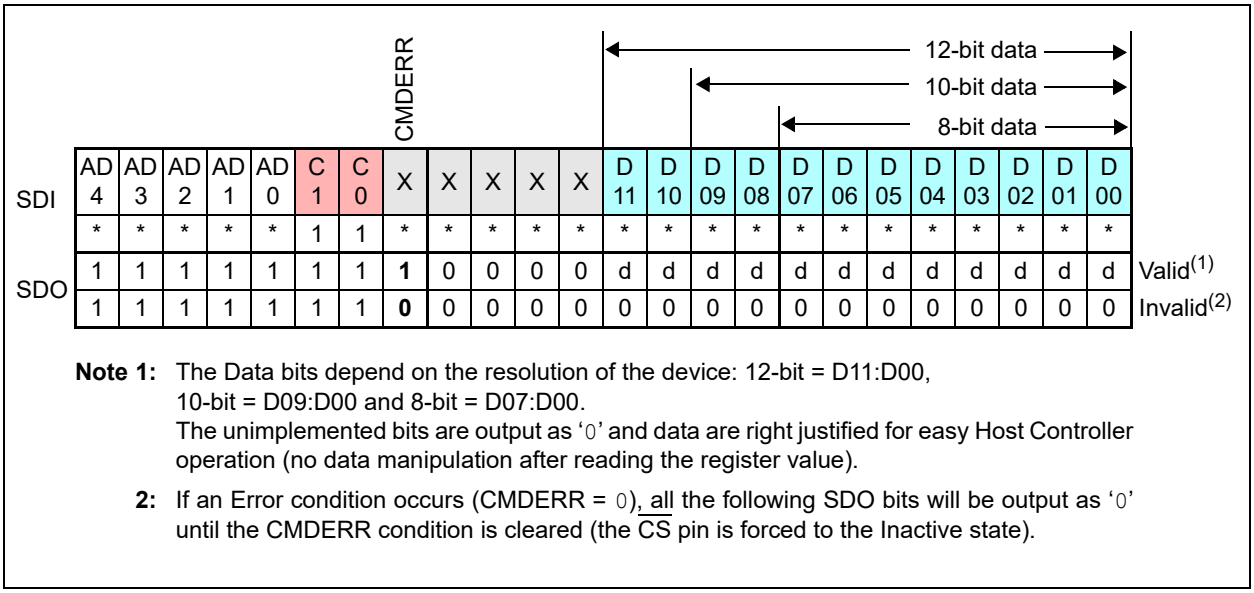
The first seven bits of the read command determine the address and the command. The eighth clock will output the CMDERR bit on the SDO pin. For the remaining 16 clocks, the device will transmit the data bits of the specified address (AD4:AD0).

Figure 4-16 shows the SDI and SDO information for a read command.

During an MTP write cycle, the read command can only be issued to the volatile memory locations. By reading the Status register, the Host Controller can determine when the write cycle is completed (via the state of the MTPMA bit).

4.6.7.1 Single Read

The read operation requires that the $\overline{CS}$ pin be in the Active state (V_{IL}). Typically, the $\overline{CS}$ pin will be in the Inactive state (V_{IH}) and is driven to the Active state (V_{IL}). The 24-bit read command (command byte and data word) is then clocked in on the SCK and SDI pins. The SDO pin starts driving high (V_{IH}) when the $\overline{CS}$ goes active and starts driving data on the eighth bit (CMDERR bit); the addressed data come out on the 9th through 24th clocks.



Note 1: The Data bits depend on the resolution of the device: 12-bit = D11:D00, 10-bit = D09:D00 and 8-bit = D07:D00.
The unimplemented bits are output as '0' and data are right justified for easy Host Controller operation (no data manipulation after reading the register value).

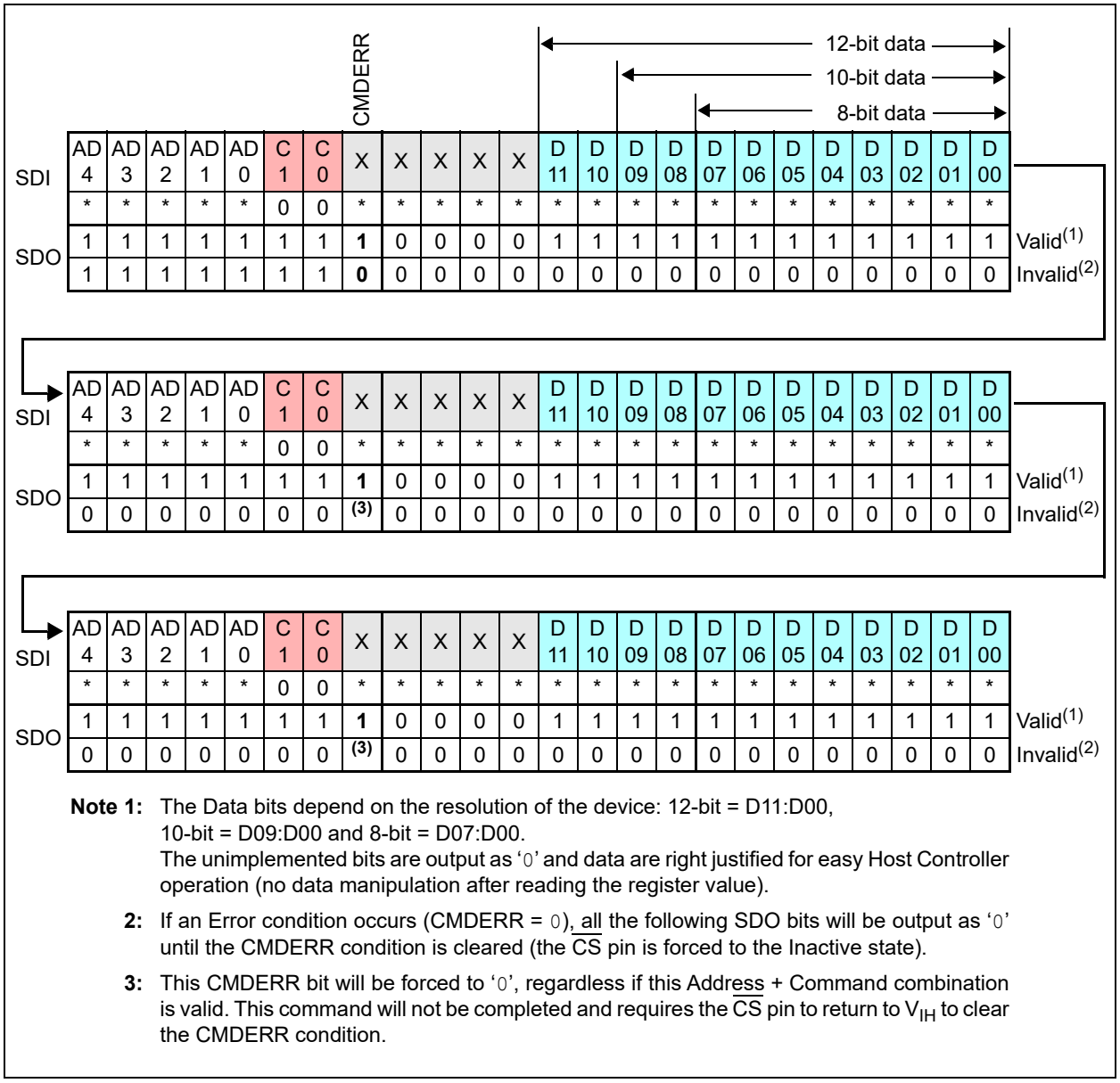
2: If an Error condition occurs (CMDERR = 0), all the following SDO bits will be output as '0' until the CMDERR condition is cleared (the $\overline{CS}$ pin is forced to the Inactive state).

FIGURE 4-16: *Read Single Memory Location Command – SDI and SDO States.*

4.6.7.2 Continuous Reads

Continuous reads allow the device's memory to be read quickly. Continuous reads are possible to all memory locations. Read commands may only access volatile memory locations during an MTP write cycle.

Figure 4-17 shows the sequence for three continuous reads. The reads do not need to be to the same memory address.



Note 1: The Data bits depend on the resolution of the device: 12-bit = D11:D00, 10-bit = D09:D00 and 8-bit = D07:D00.
The unimplemented bits are output as '0' and data are right justified for easy Host Controller operation (no data manipulation after reading the register value).

2: If an Error condition occurs (CMDERR = 0), all the following SDO bits will be output as '0' until the CMDERR condition is cleared (the $\overline{CS}$ pin is forced to the Inactive state).

3: This CMDERR bit will be forced to '0', regardless if this Address + Command combination is valid. This command will not be completed and requires the $\overline{CS}$ pin to return to V_{IH} to clear the CMDERR condition.

FIGURE 4-17: *Continuous Read Sequence.*

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5.0 APPLICATIONS INFORMATION

The MCP48CXBX4/8 devices are general purpose, quad/octal-channel voltage output DACs for various applications where a precision operation with low power and nonvolatile memory is needed.

Since the devices include an MTP memory, they can be utilized in applications that require the output to return to the previous setup value on subsequent power-ups. The 32-times programmable MTP memory offers the possibility of factory or field calibration of the DAC, in the application circuit. The configurable SPI address, combined with the dedicated pins, offers the possibility of having more than one DAC on the same bus, while increasing the interconnection compatibility with other device types, which do not have a user-programmable address.

Applications generally suited for the devices are:

- Digitally Controlled Power Supplies
- Set Point or Offset Trimming
- Sensor Calibration
- Portable Instrumentation (Battery-Powered)
- Motor Control

5.1 SPI Bus Connection Considerations

5.1.1 OUTPUT UPDATE RATE

The supported commands and their associate clock cycles are shown in Table 5-1. The table also indicates the theoretical maximum update rate for different SPI bus speeds.

Note: The output update rate also depends on the slew rate and output load. The values in the table are calculated neglecting other influencing factors and must be used for orientation only.

TABLE 5-1: SPI COMMANDS – NUMBER OF CLOCKS

Command					# of Bit Clocks(2)	Data Update Rate (8-bit/10-bit/12-bit) (Data Words/Second)			Comments
Operation	Code			Mode(1)		1 MHz	10 MHz	50 MHz	
	C1	C0	HV (4, 7)						
Write Command(3, 6)	0	0	Y	Single	24	41,666	416,666	2,083,333	
	0	0	N	Continuous	24 * n	41,666	416,666	2,083,333	For 10 data words
Read Command(5)	1	1	N	Random	24	41,666	416,666	2,083,333	
	1	1	N	Continuous	24 * n	41,666	416,666	2,083,333	For 10 data words

Note 1: Nonvolatile registers can only use the Single mode.

2: "n" indicates the number of times the command operation is to be repeated.

3: The registers are updated after the 24th clock bit or after the $\overline{CS}$ rising, depending on mode.

4: If the state of the HVC pin is V_{IHH}, the command is ignored, but a CMDERR condition will NOT be generated.

5: This command is useful to determine when an MTP programming cycle is completed.

6: This command can be either normal voltage or high voltage.

7: The MTP write cycle starts after the $\overline{CS}$ rising edge. A High-Voltage command requires the HVC pin to be at V_{IHH} for the entire command, until the completion of the MTP write cycle.

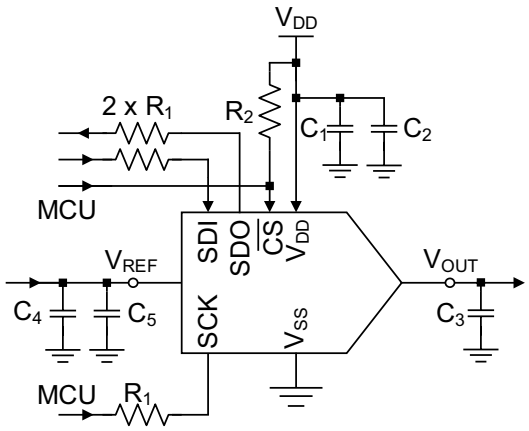
5.2 Power Supply Considerations

The power source must be as clean as possible. Any noise induced on the V_{DD} line can affect the DAC performance.

Typical applications will require a bypass capacitor in order to filter out high-frequency noise on the V_{DD} line. The noise can be induced onto the power supply's traces or as a result of changes on the DAC output. The bypass capacitor helps to minimize the effect of these noise sources on signal integrity.

If the internal V_{DD} is selected as the resistor ladder's reference voltage (VRnB:VRnA = 00), the power supply to the device is also used for the DAC voltage reference internally.

Figure 5-1 shows an example of using bypass capacitors to improve performance. The capacitors must be chosen according to the intended application and other external components used in the circuit.



Comp.	Value	Comments
R_1	33Ω	SPI bus isolation resistors (optional)
R_2	10 kΩ	$\overline{CS}$ pull-up resistor (optional)
C_1	0.1 µF	Ceramic
C_2	10 µF	Tantalum or ceramic
C_3	0.1 µF	Optional to reduce transition noise on the output (ceramic)
C_4	0.1 µF	Ceramic
C_5	10 µF	Optional: tantalum or ceramic

FIGURE 5-1: *Circuit Example.*

A ceramic 0.1 µF capacitor must be placed as close to the V_{DD} pin as possible (within 4 mm). If the power supply lacks proper stabilization, another higher value capacitor, tantalum or ceramic, can be added on the application board to reduce supply variations that could have an influence on the output.

When the DAC is in External Reference mode (VRnB:VRnA = 11 or 10), if using a dedicated voltage reference chip, the capacitors must be chosen according to the external reference specifications. If the reference voltage is derived from a source with significant noise, a similar decoupling scheme as for V_{DD} can be used.

For Internal Band Gap mode (VRnB:VRnA = 01), the V_{REF} pin must be left floating and surrounded with a ground guard structure to attenuate parasitic noise. A small capacitor can be used to further reduce the possibility of external noise pick-up.

If the application circuit has separate digital and analog power supplies, the V_{DD} and V_{SS} pins of the device must reside on the analog plane.

5.3 Output Circuit Design Considerations

The MCP48CXBX4/8 devices have a buffered output. This means that no filtering is required on the V_{OUT} pin in most cases. There are some applications where a slower rise time or protection against glitches is required, for example in power supplies. In those particular cases, an extra capacitor can be added on the output, that will smooth out any transition noise that may happen during operation.

Refer to the Output Amplifier section in the **DC Characteristics** table for details about the internal precision operational amplifier used on the output.

5.3.1 DRIVING RESISTIVE AND CAPACITIVE LOADS

The V_{OUT} pin can drive up to 100 pF of capacitive load in parallel with a 5 kΩ resistive load (to meet electrical specifications). V_{OUT} drops slowly as the load resistance decreases after about 3.5 kΩ. It is recommended to use a load with R_L greater than 2 kΩ.

Driving large capacitive loads can cause stability problems for voltage feedback output amplifiers. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response with overshoot and ringing in the step response. That is, since the V_{OUT} pin's voltage does not quickly follow the buffer's input voltage (due to the large capacitive load), the output buffer will overshoot the desired target voltage. Once the driver detects this overshoot, it compensates by forcing it to a voltage below the target. This causes voltage ringing on the V_{OUT} pin.

So, when driving large capacitive loads with the output buffer, a small series resistor (R_{ISO}) at the output (see Figure 5-2) improves the output buffer's stability (feedback loop's phase margin) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.

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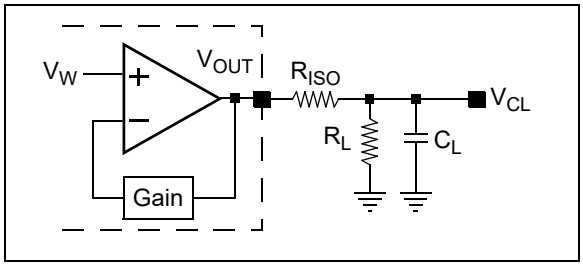

FIGURE 5-2: *Circuit to Stabilize the Output Buffer for Large Capacitive Loads (C_L).*

The R_{ISO} resistor value for the circuit needs to be selected. The resulting frequency response peaking and step response overshoot for this R_{ISO} resistor value must be verified on the bench. Modify the R_{ISO}'s resistance value until the output characteristics meet your requirements.

A method to evaluate the system's performance is to inject a step voltage on the V_{REF} pin and observe the V_{OUT} pin's characteristics.

Note:	Additional insight into circuit design for driving capacitive loads can be found in *AN884, "Driving Capacitive Loads With Op Amps"* (DS00884).

5.4 Layout Considerations

Several layout considerations may be applicable to your application. These may include:

- **Noise**
- **PCB Area Requirements**

5.4.1 NOISE

Particularly harsh environments may require shielding of critical signals. Inductively-coupled AC transients and digital switching noise can degrade the input and output signal integrity, potentially masking the MCP48CXBX4/8's performance. Careful board layout minimizes these effects and increases the Signal-to-Noise Ratio (SNR).

Multilayer boards utilizing a low-inductance ground plane, isolated inputs, isolated outputs and proper decoupling are critical to achieving the performance that the silicon is capable of providing.

Separate digital and analog ground planes are recommended. In this case, the V_{SS} pin and the ground pins of the V_{DD} capacitors must be terminated to the analog ground plane.

Note:	Breadboards and wire-wrapped boards are not recommended.

5.4.2 PCB AREA REQUIREMENTS

In some applications, the PCB area is a criteria for device selection. Table 5-2 shows the typical package dimensions and area for the different package options.

TABLE 5-2: PACKAGE FOOTPRINT(1)

Package			Package Footprint		
Pins	Type	Code	Dimensions (mm)		Area (mm^2)
			Length	Width	
20	TSSOP	ST	6.50	6.40	41.60
20	QFN	ML	4.00	4.00	16.00

Note 1: Does not include recommended land pattern dimensions. Dimensions are typical values.

NOTES:

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6.0 DEVELOPMENT SUPPORT

Development support can be classified into two groups:

- **Development Tools**
- **Technical Documentation**

6.1 Development Tools

Several development tools are available to assist in your design and evaluation of the MCP48CXBX4/8 devices. The currently available tools are shown in Table 6-1.

Figure 6-1 shows how the TSSOP20EV bond-out PCB can be populated to easily evaluate the MCP48CXBX4/8 devices. Device evaluation can use the PICkit™ Serial Analyzer to control the DAC output registers and state of the Configuration, Control and Status registers.

The TSSOP20EV boards may be purchased directly from the Microchip website at www.microchip.com.

6.2 Technical Documentation

Several additional technical documents are available to assist you in your design and development. These technical documents include Application Notes, Technical Briefs and Design Guides. Table 6-2 shows some of these documents.

TABLE 6-1: DEVELOPMENT TOOLS (Note 1)

Board Name	Part #	Comment
20-Pin TSSOP and SSOP Evaluation Board	TSSOP20EV	Most flexible option – recommended bond-out PCB

Note 1: Supports the PICkit™ Serial Analyzer. See the User's Guide for additional information and requirements.

TABLE 6-2: TECHNICAL DOCUMENTATION

Application Note Number	Title	Literature #
AN1326	Using the MCP4728 12-Bit DAC for LDMOS Amplifier Bias Control Applications	DS01326
—	Signal Chain Design Guide	DS21825
—	Analog Solutions for Automotive Applications Design Guide	DS01005

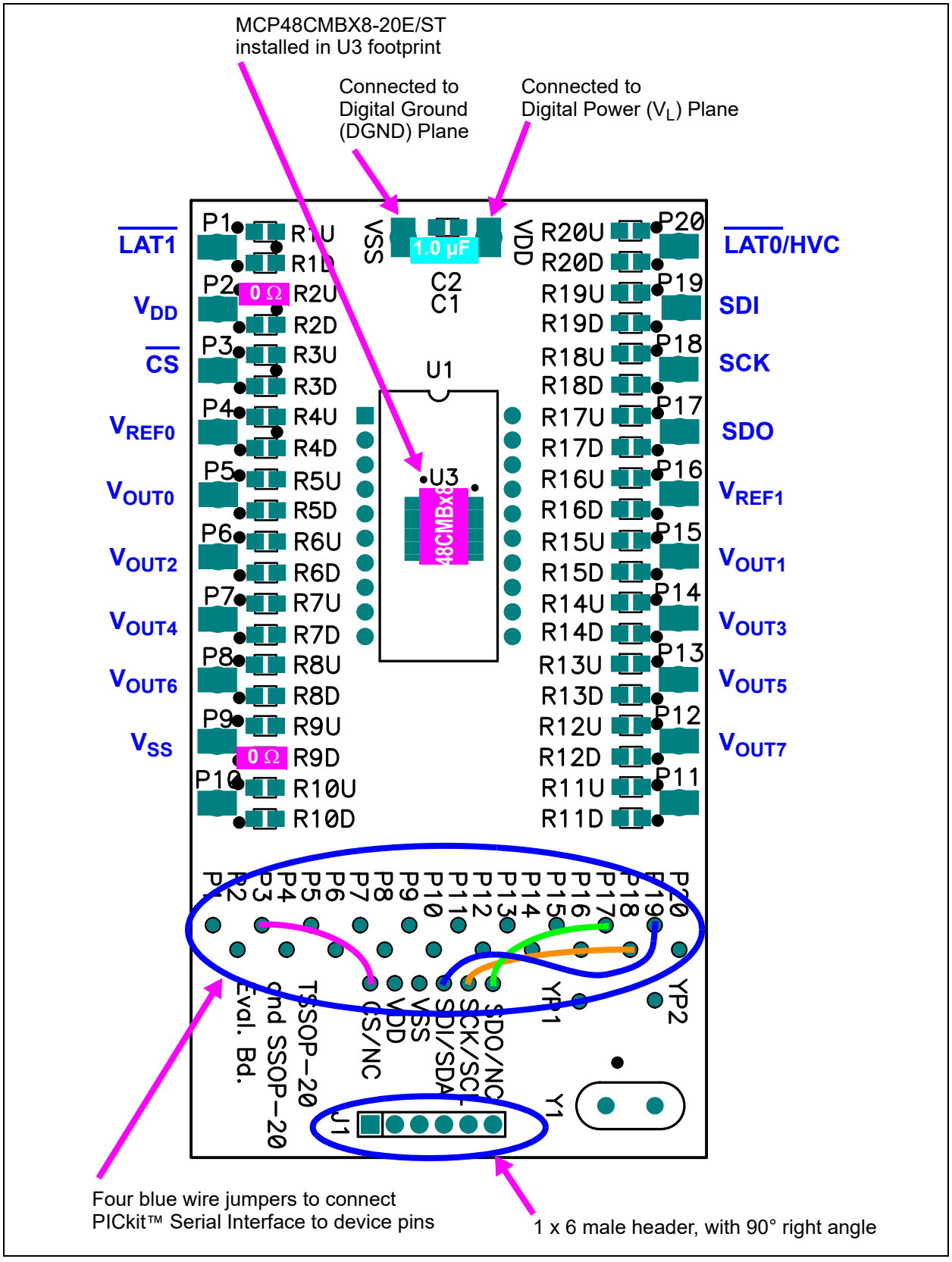

FIGURE 6-1: *MCP48CXBX4/8 Evaluation Board Circuit Using TSSOP20EV.*

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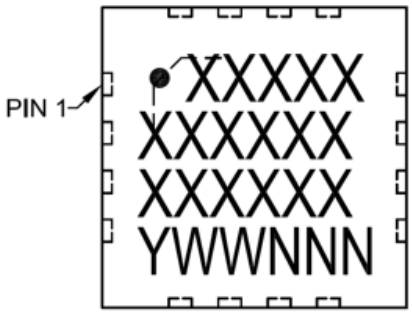
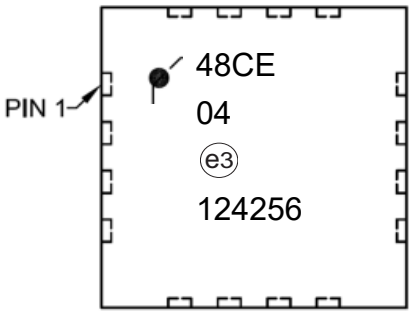
7.0 PACKAGING INFORMATION

7.1 Package Marking Information

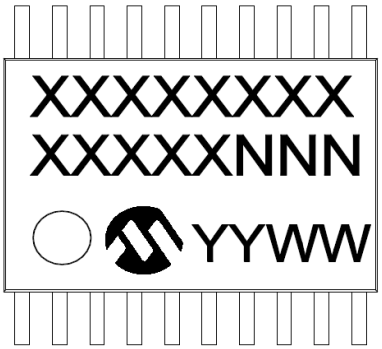
20-Lead 4 mm x 4 mm QFN



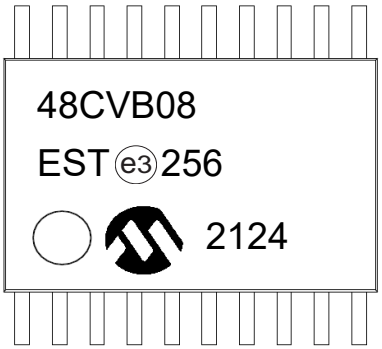
Example



20-Lead TSSOP



Example

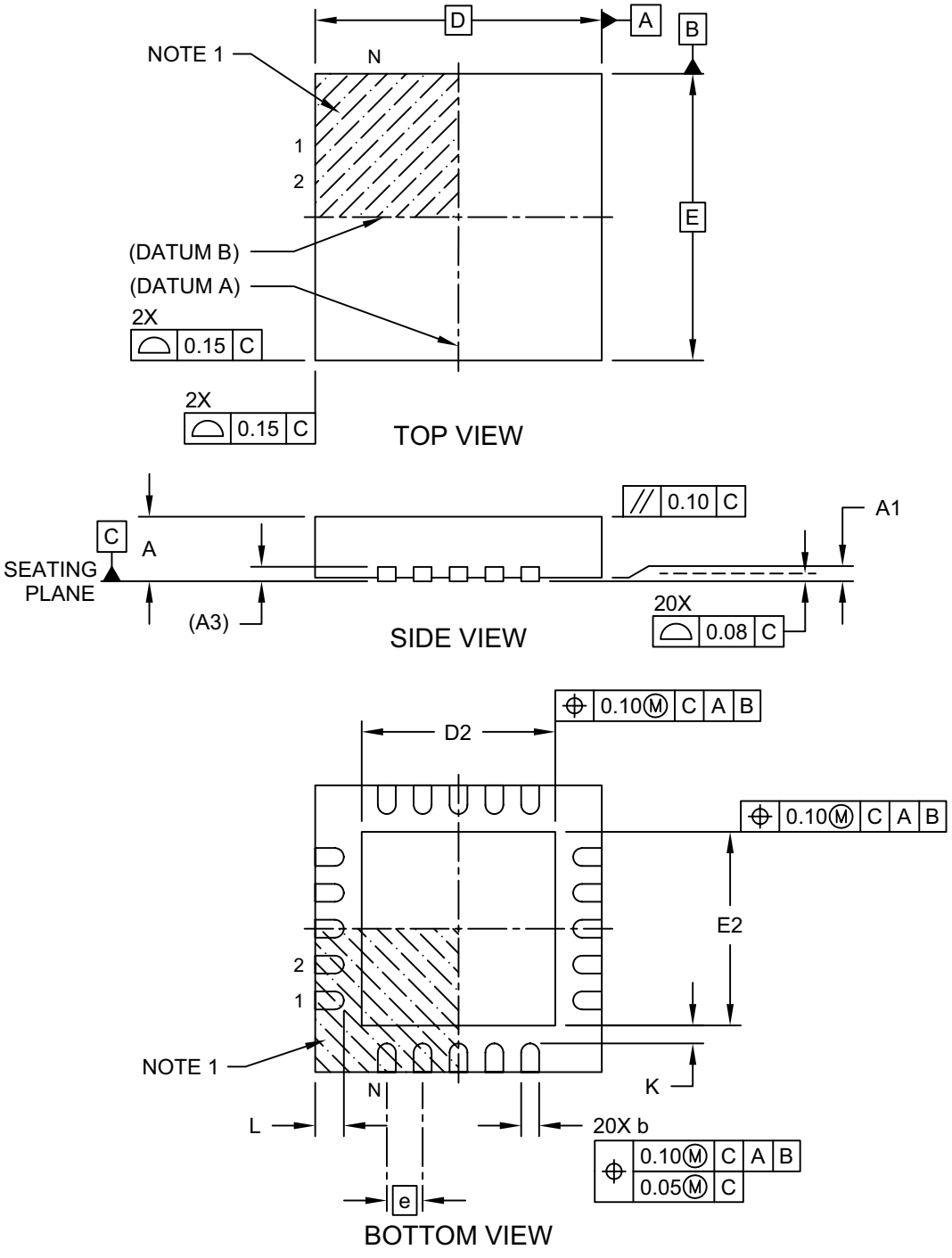


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

20-Lead Plastic Quad Flat, No Lead Package (ML) - 4x4 mm Body [QFN]
Also called VQFN

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-126 Rev C Sheet 1 of 2

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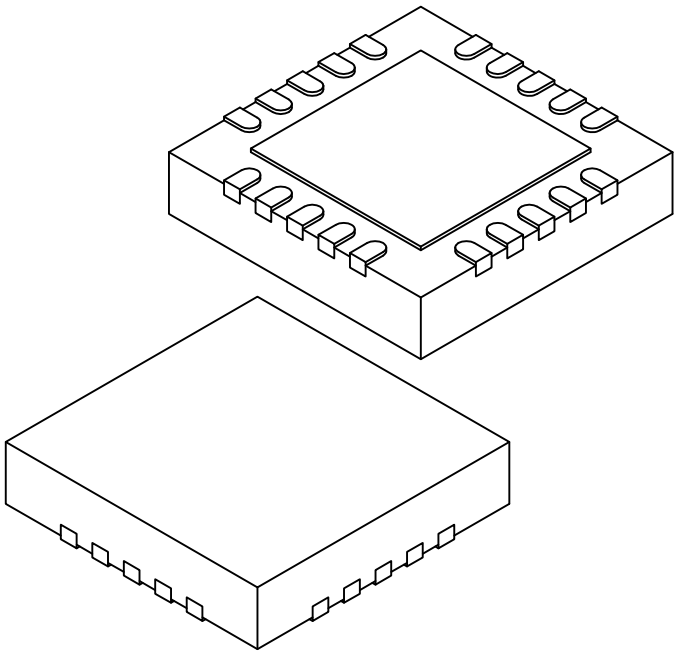
20-Lead Plastic Quad Flat, No Lead Package (ML) - 4x4 mm Body [QFN]
Also called VQFN

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		20	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.60	2.70	2.80
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.60	2.70	2.80
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

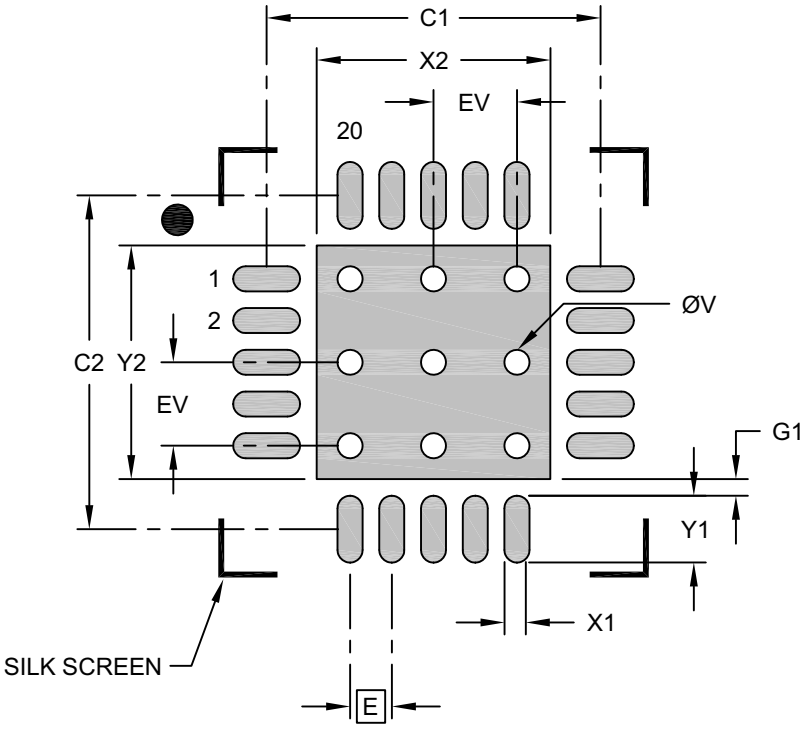
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-126 Rev C Sheet 2 of 2

20-Lead Plastic Quad Flat, No Lead Package (ML) - 4x4 mm Body [QFN]
Also called VQFN

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			2.80
Optional Center Pad Length	Y2			2.80
Contact Pad Spacing	C1		4.00	
Contact Pad Spacing	C2		4.00	
Contact Pad Width (X20)	X1			0.30
Contact Pad Length (X20)	Y1			0.80
Contact Pad to Center Pad (X16)	G1	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2126 Rev B

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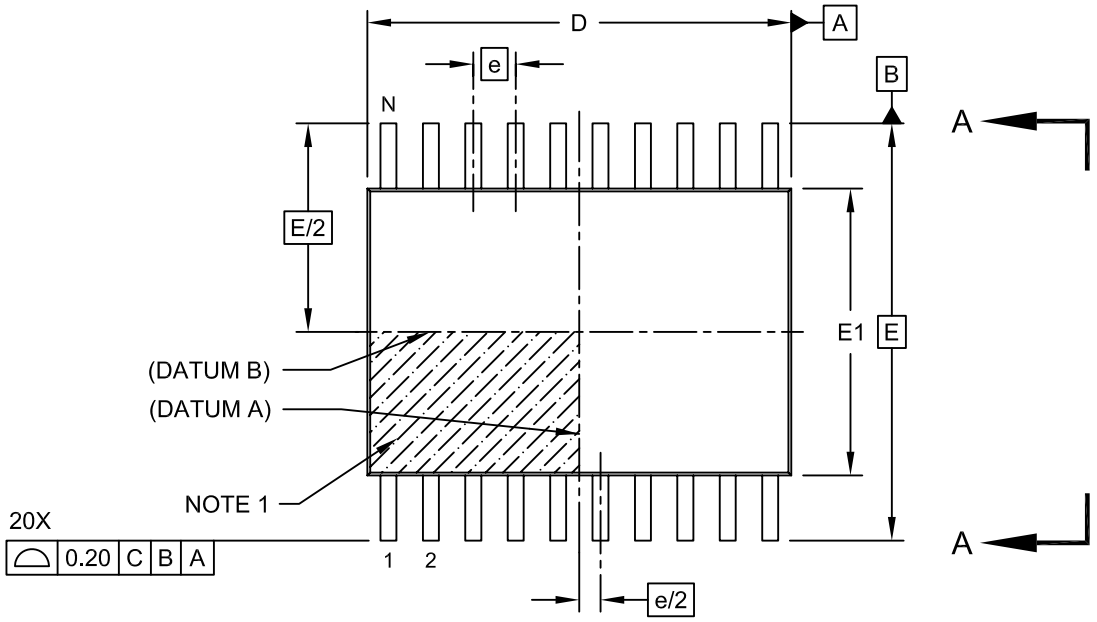
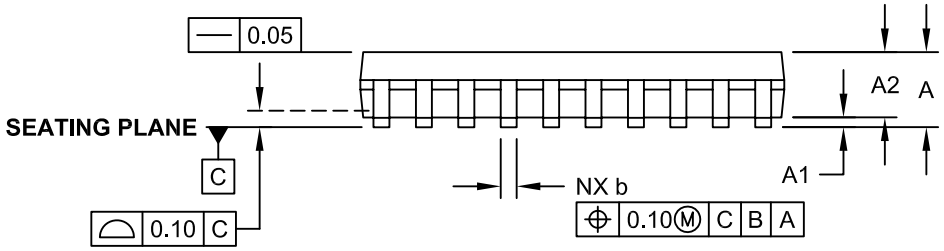
20-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

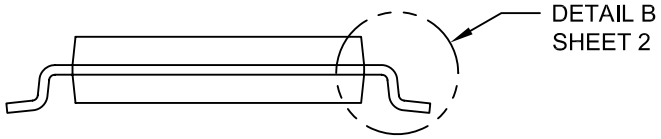
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

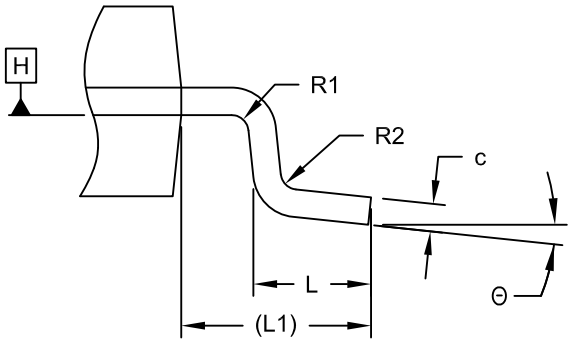


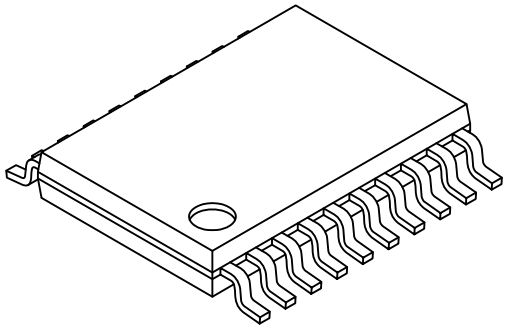
VIEW A—A

Microchip Technology Drawing C04-088C Sheet 1 of 2

20-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





DETAIL B

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	-	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	6.40	6.50	6.60
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	Θ	0°	-	8°
Lead Width	b	0.19	-	0.30
Lead Thickness	c	0.09	-	0.20
Bend Radius	R1	0.09	-	-
Bend Radius	R2	0.09	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-088C Sheet 2 of 2

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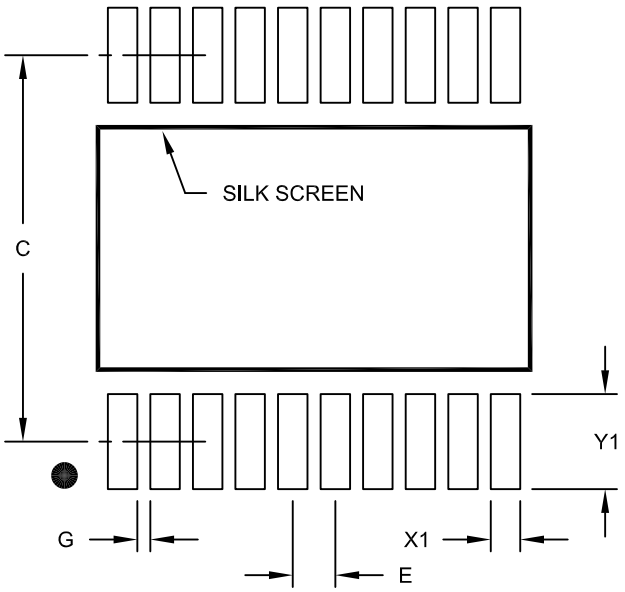
20-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		5.90	
Contact Pad Width (X20)	X1			0.45
Contact Pad Length (X20)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2088A

NOTES:

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APPENDIX A: REVISION HISTORY

Revision B (July 2021)

The following is the list of modifications:

- Updated the TSSOP package drawing in **Section 7.1, "Package Marking Information"**.

Revision A (June 2021)

- Original release of this document.

Note: The SPI standard uses the terminology "Master" and "Slave". The equivalent Microchip terminology used in this document is "Host" and "Client", respectively.

NOTES:

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APPENDIX B: TERMINOLOGY

B.1 Resolution

The resolution is the number of DAC output states that divide the Full-Scale Range (FSR). For the 12-bit DAC, the resolution is 2^{12}, meaning the DAC code ranges from 0 to 4095.

When there are 2^N resistors in the resistor ladder and 2^N tap points, the full-scale DAC register code is the resistor element positioned at 1 LSb from the source reference voltage (V_{DD} or V_{REF}).

B.2 Least Significant Bit (LSb)

This is the voltage difference between two successive codes. For a given output voltage range, it is divided by the resolution of the device (Equation B-1).

EQUATION B-1: LSb VOLTAGE CALCULATION

Ideal

$$V_{LSb(IDEAL)} = \frac{V_{DD}}{2^N} \text{ or } \frac{V_{REF}}{2^N}$$

Measured 1

$$V_{LSb(Measured)} = \frac{V_{OUT(@4032)} - V_{OUT(@64)}}{(4032 - 64)}$$

Measured 2

$$V_{LSb} = \frac{V_{OUT(@FS)} - V_{OUT(@ZS)}}{2^N - 1}$$

2^N = 4096 (MCP48CVB2X)
= 1024 (MCP48CVB1X)
= 256 (MCP48CVB0X)

The range may be V_{DD} (or V_{REF}) to V_{SS} (ideal); the DAC register codes across the linear range of the output driver (Measured 1) or full scale to zero scale (Measured 2).

B.3 Monotonic Operation

The monotonic operation means that the device's output voltage (V_{OUT}) increases with every one code step (LSb) increment (from V_{SS} to the DAC's reference voltage, V_{DD} or V_{REF}).

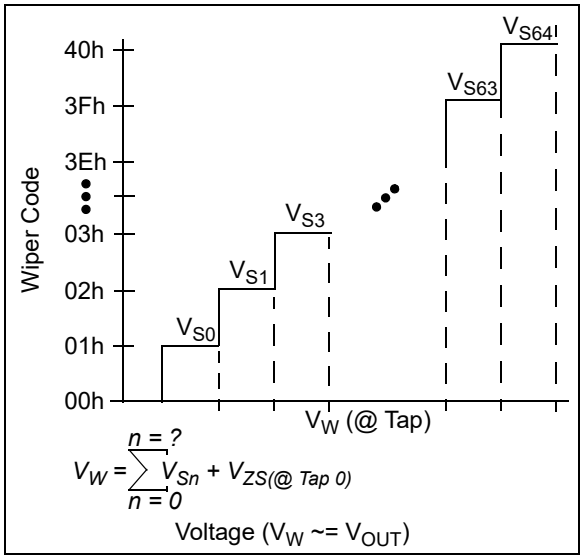

FIGURE B-1: *V_W (V_{OUT}).*

B.4 Zero-Scale Error (E_{ZS})

The zero-scale error, E_{ZS} (see Figure B-2), is the difference between the ideal and the measured V_{OUT} voltage with the DAC register code equal to 000h (Equation B.5).

EQUATION B-2: ZERO-SCALE ERROR

$$E_{ZS} = \frac{V_{OUT(@ZS)}}{V_{LSb(IDEAL)}}$$

Where:

E_{ZS} = expressed in LSb
$V_{OUT(@ZS)}$ = V_{OUT} voltage when the DAC register code is at zero scale
$V_{LSb(IDEAL)}$ = theoretical voltage step-size

The error depends on the resistive load on the V_{OUT} pin (and where that load is tied to, such as V_{SS} or V_{DD}). For loads (to V_{DD}) greater than specified, the zero-scale error is greater.

The error in bits is determined by the theoretical voltage step-size to give an error in LSb.

B.5 Full-Scale Error (E_{FS})

The full-scale error, E_{FS} (see Figure B-3), is the error on the V_{OUT} pin relative to the expected V_{OUT} voltage (theoretical) for the maximum device DAC register code (FFFh for 12-bit, 3FFh for 10-bit and FFh for 8-bit); see Equation B-3. The error depends on the resistive load on the V_{OUT} pin (and where that load is tied to, such as V_{SS} or V_{DD}). For loads (to V_{SS}) greater than specified, the full-scale error will be greater.

The error in bits is determined by the theoretical voltage step-size to give an error in LSb.

EQUATION B-3: FULL-SCALE ERROR

$$E_{FS} = \frac{V_{OUT(@FS)} - V_{IDEAL(@FS)}}{V_{LSb(IDEAL)}}$$

Where:

E_{FS} = expressed in LSb

$V_{OUT(@FS)}$ = V_{OUT} voltage when the DAC register code is at full scale

$V_{IDEAL(@FS)}$ = ideal output voltage when the DAC register code is at full scale

$V_{LSb(IDEAL)}$ = theoretical voltage step-size

B.6 Offset Error (E_{OS})

The offset error (E_{OS}) is the delta voltage of the V_{OUT} voltage from the ideal output voltage at the specified code. This code is specified where the output amplifier is in the linear operating range; for the MCP48CXBX4/8, we specify code 64 (decimal). Offset error does not include gain error, which is illustrated in Figure B-2.

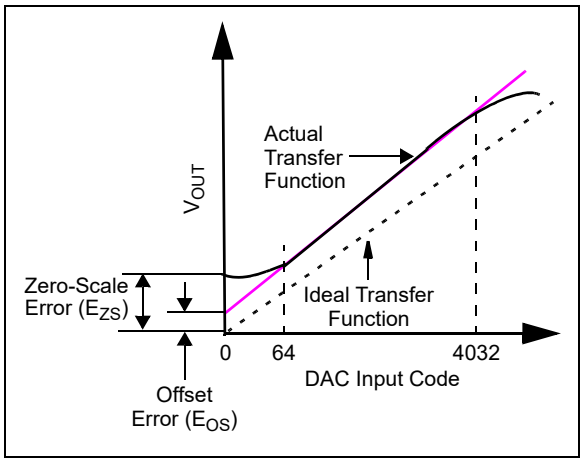

FIGURE B-2: *Offset Error (Zero Gain Error).*

This error is expressed in mV. Offset error can be negative or positive. The error can be calibrated by software in application circuits.

B.7 Offset Error Drift (E_{OSD})

The offset error drift (E_{OSD}) is the variation in offset error due to a change in ambient temperature. The offset error drift is typically expressed in ppm/°C or µV/°C.

B.8 Gain Error (E_G)

Gain error (E_G) is a calculation based on the ideal slope using the voltage boundaries for the linear range of the output driver (e.g., code 64 and code 4032); see Figure B-3. The gain error calculation nullifies the device's offset error.

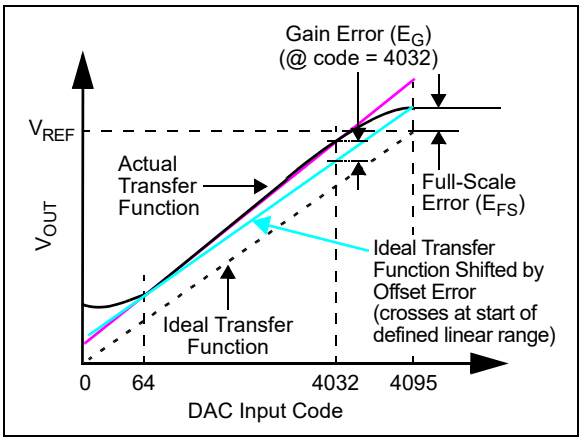

FIGURE B-3: *Gain Error and Full-Scale Error Example.*

The gain error indicates how well the slope of the actual transfer function matches the slope of the ideal transfer function. The gain error is usually expressed as a percentage of FSR or in LSb. FSR is the ideal full-scale voltage of the DAC (see Equation B-4).

EQUATION B-4: GAIN ERROR EXAMPLE

$$E_G = \frac{(V_{OUT(@4032)} - V_{OS} - V_{OUT\_Ideal(@4032)})}{V_{Full\text{-}Scale\ Range}} * 100$$

Where:

E_G is expressed in % of FSR

$V_{OUT(@4032)}$ = measured DAC output voltage at the specified code

$V_{OUT\_Ideal(@4032)}$ = calculated DAC output voltage at the specified code (4032 * $V_{LSb(Ideal)}$)

V_{OS} = measured offset voltage

$V_{Full\text{-}Scale\ Range}$ = expected full-scale output value (such as the V_{REF} voltage)

B.9 Gain Error Drift (E_{GD})

The gain error drift (E_{GD}) is the variation in gain error due to a change in ambient temperature. The gain error drift is typically expressed in ppm/°C (of FSR).

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B.10 Total Unadjusted Error (E_T)

The total unadjusted error (E_T) is the difference between the ideal and the measured V_{OUT} voltage. Typically, calibration of the output voltage is implemented to improve the system's performance.

The error in bits is determined by the theortical voltage step-size to give an error in LSb.

Equation B-5 shows the total unadjusted error calculation.

EQUATION B-5: TOTAL UNADJUSTED ERROR CALCULATION

$$E_T = \frac{(V_{OUT\_Actual(@code)} - V_{OUT\_Ideal(@code)})}{V_{LSb(Ideal)}}$$

Where:

E_T = expressed in LSb

$V_{OUT\_Actual(@code)}$ = measured DAC output voltage at the specified code

$V_{OUT\_Ideal(@code)}$ = calculated DAC output voltage at the specified code (*code* * $V_{LSb(Ideal)}$)

$V_{LSb(Ideal)}$ = V_{REF}/# Steps
12-bit = V_{REF}/4096
10-bit = V_{REF}/1024
8-bit = V_{REF}/256

B.11 Integral Nonlinearity (INL)

The integral nonlinearity error (INL) is the maximum deviation of an actual transfer function, from an ideal transfer function (straight line), passing through the defined end-points of the DAC transfer function (after offset and gain errors are removed).

For the MCP48CXBX4/8, INL is calculated using the defined end-points, DAC code 64 and code 4032. INL can be expressed as a percentage of FSR or in LSb. INL is also called relative accuracy. Equation B-6 shows how to calculate the INL error in LSb and Figure B-4 shows an example of INL accuracy.

Positive INL means a V_{OUT} voltage higher than the ideal one. Negative INL means a V_{OUT} voltage lower than the ideal one.

EQUATION B-6: INL ERROR

$$E_{INL} = \frac{(V_{OUT} - V_{Calc\_Ideal})}{V_{LSb(Measured)}}$$

Where:

INL = expressed in LSb

V_{Calc_Ideal} = Code * $V_{LSb(Measured)}$ + V_{OS}

$V_{OUT(Code = n)}$ = measured DAC output voltage with a given DAC register code

$V_{LSb(Measured)}$ = for measured:
($V_{OUT(4032)}$ – $V_{OUT(64)}$)/3968

V_{OS} = measured offset voltage

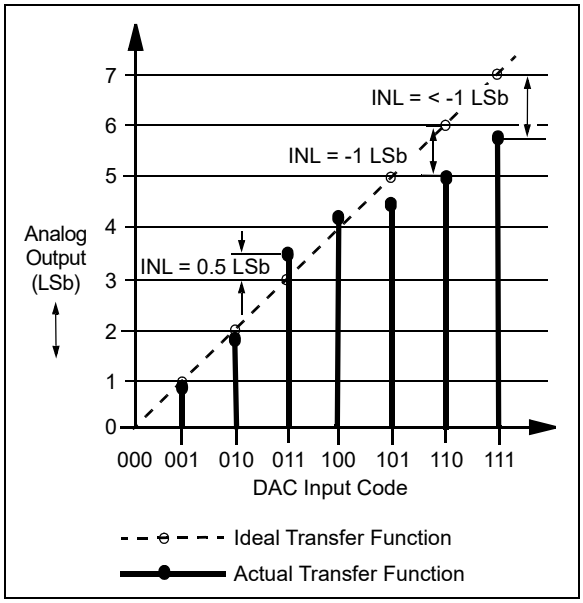

FIGURE B-4: *INL Accuracy.*

B.12 Differential Nonlinearity (DNL)

The differential nonlinearity error (DNL) (see Figure B-5) is the measure of step-size between codes in an actual transfer function. The ideal step-size between codes is 1 LSb. A DNL error of zero implies that every code is exactly 1 LSb wide. If the DNL error is less than 1 LSb, the DAC ensures monotonic output and no missing codes. Equation B-7 shows how to calculate the DNL error between any two adjacent codes in LSb.

EQUATION B-7: DNL ERROR

$$E_{DNL} = \frac{(V_{OUT(code=n+1)} - V_{OUT(code=n)})}{V_{LSb(Measured)}} - 1$$

Where:

DNL = expressed in LSb

$V_{OUT(Code=n)}$ = measured DAC output voltage with a given DAC register code

$V_{LSb(Measured)}$ = for measured: $(V_{OUT(4032)} - V_{OUT(64)})/3968$

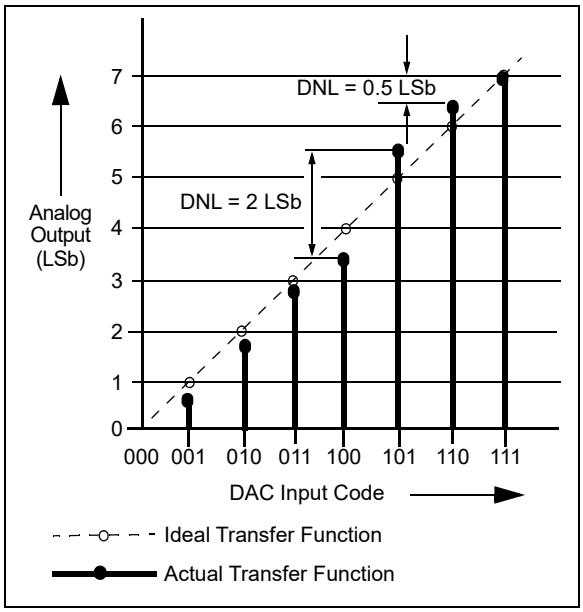

FIGURE B-5: *DNL Accuracy.*

B.13 Settling Time

The settling time is the time delay required for the V_{OUT} voltage to settle into its new output value. This time is measured from the start of code transition to when the V_{OUT} voltage is within the specified accuracy.

For the MCP48CXBX4/8, the settling time is a measure of the time delay until the V_{OUT} voltage reaches within 0.5 LSb of its final value, when the volatile DAC register changes from 1/4 to 3/4 of the FSR (12-bit device: 400h to C00h).

B.14 Major Code Transition Glitch

Major code transition glitch is the impulse energy injected into the DAC analog output when the code in the DAC register changes the state. It is normally specified as the area of the glitch in nV-Sec and is measured when the digital code is changed by 1 LSb at the major carry transition (Example: `011...111` to `100...000`, or `100...000` to `011...111`).

B.15 Digital Feedthrough

The digital feedthrough is the glitch that appears at the analog output caused by coupling from the digital input pins of the device. The area of the glitch is expressed in nV-Sec and is measured with a full-scale change (example: all '0's to all '1's and vice versa) on the digital input pins. The digital feedthrough is measured when the DAC is not being written to the output register.

B.16 -3 dB Bandwidth

This is the frequency of the signal at the V_{REF} pin that causes the voltage at the V_{OUT} pin to fall to -3 dB from a static value on the V_{REF} pin. The output decreases due to the RC characteristics of the resistor ladder and the characteristics of the output buffer.

B.17 Power Supply Sensitivity (PSS)

PSS indicates how the output of the DAC is affected by changes in the supply voltage. PSS is the ratio of the change in V_{OUT} to a change in V_{DD} for mid-scale output of the DAC. The V_{OUT} is measured while the V_{DD} is varied from 5.5V to 2.7V as a step (V_{REF} voltage held constant) and expressed in %/%, which is the % change of the DAC output voltage with respect to the % change of the V_{DD} voltage.

EQUATION B-8: PSS CALCULATION

$$PSS = \frac{(V_{OUT(@5.5V)} - V_{OUT(@2.7V)})/V_{OUT(@5.5V)}}{(5.5V - 2.7V)/(5.5V)}$$

Where:

PSS = expressed in %/%

$V_{OUT(@5.5V)}$ = measured DAC output voltage with V_{DD} = 5.5V

$V_{OUT(@2.7V)}$ = measured DAC output voltage with V_{DD} = 2.7V

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B.18 Power Supply Rejection Ratio (PSRR)

PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. The V_{OUT} is measured while the V_{DD} is varied ±10% (V_{REF} voltage held constant) and expressed in dB or µV/V.

B.19 V_{OUT} Temperature Coefficient

The V_{OUT} temperature coefficient quantifies the error in the resistor ladder's resistance ratio (DAC register code value) and output buffer due to temperature drift.

B.20 Absolute Temperature Coefficient

The absolute temperature coefficient quantifies the error in the end-to-end output voltage (nominal output voltage, V_{OUT}) due to temperature drift. For a DAC, this error is typically not an issue due to the ratiometric aspect of the output.

B.21 Noise Spectral Density

The noise spectral density is a measurement of the device's internally generated random noise and is characterized as a spectral density (voltage per √Hz). It is measured by loading the DAC to the mid-scale value and measuring the noise at the V_{OUT} pin. It is measured in nV/√Hz.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X(1)	—	XX	X	/XX
Device	Tape and Reel		Pin Count	Temperature Range	Package

Device:	MCP48CXBX4/8:	1 LSb INL Voltage Output, Digital-to-Analog Converters with SPI Interface, 8/10/12-Bit Resolution, Quad/Octal Outputs and Volatile/MTP Memory
Tape and Reel:	T =	Tape and Reel
Temperature Range:	E =	-40°C to +125°C (Extended)
Package:	ST =	Thin Shrink Small Outline Package (TSSOP), 20-Lead
	ML =	Plastic Quad Flat, No Lead Package (QFN), 4 mm x 4 mm, 20-Lead

Examples:

a) MCP48CVB04-20E/ST: 1 LSb INL Voltage Output Digital-to-Analog Converter, 8-Bit Resolution, Extended Temperature, 20LD TSSOP, with Volatile Memory

b) MCP48CVB04T-20E/ST: 1 LSb INL Voltage Output Digital-to-Analog Converter, 8-Bit Resolution, Tape and Reel, Extended Temperature, 20LD TSSOP, with Volatile Memory

c) MCP48CVB18-E/ML: 1 LSb INL Voltage Output Digital-to-Analog Converter, 10-Bit Resolution, Extended Temperature, 20LD QFN, with Volatile Memory

d) MCP48CVB18T-E/ML: 1 LSb INL Voltage Output Digital-to-Analog Converter, 10-Bit Resolution, Tape and Reel, Extended Temperature, 20LD QFN, with Volatile Memory

e) MCP48CMB24-E/ML: 1 LSb INL Voltage Output Digital-to-Analog Converter, 12-Bit Resolution, Extended Temperature, 20LD QFN, with MTP Memory

f) MCP48CMB28T-20E/ST: 1 LSb INL Voltage Output Digital-to-Analog Converter, 12-Bit Resolution, Tape and Reel, Extended Temperature, 20LD TSSOP, with MTP Memory

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