

Ultra-Low Power Audio CODEC for Headphone/Headsets Application With 124dB Class G Headphone Drive and Advanced Headset Features

Description

The NAU88L25B® is an Ultra-Low-Power High-Performance Audio CODEC Ground-Referenced Headphone Amplifier with Advanced Headset Detection. The single-chip solution with microphone and ground detection and switching capabilities is designed for smartphones, tablets, Personal Computers (PCs), and other portable devices that support both analog and digital audio functions. The NAU88L25B is a cost-optimized solution for audio jack applications that benefit from enhanced audio quality and more integrated detection and suppression functions. Additionally, when used in combination with the Nuvoton NuMicro® NUC123, an ARM® Cortex MO-based microprocessor, the NAU88L25B Audio CODEC provides an easy-to-implement design solution for USB headphones.

The highly-integrated NAU88L25B features one I2S/PCM Interface, one digital mixer, two high-quality audio Digital-to-Analog Converters (DACs), one high-quality audio Analog-to-Digital Converter (ADC), one monophonic differential analog microphone input, two analog single-ended microphone inputs, and one stereophonic Class G headphone amplifier with automatic headset detection. After automatically detecting which type of headset is in use—Stereo headphone, Nokia-type headsets, or Apple-type headsets—the NAU88L25B switches internal connections to support the appropriate format.

The advanced on-chip Digital Signal Processing (DSP) engine includes a Dynamic Range Compressor (DRC), and Programmable Bi-Quad Filters for various types of filters to optimize audio quality and eliminate undesirable frequency components. The NAU88L25B Audio CODEC provides comprehensive headset detection features that support jack insertion/ejection, microphone detection, distinct key / short key / long key / key release detection and Crosstalk detection/suppression. The chip also provides an integrated Frequency Locked Loop (FLL) to support various clocks.

The NAU88L25 operates with analog supply voltages from 1.6V to 1.8V, while the digital core can operate from 1.1V to 1.98V to conserve power. The NAU88L25 is specified for operation from -40°C to +85°C, and is available in QFN 32 or CSP package with 0.4mm pitch.

Features

- DAC with auto attenuate : 124dB SNR; without auto mute: 113dB SNR, (A-weighted) @ 0dB gain, 1.8V and -89dB THDN @ 20mW and RL= 32Ω, DAC playback to headphone output mode
- ADC : 101dB SNR (A-weighted) @ 0dB MIC gain, 1.8V, Fs = 48kHz and -91dB THD , 1.8V, MIC gain 0dB, OSR 128x
- One Digital I2S/PCM I/O port
- Dynamic Range Compressor (DRC)
- Programmable Biquad filter
- One Headset Mic: One Differential Analog Mic input, Line-input or two single-ended Mic input
- One Class G Stereo Headphone Amplifier(28mW @ 32Ω, 1% THD+N)
- Sampling rate from 8K to 192 KHz
- Autonomous Headset Microphone & Ground Detection and Switching
- Jack Insertion and Ejection Detection
- Distinct Keys Detection
- Package : 32 Pin QFN package, and 42 Balls WLCSP with 0.4mm Pitch

Applications

- Ultra-Portable Laptop
- Mobile Device
- Wireless or USB Headphone
- Smart Remote Controller
- Gaming Controller

Block Diagram

The NAU88L25B Audio CODEC is available in a QFN 32-Lead package and, in a WLCSP 42-Ball package, as shown in Figure 1 and Figure 2, respectively.

Figure 1: NAU88L25B Block Diagram for 32-Lead QFN Package

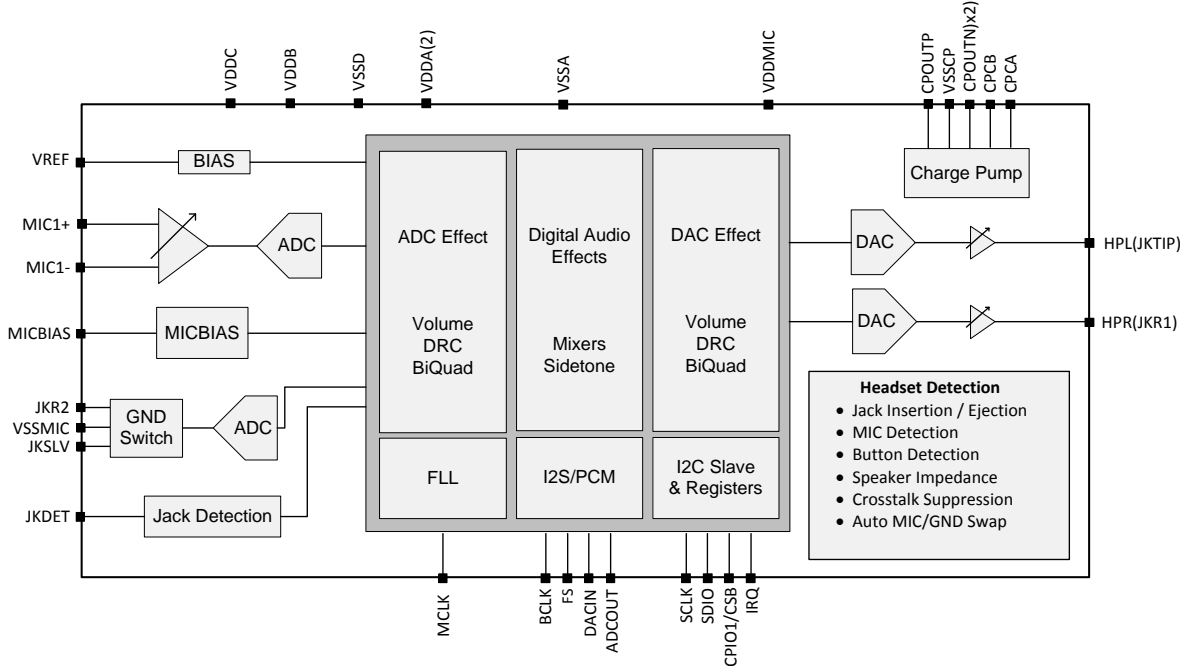
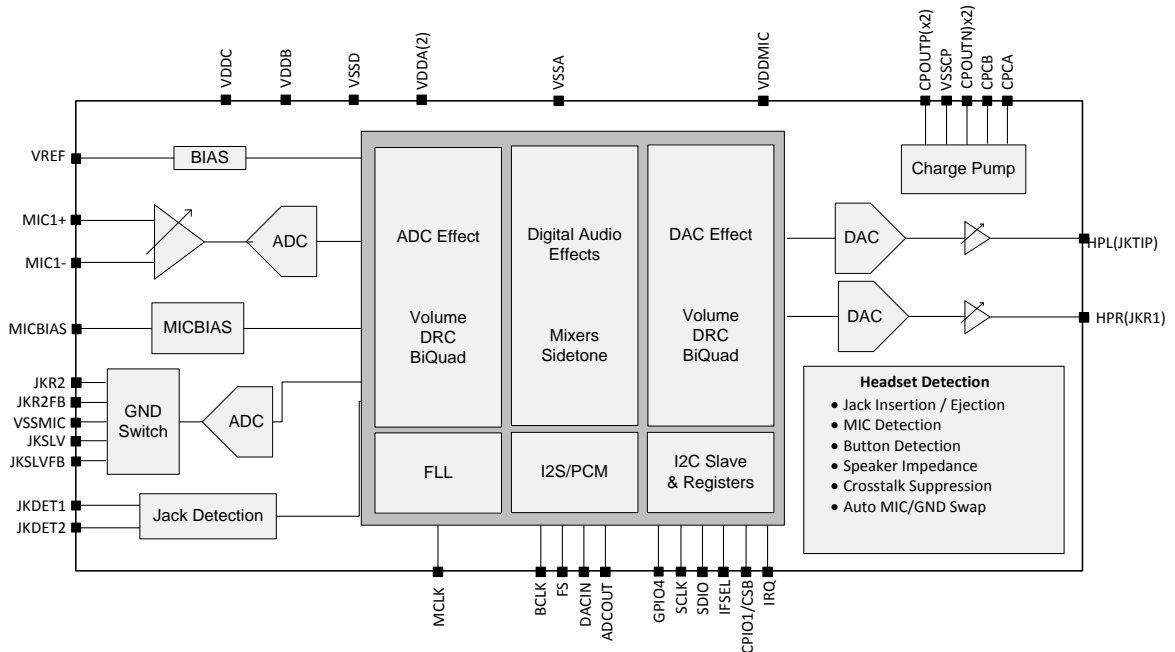


Figure 2: NAU88L25B Block Diagram for 42-Ball WLCSP Package



Pin Diagram

Figure 3 and 4 shows the pin diagram of QFN 32-Lead and WLCSP 42 ball package respectively.

Figure 3: NAU88L25B Pin Diagram for 32-Lead QFN Package

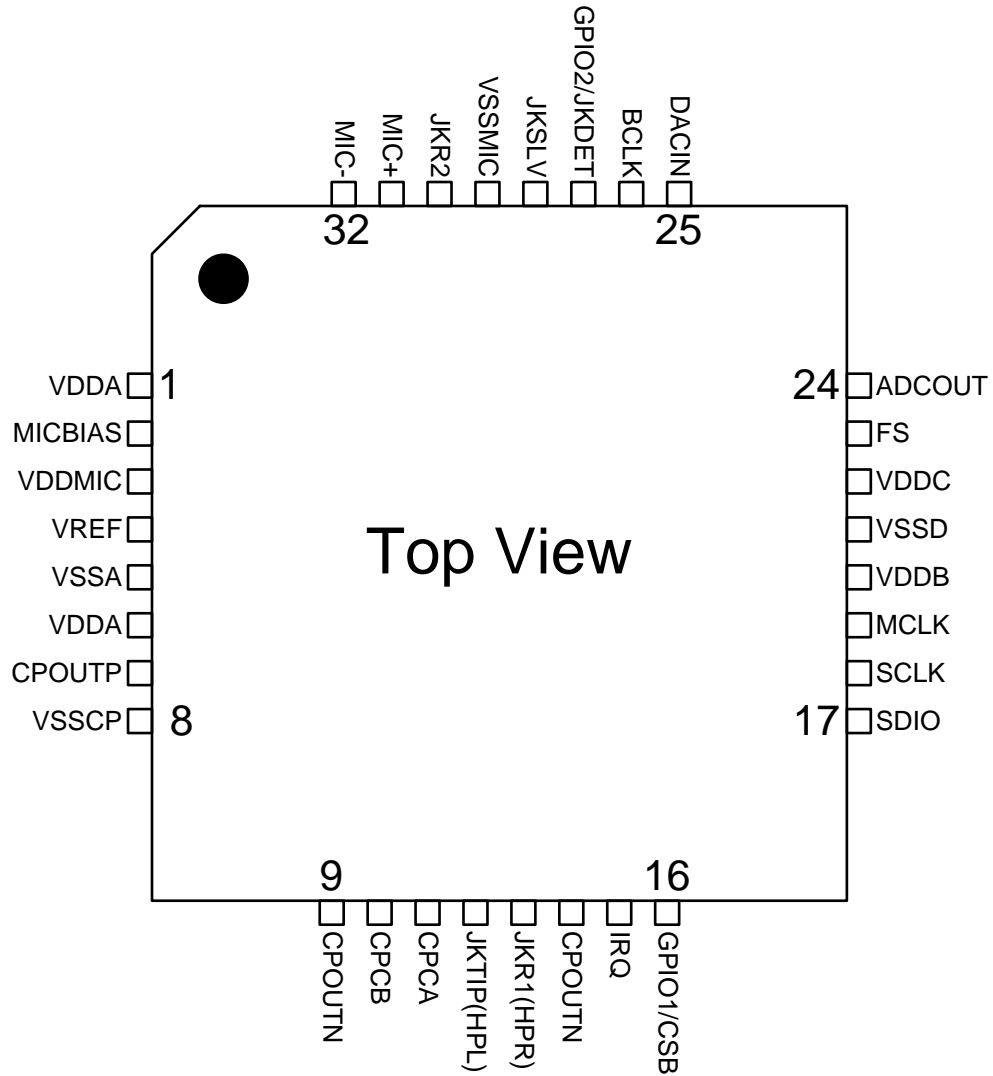
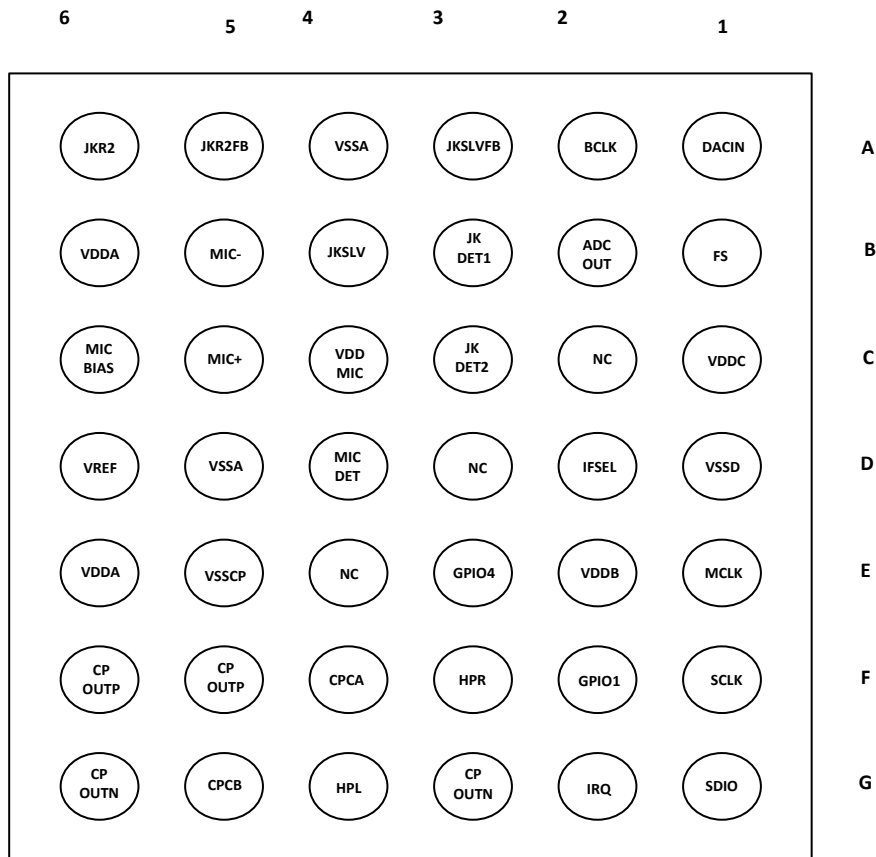


Figure 4: NAU88L25B Pin Diagram for 42-Ball WLCSP Package



Bottom View

Pin Descriptions

Pin Descriptions for the NAU88L25B are shown in **Table 1** and **Table 2** by package type.

Table 1 Pin Descriptions for 32-Lead QFN

| Pin # | Name | Type | Functionality |
|-------|------------|----------------|---|
| 1 | VDDA | Supply | Analog Supply |
| 2 | MICBIAS | Analog Output | Microphone Bias Output |
| 3 | VDDMIC | Supply | Microphone Supply |
| 4 | VREF | Analog I/O | Internal DAC & ADC Voltage Reference Decoupling I/O |
| 5 | VSSA | Ground | Analog Supply Ground |
| 6 | VDDA | Supply | Analog Supply |
| 7 | CPOUTP | Analog I/O | Charge Pump Positive Voltage |
| 8 | VSSCP | Ground | Charge Pump Supply Ground |
| 9 | CPOUTN | Analog I/O | Charge Pump Negative Voltage |
| 10 | CPCB | Analog I/O | Charge Pump Switching Capacitor Node B |
| 11 | CPCA | Analog I/O | Charge Pump Switching Capacitor Node A |
| 12 | JKTIP(HPL) | Analog Output | Jack Tip; Headphone Left Channel Output |
| 13 | JKR1(HPR) | Analog Output | Jack Ring 1; Headphone Right Channel Output |
| 14 | CPOUTN | Analog I/O | Charge Pump Negative Voltage |
| 15 | IRQ | Digital Output | Programmable Interrupt Output |
| 16 | GPIO1 | Digital I/O | General Purpose I/O/I2C Address |
| 17 | SDIO | Digital I/O | Serial Data for I2C |
| 18 | SCLK | Digital Input | Serial Data Clock for I2C |
| 19 | MCLK | Digital Input | CODEC Master Clock Input |
| 20 | VDDDB | Supply | Digital IO Supply |
| 21 | VSSD | Ground | Digital IO Ground |
| 22 | VDDC | Supply | Digital Core Supply |
| 23 | FS | Digital I/O | Frame Sync Input or Output for I2S or PCM Data |
| 24 | ADCOUT | Digital Output | Serial Audio Data Output for I2S or PCM Data |
| 25 | DACIN | Digital Input | Serial Audio Data Input for I2S or PCM Data |
| 26 | BCLK | Digital I/O | Serial Data Bit Clock Input or Output for I2S or PCM Data |
| 27 | JKDET | Analog Input | Jack Detect Input |
| 28 | JKSLV | Analog I/O | Jack Sleeve; Headset Jack Pin 4 |
| 29 | VSSMIC | Ground | Analog Supply Ground |
| 30 | JKR2 | Analog I/O | Jack Ring 2; Headset Jack Pin 3 |
| 31 | MIC+ | Analog Input | PGA MIC+ Analog Input |
| 32 | MIC- | Analog Input | PGA MIC- Analog Input |

Table 2 Pin Descriptions 42-Ball WLCSP

| Pin # | Name | Type | Functionality |
|-------|-----------|----------------|---|
| A1 | DACIN | Digital Input | Serial Audio Data Input for I2S or PCM Data |
| A2 | BCLK | Digital I/O | Serial Data Bit Clock Input or Output for I2S or PCM Data |
| A3 | JKSLVFB | Analog I | Jack Sleeve Feedback Sense Input |
| A4 | VSSA | Ground | Analog Supply Ground |
| A5 | JKR2FB | Analog I | JackRing 2 Feedback Sense Input |
| A6 | JKR2 | Analog I/O | JackRing 2 Jack Terminal |
| B1 | FS | Digital I/O | Frame Sync Input or Output for I2S or PCM Data |
| B2 | ADCOUT | Digital Output | Serial Audio Data Output for I2S or PCM Data |
| B3 | JKDET1 | Analog Input | Jack Detect Input |
| B4 | JKSLV | Analog I/O | Jack Sleeve Jack Terminal |
| B5 | MIC- | Analog Input | PGA MIC- Analog Input |
| B6 | VDDA | Supply | Analog Supply |
| C1 | VDDC | Supply | Digital Core Supply |
| C2 | NC | No Connect | This pin should remain not connected |
| C3 | JKDET2 | Analog Input | Jack Detect Input |
| C4 | VDDMIC | Supply | Microphone Supply |
| C5 | MIC+ | Analog Input | PGA MIC+ Analog Input |
| C6 | MICBIAS | Analog Output | Microphone Bias Output |
| D1 | VSSD | Ground | Analog Supply Ground |
| D2 | IFSEL | Digital Input | I2C/SPI Interface selection |
| D3 | NC | No Connect | This pin should remain not connected |
| D4 | MICDET | Analog I/O | Microphone Signal and SAR ADC Input |
| D5 | VSSA | Ground | Analog Supply Ground |
| D6 | VREF | Analog I/O | Internal DAC & ADC Voltage Reference Decoupling I/O |
| E1 | MCLK | Digital Input | CODEC Master Clock Input |
| E2 | VDDDB | Supply | Digital IO Supply |
| E3 | GPIO4 | Digital Output | Serial Data Output for SPI Data |
| E4 | NC | No Connect | This pin should remain NOT CONNECTED |
| E5 | VSSCP | Ground | Charge Pump Supply Ground |
| E6 | VDDA | Supply | Analog Supply |
| F1 | SCLK | Digital Input | Serial Data Clock for I2C |
| F2 | GPIO1 | Digital I/O | General Purpose Input Output/I2C Address |
| F3 | JKR1(HPR) | Analog Output | Jack Ring 1; Headphone Right Channel Output |
| F4 | CPCA | Analog I/O | Charge Pump Switching Capacitor Node A |
| F5 | CPOUTP | Analog I/O | Charge Pump Positive Voltage |
| F6 | CPOUTP | Analog I/O | Charge Pump Positive Voltage |
| G1 | SDIO | Digital I/O | Serial Data for I2C |

| Pin # | Name | Type | Functionality |
|-------|------------|----------------|---|
| G2 | IRQ | Digital Output | Programmable Interrupt Output |
| G3 | CPOUTN | Analog I/O | Charge Pump Negative Voltage |
| G4 | JKTIP(HPL) | Analog Output | Jack Tip; Headphone left channel output |
| G5 | CPCB | Analog I/O | Charge Pump Switching Capacitor Node B |
| G6 | CPOUTN | Analog I/O | Charge Pump Negative Voltage |

Note: Analog I/O supply is VDDA; Digital I/O supply is VDDB.

Electrical Characteristics

Absolute Maximum Ratings

Table 3 provides the absolute maximum ratings for the NAU88L25B Audio CODEC.

CAUTION: Do not operate at or near maximum ratings extended periods. Stresses above those listed in Table 3 may cause permanent damage to the device. Exposure to conditions beyond these ratings may adversely affect the life and reliability of the device and result in failures not covered by warranty.

Table 3 Absolute Maximum Ratings

| Parameter | Min | Max | Units |
|--------------------------------|------------|-----------|-------|
| Junction Temperature, T_J | -40 | +150 | °C |
| Storage Temperature | -65 | +150 | °C |
| Analog Supply Range | -0.3 | 2.2 | V |
| Digital I/O Supply Range | -0.3 | 6.0 | V |
| Digital Supply Range | -0.3 | 2.2 | V |
| Input Voltage Digital Range | DGND - 0.3 | VDD + 0.3 | V |
| Input Voltage Analog Range | AGND - 0.3 | VDD + 0.3 | V |
| Headphone Supply Range | -0.3 | 2.2 | V |
| Microphone Bias Supply Voltage | -0.3 | 6.0 | V |

Operating Conditions

Table 4 provides the recommended operating conditions for the NAU88L25B.

Table 4 Operating Conditions

| Condition | Symbol | Min | Typical | Max | Units |
|---|---------------------|---------------------|---------|------|-------|
| Analog Supply Range | VDDA | 1.6 | 1.8 | 2.0 | V |
| Digital Supply Range | VDDC | 1.1 | 1.2 | 1.98 | V |
| Digital Supply Range for FLL Operation and for $F_s > 48$ KHz | VDDC | 1.61 | 1.8 | 1.98 | V |
| Digital I/O Supply Range | Vddb | 1.6 | 1.8 | 3.6 | V |
| Headphone Supply Range | VDDA | 1.6 | 1.8 | 2.0 | V |
| Microphone Bias Supply Voltage | VDDMIC | 2.5 | 4.2 | 5.0 | V |
| Temperature Range | TA | -40 | | +85 | °C |
| QFN Package | Junction to Ambient | η_{ja}° | 33.1 | | °C/W |
| | Junction to Case | η_{jc}° | 3.1 | | °C/W |

Shutdown and Standby Current

Table 5 provides Shutdown and Standby currents.

Table 5 Shutdown and Standby Current

| Parameter | Symbol | Conditions | Typical | Limit | Units |
|------------------|--------|---------------------------------------|---------|-------|---------------|
| Shutdown Current | ISD | VDDA in Shutdown Mode | 0.2 | 1 | μA |
| | | VDDA When VDDC=1.2 V | 17.2 | | |
| | | VDDDB | 0.2 | 1 | |
| | | VDDC | 2 | 10 | |
| | | VDDMIC | 0.2 | 1 | |
| Standby Current | IDD | MCLK off, Jack Insertion, IRQ enabled | 5 | | μA |

ADC Characteristics

Table 6 provides the ADC electrical characteristics for the NAU88L25B Audio CODEC.

Conditions: VDDA = VDDDB = VDDC = 1.8 V; VDDMIC= 4.2 V. RL(Headphone) = 32 Ω , f = 1 kHz, MCLK=12.88 MHz, unless otherwise specified. Limits apply for TA = 25° C.

Table 6 ADC Electrical Characteristics

| Parameter | Symbol | Conditions | Typical | Limit | Units |
|---------------------------------------|--------|--|---------|-------|------------------|
| ADC Total Harmonic Distortion + Noise | THD+N | MIC Input, MIC_GAIN = 0 dB, VIN = 0.8 Vrms, f = 1 KHz, fs = 48 KHz, Mono Differential Input | -91 | | dB |
| | | MIC Input, MIC_GAIN = 30 dB, Volume = 0 dB, VIN = 28.5 Vrms, fs = 1 k, Digital Gain = 0 dB, Mono Differential Input | -80 | | dB |
| Signal-to-Noise Ratio | SNR | Reference = VOUT(0dBFS), A-Weighted, MIC Input, MIC Gain = 0 dB, fs = 8 KHz, Mono Differential Input | 101 | | dB |
| | | Reference = VOUT(0 dB FS), A-Weighted, MIC Input, MIC Gain = 6 dB, fs = 8 KHz, Mono Differential Input | 98 | | dB |
| Power Supply Rejection Ratio | PSRR | V _{RIPPLE} = 200 mV _{PP} applied to VDDA, f _{RIPPLE} = 217 Hz, Input Referred, MIC_GAIN = 0 dB Differential Input | 78 | | dB |
| Common Mode Rejection Ratio | CMRR | Differential Input 100 Vrms, PGA Gain = 20 dB, frequency sweep from 20 Hz to 20 KHz | 64 | | dB |
| ADC Full Scale Input Level | FSADC | VDDA= 1.8 V | 1 | | V _{RMS} |
| Minimum Input Impedance | | | 12 | | KOhm |

| Parameter | Symbol | Conditions | Typical | Limit | Units |
|--------------------|--------|--|---------|-------|-------|
| Frequency Response | | $f = 20 \text{ Hz} \sim 20 \text{ KHz}$ | +/-0.02 | | dB |
| Power Consumption | | No Load, No Signal, ADC on, PGA on; $f_s = 44.1 \text{ kHz}$ | 5.4 | | mW |

Headphone Amplifier Characteristics

Table 7 provides the headphone amplifier electrical characteristics for the NAU88L25B.

Conditions: $V_{DDA} = V_{DDB} = V_{DDC} = 1.8 \text{ V}$; $V_{DDMIC} = 4.2 \text{ V}$. $R_L(\text{Headphone}) = 32 \Omega$, $f = 1 \text{ kHz}$, $MCLK = 12.88 \text{ MHz}$, unless otherwise specified. Limits apply for $T_A = 25^\circ \text{ C}$.

Table 7 Headphone Amplifier Electrical Characteristics

| Parameter | Symbol | Conditions | Typical | Limit | Units |
|--|--------|--|---------|-------|-------|
| Output Power 32-Lead QFN Package | PO | Stereo $R_L = 16 \Omega$, DAC Input, $CPVDD = 1.8 \text{ V}$, $f = 1 \text{ kHz}$, 22 kHz BW, THD+N = 1% w. Headset Switch | 35 | | mW |
| | | Stereo $R_L = 32 \Omega$, DAC Input, $CPVDD = 1.8 \text{ V}$, $f = 1 \text{ kHz}$, 22 kHz BW, THD+N = 1%, w. Headset Switch | 28 | | mW |
| Output Power 42-Ball WLCSP Package | | Stereo $R_L = 16 \Omega$, DAC Input, $CPVDD = 1.8 \text{ V}$, $f = 1 \text{ kHz}$, 22 kHz BW, THD+N = 1%, w. Headset Switch | 39.5 | | mW |
| | | Stereo $R_L = 32 \Omega$, DAC Input, $CPVDD = 1.8 \text{ V}$, $f = 1 \text{ kHz}$, 22 kHz BW, THD+N = 1%, w. Headset Switch | 30.5 | | mW |
| Total Harmonic Distortion + Noise | THD+N | $R_L = 32 \Omega$, $f = 1 \text{ kHz}$, $PO = 20 \text{ mW}$, w. Headset Switch | -89 | | dB |
| Signal to Noise Ratio | SNR | $V_{OUT} = 1 \text{ VRMS}$, DAC Input, $DAC_Gain = 0 \text{ dB}$, $HP_Gain = 0 \text{ dB}$, Digital Zero Input, $f = 1 \text{ kHz}$, A-Weighted, w. Headset Switch | 113 | | dB |
| | | $V_{OUT} = 1 \text{ V}_{RMS}$, DAC Input, $DAC_Gain = 0 \text{ dB}$, $HP_Gain = 0 \text{ dB}$, Digital Zero Input, $f = 1 \text{ kHz}$, A-Weighted, Auto Mute Enabled, w. Headset Switch | 124 | | dB |

| Parameter | Symbol | Conditions | Typical | Limit | Units |
|------------------------------|-------------------|---|----------|-------|-------------------|
| Power Supply Rejection Ratio | PSRR | f _{RIPPLE} = 217 Hz, V _{RIPPLE} = 200 mV _{P-P} Input Referred, HP_GAIN = 0 dB DAC Input, DAC_Gain = 0 dB Ripple Applied to VDDA | 81 | | dB |
| Channel Crosstalk | X _{TALK} | Left Channel to Right Channel, -1 dB FS, Gain = 0 dB, f = 1 kHz, MIC/GND Switching Off without HCS | 88 | | dB |
| | | Left Channel to Right Channel, -1 dB FS, Gain = 0 dB, f = 1 kHz, MIC/GND Switching On with HCS (QFN) | 91 | | dB |
| | | Left Channel to Right Channel, -1 dB FS, Gain = 0 dB, f = 1 kHz, MIC/GND Switching On with HCS (WLCSP) | 98 | | dB |
| Interchannel Level Mismatch | | Headphone Right and Left Channel Difference with 0 dB FS Input Sweep from 20 Hz to 20 KHz | +/- 0.1 | | dB |
| Frequency Response | | F = 20 Hz ~ 20 KHz | +/-0.005 | | dB |
| Output Noise | e _{OS} | DAC_Gain = 0 dB, HP_Gain = 0 dB, f _S =48 kHz, OSRDAC = 128, A-Weighted | 2.2 | | μV _{RMS} |
| Out-of-Band Noise Level | | BW= 400 Hz to 500 KHz | -86 | | dB |
| Output Offset Voltage | VOS | HP_Gain = 0 dB, DAC_Gain= 0 dB, DAC Input | 0.1 | ±0.5 | mV |
| Power Consumption | | No Load, No Signal, Amp on f _S = 48 kHz, Stereo DAC On, Amp On, POUT = 0 mW. R _L = 32 Ω | 5.7 | | mW |
| Pop-and-Click Noise | | Into or out of DAC to Headphone Shutdown, Headphone Impedance & Crosstalk Detection Disabled | .1 | | mVrms |
| Ground Switch ON Resistance | | ON Resistance between JKR2 and GND or JKSLV and GND (QFN) | .09 | | Ohm |
| | | ON Resistance between JKR2 and GND or JKSLV and GND (WLCSP) | 0.075 | | Ohm |

Digital I/O Characteristics

Table 8 provides the headphone amplifier electrical characteristics for the NAU88L25B.

Conditions: $V_{DDA} = V_{DDB} = V_{DDC} = 1.8\text{ V}$; $V_{DDMIC} = 4.2\text{ V}$. $R_L(\text{Headphone}) = 32\ \Omega$, $f = 1\text{ kHz}$, $MCLK = 12.88\text{ MHz}$, unless otherwise specified. Limits apply for $T_A = 25^\circ\text{ C}$.

Table 8 Digital I/O Characteristics

| Parameter | Symbol | Comments/Conditions | Min | Max | Units |
|-------------------|--------|--------------------------|--------------------------|------------------------|-------|
| Input LOW Level | VIL | V _{DDB} = 1.8 V | | 0.33* V _{DDB} | V |
| | | V _{DDB} = 3.3 V | | 0.37**V _{DDB} | |
| Input HIGH Level | VIH | V _{DDB} = 1.8 V | 0.67* V _{DDB} | | V |
| | | V _{DDB} = 3.3 V | 0.63* V _{DDB} | | |
| Output HIGH Level | VOH | I _{Load} = 1mA | V _{DDB} = 1.8 V | 0.9* V _{DDB} | V |
| | | | V _{DDB} = 3.3 V | 0.95* V _{DDB} | |
| Output LOW Level | VOL | I _{Load} = 1mA | V _{DDB} = 1.8 V | 0.1* V _{DDB} | V |
| | | | V _{DDB} = 3.3 V | 0.05* V _{DDB} | |

Ordering Information

Table 9 provides dimensions and packaging information for the NAU88L25B Audio CODECs.

Table 9 Ordering Information

| Part Number | Dimension | Package | Package Material |
|-------------|------------------|----------------|------------------|
| NAU88L25YGB | 5 x 5 mm | QFN-32 Lead | Green |
| NAU88L25VGB | 2.552 x 2.915 mm | WLCSP 42-Balls | Green |

NAU88L25 = Part Name

L = Low-Power Product

Lead-Free (Green) Packaging:

YG = indicates QFN packaging

VG = indicates WLCSP packaging WLCSP

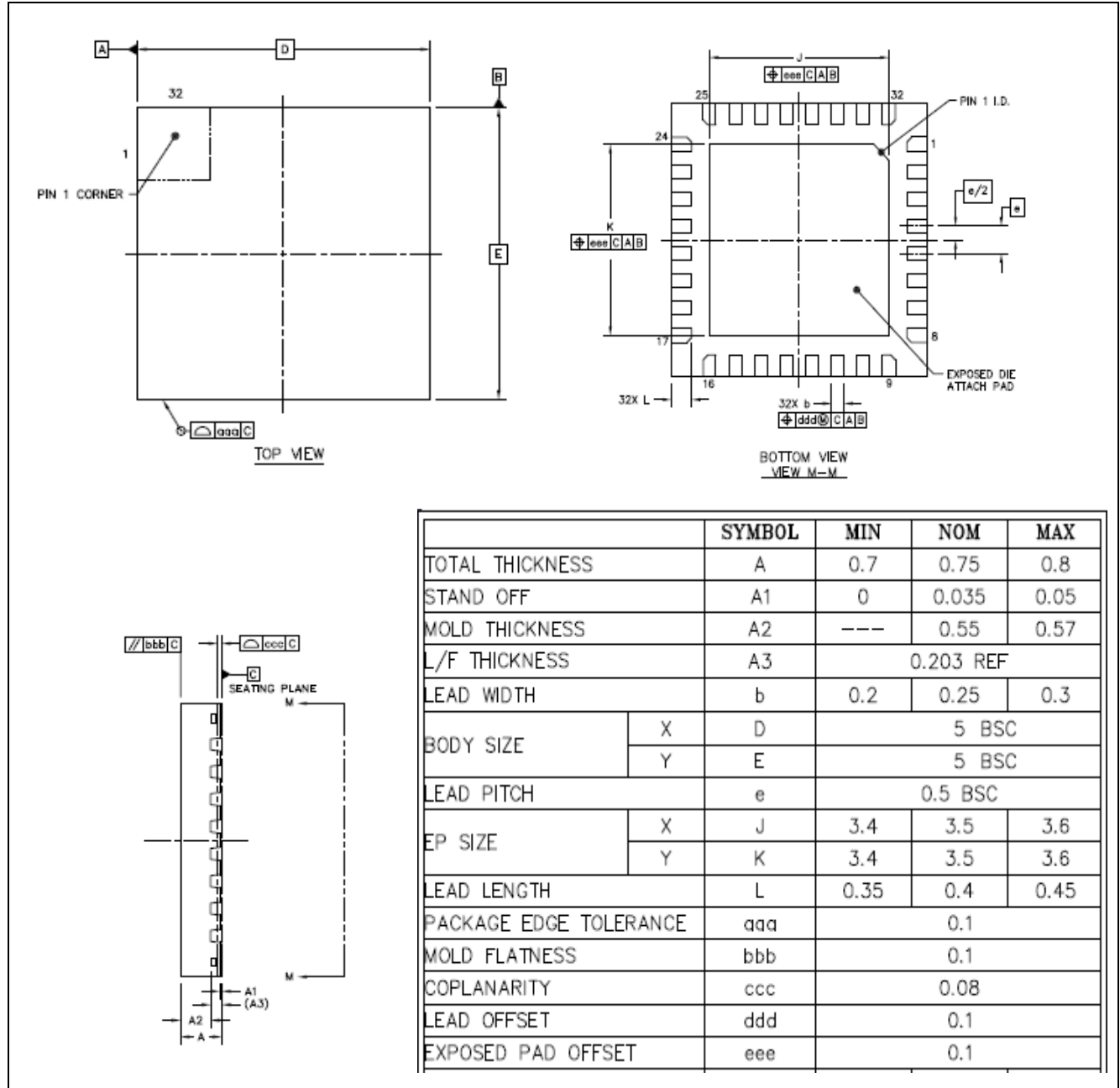
B = Chip Revision

Package Information

QFN 32-Lead Package

QFN32L 5X5 mm², Thickness 0.8 mm (Max) , Pitch 0.5 mm (Saw Type) EP SIZE 3.5 X 3.5 mm.

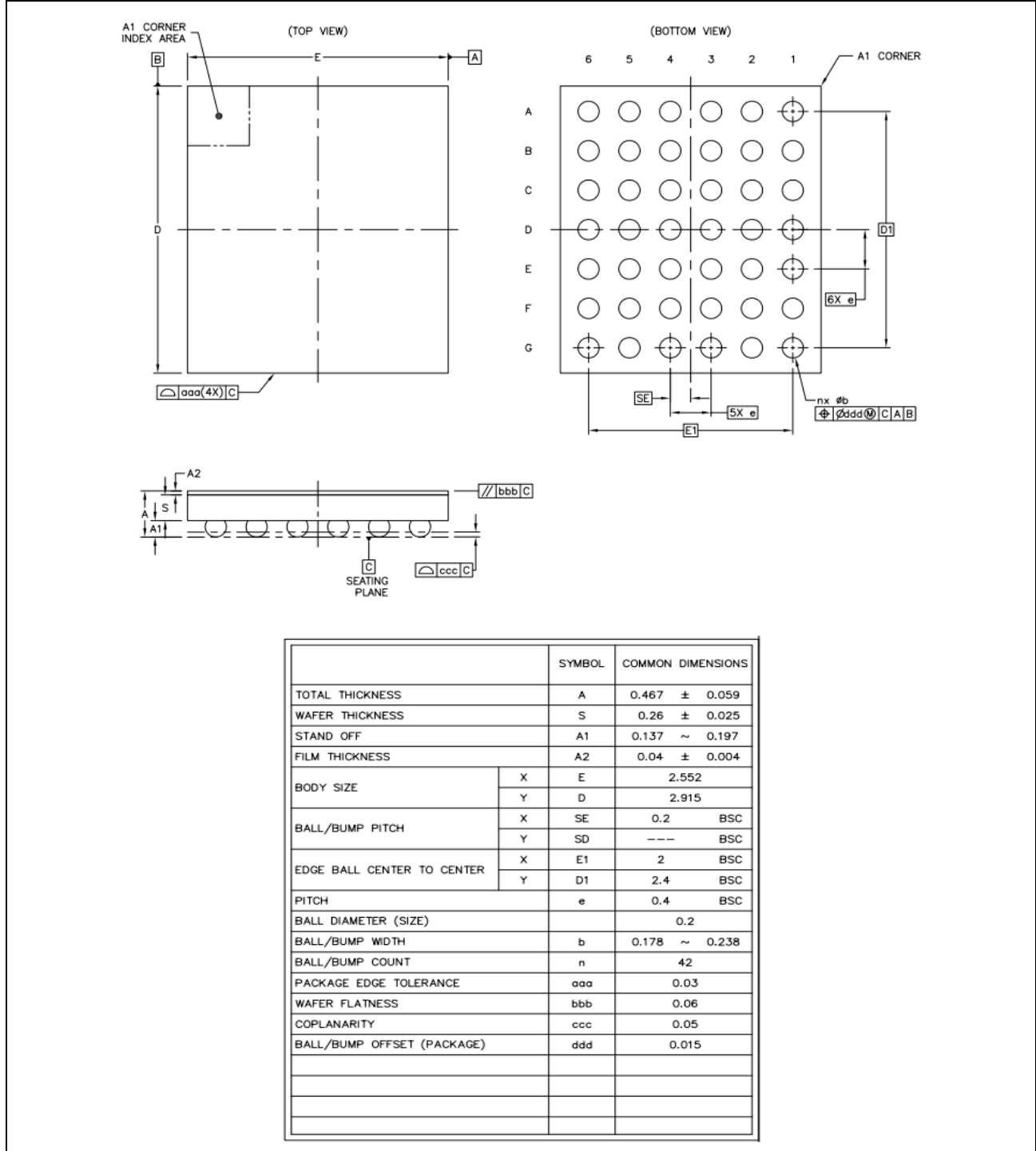
Figure 5 QFN 32-Lead Package



WLCSP 42-Ball Package

WLCSP 42-Balls package, 2.552 x 2.915 mm, with 0.4 mm Pitch.

Figure 6 WLCSP 42-Ball Package



Revision History

Table 10: Revision History

| Version | | | Description |
|---------|---------------|---------------------|---|
| # | Date | Page(s) | |
| 0.1 | Nov 20, 2014 | NA | Preliminary Version |
| 0.2 | Mar 10, 2015 | | Updated the pin-out and pin-descriptions |
| 0.3 | Apr 10, 2015 | 8 | Ordering info is added. |
| 0.4 | Jun 15, 2015 | 5, 6 | Updated Electrical Characteristics |
| 0.5 | July 16, 2015 | 1 | Updated the descriptions |
| 0.6 | Sep 28, 2015 | 1, 2, 7, 8 | Updated the descriptions and key features Updated the block diagram Changed VIH (input high voltage) Updated the package information |
| 0.7 | Oct 27, 2015 | 9 | Updated the package info |
| 1.0 | Aug 19, 2016 | All | Content format changes, edits for grammar and clarity. Color removed from graphics. |

Important Notice

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