LMH6629 Ultra-Low Noise, High-Speed Operational Amplifier with Shutdown

1 Features

- Specified for V_S = 5 V, R_L = 100 Ω, A_V = 10V/V WSON-8 Package, unless Specified. –3dB Bandwidth 900 MHz
- Input Voltage Noise 0.69 nV/√Hz
- Input Offset Voltage Max. Over Temperature ±0.8 mV
- Slew Rate 1600 V/ µs
- HD2 @ f = 1 MHz, $2V_{PP}$ −90 dBc
- HD3 @ f = 1 MHz, $2V_{PP}$ −94 dBc
- Supply Voltage Range 2.7 V to 5.5 V
- Typical Supply Current 15.5 mA
- Selectable Min. Gain ≥4 or ≥10 V/V
- Enable Time: 75 ns
- Output Current ±250 mA
- WSON-8 and SOT-23-5 Packages

2 Applications

- Instrumentation Amplifiers
- Ultrasound Pre-amps
- Wide-band Active Filters
- Opto-Electronics
- Medical Imaging Systems
- Base-Station Amplifiers
- Low-Noise Single Ended to Differential Conversion
- Trans-Impedance Amplifier

3 Description

The LMH6629 is a high-speed, ultra-low noise amplifier designed for applications requiring wide bandwidth with high gain and low noise such as in communication, test and measurement, optical and ultrasound systems.

The LMH6629 operates on 2.7-V to 5.5-V supply with an input common mode range that extends below ground and outputs that swing to within 0.8 V of the rails for ease of use in single supply applications. Heavy loads up to ±250 mA can be driven by high-frequency large signals with the LMH6629's –3dB bandwidth of 900 MHz and 1600 V/µs slew rate. The LMH6629 (WSON-8 package only) has user-selectable internal compensation for minimum gains of 4 or 10 controlled by pulling the COMP pin low or high, thereby avoiding the need for external compensation capacitors required in competitive devices. Compensation for the SOT-23-5 package is internally set for a minimum stable gain of 10 V/V. The WSON-8 package also provides the power-down enable/disable feature.

The low-input noise (0.69 nV/√Hz and 2.6 pA/√Hz), low distortion (HD2/HD3 = −90 dBc/−94 dBc) and ultra-low DC errors (800 µV V_{OS} maximum over temperature, ±0.45 µV/°C drift) allow precision operation in both ac- and dc-coupled applications.

The LMH6629 is fabricated in Texas Instruments' proprietary SiGe process and is available in a 3 mm × 3 mm 8-pin WSON package as well as the SOT-23-5 package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMH6629	SOT-23 (5)	2.90 mm × 1.60 mm
	WSON (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Transimpedance Amplifier

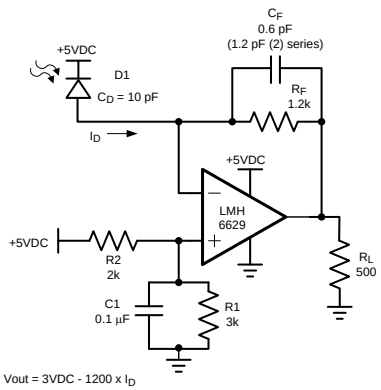


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (October 2014) to Revision I — **Page**

- Updated ESD Ratings table. ... 4
- Revised paragraph beginning with "The optimum value of "C_F in the *Low-Noise Transimpedance Amplifier* section ... 29
- Updated *Related Documentation* section ... 38

Changes from Revision G (March 2013) to Revision H — **Page**

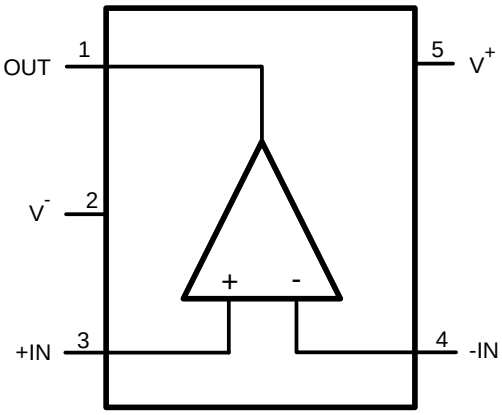
- Added, updated, or renamed the following sections: Device Information Table, *Pin Configuration and Functions*, *Application and Implementation*; *Power Supply Recommendations*; *Layout*; *Device and Documentation Support*; *Mechanical, Packaging, and Ordering Information* ... 1

Changes from Revision F (March 2013) to Revision G — **Page**

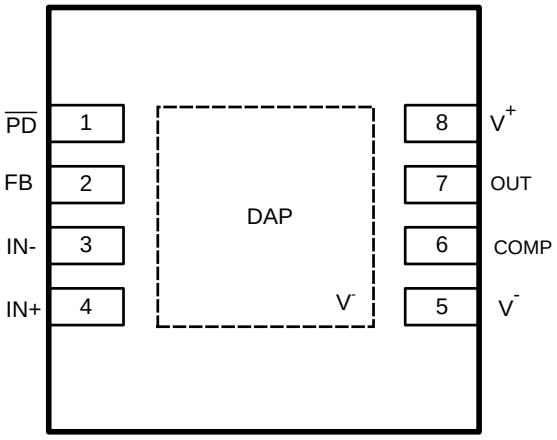
- Changed layout of National Data Sheet to TI format ... 1

5 Pin Configuration and Functions

5-Pin
Package DBV
Top View



8-Pin
Package NGQ08A
Top View



Pin Functions

NAME	NUMBER		I/O	DESCRIPTION
	DBV	NGQ08A		
COMP		6	I	Compensation
FB		2	I/O	Feedback
-IN	4	3	I	Inverting input
+IN	3	4	I	Non-inverting input
OUT	1	7	O	Output
$\overline{PD}$		1	I	Power Down
V^-	2	5	I	Negative supply
V^+	5	8	I	Positive supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)(3)

	MIN	MAX	UNIT
Positive Supply Voltage	−0.5	6.0	V
Differential Input Voltage		3	V
Input current		±10	mA
Analog Input Voltage		−0.5 to V_S	V
Digital Input Voltage		−0.5 to V_S	V
Junction Temperature		+150	°C
Storage Temperature (T_{stg})	−65	+150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Machine model	±200	
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±750 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	NOM	MAX	UNIT
Supply Voltage (V^+ - V^-)	2.7		5.5	V
Operating Temperature Range	−40		+125	°C

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.

6.4 Thermal Information

THERMAL METRIC(1)		DBV	NGQ08A	UNIT
		5 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	179	71	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics 5V

The following specifications apply for single supply with V_S = 5 V, R_L = 100 Ω terminated to 2.5 V, gain = 10V/V, V_O = $2V_{PP}$, V_{CM} = V_S/2, COMP Pin = HI (WSON-8 package), unless otherwise noted.(1)

PARAMETER		TEST CONDITIONS	T_A = 25°C			UNIT
			MIN(2)	TYP(3)	MAX(2)	
DYNAMIC PERFORMANCE						
SSBW	Small Signal −3dB bandwidth	V_O = 200 mV_{PP}, WSON-8 package		900		MHz
		V_O = 200 mV_{PP}, SOT-23-5 package		1000		
		A_V= 4, V_O = 200 mV_{PP}, COMP Pin = LO		800		
LSBW	Large signal −3dB bandwidth	V_O = $2V_{PP}$		380		MHz
		COMP Pin = LO, A_V= 4, V_O = $2V_{PP}$		190		
	0.1 dB bandwidth	A_V= 10, V_O = 200 mV_{PP}, WSON-8 package		330		MHz
		A_V= 10, V_O = 200 mV_{PP}, SOT-23-5 package		190		
		A_V= 4, V_O = 200 mV_{PP}, COMP Pin = LO		95		
	Peaking	V_O = 200 mV_{PP}, WSON-8 package		0		dB
		V_O = 200 mV_{PP}, SOT-23-5 package		2		
SR	Slew rate	A_V= 10, 2 V step		1600		V/µs
		A_V= 4, 2 V step, COMP Pin = LO		530		
t_r/ t_f	Rise/fall time	A_V= 10, 2 V step, 10% to 90%, WSON-8 package		0.90		ns
		A_V= 10, 2 V step, 10% to 90%, SOT-23-5 package		0.95		
		A_V= 4, 2 V step, 10% to 90%, COMP Pin = LO, (Slew Rate Limited)		2.8		
T_s	Settling time	A_V= 10, 1 V step, ±0.1%		42		
	Overload recovery	V_{IN} = 1 V_{PP}		2		
NOISE and DISTORTION						
HD2	2nd Order distortion	fc = 1 MHz, V_O = 2 V_{PP}		−90		dBc
		COMP Pin = LO, A_V= 4, fc = 1 MHz, V_O = 2 V_{PP}		−88		
		fc = 10 MHz, V_O = 2 V_{PP}		−70		
		COMP Pin = LO, fc = 10 MHz, A_V= 4 V, V_O = 2 V_{PP}		−65		
HD3	3rd Order distortion	fc = 1 MHz, V_O = $2V_{PP}$		−94		dBc
		COMP Pin = LO, A_V= 4, fc = 1 MHz, V_O = 2 V_{PP}		−87		
		fc = 10 MHz, V_O = 2 V_{PP}		−82		
		COMP Pin = LO, fc = 10 MHz, V_O = $2V_{PP}$		−75		
OIP3	Two-tone 3rd order intercept point	fc = 25 MHz, V_O = 2 V_{PP} composite		31		dBm
		fc = 75 MHz, V_O = 2 V_{PP} composite		27		
e_n	Noise voltage	Input referred f > 1MHz		0.69		nV/√Hz
i_n	Noise current			2.6		pA/√Hz
NF	Noise figure	R_S = R_T = 50 Ω		8.0		dB

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A.
(2) All limits are ensured by testing or statistical analysis
(3) Typical numbers are the most likely parametric norm.

Electrical Characteristics 5V (continued)

The following specifications apply for single supply with V_S = 5 V, R_L = 100 Ω terminated to 2.5 V, gain = 10V/V, V_O = $2V_{PP}$, V_{CM} = V_S/2, COMP Pin = HI (WSON-8 package), unless otherwise noted.(1)

PARAMETER		TEST CONDITIONS		T_A = 25°C MIN(2)	TYP(3)	MAX(2)	UNIT
ANALOG I/O							
CMVR	Input voltage range	CMRR > 70 dB, WSON-8 package		−0.30		3.8	V
		CMRR > 70 dB, SOT-23-5 package			−0.30 to 3.8		
V_O	Output voltage range	R_L = 100 Ω to V_S/2		0.89	0.82 to 4.19	4.0	V
			-40°C ≤ T_J ≤ +125°C	0.95		3.9	
		No Load		0.76	0.72 to 4.28	4.1	
			-40°C ≤ T_J ≤ +125°C	0.85		4.0	
I_{OUT}	Linear output current	V_O = 2.5 V (4)			250		mA
V_{OS}	Input offset voltage				±150	±780	µV
		-40°C ≤ T_J ≤ +125°C				±800	
TcV_{OS}	Input offset voltage temperature drift	See (5)			±0.45		µV/°C
I_{BI}	Input bias current	See (6)			−15	−23	µA
			-40°C ≤ T_J ≤ +125°C			−37	
I_{OS}	Input offset current				±0.1	±1.8	µA
		-40°C ≤ T_J ≤ +125°C				±3.0	
T_CI_{OS}	Input offset voltage temperature drift	See (5)			±2.8		nA/°C
C_{CM}	Input capacitance	Common Mode			1.7		pF
C_{DIFF}		Differential Mode(7)			4		
R_{CM}	Input resistance	Common Mode			450		kΩ
MISCELLANEOUS PARAMETERS							
CMRR	Common mode rejection ratio	V_{CM} from 0 V to 3.7 V, WSON-8 package		82	87		dB
			-40°C ≤ T_J ≤ +125°C	70			
		V_{CM} from 0 V to 3.7 V, SOT-23-5 package			87		
PSRR	Power supply rejection ratio			81	83		
		-40°C ≤ T_J ≤ +125°C		78			
A_{VOL}	Open loop gain	WSON-8 package		74	78		
			-40°C ≤ T_J ≤ +125°C	72			
		SOT-23-5 package			78		

(4) The maximum continuous output current (I_{OUT}) is determined by device power dissipation limitations. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C
(5) Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.
(6) Negative input current implies current flowing out of the device
(7) Simulation results.

Electrical Characteristics 5V (continued)

The following specifications apply for single supply with V_S = 5 V, R_L = 100 Ω terminated to 2.5 V, gain = 10V/V, V_O = $2V_{PP}$, V_{CM} = V_S/2, COMP Pin = HI (WSON-8 package), unless otherwise noted.(1)

PARAMETER		TEST CONDITIONS		T_A = 25°C MIN(2)	T_A = 25°C TYP(3)	T_A = 25°C MAX(2)	UNIT
DIGITAL INPUTS/TIMING							
V_{IL}	Logic low-voltage threshold	$\overline{PD}$ and COMP pins, WSON-8 package				0.8	V
V_{IH}	Logic high-voltage threshold	$\overline{PD}$ and COMP pins, WSON-8 package		2.5			V
I_{IL}	Logic Low-bias current	$\overline{PD}$ and COMP pins = 0.8 V, WSON-8 package(6)		−23	−28	−34	µA
			-40°C ≤ T_J ≤ +125°C	−19		−38	µA
I_{IH}	Logic High-bias current	$\overline{PD}$ and COMP pins = 2.5 V, WSON-8 package(6)		−16	−22	−27	µA
			-40°C ≤ T_J ≤ +125°C	−14		−29	µA
T_{en}	Enable time	WSON-8 package			75		ns
T_{dis}	Disable time				80		ns
POWER REQUIREMENTS							
I_S	Supply current	No Load, Normal Operation ($\overline{PD}$ Pin = HI or open for WSON-8 package)			15.5	16.7	mA
			-40°C ≤ T_J ≤ +125°C			18.2	mA
		No Load, Shutdown ($\overline{PD}$ Pin =LO for WSON-8 package)			1.1	1.85	mA
			-40°C ≤ T_J ≤ +125°C			2.0	mA

6.6 Electrical Characteristics 3.3V

The following specifications apply for single supply with V_S = 3.3 V, R_L = 100 Ω terminated to 1.65 V, gain = 10V/V, V_O = 1 V_{PP}, V_{CM} = V_S/2, COMP Pin = HI (WSON-8 package), unless otherwise noted.(1)

PARAMETER		TEST CONDITIONS	T_A = 25°C			UNIT
			MIN(2)	TYP(3)	MAX(2)	
DYNAMIC PERFORMANCE						
SSBW	Small signal −3dB bandwidth	V_O = 200 mV_{PP}, WSON-8 package		820		MHz
		V_O = 200 mV_{PP}, SOT-23-5 package		950		
		COMP Pin = LO, A_V= 4, V_O = 200 mV_{PP}		730		
LSBW	Large signal −3dB bandwidth	V_O = 1V_{PP}		540		MHz
		COMP Pin = LO, A_V= 4, V_O = 1V_{PP}		320		
	0.1 dB Bandwidth	A_V= 10, V_O = 200 mV_{PP}, WSON-8 package		330		MHz
		A_V= 10, V_O = 200 mV_{PP}, SOT-23-5 package		190		
		COMP Pin = LO, A_V= 4, V_O = 200 mV_{PP}		85		
	Peaking	V_O = 200 mV_{PP}, WSON-8 package		0		dB
		V_O = 200 mV_{PP}, SOT-23-5 package		1.8		
SR	Slew rate	A_V= 10, 1.3V step		1100		V/µs
		COMP Pin = LO, A_V= 4, 1.3V step		500		
t_r/ t_f	Rise/fall time	A_V= 10, 1V step, 10% to 90%, WSON-8 package		0.7		ns
		A_V= 10, 1V step, 10% to 90%, SOT-23-5 package		0.55		
		A_V= 4, COMP Pin = LO, 1V step, 10% to 90% (Slew Rate Limited)		1.3		
T_s	Settling time	A_V= 10, 1V step, ±0.1%		70		
	Overload recovery	V_{IN} = 1V_{PP}		2		
NOISE and DISTORTION						
HD2	2nd Order distortion	fc = 1MHz, V_O = 1V_{PP}		-82		dBc
		COMP Pin = LO, A_V= 4, fc = 1MHz, V_O = 1V_{PP}		-88		
		fc = 10 MHz, V_O = 1V_{PP}		-67		
		COMP Pin = LO, fc = 10 MHz, A_V= 4V, V_O = 1V_{PP}		-74		
HD3	3rd Order distortion	fc = 1MHz, V_O = 1V_{PP}		-94		dBc
		COMP Pin = LO, A_V= 4, fc = 1MHz, V_O = 1V_{PP}		-112		
		fc = 10 MHz, V_O = 1V_{PP}		-79		
		COMP pin = LO, fc = 10 MHz, V_O = 1V_{PP}		-96		
OIP3	Two-tone 3rd order intercept point	fc = 25 MHz, V_O = 1V_{PP} composite		30		dBm
		fc = 75 MHz, V_O = 1V_{PP} composite		26		
e_n	Noise voltage	Input referred, f > 1MHz		0.69		nV/√Hz
i_n	Noise current			2.6		pA/√Hz
NF	Noise figure	R_S = R_T = 50 Ω		8.0		dB

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A.
(2) All limits are ensured by testing or statistical analysis.
(3) Typical numbers are the most likely parametric norm.

Electrical Characteristics 3.3V (continued)

The following specifications apply for single supply with V_S = 3.3 V, R_L = 100 Ω terminated to 1.65 V, gain = 10V/V, V_O = 1 V_{PP}, V_{CM} = V_S/2, COMP Pin = HI (WSON-8 package), unless otherwise noted.(1)

PARAMETER		TEST CONDITIONS		T_A = 25°C MIN(2)	T_A = 25°C TYP(3)	T_A = 25°C MAX(2)	UNIT
ANALOG I/O							
CMVR	Input voltage range	CMRR > 70 dB, WSON-8 package		-0.30		2.1	V
		CMRR > 70 dB, SOT-23-5 package			-0.30 to 2.1		
V_O	Output voltage range	R_L = 100 Ω to V_S/2		0.90	0.79 to 2.50	2.4	
			-40°C ≤ T_J ≤ +125°C	0.95		2.3	
		No load		0.76	0.70 to 2.60	2.5	
			-40°C ≤ T_J ≤ +125°C	0.80		2.4	
I_{OUT}	Linear output current	V_O = 1.65 V(4)			230		mA
V_{OS}	Input offset voltage				±150	±680	µV
		-40°C ≤ T_J ≤ +125°C				±700	
TcV_{OS}	Input offset voltage temperature drift	See (5)			±1		µV/°C
I_{BI}	Input bias current	See (6)			-15	-23	µA
			-40°C ≤ T_J ≤ +125°C			-35	
I_{OS}	Input offset current				±0.13	±1.8	
		-40°C ≤ T_J ≤ +125°C				±3.0	
T_CI_{OS}	Input offset voltage temperature drift	See (5)			±3.2		nA/°C
C_{CM}	Input capacitance	Common Mode			1.7		pF
C_{DIFF}		Differential Mode(7)			4		
R_{CM}	Input resistance	Common Mode			1		MΩ
MISCELLANEOUS PARAMETERS							
CMRR	Common mode rejection ratio	V_{CM} from 0 V to 2.0 V, WSON-8 package		84	87		dB
			-40°C ≤ T_J ≤ +125°C	81			
		V_{CM} from 0 V to 2.0 V, SOT-23-5 package			87		
PSRR	Power supply rejection ratio			82	84		
		-40°C ≤ T_J ≤ +125°C		79			
A_{VOL}	Open loop gain	WSON-8 package		78	79		
			-40°C ≤ T_J ≤ +125°C	73			
		SOT-23-5 package			79		

(4) The maximum continuous output current (I_{OUT}) is determined by device power dissipation limitations. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C
(5) Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.
(6) Negative input current implies current flowing out of the device.
(7) Simulation results.

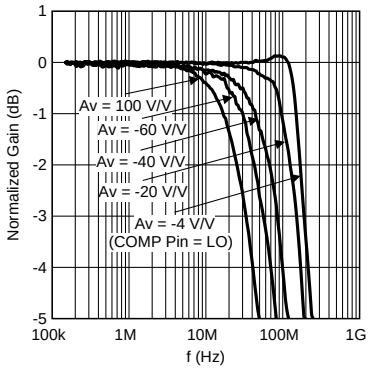
Electrical Characteristics 3.3V (continued)

The following specifications apply for single supply with V_S = 3.3 V, R_L = 100 Ω terminated to 1.65 V, gain = 10V/V, V_O = 1 V_{PP}, V_{CM} = V_S/2, COMP Pin = HI (WSON-8 package), unless otherwise noted.(1)

PARAMETER		TEST CONDITIONS		T_A = 25°C			UNIT
				MIN(2)	TYP(3)	MAX(2)	
DIGITAL INPUTS/TIMING							
V_{IL}	Logic low-voltage threshold	$\overline{PD}$ and COMP pins, WSON-8 package				0.8	V
V_{IH}	Logic high-voltage threshold			2.0			
I_{IL}	Logic low-bias current	$\overline{PD}$ and COMP pins = 0.8 V, WSON-8 package(6)		-17	-23	-28	µA
			-40°C ≤ T_J ≤ +125°C	-14		-32	
I_{IH}	Logic high-bias current	$\overline{PD}$ and COMP pins = 2.0 V, WSON-8 package(6)		-16	-22	-27	
			-40°C ≤ T_J ≤ +125°C	-13		-31	
T_{en}	Enable time	WSON-8 package			75		ns
T_{dis}	Disable time				80		
POWER REQUIREMENTS							
I_S	Supply current	No Load, Normal Operation ($\overline{PD}$ Pin = HI or open for WSON-8 package)			13.7	14.9	mA
			-40°C ≤ T_J ≤ +125°C			16.0	
		No Load, Shutdown ($\overline{PD}$ Pin = LO for WSON-8 package)			0.89	1.4	
			-40°C ≤ T_J ≤ +125°C			1.5	

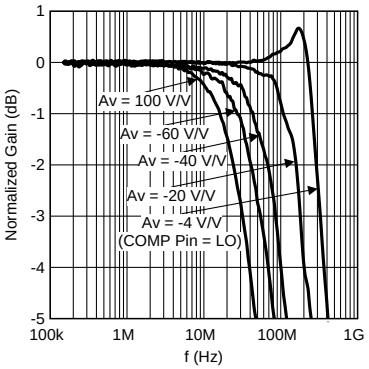
6.7 Typical Performance Characteristics

Unless otherwise specified, V_S = ±2.5V, R_f = 240 Ω, R_L = 100 Ω, V_O = 2 V_{PP}, COMP pin = HI, A_V = +10 V/V, WSON-8 and SOT-23-5 packages (unless specifically noted).



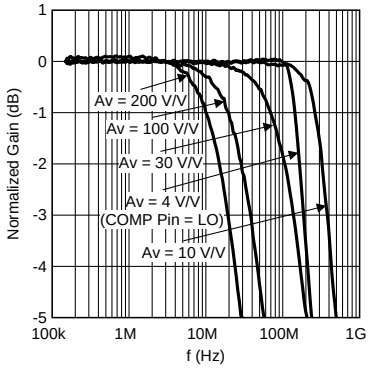
Vo = 2 Vpp

Figure 1. Inverting Frequency Response



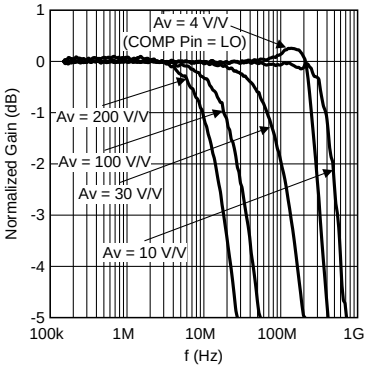
Vo = 1 Vpp Vs = ±1.5V

Figure 2. Inverting Frequency Response



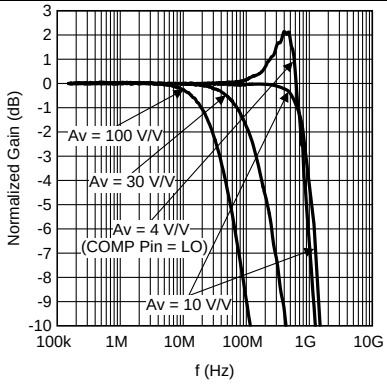
Vo = 2 Vpp

Figure 3. Non-Inverting Frequency Response



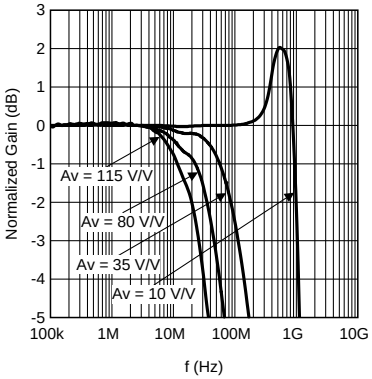
Vo = 1 Vpp Vs = ±1.5 V

Figure 4. Non-Inverting Frequency Response



Vo = 0.2 Vpp

Figure 5. Non-Inverting Frequency Response, WSON-8 Package

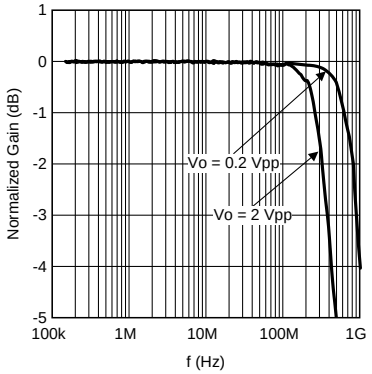


Vo = 0.2 Vpp

Figure 6. Non-Inverting Frequency Response, SOT-23-5 Package

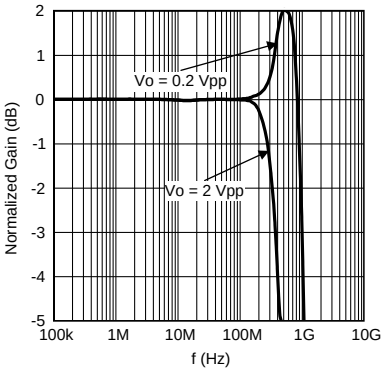
Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = ±2.5V, R_f = 240 Ω, R_L = 100 Ω, V_O = 2 V_{PP}, COMP pin = HI, A_V = +10 V/V, WSON-8 and SOT-23-5 packages (unless specifically noted).



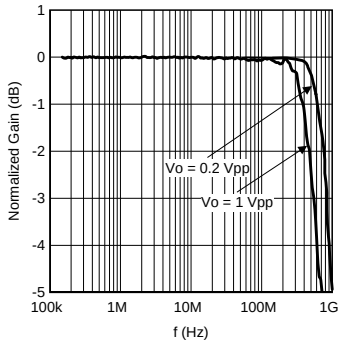
Av = 10 V/V

Figure 7. Non-Inverting Frequency Response with Varying V_O, WSON-8 Package



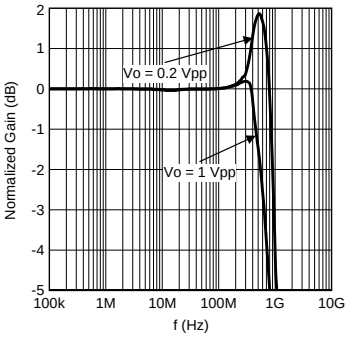
Av=10 V/V

Figure 8. Non-Inverting Frequency Response with Varying V_O, SOT-23-5 Package



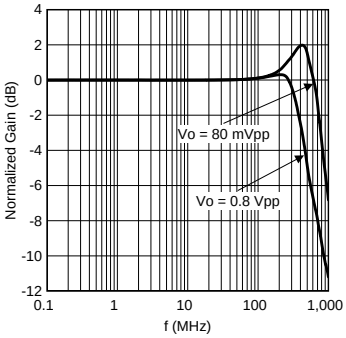
Av = 10 V/V Vs = +/-1.5 V

Figure 9. Non-Inverting Frequency Response with Varying V_O, WSON-8 Package



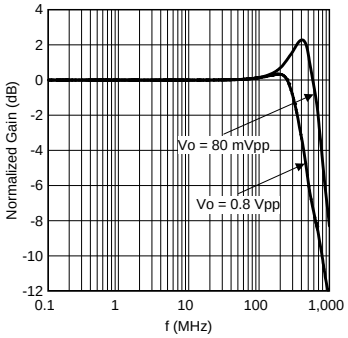
Av=10 V/V Vs= +/-1.5 V

Figure 10. Non-Inverting Frequency Response with Varying V_O, SOT-23-5 Package



Av = 4 V/V COMP Pin = LO

Figure 11. Non-Inverting Frequency Response with Varying V_O, WSON-8 Package

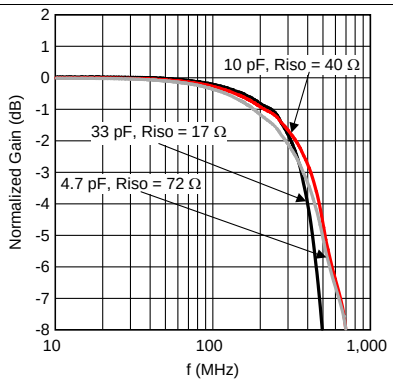


Av = 4 V/V Vs = ±1.5 V COMP Pin = LO

Figure 12. Non-Inverting Frequency Response with Varying V_O, WSON-8 Package

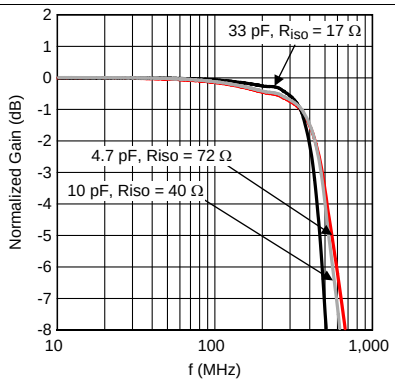
Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = ±2.5V, R_f = 240 Ω, R_L = 100 Ω, V_O = 2 V_{PP}, COMP pin = HI, A_V = +10 V/V, WSON-8 and SOT-23-5 packages (unless specifically noted).



R_L = 100 Ω || C_L
R_{ISO} as noted (measured @ C_L)

Figure 13. Frequency Response with Cap. Loading



R_L = 100 Ω || C_L, A_V = 4 V/V
COMP Pin = LO
R_{ISO} as noted (measured @ C_L)

Figure 14. Frequency Response Cap. Loading, WSON-8 Package

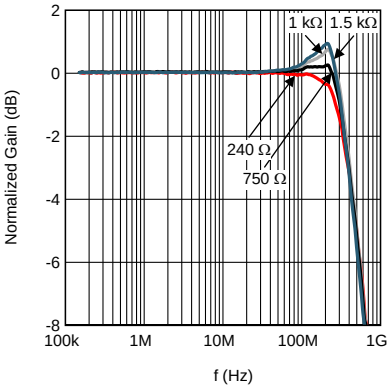


Figure 15. Frequency Response vs. R_f, WSON-8 Package

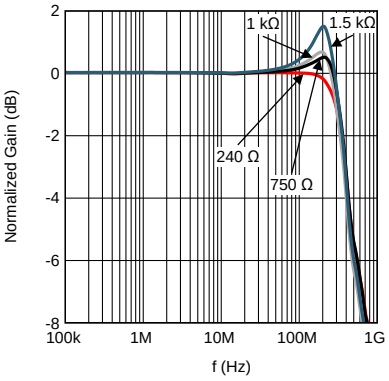
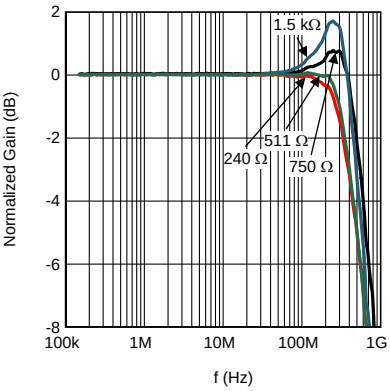
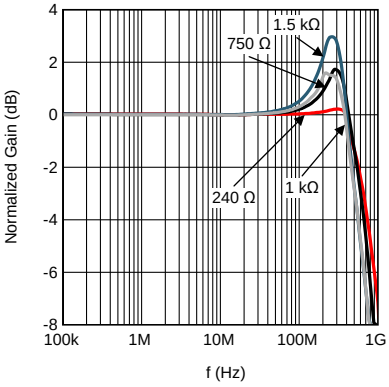


Figure 16. Frequency Response vs. R_f, SOT-23-5 Package



V_S = ±1.5 V V_O = 1 V_{PP}

Figure 17. Frequency Response vs. R_f, WSON-8 Package

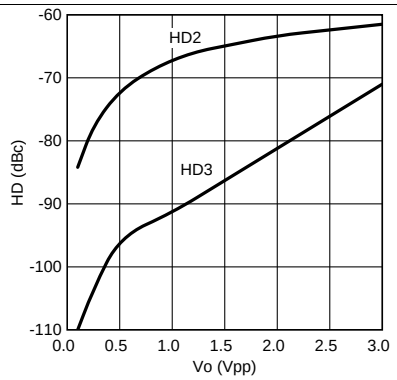


V_S = ± 1.5 V V_O = 1 V_{PP}

Figure 18. Frequency Response vs. R_f, SOT-23-5 Package

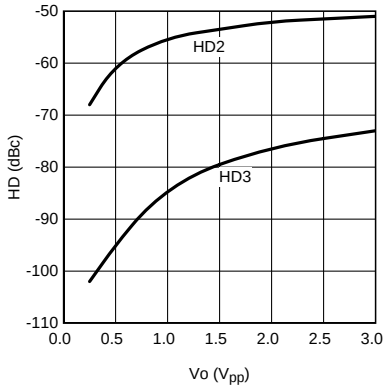
Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = ±2.5V, R_f = 240 Ω, R_L = 100 Ω, V_O = 2 V_{PP}, COMP pin = HI, A_V = +10 V/V, WSON-8 and SOT-23-5 packages (unless specifically noted).



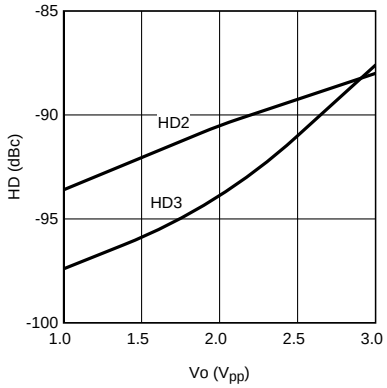
20 MHz

Figure 19. Distortion vs. Swing, WSON-8 Package



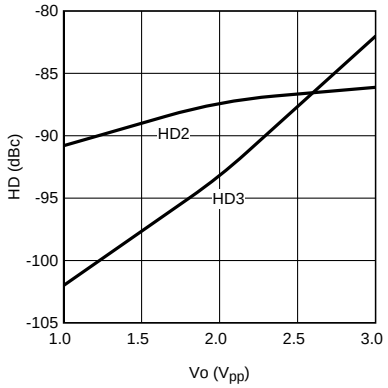
20 MHz

Figure 20. Distortion vs. Swing, SOT-23-5 Package



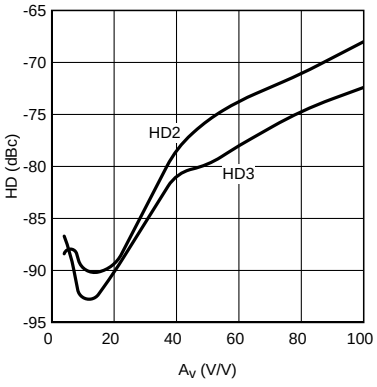
1 MHz

Figure 21. Distortion vs. Swing, WSON-8 Package



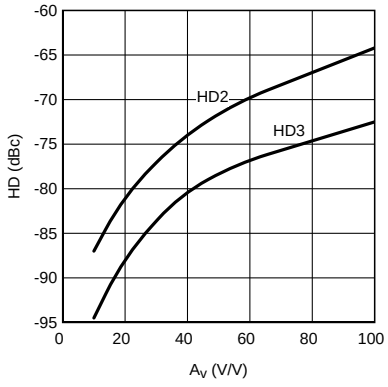
1 MHz

Figure 22. Distortion vs. Swing, SOT-23-5 Package



1 MHz Vout = 2 Vpp

Figure 23. Distortion vs. Gain, WSON-8 Package



1 MHz Vout = 2 Vpp

Figure 24. Distortion vs. Gain, SOT-23-5 Package

Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = ±2.5V, R_f = 240 Ω, R_L = 100 Ω, V_O = 2 V_{PP}, COMP pin = HI, A_V = +10 V/V, WSON-8 and SOT-23-5 packages (unless specifically noted).

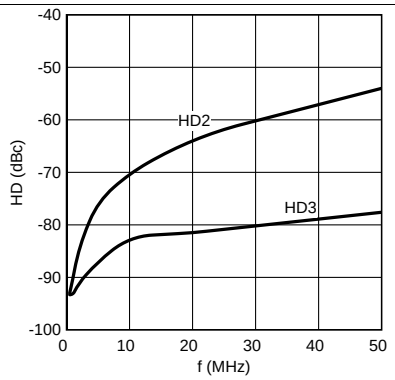


Figure 25. Distortion vs. Frequency, WSON-8 Package

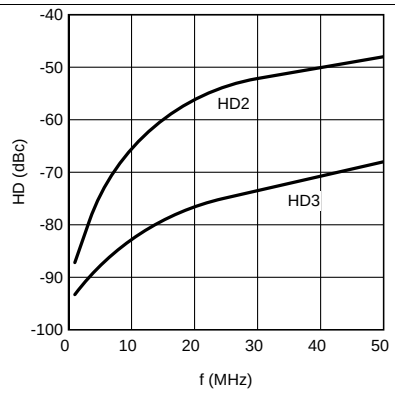


Figure 26. Distortion vs. Frequency, SOT-23-5 Package

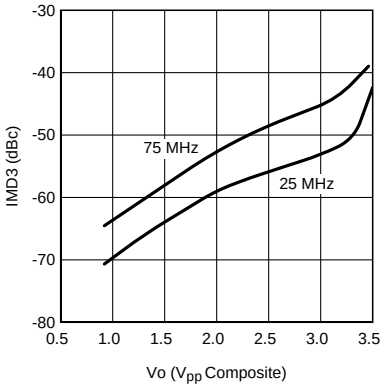


Figure 27. 3rd Order Intermodulation Distortion vs. Output Voltage

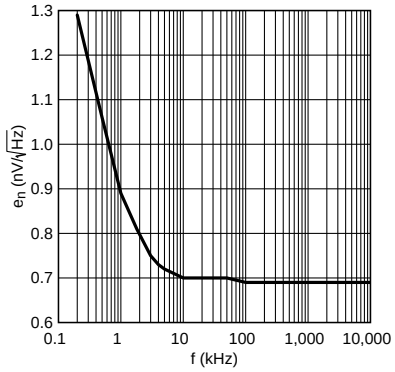


Figure 28. Input Noise Voltage vs. Frequency

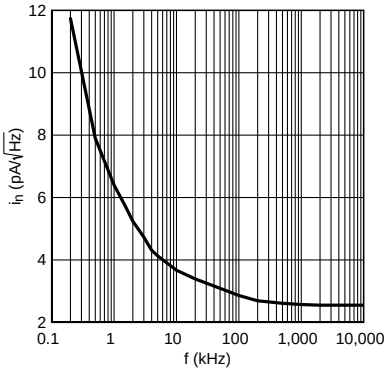


Figure 29. Input Noise Current vs. Frequency

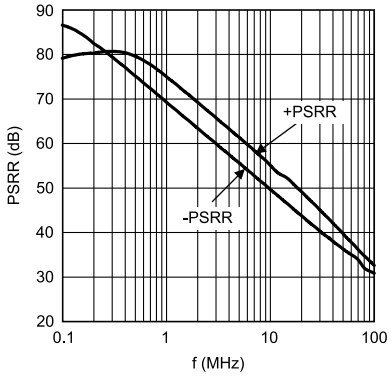


Figure 30. PSRR vs. Frequency

Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = ±2.5V, R_f = 240 Ω, R_L = 100 Ω, V_O = 2 V_{PP}, COMP pin = HI, A_V = +10 V/V, WSON-8 and SOT-23-5 packages (unless specifically noted).

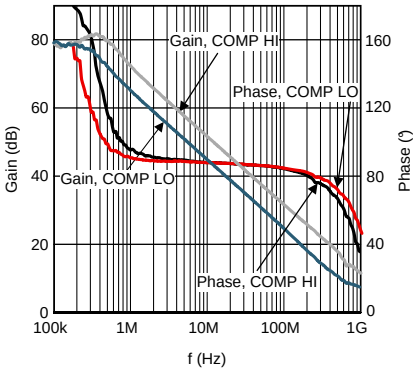


Figure 31. Open Loop Gain/Phase Response

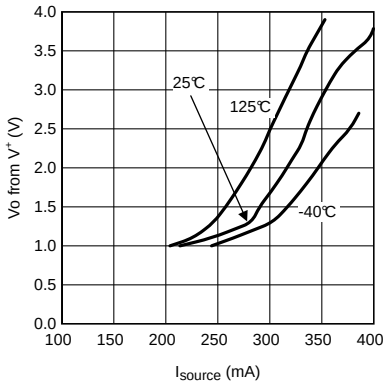


Figure 32. Output Source Current, WSON-8 Package

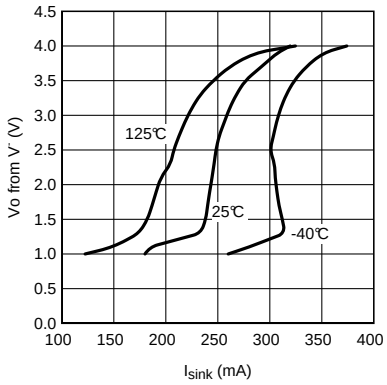


Figure 33. Output Sink Current WSON-8 Package

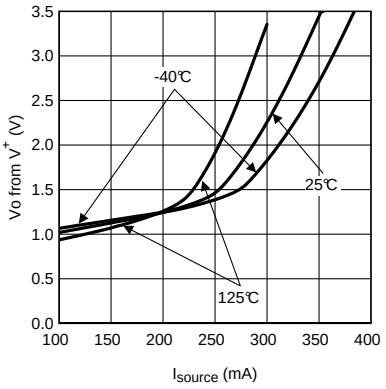


Figure 34. Output Source Current, SOT-23-5 Package

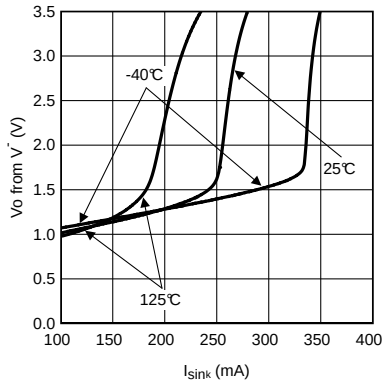


Figure 35. Output Sink Current, SOT-23-5 Package

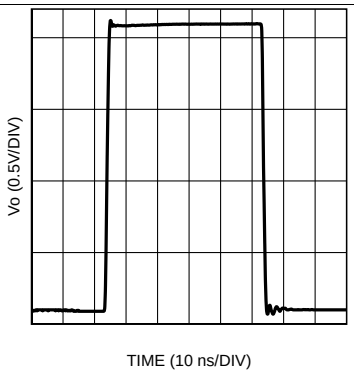
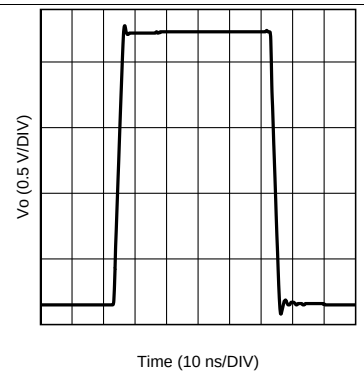


Figure 36. Large Signal Step Response

Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = ±2.5V, R_f = 240 Ω, R_L = 100 Ω, V_O = 2 V_{PP}, COMP pin = HI, A_V = +10 V/V, WSON-8 and SOT-23-5 packages (unless specifically noted).



A_V= 4V/V COMP Pin = LO

Figure 37. Large Signal Step Response

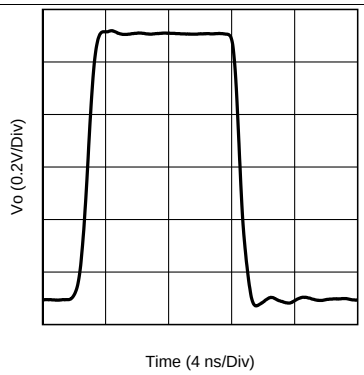
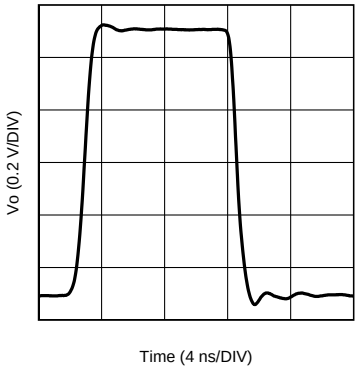


Figure 38. Large Signal Step Response



Vs = 3.3 V

Figure 39. Large Signal Step Response

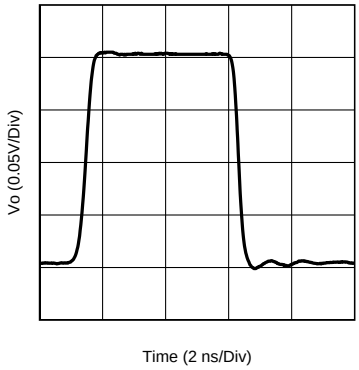
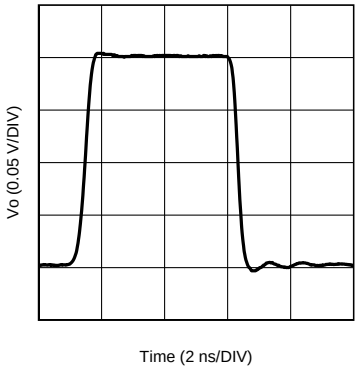


Figure 40. Small Signal Step Response, WSON-8 Package



Vs = 3.3 V

Figure 41. Small Signal Step Response, WSON-8 Package

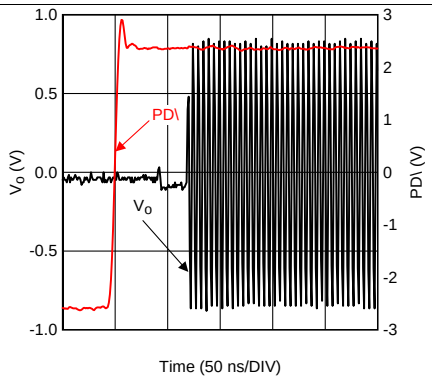


Figure 42. Turn-On Waveform, WSON-8 Package

Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = ±2.5V, R_f = 240 Ω, R_L = 100 Ω, V_O = 2 V_{PP}, COMP pin = HI, A_V = +10 V/V, WSON-8 and SOT-23-5 packages (unless specifically noted).

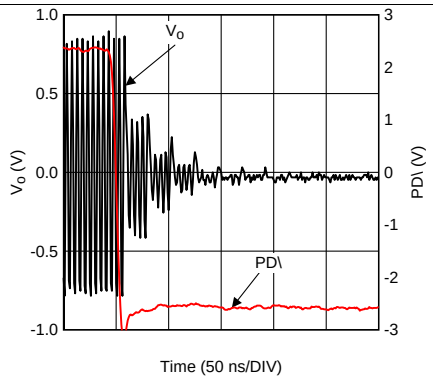


Figure 43. Turn-Off Waveform, WSON-8 Package

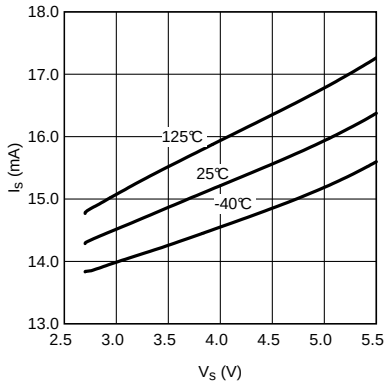


Figure 44. Supply Current vs. Supply Voltage

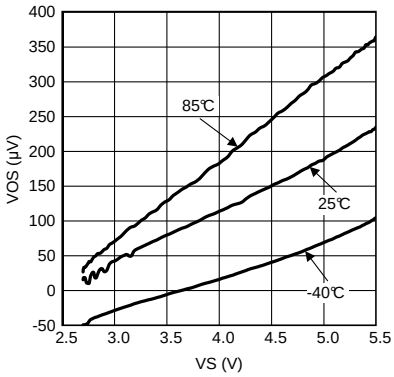


Figure 45. Offset Voltage vs. Supply Voltage (Typical Unit)

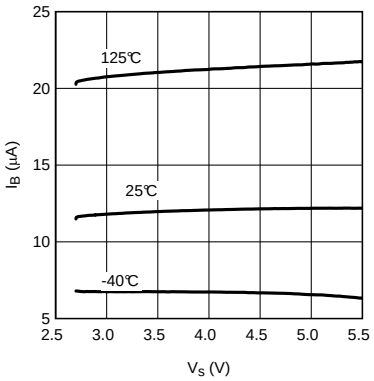


Figure 46. Input Bias Current vs. Supply Voltage (Typical Unit)

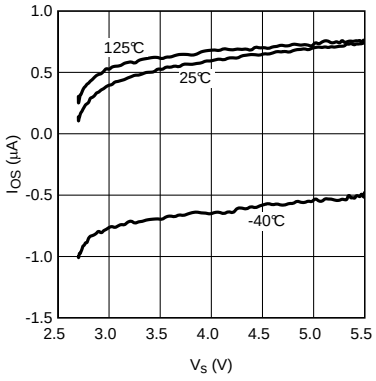


Figure 47. Input Offset Current vs. Supply Voltage (Typical Unit)

7 Detailed Description

7.1 Overview

The LMH6629 is a high gain bandwidth, ultra low-noise voltage feedback operational amplifier. The excellent noise and bandwidth enables applications such as medical diagnostic ultrasound, magnetic tape and disk storage and fiberoptics to achieve maximum high frequency signal-to-noise ratios. The following discussion will enable the proper selection of external components to achieve optimum system performance.

7.2 Functional Block Diagram

The LMH6629 (WSON-8 package only) has some additional features to allow maximum flexibility. As shown in Figure 48, there are provisions for low-power shutdown and two internal compensation settings, which are discussed in more detail in *Compensation*. Also provided is a feedback (FB) pin which allows the placement of the feedback resistor directly adjacent to the inverting input (IN-) pin. This pin simplifies printed circuit board layout and minimizes the possibility of unwanted interaction between the feedback path and other circuit elements.

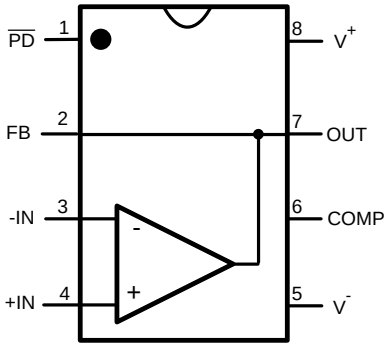


Figure 48. 8-Pin WSON Pinout Diagram

The WSON-8 package requires the bottom-side Die Attach Paddle (DAP) to be soldered to the circuit board for proper thermal dissipation and to get the thermal resistance number specified. The DAP is tied to the V^- potential within the LMH6629 package. Thus, the circuit board copper area devoted to DAP heatsinking connection should be at the V- potential as well. Please refer to the package drawing for the recommended land pattern and recommended DAP connection dimensions.

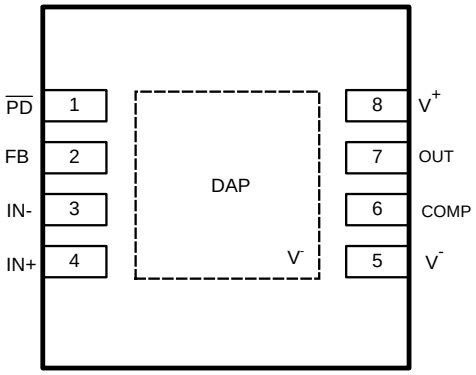


Figure 49. WSON–8 DAP(Top View)

7.3 Feature Description

7.3.1 WSON-8 Control Pins and SOT-23-5 Comparison

The LMH6629 WSON-8 package has two digital control pins; $\overline{PD}$ and COMP pins. The $\overline{PD}$ pin, used for power down, floats high (device on) when not driven. When the $\overline{PD}$ pin is pulled low, the amplifier is disabled and the amplifier output stage goes into a high impedance state so the feedback and gain set resistors determine the output impedance of the circuit. The other control pin, the COMP pin, allows control of the internal compensation and defaults to the lower gain mode or logic 0.

The SOT-23-5 package has the following differences relative to the WSON-8 package:

1. No power down (shutdown) capability.
2. No COMP pin to set the minimum stable gain. SOT-23–5 package minimum stable gain is internally fixed to be 10V/V.
3. No feedback (FB) pin.

From a performance point of view, the WSON-8 and the SOT-23-5 packages perform very similarly except in the following areas:

1. **SSBW, Peaking, and 0.1 dB Bandwidth:** These differences are highlighted in the *Typical Performance Characteristics* and the *Electrical Characteristics 5V* tables. Most notable differences are with small signal (0.2 Vpp) and close to the minimum stable gain of 10V/V.
2. **Distortion:** It is possible to get slightly different distortion performance. The board layout and decoupling capacitor return current routing strongly influence distortion performance.
3. **Output Current:** In heavy current applications, there will be differences between these package types because of the difference in their respective Thermal Resistances ($R_{\theta JA}$).

7.3.2 Compensation

The LMH6629 has two compensation settings that can be controlled by the COMP pin (WSON-8 package only). The default setting is set through an internal pulldown resistor and places the COMP pin at the logic 0 state. In this configuration the on-chip compensation is set to the maximum and bandwidth is reduced to enable stability at gains as low as 4V/V.

When this pin is driven to the logic 1 state, the internal compensation is decreased to allow higher bandwidth at higher gains. In this state, the minimum stable gain is 10V/V. Due to the reduced compensation, slew rate and large signal bandwidth are significantly enhanced for the higher gains.

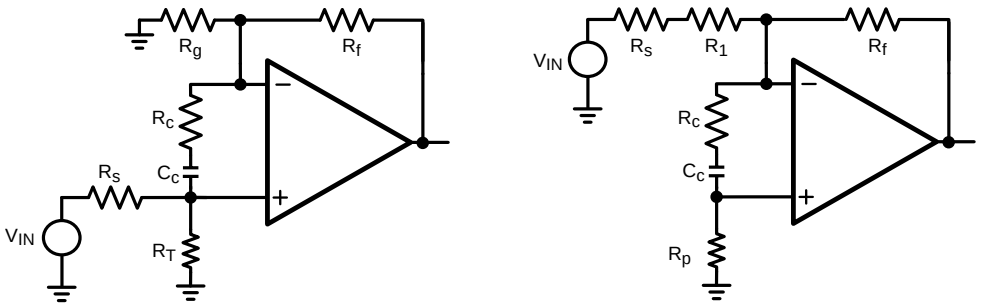
NOTE

As mentioned earlier, the SOT-23-5 package does not offer the two compensation settings that the WSON-8 offers. The SOT-23-5 is internally set for a minimum gain of 10 V/V.

It is possible to externally compensate the LMH6629 for any of the following reasons, as shown in Figure 50.

- To operate the SOT-23-5 package (which does not offer the COMP pin) at closed loop gains < 10V/V.
- To operate the WSON-8 package at gains below the minimum stable gain of 4V /V when the COMP pin is LO. **NOTE**: In this case, Figure 50 “Constraint 1” may be changed to ≥ 4 V/V instead of ≥ 10 V/V.
- To operate either package at low gain and need maximum slew rate (COMP pin HI).

Feature Description (continued)



a) Non-inverting

$R_p = R_s \| R_T$

COMP pin = HI

$R_{EQ} = R_f \| R_g$

b) Inverting

$R_g = R_s + R_1$

$$\text{Constraint 1:}\quad \left(1+\frac{R_f}{R_g}\right)\left(1+\frac{R_p+R_{EQ}}{R_c}\right) \geq 10\ \text{V/V}$$

$$\text{Costraint 2:}\quad \frac{1}{2\pi C_c R_c} \leq 90\ \text{MHz}$$

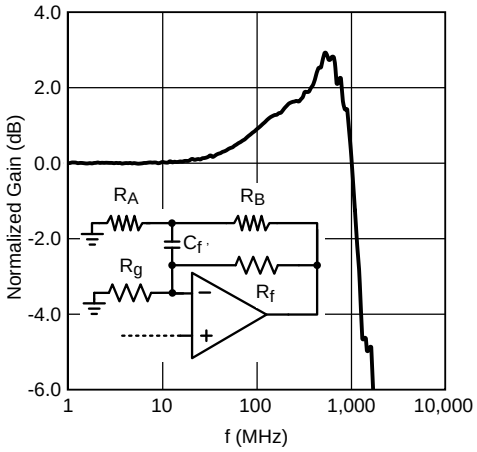
Figure 50. External Compensation

This circuit operates by increasing the Noise Gain (NG) beyond the minimum stable gain of the LMH6629 while maintaining a positive loop gain phase angle at 0 dB. There are two constraints shown in Figure 50: “Constraint 1” ensures that NG has increased to at least 10 V/V when the loop gain approaches 0dB, and “Constraint 2” places an upper limit on the feedback phase lead network frequency to make sure it is fully effective in the frequency range when loop gain approaches 0dB. These two constraints allow one to estimate the “starting value” for R_c and C_c which may need to be fine tuned for proper response.

Here is an example worked out for more clarification:

- Assume that the objective is to use the SOT-23-5 version of the LMH6629 for a closed loop gain of +3.7 V/V using the technique shown in Figure 50.
- Selecting R_f = 249 Ω → R_g = 91 Ω → R_{EQ}= 66.6 Ω.
- For 50-Ω source termination (R_s= 50 Ω), select R_T= 50 Ω → R_p = 25 Ω.
- Using “Constraint 1” (= 10V/V) allows one to compute Rc ≅ 56 Ω. Using “Constraint 2” (= 90 MHz) defines the appropriate value of C_c ≅ 33 pF.
- The frequency response plot shown in Figure 51 is the measured response with R_c and C_c values computed above and shows a -3 dB response of about 1 GHz.

Feature Description (continued)



C_f = 1.5 pF

R_A = 33 Ω

R_B = 91 Ω

Figure 51. SOT-23-5 Package Low Closed Loop Gain Operation with External Compensation

For the Figure 51 measured results, a compensation capacitor (C_f) was used across R_f to compensate for the summing node net capacitance due to the board and the SOT-23–5 LMH6629. The R_A and R_B combination reduces the effective capacitance of Cf‘ by the ratio of 1+R_B / R_A, with the constraint that R_B << R_f, thereby allowing a practical capacitance value (> 1pF) to be used. The WSON-8 package does not need this compensation across R_f due to its lower parasitics.

With the COMP pin HI (WSON-8 package only) or with the SOT-23–5 package, this circuit achieves high slew rate and takes advantage of the LMH6629's superior low-noise characteristics without sacrificing stability, while enabling lower gain applications. It should be noted that the R_c, C_c combination *does* lower the input impedance and increases noise gain at higher frequencies. With these values, the input impedance reduces by 3 dB at 490 MHz. The Noise Gain transfer function "zero" is given by Equation 1 and it has a 3-dB increase at 32.8 MHz with these values:

External Compensation Noise Gain Increase:

$$\text{Noise Gain "zero"} \cong \frac{1}{2\pi(R_C + R_p + R_{EQ})C_C} \quad (1)$$

Feature Description (continued)

7.3.3 Cancellation of Offset Errors Due to Input Bias Currents

The LMH6629 offers exceptional offset voltage accuracy. In order to preserve the low offset voltage errors, care must be taken to avoid voltage errors due to input bias currents. This is important in both inverting and non-inverting applications.

The non-inverting circuit is used here as an example. To cancel the bias current errors of the non-inverting configuration, the parallel combination of the gain setting (R_g) and feedback (R_f) resistors should equal the equivalent source resistance (R_{seq}) as defined in Figure 52. Combining this constraint with the non-inverting gain equation also seen in Figure 52 allows both R_f and R_g to be determined explicitly from Equation 2:

$$R_f = A_V R_{seq} \text{ and } R_g = R_f/(A_V-1) \quad (2)$$

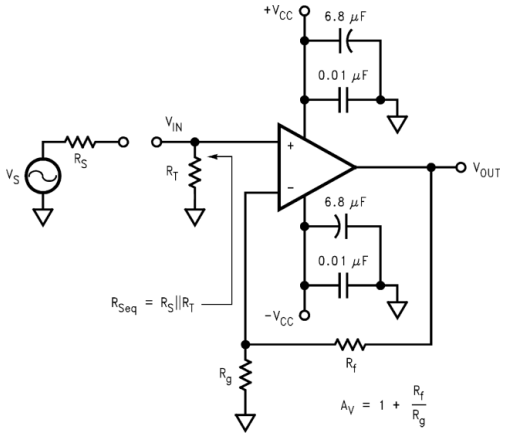


Figure 52. Non-Inverting Amplifier Configuration

When driven from a 0-Ω source, such as the output of an op amp, the non-inverting input of the LMH6629 should be isolated with at least a 25-Ω series resistor.

As seen in Figure 53, bias current cancellation is accomplished for the inverting configuration by placing a resistor (R_b) on the non-inverting input equal in value to the resistance seen by the inverting input (R_f || (R_g+R_s)). R_b should to be no less than 25 Ω for optimum LMH6629 performance. A shunt capacitor (not shown) can minimize the additional noise of R_b.

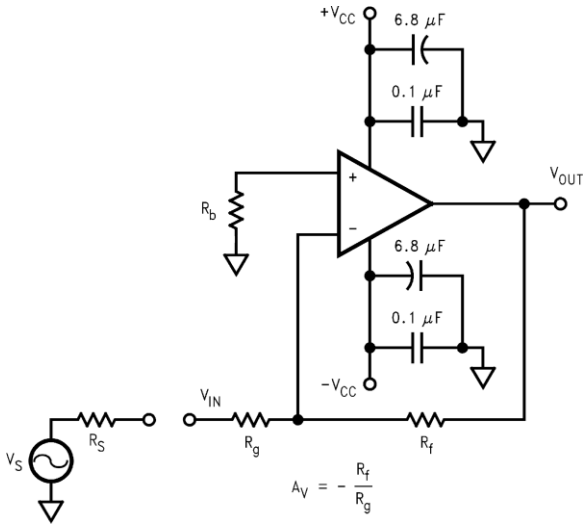


Figure 53. Inverting Amplifier Configuration

Feature Description (continued)

7.3.4 Total Input Noise vs. Source Resistance

To determine maximum signal-to-noise ratios from the LMH6629, an understanding of the interaction between the amplifier's intrinsic noise sources and the noise arising from its external resistors is necessary. Figure 54 describes the noise model for the non-inverting amplifier configuration showing all noise sources. In addition to the intrinsic input voltage noise (e_n) and current noise ($i_n = i_n^+ = i_n^-$) source, there is also thermal voltage noise ($e_t = \sqrt{(4KTR)}$) associated with each of the external resistors.

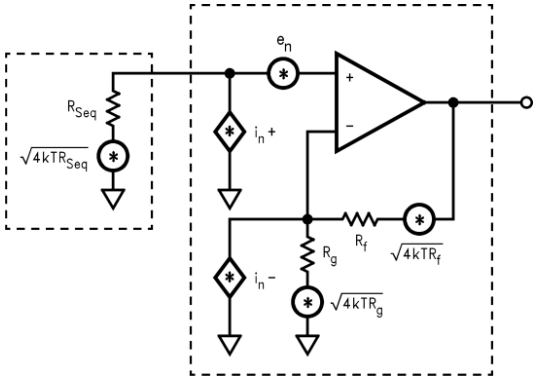


Figure 54. Non-Inverting Amplifier Noise Model

Equation 3 provides the general form for total equivalent input voltage noise density (e_{ni}).

General Noise Equation:

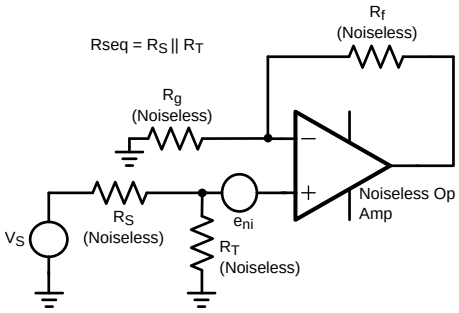
$$e_{ni} = \sqrt{e_n^2 + \left(i_{n+} R_{Seq}\right)^2 + 4kTR_{Seq} + \left(i_{n-}\left(R_f \| R_g\right)\right)^2 + 4kT\left(R_f \| R_g\right)} \quad (3)$$

Equation 4 is a simplification of Equation 3 that assumes $R_f \| R_g = R_{seq}$ for bias current cancellation:

$$e_{ni} = \sqrt{e_n^2 + 2(i_n R_{Seq})^2 + 4kT(2R_{Seq})}$$

Equation 4: Noise Equation with $R_f \| R_g = R_{seq}$ (4)

Figure 55 schematically shows e_{ni} alongside V_{IN} (the portion of V_S source which reaches the non-inverting input of Figure 52) and external components affecting gain ($A_v = 1 + R_f / R_g$), all connected to an ideal noiseless amplifier.



Set $R_{Seq} = R_f \| R_g$ for bias current offset cancellation

Figure 55. Non-Inverting Amplifier Equivalent Noise Source Schematic

Feature Description (continued)

Figure 56 illustrates the equivalent noise model using this assumption. Figure 57 is a plot of e_{ni} against equivalent source resistance (R_{seq}) with all of the contributing voltage noise source of Equation 4. This plot gives the expected e_{ni} for a given (R_{seq}) which assumes $R_f||R_g = R_{seq}$ for bias current cancellation. The total equivalent output voltage noise (e_{no}) is $e_{ni}*A_V$.

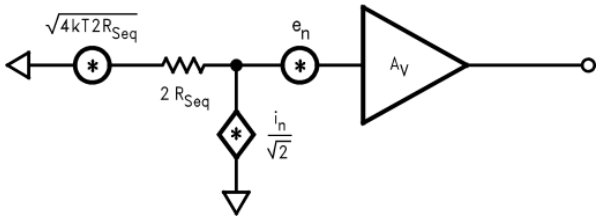
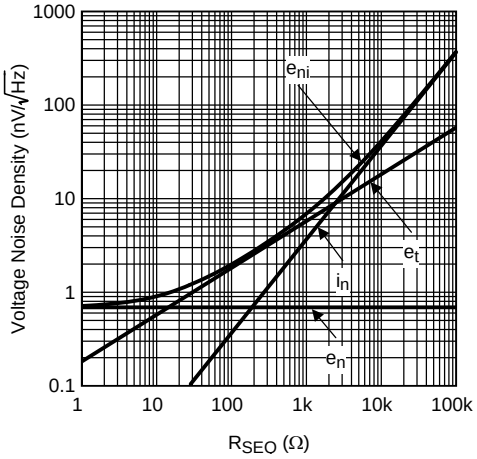


Figure 56. Noise Model with $R_f||R_g = R_{seq}$

As seen in Figure 57, e_{ni} is dominated by the intrinsic voltage noise (e_n) of the amplifier for equivalent source resistances below 15 Ω. Between 15 Ω and 2.5 kΩ, e_{ni} is dominated by the thermal noise ($e_t = \sqrt{(4kT(2R_{seq}))}$ of the equivalent source resistance R_{seq}. Incidentally, this is the range of R_{seq} values where the LMH6629 has the best (lowest) Noise Figure (NF) for the case where $R_{seq} = R_f \,||\, R_g$.

Above 2.5 kΩ, e_{ni} is dominated by the amplifier's current noise ($i_n = \sqrt{2} * i_n R_{seq}$). When R_{seq} = 190 Ω (that is, $R_{seq} = e_n/\sqrt{2} * i_n$), the contribution from voltage noise and current noise of LMH6629 is equal. For example, configured with a gain of +10V/V giving a −3dB of 825 MHz and driven from $R_{seq} = R_f \,||\, R_g$ = 20 Ω (e_{ni} = 1.07 nV√Hz from Figure 57), the LMH6629 produces a total equivalent output noise voltage (e_{ni} * 10 V/V * √(1.57 * 825 MHz)) of 385 μV_{rms}.



$R_{SEQ} = R_F \,||\, R_G$

Figure 57. Voltage Noise Density vs. Source Resistance

Feature Description (continued)

If bias current cancellation is not a requirement, then R_f || R_g does not need to equal R_{seq}. In this case, according to Equation 3, R_f || R_g should be as low as possible to minimize noise. Results similar to Equation 3 are obtained for the inverting configuration of Figure 53 if R_{seq} is replaced by R_b and R_g is replaced by R_g + R_s. With these substitutions, Equation 3 will yield an e_{ni} referred to the non-inverting input. Referring e_{ni} to the inverting input is easily accomplished by multiplying e_{ni} by the ratio of non-inverting to inverting gains ($1+R_g/ R_f$).

7.3.5 Noise Figure

Noise Figure (NF) is a measure of the noise degradation caused by an amplifier.

General Noise Figure Equation:

$$NF = 10LOG\left\{\frac{S_i / N_i}{S_o / N_o}\right\} = 10LOG\left\{\frac{e_{ni}^2}{e_t^2}\right\} \quad (5)$$

Looking at the two parts of the NF expression (inside the log function) yields:

- $S_i/ S_o \rightarrow$ Inverse of the power gain provided by the amplifier
- $N_o/ N_i \rightarrow$ Total output noise power, including the contribution of R_S, divided by the noise power at the input due to R_S
- To simplify this, consider N_a as the noise power added by the amplifier (reflected to its input port):
- $S_i/ S_o \rightarrow 1/ G$
- $N_o/ N_i \rightarrow G * (N_i+N_a) / N_i$ (where $G*(N_i +N_a) = N_o$)

Substituting these two expressions into the NF expression:

$$NF = 10 \log\left[\frac{1}{G}\left(\frac{G(N_i + N_a)}{N_i}\right)\right] = 10 \log\left(1 + \frac{N_a}{N_i}\right) \quad (6)$$

The noise figure expression has simplified to depend only on the ratio of the noise power added by the amplifier at its input (considering the source resistor to be in place but noiseless in getting N_a) to the noise power delivered by the source resistor (considering all amplifier elements to be in place but noiseless in getting N_i).

For a given amplifier with a desired closed loop gain, to minimize noise figure:

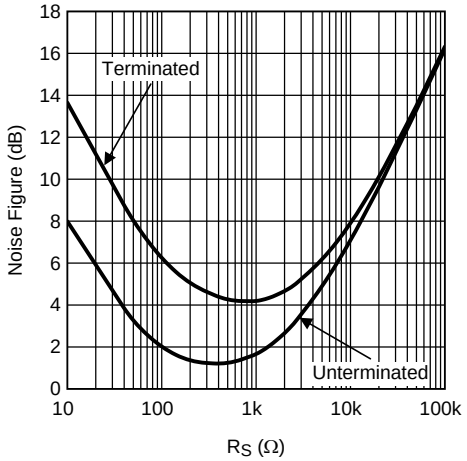
- Minimize R_f || R_g
- Choose the Optimum R_S (R_{OPT})

R_{OPT} is the point at which the NF curve reaches a minimum and is approximated by:

$$R_{OPT} \approx e_n/ i_n \quad (7)$$

Feature Description (continued)

Figure 58 is a plot of NF vs R_S with the circuit of Figure 52 (R_f = 240 Ω, A_V = +10V/V). The NF curves for both Unterminated (R_T = open) and Terminated systems (R_T = R_S) are shown. Table 1 indicates NF for various source resistances including R_S = R_{OPT}.



f > 1 MHz

Figure 58. Noise Figure vs. Source Resistance

Table 1. Noise Figure for Various R_s

R_S (Ω)	NF (TERMINATED) (dB)	NF (UNTERMINATED) (dB)
50	8	3.2
R_{OPT}	4.1 (R_{OPT} = 750 Ω)	1.1 (R_{OPT} = 350 Ω)

7.3.6 Single-Supply Operation

The LMH6629 can be operated with single power supply as shown in Figure 59. Both the input and output are capacitively coupled to set the DC operating point.

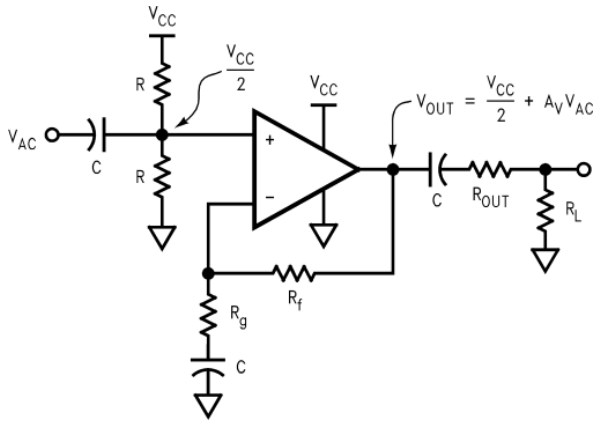


Figure 59. Single-Supply Operation

7.3.7 Low-Noise Transimpedance Amplifier

Figure 60 implements a high-speed, single-supply, low-noise Transimpedance amplifier commonly used with photo-diodes. The transimpedance gain is set by R_F.

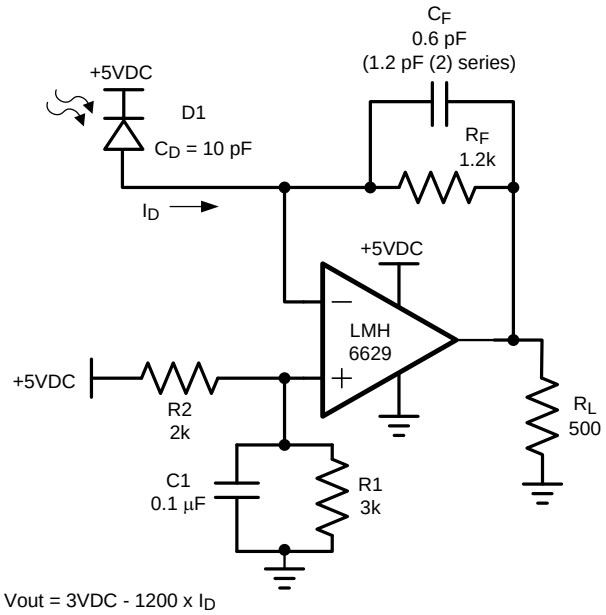


Figure 60. 200 MHz Transimpedance Amplifier Configuration

Figure 61 shows the Noise Gain (NG) and transfer function (I-V Gain). As with most Transimpedance amplifiers, it is required to compensate for the additional phase lag (Noise Gain zero at f_Z) created by the total input capacitance (C_D (diode capacitance) + C_{CM} (LMH6629 CM input capacitance) + C_{DIFF} (LMH6629 DIFF input capacitance)) looking into R_F. This is accomplished by placing C_F across R_F to create enough phase lead (Noise Gain pole at f_P) to stabilize the loop.

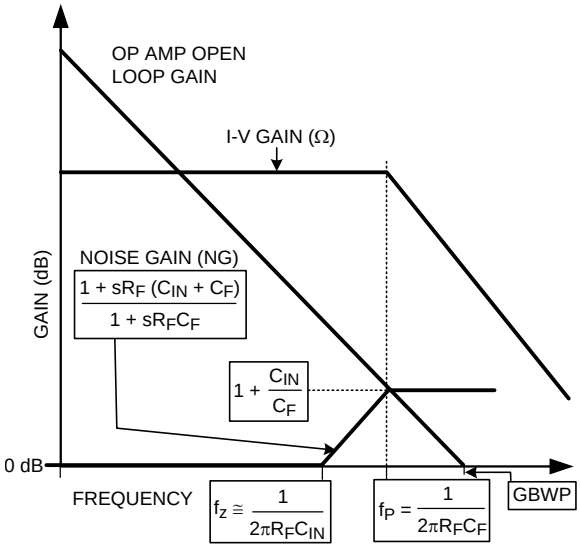


Figure 61. Transimpedance Amplifier Noise Gain and Transfer Function

The optimum value of C_F is given by Equation 8 resulting in the I-V -3dB bandwidth shown in Equation 9, or around 200 MHz in this case (assuming GBWP= 4GHz with COMP pin = HI for WSON-8 package). This C_F value is a "starting point" and C_F needs to be tuned for the particular application as it is often less than 1 pF and thus is easily affected by board parasitics. For maximum speed, the LMH6629 COMP pin should be HI (or use the SOT-23 package).

Optimum C_F Value:

$$C_F = \sqrt{\frac{C_{IN}}{2\pi(GBWP)R_F}} \tag{8}$$

Resulting -3dB Bandwidth

$$f_{-3\,dB} \cong \sqrt{\frac{GBWP}{2\pi R_F C_{IN}}} \tag{9}$$

Equation 10 provides the total input current noise density (i_{ni}) equation for the basic Transimpedance configuration and is plotted against feedback resistance (R_F) showing all contributing noise sources in Figure 62. The plot indicates the expected total equivalent input current noise density (i_{ni}) for a given feedback resistance (R_F). This is depicted in the schematic of Figure 63 where total equivalent current noise density (i_{ni}) is shown at the input of a noiseless amplifier and noiseless feedback resistor (R_F). The total equivalent output voltage noise density (e_{no}) is $i_{ni}*R_F$.

Noise Equation for Transimpedance Amplifier:

$$i_{ni} = \sqrt{i_n^2 + \left(\frac{e_n}{R_f}\right)^2 + \frac{4kT}{R_f}} \tag{10}$$

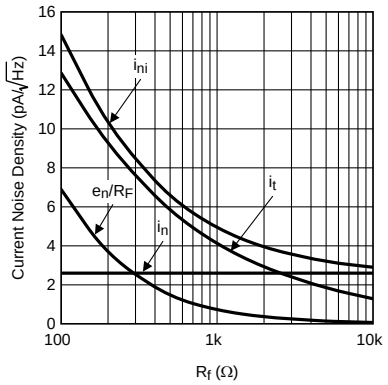


Figure 62. Current Noise Density vs. Feedback Resistance

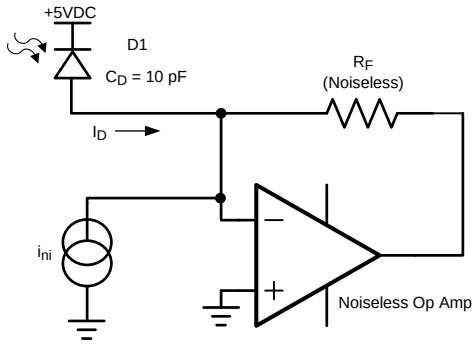


Figure 63. Transimpedance Amplifier Equivalent Input Source Model

From Figure 62, it is clear that with LMH6629's extremely low-noise characteristics, for R_F < 2.5 kΩ, the noise performance is entirely dominated by R_F thermal noise. Only above this R_F threshold, LMH6629's input noise current (i_n) starts being a factor and at no R_F setting does the LMH6629 input noise voltage play a significant role. This noise analysis has ignored the possible noise gain increase, due to photo-diode capacitance, at higher frequencies.

7.3.8 Low-Noise Integrator

Figure 64 shows a deBoo integrator implemented with the LMH6629. Positive feedback maintains integration linearity. The LMH6629's low input offset voltage and matched inputs allow bias current cancellation and provide for very precise integration. Keeping R_G and R_S low helps maintain dynamic stability.

$$V_O \cong V_{IN} \frac{K_O}{sR_SC} \quad ; \quad K_O = 1 + \frac{R_F}{R_G}$$

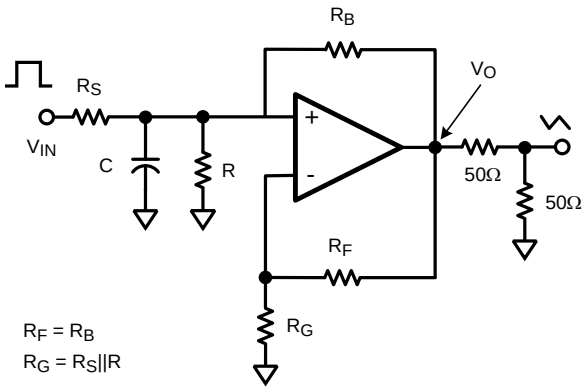
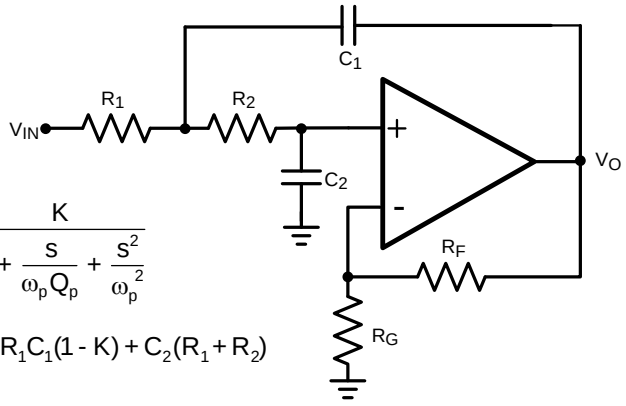


Figure 64. Low-Noise Integrator

7.3.9 High-Gain Sallen-Key Active Filters

The LMH6629 is well suited for high-gain Sallen-Key type of active filters. Figure 65 shows the 2nd order Sallen-Key low-pass filter topology. Using component predistortion methods discussed in OA-21, *Component Pre-Distortion for Sallen Key Filters* (SNOA369), enables the proper selection of components for these high-frequency filters.



$$\frac{V_o}{V_{IN}} \cong \frac{K}{1 + \frac{s}{\omega_p Q_p} + \frac{s^2}{\omega_p^2}}$$

$$\frac{1}{\omega_p Q_p} = R_1C_1(1 - K) + C_2(R_1 + R_2)$$

$$\frac{1}{\omega_p^2} = R_1R_2C_1C_2$$

Figure 65. Low Pass Sallen-Key Active Filter Topology

7.4 Device Functional Modes

With an industry-leading low noise voltage operating off a supply voltage as low as 2.7-V and a common mode input voltage range that extends 0.3 V below V−, the LMH6629 finds applications in single supply, high bandwidth, ultra-low noise applications. With a GBWP of 4GHz, the LMH6629 can operate at large gains and deliver exceptional speed and low noise. Choose the WSON(8) package for the ultimate flexibility (including Power Down and COMP pin which allows tailoring internal compensation to the operating gain conditions), or the SOT23-5 package if Power Down is not needed and closed loop gain is ≥ 20dB.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

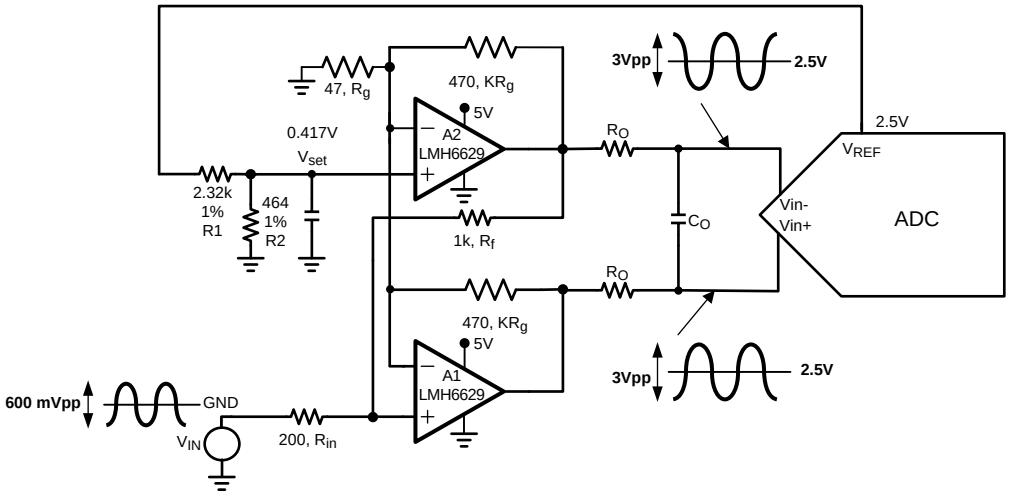
The following discussion details some of the applications that can benefit from the LMH6629's ultra-low noise, wide bandwidth, and single supply capability.

Note that It is essential to use a low-noise / low-distortion device to drive a high resolution ADC. This will minimize the impact on the quantization noise and to make sure that the driver's distortion does not dominate the acquired data.

Equation 11 demonstrates the converter noise expression and Equation 12 shows the converter noise expression evaluated for the example depicted in Figure 66. Figure 67 shows a high-performance low-noise equalizer for such applications as magnetic tape channels using the LMH6629. Figure 68 shows the circuit's simulated frequency response.

8.2 Typical Application

Many high-resolution data converters (ADC's) require a differential input driver. In order to preserve the ADC's dynamic range, the analog input driver must have a noise floor which is lower than the ADC's noise floor. Figure 66 shows a ground referenced bipolar input (symmetrical swing around 0V) SE to differential converter used to drive a high resolution ADC. The combination of LMH6629's low noise and the converter architecture reduces the impact on the ADC noise.



Governing Expressions:

$$K = \frac{V_{o\_diff}}{V_{in}}$$

$$R_{in} = \frac{2R_f}{K}$$

$$V_{set} = \frac{2V_{o\_CM}}{K+2}$$

Example:

$V_{o\_CM} = 2.5V$; $K = 10$, Let $R_f = 1k\Omega \rightarrow Rin = 200\Omega$

$V_{o\_diff} = 6Vpp$; $V_{set} = \frac{2 \times 2.5V}{10+2} = 0.417V$

$V_{in} = 600\,mVpp$

Figure 66. Low-Noise Single-Ended (SE) to Differential Converter

Typical Application (continued)

8.2.1 Design Requirements

For an ADC with N bits, the quantization Signal-to-noise ratio (SNR) is 6.02* N + 1.76 in dB. For example, a 12-bit ADC has a SNR of 74 dB (= 5000 V/V). Assuming a full-scale differential input of 2Vpp (0.707 V_RMS), the quantization oise referred to the ADC's input is ~140 µV_RMS (= 0.707 V_RMS / 5000 V/V) over the bandwidth "visible" to the ADC. Assuming an ADC input bandwidth of 20 MHz, this translates to just 25 nV/RtHz (= 141 µV_RMS / SQRT(20 MHz * π/2)) noise density at the output of the driver. Using an amplifier to form the single-ended (SE) to Differential converter / driver for such an application is challenging, especially when there is some gain required. In addition, the input driver's linearity (harmonic distortion) must also be high enough such that the spurs that get through to the ADC input are below the ADC's LSB threshold or -73 dBc (= 20*log (1/ 2^{12})) or lower in this case. Therefore, it is essential to use a low-noise / low-distortion device to drive a high resolution ADC in order to minimize the impact on the quantization noise and to make sure that the driver's distortion does not dominate the acquired data.

8.2.2 Detailed Design Procedure

In the circuit depicted in Figure 66, the required gain dictates the resistor ratio "K". With "K" and the driver output CM voltage (V_{O_CM}) known, V_{SET} can be established. Reasonable values for R_f and R_g can be set to complete the design.

In terms of output swing, with the LMH6629 output swing capability which requires ~0.85 V of headroom from either rail, the maximum total output swing into the ADC is limited to 6.6 V_{PP} (=(5 – 2 x 0.85V) x 2); that is true with V_{O_CM} set to mid-rail between V^+ and V^-. It should also be noted that the LMH6629's input CMVR range includes the lower rail (V^-) and that is the reason there is great flexibility in setting V_{o_CM} by controlling V_{SET}. Another feature is that A1 and A2 inputs act like "virtual grounds" and thus do not see any signal swing. Note that due to the converter's biasing, the source, V_{IN}, needs to sink a current equal to V_{SET} / R_{IN}.

The converter example shown in Figure 66 operates with a noise gain of 6 (=1+ K / 2) and thus requires that the COMP pin to be tied low (WSON-8 package only). The 1st order approximated small signal bandwidth will be 280 MHz (=1.7 GHz / 6 V/V) which is computed using 1.7 GHz as the GBWP with COMP pin LO.

From a noise point of view, concentrating only on the dominant noise sources involved, here is the expression for the expected differential noise density at the input of the ADC.

Converter Noise Expression:

$$V_{noise} \cong \sqrt{\left[e_n(1+K/2)\right]^2.2^3+\left[(e_{Rin\_thermal})K/2)\right]^2.2^2+\left[(e_{Rg\_thermal})K)\right]^2} \tag{11}$$

e_n is the LMH6629 input noise voltage and $e_{Rin\_thermal}$ is the thermal noise of R_{IN}. The "2^3" and the "2^2" multipliers account for the different instances of each noise source (2 for e_n, and 1 for $e_{Rin\_thermal}$).

Equation 11, evaluated for the circuit example of Figure 66, is shown in Equation 12:

$$V_{noise} \cong \sqrt{\left[0.69\,nV/RtHz\ x\,6\right]^2.2^3+\left[1.82\,nV/RtHz\ x\,5\right]^2.2^2+\left[0.88\,nV/RtHz\ x\,10\right]^2} = 23.4\,nV/RtHz \tag{12}$$

Because of the LMH6629's low input noise voltage (e_n), noise is dominated by the thermal noise of R_{IN}. It is evident that the input resistor, R_{IN}, can be reduced to lower the noise with lower input impedance as the trade-off.

8.2.2.1 Low-Noise Magnetic Media Equalizer

Figure 67 shows a high-performance low-noise equalizer for such applications as magnetic tape channels using the LMH6629. The circuit combines an integrator (used to limit noise) with a bandpass filter (used to boost the response centered at a frequency or over a band of interest) to produce the low-noise equalization. The circuit's simulated frequency response is illustrated in Figure 68.

In this circuit, the bandpass filter center frequency is set by Equation 13:

$$f_C = \frac{1}{2\pi\sqrt{LC}} \tag{13}$$

For higher selectivity, use high C values; for wider bandwidth, use high L values, while keeping the product of L and C values the same to keep f_c intact. The integrator's -3dB roll-off is set by

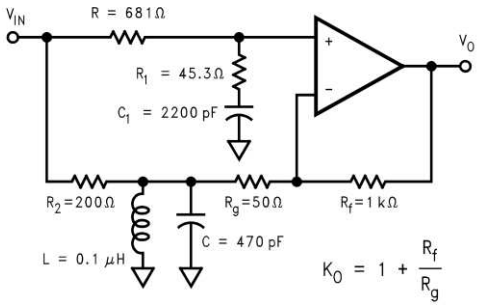
Typical Application (continued)

$$\frac{1}{2\pi C_1(R_1 + R)} \tag{14}$$

If:

$$\frac{1}{2\pi C_1 R_1} << f_C \tag{15}$$

The integrator and the bandpass filter frequency interaction is minimized so that the operating frequencies of each can be set independently. Lowering the value of R2 increases the bandpass gain (boost) without affecting the integrator frequencies. With the LMH6629's wide Gain Bandwidth (4 GHz), the center frequency could be adjusted higher without worries about loop gain limitation. This increases flexibility in tuning the circuit.



$$\frac{V_O}{V_{IN}} = K_O \left(\frac{sC_1 R_1 + 1}{sC_1 (R_1 + R) + 1} - \left(\frac{R_f}{R_f + R_g} \right) \frac{sLR_g}{s^2 LCR_2 R_g + sL(R_2 + R_g) + R_2 R_g} \right)$$

Figure 67. Low-Noise Magnetic Media Equalizer

8.2.3 Application Curves

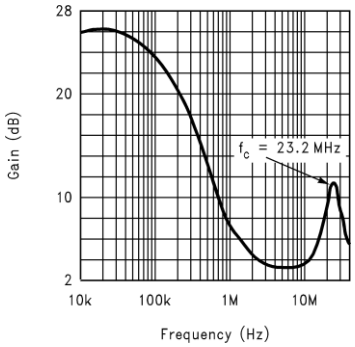


Figure 68. Equalizer Frequency Response

9 Power Supply Recommendations

The LMH6629 can operate off a single supply or with dual supplies. The input CM capability of the part (CMVR) extends all the way down to the V- rail to simplify single supply applications. Supplies should be decoupled with low inductance, often ceramic, capacitors to ground less than 0.5 inches from the device pins. The use of ground plane is recommended, and as in most high speed devices, it is advisable to remove ground plane close to device sensitive pins such as the inputs.

10 Layout

10.1 Layout Guidelines

Texas Instruments offers evaluation board(s) to aid in device testing and characterization and as a guide for proper layout. As is the case with all high-speed amplifiers, accepted-practice RF design technique on the PCB layout is mandatory. Generally, a good high-frequency layout exhibits a separation of power supply and ground traces from the inverting input and output pins. Parasitic capacitances between these nodes and ground may cause frequency response peaking and possible circuit oscillations. See Application Note OA-15, *Frequent Faux Pas in Applying Wideband Current Feedback Amplifiers* (SNOA367) for more information. Use high-quality chip capacitors with values in the range of 1000 pF to 0.1 µF for power supply bypassing. One terminal of each chip capacitor is connected to the ground plane and the other terminal is connected to a point that is as close as possible to each supply pin as allowed by the manufacturer's design rules. In addition, connect a tantalum capacitor with a value between 4.7 µF and 10 µF in parallel with the chip capacitor.

Harmonic Distortion, especially HD2, is strongly influenced by the layout and in particular can be affected by decoupling capacitors placed between the V^+ and V^- terminals as close to the device leads as possible.

Signal lines connecting the feedback and gain resistors should be as short as possible to minimize inductance and microstrip line effect. Place input and output termination resistors as close as possible to the input/output pins. Traces greater than 1 inch in length should be impedance matched to the corresponding load termination.

Symmetry between the positive and negative paths in the layout of differential circuitry should be maintained to minimize the imbalance of amplitude and phase of the differential signal.

Component value selection is another important parameter in working with high-speed / high-performance amplifiers. Choosing external resistors that are large in value compared to the value of other critical components will affect the closed loop behavior of the stage because of the interaction of these resistors with parasitic capacitances. These parasitic capacitors could either be inherent to the device or be a by-product of the board layout and component placement. Moreover, a large resistor will also add more thermal noise to the signal path. Either way, keeping the resistor values low will diminish this interaction. On the other hand, choosing very low value resistors could load down nodes and will contribute to higher overall power dissipation and high distortion.

10.2 Layout Example

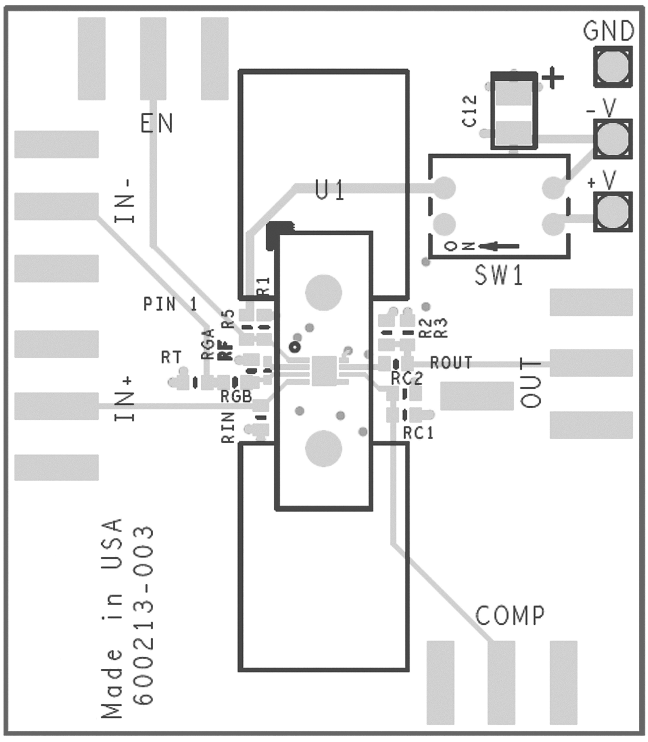


Figure 69. Evaluation Board Top Layer, WSON-8 Package

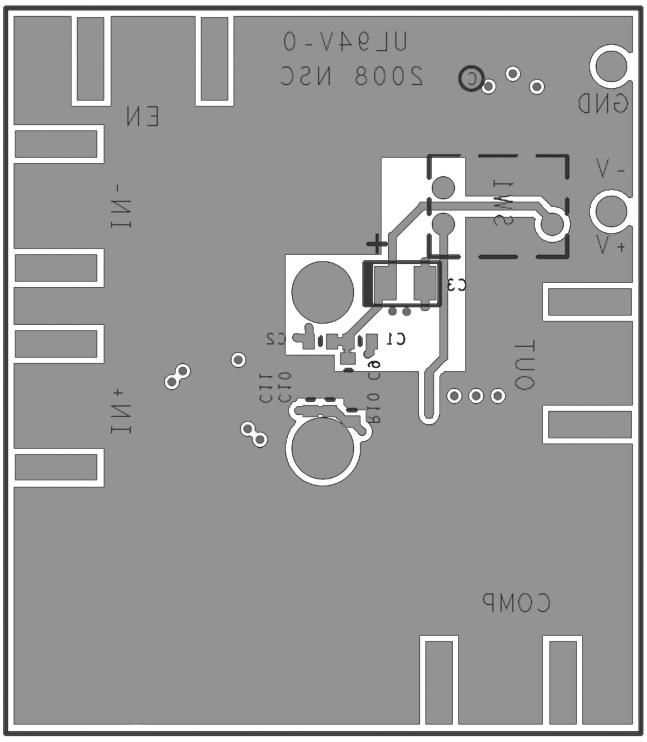


Figure 70. Evaluation Board Bottom Layer, WSON-8 Package

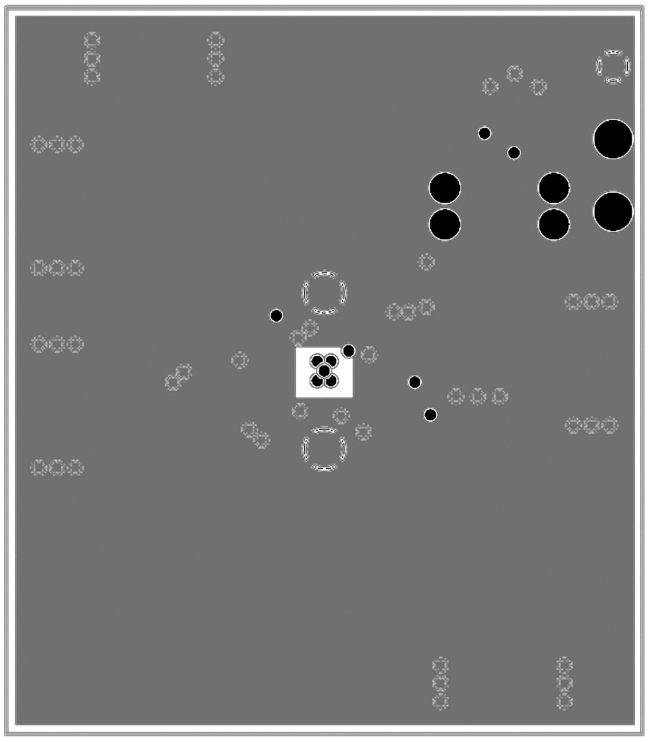


Figure 71. Evaluation Board Layer 2, WSON-8 Package

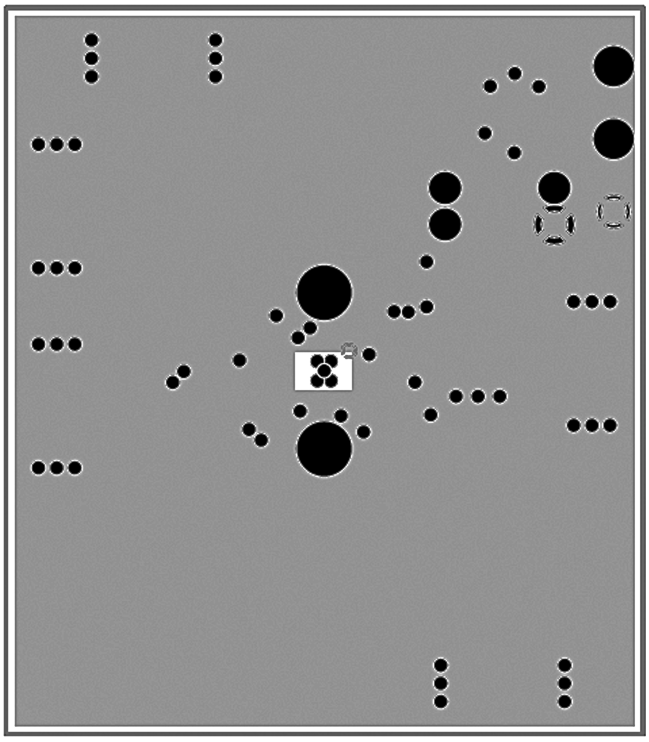


Figure 72. Evaluation Board Layer 3, WSON-8 Package

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- *Absolute Maximum Ratings for Soldering* (SNOA549)
- *Component Pre-Distortion for Sallen Key Filters*, Application Note OA-21 (SNOA369)
- *Frequent Faux Pas in Applying Wideband Current Feedback Amplifiers*, Application Note OA-15 (SNOA367)
- *Semiconductor and IC Package Thermal Metrics* (SPRA953)

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6629MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AE7A	Samples
LMH6629MFE/NOPB	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AE7A	Samples
LMH6629MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AE7A	Samples
LMH6629SD/NOPB	ACTIVE	WSON	NGQ	8	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L6629	Samples
LMH6629SDE/NOPB	ACTIVE	WSON	NGQ	8	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L6629	Samples
LMH6629SDX/NOPB	ACTIVE	WSON	NGQ	8	4500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L6629	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

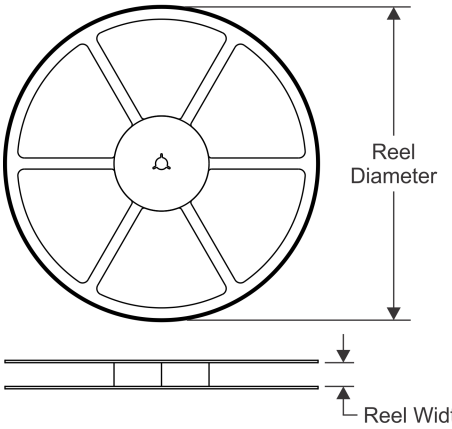
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

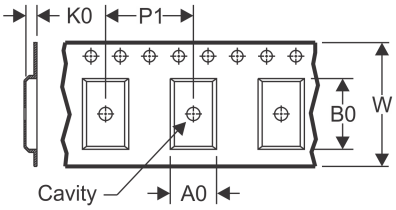
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

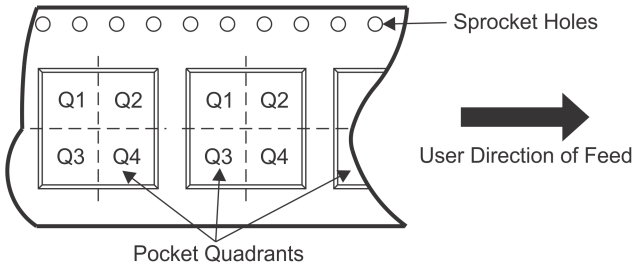


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

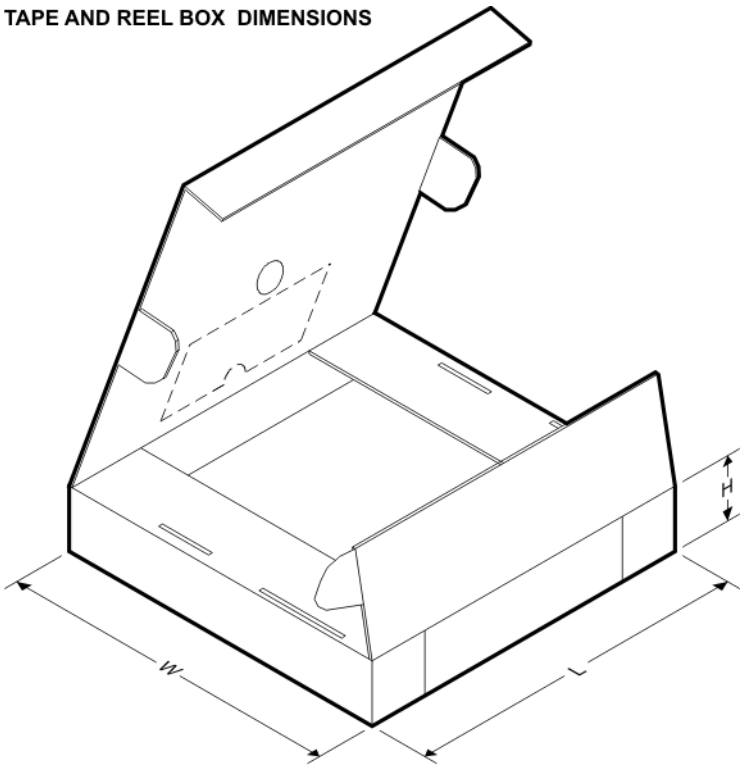
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6629MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6629MFE/NOPB	SOT-23	DBV	5	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6629MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6629SD/NOPB	WSON	NGQ	8	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LMH6629SDE/NOPB	WSON	NGQ	8	250	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LMH6629SDX/NOPB	WSON	NGQ	8	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

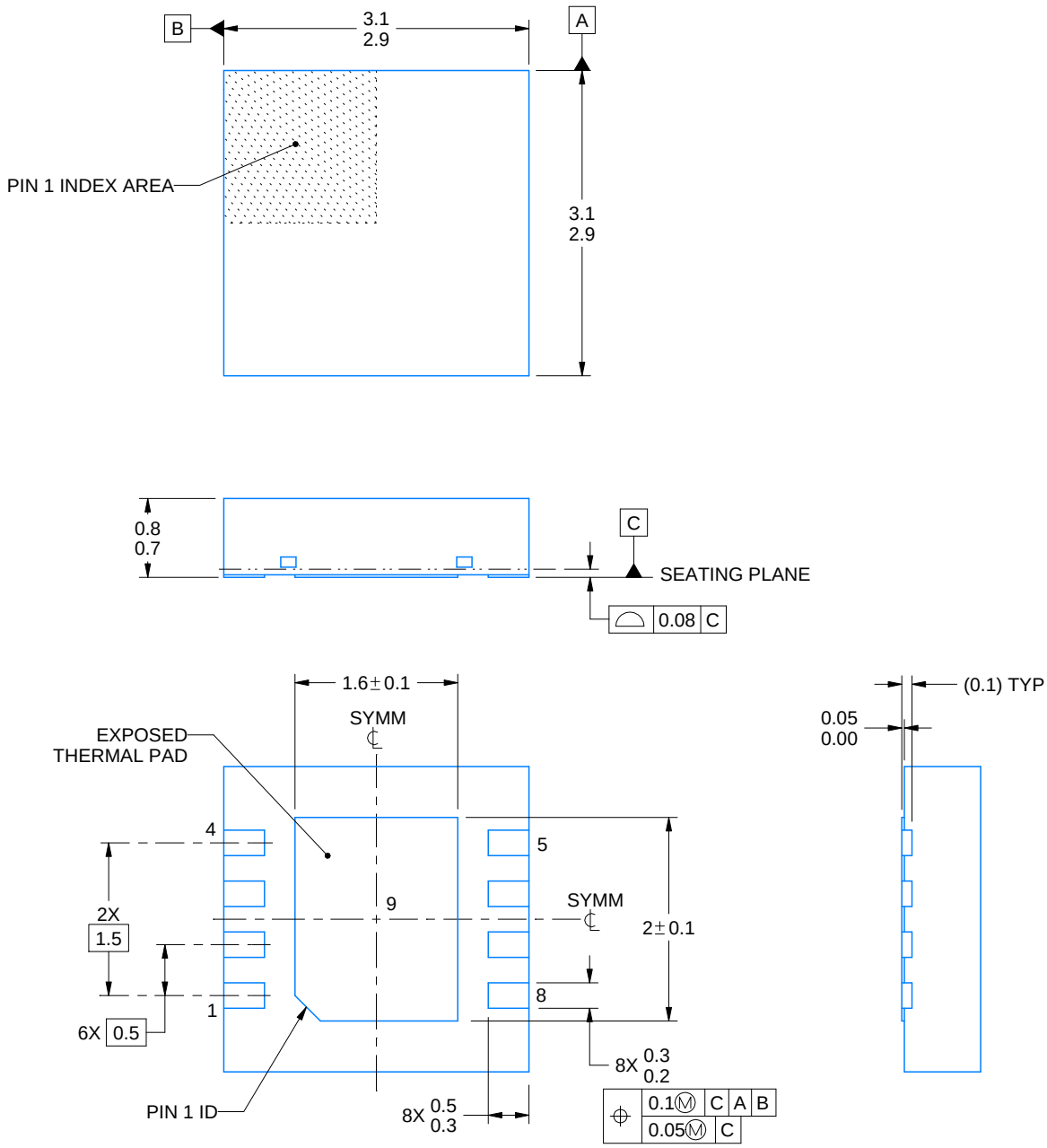
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6629MF/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMH6629MFE/NOPB	SOT-23	DBV	5	250	208.0	191.0	35.0
LMH6629MFX/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LMH6629SD/NOPB	WSON	NGQ	8	1000	208.0	191.0	35.0
LMH6629SDE/NOPB	WSON	NGQ	8	250	208.0	191.0	35.0
LMH6629SDX/NOPB	WSON	NGQ	8	4500	853.0	449.0	35.0

PACKAGE OUTLINE

NGQ0008A

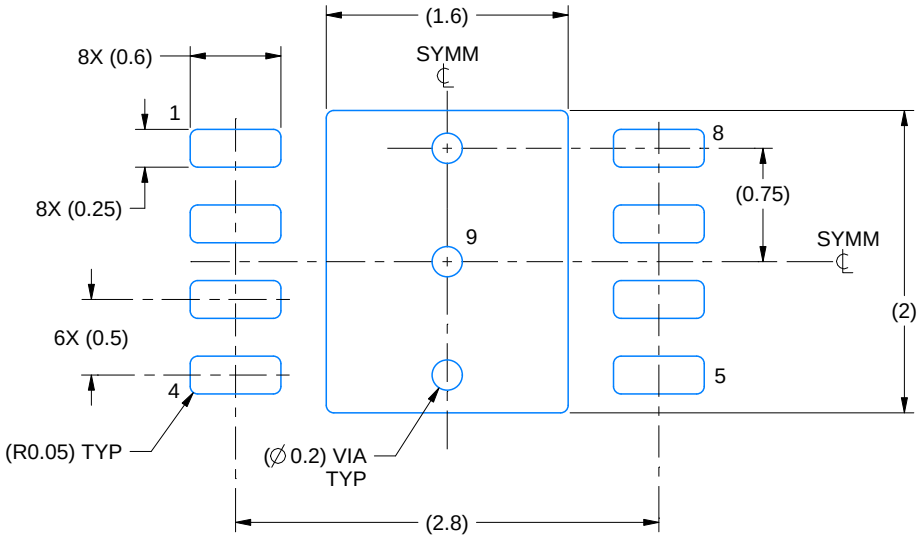
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

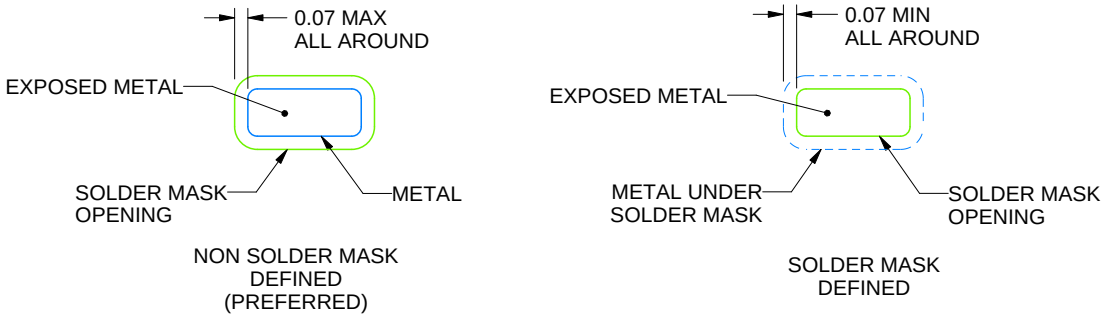


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

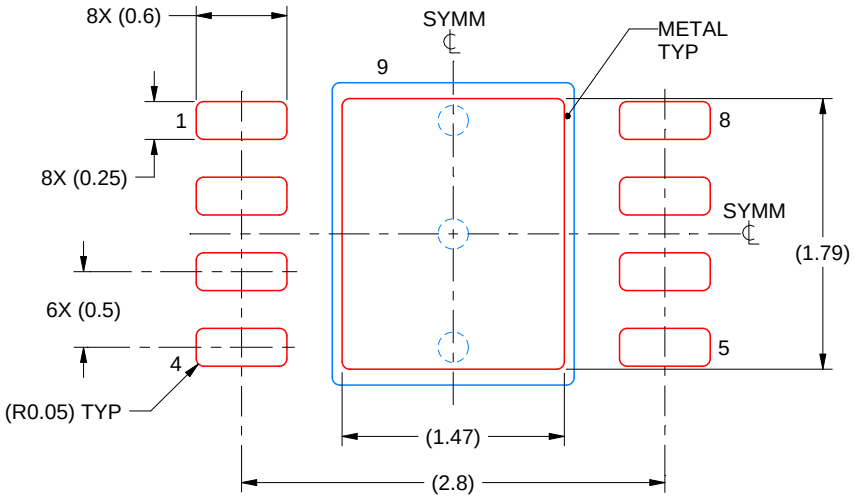


SOLDER MASK DETAILS

4214922/A 03/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 9:
82% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4214922/A 03/2018

NOTES: (continued)

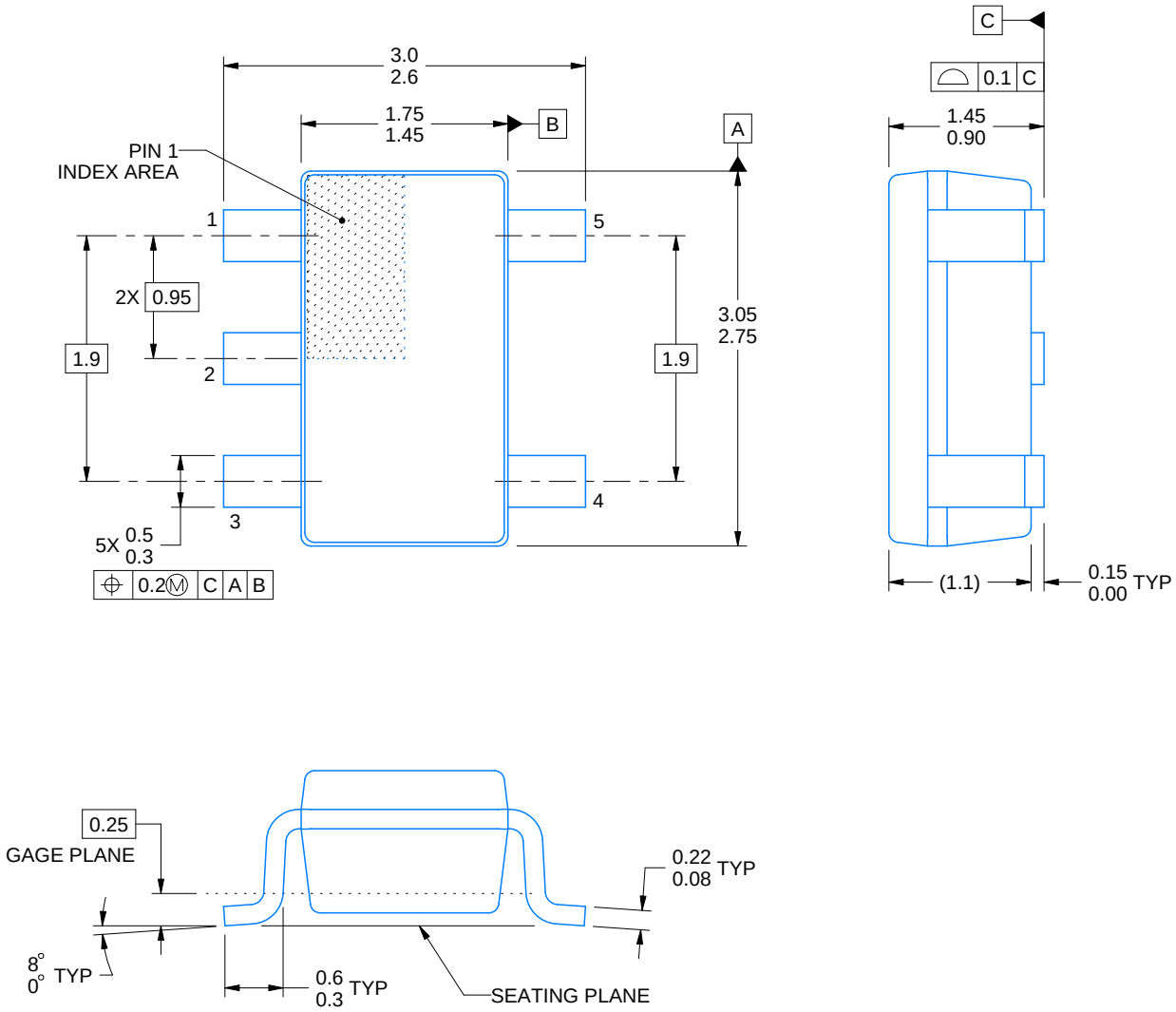
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

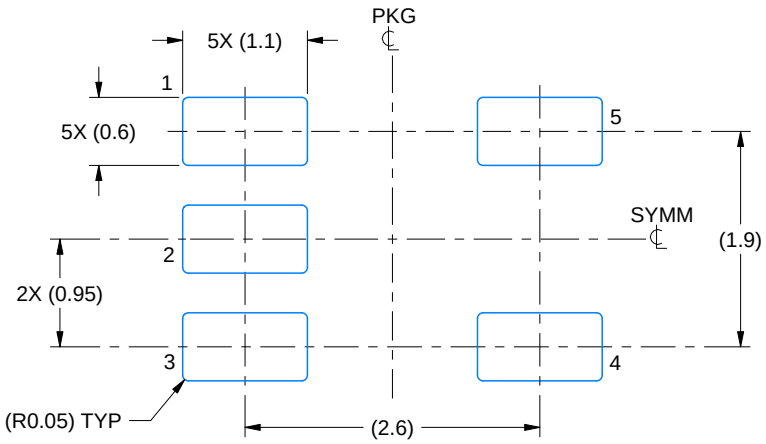
SMALL OUTLINE TRANSISTOR



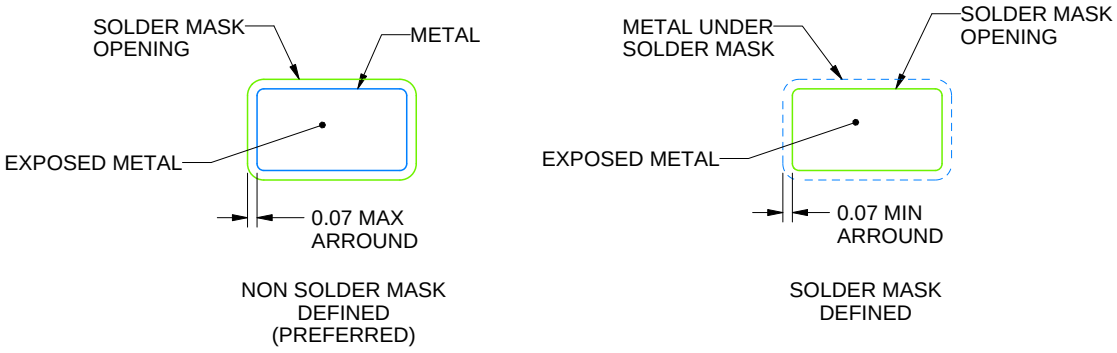
4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

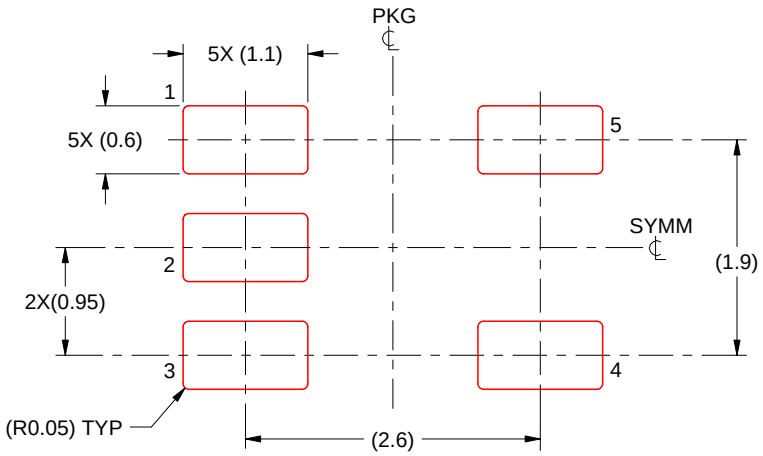


SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265