EMIPAK 1B PressFit Power Module
600 V Full Bridge MOSFET, 50 A

EMIPAK 1B
(package example)

PRIMARY CHARACTERISTICS	
FULL BRIDGE - QB1 to QB4 MOSFET	
V_{DSS}	600 V
$R_{DS(ON)}$ typical at I_D = 50 A	37 mΩ
I_D at T_C = 77 °C	50 A
Package	EMIPAK 1B
Circuit configuration	MOSFET full bridge inverter
Type	Modules - MOSFET

FEATURES

RoHS COMPLIANT

- EF series power MOSFET
- Low input capacitance (C_{iss})
- Ultra low gate charge (Q_g)
- Exposed Al_2O_3 substrate with low thermal resistance
- Avalanche energy rated (UIS)
- Low internal inductance
- Qualified using AQG324 guideline as reference
- PressFit pins locking technology
  PATENT(S): www.vishay.com/patents
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

DESCRIPTION

The EMIPAK 1B package is easy to use thanks to the PressFit pins. The exposed substrate provides improved thermal performance.

The optimized layout also helps to minimize stray parameters, allowing for better EMI performance.

ABSOLUTE MAXIMUM RATINGS (T_J = 25 °C unless otherwise noted)				
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MAX.**	**UNITS**
Operating junction temperature	T_J		150	°C
Storage temperature range	T_{Stg}		-40 to +150	
RMS isolation voltage	V_{ISOL}	T_J = 25 °C, all terminals shorted, f = 50 Hz, t = 1 s	3500	V
QB1 to QB4 - MOSFET				
Drain to source voltage	V_{DSS}		600	V
Gate to source voltage	V_{GS}		± 30	
Pulsed drain current	I_{DM} (1)	V_{GS} = 10 V	135	A
Continuous drain current	I_D	T_{SINK} = 25 °C	44	A
		T_{SINK} = 80 °C	34	
Power dissipation	P_D	T_{SINK} = 25 °C	173	W
		T_{SINK} = 80 °C	97	
Single pulse avalanche energy	E_{AS}	L = 10 mH, I_{AS} = 23 A, T_J = 25 °C	2645	mJ
Pulsed source current (body diode)	I_{SM}		135	A

Note
(1) Pulse width limited by safe operating area

PATENT(S): www.vishay.com/patents
This Vishay product is protected by one or more United States and international patents.

ELECTRICAL SPECIFICATIONS (T_J = 25 °C unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
QB1 to QB4 - MOSFET						
Drain to source breakdown voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 250 μA	600	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA	-	0.46	-	V/°C
Drain to source on resistance	$R_{DS(ON)}$	V_{GS} = 10 V, I_D = 50 A	-	37	48	mΩ
		V_{GS} = 10 V, I_D = 50 A, T_J = 150 °C	-	82	-	
Gate threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	1.8	2.7	4.4	V
Temperature coefficient of threshold voltage	$\Delta V_{GS(th)}/\Delta T_J$	V_{DS} = V_{GS}, I_D = 250 μA (25 °C to 125 °C)	-	-11.5	-	mV/°C
Forward transconductance	g_{fs}	V_{DS} = 20 V, I_D = 50 A	-	48	-	S
Transfer characteristics	V_{GS}	V_{DS} = 20 V, I_D = 50 A	-	5.3	-	V
Zero gate voltage drain current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 600 V	-	0.7	10	μA
		V_{GS} = 0 V, V_{DS} = 600 V, T_J = 150 °C	-	1.1	-	mA
Gate to source leakage current	I_{GSS}	V_{GS} = ± 20 V, V_{DS} = 0 V	-	-	± 150	nA
QB1 to QB4 - BODY DIODE						
Source to drain voltage drop	V_{SD}	I_{SD} = 40 A, V_{GS} = 0 V	-	0.92	1.32	V

SWITCHING CHARACTERISTICS (T_J = 25 °C unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
QB1 to QB4 - MOSFET						
Total gate charge (turn-on)	Q_g	I_D = 50 A, V_{DS} = 480 V, V_{GS} = 10 V	-	240	-	nC
Gate to source charge (turn-on)	Q_{gs}		-	65	-	
Gate to drain charge (turn-on)	Q_{gd}		-	105	-	
Turn-off energy loss	E_{OFF}	I_D = 50 A, V_{DD} = 450 V, V_{GS} = +10 V / -10 V, R_g = 10 Ω, L = 500 μH	-	0.20	-	mJ
Turn-off delay time	$t_{d(off)}$		-	141	-	ns
Fall time	t_f		-	17	-	
Turn-off energy loss	E_{OFF}	I_D = 50 A, V_{DD} = 450 V, V_{GS} = +10 V / -10 V, R_g = 10 Ω, L = 500 μH, T_J = 125 °C	-	0.24	-	mJ
Turn-off delay time	$t_{d(off)}$		-	149	-	ns
Fall time	t_f		-	18	-	
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz	-	7500	-	pF
Output capacitance	C_{oss}		-	378	-	
Reverse transfer capacitance	C_{rss}		-	5	-	
Effective output capacitance, energy related	$C_{D(er)}$ (1)	V_{GS} = 0 V, V_{DS} = 0 V to 480 V	-	263	-	pF
Effective output capacitance, time related	$C_{D(tr)}$ (2)		-	926	-	
Reverse bias safe operating area	RBSOA	T_J = 150 °C, I_D = 120 A, V_{DD} = 400 V, V_p = 600 V, R_g = 10 Ω, V_{GS} = ± 10 V				
QB1 to QB4 - BODY DIODE						
Diode reverse recovery time	t_{rr}	V_R = 200 V, T_J = 25 °C, I_S = 50 A, dI/dt = 100 A/μs	-	220	-	ns
Diode reverse recovery current	I_{rr}		-	18	-	A
Diode reverse recovery charge	Q_{rr}		-	2000	-	nC

Notes

(1) $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}

(2) $C_{oss(tr)}$ is a fixed capacitance that gives the charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}

INTERNAL NTC - THERMISTOR SPECIFICATIONS				
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**VALUE**	**UNITS**
Resistance	R_{25}	T_C = 25 °C	5000	Ω
	R_{100}	T_C = 100 °C	493 ± 5 %	
B-value	$B_{25/50}$	$R_2 = R_{25}$ exp. [$B_{25/50}$(1/T2 - 1/(298.15K))]	3375 ± 5 %	K
Maximum operating temperature			220	°C
Dissipation constant			2	mW/°C
Thermal time constant			8	s

THERMAL AND MECHANICAL SPECIFICATIONS					
PARAMETER	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
QB1 to QB4 - MOSFET - Junction to case thermal resistance (per switch)	R_{thJC}	-	-	0.3	°C/W
QB1 to QB4 - MOSFET - Case to sink thermal resistance (per switch) [1]	R_{thCS}	-	0.42	-	°C/W
Case to sink thermal resistance (per module) [1]		-	0.1	-	
Mounting torque (M4)		2	-	3	Nm
Weight		-	28	-	g

Note

[1] Mounting surface flat, smooth, and greased, λ_{grease} = 0.67 W/mK

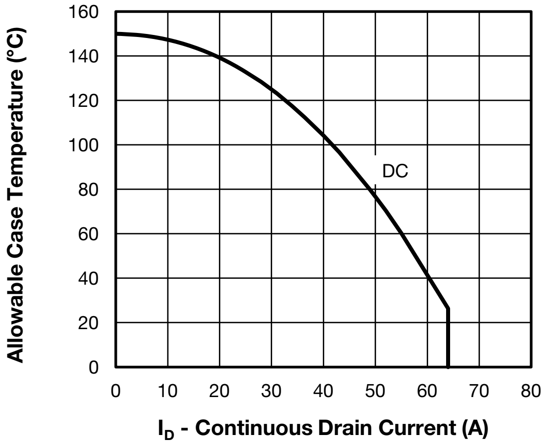


Fig. 1 - Maximum Continuous Drain Current vs. Case Temperature

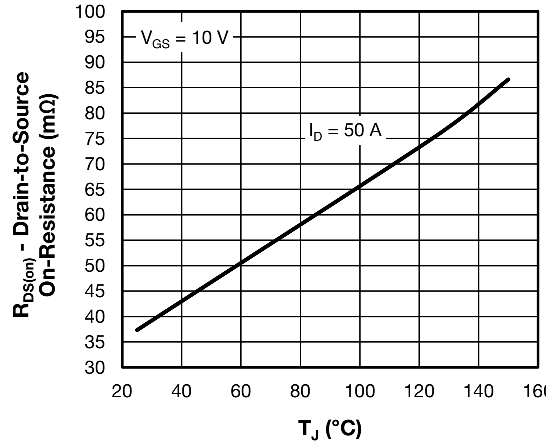


Fig. 4 - Typical Drain to Source On-Resistance vs. Temperature

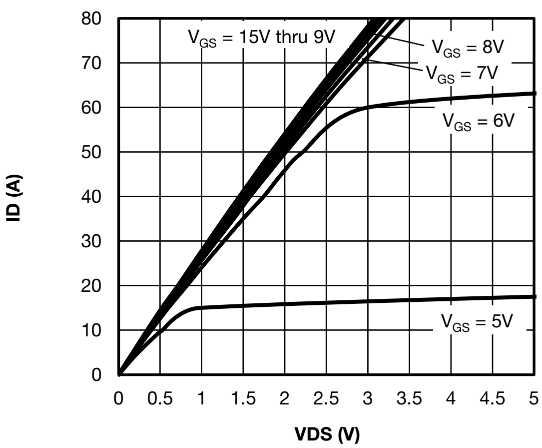


Fig. 2 - Typical Drain to Source Current Output Characteristics at T_J = 25 °C

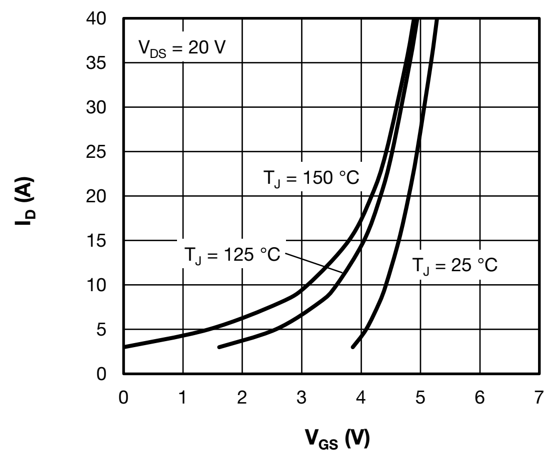


Fig. 5 - Typical Transfer Characteristics

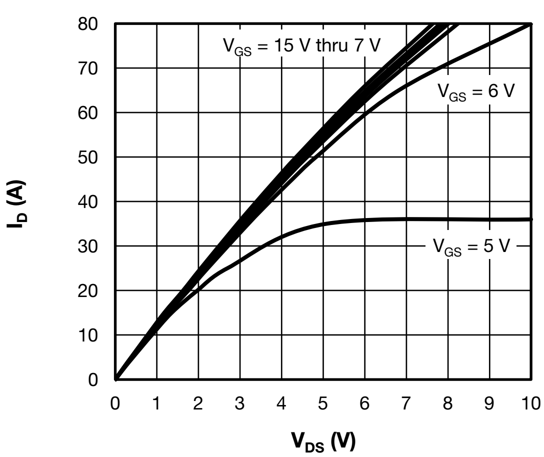


Fig. 3 - Typical Drain to Source Current Output Characteristics at T_J = 150 °C

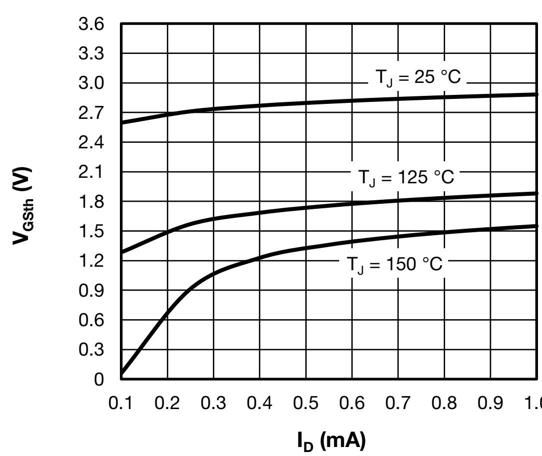


Fig. 6 - Typical Gate Threshold Voltage Characteristics

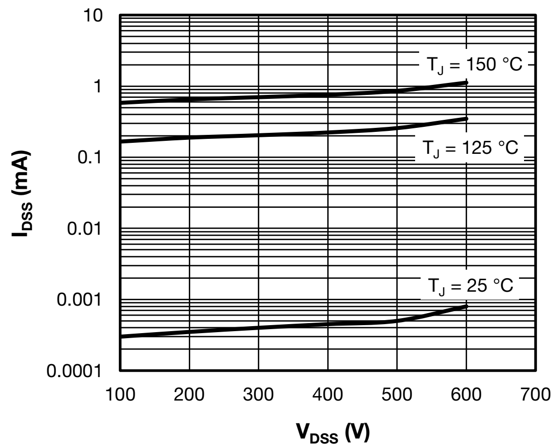


Fig. 7 - Typical Zero Gate Voltage Drain Current

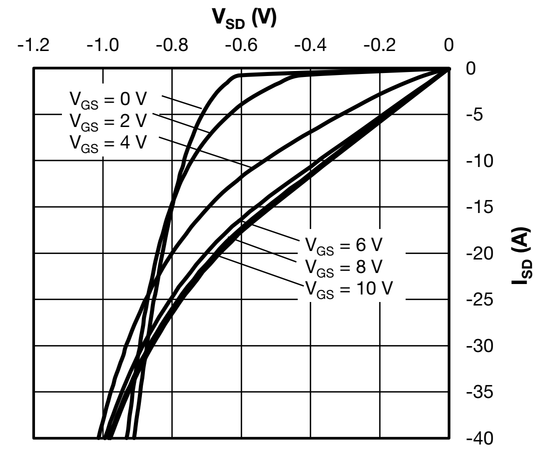


Fig. 10 - Typical Source to Drain Current Characteristics at T_J = 25 °C

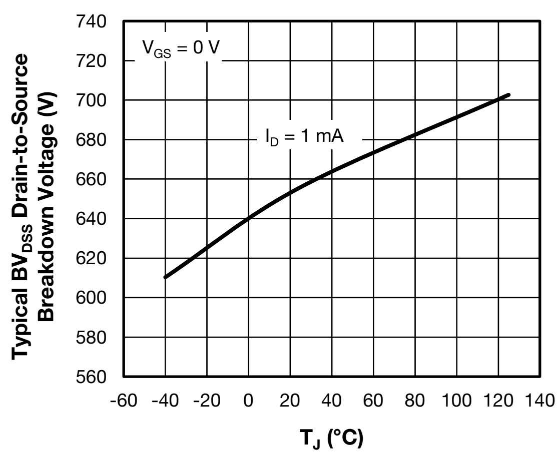


Fig. 8 - Typical Drain to Source Breakdown Voltage vs. Temperature

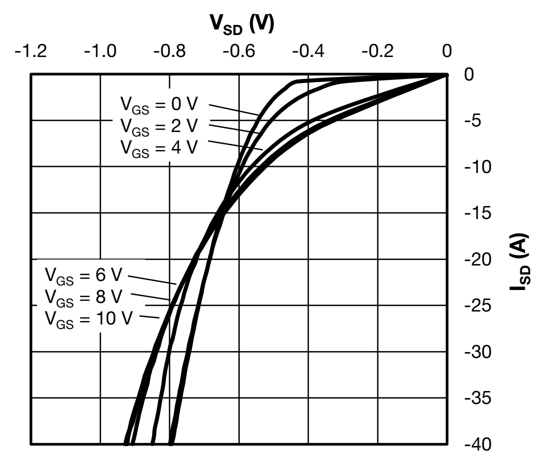


Fig. 11 - Typical Source to Drain Current Characteristics at T_J = 125 °C

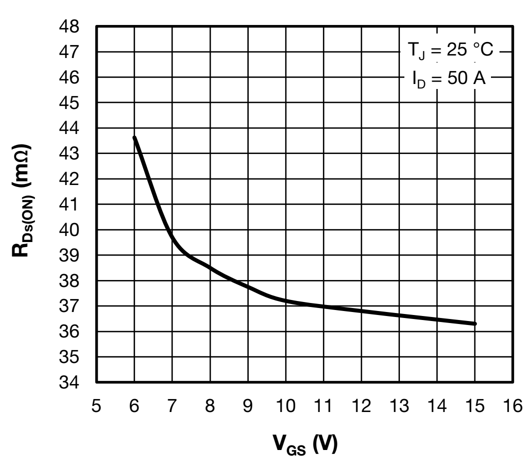


Fig. 9 - Typical Drain-State Resistance vs. Gate to Source Voltage

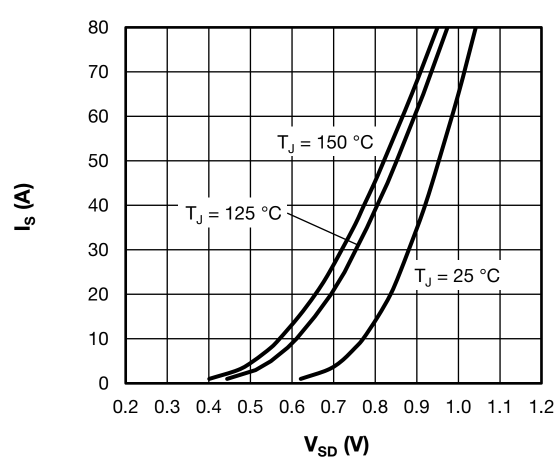


Fig. 12 - Typical Body Diode Source to Drain Current Characteristics

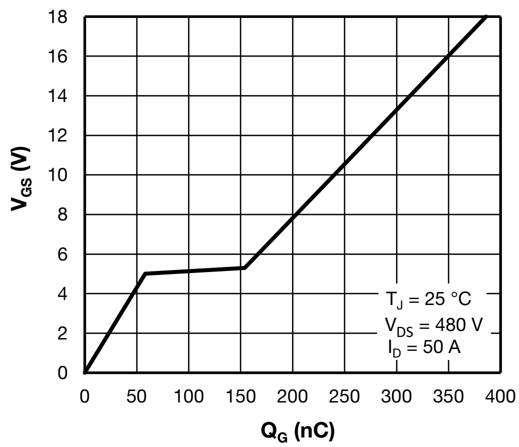


Fig. 13 - Typical Gate Charge vs. Gate to Source Voltage

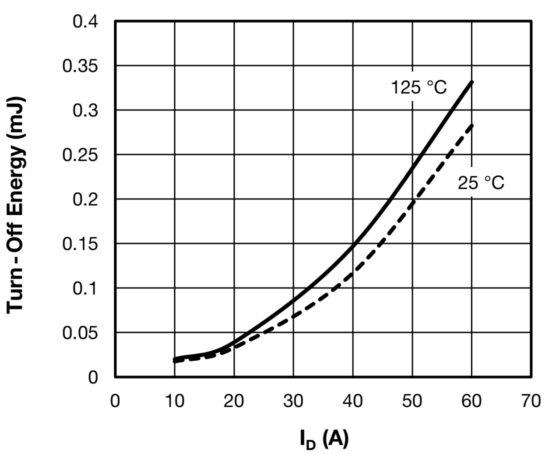


Fig. 14 - Typical Turn-off Energy Loss vs. I_D
V_{DD} = 450 V, R_g = 10 Ω, V_{GS} = ± 10 V, L = 500 µH

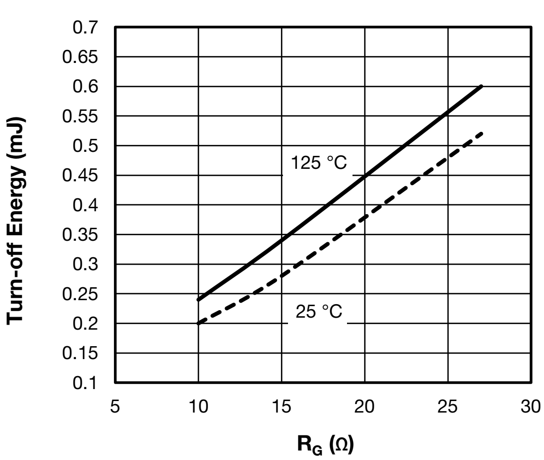


Fig. 15 - Typical Turn-off Energy Loss vs. R_g
V_{DD} = 450 V, I_D = 50 A, V_{GS} = ± 10 V, L = 500 µH

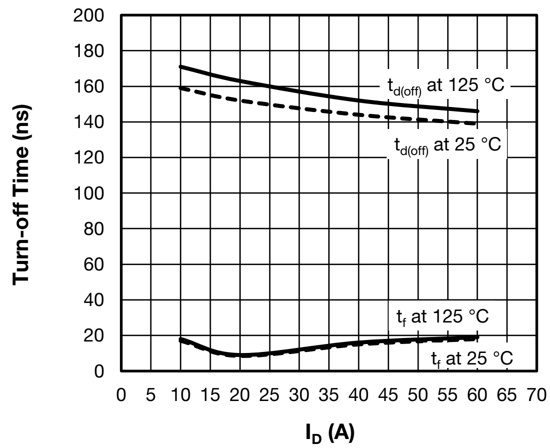


Fig. 16 - Typical Turn-off Switching Time vs. I_D
V_{DD} = 450 V, R_g = 10 Ω, V_{GS} = ± 10 V, L = 500 µH

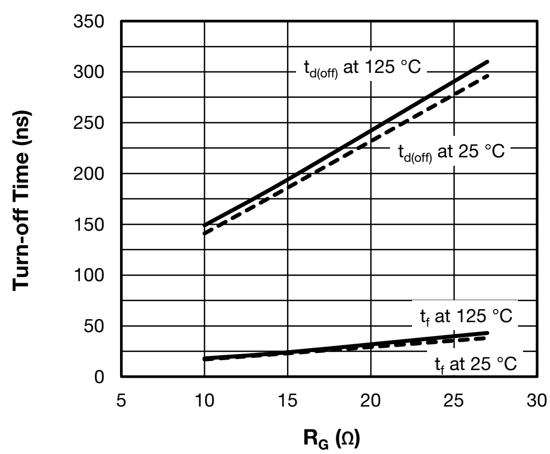


Fig. 17 - Typical Turn-off Switching Time vs. R_g
V_{DD} = 450 V, I_D = 50 A, V_{GS} = ± 10 V, L = 500 µH

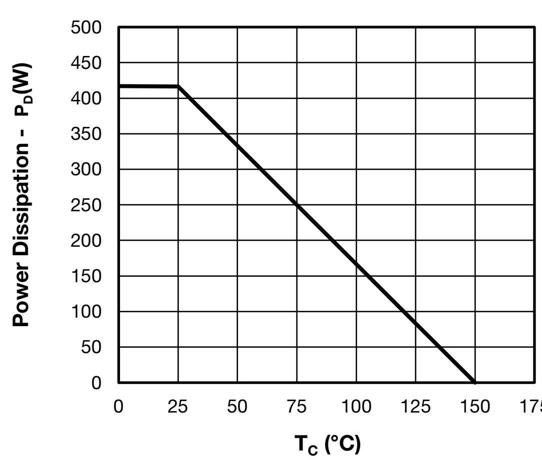


Fig. 18 - Power Dissipation Curve

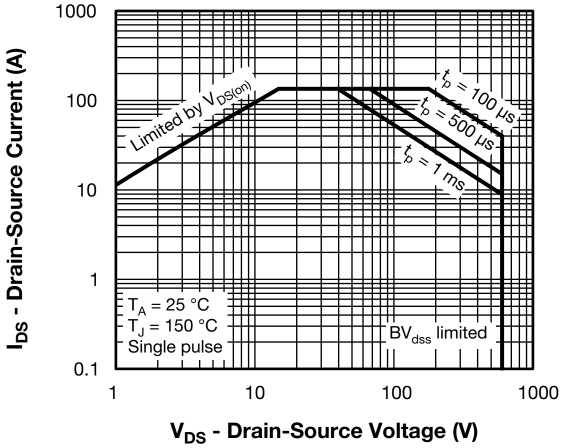


Fig. 19 - Safe Operating Area

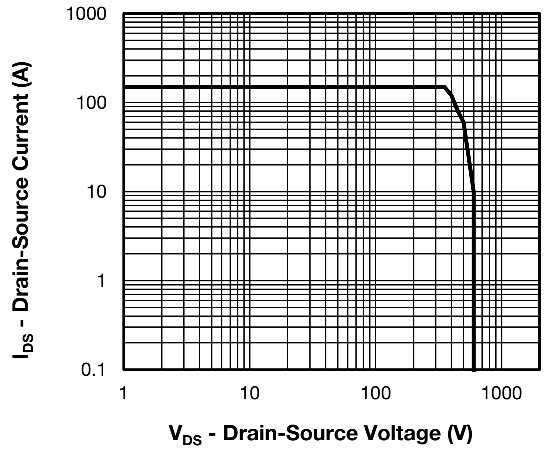


Fig. 20 - Reverse BIAS SOA

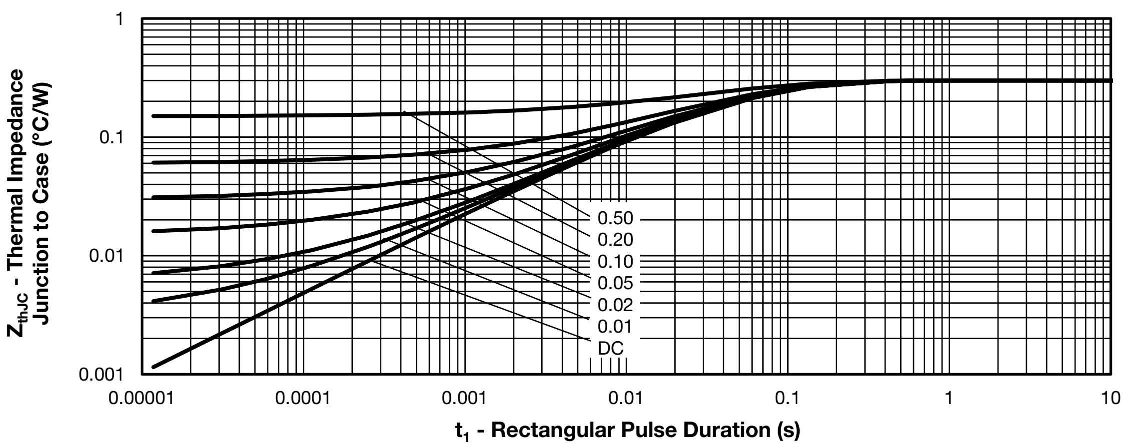
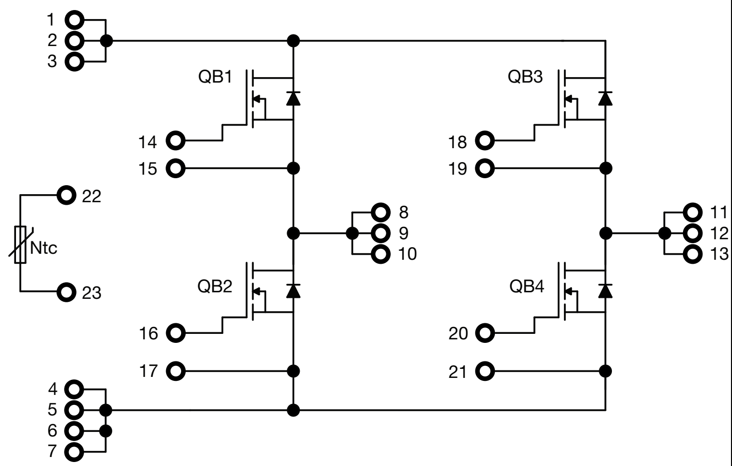


Fig. 21 - Maximum Thermal Impedance Z_{thJC} Characteristics

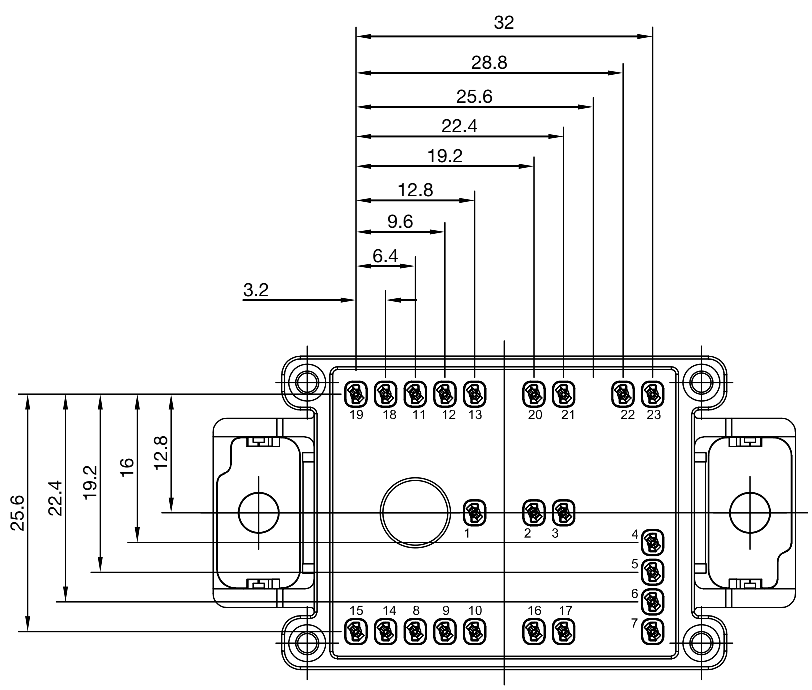
ORDERING INFORMATION TABLE

Device code	VS-	EN	Y	050	C	60
	1	2	3	4	5	6

- **1** - Vishay Semiconductors product
- **2** - Package indicator (EN = EMIPAK 1B)
- **3** - Circuit configuration (Y = MOSFET full bridge inverter)
- **4** - Current rating (050 = 50 A)
- **5** - Switch die technology (C = PowerMOS)
- **6** - Voltage rating (60 = 600 V)

CIRCUIT CONFIGURATION		
CIRCUIT	**CIRCUIT CONFIGURATION CODE**	**CIRCUIT DRAWING**
MOSFET full bridge inverter	Y	

PACKAGE



LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95558
Application Note	www.vishay.com/doc?95580

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