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TFT | CHARACTER | UWVD | FSC | SEGMENT | CUSTOM | REPLACEMENT

TFT Display Module

Part Number

E35RG73248LW6M250-R

Overview:

- 3.5-inch TFT (55.50x84.96mm)
- 320(RGB)x480 pixels
- 8/9/16/18-bit MCU
- 3/4-SPI+16/18-bit RGB
- White LED back-light
- Transmissive/ Normally White
- Resistive Touch Screen
- 250 NITS
- Controller: ILI9488
- RoHS Compliant

Description

This is a color active matrix TFT (Thin Film Transistor) LCD (Liquid Crystal Display) that uses amorphous silicon TFT as a switching device. This model is composed of a transmissive type TFT-LCD Panel, driver circuit, resistive touch panel and a backlight unit. The resolution of the 3.5" TFT-LCD contains 320x480 pixels and can display up to 65K/262K colors.

TFT Features

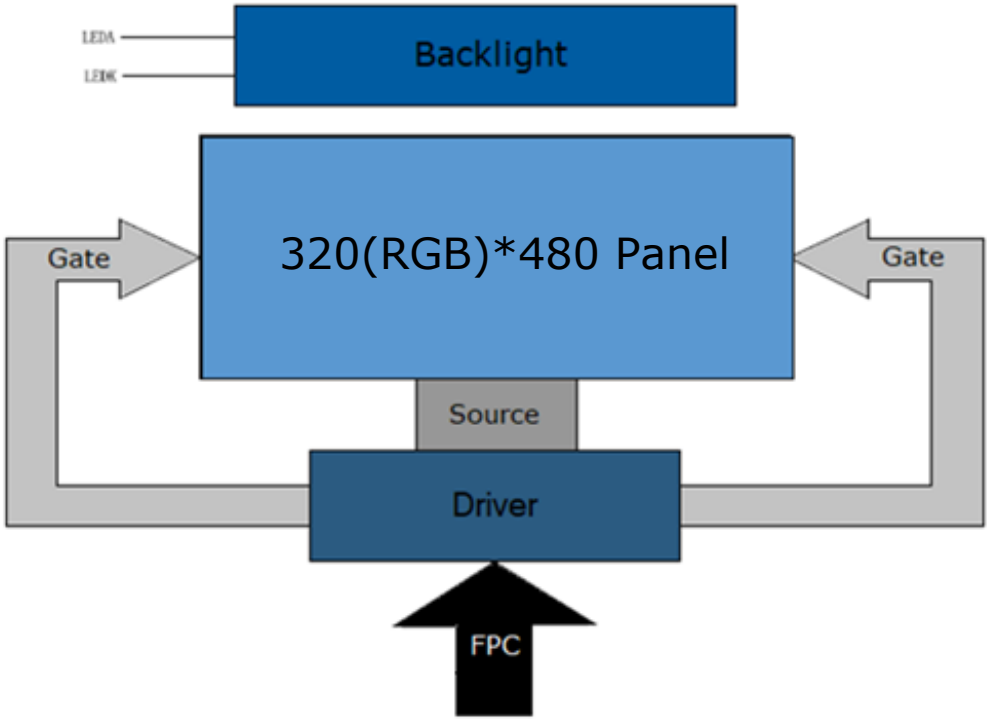
Low Input Voltage: 3.3V (TYP)
Display Colors: 65K/262K
Interfaces: 8/9/16/18-bit 8080 MCU
3/4 SPI + 16/18-bit RGB
3/4-wire Serial

General Information Items	Specification Main Panel	Unit	Note
TFT Display area (AA)	48.96 (H) x 73.44 (V) (3.5 inch)	mm	-
Driver element	TFT active matrix	-	-
Display colors	65K/262K	colors	-
Number of pixels	320(RGB)x480	dots	-
TFT Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.153 (H) x 0.153 (V)	mm	-
Viewing angle	6:00	o'clock	-
TFT Controller IC	ILI9488	-	-
Display mode	Transmissive/ Normally White	-	-
Operating temperature	-20～+70	℃	-
Storage temperature	-30～+80	℃	-

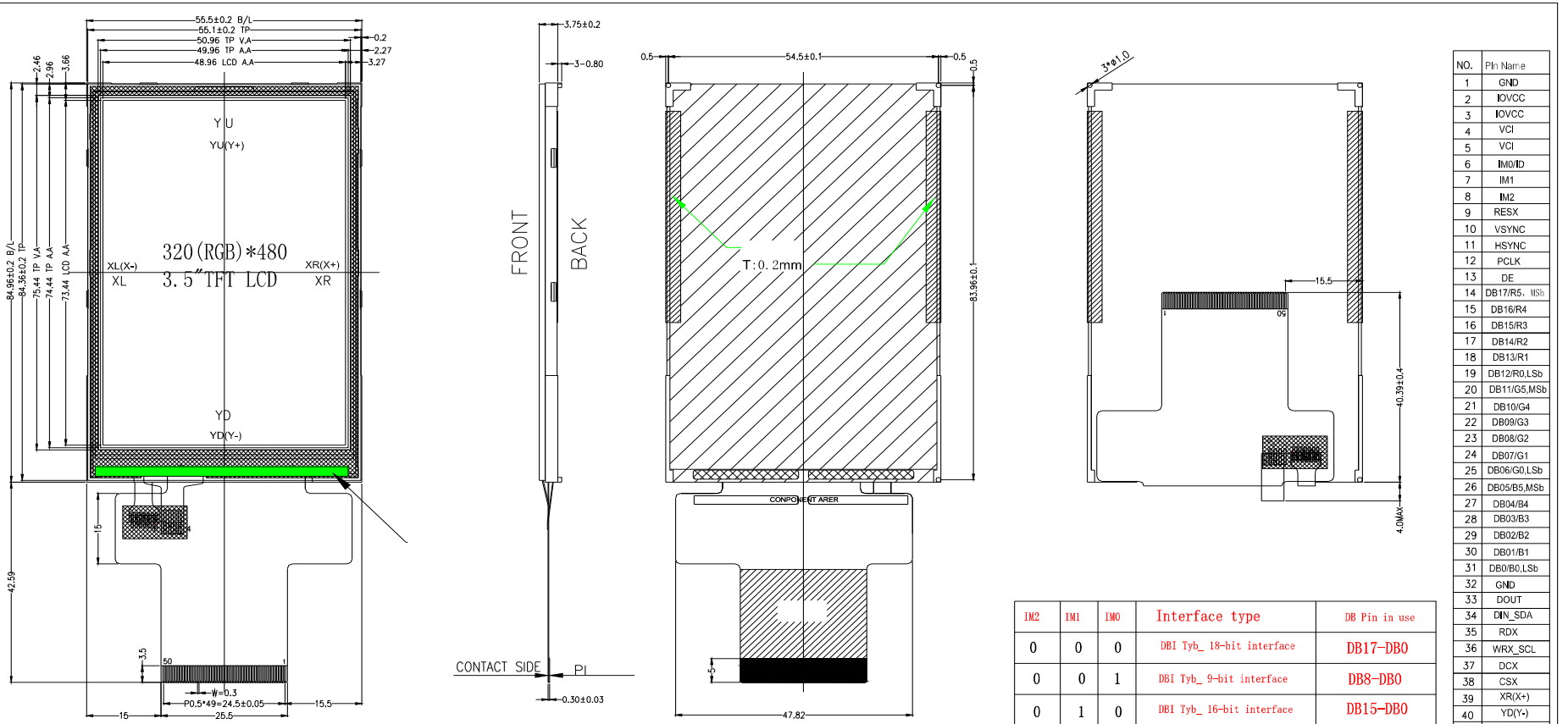
Mechanical Information

Item		Min	Typ.	Max	Unit	Note
Module size	Height (H)		55.50		mm	-
	Vertical (V)		84.96		mm	-
	Depth (D)		3.6		mm	-
Weight			TBD		g	-

1. Block Diagram



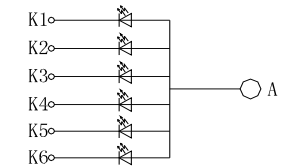
2. Outline Dimensions



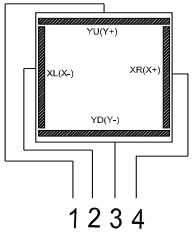
NO.	Pin Name
1	GND
2	IOVCC
3	IOVCC
4	VCI
5	VCI
6	IM0/ID
7	IM1
8	IM2
9	RESX
10	VSYNC
11	HSYNC
12	PCLK
13	DE
14	DB17/R5, MSb
15	DB16/R4
16	DB15/R3
17	DB14/R2
18	DB13/R1
19	DB12/R0,LSb
20	DB11/G5,MSb
21	DB10/G4
22	DB09/G3
23	DB08/G2
24	DB07/G1
25	DB06/G0,LSb
26	DB05/B5,MSb
27	DB04/B4
28	DB03/B3
29	DB02/B2
30	DB01/B1
31	DB0/B0,LSb
32	GND
33	DOUT
34	DIN_SDA
35	RDX
36	WRX_SCL
37	DCX
38	CSX
39	XR(X+)
40	YD(Y-)
41	XL(X-)
42	YU(Y+)
43	LEDA
44	LEDK1
45	LEDK2
46	LEDK3
47	LEDK4
48	LEDK5
49	LEDK6
50	GND

IM2	IM1	IM0	Interface type	DB Pin in use
0	0	0	DBI Tyb_ 18-bit interface	DB17-DB0
0	0	1	DBI Tyb_ 9-bit interface	DB8-DB0
0	1	0	DBI Tyb_ 16-bit interface	DB15-DB0
0	1	1	DBI Tyb_ 8-bit interface	DB7-DB0
1	0	1	3-Wire 9 BIT data serial interface	SDI SCL CS
1	1	1	4-Wire 8 BIT data serial interface	SDI SCL CS RS

NOTE:
1. If not use PIN, fix to the GND , IOVCC or NC.
2. If use RGB interface must select serial interface



LED(B/L) CIRCUIT



NOTES:

1. DISPLAY TYPE: 3.5", TFT-LCD, 65K/262K COLORS
2. DISPLAY MODE: T/N NORMALLY WHITE
3. VIEWING DIRECTION: 6:00
4. DRIVER IC: ILI9488 (COG)
5. VCI: 3.3V,
6. OPERATING TEMP: -20°C TO 70°C
   STORAGE TEMP: -30°C TO 80°C
7. BACK LIGHT: LED WHITE, 6 LED, 90mA, 3.2V±0.3V
8. RoHS COMPLIANT.

ReV.	Revision content description	Date

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TOLERANCE		DRAWING NAME	E35RG73248LW6M250-R
		PARTS NO.	
TOLERANCE UNLESS OTHERWISE SPECIFIED	X.X±0.3 X.XX±0.2	Drawn	Unit
		Checked	mm
Scale 1:1		Approve	Page 1/1

3. Input Terminal Pin Assignment

NO.	Symbol	Description	I/O
1	GND	Ground	P
2	IOVCC	Supply voltage (3.3V)	P
3	IOVCC	Supply voltage (3.3V)	P
4	VCI	Supply voltage (3.3V)	P
5	VCI	Supply voltage (3.3V)	P
6	IM0/ID	Interface select:	I
7	IM1		I
8	IM2		I
9	RESX	Reset signal of the device. Must be applied to properly initialize the chip.	I
10	VSYNC	Frame synchronizing signal for RGB interface. Fix to VCI or GND when not in use.	I
11	HSYNC	Line synchronizing signal for RGB interface. Fix to VCI or GND when not in use.	I
12	PCLK	Dot clock signal for RGB interface. Fix to VCI or GND when not in use.	I
13	DE	Data enable signal for RGB interface. Fix to VCI or GND when not in use.	I
14-31	DB17-DB0	18-bit parallel bi-directional data bus for MCU and RGB interface modes. Fix to GND when not in use.	I
32	GND	Ground	P
33	DOUT	Serial data output pin in serial system interface. Leave open if not used.	O
34	DIN_SDA	Serial input signal. Data applied on the rising edge of the SCL signal. Fix to VCI or GND when not in use.	I
35	RDX	Read signal and MCU read data at the rising edge. Fix to VCI or GND when not used.	I
36	WRX_SCL	Write signal for parallel interface. Clock in serial interface. Fix to VCI or GND when not in use.	I
37	D/CX	Data/Command selection. Low: Command, High: Parameter. Fix to VCI or GND when not used.	I
38	CSX	Chip select signal. (Low enable). Fix to VCI or GND when not in use.	I
39	XR	Touch panel right glass terminal	A/D
40	YD	Touch panel bottom film terminal	A/D
41	XL	Touch panel left glass terminal	A/D
42	YU	Touch panel top film terminal	A/D
43	LEDA	Anode pin of the backlight	P
44	LEDK1	Cathode pin of the backlight	P
45	LEDK2	Cathode pin of the backlight	P
46	LEDK3	Cathode pin of the backlight	P
47	LEDK4	Cathode pin of the backlight	P
48	LEDK5	Cathode pin of the backlight	P
49	LEDK6	Cathode pin of the backlight	P
50	GND	Ground	P

IM2	IM1	IM0	Interface
0	0	0	MIPI-DBI Type B 24-bit bus (DB_EN = 1)
0	0	0	MIPI-DBI Type B 18-bit bus (DB_EN = 0)
0	0	1	MIPI-DBI Type B 9-bit bus
0	1	0	MIPI-DBI Type B 16-bit bus
0	1	1	MIPI-DBI Type B 8-bit bus
1	0	1	MIPI-DBI Type C Option 1 (3-line SPI)
1	1	0	MIPI DSI
1	1	1	MIPI-DBI Type C Option 3 (4-line SPI)

I: Input, O: Output, P: Power

4. LCD Optical Characteristics

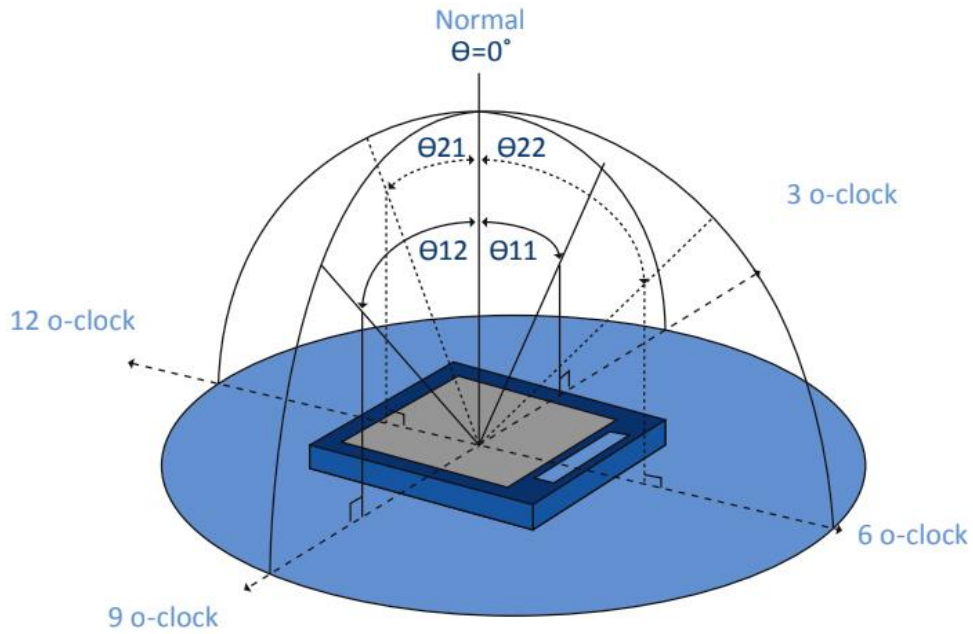
4.1 Optical Specifications

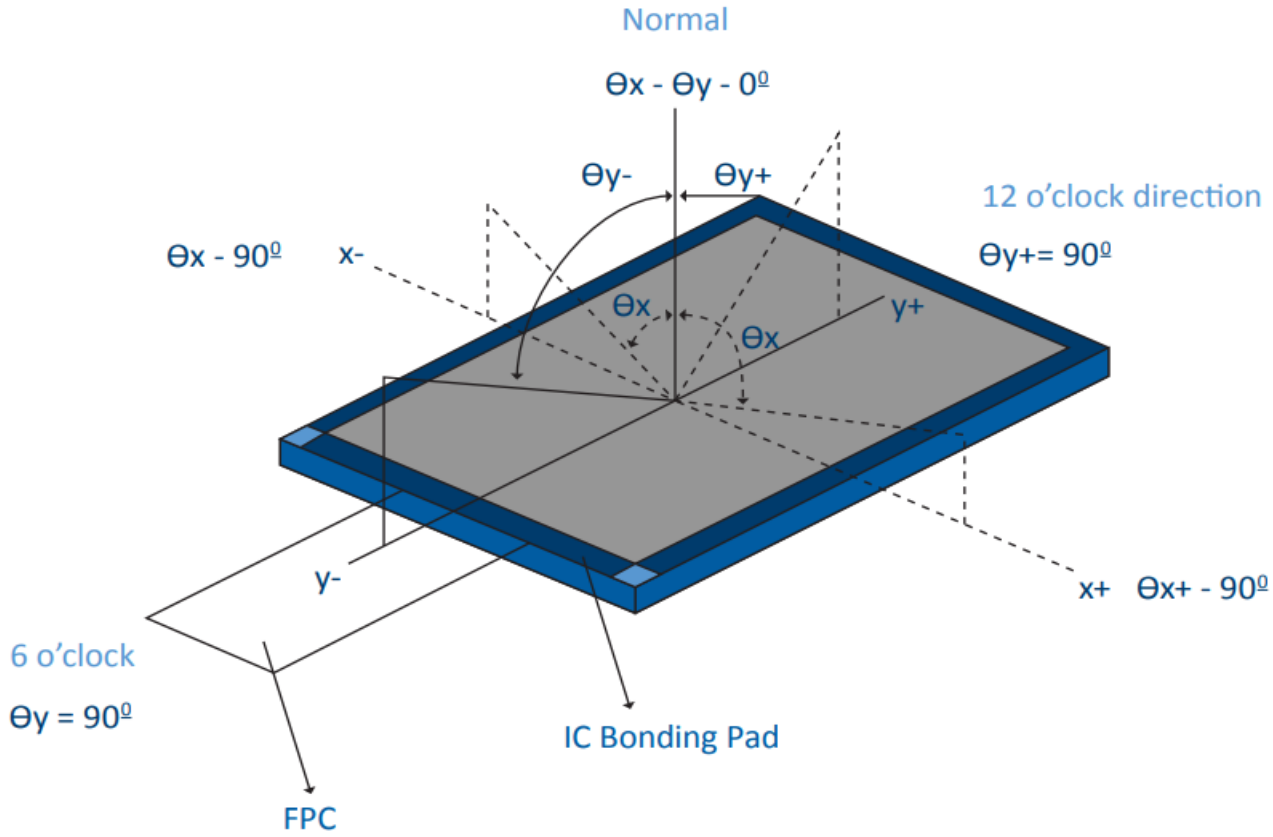
Item		Symbol	Condition	Min	Typ.	Max	Unit	Note
Contrast Ratio		CR	θ=0 Normal viewing angle	--	500	--	%	(2)
Response Time	Rising	TR+TF		--	20	40	msec	(4)
	Falling							
Color Gamut		S(%)		57	60	--	%	(5)
Cross Talk		Ct		--	--	2	%	
Transmittance		Trans		--	5.5	--	%	
Color Filter Chromaticity	White	W_X		0.292	0.307	0.322		(5)(6)
		W_Y		0.312	0.327	0.342		
	Red	R_X		0.609	0.624	0.639		
		R_Y		0.316	0.331	0.346		
	Green	G_X		0.281	0.296	0.311		
		G_Y		0.562	0.577	0.592		
	Blue	B_X		0.128	0.143	0.158		
		B_Y		0.094	0.109	0.124		
Viewing angle	Hor.	ΘL	CR≥10	--	60	--	degree	(1)(6)
		ΘR		--	60	--		
	Ver.	ΘT		--	70	--		
		ΘB		--	70	--		
Option View Direction		6:00 o'clock						(1)

Note: Ambient temperature =25˚C. To be measured with a viewing cone of 2˚ by Topcon luminance meter BM-5A. To be measured with Otsuta chromacity meter LCF-2100M, CF only measured under C light simulation. CTC shipping status is cell without polarizer. Transmittance of specification is cell with polarizer. The tolerance of transmittance is ±10%.

Optical Specification Reference Notes:

(1) Definition of Viewing Angle: The viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3,9 o'clock direction and the vertical or 6,12 o'clock direction with respect to the optical axis which is normal to the LCD surface.

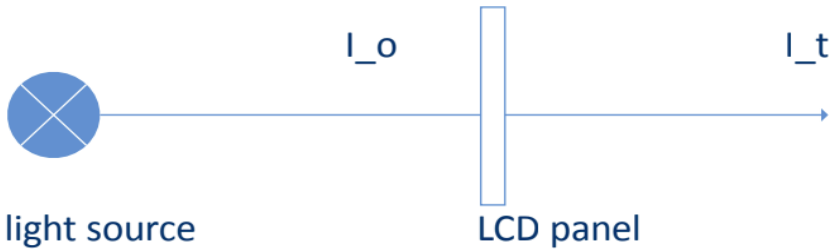




(2) Definition of Contrast Ratio (Cr): measured at the center point of panel. The contrast ratio (Cr) measured on a module, is the ratio between the luminance (Lw) in a full white area (R=G=B=1) and the luminance (Ld) in a dark area (R=G=B=0).

$$Cr = \frac{Lw}{Ld}$$

(3) Definition of transmittance (T%): The transmittance of the panel including the polarizers is measured with electrical driving.

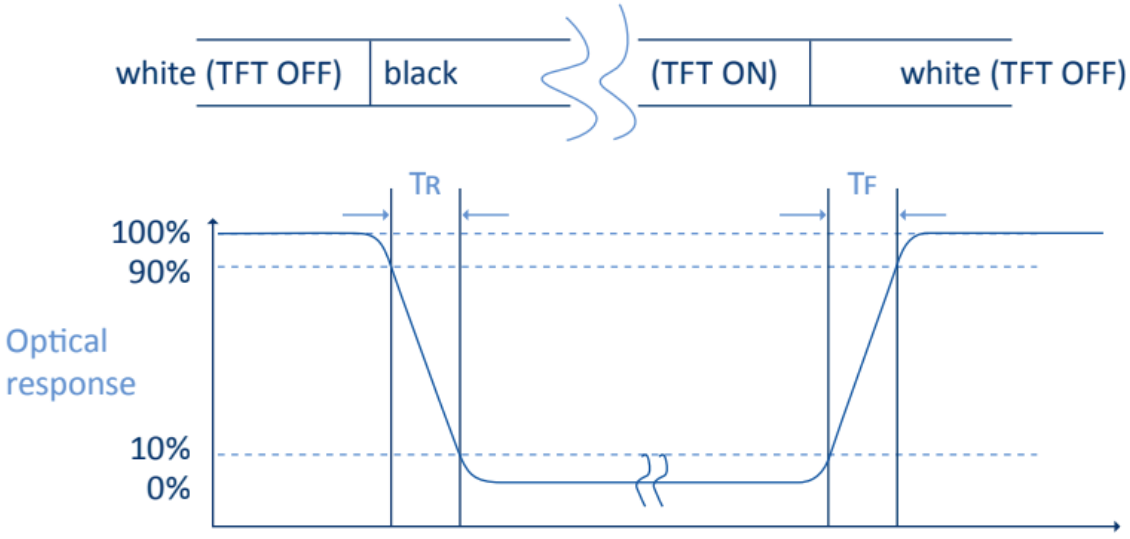


The transmittance is defined as:

$$Tr = \frac{It}{Io}\ x\ 100\%$$

Io = the brightness of the light source.
It = the brightness after panel transmission

(4) Definition of Response Time (Tr, Tf): The rise time 'Tr' is defined as the time for luminance to change from 90% to 10% as a result of a change of the electrical condition. The fall time 'Tf' is defined as the time for luminance to change from 10% to 90% as a result of a change of the electrical condition.



(5) Definition of Color Gamut: Measuring machine CFT-01. NTSC's Primaries: R(x,y,Y),G(x,y,Y), B(x,y,Y). FPM520 of Westar Display Technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics. The color chromaticity shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

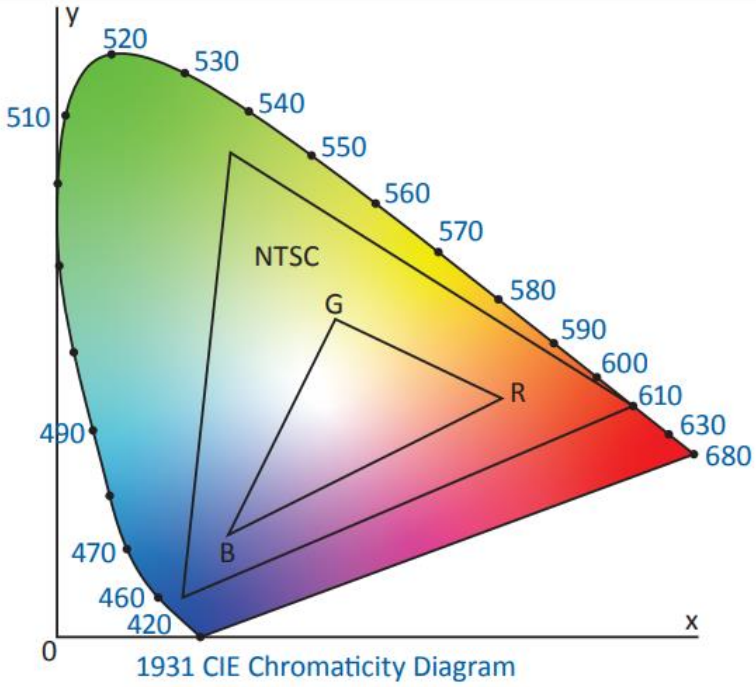
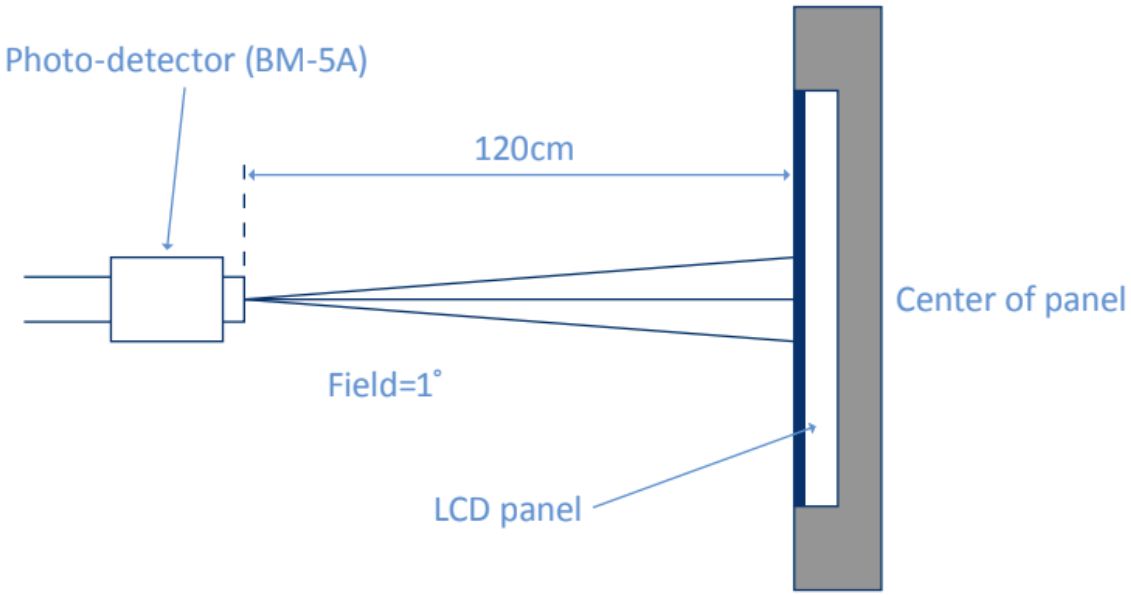


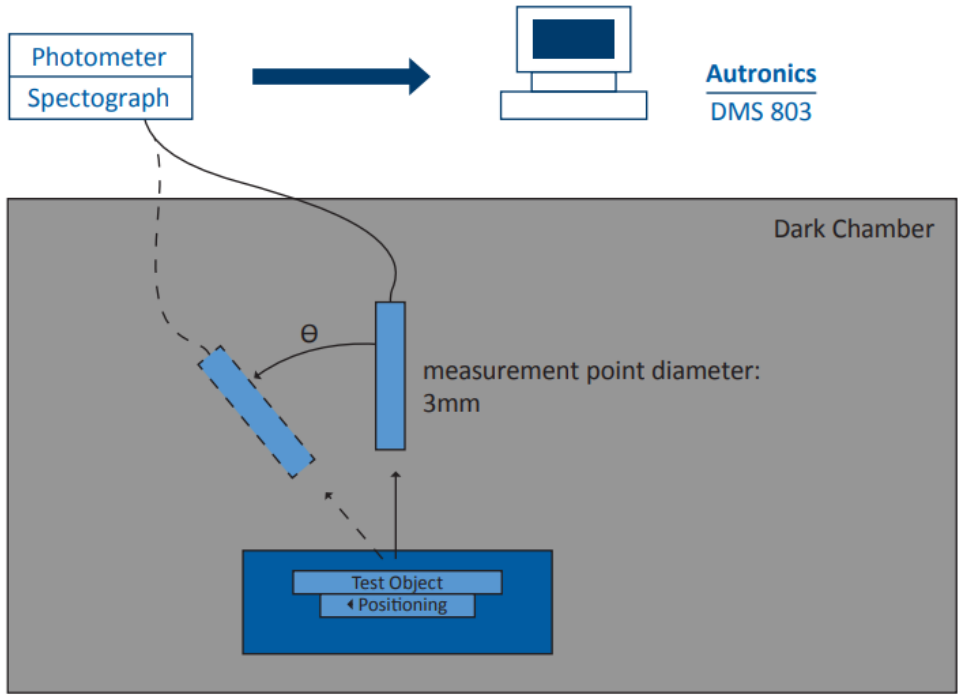
Fig. 1931 CIE chromacity diagram

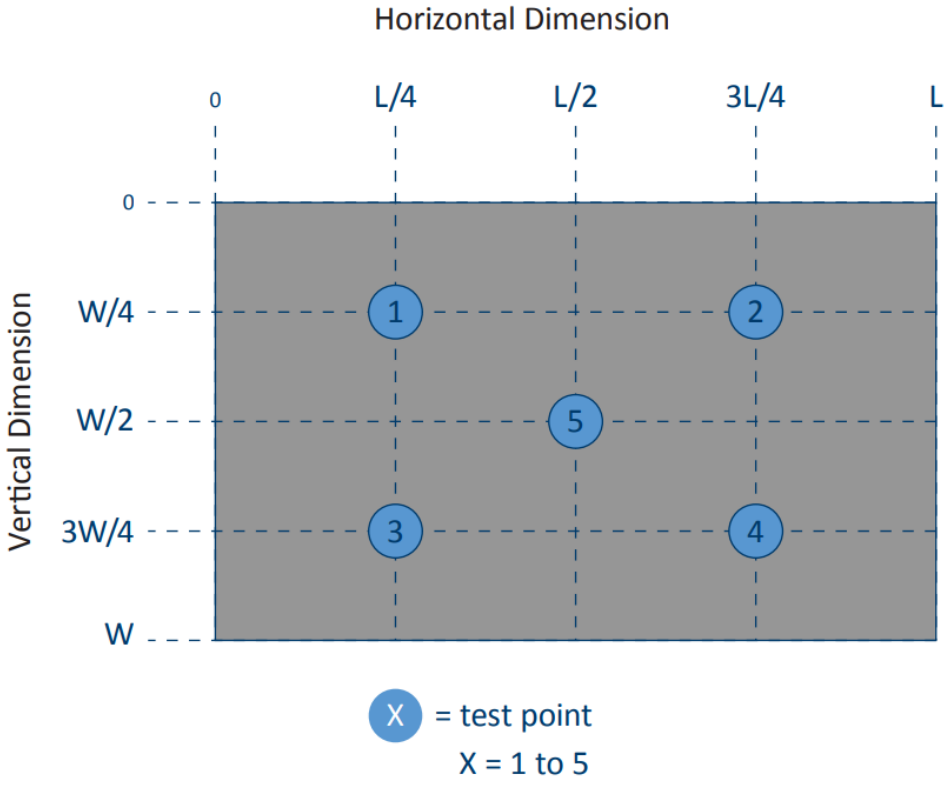
$$\text{Color gamut: } S = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}} \times 100\%$$

(6) Definition of Optical Measurement Setup:



(6) Optical Measurement Setup Continued:
The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 20 minutes.





5. TFT Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 ˚C, VSS=0V)

Characteristics	Symbol	Min	Max	Unit
Digital Supply Voltage	VDD	-0.3	4.6	V
Digital Interface Supply Voltage	VDDIO	-0.3	4.6	V
Operating Temperature	TOP	-20	+70	℃
Storage Temperature	TST	-30	+80	℃

NOTE: If the absolute maximum rating of the above parameters is exceeded, even momentarily, the quality of the product may be degraded. Absolute maximum ratings specify the values which the product may be physically damaged if exceeded. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min	Typ.	Max	Unit	Note
Digital Supply Voltage	VDD	2.4	3.3	4.2	V	
Digital Interface Supply Voltage	VDDIO	1.65	3.3	4.2	V	
Normal Mode Current Consumption	IDD	--	8	--	mA	
Level Input Voltage	VIH	0.7VDDIO	--	VDDIO	V	
	VIL	GND	--	0.3VDDIO	V	
Level Output Voltage	VOH	0.8VDDIO	--	VDDIO	V	
	VOL	GND	--	0.2VDDIO	V	

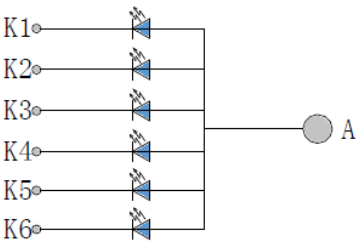
5.3 LED Backlight Characteristics

The backlight system is edge lighting type with 6 chips LED.

Item	Symbol	Min	Typ.	Max	Unit	Note
Forward Current	I_F	85	90	--	mA	
Forward Voltage	V_F	--	3.2	--	V	
LCM Luminance	LV	--	250	--	cd/m2	Note 3
LED lifetime	Hr	50000	--	--	hour	Note1 & 2
Uniformity	AVg	80	--	--	%	Note 3

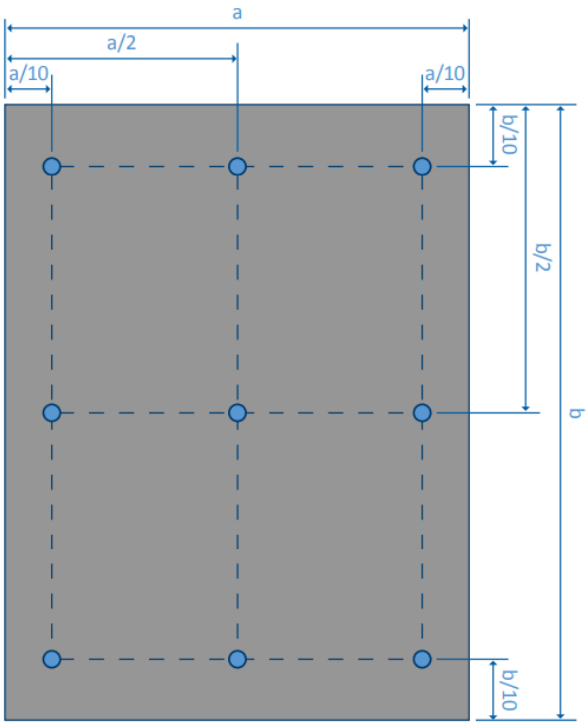
Note 1: LED lifetime (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25 ±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The "LED lifetime" is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL = 90mA. The LED lifetime could be decreased if operating IL is larger than 90mA. The constant current driving method is suggested.



Backlight LED Circuit

Note 3: Luminance Uniformity of these 9 points is defined as below:



$$\text{Luminance} = \frac{\text{(Total Luminance of 9 points)}}{9}$$

$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points(1-9)}}{\text{maximum luminance in 9 points(1-9)}}$$

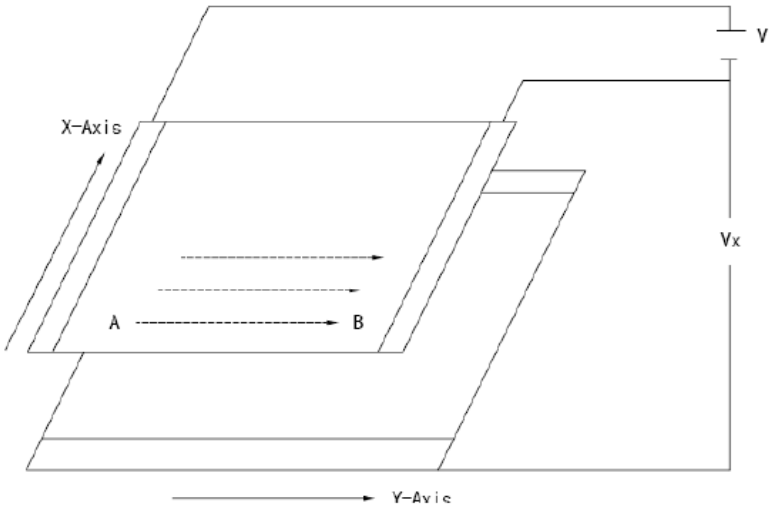
6. TP Feature

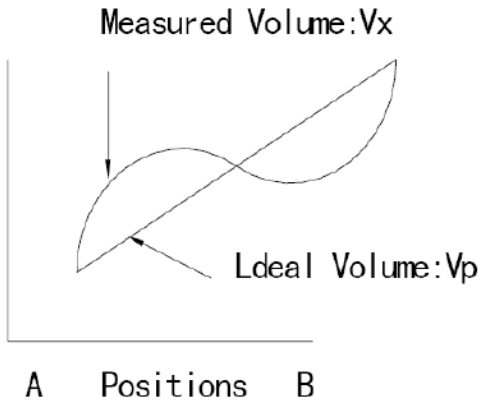
6.1 Conditions of Use and Storage

Item	Condition	Note
Temperature range upon operation	Humidity: 20%-90% non-dew, condensation -20℃~70℃	In a simple substance
Temperature range upon storage	Humidity: 20%-90% non-dew, condensation -30℃~80℃	In a simple substance

6.2 Electrical Property

Item	Value	Note
Maximum voltage	DC 5V	
Resistance between terminal	X direction (film side): 200-600 Ω	
	Y direction (glass side): 300-900 Ω	
Insulation resistance	DC 25V, 20MΩ or above	Connect X + ~X and Y+ ~Y, apply 25V DC Between X and Y for perform measurements
Chattering	10ms or below	
Rating	Voltage is 5V DC	





6.3 Mechanical Property

Item	Value		Note
Input method	Used of an exclusive pen or finger		
Load upon operation	Exclusive pen	60-100g or below	Operation and measurement with a pen must be carried out under the following tip conditions: Stylus pen material: POM (ployacetal) Tip: Diameter 3.0mm, SR 0.8 mm
	Finger	60-100g or below	Operation and measurement with a pen must be carried out under the following tip conditions: Stylus pen material: Silicon rubber (Hardness: 30°Hs) Tip: Diameter 12.0mm, SR 12.5 mm
Surface hardness	Pencil hardness: 3H or above		It complies with the way of test method JIS K5400

6.4 Optical Property

Item	Performance	Note
Total light transmittance	80% or above	JIS K7105
Haze	5% or below	JIS K7136
Film specification	Polished type with hard coated surface	

7. AC Characteristics

7.1 Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080 system)

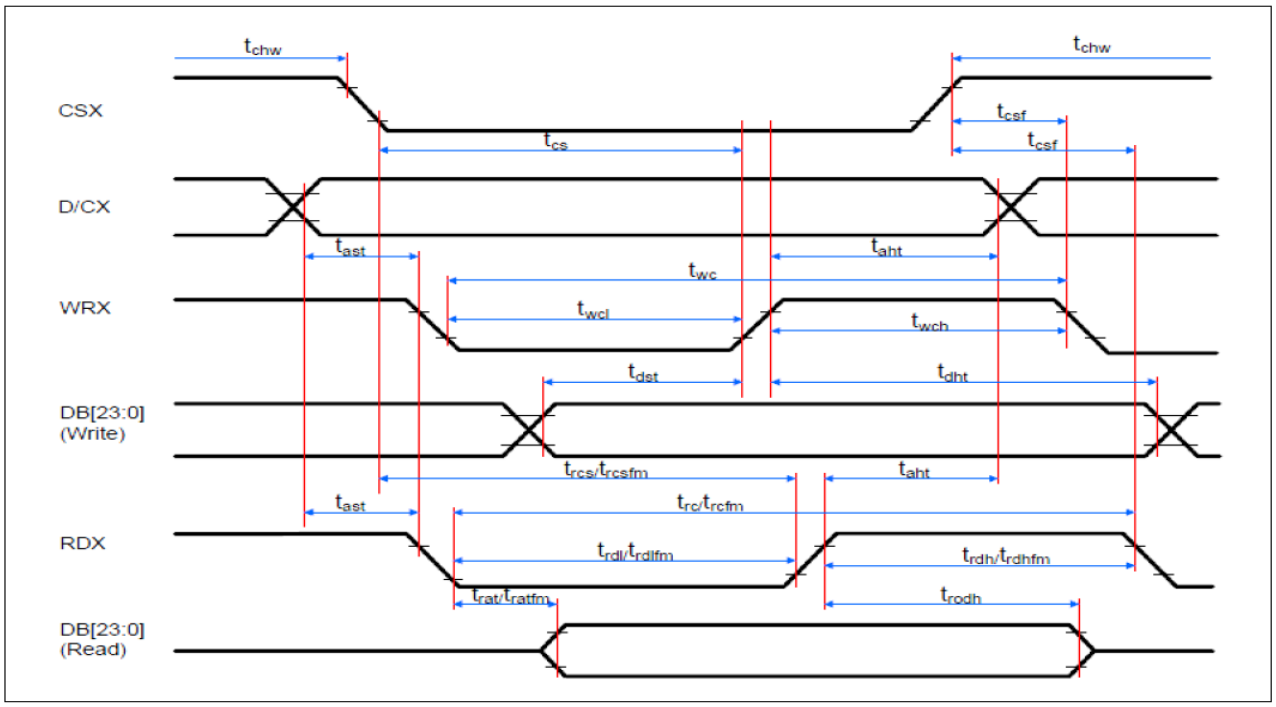
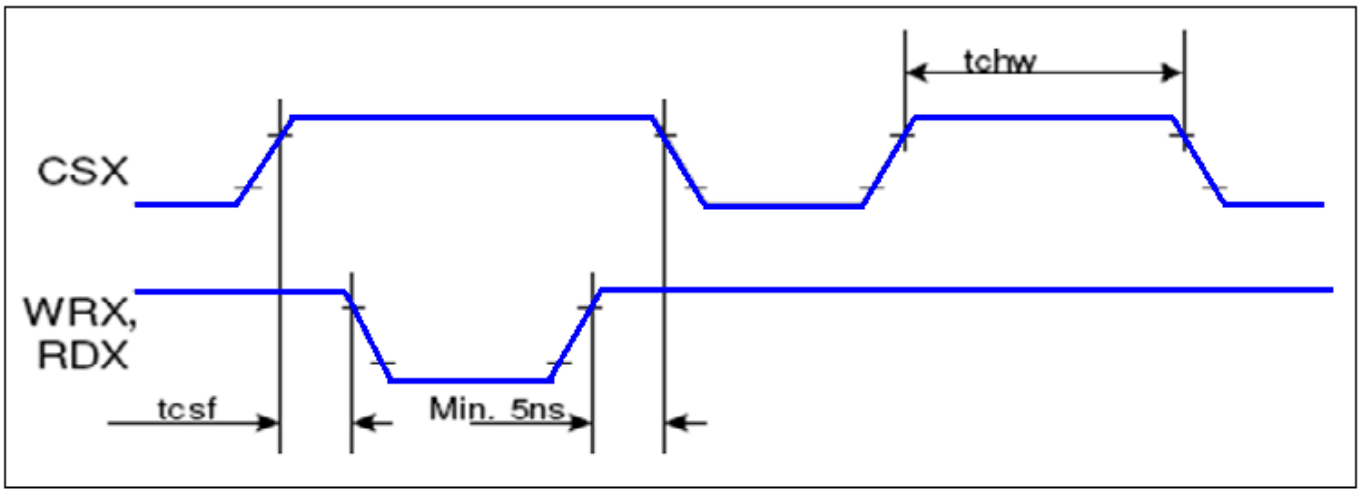


Figure 7.1: Parallel Interface Timing Diagram

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	tast	Address setup time	0	-	ns	
	that	Address hold time (Write/Read)	0	-	ns	
CSX	tchw	CSX "H' pulse width	0	-	ns	
	tcs	Chip select setup time (Write)	15	-	ns	
	trcs	Chip select setup time (Read ID)	45	-	ns	
	trcsfm	Chip select setup time (Read FM)	355	-	ns	
	tcsf	Chip select wait time (Write/Read)	0	-	ns	
WRX	twc	Write cycle	40	-	ns	
	twrh	Write control pulse H duration	15	-	ns	
	twrl	Write control pulse L duration	15	-	ns	
RDX(FM)	trcfm	Read cycle (FM)	450	-	ns	When read from frame memory
	trdhfm	Read control H duration (FM)	90	-	ns	
	trdlfm	Read control L duration (FM)	355	-	ns	
RDX(ID)	trc	Read cycle (ID)	160	-	ns	When read ID data
	trdh	Read control pulse H duration	90	-	ns	
	trdl	Read control pulse L duration	45	-	ns	
DB[23:0} DB[17:0] DB[15:0] DB[8:0] DB[7:0]	tdst	Write data setup time	10	-	ns	For maximum, CL=30pF For minimum, CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

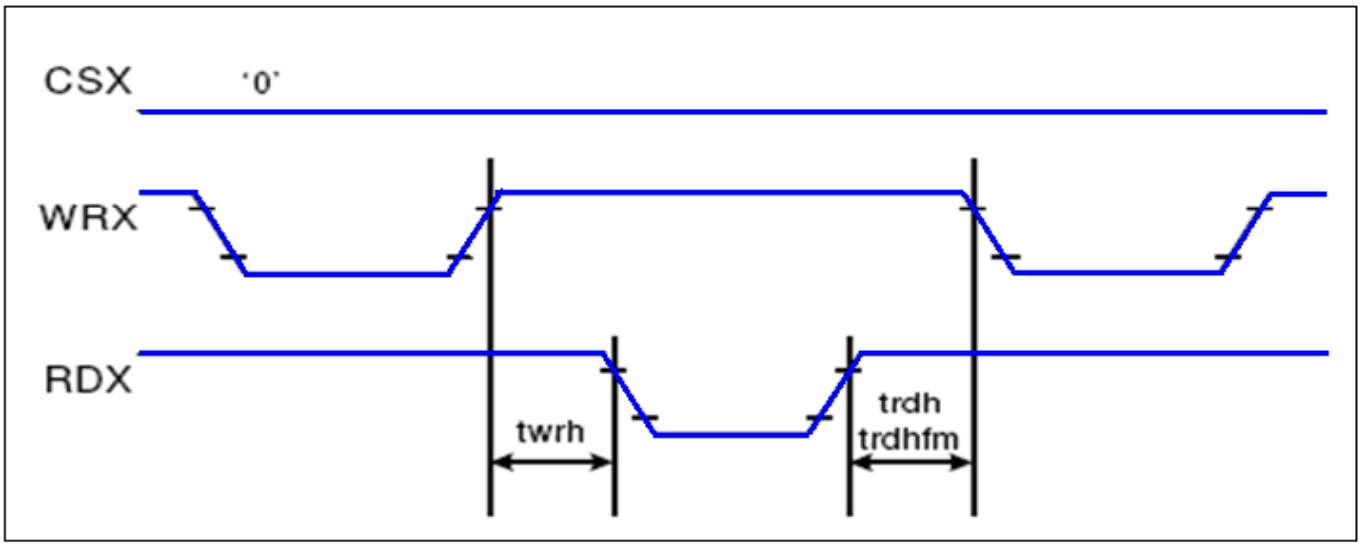
Table 7.1: Parallel Interface Timing Characteristics

CSX timings:

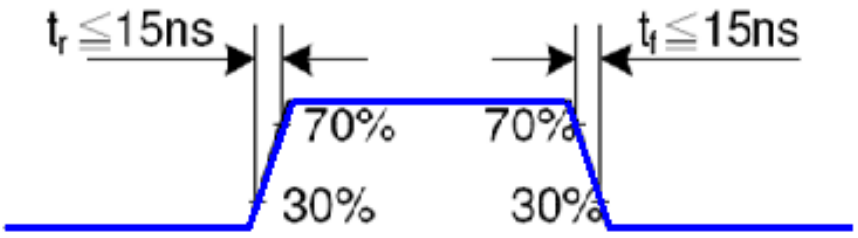


Note: Logic high and low levels are specified as 30% and 70% of IOVCC for input signals.

Write to read or read to write timings:



Note: Ta = -30 to 70 C, IOVCC = 1.65V to 2.8V, VCI = 2.5V to 3.3V, GND = 0V.



7.2 Display Serial Interface Characteristics (3-line SPI system)

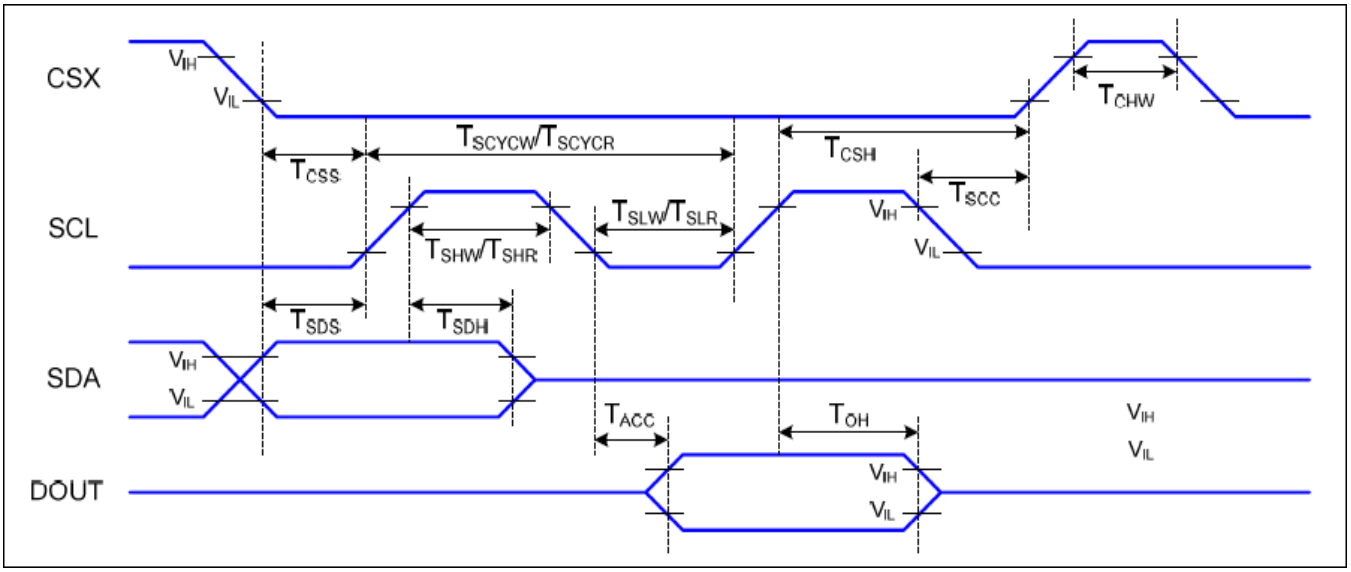


Figure 7.2: 3-line Serial Interface Timing Diagram

VDDI = 1.64 to 3.3V, VDD = 2.4 to 3.3V, AGND=DGND=0V, Ta=-30 to 70 C°

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CS}	SCL-CSX	15		ns	
	T_{CSH}	Chip select hold time (write)	65		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (write)	150		ns	
	T_{SHW}	SCL "H" pulse width (write)	15		ns	
	T_{SLW}	SCL "L" width (write)	15		ns	
	T_{SCYCR}	Serial clock cycle (read)	150		ns	
	T_{SHR}	SCL "H" pulse width (read)	60		ns	
	T_{SLR}	SCL "L" pulse width (read)	60		ns	
SDA/SDI (Input)	T_{SDS}	Data setup time (write)	10		ns	
	T_{SDH}	Data hold time (Write)	10			
SDA/SDO (Output)	T_{ACC}	Access time (read)	10	50	ns	For max CL=30pF
	T_{OH}	Output disable time (read)	15	50	ns	For min CL=8pF

Table 7.2: 3-line Serial Timing Characteristics

Note: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals

7.3 Display Serial Interface Characteristics (4-line SPI serial)

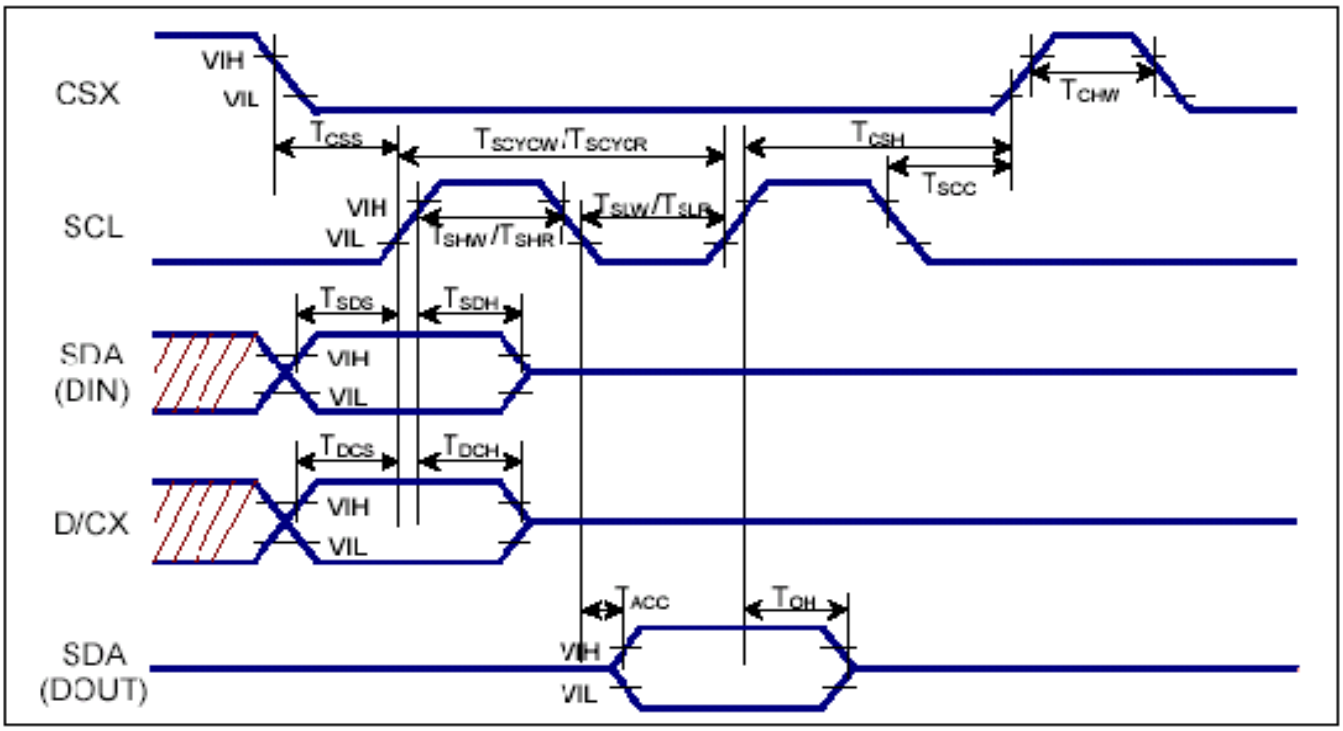


Figure 7.3: 4-line SPI Serial Interface Timing Diagram

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (read)	15		ns	
	T_{CHW}	Chip select “H” pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (write)	50		ns	write command & data ram
	T_{SHW}	SCL “H” pulse width (write)	10		ns	
	T_{SLW}	SCL “L” width (write)	10		ns	
	T_{SCYCR}	Serial clock cycle (read)	150		ns	read command & data ram
	T_{SHR}	SCL “H” pulse width (read)	60		ns	
	T_{SLR}	SCL “L” pulse width (read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time (read)	10	50	ns	For max CL=30pF For min CL=8pF
	T_{OH}	Output disable time	15	50	ns	

Table 7.3: 4-line Serial Interface Timing Characteristics

Note: The rising time and falling time (Tr, Tf) of input signal are specified at 15ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

7.4 Parallel RGB Interface Characteristics

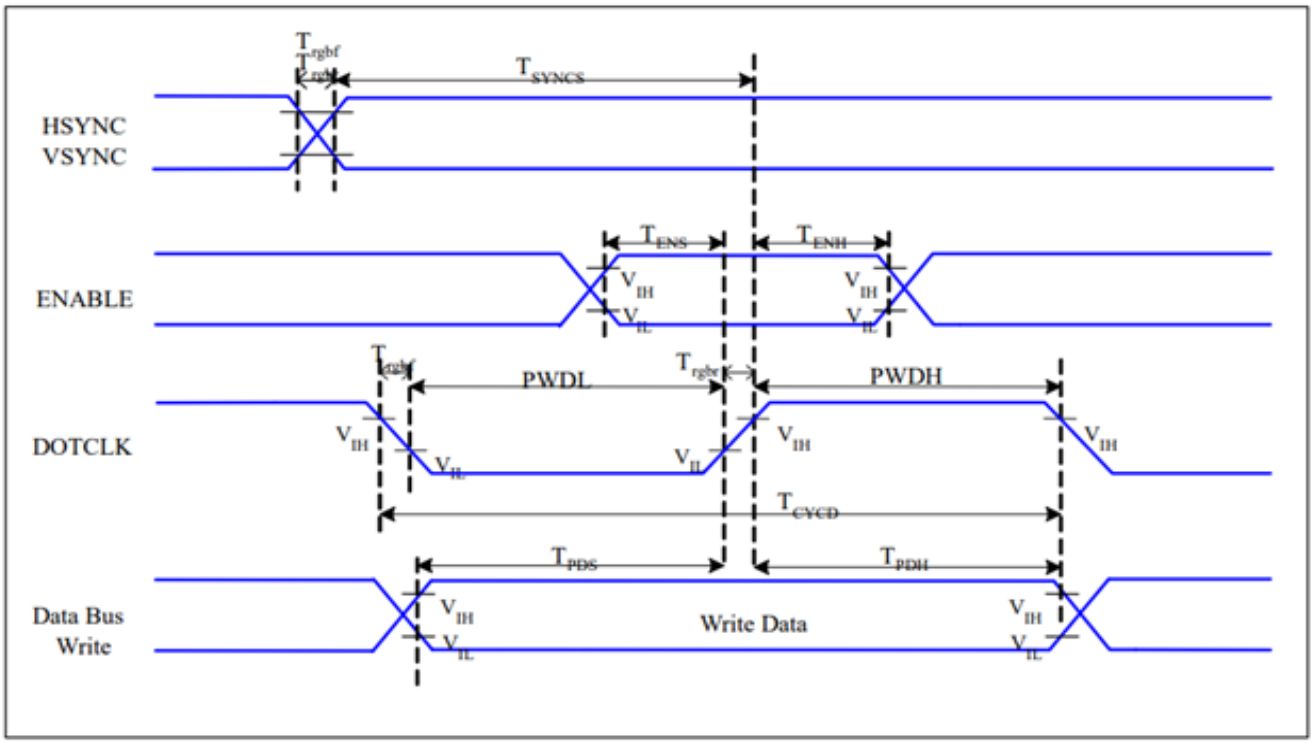
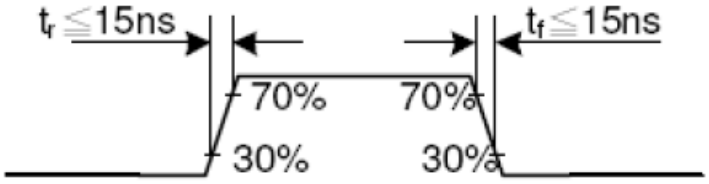


Figure 7.4: Parallel RGB Timing Diagram

Signal	Symbol	Parameter	Min	Max	Unit	Description
HSYNC/ VSYNC	T_{SYNCS}	VSYNC, HSYNC setup time	15	-	ns	16/18/24-bit bus RGB interface mode
	T_{SYNCH}	VSYNC, HSYNC hold time	15			
DE	T_{ENS}	Enable Setup Time	15	-	ns	
	T_{ENH}	Enable Hold Time	15	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	20	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	20	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	50	-	ns	
	T_{RGHR}, T_{RGHF}	DOTCLK, HSYNC, VSYNC Rise/Fall Time	-	15	ns	
D[23:0]	T_{PDS}	Data Setup Time	15	-	ns	
	T_{PDH}	Data Hold Time	15	-	ns	

Table 7.4: Parallel RGB Timing Characteristics



7.5 Reset Timing

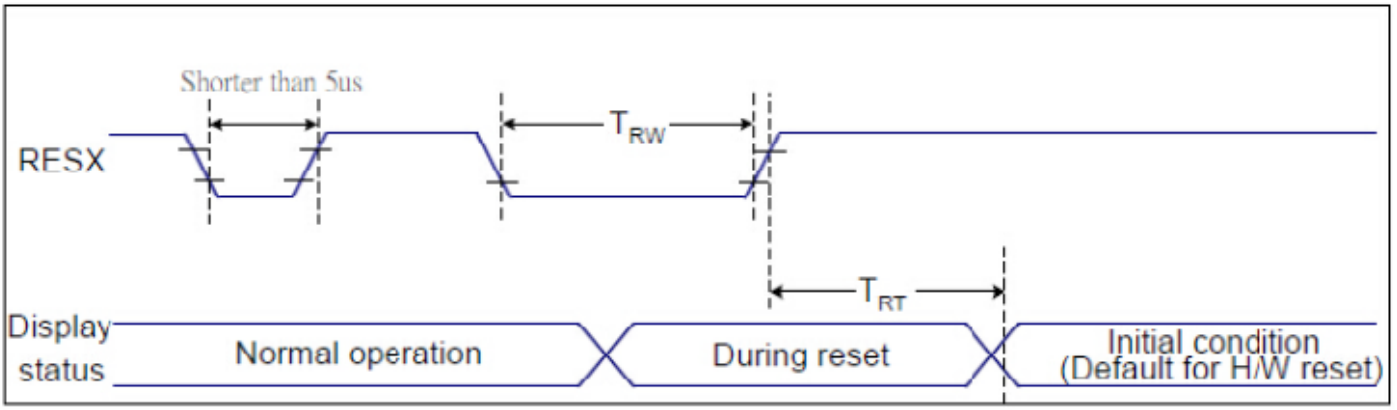


Figure 7.5: Reset Timing Diagram

Related Pins	Symbol	Parameter	Min	Max	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1,5)	ms
				120 (Note 1, 6, 7)	ms

Notes:

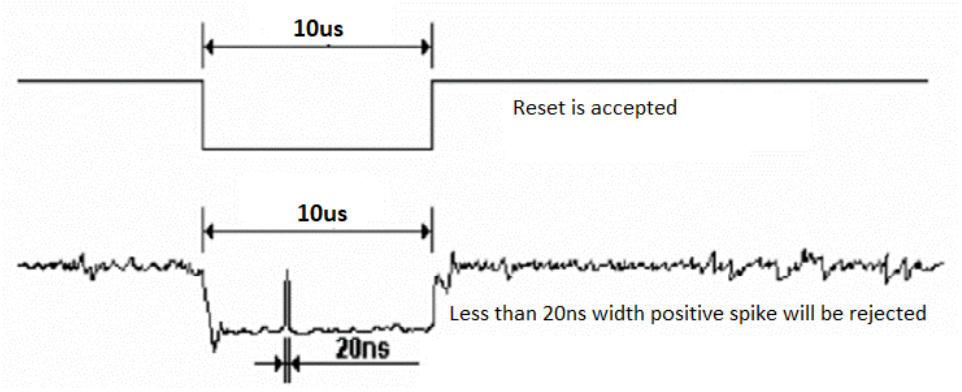
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not because irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9 us	Reset starts

3. During the resetting period, the display will be blanked (the display is entering blanking sequence, which maximum time is 120ms, when reset starts in Sleep Out mode. The display remains the blank state in Sleep in mode) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5ms after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120ms.

8. Cautions and Handling Precautions

8.1 Handling and Operating the Module

1. When the module is assembled, it should be attached to the system firmly. Do not warp or twist the module during assembly work.
2. Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
3. Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
4. Do not allow drops of water or chemicals to remain on the display surface. If you have the droplets for a long time, staining and discoloration may occur.
5. If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
6. The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
7. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
8. Protect the module from static; it may cause damage to the CMOS ICs.
9. Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
10. Do not disassemble the module.
11. Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
12. Pins of I/F connector shall not be touched directly with bare hands.
13. Do not connect, disconnect the module in the “Power ON” condition.
14. Power supply should always be turned on/off by the item Power On Sequence & Power Off Sequence

8.2 Storage and Transportation.

1. Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%
2. Do not store the TFT-LCD module in direct sunlight.
3. The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
4. It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module. In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
5. This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.