4th Generation SiC MOSFET
Half Bridge Evaluation Board
User's Manual

User's Guide

<High Voltage Precautions>

◇Before you start operation!

This document describes only how to handle evaluation boards for **SiC MOSFETs** (**P04SCT4018KE-EVK-001, P05SCT4018KR-EVK-001**).
Please refer to the product specifications for detailed information on schematics, BOM, layout, etc.

In order to ensure safe operation, please read this document thoroughly before using the evaluation board!

Also, depending on the voltage used and the structure of the board,
life-threatening voltages may be generated.
Be sure to strictly observe the precautions in the box below.

<Before Use>

① Make sure that no parts are damaged or missing, for example because the board has been dropped.

② Make sure that no conductive objects have fallen on the board.

③ When soldering the module to the evaluation board, be careful of solder splattering.

④ Make sure that there is no condensation or water droplets on the board.

<During Energization>

⑤ Make sure that no conductive objects come into contact with the board.

⑥ During operation, even a brief accidental contact or discharge due to bringing your hand near the board may result in serious or life-threatening injury.

Never touch the board with bare hands or bring it too close to your hand.
Also, be careful when working with conductive instruments such as tweezers or screwdrivers, as described above.

⑦ If a higher voltage than the rated voltage is applied, the parts may explode depending on the specification conditions such as short circuit. Also consider the danger of parts scattering.

⑧ During operation, be careful of discoloration of the board and components due to heat, liquid leakage, etc., and condensation when evaluating at low temperature.

<After Use>

⑨ The evaluation board may contain a circuit that stores high voltage. Even if the connected power supply circuit is disconnected, it still stores electric charge, so be sure to discharge it after use and confirm that it is discharged before handling.

⑩ Be careful of burns, etc. caused by contact with overheated components.

This evaluation board is to be used in research and development facilities and **can only be used by persons who are authorized to handle high voltage in each facility.** When working with high voltages, it is recommended to install signage such as "high voltage work underway," to use a cover with interlocks, etc., and to wear protective goggles to ensure a safe working environment. Please read the cautionary note on **short circuit protection** for this board at the beginning of this document.

SiC MOSFET Evaluation Board

4th Generation MOSFET Evaluation Board User's Manual

This user guide explains how to use the evaluation board to evaluate 4th Generation SiC MOSFETs.

SiC MOSFETs handle high voltage and high current and need to be evaluated under various conditions to determine the operating conditions for optimizing EMC noise and power supply efficiency. However, creating an appropriate evaluation environment is not an easy task. To solve this problem, we have prepared an evaluation board that allows you to easily set various conditions for evaluating the switching characteristics, so that you can efficiently evaluate SiC MOSFETs.

This user guide explains how to handle the evaluation boards for the TO-247N package and TO-247-4L. For detailed information on product specifications, please refer to "4th generation SiC MOSFET Evaluation Board Product Specifications"

This evaluation board does not have a short circuit protection function for the evaluation device.
Therefore, even with the normal evaluation method, if the usage deviates from the electrical specifications (maximum current, etc.) of the evaluation device selected by the customer, the device may be severely damaged with a popping sound. Therefore, never use the evaluation board in a way that deviates from the specifications of the evaluation device. Also, take precautions to prevent fragments from scattering and use protective equipment in case severe

1. Introduction

Since this board has multiple voltage and signal sources supplied from external sources, be sure to follow the on/off sequence specified below to avoid problems such as destruction.

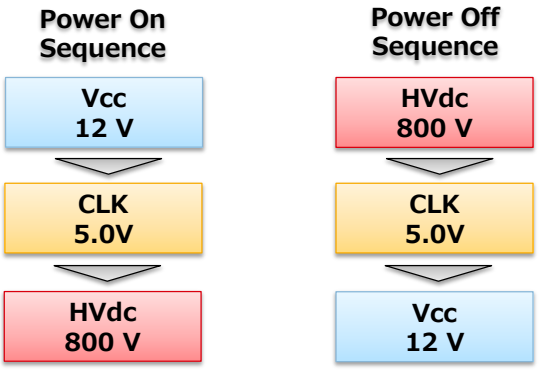


Figure 1 On/Off sequence

In addition, this board is designed with the optimum gate drive circuit for "SCT4018KE" or "SCT4018KR" as a default setting, surely other devices in "TO-247N" or "TO-247-4L" packages can also be mounted and evaluated. In this case, change the gate drive circuit constants according to the characteristics of each device, referring to "4. How to set the gate drive voltage" and "5. How to set the gate resistance".

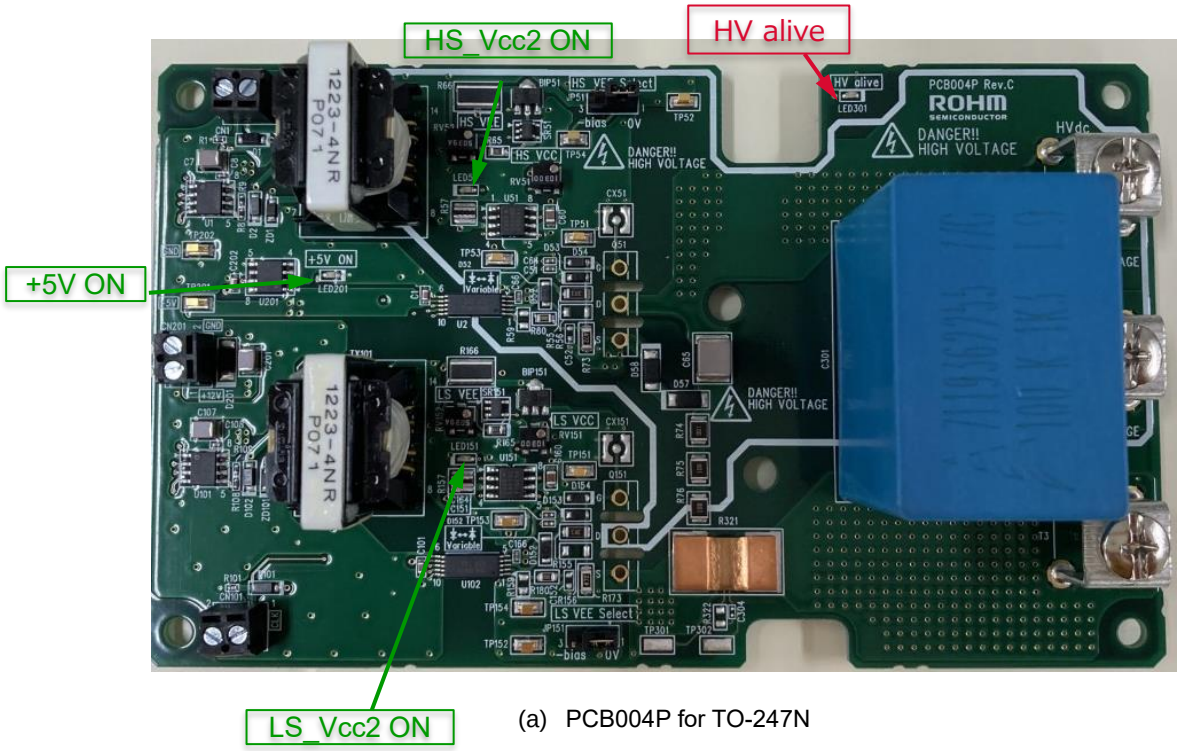
Table.1 shows the lineup and specifications of the 4th generation SiC MOSFET series.

Product Name	V_{DSS}(V)	R_{ON}(Typ.) (mΩ)	I_D (A)	P_D (W)	Tj(Max) (℃)	Package
SCT4045DE	750	45	34	115	175	TO-247N 
SCT4026DE		26	56	176		
SCT4013DE		13	105	312		
SCT4062KE	1200	62	26	115		
SCT4036KE		36	43	176		
SCT4018KE		18	81	312		
SCT4045DR	750	45	34	115		TO-247-4L 
SCT4026DR		26	56	176		
SCT4013DR		13	105	312		
SCT4062KR	1200	62	26	115		
SCT4036KR		36	43	176		
SCT4018KR		18	81	312		

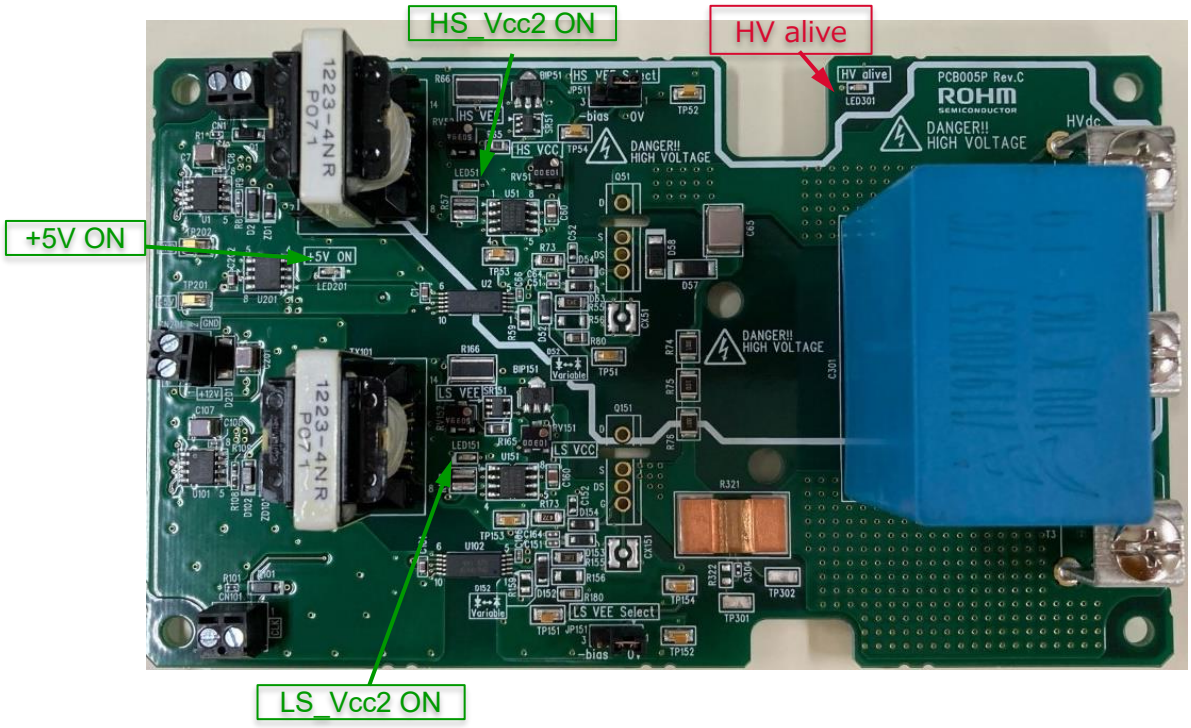
2. LED Display

The board is equipped with a number of LEDs to make it easy to monitor the board's operating status.

The approximate locations of the LEDs are shown in Figure 2 and their details are shown in Table 2.



(a) PCB004P for TO-247N



(b) PCB005P for TO-247-4L

Figure 2. LED Location

Table 2 LED lights and their meanings

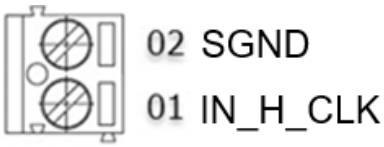
Silkscreen notation	LED	LED lighting	Details
HV alive	Red	Lit	The LED lights up when there is a voltage of 20 V or more in the high-voltage power supply HVdc. Never touch the board when this LED is lit, as it may be lit even when the high-voltage power supply is disconnected.
		Off	HVdc voltage is 20 V or less.
+5V_ON	Green	Lit	Lit during normal operation. When lit, control power (+12 V) is being output.
		Off	No control power is applied.
HS_Vcc2_ON LS_Vcc2_ON	Green	Lit	Lit during normal operation. The gate drive isolated power supply is rising normally.
		Off	No gate drive isolated power supply is being output.

3. Connector Pin Assignment

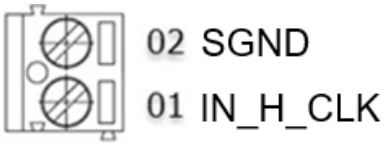
Connector pin assignments are shown in Figure 3.

The definitions of each signal and power pin are shown in Table 3 and Table 4.

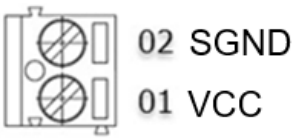
(1) CN1 (H-side signal input connector)



(2) CN101 (L-side signal input connector)



(3) CN201 (Control power supply power connector)



(4) JP51 (H-side negative bias/0 V switching connector)

(5) JP151 (L-side negative bias/0 V switching connector)

Figure 3 Connector pin assignment (Top view)

Table 3 Definition of power supply pins

Power supply pin	Signal	Details
T1	HVdc	High-voltage input pin The input pin during buck or inverter operation, but the output pin during boost operation.
T2	Vsw	Power source pin of H-side MOSFET and drain pin of L-side MOSFET This pin is connected in the board and cannot be disconnected.
T3	PGND	Power GND pin Connected to SGND on the input signal side.

Table 4 Definition of signal lines

Connector	Pin No.	Signal	I/O	Details
CN1	01	IN_H_CLK	I	Signal to turn on/off the H-side MOSFET. Turns on when at "H" level. When open, it is pulled down with a 2.2 kΩ resistor.
	02	SGND	--	Input signal side GND. Completely separated from the DUT side GND.
CN101	01	IN_L_CLK	I	Signal to turn on/off the L-side MOSFET. Turns on when at "H" level. When open, it is pulled down with a 2.2 kΩ resistor.
	02	SGND	--	Input signal side GND.
CN201	01	Vcc	--	Power supply pin for driver IC and internal control. The gate drive power supply is generated internally from this power supply.
	02	SGND	--	Input signal side GND.
JP51	01	SOURCE_HS	--	PCB004P: SOURCE signal of H-side DUT. PCB005P: DRIVER SOURCE signal of H-side DUT.
	02	GND2_HS	--	GND2 signal of H-side driver IC.
	03	VEE_HS	--	H-side negative bias power supply.
JP151	01	SOURCE_LS	--	PCB004P: SOURCE signal of L-side DUT. PCB005P: DRIVER SOURCE signal of L-side DUT.
	02	GND2_LS	--	GND2 signal of L-side driver IC.
	03	VEE_LS	--	L-side negative bias power supply.

4. How to Set the Gate Drive Voltage

The gate drive voltage is supplied by an isolated flyback power supply mounted on-board. This flyback power supply uses a photo-coupler-less control IC (BD7F200EFJ) manufactured by ROHM, and is equipped with transformers that output positive and negative drive voltages on the HS and L-sides, respectively.
Figure 4 shows the layout of the on-board power supply.

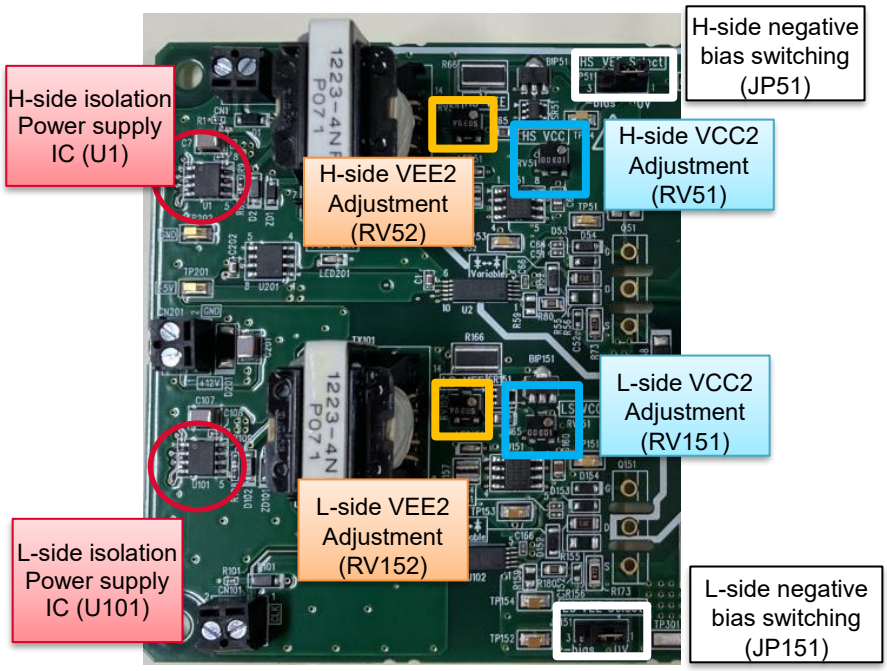


Figure 4 Gate power supply configuration (Top view of PCB004P)

4.1 How to adjust the positive bias (VCC2)

The transformer (TX1, TX101) outputs of the isolated flyback power supply have a positive voltage and a negative voltage. VCC2, which is the drive voltage (positive bias) of the MOSFET, is generated from the transformer positive output through LDO, and the output voltage of LDO can be adjusted by the variable resistors RV51 and RV151. Rotating the variable resistors clockwise increases the output voltage.

4.2 How to adjust the negative bias (VEE2)

The negative bias VEE2, which is the bias voltage when the MOSFET is off, is adjusted from the negative output of transformers TX1 and TX101 by the shunt regulators SR1 and SR101 (TIV431 manufactured by TI) and by the variable resistors RV51 and RV151 can be set in the range of -4.5 V to -2 V. VEE2 is supplied via the negative bias switching pins JP51 and JP151 to select between zero bias and VEE2 bias. The setting method is shown in Table 5.

Table 5 Negative bias (VEE2) setting method

Connector	Pin No.	Signal	Setting method
JP51 JP151	01	SOURCE DRIVER_SOURCE	Pin 1-2 connection: 0 V bias setting
	02	GND2	
	03	VEE	Pin 2-3 connection: Negative bias setting

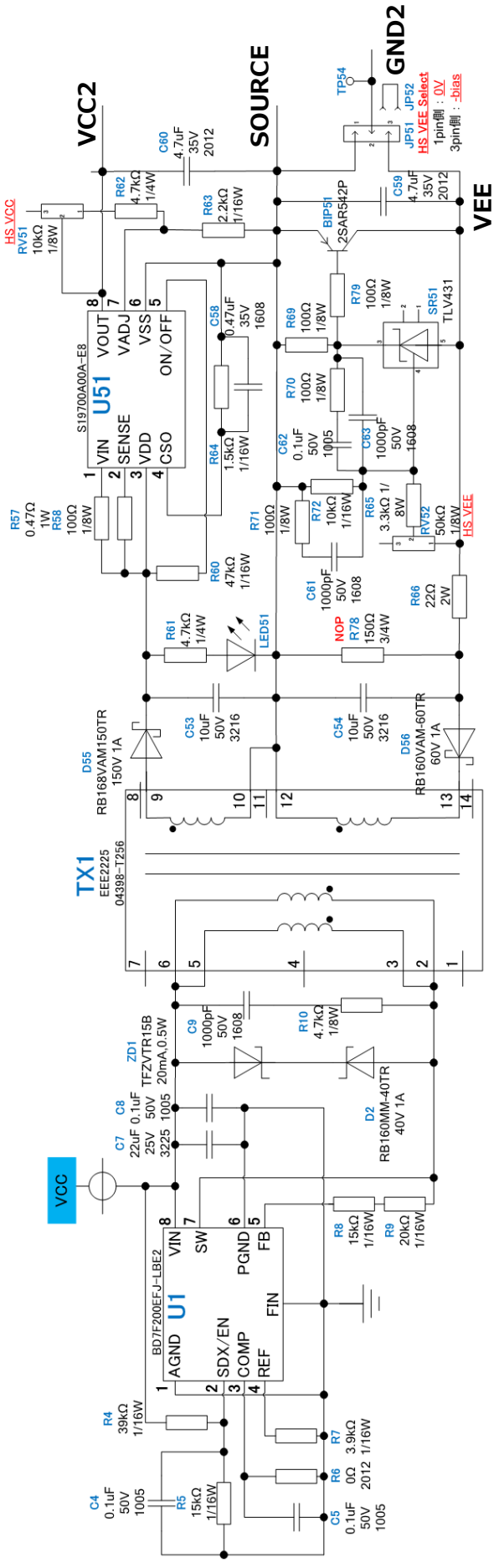


Figure 5 Gate drive power supply circuit (HS-side)

5. How to Set the Gate Resistance

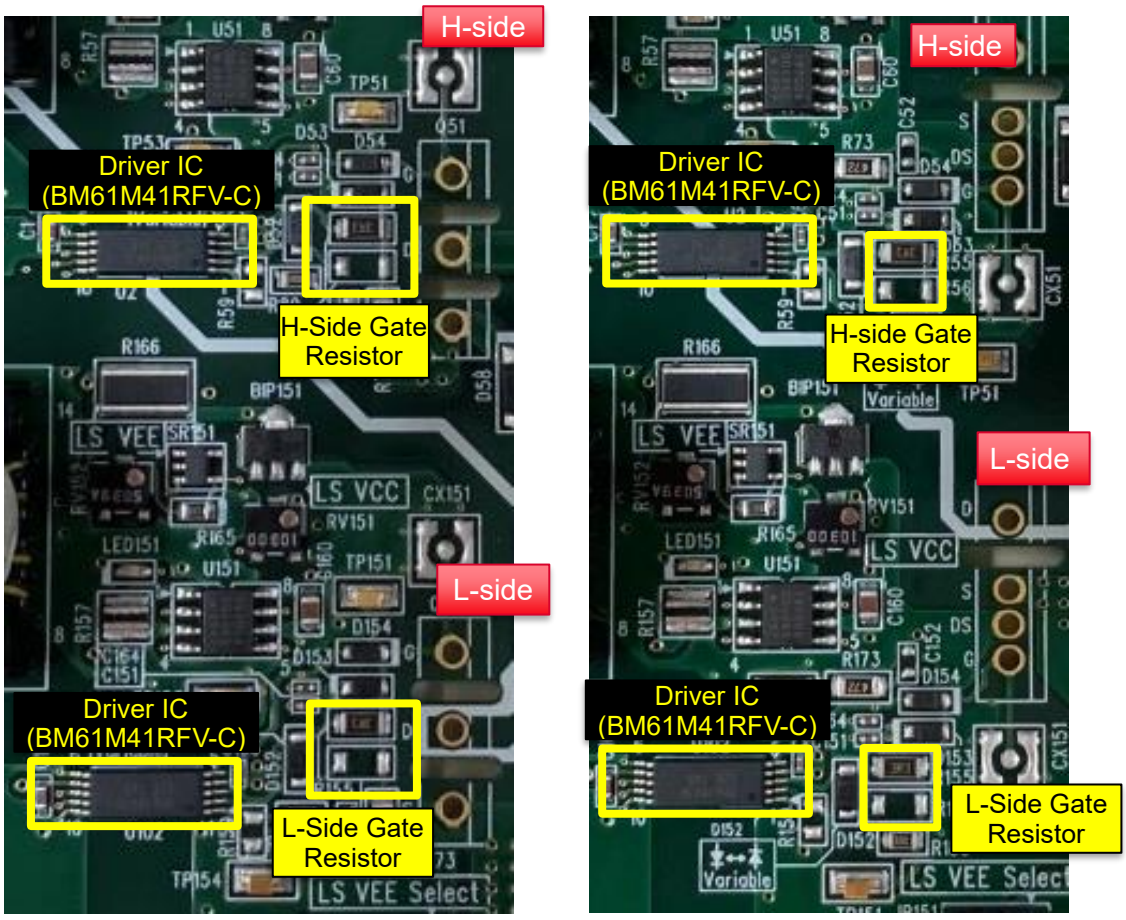
A gate resistor is provided to adjust the switching speed of the MOSFET, and diodes (D52, D152) are connected in order to set the turn-off side low, so that the switching speed of turn-on and turn-off can be adjusted separately.

Turn-on: H-side R55
L-side R155
Turn-off: H-side R56, D52
L-side R156, D152

Figures 6 (a) and (b) show the mounted state of the gate drive circuits of TO-247N and TO-247-4L, respectively, and Figure 7 shows the circuit diagram of TO-247N.

The output signal of the ROHM MOSFET driver IC (BM61M41RFV-C) directly drives the MOSFET via the gate resistor. Since the pattern inductance of the driver circuit affects the surge voltage characteristics of the gate-source signal, it is recommended to keep the wiring length as short as possible, so the circuit is composed of a minimum number of adjustment components.

Since the pin assignment of the gate pin is different between TO-247N and TO-247-4L, the board layout is optimized for each package.



(a) For TO-247N (PCB004P) (b) For TO-247-4L (PCB005P)

Figure 6 Gate drive circuit mounted state

In the default setting, the turn-on and turn-off adjustment resistors have the same circuit configuration and are adjusted by R55. However, if you want to set individual switching speeds for turn-on and turn-off, mount R56 and transmit the drive signal to the MOSFET through resistor R55 for turn-on, and through D52 and R56 for turn-off. In this case, the gate resistor R55 is used for turn-on, and R55 // R56 are connected in parallel for turn-off, resulting in faster turn-off.

Note that the footprint of diode D52 is for the anode and cathode, so it can be mounted in reverse. If the anode is connected to the OUT pin of the driver IC (U2), the turn-on speed can be increased, so it can be used in different ways depending on the characteristics of the device used.

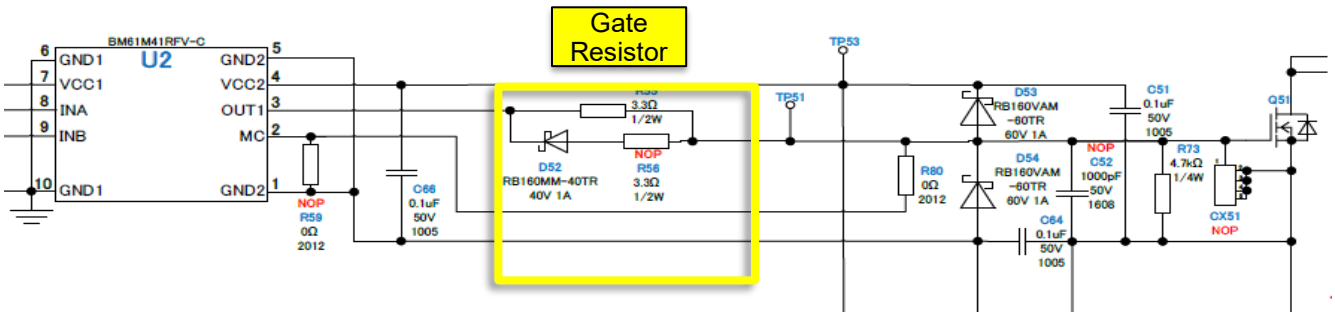
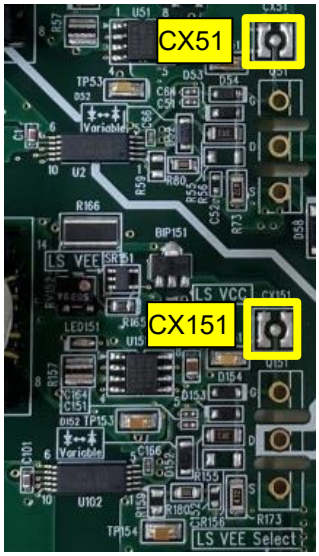


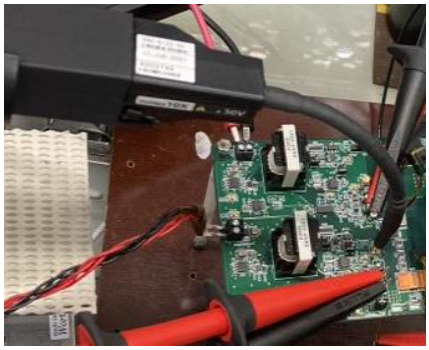
Figure 7 Gate driver circuit (PCB004P)

6. Gate-source voltage measurement using an optical isolation probe

This evaluation board has patterns CX51 and CX151 near the gate terminals at the H-side and L-side DUT, respectively, and by mounting the connectors, gate-source voltage measurement using an optical isolation probe can be performed. By using an optically isolated probe, interference from common-mode noise can be removed and more accurate waveforms can be obtained.



(a) Connector mounting pattern



b) Measurement using an optical isolation probe

(c) Probe connections

Figure 8. Measurement method with Coaxial type shunt resistor

7. How to Measure the Device Current

7.1 Measurement with a Rogowski-type current probe

This evaluation board has one through-hole (without plating) on each of the HS and L-sides, and a notch on the edge of the board, so that the current flowing to each device can be easily measured using a Rogowski-type current probe. The H-side can measure the current at the drain pin, and the L-side can measure the current at the power source side. Figure 9 shows the appearance of the probe-related connections during measurement, and the enlarged photo shows the attachment of the current probe.

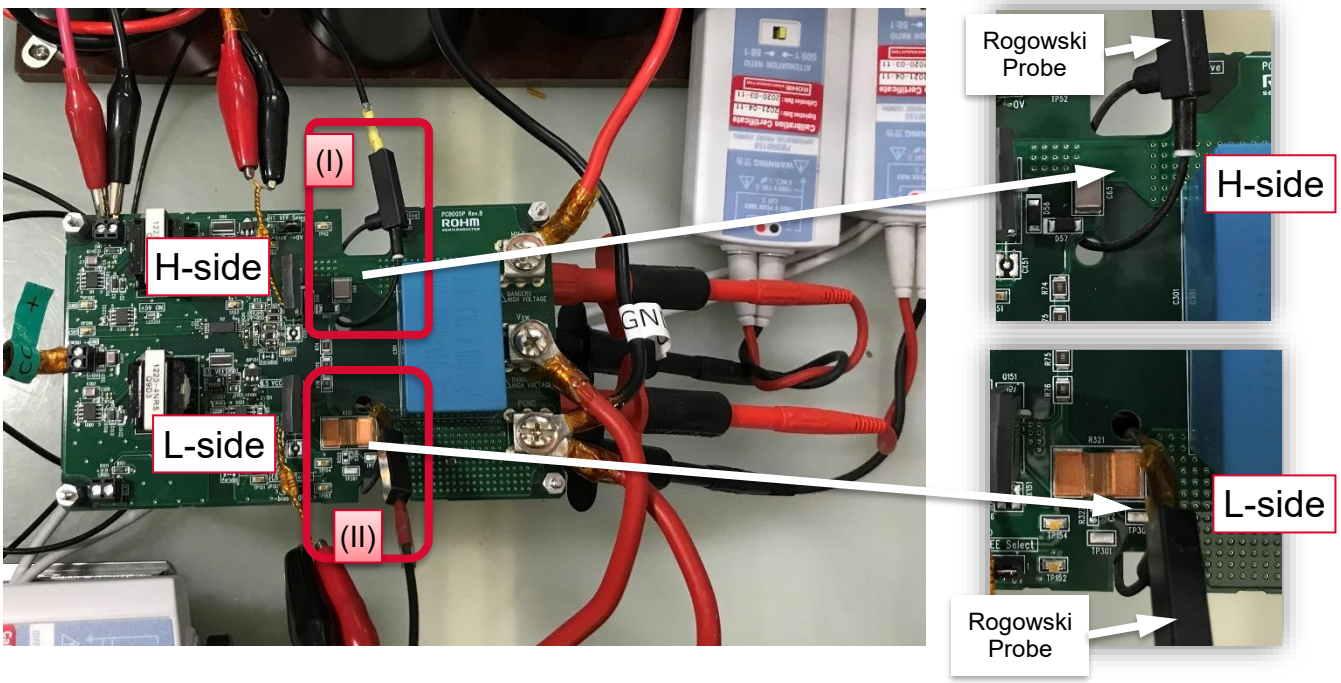


Figure 9 Current measurement with a Rogowski-type current probe (PCB005P)

The head of the Rogowski-type current probe is available in various sizes, and the applicable head is shown in Figure 10, with a diameter of 25 mm to 30 mm and a wire diameter of 3 mm or less.

Figure 10 Applicable head part of Rogowski-type current probe

7.2 Measurement with a coaxial-type shunt resistor

Rogowski-type current probes can be used for measurement without breaking up the current path during measurement, so that waveforms can be observed while reproducing the circuit used in the device. On the other hand, the frequency band of the measurement is not very wide.

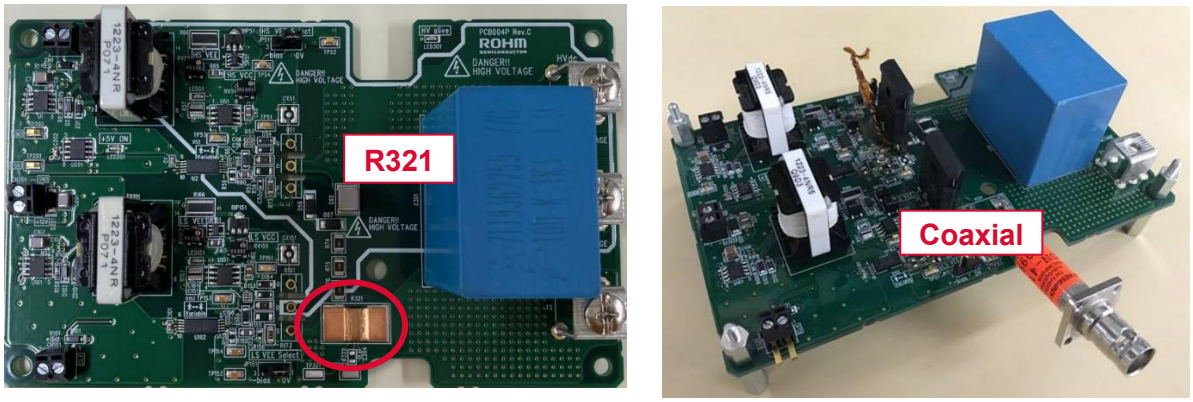
In addition to the Rogowski-type current probe, there are other methods for observing current waveforms, such as using a clamp-type current probe or a shunt resistor, and it is necessary to select the measuring instrument that matches the measurement conditions. Clamp-type current probes are not recommended because they require an extension of the wiring to attach the probe, which affects the switching characteristics of the DUT to some extent. In addition, general shunt resistors generate a large amount of noise due to their own package inductance, making it impossible to accurately measure the current waveform during switching. Therefore, a coaxial-type shunt resistor that can measure the rise in current at the ns level should be used to measure the switching characteristics of the DUT.

Table 6 shows a comparison of the characteristics of a general Rogowski-type current probe and a coaxial-type shunt resistor. While the Rogowski-type has a measurement bandwidth of several tens of MHz, the coaxial type supports up to several GHz.

Table 6 Comparison of the characteristics of a Rogowski-type current probe and a coaxial-type shunt resistor

	Rogowski			Coaxial		
Model (Manufacturer)	SS-285A (IWATSU)	CWT3 (PEM)	TRCP0600 (Tektronix)	SDN-414-01 (T&M Research)	SDN-414-025 (T&M Research)	SDN-414-10 (T&M Research)
HF frequency	30MHz	16MHz	30MHz	400MHz	1200MHz	2000MHz
di/dt or rise time (Peak Value)	4A/ns (N/A)	4A/ns (40A/ns)	N/A	1ns	0.3ns	0.18ns

This evaluation board has a layout that allows measurement with coaxial-type shunt resistors. Remove the resistor R321 (0.1 mΩ) shown in Figure 11(a), disconnect the source line of the lower arm, solder the coaxial-type shunt resistor as shown in (b), and measure the source current of the lower arm DUT. At that time, the GND side of the coaxial-type shunt resistor should be the source side of the DUT, and the GND of the coaxial-type shunt resistor (GND in the oscilloscope) should be based on the source side of the DUT. This is to prevent mismatch of the GND level when measuring the gate-source voltage V_{GS} of the lower arm DUT with a general passive probe.



(a) R321 mounting position (b) Replaced with coaxial-type shunt resistor

Figure 11 Measurement method with coaxial-type shunt resistor

8. How to Mount the Heat Sink

When performing power conversion of several kW using this board, such as when taking efficiency measurements based on the power supply topology, cooling by a heat sink or similar is essential because the power consumption of the device itself reaches several tens of Watts. To install a heat sink, the device must be mounted on the solder side. The DUT is laid out on the same side so that the commutation device can also be installed on the same heat sink. Figure 12 shows a schematic of the mounting example, and Figure 13 shows a photograph of the mounted state. An equivalent product (33BS136) is available from Sankyo Thermo-Tech with a thermal resistance of 1.16ºC/W.

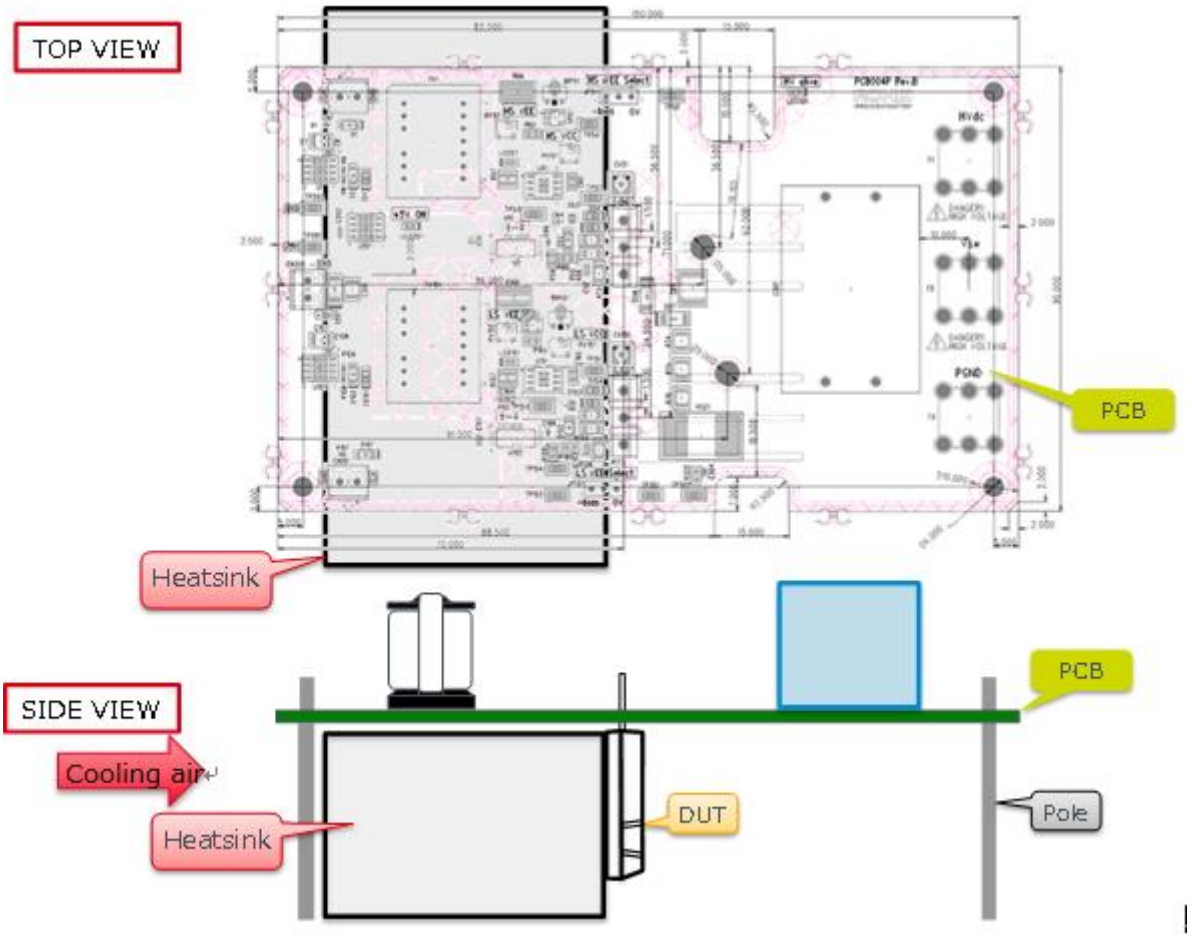
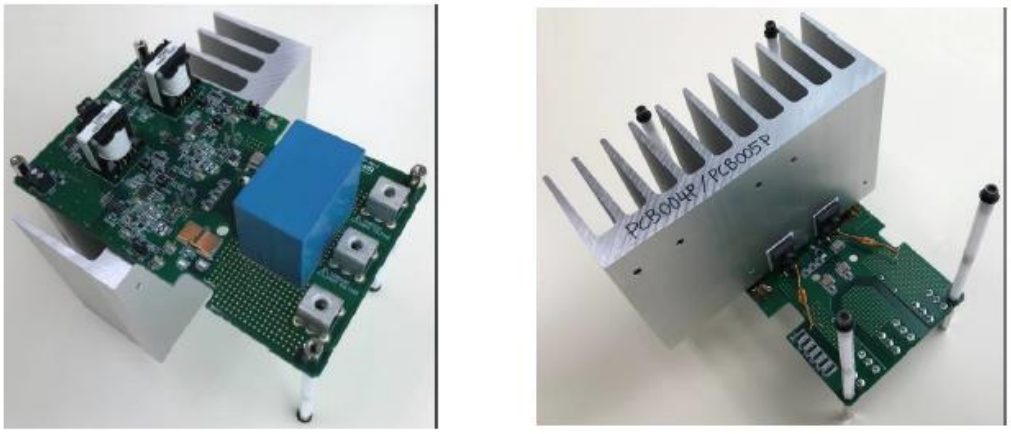


Figure 12 Heat sink installation diagram



(a) Top view (b) Bottom view

Figure 13 Example of heat sink installation

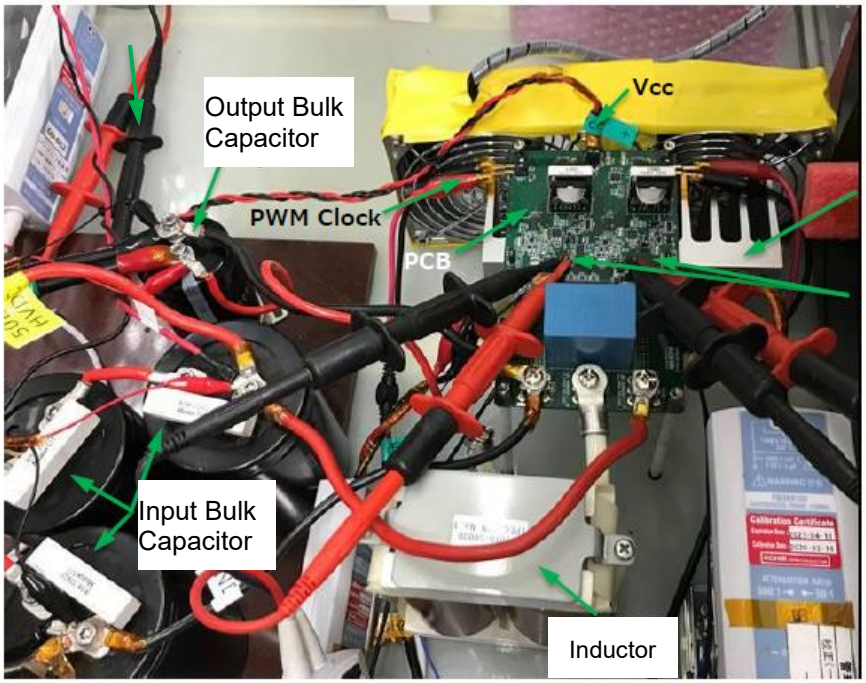


Figure 14 Measurement view of heat sink installation

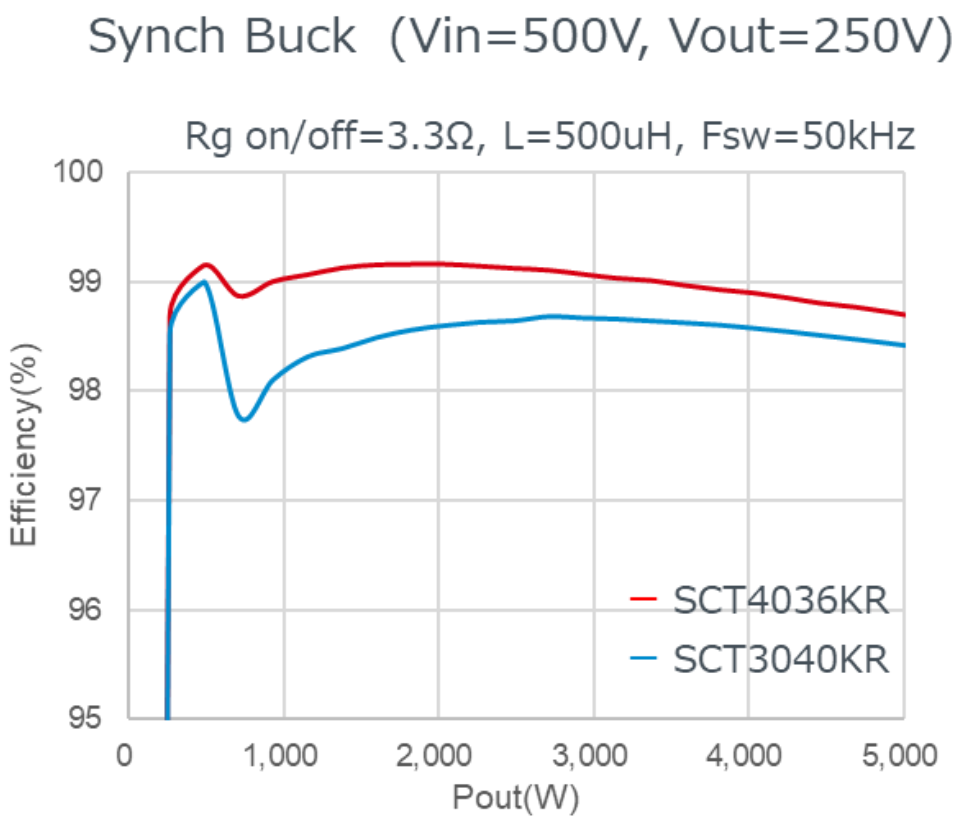


Figure 15 Efficiency
(SCT4036KR, BUCK, Rg=3.3Ω)

9. Evaluation Board Connection Example

9.1 Double-pulse test for H-side MOSFET

Figure 16 shows a double-pulse test circuit using a MOSFET on the H-side.

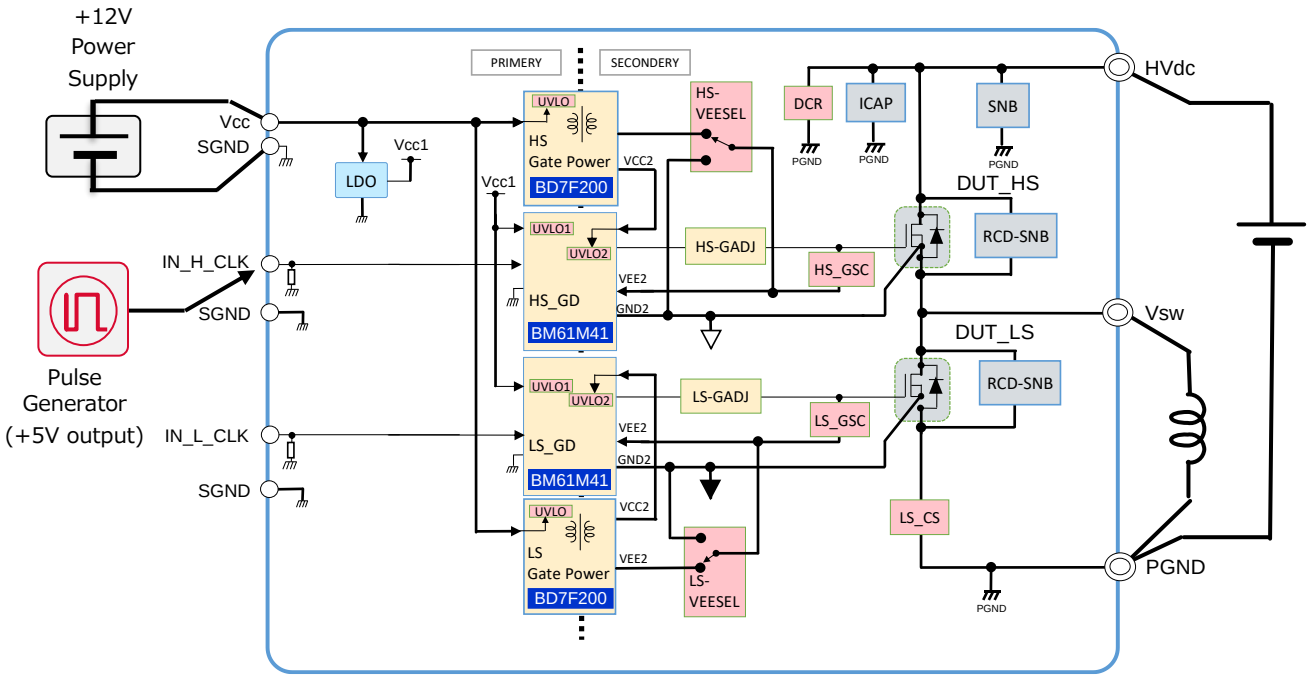


Figure 16 H-side double-pulse circuit

Prepare a pulse generator and connect the CLK signal to the IN_H_CLK pin (CN1 pin 1). Connect the 12 V power supply for control to the Vcc pin (CN201) and the high-voltage HVdc power supply to the HVdc pin (T1). The operating procedure is as follows.

① Turn on the power supply in the order of +12 V to HVdc.

② Input a pulse signal using the pulse generator.

The maximum current $I_{D(peak)}$ flowing through the inductor (L) can be roughly calculated by the following formula.

$$I_{D(PEAK)} \approx HVdc/L*T_{DP\_TTL}\ [A].$$

HVdc: Applied voltage [V]

L: Inductor value [μH].

T_{DP_TTL}: Total time of double-pulse signal [μs]

Normally, the double-pulse signal is a single shot, but when it is applied periodically, it is necessary to ensure sufficient reset time for the inductor current $I_{D\ (PEAK)}$. Since the reset voltage is only equal to the forward voltage V_F of the flywheel diode, determine the rough time using:

$$T_{RST} = I_{D(PEAK)}*L/V_F\ [\mu s]$$

and ensure that the reset time T_{RST} is about twice that value. Note that a heat sink is not necessary, but be careful not to raise the temperature of the flywheel diode when performing repeated double-pulse tests.

9.2 Double-pulse test with L-side MOSFET

Figure 17 shows the double-pulse test circuit using the L-side MOSFET.

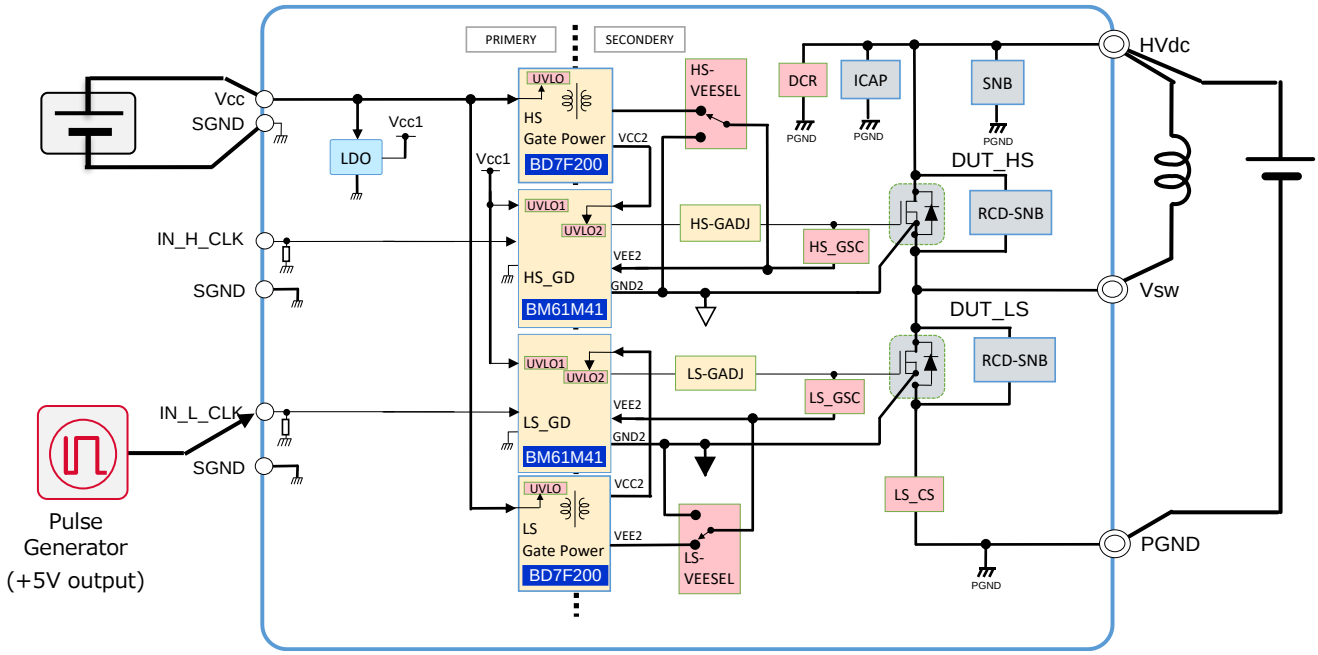


Figure 17 L-side double-pulse circuit

After preparing the pulse generator and connecting the external CLK signal to the IN_L_CLK pin (CN101 pin 1), the procedure is the same as for the H-side.

9.3 Boost power supply circuit

Figure 18 shows the boost operation test circuit in which the L-side MOSFET is switched.

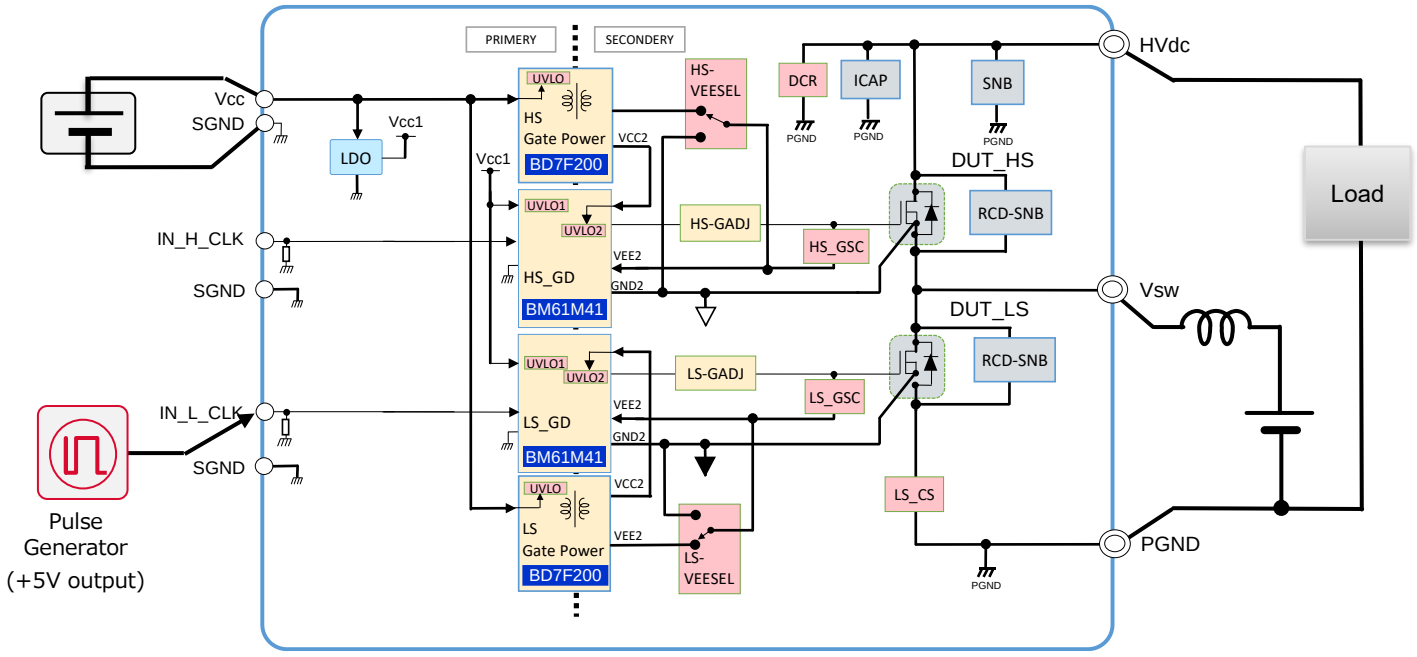


Figure 18 Operation test circuit based on boost circuit

First, prepare a pulse generator and connect the CLK signal to the IN_L_CLK pin (CN101 pin 1). Connect the 12 V power supply for control to the Vcc pin (CN201), the load inductance to the Vsw pin (T2), the high-voltage HVdc power supply to the load inductance, and the electronic load to the HVdc pin (T1) as shown in Figure 17. The HVdc side is the output, and since the output capacitor is mounted on the board, it is basically not necessary. However, if the oscillation frequency is low, it is recommended to add an appropriate value externally. In this case, ensure that the rated voltage of the capacitor is sufficient.

The operating procedure is as follows.

① Turn on the +12 V power supply.
② Set the switching frequency and duty ratio using the pulse generator and input the CLK signal.
③ Turn on the HVdc power supply.
④ Adjust the output current with an electronic load device.

In CCM mode, where the inductor current is continuous, the output voltage will be approximately as follows.

Vout=Vin/(1-Duty)

If the inductor current is discontinuous (output current is small), the output voltage will increase out of proportion to the duty ratio (output voltage varies with load current). This is because the pulses are not thinned out due to the open-loop control, but since the output voltage reaches several tens of times the input voltage, care must be taken to gradually increase the input voltage while keeping track of the output voltage value. When increasing the load current, pay attention to the heat generation of the evaluation device, and if necessary, install a heat sink capable of sufficient cooling or consider the ambient temperature.

9.4 Two-level inverter circuit

Figure 19 shows the operation test circuit for a 2-level inverter with a half-bridge configuration.

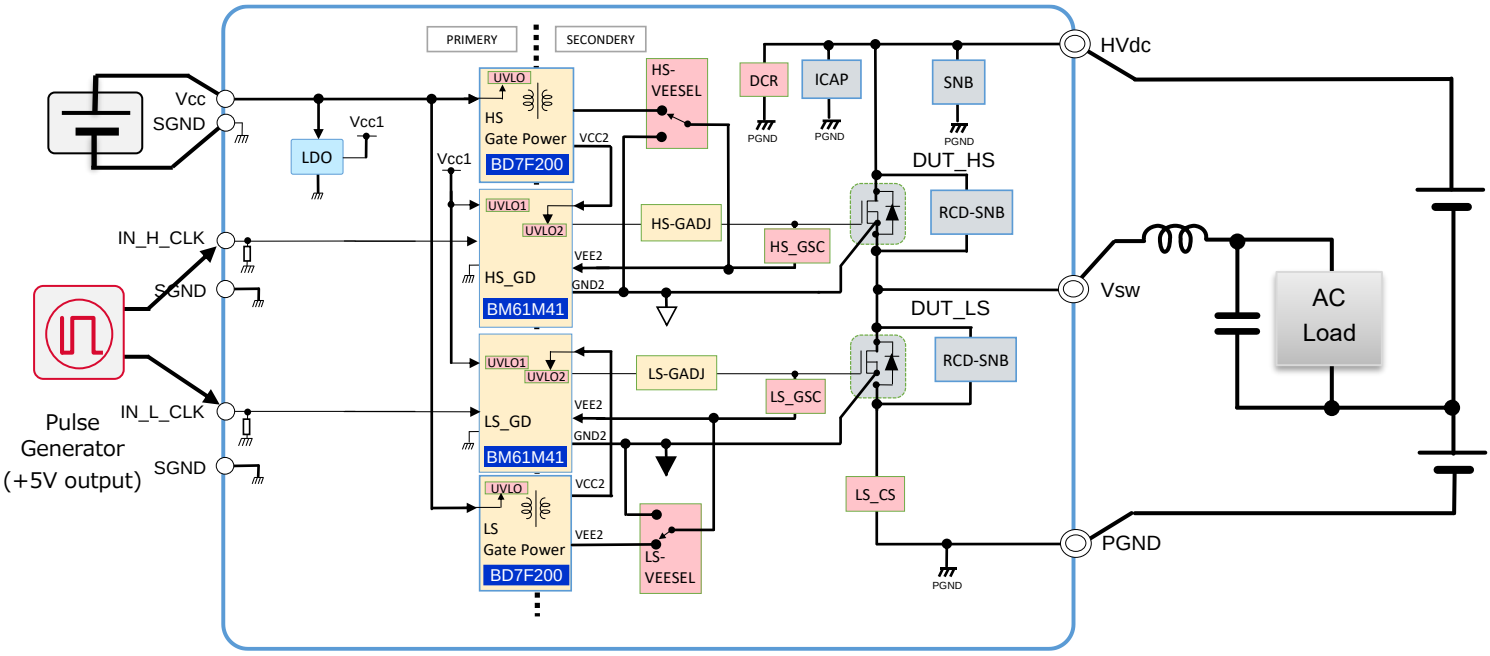


Figure 19 Operation test circuit for a 2-level inverter circuit

First, prepare a pulse generator and connect CLK signals to the IN_H_CLK and IN_L_CLK pins (CN1, CN101 pin 1). Connect the 12 V power supply for control to the Vcc pin (CN201) and the load inductance to the Vsw pin (T2). Prepare two high-voltage HVdc power supplies with the same voltage, connect them in series, and connect the upper one to the HVdc pin (T1) and the lower one to the PGND pin (T3). Connect a smoothing capacitor and an AC load to one side of the load inductance and connect its return line to the middle point of the series-connected high-voltage HVdc power supply.

When the AC output is on the + side, the H-side switches, and when it is on the - side, the L-side switches, and by controlling the duty cycle of the CLK signal, a sinusoidal voltage is output.

The operating procedure is as follows.

① Turn on the +12 V power supply.
② Set the switching frequency and duty ratio using the pulse generator and input the CLK signal.
③ Turn on the HVdc power supply.
④ Adjust the output current with an AC load device.

When increasing the load current, pay attention to the heat generation of the evaluation device, and if necessary, install a heat sink capable of sufficient cooling or consider the ambient temperature.

9.5 Synchronous rectification-type buck power circuit

Figure 20 shows the buck operation test circuit using an H-side MOSFET.

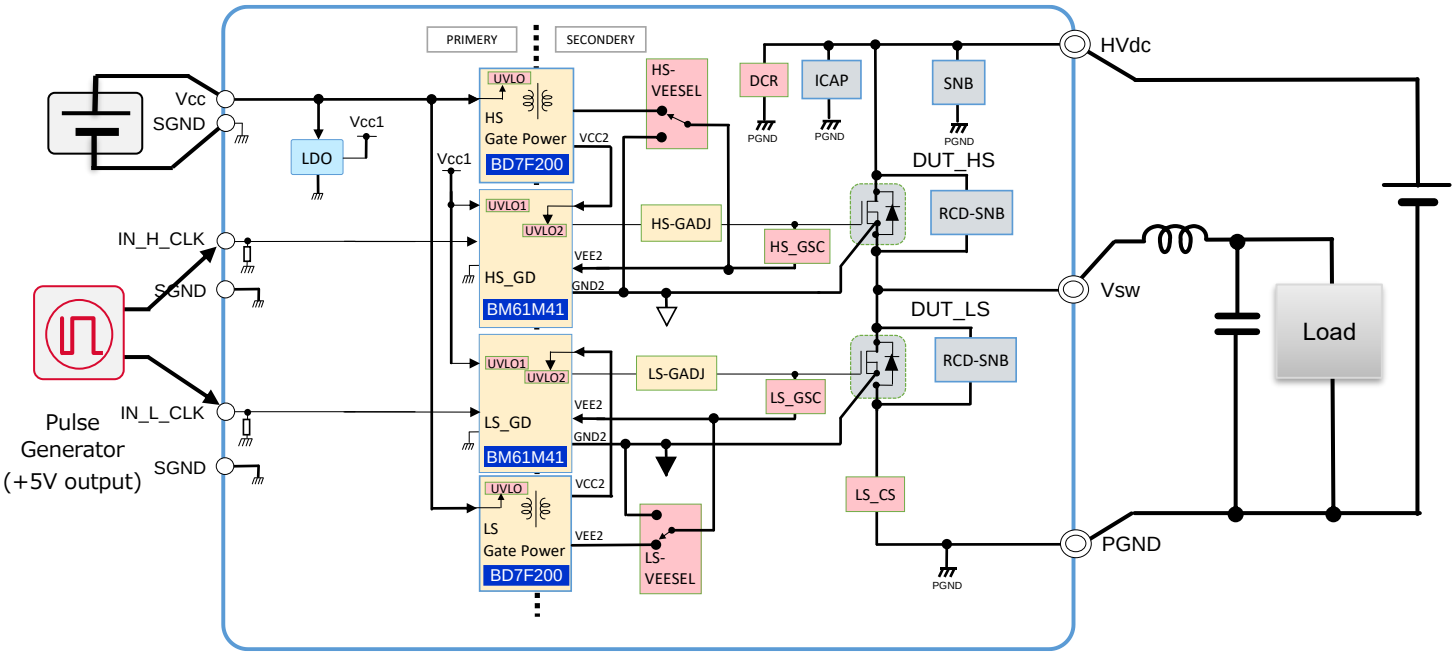


Figure 20 Operation test circuit based on synchronous rectification-type buck power supply circuit

Prepare a pulse generator and connect CLK signals from outside to the IN_H_CLK pin (CN1, pin 1) and IN_L_CLK pin (CN101, pin 1). Connect the 12 V power supply for control to the Vcc pin (CN201), the high-voltage HVdc power supply to the HVdc pin (T1), and the load inductance to the Vsw pin (T2). Connect the smoothing capacitor and load to one side of the load inductance. Since the HVdc side is the input, the input capacitor is mounted on the board and is basically not necessary. However, if the oscillation frequency is low, it is recommended to add an appropriate value externally. In this case, ensure that the rated voltage of the capacitor is sufficient.

The operating procedure is as follows.

① Turn on the +12 V power supply.
② Set the switching frequency and duty ratio using the pulse generator and input the CLK signal.
③ Turn on the HVdc power supply.
④ Adjust the output current with an electronic load device.

In CCM mode, where the inductor current is continuous, the output voltage will be approximately as follows.

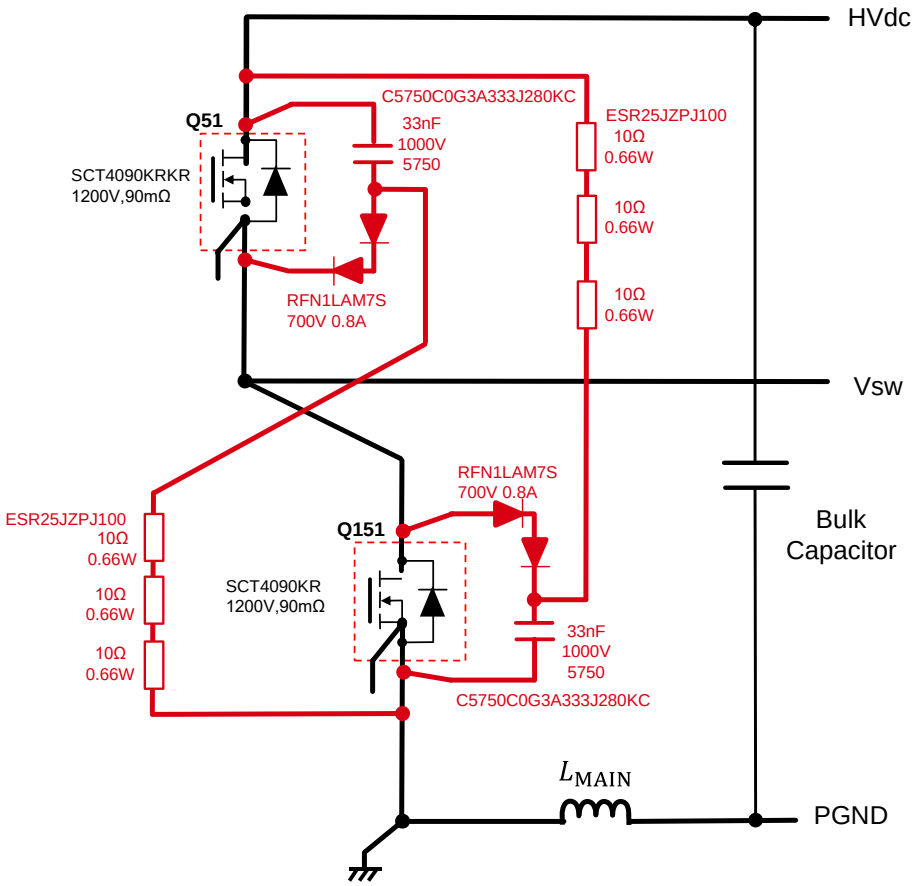
Vout=Duty*Vin

On the other hand, in DCM mode, where the inductor current is discontinuous, the output voltage is equal to the input voltage because the pulses are not thinned out due to open loop control. Since the output voltage is equal to the input voltage, pay attention to the withstand voltage of the electronic load device.

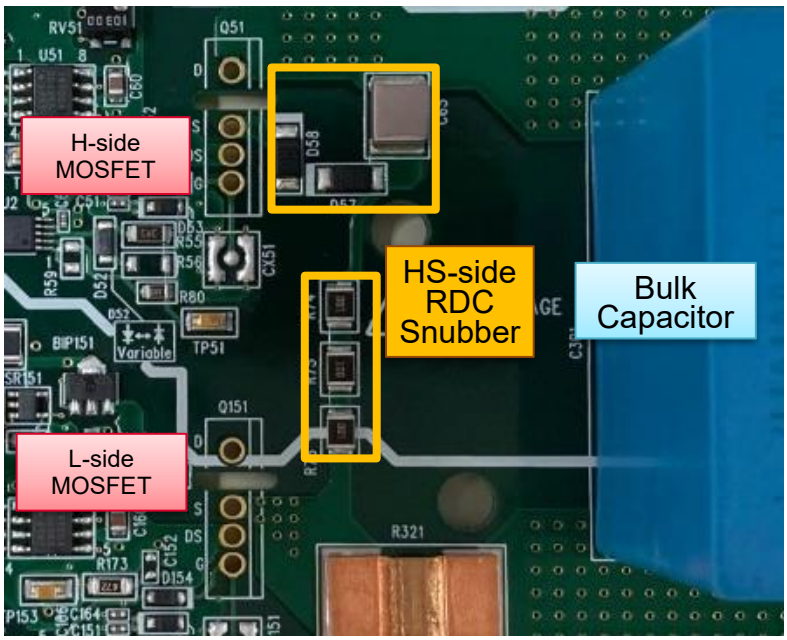
To prevent the H-side and L-side MOSFETs from being turned on simultaneously, make sure there is enough dead time between the IN_H_CLK and IN_L_CLK signals. When increasing the load current, pay attention to the heat generation of the evaluation device, and if necessary, install a heat sink capable of sufficient cooling or consider the ambient temperature.

10. Snubber Circuit

This board includes a non-discharge-type RCD snubber circuit (*3) layout between drain and source to suppress the turn-off surge of the MOSFET. Figure 21 shows the circuit diagram and an example of its mounting.



(a) Circuit diagram



(b) Mounting example (PCB005P, H-side)

Figure 21 RCD non-discharge snubber circuit

The non-discharge snubber circuit is ideal for high-frequency switching circuits because only the surge exceeding the high-voltage input HVdc is consumed by the resistors in the snubber circuit. However, since the pattern layout is complicated, it should be used on boards with four or more layers.

The power P_{SNB} consumed by the resistor in the snubber circuit is entirely consumed by the resistor R_{SNB} in the snubber circuit. The following equation applies:

$$P_{SNB} = \frac{L_{MAIN} \times {I_{MAIN}}^2 \times f_{SW}}{2}$$

Here, L_{MAIN} is the wiring inductance of the main circuit up to the bulk capacitor, I_{MAIN} is the drain current of the MOSFET at turn-off, and f_{SW} is the switching frequency of the MOSFET.

On the other hand, the capacitance C_{SNB} of the snubber capacitor is calculated from the energy stored in the inductance by the following equation

$$C_{SNB} = \frac{L_{MAIN} \times {I_{MAIN}}^2}{{V_{SURGE}}^2 - {V_{HVdc}}^2}$$

Where V_{HVdc} is the high-voltage power supply and V_{SURGE} is the maximum surge voltage.

Furthermore, the resistance of R_{SNB} can be obtained by the following equation.

$$R_{SNB} < \frac{-1}{C_{SNB} \times \ln[(V_{SURGE} - V_{SNB})/(V_{SURGE})]} \times \frac{1}{f_{sw}}$$

This maximizes the surge absorption effect by discharging all the energy absorbed by C_{SNB} during one cycle of the MOSFET.

Figure 22 shows the verification results of the snubber circuit of the SCT4018KR from double-pulse testing. During turn-on, there is no difference between with and without snubber circuit, but during turn-off, the V_{DS} turn-off surge is reduced from 1207 V to 1070 V. On the other hand, there is little effect on the switching speed.

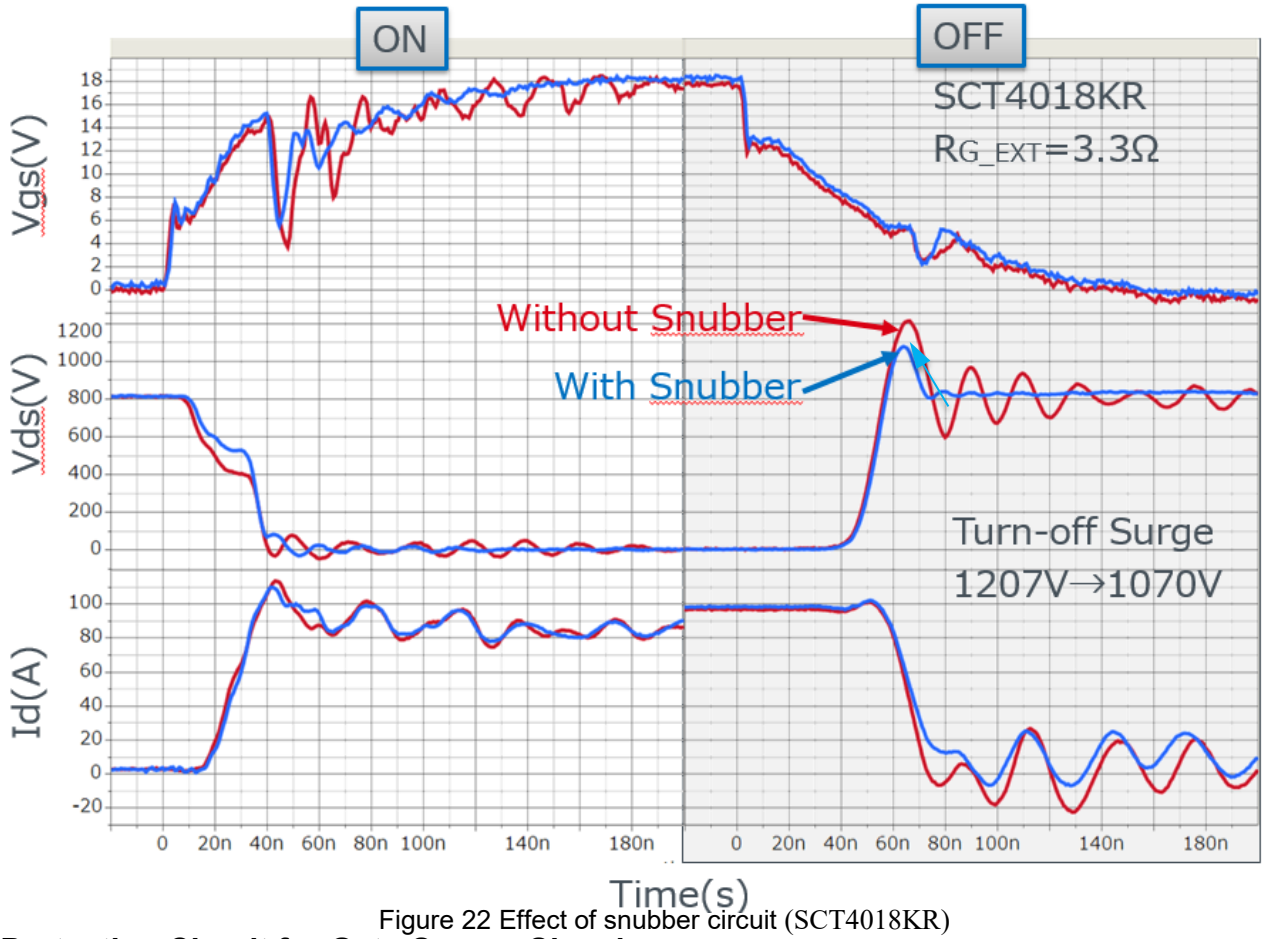


Figure 22 Effect of snubber circuit (SCT4018KR)

11. Protection Circuit for Gate-Source Signal

11.1 Types of protection circuits

This board has a built-in protection circuit that absorbs surge voltage generated at the gate-source pin of the MOSFET. The protection circuit has three functions (clamp circuit) and four countermeasure circuits as shown in Table 7. Since the gate-source voltage is greatly affected by the change in V_{DS} and I_D during switching operation, it is necessary to suppress the surge voltage appropriately with these protective circuits. For more information on gate-source voltage behavior and surge suppression methods, please refer to the application notes (*1) and (*2) that have been published separately.

Figure 23 shows the circuit diagram.

Table 7 Protection circuit and operation details

Item	Function (clamp circuit)	Target component	Operation details	Default setting
(I)	Positive surge suppression	D53, C51 D153, C151	Positive surge that occurs when the V_{DS} change of the MOSFET is completed. During turn-on, it may exceed the maximum V_{DS} rating, so it is clamped to Vcc2 by D53 (D153). C51 (C151) is a bypass capacitor and is laid out in the vicinity of D53 (D153).	Mounting
(II)	Negative surge suppression	D54, C64 D154, C164	During turn-off operation of the MOSFET in bridge configuration, a negative surge occurs in V_{GS} of the non-switching side MOSFET, which may exceed the maximum rating. Therefore, it is clamped to the turn-off drive voltage (VEE2). C64 (C164) is a bypass capacitor and is laid out in the vicinity of D54 (D154).	Mounting
(III)	Self-turn-on prevention Self-turn-on surge suppression	R80 R180	During turn-on operation of the MOSFET in bridge configuration, V_{GS} of the non-switching side MOSFET may rise (linked to the rise of V_{DS}) and turn on when the gate threshold $V_{GS(th)}$ is exceeded (so-called self-turn-on). Therefore, this rise of V_{GS} is suppressed by clamping it to the turn-off drive voltage using the MC signal of the driver IC (BM61M41RFV-C).	Mounting
(IV)		C52 C152	As the Crss/Ciss ratio of the MOSFET becomes larger, V_{GS} tends to rise. (Because the charging current is proportional to Crss) By adding capacitance in parallel with Ciss and reducing the Crss/Ciss ratio, VGS can be prevented from rising above $V_{GS(th)}$. The larger the capacitance value to be added, the smaller the amount of rise becomes, but the additional capacitance must be determined while considering heat generation, because it not only requires more drive capability but also involves an increase in switching loss.	Not mounted

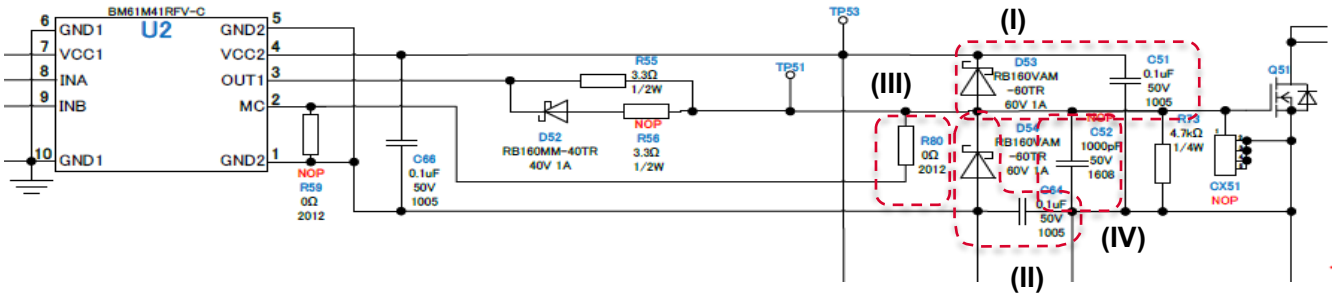


Figure 23 Protection circuit for gate-source signal (PCB004P)

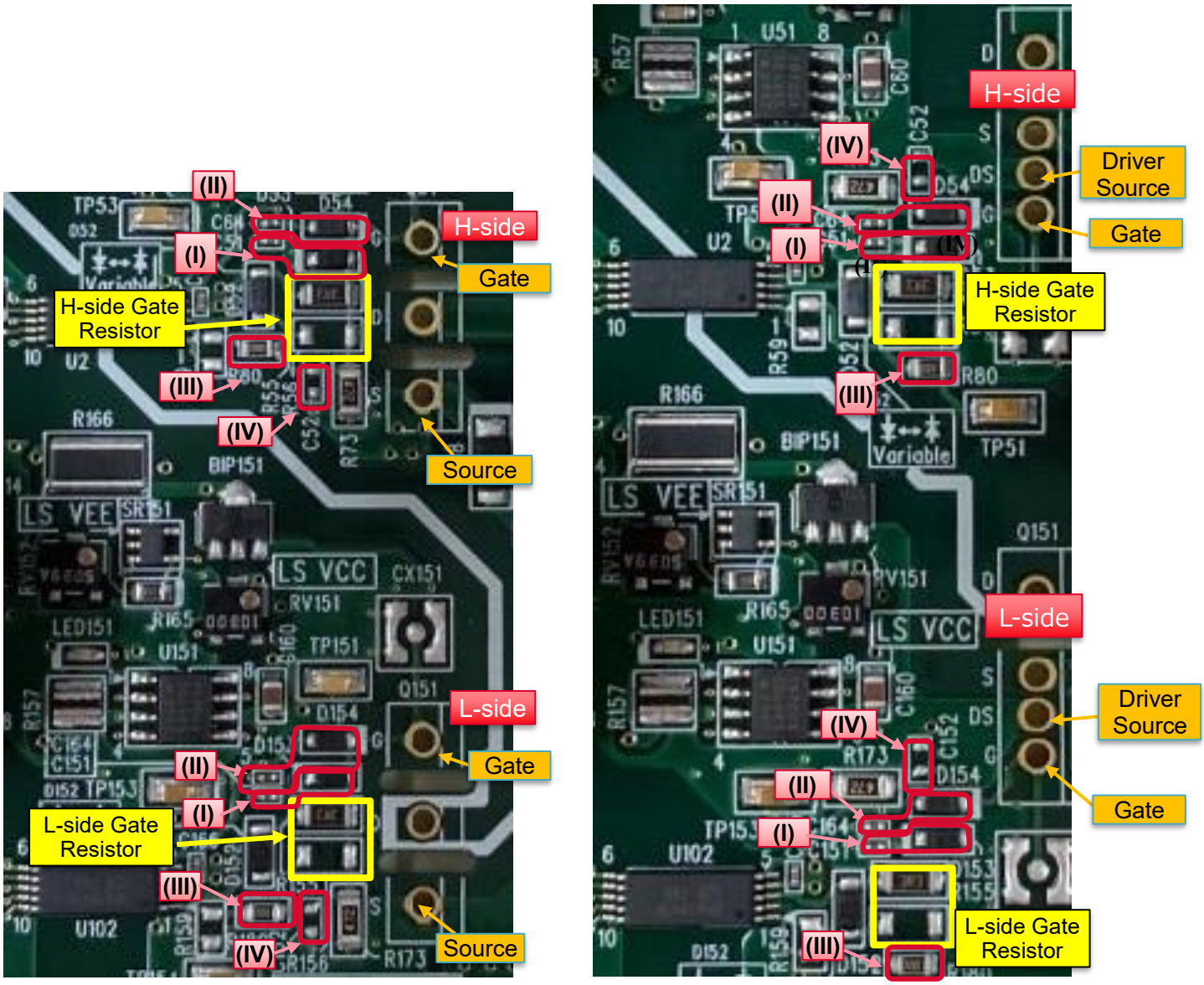
Since V_{GS} surge voltages occur over a short time period of a few tens of ns, the pattern inductance of these clamping circuits should be laid out in the immediate vicinity of the MOSFET to minimize inductance.

SiC MOSFETs generally have narrower gate-source voltage ratings than Si MOSFETs, so it is recommended to install these clamping circuits. By using several of these countermeasure circuits, it is possible to suppress the surge voltage of V_{GS} more effectively. However, the priorities for laying out components in the vicinity of the MOSFET are as follows, and if a driver IC with a built-in mirror clamp (MC) signal is used, it should be laid out as close as possible to the MOSFET to be driven, and the parasitic inductance should be reduced by shortening the pattern line length between the MC pin and the MOSFET.

(II) Negative surge clamp circuit ➔(I) Positive surge clamp circuit ➔(IV) Additional capacitance between GS (C_{GS})

Figure 24 shows an example of a protective circuit mounting. (a) is the board for TO-247N (PCB004P) and (b) is the board for TO-247-4L (PCB005P). Since the pin assignment of the gate pin is opposite for TO-247N and TO247-4L, the protection circuit has the optimal mounting layout for each package.

Figure 25 shows some examples of differences in waveforms with and without the protection circuit. However, actual operation is greatly affected not only by the characteristics of the device itself, but also by the board on which it is mounted, so it is necessary to check the actual device.



(a) PCB004P (b) PCB005P

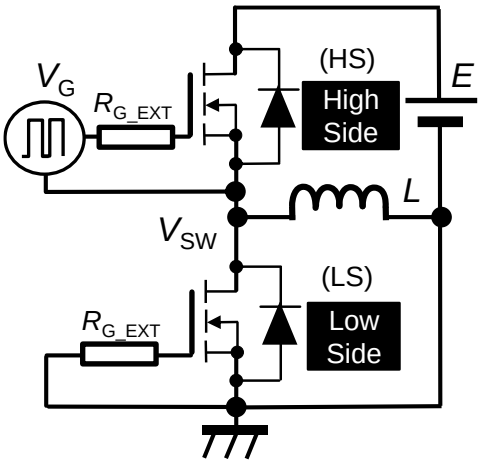
Figure 24 Mounting position of gate-source voltage protection circuit

11.2 Surge suppression effect of protective circuit

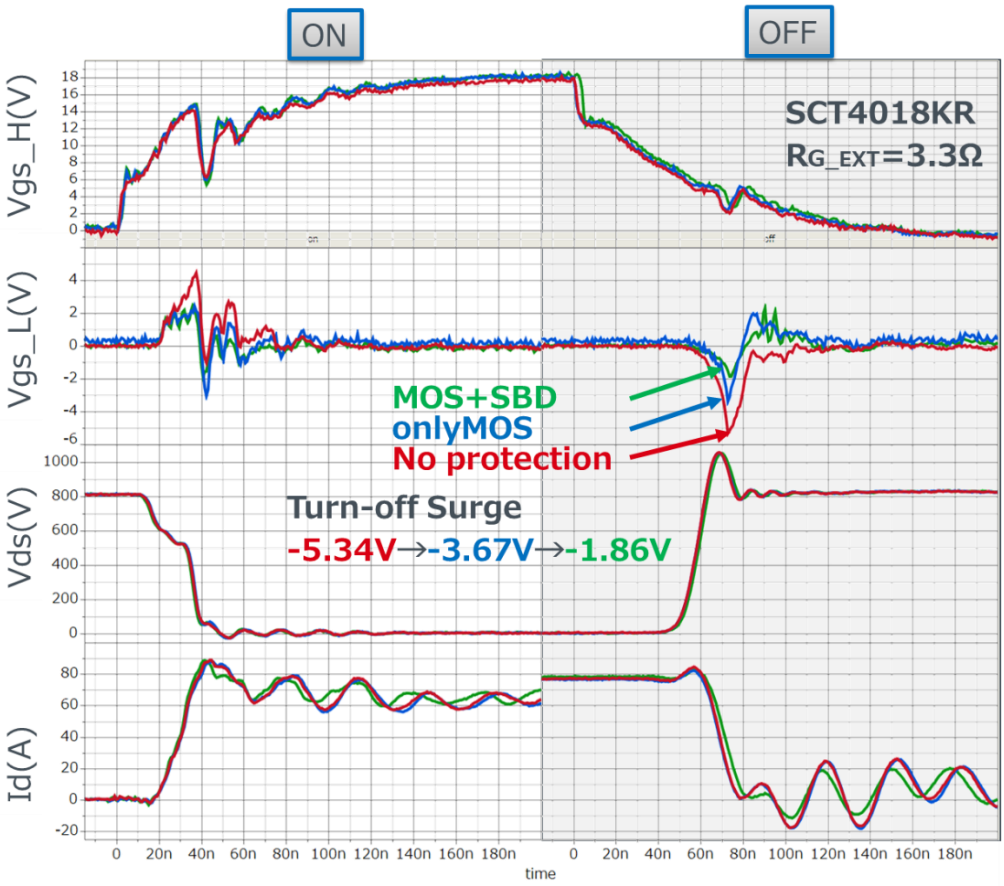
A double-pulse test was conducted by connecting SCT4090KR in a bridge configuration and switching the high-side (HS), and the following is an example of how the protective circuit reduces the V_{GS} surge voltage. Figure 24(a) shows the measurement circuit and (b) shows the measurement waveform.

The external gate resistor R_{G_EXT} is 3.3Ω. The top waveform is V_{GS} on the H-side, the second is V_{GS} on the L-side, the third is V_{DS} on the H-side, and the bottom waveform is I_D on the H-side. The gate-source pin surge is positive on the H-side during turn-on, and negative on the HS and L-sides during turn-off. Separate application notes (*1),(*4) on the causes of surges have been prepared, so they are not discussed in detail here. However, if no protection circuit is mounted (No Protection), a surge exceeding the rated gate voltage of the MOSFET may occur.

■ Measurement conditions
DUT: SCT4018KR
E: 800V
L: 250μH
Drain current: Approx. 80 A
Pulse width: 2.5μs
R_{G_EXT}: 3.3Ω
Evaluation board: PCB005P Rev.C



(a) Measurement circuit



(b) Measurement waveform

Figure 25 Effect of protection circuit (SCT4090KR)

On the other hand, by connecting the mirror clamp signal (MC signal) of the driver IC (BM61M41RFV-C), which is one of the protection circuits, the surge at turn-off can be suppressed. However, since the MC signal needs to respond at high speed, the wiring length to the MOSFET should be made as short as possible. The mounting position of the gate resistor for speed adjustment R_{G_EXT}, etc. has priority, and it may not be possible to mount it near the MOSFET, so the clamping effect may not be sufficient depending on the layout. Based on experience, the clamping effect becomes extremely low when the distance is 20 mm or more.

Therefore, by placing the clamp SBD directly under the MOSFET and adding a circuit that suppresses negative surges (MC signal + Clamp SBD), the surge suppression effect can be further enhanced, and it can be seen that the gate surge voltage is suppressed to within the rating in this measurement.

As shown above, surges linked to the transient operation of the MOSFET are generated at the gate pin in both positive and negative directions, so it is important to place a protection circuit near the MOSFET from the design stage.

12. Precautions

Since this evaluation board handles voltages of several hundred volts, care must be taken at all times to avoid dangerous situations due to malfunctions. Defects may occur not only in this board, but also due to incorrect handling, such as misconnection of wiring or application of out-of-specification voltages.

Table 8 shows the points to pay attention to, but please take all possible measures to prevent other problems before using the product.

Table 8 List of typical faults

Function	Items	Details
DCR	LED does not light up	When voltage is applied to the HVdc-PGND pins, check that LED301 (red) is lit. If the LED does not light up, check the applied voltage source and wiring. The LED lights up when the input/output voltage is approximately 20 V or more.
HVdc Vsw	Misconnection of wiring Application of out-of-specification voltage	It is strictly prohibited to apply a voltage higher than the specified value (1200 V), and care must be taken to ensure that there is no misconnection of wiring, etc. Also, never touch the product while it is in operation.
Vcc	Misconnection of wiring Application of out-of-specification voltage	Check the wiring of Vcc before use to prevent the application of positive and negative reverse voltages. However, since a diode for reverse connection is included, the OPC setting of the Vcc power supply should be set to 1 A to 3 A. (To protect the diode for reverse connection). Also, applying a voltage other than the specified voltage may cause a failure, so operate the circuit only after thorough confirmation.
SNB RDC_SNB	MLCC burnout	An MLCC, that is prone to cracks and other short-circuit failures due to mechanical stress, is used. Therefore, handle the board with care to avoid excessive shocks. If you have even the slightest concern when voltage is applied, immediately take measures to avoid danger, such as cutting off the applied voltage.
IN_H_CLK IN_L_CLK	Continuous pulse application	Continuous application of the CLK signal to drive the DUT may cause a current exceeding the specified value to flow and may damage the DUT. Therefore, always use the DUT within the range that satisfies its electrical characteristics.
DUT	Driver IC damage	If the gate-source of the DUT is short-circuited and the CLK signal to be driven is turned on, a short-circuit current will flow from Vcc2 through the OUT pin to GND2, which may destroy the OUT pin of the driver IC if the external resistance is small. Therefore, be sure to check the gate-source short circuit conditions before operation.

References:

*1 "Gate-source voltage behavior in a bridge configuration"
Application Note (No. 60AN135ERev.002)
ROHM Co., Ltd., May 2018
https://fscdn.rohm.com/en/products/databook/applinote/discrete/sic/mosfet/sic-mosfet_gate-source_voltage_an-e.pdf

*2 "Gate-Source Voltage Surge Suppression Methods"
Application Note (No. 62AN010ERev.002)
ROHM Co., Ltd., May 2019
https://fscdn.rohm.com/en/products/databook/applinote/discrete/sic/mosfet/sicmosfet-surge%20suppression_an-e.pdf

*3 "Snubber Circuit Design Methods"
Application Note (No. 62AN0036JRev.001)
ROHM Co., Ltd., June 2019
https://fscdn.rohm.com/en/products/databook/applinote/discrete/sic/mosfet/sic-mos_snubber_circuit_design_an-e.pdf

*4 "Improvement of Switching Loss by Driver Source Pin"
Application Note (No. 62AN0039JRev.001)
ROHM Co., Ltd., August 2019
https://fscdn.rohm.com/en/products/databook/applinote/discrete/sic/mosfet/sicmosfet_swloss_an-e.pdf

*5 Nippon Automatic Control Co., Ltd. website
https://naccjp.com/nacc/lp/cwt/

*6 T&M Research Products, Inc. website
https://www.tandmresearch.com/index.php?mact=ListIt2Products,cntnt01,detail,0&cntnt01item=series-sdn-414&cntnt01template_summary=Side&cntnt01returnid=19

*7 "How to Select the Right Current Probe"
Application Note (No. 5992-2656EN)
KEYSIGHT TECHNOLOGIES, September 2018

Notes

1) The information contained herein is subject to change without notice.

2) Before you use our Products, please contact our sales representative and verify the latest specifications :

3) Although ROHM is continuously working to improve product reliability and quality, semiconductors can break down and malfunction due to various factors.
Therefore, in order to prevent personal injury or fire arising from failure, please take safety measures such as complying with the derating characteristics, implementing redundant and fire prevention designs, and utilizing backups and fail-safe procedures. ROHM shall have no responsibility for any damages arising out of the use of our Poducts beyond the rating specified by ROHM.

4) Examples of application circuits, circuit constants and any other information contained herein are provided only to illustrate the standard usage and operations of the Products. The peripheral conditions must be taken into account when designing circuits for mass production.

5) The technical information specified herein is intended only to show the typical functions of and examples of application circuits for the Products. ROHM does not grant you, explicitly or implicitly, any license to use or exercise intellectual property or other rights held by ROHM or any other parties. ROHM shall have no responsibility whatsoever for any dispute arising out of the use of such technical information.

6) The Products specified in this document are not designed to be radiation tolerant.

7) For use of our Products in applications requiring a high degree of reliability (as exemplified below), please contact and consult with a ROHM representative : transportation equipment (i.e. cars, ships, trains), primary communication equipment, traffic lights, fire/crime prevention, safety equipment, medical systems, servers, solar cells, and power transmission systems.

8) Do not use our Products in applications requiring extremely high reliability, such as aerospace equipment, nuclear power control systems, and submarine repeaters.

9) ROHM shall have no responsibility for any damages or injury arising from non-compliance with the recommended usage conditions and specifications contained herein.

10) ROHM has used reasonable care to ensure the accuracy of the information contained in this document. However, ROHM does not warrants that such information is error-free, and ROHM shall have no responsibility for any damages arising from any inaccuracy or misprint of such information.

11) Please use the Products in accordance with any applicable environmental laws and regulations, such as the RoHS Directive. For more details, including RoHS compatibility, please contact a ROHM sales office. ROHM shall have no responsibility for any damages or losses resulting non-compliance with any applicable laws or regulations.

12) When providing our Products and technologies contained in this document to other countries, you must abide by the procedures and provisions stipulated in all applicable export laws and regulations, including without limitation the US Export Administration Regulations and the Foreign Exchange and Foreign Trade Act.

13) This document, in part or in whole, may not be reprinted or reproduced without prior consent of ROHM.

ROHM SEMICONDUCTOR

Thank you for your accessing to ROHM product informations.
More detail product informations and catalogs are available, please contact us.

ROHM Customer Support System

http://www.rohm.com/contact/