

Dual, 200-mA, Low- I_Q Low-Dropout Regulator for Portable Devices

Check for Samples: [TLV7103318-Q1](#) , [TLV7101828-Q1](#)

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
 - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
 - Device HBM ESD Classification Level H2
 - Device CDM ESD Classification Level C4B
- Very Low Dropout:
 - 150 mV at $I_{\text{OUT}} = 200\text{ mA}$ and $V_{\text{OUT}} = 2.8\text{ V}$
 - 75 mV at $I_{\text{OUT}} = 100\text{ mA}$ and $V_{\text{OUT}} = 2.8\text{ V}$
 - 40 mV at $I_{\text{OUT}} = 50\text{ mA}$ and $V_{\text{OUT}} = 2.8\text{ V}$
- 2% Accuracy Over Temperature
- Low I_Q of 35 μA per Regulator
- Multiple Fixed-Output Voltage Combinations Possible from 1.2 V to 4.8 V
- High PSRR: 70 dB at 1kHz
- Stable With Effective Capacitance of 0.1 μF ⁽¹⁾
- Overcurrent and Thermal Protection
- Dedicated V_{REF} for Each Output Minimizes Crosstalk
- Available in 1.5mm \times 1.5mm SON-6 Package

⁽¹⁾ See the [Input and Output Capacitor Requirements](#) in the [Application Information](#) section

APPLICATIONS

- Automotive Applications
- Wireless Handsets, Smart Phones, PDAs
- MP3 Players and Other Handheld Products

DESCRIPTION

The TLV7103318-Q1 and TLV7101828-Q1 family of dual, low-dropout (LDO) linear regulators are low quiescent current devices with excellent line and load transient performance. These LDOs are designed for power-sensitive applications. These devices provide a typical accuracy of 2% over temperature.

The TLV7103318-Q1 and TLV7101828-Q1 family are available in a 1,5-mm \times 1,5-mm SON-6 package, and are ideal for handheld applications.

TLV7103318-Q1
TLV7101828-Q1
1,5-mm \times 1,5-mm SON-6
(TOP VIEW)

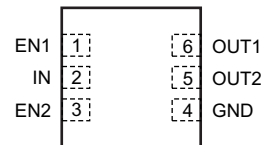
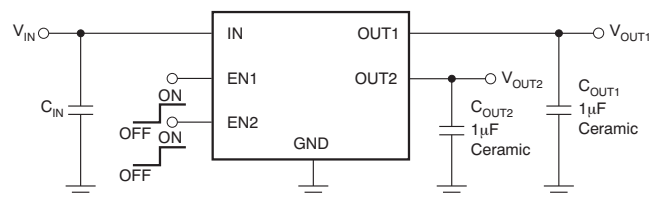


Figure 1. Typical Application Circuit



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DEVICE DETAILS

PRODUCT	V _{OUT} ⁽¹⁾
TLV710xyyqwwwz	XX is nominal output voltage of channel 1 (for example 18 = 1.8 V). YY is nominal output voltage of channel 2 (for example 28 = 2.8V). Q is optional. Use "U" for devices with EN pin pull-up resistor, and "D" for devices with EN pin pull-down resistor. WWW is package designator. Z is package quantity. Use "R" for reel (3000 pieces), and "T" for tape (250 pieces).

(1) Output voltages from 1.2V to 4.8V in 50mV increments are available through the use of innovative factory OTP programming; minimum order quantities may apply. Contact factory for details and availability.

ORDERING INFORMATION⁽¹⁾

ORDERABLE PART NUMBER	T _A	PACKAGE ⁽²⁾		TOP-SIDE MARKING
TLV7103318QDSERQ1	-40°C to 125°C	WSO-N-DSE	Reel of 3000	ZD
TLV7101828QDSERQ1				CP

(1) For the most-current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

At T_A = -40°C to 125°C (unless otherwise noted).

		VALUE		UNIT
		MIN	MAX	
Voltage ⁽²⁾	IN	-0.3	6	V
	EN	-0.3	V _{IN} 0.3	V
	OUT	-0.3	6	V
Current	OUT	Internally limited		A
Output short-circuit duration		Indefinite		s
Temperature	Operating ambient, T _A	-40	125	°C
	Junction, T _J	150		°C
	Storage, T _{stg}	-55	150	°C
Electrostatic Discharge (ESD) rating	Human-Body Model (HBM) AEC-Q100 Classification Level H2	2		kV
	Charged-Device Model (CDM) AEC-Q100 Classification Level C4B	750		V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages with respect to ground.

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		TLV7103318-Q1, TLV7101828-Q1		UNIT
		DSE		
		6 PINS		
θ_{JA}	Junction-to-ambient thermal resistance ⁽²⁾	190.5		°C/W
θ_{JcTop}	Junction-to-case (top) thermal resistance ⁽³⁾	94.9		°C/W
θ_{JB}	Junction-to-board thermal resistance ⁽⁴⁾	149.3		°C/W
ψ_{JT}	Junction-to-top characterization parameter ⁽⁵⁾	6.4		°C/W
ψ_{JB}	Junction-to-board characterization parameter ⁽⁶⁾	152.8		°C/W
θ_{JcBot}	Junction-to-case (bottom) thermal resistance ⁽⁷⁾	N/A		°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter, ψ_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter, ψ_{JB} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

At $T_A = -40^\circ\text{C}$ to 125°C , $V_{IN} = V_{OUT(TYP)} + 0.5\text{ V}$ or 2 V (whichever is greater), $I_{OUT} = 10\text{ mA}$, $V_{EN1} = V_{EN2} = 0.9\text{ V}$, and $C_{OUT1} = C_{OUT2} = 1\text{ }\mu\text{F}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TLV710xxx8-Q1			UNIT
			MIN	TYP	MAX	
V_{IN}	Input voltage range		2		5.5	V
V_O	Output voltage range		1.2		4.8	V
V_{OUT}	DC output accuracy	$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$	-2		2	%
$\Delta V_O/\Delta V_{IN}$	Line regulation	$V_{OUT(NOM)} + 0.5\text{ V} \leq V_{IN} \leq$		1	5	mV
$\Delta V_O/\Delta I_{OUT}$	Load regulation	$0\text{ mA} \leq I_{OUT} \leq 200\text{ mA}$		5	15	mV
V_{DO}	Dropout voltage	$V_{IN} = 0.98\text{ V} \times V_{OUT(NOM)}$, $I_{OUT} = 200\text{ mA}$, $2\text{ V} \leq V_{OUT} < 2.4\text{ V}$		200	285	mV
		$V_{IN} = 0.98\text{ V} \times V_{OUT(NOM)}$, $I_{OUT} = 200\text{ mA}$, $2.4\text{ V} \leq V_{OUT} < 2.8\text{ V}$		175	250	mV
		$V_{IN} = 0.98\text{ V} \times V_{OUT(NOM)}$, $I_{OUT} = 200\text{ mA}$, $2.8\text{ V} \leq V_{OUT} < 3.3\text{ V}$		150	215	mV
		$V_{IN} = 0.98\text{ V} \times V_{OUT(NOM)}$, $I_{OUT} = 200\text{ mA}$, $3.3\text{ V} \leq V_{OUT} \leq 4.8\text{ V}$		140	200	mV
I_{CL}	Output current limit	$V_{OUT} = 0.9\text{ V} \times V_{OUT(NOM)}$	220	350	550	mA
I_Q	Quiescent current	$V_{EN1} = \text{high}$, $V_{EN2} = \text{low}$, $I_{OUT1} = 0\text{ mA}$		35		μA
		$V_{EN1} = \text{low}$, $V_{EN2} = \text{high}$, $I_{OUT2} = 0\text{ mA}$		35		μA
		$V_{EN1} = \text{high}$, $V_{EN2} = \text{high}$, $I_{OUT} = 0\text{ mA}$		70	110	μA
I_{GND}	Ground pin current	$I_{OUT1} = I_{OUT2} = 200\text{ mA}$		360		μA
$I_{SHUTDOWN}$	Shutdown current	$V_{EN1,2} \leq 0.4\text{ V}$, $2\text{ V} \leq V_{IN} \leq 4.5\text{ V}$		2.5	4	μA
PSRR	Power-supply rejection ratio	$V_{OUT} = 1.8\text{ V}$		$f = 10\text{ Hz}$	80	dB
				$f = 100\text{ Hz}$	75	dB
				$f = 1\text{ kHz}$	70	dB
				$f = 10\text{ kHz}$	70	dB
				$f = 100\text{ kHz}$	50	dB
V_N	Output noise voltage	$BW = 100\text{ Hz to }100\text{ kHz}$, $V_{OUT} = 1.8\text{ V}$		48		μV_{RMS}
t_{STR}	Startup time ⁽¹⁾	$C_{OUT} = 1\text{ }\mu\text{F}$, $I_{OUT} = 200\text{ mA}$		100		μs

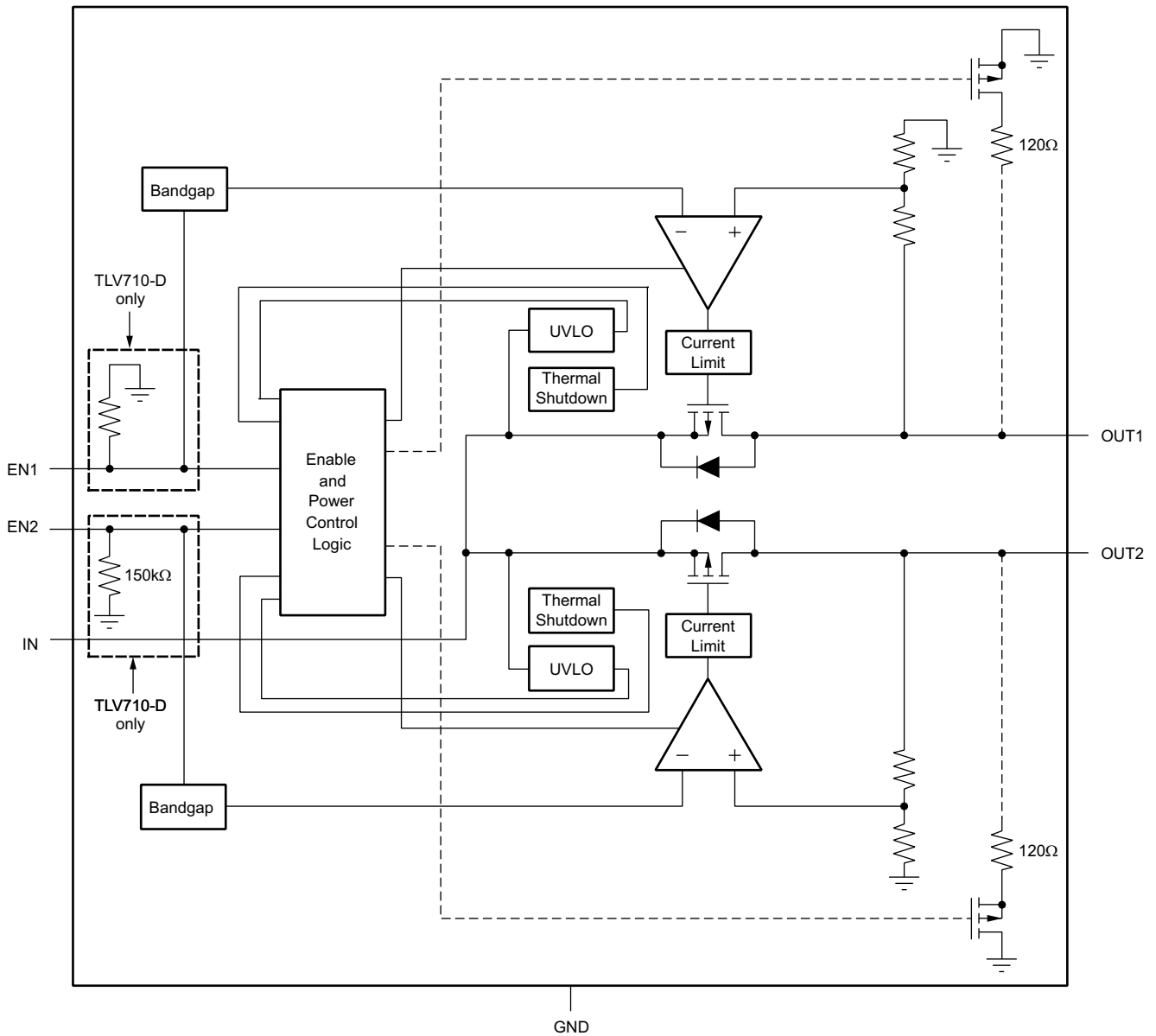
- (1) Startup time = time from EN assertion to $0.98 \times V_{OUT(NOM)}$.

RECOMMENDED OPERATING CONDITIONS (continued)

At $T_A = -40^{\circ}\text{C}$ to 125°C , $V_{IN} = V_{OUT(TYP)} + 0.5\text{ V}$ or 2 V (whichever is greater), $I_{OUT} = 10\text{ mA}$, $V_{EN1} = V_{EN2} = 0.9\text{ V}$, and $C_{OUT1} = C_{OUT2} = 1\text{ }\mu\text{F}$, unless otherwise noted.

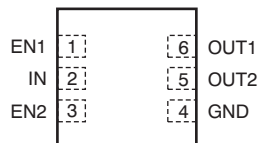
PARAMETER		TEST CONDITIONS	TLV710xxx8-Q1			UNIT
			MIN	TYP	MAX	
V_{HI}	Enable high (enabled)		0.9		V_{IN}	V
V_{LO}	Enable low (shutdown)		0		0.4	V
I_{EN}	Enable pin current, enabled	TLV7103318-Q1, TLV7101828-Q1		0.04		μA
		TLV710-D		6		μA
UVLO	Undervoltage lockout	V_{IN} rising		1.9		V
T_A	Operating ambient temperature		-40		125	$^{\circ}\text{C}$
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		165		$^{\circ}\text{C}$
		Reset, temperature decreasing		145		$^{\circ}\text{C}$

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

DSE PACKAGE
 1.5mm x 1.5mm SON-6
 (TOP VIEW)



PIN DESCRIPTIONS

NAME	PIN NO.	DESCRIPTION
EN1	1	Enable pin for regulator 1. Driving EN1 over 0.9V turns on regulator 1. Driving EN below 0.4V puts regulator 1 into shutdown mode.
IN	2	Input pin. A small capacitor is needed from this pin to ground to assure stability. See Input and Output Capacitor Requirements in the <i>Application Information</i> section for more details.
EN2	3	Enable pin for regulator 2. Driving EN2 over 0.9V turns on regulator 2. Driving EN2 below 0.4V puts regulator2 into shutdown mode.
GND	4	Ground pin.
OUT2	5	Regulated output voltage pin. A small 1µF ceramic capacitor is needed from this pin to ground to assure stability. See Input and Output Capacitor Requirements in the <i>Application Information</i> section for more details.
OUT1	6	Regulated output voltage pin. A small 1µF ceramic capacitor is needed from this pin to ground to assure stability. See Input and Output Capacitor Requirements in the <i>Application Information</i> section for more details.

TYPICAL CHARACTERISTICS

Over operating temperature range of $T_A = -40^\circ\text{C}$ to 125°C , $V_{EN1} = V_{EN2} = V_{IN}$, $C_{IN} = 1\ \mu\text{F}$, $C_{OUT1} = 1\ \mu\text{F}$, and $C_{OUT2} = 1\ \mu\text{F}$, unless otherwise noted. Typical values are at $T_A = 25^\circ\text{C}$.

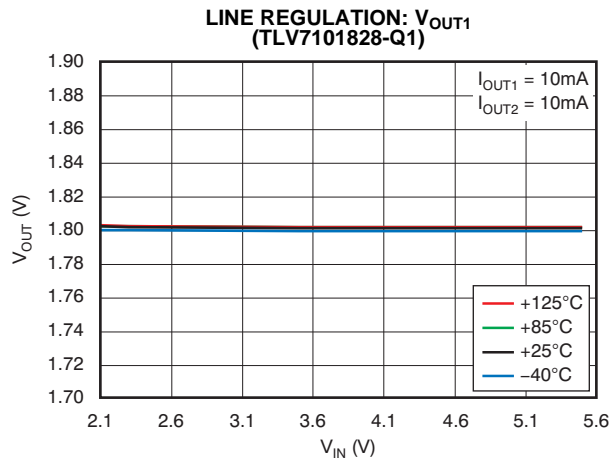


Figure 2.

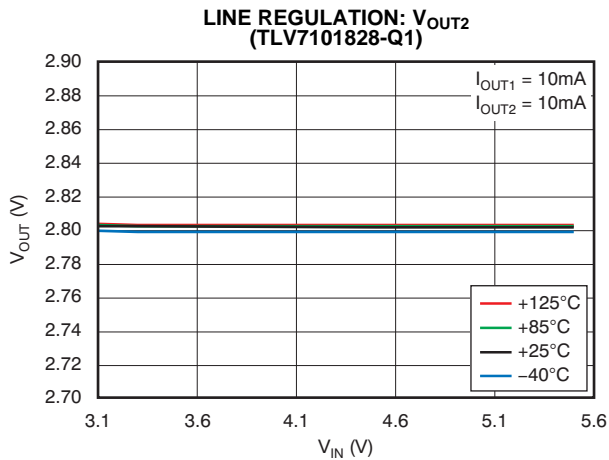


Figure 3.

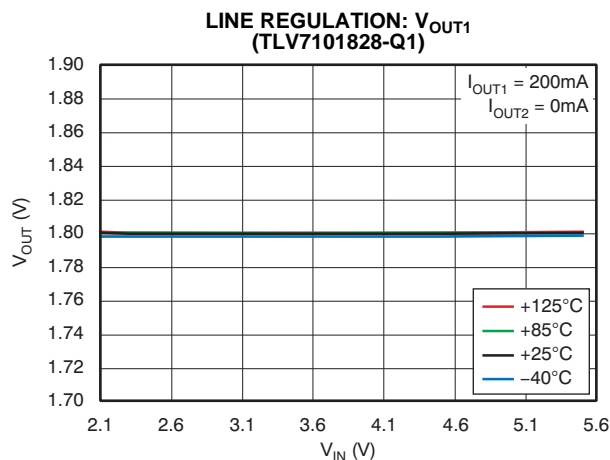


Figure 4.

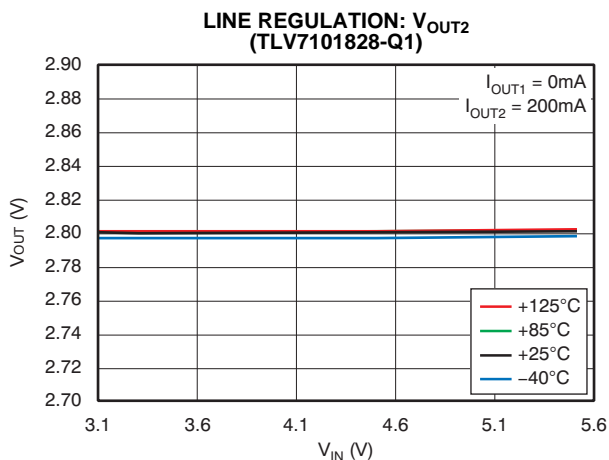


Figure 5.

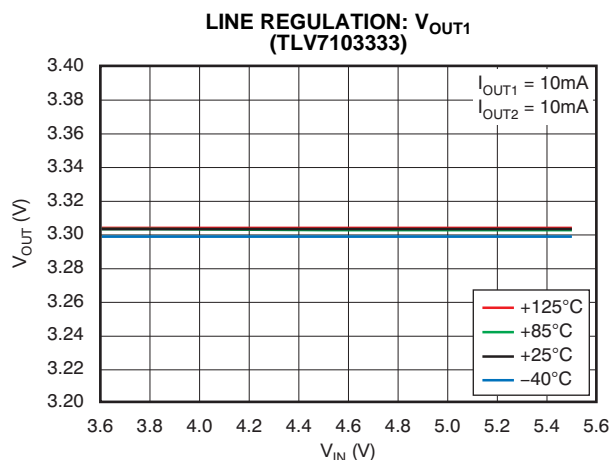


Figure 6.

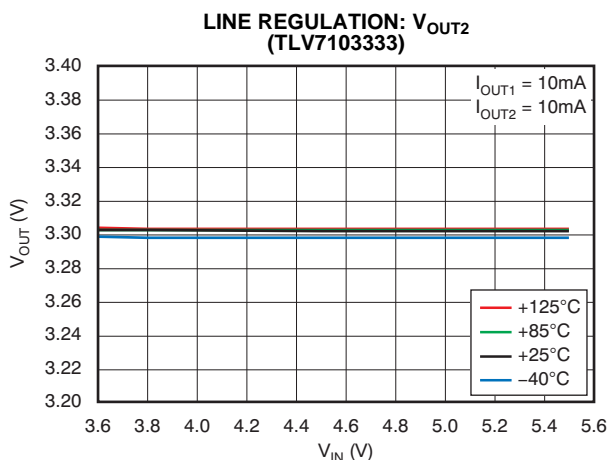


Figure 7.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of $T_A = -40^{\circ}\text{C}$ to 125°C , $V_{EN1} = V_{EN2} = V_{IN}$, $C_{IN} = 1\ \mu\text{F}$, $C_{OUT1} = 1\ \mu\text{F}$, and $C_{OUT2} = 1\ \mu\text{F}$, unless otherwise noted. Typical values are at $T_A = 25^{\circ}\text{C}$.

**LINE REGULATION: V_{OUT1}
(TLV7103333)**

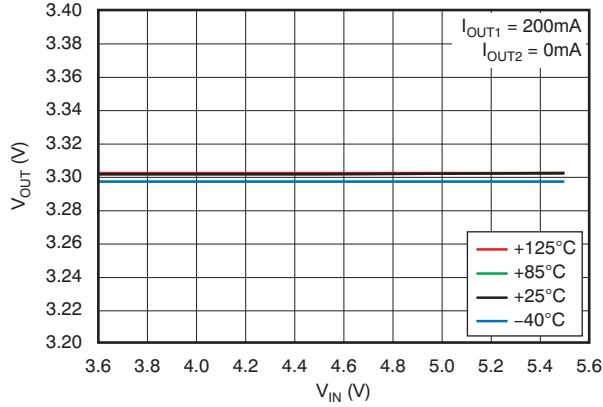


Figure 8.

**LINE REGULATION: V_{OUT2}
(TLV7103333)**

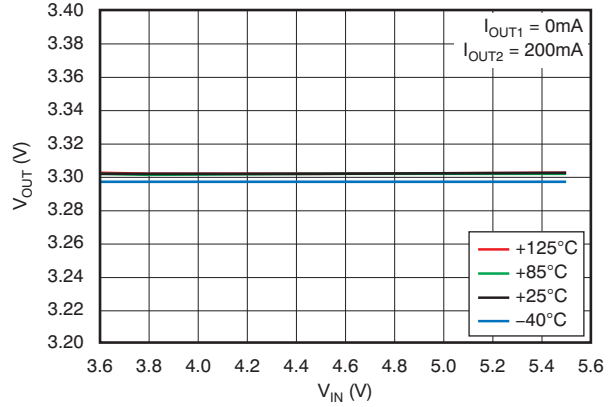


Figure 9.

**LOAD REGULATION: V_{OUT1}
(TLV7101828-Q1)**

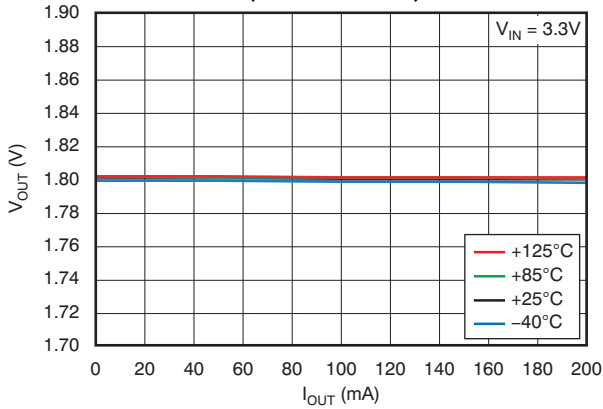


Figure 10.

**LOAD REGULATION: V_{OUT2}
(TLV7101828-Q1)**

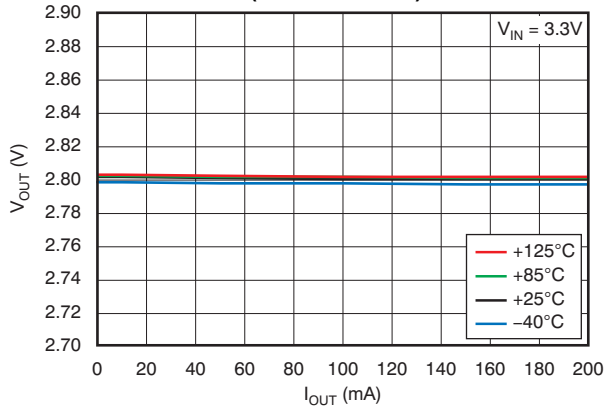


Figure 11.

**LOAD REGULATION: V_{OUT1}
(TLV7103333)**

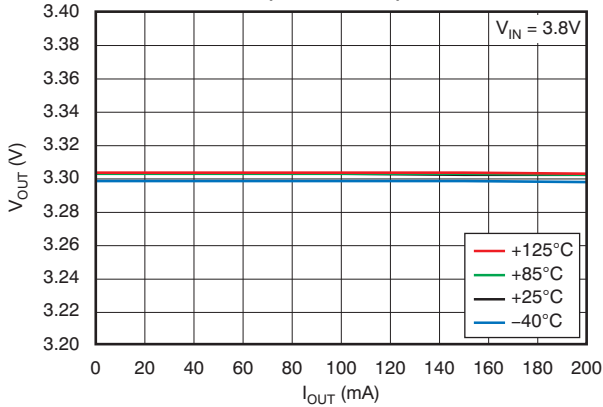


Figure 12.

**LOAD REGULATION: V_{OUT2}
(TLV7103333)**

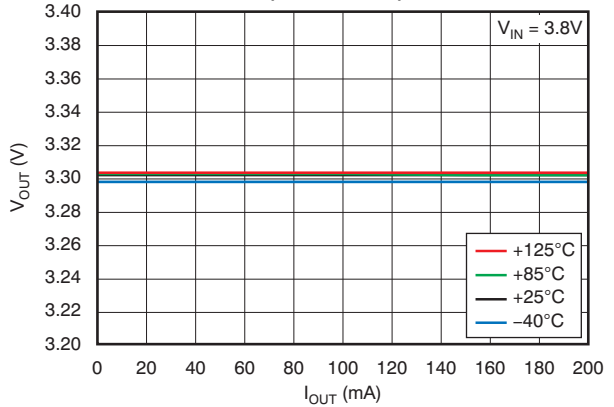


Figure 13.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of $T_A = -40^\circ\text{C}$ to 125°C , $V_{EN1} = V_{EN2} = V_{IN}$, $C_{IN} = 1\ \mu\text{F}$, $C_{OUT1} = 1\ \mu\text{F}$, and $C_{OUT2} = 1\ \mu\text{F}$, unless otherwise noted. Typical values are at $T_A = 25^\circ\text{C}$.

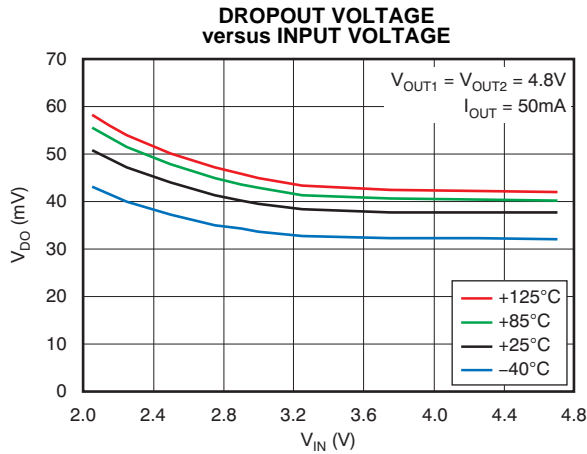


Figure 14.

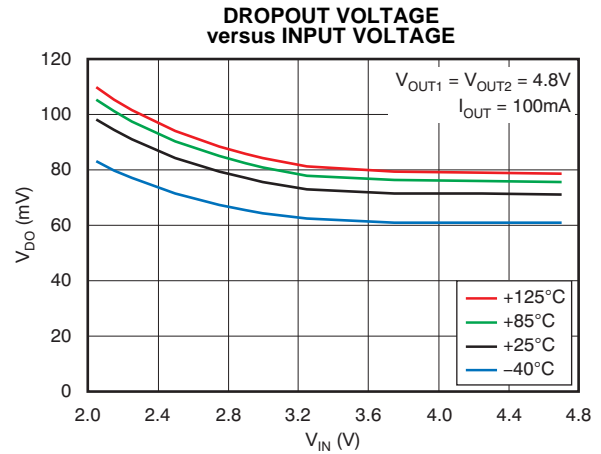


Figure 15.

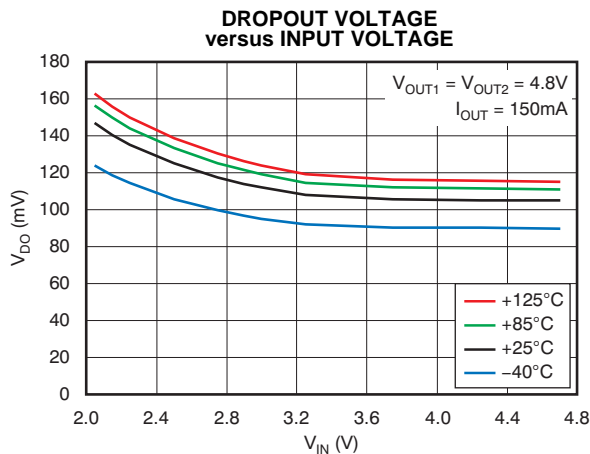


Figure 16.

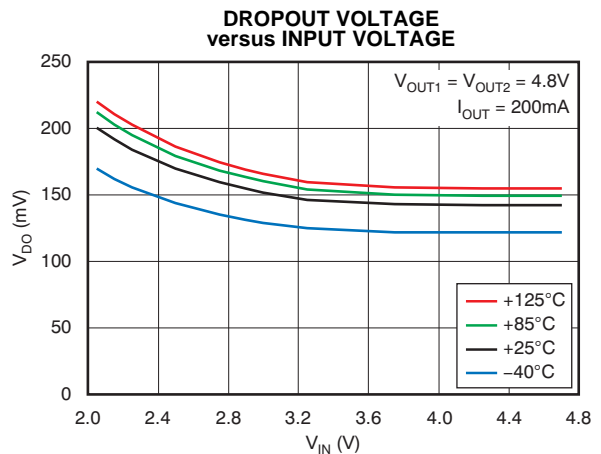


Figure 17.

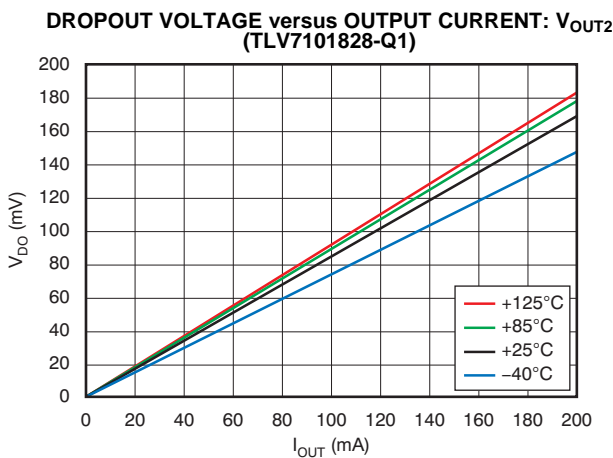


Figure 18.

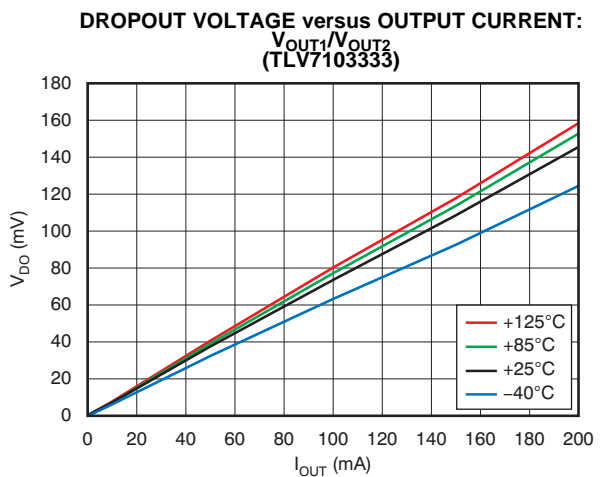


Figure 19.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of $T_A = -40^{\circ}\text{C}$ to 125°C , $V_{EN1} = V_{EN2} = V_{IN}$, $C_{IN} = 1\ \mu\text{F}$, $C_{OUT1} = 1\ \mu\text{F}$, and $C_{OUT2} = 1\ \mu\text{F}$, unless otherwise noted. Typical values are at $T_A = 25^{\circ}\text{C}$.

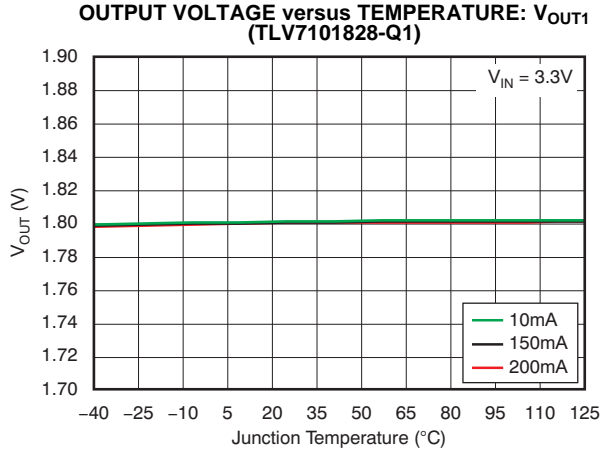


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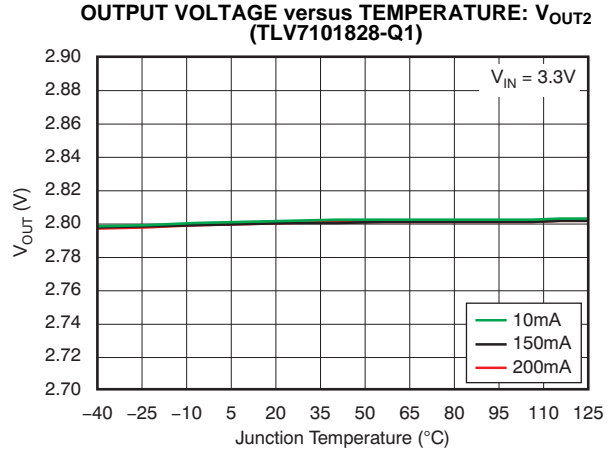


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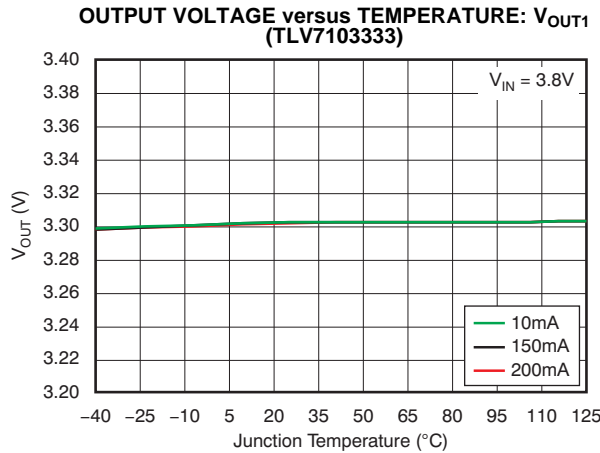


Figure 22.

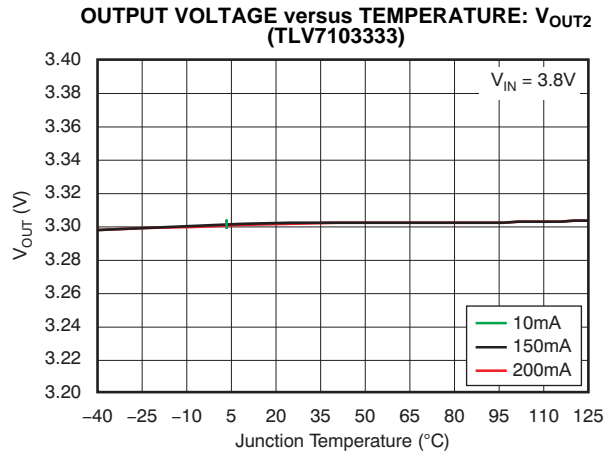


Figure 23.

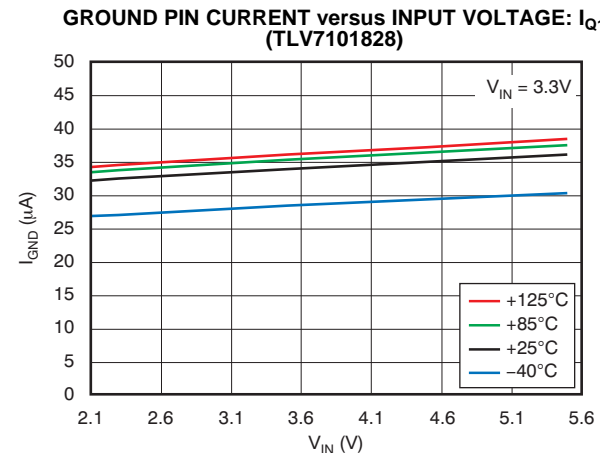


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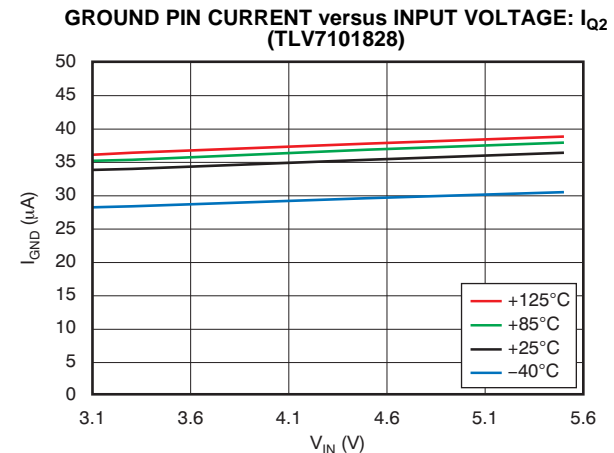


Figure 25.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of $T_A = -40^\circ\text{C}$ to 125°C , $V_{EN1} = V_{EN2} = V_{IN}$, $C_{IN} = 1\ \mu\text{F}$, $C_{OUT1} = 1\ \mu\text{F}$, and $C_{OUT2} = 1\ \mu\text{F}$, unless otherwise noted. Typical values are at $T_A = 25^\circ\text{C}$.

GROUND PIN CURRENT versus INPUT VOLTAGE: I_{Q1} (TLV7103333)

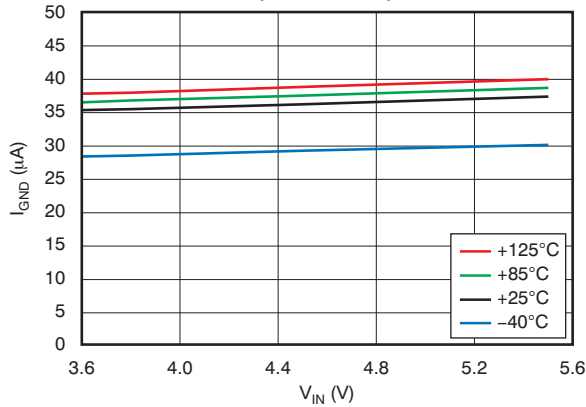


Figure 26.

GROUND PIN CURRENT versus INPUT VOLTAGE: I_{Q2} (TLV7103333)

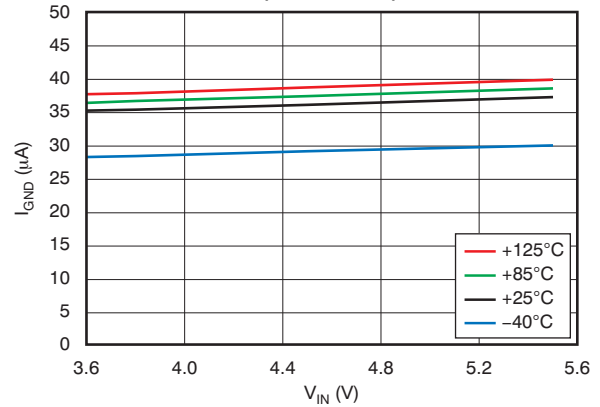


Figure 27.

GROUND PIN CURRENT versus LOAD: I_{Q1} (TLV7101828)

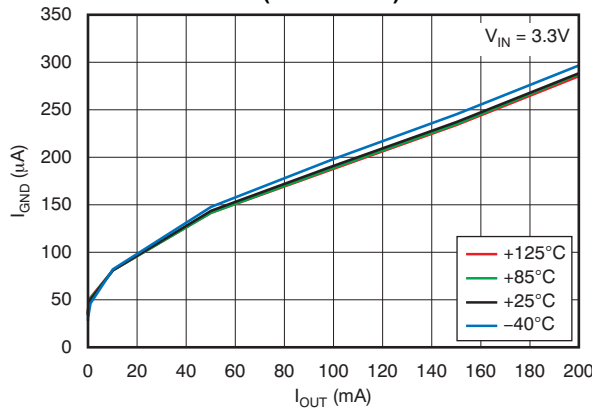


Figure 28.

GROUND PIN CURRENT versus LOAD: I_{Q2} (TLV7103333)

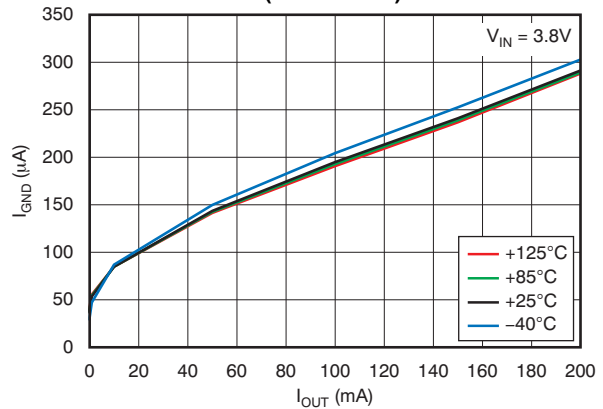


Figure 29.

SHUTDOWN CURRENT versus INPUT VOLTAGE (TLV7101828)

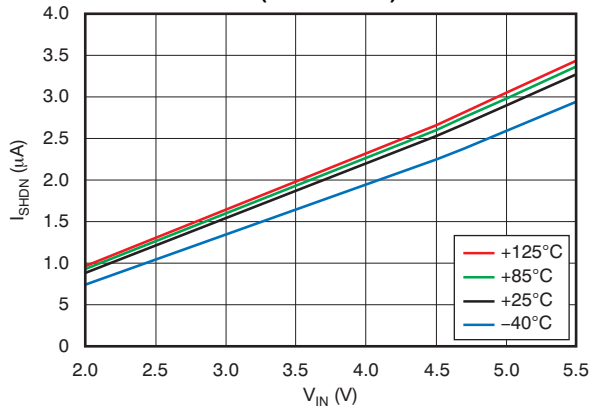


Figure 30.

SHUTDOWN CURRENT versus INPUT VOLTAGE (TLV7103333)

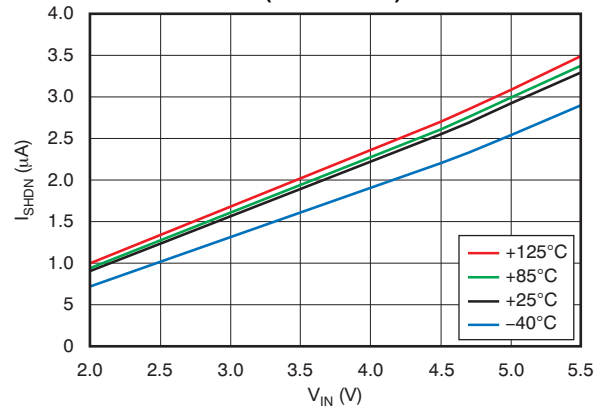


Figure 31.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of $T_A = -40^{\circ}\text{C}$ to 125°C , $V_{EN1} = V_{EN2} = V_{IN}$, $C_{IN} = 1\ \mu\text{F}$, $C_{OUT1} = 1\ \mu\text{F}$, and $C_{OUT2} = 1\ \mu\text{F}$, unless otherwise noted. Typical values are at $T_A = 25^{\circ}\text{C}$.

CURRENT LIMIT versus INPUT VOLTAGE: I_{CL1}
(TLV7101828)

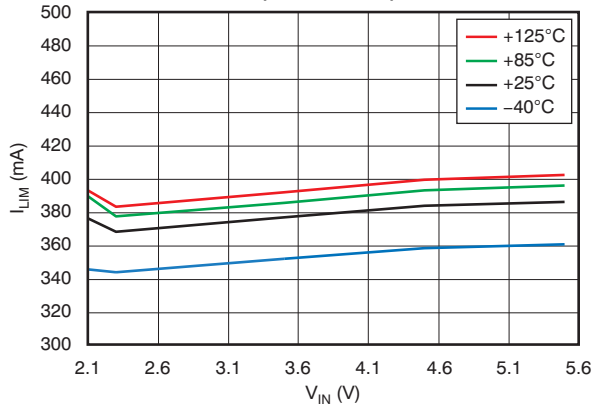


Figure 32.

CURRENT LIMIT versus INPUT VOLTAGE: I_{CL2}
(TLV7101828)

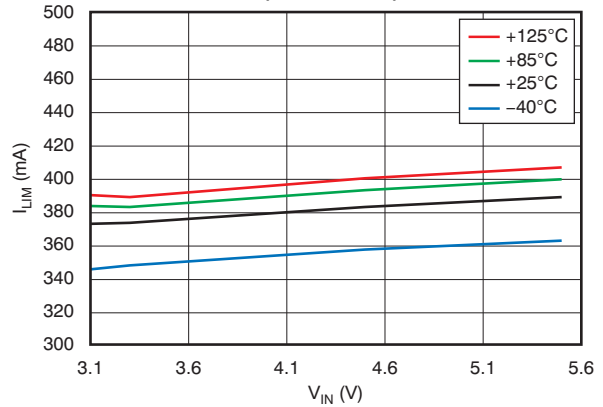


Figure 33.

CURRENT LIMIT versus INPUT VOLTAGE: I_{CL1}
(TLV7103333)

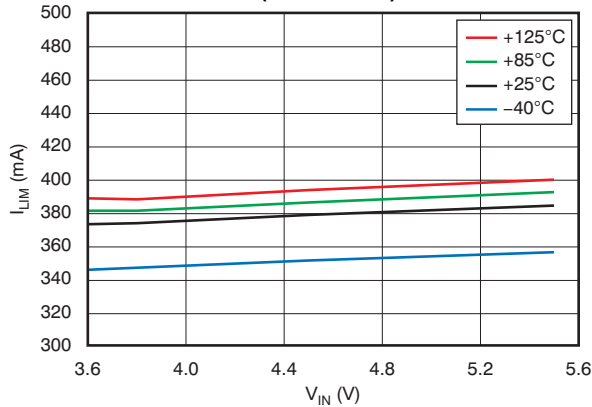


Figure 34.

CURRENT LIMIT versus INPUT VOLTAGE: I_{CL2}
(TLV7103333)

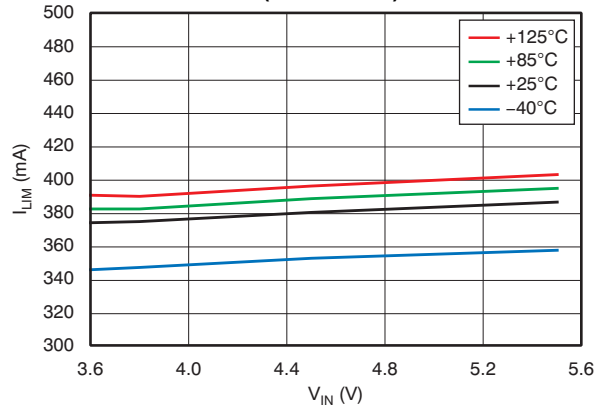


Figure 35.

POWER-SUPPLY RIPPLE REJECTION versus FREQUENCY
(TLV7101828)

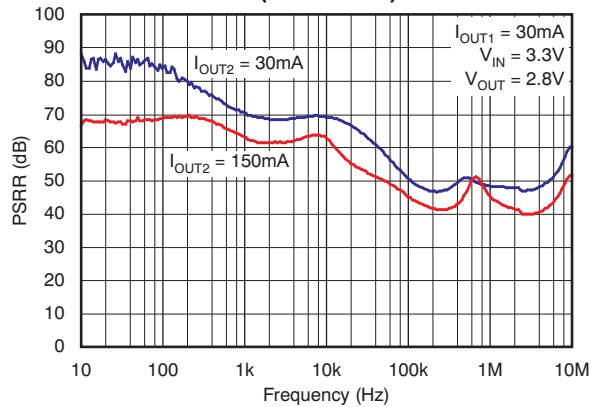


Figure 36.

POWER-SUPPLY RIPPLE REJECTION versus FREQUENCY
(TLV7103333)

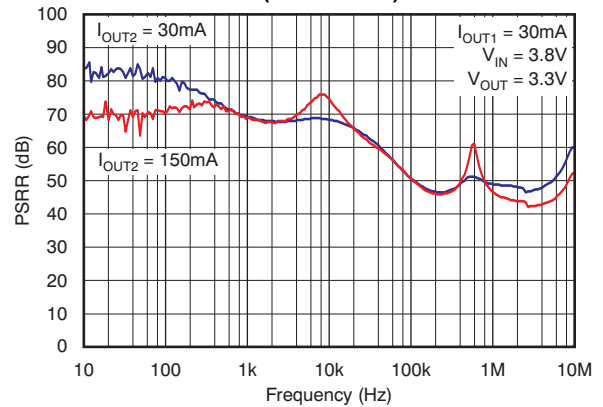


Figure 37.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of $T_A = -40^{\circ}\text{C}$ to 125°C , $V_{EN1} = V_{EN2} = V_{IN}$, $C_{IN} = 1\ \mu\text{F}$, $C_{OUT1} = 1\ \mu\text{F}$, and $C_{OUT2} = 1\ \mu\text{F}$, unless otherwise noted. Typical values are at $T_A = 25^{\circ}\text{C}$.

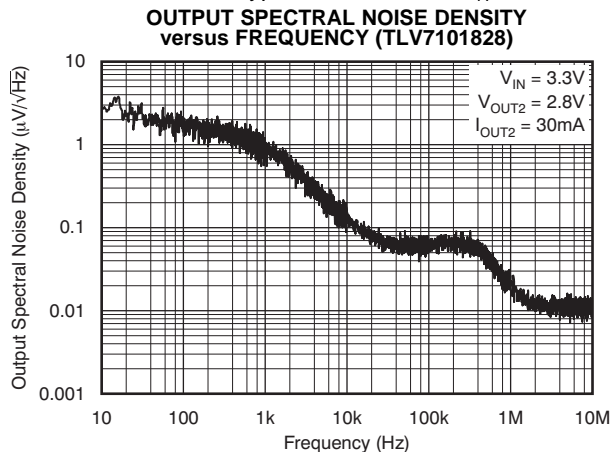


Figure 38.

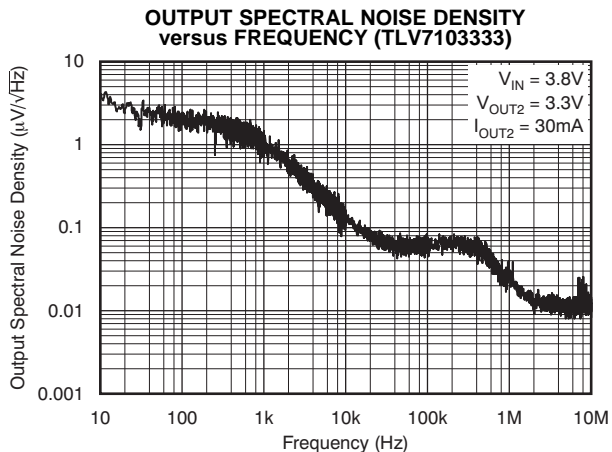


Figure 39.

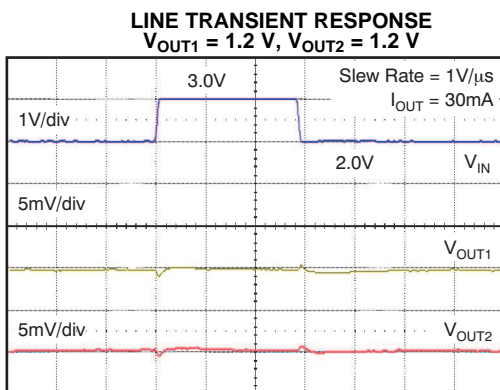


Figure 40.

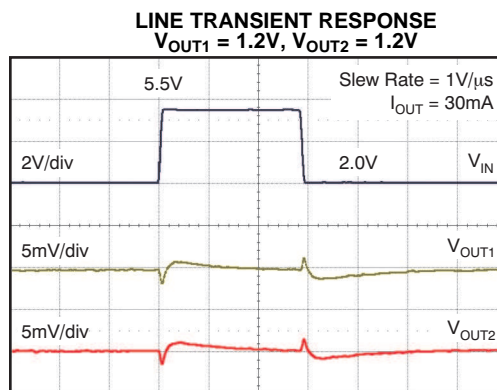


Figure 41.

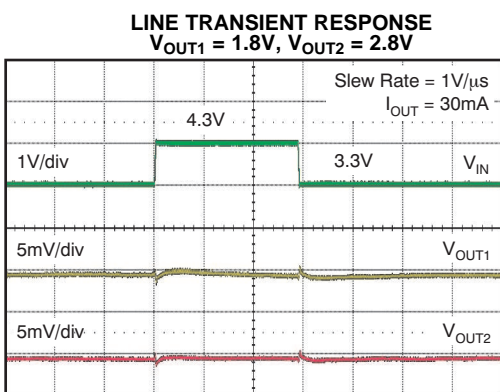


Figure 42.

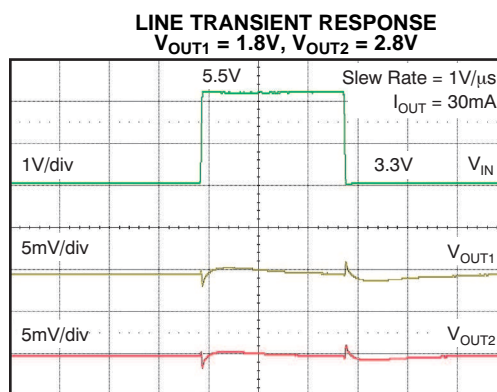
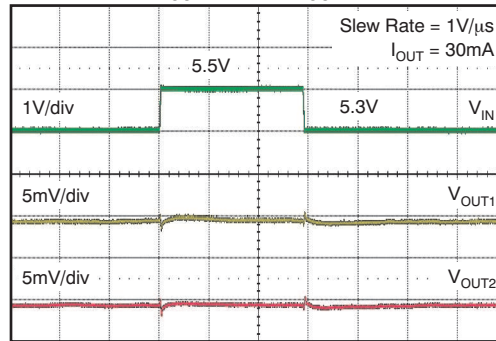


Figure 43.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of $T_A = -40^{\circ}\text{C}$ to 125°C , $V_{EN1} = V_{EN2} = V_{IN}$, $C_{IN} = 1\ \mu\text{F}$, $C_{OUT1} = 1\ \mu\text{F}$, and $C_{OUT2} = 1\ \mu\text{F}$, unless otherwise noted. Typical values are at $T_A = 25^{\circ}\text{C}$.

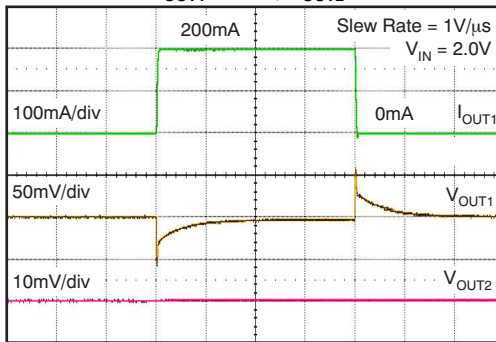
LINE TRANSIENT RESPONSE $V_{OUT1} = 4.8\text{V}$, $V_{OUT2} = 4.8\text{V}$



Time (200 μs /div)

Figure 44.

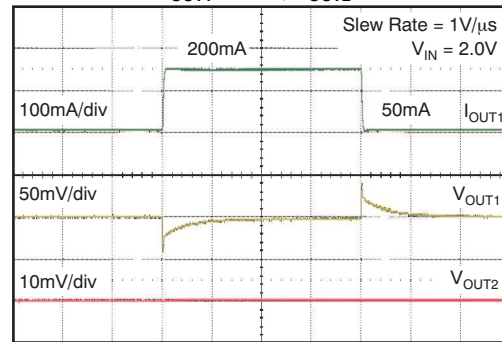
LOAD TRANSIENT RESPONSE AND CROSSTALK $V_{OUT1} = 1.2\text{V}$, $V_{OUT2} = 1.2\text{V}$



Time (50 μs /div)

Figure 45.

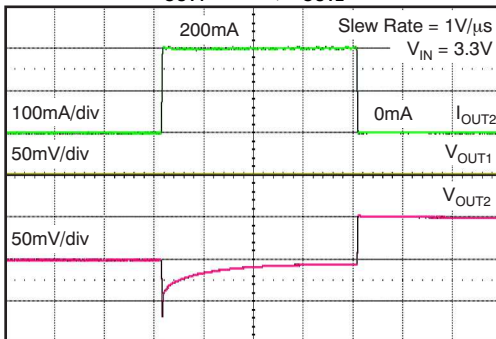
LOAD TRANSIENT RESPONSE AND CROSSTALK $V_{OUT1} = 1.2\text{V}$, $V_{OUT2} = 1.2\text{V}$



Time (50 μs /div)

Figure 46.

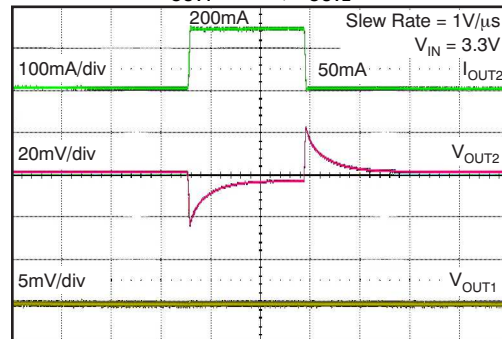
LOAD TRANSIENT RESPONSE AND CROSSTALK $V_{OUT1} = 1.8\text{V}$, $V_{OUT2} = 2.8\text{V}$



Time (50 μs /div)

Figure 47.

LOAD TRANSIENT RESPONSE AND CROSSTALK $V_{OUT1} = 1.8\text{V}$, $V_{OUT2} = 2.8\text{V}$



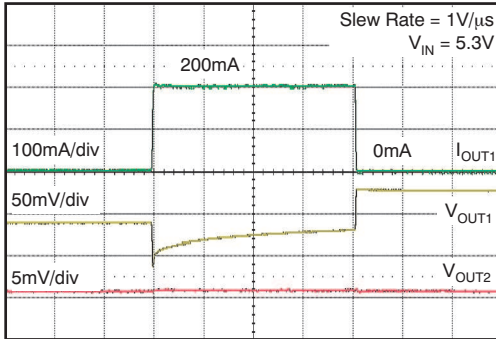
Time (50 μs /div)

Figure 48.

TYPICAL CHARACTERISTICS (continued)

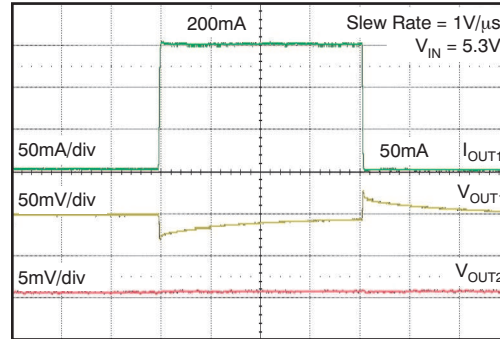
Over operating temperature range of $T_A = -40^{\circ}\text{C}$ to 125°C , $V_{EN1} = V_{EN2} = V_{IN}$, $C_{IN} = 1\ \mu\text{F}$, $C_{OUT1} = 1\ \mu\text{F}$, and $C_{OUT2} = 1\ \mu\text{F}$, unless otherwise noted. Typical values are at $T_A = 25^{\circ}\text{C}$.

LOAD TRANSIENT RESPONSE AND CROSSTALK
 $V_{OUT1} = 4.8\text{V}$, $V_{OUT2} = 4.8\text{V}$



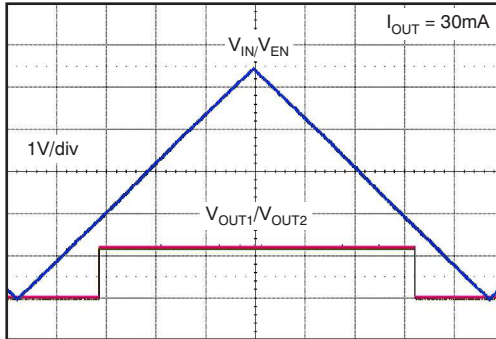
Time (50μs/div)
Figure 49.

LOAD TRANSIENT RESPONSE AND CROSSTALK
 $V_{OUT1} = 4.8\text{V}$, $V_{OUT2} = 4.8\text{V}$



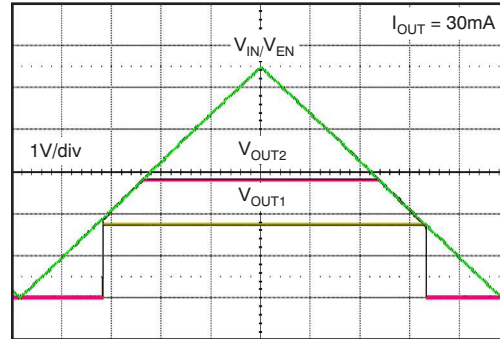
Time (50μs/div)
Figure 50.

V_{IN} RAMP UP, RAMP DOWN RESPONSE
 $V_{OUT1} = 1.2\text{V}$, $V_{OUT2} = 1.2\text{V}$



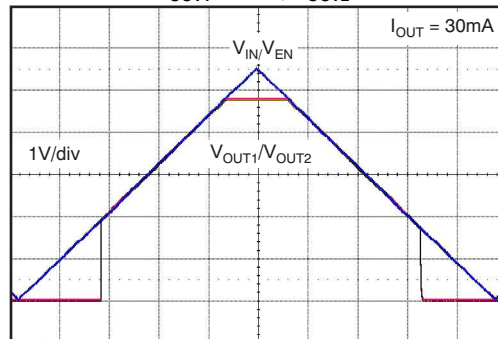
Time (200ms/div)
Figure 51.

V_{IN} RAMP UP, RAMP DOWN RESPONSE
 $V_{OUT1} = 1.8\text{V}$, $V_{OUT2} = 2.8\text{V}$



Time (200ms/div)
Figure 52.

V_{IN} RAMP UP, RAMP DOWN RESPONSE
 $V_{OUT1} = 4.8\text{V}$, $V_{OUT2} = 4.8\text{V}$



Time (200ms/div)
Figure 53.

APPLICATION INFORMATION

The TLV7103318-Q1 and TLV7101828-Q1 devices belong to a new family of next-generation, value LDO regulators. These devices consume low quiescent current and deliver excellent line and load transient performance. These features, combined with low noise, very good PSRR with little (V_{IN} to V_{OUT}) headroom, make these devices ideal for RF portable applications. This family of LDO regulators offers current limit and thermal protection, and is specified from -40°C to 125°C .

INPUT AND OUTPUT CAPACITOR REQUIREMENTS

1.0 μF X5R- and X7R-type ceramic capacitors are recommended because they have minimal variation in value and equivalent series resistance (ESR) over temperature.

However, the TLV7103318-Q1 and TLV7101828-Q1 are designed to be stable with an effective capacitance of 0.1 μF or larger at the output. Thus, the device would also be stable with capacitors of other dielectrics, as long as the effective capacitance under operating bias voltage and temperature is greater than 0.1 μF . This effective capacitance refers to the capacitance that the device sees under operating bias voltage and temperature conditions (that is, the capacitance after taking bias voltage and temperature derating into consideration.)

In addition to allowing the use of cost-effective dielectrics, these devices also enable using smaller footprint capacitors that have a higher derating in size-constrained applications.

Note that using a 0.1- μF rating capacitor at the output of the LDO regulator does not ensure stability because the effective capacitance under operating conditions would be less than 0.1 μF . The maximum ESR should be less than 200 m Ω .

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1 μF to 1.0 μF low ESR capacitor across the IN and GND pins of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast-rise-time load transients are anticipated, or if the device is not located near the power source. If source impedance is more than 2 Ω , a 0.1 μF input capacitor may be necessary to ensure stability.

BOARD LAYOUT RECOMMENDATIONS TO

IMPROVE PSRR AND NOISE PERFORMANCE

Input and output capacitors should be placed as close to the device pins as possible. To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT} , with the ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should be connected directly to the GND pin of the device. High ESR capacitors may degrade PSRR.

INTERNAL CURRENT LIMIT

The TLV7103318-Q1 and TLV7101828-Q1 internal current limits help protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. In such a case, the output voltage is not regulated, and is $V_{OUT} = I_{LIMIT} \times R_{LOAD}$.

The PMOS pass transistor dissipates $(V_{IN} - V_{OUT}) \times I_{LIMIT}$ until thermal shutdown is triggered and the device is turned off. As the device cools down, it is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between current limit and thermal shutdown. See the [Thermal Information](#) section for more details. The PMOS pass element in the TLV7103318-Q1 and TLV7101828-Q1 has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of rated output current is recommended.

SHUTDOWN

The enable pin (EN) is active high. The device is enabled when EN pin goes above 0.9V. This relatively lower value of voltage needed to turn the LDO regulator on can be used to enable the device with the GPIO of recent processors whose GPIO voltage is lower than traditional microcontrollers.

The device is turned off when the EN pin is held at less than 0.4 V. When shutdown capability is not required, the EN pin can be connected to the IN pin.

DROPOUT VOLTAGE

The TLV7103318-Q1 and TLV7101828-Q1 use a PMOS pass transistor to achieve low dropout. When $(V_{IN} - V_{OUT})$ is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with the output current because the PMOS device behaves as a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded as $(V_{IN} - V_{OUT})$ approaches dropout.

TRANSIENT RESPONSE

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response.

The TLV7103318-Q1 and TLV7101828-Q1 each have a dedicated V_{REF} . Consequently, crosstalk from one channel to the other as a result of transients is close to 0V.

UNDERVOLTAGE LOCKOUT (UVLO)

The TLV7103318-Q1 and TLV7101828-Q1 use an undervoltage lockout circuit to keep the output shut off until the internal circuitry is operating properly.

THERMAL INFORMATION

Thermal protection disables the output when the junction temperature rises to approximately 165°C, allowing the device to cool. When the junction temperature cools to approximately 145°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered;

use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TLV7103318-Q1 and TLV7101828-Q1 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TLV710-Q1 into thermal shutdown degrades device reliability.

POWER DISSIPATION

The ability to remove heat from a die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air.

Performance data for the TLV710-Q1 evaluation module (EVM) are shown in [Table 1](#). The EVM is a 2-layer board with 2 ounces of copper per side. The dimension and layout are shown in [Figure 54](#) and [Figure 55](#). Using heavier copper increases the effectiveness of removing heat from the device. The addition of plated through-holes in the heat-dissipating layer also improves the heatsink effectiveness. Power dissipation depends on input voltage and load conditions.

Power dissipation (P_D) is equal to the product of the output current and the voltage drop across the output pass element, as shown in [Equation 1](#):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (1)$$

PACKAGE MOUNTING

Solder pad footprint recommendations for the TLV7103318-Q1 and TLV7101828-Q1 are available from the Texas Instruments Web site at www.ti.com. The recommended land pattern for the DSE (SON-6) package is shown in .

Table 1. TLV7103318-Q1 and TLV7101828-Q1 EVM Dissipation Ratings

PACKAGE	$R_{\theta JA}$	$T_A < 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$	$T_A = 125^\circ\text{C}$
DSE	170°C/W	585 mW	235 mW	mW

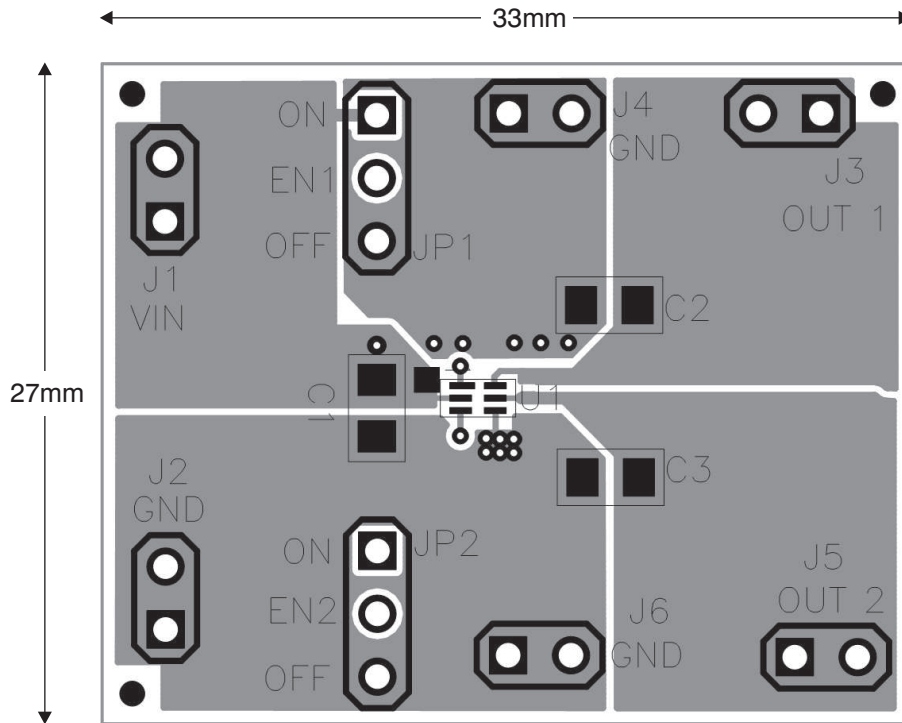


Figure 54. Top Layer

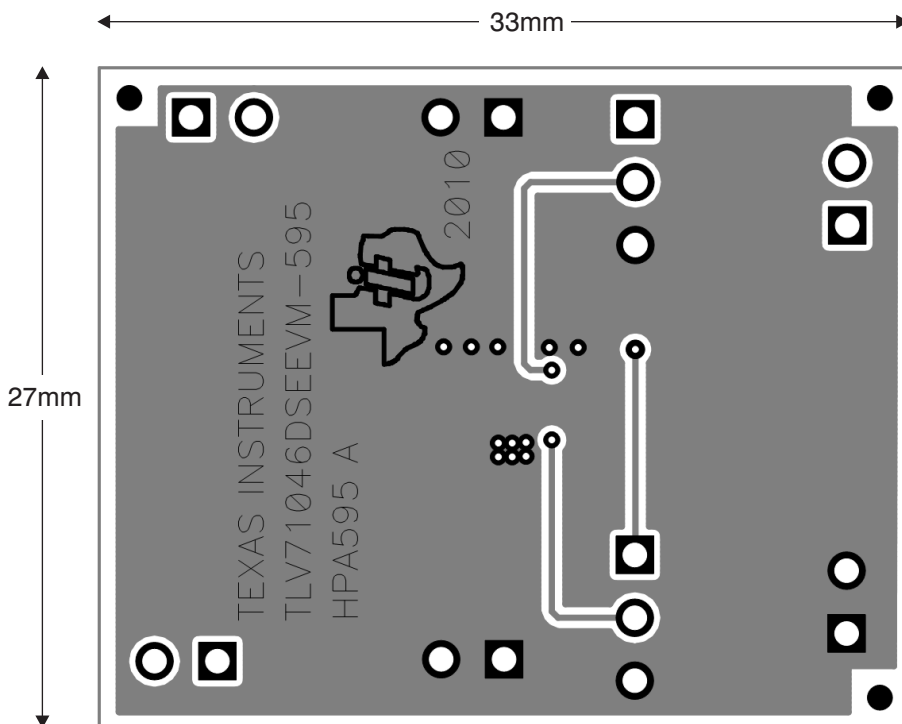


Figure 55. Bottom Layer

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV7101828QDSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CP	Samples
TLV7103318QDSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZD	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TLV710-Q1 :

- Catalog: [TLV710](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV7101828QDSERQ1	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV7103318QDSERQ1	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2

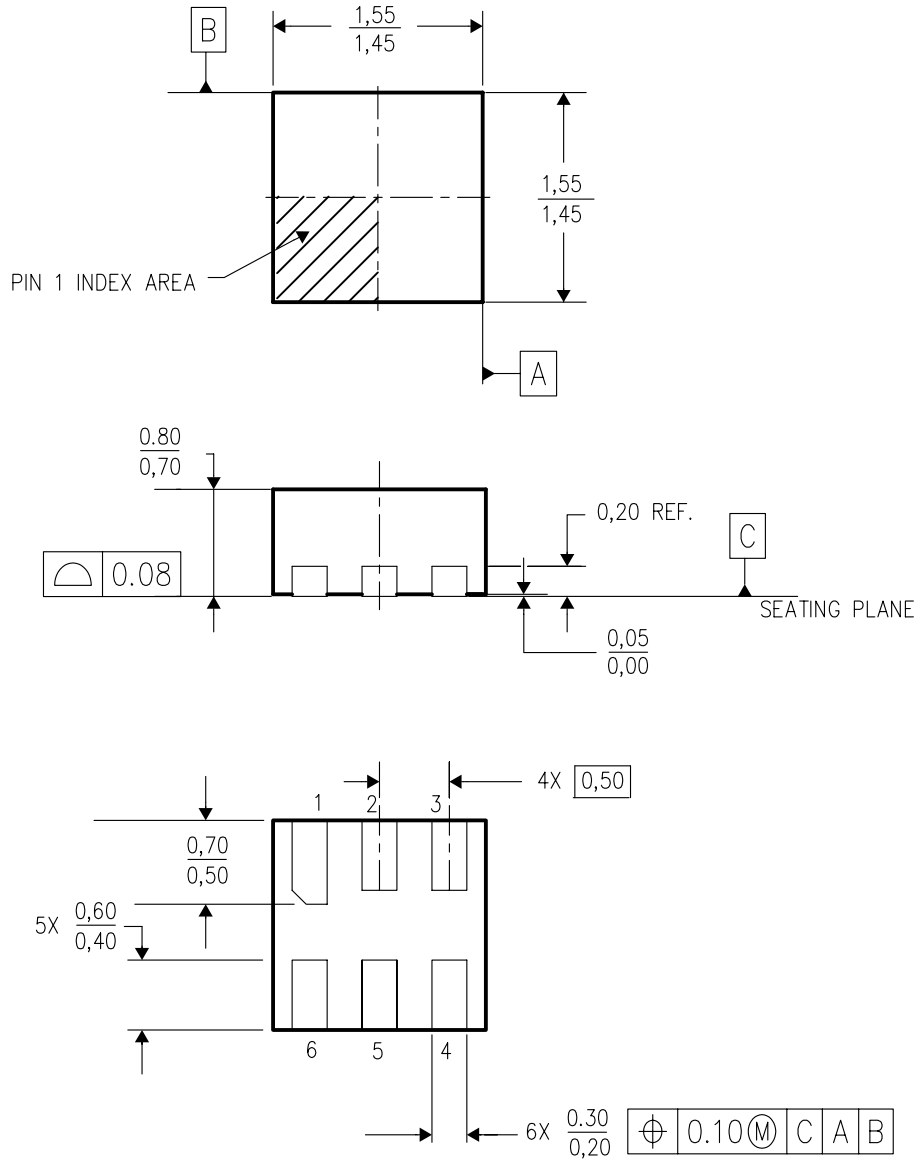
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV7101828QDSERQ1	WSON	DSE	6	3000	200.0	183.0	25.0
TLV7103318QDSERQ1	WSON	DSE	6	3000	200.0	183.0	25.0

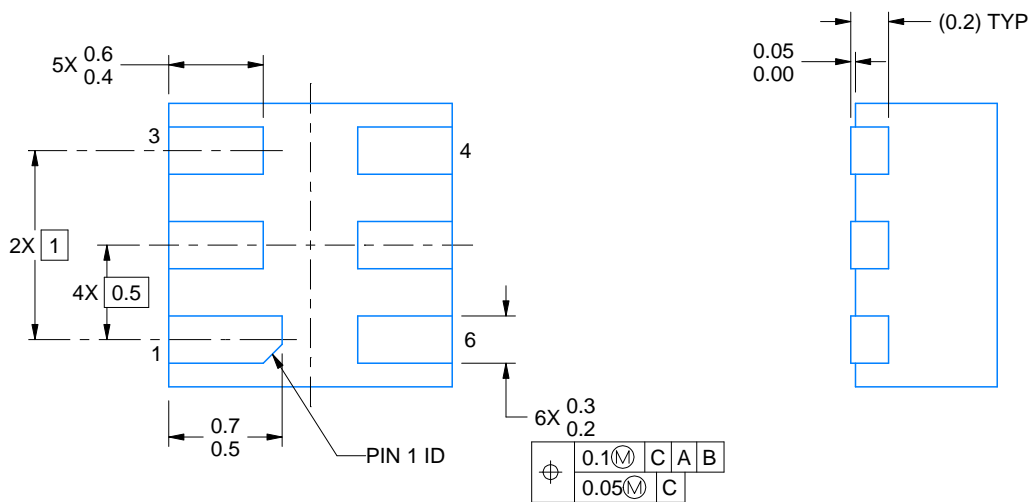
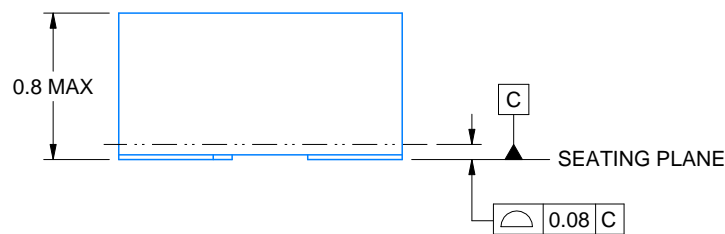
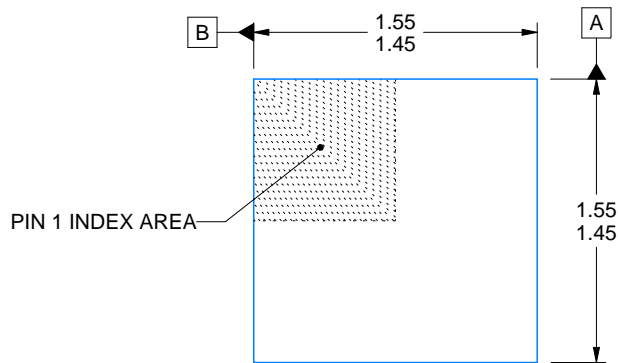
DSE (S-PDSO-N6)

PLASTIC SMALL OUTLINE



4207810/A 03/06

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Small Outline No-Lead (SON) package configuration.
 - D. This package is lead-free.



4220552/A 04/2021

NOTES:

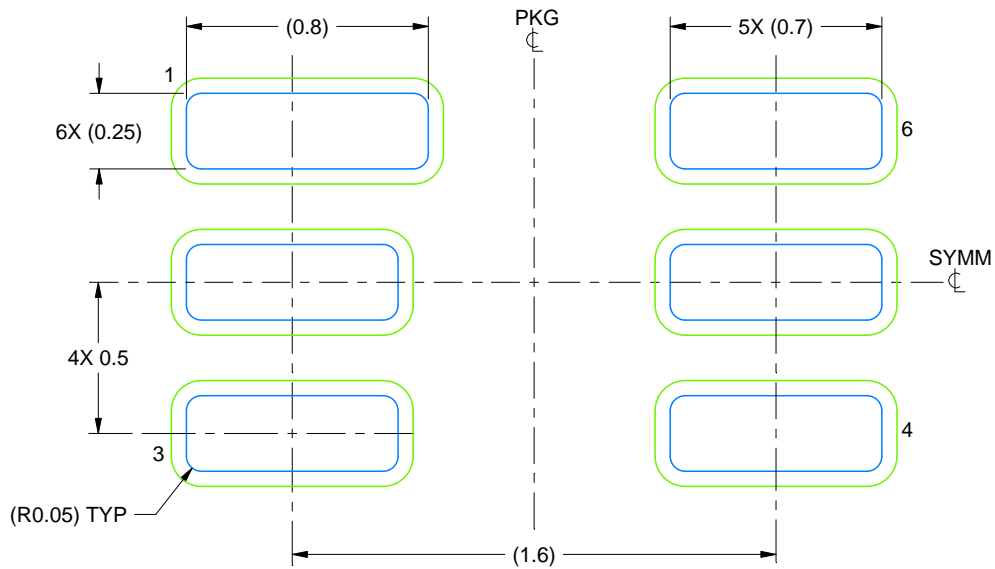
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

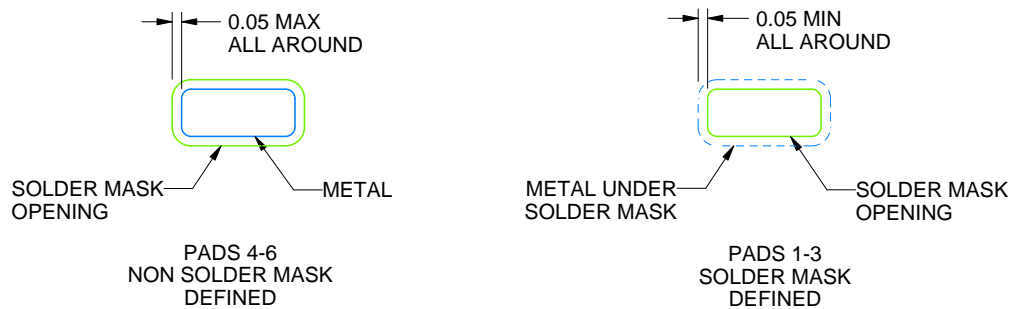
DSE0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS

4220552/A 04/2021

NOTES: (continued)

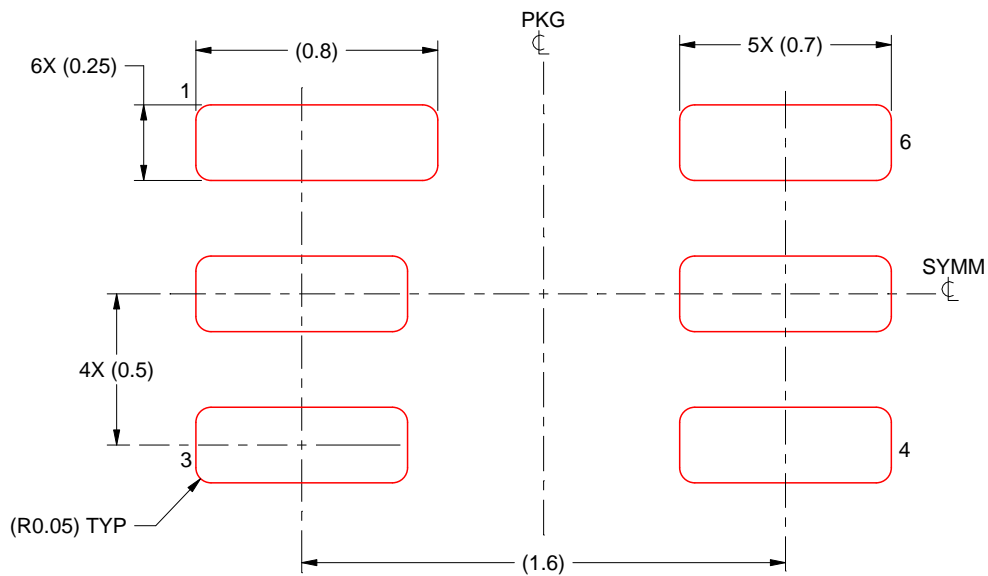
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSE0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:40X

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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