I²C-BUS OR SPI BUS LOW VOLTAGE (LV) GPIO

NXP'S "AGILE I/O" VERSIONS REDUCE SYSTEM COST AND EASE SOFTWARE DEVELOPMENT

These I²C-Bus or SPI Bus Low Voltage (LV) GPIO, available in industry-standard configurations or with special integrated functions, reduce board space and simplify firmware development for a lower overall system cost.

KEY FEATURES

- Low-voltage operation: 1.6 to 5.5 V I/O ports and 0.8 to 3.6 V (24 and 34 bit) or 1.65 to 5.5V (8 and 16 bit) I²C Interface or 1.1 to 5.5 V (14 and 22 bit) SPI Interface
- Low standby current consumption: 3 µA max.
- Bidirectional voltage-level translation and GPIO expansion between 0.8, 1.8, 2.5, 3.3, or 5 V µC Interface and 1.8, 2.5, 3.3, or 5 V totem-pole configured I/O port
- I²C-bus: 400 KHz (8 and 16 bit) and 1000 KHz (24 and 34 bit) or SPI Bus: 5 MHz (14 and 22 bit)
- Active LOW reset input
- Open-drain active LOW interrupt output
- 5 V tolerant I/O ports
- High current drive outputs drive LEDs directly
- Internal power-on reset
- Power-up with all channels configured as inputs
- No glitch on power-up
- Packages: 16/24/32/42-pin TSSOP, HWQFN, HVQFN, XQFN, VFBGA, and land grid array

UNIQUE FEATURES OF "AGILE I/O" VERSIONS

- Backward-compatible with industry-standard versions
- New registers to control configurable features
- Input latch locks in any changes on input pins until the input port register is read
- Programmable pull-up or pull-down resistors
- Output drive strength selectable to ¼, ½, ¾ or max to conserve battery power and reduce power-supply noise when simultaneous outputs switch
- Interrupt mask to limit interrupt sources
- Interrupt status register shows interrupt source
- Output selection of open-drain or push-pull configuration

NXP's family of low-voltage (LV) GPIO with Agile I/O expand the two wires of the I²C-bus or four wires of the SPI Bus into general-purpose I/O pins that can interface to keyboards, switches, LEDs, displays, or even stepping motors — saving valuable pins on the microprocessor or custom ASIC. The lower voltage devices that don't implement Agile I/O are 100% compatible with industry-standard devices, giving users supply alternatives and the advantage of second sources.

FAMILY DIFFERENCES

Devices in the LV GPIO family are differentiated by the number of I/O pins and other features like Reset and Interrupt. To aid in PCB layout, the device pinouts are similar. This lets the designer select the family and delay feature selection until later in the process.

Low-voltage operation and low current consumption make these devices ideal for a wide range of applications in portable, industrial, and automotive segments. Dual supply components allow for bidirectional level translation in systems that need to interface with the outside world.

	FEATURES	INDUSTRY-STANDARD DEVICE (2.3 TO 5.5 V)	NXP LV DEVICE (1.65 TO 5.5 V)	NXP LV DEVICE WITH AGILE I/O (1.65 TO 5.5 V)	NXP LV DEVICE WITH DUAL V_{DD} FOR VOLTAGE LEVEL TRANSLATION
8-bit	Interrupt	PCA9534			PCA(L)6408A
	Interrupt and reset	PCA9538	PCA9538A	PCAL9538A	
	Interrupt and pull-up	PCA9554 PCA9554A	PCA9554B PCA9554C	PCAL9554B PCAL9554C	
16-bit	Interrupt	PCA9535	PCA9535A	PCAL9535A	PCA(L)6416A PCAL9714 – 14 bit SPI
	Interrupt and reset	PCA9539	PCA9539A	PCAL9539A	
	Interrupt and pull-up	PCA9555	PCA9555A	PCAL9555A	
24-bit	Interrupt and reset				PCAL6524 PCAL9722 – 22 bit SPI
34-bit	Interrupt and reset				PCAL6534

RESET INPUT

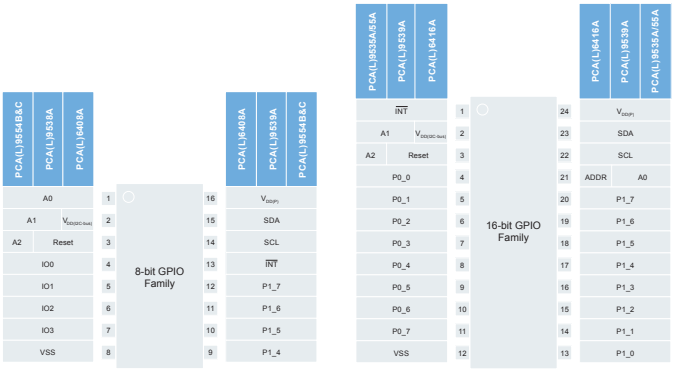
The Reset input initializes the device to its default state without removing power — the normal way to restore the default condition. This is useful in situations where the bus has a noise glitch which prevents proper transmission of data between the microprocessor and target devices. Any incorrect data can be eliminated by resetting the device. Using the Reset pin is also a convenient method for placing the device in a known state for programming. Target devices without a Reset input must lower their power supply to 0 V and then power back up to V_{DD} before the target device can return to its default state — and this can be inefficient and time-consuming for the system.

INTERRUPT OUTPUT

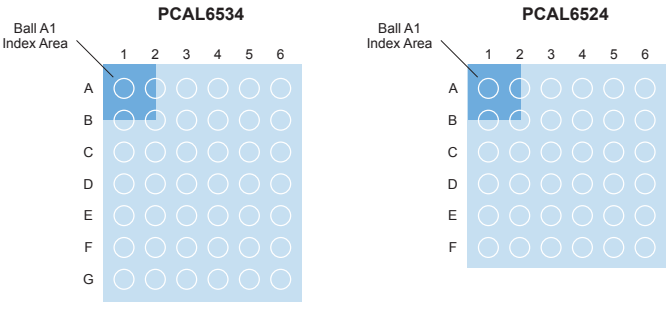
The interrupt output is activated when any input pin changes state. The interrupt output directly notifies the system controller or microprocessor that an event has occurred. This saves on software overhead, because there's no need to continuously poll or read inputs to determine a state change.

LEVEL TRANSLATION

Another important element of the LV GPIO family is the ability to interface with different voltage levels. Modern microprocessors operate at reduced power supplies to minimize power consumption, but real-world signals often use much higher voltage levels. The dual V_{DD} LV GPIO family can interface to the microprocessor and withstand higher voltages on the inputs and outputs. Both the single and the dual V_{DD} versions have 5 V tolerant inputs.



	PCAL6524	PCAL6534
SCL	A3	A3
SDA	A2	A2
V_{DD}(I^2C-bus)	A1	A1
/INT	C4	B1
VSS	A6	B6
ADDR	A5	A4
VDD(P)	A4	A6
/RESET	B4	A5
I/O	All others	All others
No Connect	B2, B3, C2, C3	



AGILE I/O FEATURES

The groundbreaking Agile I/O features significantly reduce system cost while reducing development time, so products can get to market faster. These devices offer an unmatched range of configurable features, so the designer can customize the GPIO for the application. Some of the Agile I/O advanced features are: selectable output drive strength, outputs configurable as opendrain or push-pull outputs, configurable pull-up or pull-down resistors on the input pins, interrupt masking and interrupt status, and selectable input latches. Designers can easily switch from the industry-standard devices to Agile I/O parts with no change in the board design or software. Simply add the needed features as desired.

SELECTABLE OUTPUT DRIVE STRENGTH

Drive strength control allows one to modify the current drive capability of the output pin from 25%, 50% or 75% to 100%. Reducing the current drive capability may be desirable to reduce system noise. When the output switches (transitions from H/L), there is a peak current that is a function of the output drive selection. Switching many outputs at the same time will create ground and supply noise. The output drive strength control allows the user to minimize simultaneous switching noise issues without any additional external components.

OUTPUT CONFIGURATION

The output configuration customizes the outputs for optimum performance in the application. Previously, separate part numbers were needed for open-drain output versions or push-pull versions. With Agile I/O, outputs can be configured to either arrangement, which minimizes stocking levels and changes with a simple software configuration.

INPUT PULL-UP/PULL-DOWN RESISTORS

Input pull-up/pull-down resistors are needed to guarantee that inputs are at a valid logic level. This usually involves external discrete components that complicate routing and take up PCB area. The internal pull-up or pull-down resistors are integrated, minimizing the bill of materials, and can be enabled with a simple software command.

INPUT PULL-UP/PULL-DOWN RESISTORS

Input pull-up/pull-down resistors are needed to guarantee that inputs are at a valid logic level. This usually involves external discrete components that complicate routing and take up PCB area. The internal pull-up or pull-down resistors are integrated, minimizing the bill of materials, and can be enabled with a simple software command.

INTERRUPT MASK

The interrupt mask selects which inputs can cause an interrupt event on the $\overline{\text{INT}}$ output pin. Normally, any input transition will cause the $\overline{\text{INT}}$ pin to trigger an alert to the microprocessor. If one pin is connected to a signal that switches abnormally, this initiates a lot of unnecessary interrupt service software traffic on the microprocessor. By simply masking the abnormal input from generating an event on the $\overline{\text{INT}}$ pin, a large amount of software performance is saved with no extra hardware.

INTERRUPT STATUS

The interrupt status register shows which input caused an event on the $\overline{\text{INT}}$ pin, simplifying the interrupt service routine software and minimizing software development and verification, and system testing.

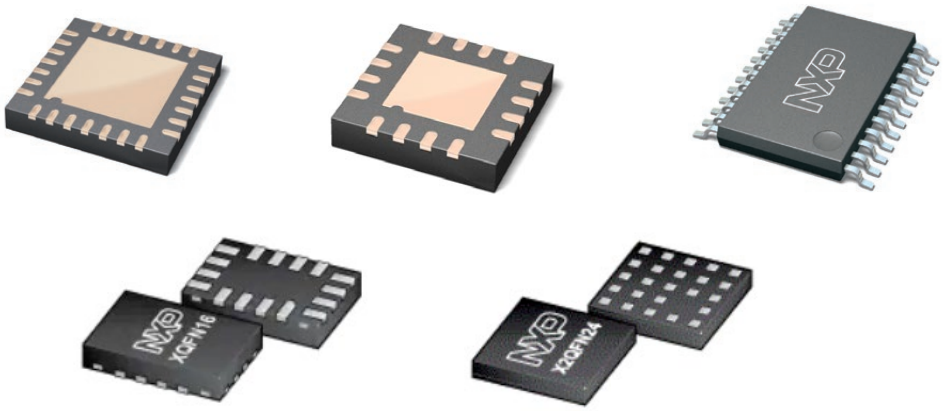
INPUT LATCH

The input latch feature eliminates external hardware by implementing latches on all input pins. This lets the microprocessor sample inputs at a reduced rate and still determine which inputs have changed states. This is important for interrupt service routines. Inputs can change states quickly, yet still require attention from the microprocessor software. The latch holds the input state until the software can read the input pins, putting fewer real-time demands on the microprocessor. This increases system reliability without additional hardware.

SPI BUS INTERFACE

PCAL97xx are SPI interface with the /Q900 versions AEC-Q100 compliant with wettable flanks HVQFN packages for automotive applications.

FEATURES	FUNCTION	BENEFIT
Output configuration	Select outputs as open drain or push-pull	• Tailor output characteristic to load • Eliminate different types of GPIO
Output drive strength control	Select output current drive	• Minimizes system noise when multiple outputs switch • Match to transmission line impedance
Input latch	Save the status of any input transitions	• Eliminates external latches • Simplifies software
Interrupt mask	Mask inputs from causing an interrupt	• Reduces interrupt traffic to micro • Improves interrupt service response
Input pull-up / pull-down resistors	Input pull-up / pull-down resistors	• Reduces bill of materials
Interrupt mask	Mask inputs from causing an interrupt	• Reduces bill of materials • Eliminates complex external logic
Interrupt status	Identify which input is the cause of an interrupt	• Eliminates complex external logic • Simplifies software logic



DEVELOPMENT TOOLS

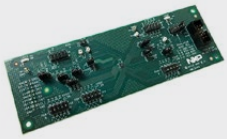
NXP offers a full range of tools to speed evaluation and product development. The 8 and 16-bit Universal boards allow evaluation of almost all of NXP's 8 and 16-bit I²C GPIO Expanders. Pinout differences between devices are handled via jumpers and customer must mounted desired GPIO on the board. The PCAL6524/34 boards are dedicated to those devices with devices premounted. Connectors allow direct connection to the µC or system controllers like TotalPhase Beagle.

ARD Arduino Shield demo boards allow easy integration with Arduino EVKs to evaluate the general-purpose I/O expander features for interfacing to sensors, push buttons, keypads and more. A downloadable graphical interface allows the user to easily explore the different functions of the GPIO expander to create an evaluation system.

ADDITIONAL INFORMATION

To order the daughter card, visit **www.digikey.com** or **www.mouser.com**.

For downloadable support tools, visit **www.nxp.com/GPIO**.

	ORDER NUMBER	DESCRIPTION
	OM13488	Universal 8-bit GPIO Daughter Card for the Fm+ Development Board
	OM13489	Universal 16-bit GPIO Daughter Card or the Fm+ Development Board
	OM13526	PCAL6524 Fm+ I²C 24-bit GPIO demo board
	OM13541	PCAL6534 Fm+ I2C 34-bit GPIO demo board
	PCAL6408A-ARD	PCAL6408A 8-Bit GPIO Arduino® Shield
	PCAL6416AEV-ARD	PCAL6416A 16-bit GPIO Arduino® Shield Evaluation Board
	PCAL6524EV-ARD	PCAL6524EV 24-Bit GPIO Arduino® Shield
	PCAL6534EV-ARD	PCAL6534EV 34-Bit GPIO Arduino® Shield

www.nxp.com and www.nxp.com/GPIO

Document Number: 939775017329 REV 3