Revision 1.0.0
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CUSTOMER ADVISORY

ADV1829

Stratix®10 GX and SX L-Tile Device Updates

Change Description:

Intel Programmable Solutions Group ("Intel PSG," formerly Altera) is notifying customers of the following changes to the Intel Stratix 10 GX and Intel Stratix 10 SX L-tile devices:

1. Timing Model
    a. Updated timing models for L-tile devices with improved accuracy in Intel Quartus® Prime Pro Edition software version 18.1.1.
2. Power Model
    a. Updated power models for L-tile devices with improved accuracy in Intel Quartus Prime Pro Edition software version 18.1.1 for VCCIO3v power rail with worst case power increase of ~80mW.
3. Software Bug Fix
    a. A bug fix in Intel Quartus Prime Pro Edition software version 18.1.1 code to prevent incorrect LUT logic implementation.

Recommended Actions:

1. Timing Model
    a. For designs in production:
        i. Run a script to identify paths impacted by the timing model change.
        ii. If the script identifies no impacted paths, no further action is required.

iii. If the script identifies impacted paths, and you are using Intel Quartus Prime Pro Edition software version 18.1 or earlier, download the patch and rerun timing analysis.
    1. If timing analysis shows insufficient margin, recompile the design.
    2. If timing analysis shows sufficient margin, no further action is required.

b. For designs still in development:
    i. Download the patch and recompile or migrate to Intel Quartus Prime Pro Edition software version 18.1.1.

For details on the script, patches, and steps to rerun timing analysis, refer to the following knowledge database link:

https://www.intel.com/content/altera-www/global/en_us/index/support/support-resources/knowledge-base/tools/2018/is-the-intel-stratix-10-timing-model-correct-in-the-intel-quartu.html

2. Power Model
    a. If the design can tolerate the 80mW power increase, no further action is required.
        a. To determine the exact power impact, customers can rerun Intel Quartus Prime Pro Edition software version 18.1.1 Early Power Estimator (EPE) for their design.
    b. If design cannot tolerate the power increase, changes to logic or design optimization are required.

Refer to the following knowledge database link for details:
https://www.intel.com/content/altera-www/global/en_us/index/support/support-resources/knowledge-base/tools/2018/is-the-intel-stratix-10-fpga-power-model-correct-in-the-intel-qu.html

3. Software Bug Fix
    a. For designs in production:
        i. Run a script to identify if your design has a LUT with the wrong bit settings.
        ii. If your design does not have an impacted LUT, no action is required.

iii. If the design has an impacted LUT, download the patch and recompile the design.

b. For designs still in development:
   i. Download the patch and recompile or migrate to Intel Quartus Prime Pro Edition software version 18.1.1.

Refer to the following knowledge database link for details on the script and patches:
https://www.intel.com/content/altera-www/global/en_us/index/support/support-resources/knowledge-base/tools/2019/why-do-i-see-functional-errors-in-my-intel-stratix-10-design-.html

For any additional questions or support, please contact your local Field Applications Engineer (FAE) or submit a Service Request at the My Intel support page.

Products Affected:

All Intel Stratix 10 GX and Intel Stratix 10 SX L-tile devices.

The list of affected OPNs can be downloaded in Excel form:
https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/pcn/adv1829-opn-list.xlsx

Reason for Change:

1. Timing Model
   a. Due to a problem in the timing model for Intel Stratix 10 devices associated with Intel Quartus Prime Pro Edition software version 18.1 and earlier, the delays from all the general-purpose inputs of the FPGA were miscalculated.
2. Power Model
   a. Due to a problem in the power model for Intel Stratix 10 devices associated with Intel Quartus Prime Pro Edition software version 18.1 and earlier, the power associated with VCCIO3v power rail was miscalculated.
3. Software Bug Fix

a. Due to a problem in Intel Quartus Prime Pro Edition software version 18.1 and earlier, Intel Stratix 10 designs were susceptible to incorrect optimization applied to LUT configurations of 7 or 8 inputs. The issue affects some but not all scenarios where such LUT configurations (7 or 8 inputs) are used.

Change Implementation

Table 1

Milestone	***Date of Availability***
Updated timing model in Intel Quartus Prime Pro Edition software version 18.1.1.	Now
Updated power model in Intel Quartus Prime Pro Edition software version 18.1.1.	Now
Updated Intel Quartus Prime Pro Edition software version 18.1.1 to prevent wrong translation from user netlist to bit settings.	Now

Contact

For more information, please contact your local Field Applications Engineer (FAE) or submit a Service Request at the My Intel support page.

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https://www.intel.com/content/www/us/en/programmable/my-intel/mal-emailsub/technical-updates.html

Revision History

Date	Rev	Description
02/15/2019	1.0.0	Initial Release