NuMicro™ Family
Nano102/112 Series
Datasheet

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1 GENERAL DESCRIPTION

The Nano112 series ultra-low-power 32-bit microcontroller embeded with ARM® Cortex™-M0 core operates at low voltage range from 1.8V to 3.6V and runs up to 32 MHz frequency with 16/32 Kbytes embedded Flash and 4/8 Kbytes embedded SRAM and 4 Kbytes Flash loader memory for In-System Programming (ISP). The Nano112 series integrates 4 COM x 36 SEG or 6 COM x 34 SEG LCD controller, RTC, 12-bit SAR ADC, comparators and provides high performance connectivity peripheral interfaces such as UART, SPI, I^2C, GPIOs, and ISO-7816-3 for Smart card. The Nano112 series supports Brown-out Detector, Power-down mode with RTC turn on, RAM retention is less than 1.5 uA, Deep power down mode with RAM retention is less than 650 nA and fast wake-up via many peripheral interfaces.

The Nano112 series provides low voltage, low operating power consumption, low standby current, high integration peripherals, high-efficiency operation, fast wake-up function and the lowest cost 32-bit microcontrollers. The Nano112 series is suitable for a wide range of battery device applications such as:

- Wearable Device
- Smart Watch
- Wireless Gaming Control
- Hand-Held Medical Device
- RFID Reader
- Mobile Payment Smart Card Reader
- Security Alarm System
- Smart Home Appliance
- Wireless Thermostats
- Wireless Sensors Node Device (WSND)
- Wireless Auto Meter Reading (AMR)
- Portable Wireless Data Collector
- Smart Water, Gas, Heat Meters

The Nano112 series includes two product lines: Nano102 Base line and Nano112 LCD line.

The Nano102 Base line, an ultra-low-power 32-bit microcontroller embedded with ARM® Cortex™-M0 core, operates at low voltage range from 1.8V to 3.6V and runs up to 32 MHz frequency with 16/32 Kbytes embedded flash and 4/8 Kbytes embedded SRAM and 4 Kbytes Flash loader memory for In-System Programming (ISP). It integrates RTC, 8- channels 12-bit SAR ADC, 2xComparators and provides high performance connectivity peripheral interfaces such as 2 x Low Power UARTs, 2 x SPIs, 2 x I^2Cs, GPIOs, and 2 x ISO-7816-3 for Smart card. The Nano102 Base line supports Brown-out Detector, Power-down mode with RAM retention and fast wake-up via many peripheral interfaces.

The Nano112 LCD line, an ultra-low-power 32-bit microcontroller embedded with ARM® Cortex™-M0 core, operates at low voltage range from 1.8V to 3.6V and runs up to 32 MHz frequency with 16/32 Kbytes embedded flash and 4/8 Kbytes embedded SRAM and 4 Kbytes Flash loader memory for In-System Programming (ISP). It integrates 4 COM x 36 SEG or 6 COM x 34 SEG LCD controller, RTC, 8-channels 12-bit SAR ADC, 2 x Comparators and provides high performance connectivity peripheral interfaces such as 2 x Low Power UARTs, 2 x SPIs, 2 x I^2Cs, GPIOs, and 2 x ISO-7816-3 for Smart card. The Nano112 LCD line supports Brown-out Detector, Power-down mode with RAM retention and fast wake-up via many peripheral interfaces.

Product Line	UART	SPI	I^2C	ADC	ACMP	RTC	SC	Timer	LCD
Nano102	●	●	●	●	●	●	●	●	
Nano112	●	●	●	●	●	●	●	●	●

Table 1-1 Connectivity Support Table

2 FEATURES

The equipped features are dependent on the product line and their sub products.

2.1 Nano102 Features – Base Line

- Low Supply Voltage Range: 1.8 V to 3.6 V
- Ultra-Low Power Consumption
  - Operation mode : 150 uA/MHz
  - Power-down mode : 1.5 uA (RTC on, RAM retention)
  - Deep power down mode : 650 nA (RAM retention)
- Fast Wake-Up From Standby Mode : Less than 6 μs
- Core
  - ARM® Cortex™-M0 core running up to 32 MHz
  - One 24-bit system timer
  - Supports Low Power Sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Flash EPROM Memory
  - Runs up to 32 MHz with zero wait state for discontinuous address read access
  - 16/32 Kbytes application program memory (APROM)
  - 4 KB in system programming (ISP) loader program memory (LDROM)
  - Programmable data flash start address and memory size with 512 bytes page erase unit
  - In System Program (ISP)/In Application Program (IAP) to update on-chip Flash EPROM
- SRAM Memory
  - 4/8 Kbytes embedded SRAM
  - Supports DMA mode
- DMA: Supports 5 channels: 4 PDMA channels and one CRC channel
  - PDMA
    - Peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer
    - Supports word boundary address
    - Supports word alignment transfer length in memory-to-memory mode
    - Supports word/half-word/byte alignment transfer length in peripheral-to-memory and memory-to-peripheral mode
    - Supports word/half-word/byte transfer data width from/to peripheral
    - Supports address direction: increment, fixed, and wrap around
  - CRC

- Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
  - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
  - CRC-8: $X^8 + X^2 + X + 1$
  - CRC-16: $X^{16} + X^{15} + X^2 + 1$
  - CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$

- Clock Control
  - Flexible selection for different applications
  - Built-in 12/16 MHz OSC, can be trimmed to 1 % deviation within all temperature range when turning on auto-trim function (system must have external 32.768 kHz crystal input) otherwise 12/16 MHz OSC has 2 % deviation within all temperarure range.
  - Low power 10 kHz OSC for watchdog and low power system operation
  - Supports one PLL, up to 32 MHz, for high performance system operation External 4~24 MHz crystal input for precise timing operation
  - External 32.768 kHz crystal input for RTC function and low power system operation
- GPIO
  - Three I/O modes:
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - All inputs with Schmitt trigger
  - I/O pin configured as interrupt source with edge/level setting
  - Supports High Driver and High Sink I/O mode
  - Supports input 5V tolerance, except PA.0 ~ PA.7, PA.12, PA.13, PF.0(X32I), PF.1(X32O).
- Timer
  - Supports 4 sets of 32-bit timers, each with 24-bit up-counting timer and one 8-bit pre-scale counter
  - Independent Clock Source for each timer
  - Provides one-shot,periodic, output toggle and continuous operation modes
  - Internal trigger event to ADC and PDMA
  - Supports PDMA mode
  - Wake system up from Power-down mode
- Watchdog Timer
  - Clock Source from LIRC (Internal 10 kHz Low Speed Oscillator Clock)
  - Selectable time-out period from 1.6 ms ~ 26 sec (depending on clock source)
  - Interrupt or reset selectable when watchdog time-out

- Wake system up from Power-down mode

- Window Watchdog Timer(WWDT)
  - 6-bit down counter and 6-bit compare value to make the window period flexible
  - Selectable WWDT clock pre-scale counter to make WWDT time-out interval variable.

- RTC
  - Supports software compensation by setting frequency compensate register (FCR)
  - Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
  - Supports Alarm registers (second, minute, hour, day, month, year)
  - Selectable 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Supports periodic time tick interrupt with 8 periodic options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
  - Wake system up from Power-down mode
  - Supports 80 bytes spare registers and a snoop pin to clear the content of these spare registers
  - Supports 1, 1/2, 1/4, 1/8, 1/16 Hz clock output

- PWM/Capture
  - Supports 1 PWM module with two 16-bit PWM generators
  - Provides four PWM outputs or two complementary paired PWM outputs
  - Each PWM generator equipped with one clock divider, one 8-bit prescaler, two clock selectors, and one Dead-zone generator for complementary paired PWM
  - (Shared with PWM timers) with four 16-bit digital capture timers provides four rising/ falling/both capture inputs.
  - Supports One-shot and Continuous mode
  - Supports Capture interrupt

- UART
  - Up to 1 Mbit/s baud rate and support 9600 baud rate @ 32kHz, low power mode
  - Up to two 16-byte FIFO UART controllers
  - UART ports with flow control (TX, RX, CTSn and RTSn)
  - Supports IrDA (SIR) function
  - Supports LIN function
  - Supports RS-485 9 bit mode and direction control.
  - Programmable baud rate generator
  - Supports PDMA mode
  - Wake system (CTSn, received data or RS-485 address matched) up from Power-down mode

- SPI

- Up to two sets of SPI controllers
- Master up to 32 MHz, and Slave up to 16 MHz
- Supports SPI/MICROWIRE Master/Slave mode
- Full duplex synchronous serial data transfer
- Variable length of transfer data from 4 to 32 bits
- MSB or LSB first data transfer
- RX and TX on both rising or falling edge of serial clock independently
- Two slave/device select lines when SPI controller is used as the master, and 1 slave/device select line when SPI controller is used as the slave
- Supports byte suspend mode in 32-bit transmission
- Supports two channel PDMA requests, one for transmit and another for receive
- Supports three wire mode, no slave select signal, bi-direction interface
- Wake system up(SPI clock toggle) from Power-down mode

- I^2C
  - Up to two sets of I^2C device
  - Master/Slave up to 1 Mbit/s
  - Bi-directional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
  - Built-in 14-bit time-out counter requesting the I^2C interrupt if the I^2C bus hangs up and timer-out counter overflows
  - Programmable clocks allowing for versatile rate control
  - Supports 7-bit addressing mode
  - Supports multiple address recognition (four slave addresses with mask option)
  - Wake system up(address match) from Power-down mode
- ADC
  - 12-bit SAR ADC up to 1Msps conversion rate
  - Up to 8-ch single-ended input from external pin (PA.0 ~ PA.7)
  - Four internal channels from internal reference voltage (Int_V_{REF}), Temperature sensor, AV_{DD}, and AV_{SS}.
  - Supports three reference voltage sources from V_{REF} pin, internal reference voltage (Int_V_{REF}), and AV_{DD}.
  - Supports Single Scan, Single Cycle Scan, and Continuous Scan mode
  - Each channel with individual result register
  - Only scan on enabled channels

- Threshold voltage detection (comparator function)
- Conversion started by software programming or external input
- Supports PDMA mode
- Supports up to four timer time-out events (TMR0, TMR1, TMR2 and TMR3) to enable ADC

- SmartCard (SC)
  - Compliant to ISO-7816-3 T=0, T=1
  - Supports up to two ISO-7816-3 ports
  - Separates receive/transmit 4 bytes entry FIFO for data payloads
  - Programmable transmission clock frequency
  - Programmable receiver buffer trigger level
  - Programmable guard time selection (11 ETU ~ 267 ETU)
  - A 24-bit and two 8-bit time-out counters for Answer to Request (ATR) and waiting times processing
  - Supports auto inverse convention function
  - Supports transmitter and receiver error retry and error limit function
  - Supports hardware activation sequence process
  - Supports hardware warm reset sequence process
  - Supports hardware deactivation sequence process
  - Supports hardware auto deactivation sequence when detect the card is removal
  - Supports UART mode (full–duplex)
- ACMP
  - Supports up to 2 analog comparators
  - Analog input voltage range: 0 ~ AV_{DD}
  - Supports Hysteresis function
  - Two analog comparators with optional internal reference voltage input at negative end
- Wake-up source
  - Support RTC, WDT, I²C, Timer, UART, SPI, BOD, GPIO
- One built-in temperature sensor with 1℃ resolution
- Brown-out
  - Built-in 2.5V/2.0V/1.7V BOD for wide operating voltage range operation
- 96-bit unique ID
- 128-bit unique customer ID
- Operating Temperature: -40℃~85℃
- Packages:
  - All Green package (RoHS)
  - LQFP 64-pin(7x7) / 48-pin(7x7)/ QFN33-pin(5x5)

2.2 Nano112 Features – LCD Line

- Low Supply Voltage Range: 1.8 V to 3.6 V
- Ultra-Low Power Consumption
  - Operation mode : 150 uA/MHz
  - Power-down mode : 1.5 uA (RTC on, RAM retention)
  - Deep power down mode : 650 nA (RAM retention)
- Fast Wake-Up From Standby Mode : Less than 6 μs
- Core
  - ARM® Cortex™-M0 core running up to 32 MHz
  - One 24-bit system timer
  - Supports Low Power Sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Flash EPROM Memory
  - Runs up to 32 MHz with zero wait state for discontinuous address read access.
  - 16/32 Kbytes application program memory (APROM)
  - 4 Kbytes In System Programming (ISP) loader program memory (LDROM)
  - Programmable data flash start address and memory size with 512 bytes page erase unit
  - In System Program (ISP)/In Application Program (IAP) to update on chip Flash EPROM
- SRAM Memory
  - 4/8 Kbytes embedded SRAM
  - Supports DMA mode
- DMA : Supports 5 channels: 4 PDMA channels, and one CRC channel
  - PDMA
    - Peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer
    - Supports word boundary address
    - Supports word alignment transfer length in memory-to-memory mode
    - Supports word/half-word/byte alignment transfer length in peripheral-to-memory and memory-to-peripheral mode
    - Supports word/half-word/byte transfer data width from/to peripheral
    - Supports address direction: increment, fixed, and wrap around
  - CRC
    - Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
      - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$

- CRC-8: $X^8 + X^2 + X + 1$
- CRC-16: $X^{16} + X^{15} + X^2 + 1$
- CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$

- Clock Control
  - Flexible selection for different applications
  - Built-in 12/16 MHz OSC, can be trimmed to 1 % deviation within all temperature range when turning on auto-trim function (system must have external 32.768 kHz crystal input) otherwise 12/16 MHz OSC has 2 % deviation within all temperarure range.
  - Low power 10 kHz OSC for watchdog and low power system operation
  - Supports one PLL, up to 32 MHz, for high performance system operation
  - External 4~24 MHz crystal input for precise timing operation
  - External 32.768 kHz crystal input for RTC function and low power system operation
- GPIO
  - Three I/O modes:
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - All inputs with Schmitt trigger
  - I/O pin configured as interrupt source with edge/level setting
  - Supports High Driver and High Sink I/O mode
  - Supports input 5V tolerance, except PA.0 ~ PA.7, PA.12, PA.13, P.0(X32I), PF.1(X32O)
- Timer
  - Supports 4 sets of 32-bit timers, each with 24-bit up-timer and one 8-bit pre-scale counter
  - Independent Clock Source for each timer
  - Provides one-shot,periodic, output toggle and continuous operation modes
  - Internal trigger event to ADC and PDMA
  - Supports PDMA mode
  - Wake system up from Power-down mode
- Watchdog Timer
  - Clock Source from LIRC (Internal 10 kHz Low Speed Oscillator Clock)
  - Selectable time-out period from 1.6 ms ~ 26 sec (depending on clock source)
  - Interrupt or reset selectable when watchdog time-out
  - Wake system up from Power-down mode
- Window Watchdog Timer(WWDT)
  - 6-bit down counter and 6-bit compare value to make the window period flexible

- Selectable WWDT clock pre-scale counter to make WWDT time-out interval variable.

- RTC
  - Supports software compensation by setting frequency compensate register (FCR)
  - Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
  - Supports Alarm registers (second, minute, hour, day, month, year)
  - Selectable 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Supports periodic time tick interrupt with 8 periodic options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
  - Wake system up from Power-down mode
  - Supports 80 bytes spare registers and a snoop pin to clear the content of these spare registers
  - Supports 1, 1/2, 1/4, 1/8, 1/16 Hz clock output
- PWM/Capture
  - Supports 1 PWM module with two 16-bit PWM generators
  - Provides four PWM outputs or two complementary paired PWM outputs
  - Each PWM generator equipped with one clock divider, one 8-bit prescaler, two clock selectors, and one Dead-zone generator for complementary paired PWM
  - (Shared with PWM timers) with four 16-bit digital capture timers provides four rising/ falling/both capture inputs.
  - Supports Capture interrupt
- UART
  - Up to 1 Mbit/s baud rate and support 9600 baud rate @ 32kHz, low power mode
  - Up to two 16-byte FIFO UART controllers
  - UART ports with flow control (TX, RX, CTSn and RTSn)
  - Supports IrDA (SIR) function
  - Supports LIN function
  - Supports RS-485 9 bit mode and direction control (Low Density Only)
  - Programmable baud rate generator
  - Supports PDMA mode
  - Wake system up (CTS, received data or RS-485 address matched) from Power-down mode
- SPI
  - Up to two sets of SPI controller
  - Master up to 32 MHz, and Slave up to 16 MHz
  - Supports SPI/MICROWIRE Master/Slave mode
  - Full duplex synchronous serial data transfer

- Variable length of transfer data from 4 to 32 bits
- MSB or LSB first data transfer
- RX and TX on both rising or falling edge of serial clock independently
- Two slave/device select lines when SPI controller is as the master, and 1 slave/device select line when SPI controller is as the slave
- Supports byte suspend mode in 32-bit transmission
- Supports two channel PDMA requests, one for transmit and another for receive
- Supports three wire mode, no slave select signal, bi-direction interface
- Wake system up (SPI clock toggle) from Power-down mode

- I^2C
  - Up to two sets of I^2C devices
  - Master/Slave up to 1Mbit/s
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
  - Built-in 14-bit time-out counter requestING the I^2C interrupt if the I^2C bus hangs up and timer-out counter overflows
  - Programmable clocks allow versatile rate control
  - Supports 7-bit addressing mode
  - Supports multiple address recognition (four slave address with mask option)
  - Wake system up (address match) from Power-down mode
- ADC
  - 12-bit SAR ADC up to 1Msps conversion rate
  - Up to 7-ch single-ended input from external pin (PA.0 ~ PA.6)
  - Four internal channels from internal reference voltage (Int_V_{REF}), Temperature sensor, AV_{DD}, and AV_{SS}
  - Supports three reference voltage sources from V_{REF} pin, internal reference voltage (Int_V_{REF}), and AV_{DD}.
  - Single scan/single cycle scan/continuous scan
  - Each channel with individual result register
  - Only scan on enabled channels
  - Threshold voltage detection (comparator function)
  - Conversion start by software programming or external input
  - Supports PDMA mode
  - Supports up to four timer time-out events (TMR0, TMR1, TMR2, and TMR3) to

enable ADC

- SmartCard (SC)
  - Compliant to ISO-7816-3 T=0, T=1
  - Supports up to two ISO-7816-3 ports
  - Separates receive / transmit 4 bytes entry FIFO for data payloads
  - Programmable transmission clock frequency
  - Programmable receiver buffer trigger level
  - Programmable guard time selection (11 ETU ~ 267 ETU)
  - A 24-bit and two 8-bit time-out counter for Answer to Request (ATR) and waiting times processing
  - Supports auto inverse convention function
  - Supports transmitter and receiver error retry and error limit function
  - Supports hardware activation sequence process
  - Supports hardware warm reset sequence process
  - Supports hardware deactivation sequence process
  - Supports hardware auto deactivation sequence when detect the card is removal
  - Supports UART mode (full-duplex)
- ACMP
  - Suuports up to 2 analog comparators
  - Analog input voltage range: 0 ~ AV_{DD}
  - Supports Hysteresis function
  - Two analog comparators with optional internal reference voltage input at negative end
- Wake-up source
  - Support RTC, WDT, I²C, Timer, UART, SPI, BOD, GPIO
- LCD
  - LCD driver for up to 4 COM x 36 SEG or 6 COM x 34 SEG
  - Supports Static,1/2 bias and 1/3 bias voltage
  - Six display modes; Static, 1/2 duty, 1/3 duty, 1/4 duty, 1/5 duty and 1/6 duty.
  - Selectable LCD frequency by frequency divider
  - Configurable frame frequency
  - Internal Charge pump, adjustable contrast adjustment
  - Configurable Charge pump frequency
  - Blinking capability
  - Supports R-type/C-type/External C-type method
  - Configurable internal R-ladder resistor value (200K/300K/400K)
  - LCD frame interrupt
- One built-in temperature sensor with 1℃ resolution

- Brown-out
  - Built-in 2.5V/2.0V/1.7V BOD for wide operating voltage range operation
- 96-bit unique ID
- 128-bit unique customer ID
- Operating Temperature: -40℃~85℃
- Packages:
  - All Green package (RoHS)
  - LQFP 100-pin(14x14) / 64-pin(10x10) / 64-pin(7x7) / 48-pin(7x7)

3 ABBREVIATIONS

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
CAN	Controller Area Network
DAP	Debug Access Port
DES	Data Encryption Standard
EBI	External Bus Interface
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	12/16 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NTC	Negative Temperature Coefficient
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PTC	Positive Temperature Coefficient
PT1000	Thermal Resistance
PWM	Pulse Width Modulation

QEI	Quadrature Encoder Interface
SDIO	Secure Digital Input/Output
SPI	Serial Peripheral Interface
SPS	Samples per Second
TDES	Triple Data Encryption Standard
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 3-1 List of Abbreviations

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 NuMicro™ Nano102/112 Series Selection Code

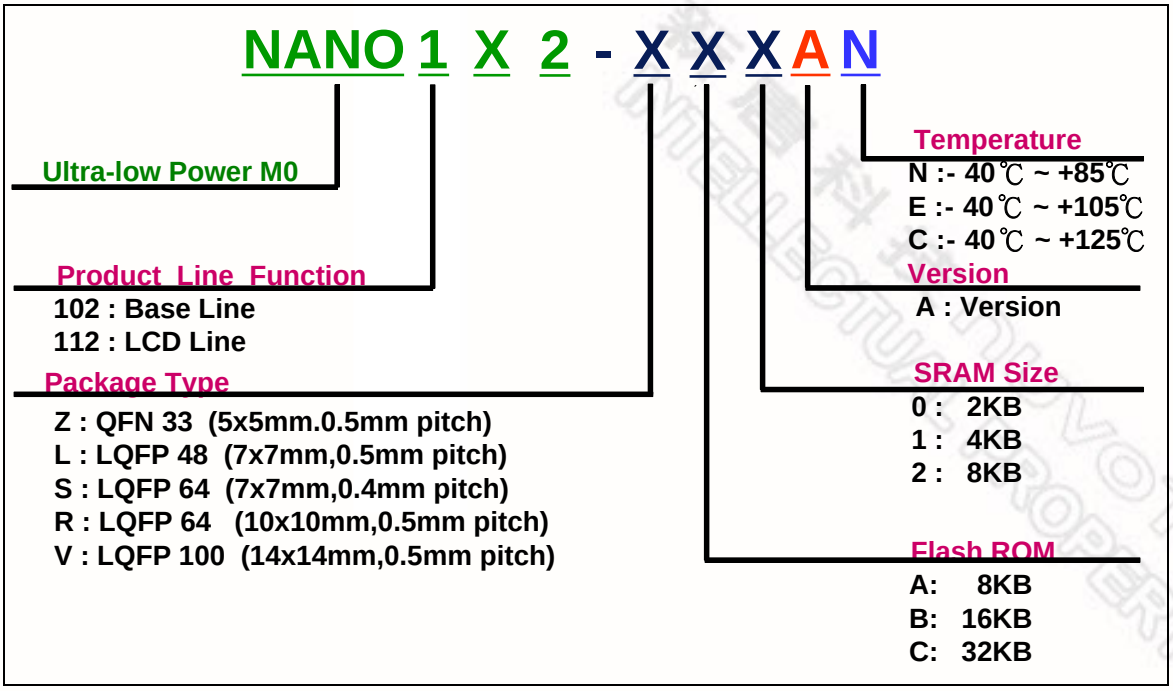


Figure 4-1 NuMicro™ Nano112 Series Selection Code

4.2 NuMicro™ Nano112 Products Selection Guide

4.2.1 NuMicro™ Nano102 Base Line Selection Guide

Part No.	Flash	SRAM	Data Flash	ISP ROM	I/O	Timer (32-bit)	Connectivity			Comp	PWM (16-bit)	ADC (12-bit)	RTC	IRC 10 kHz / 12 MHz / 16 MHz	PDMA	LCD	ISO-7816-3	ISP ICP	Package	Maximum Operating Temp. Range (°C)
							UART	SPI	I²C											
NANO102ZB1AN	16K	4K	Configurable	4K	up to 27	4	3	2	2	2	4	2	√	√	4	-	1	√	QFN33	-40 to +85
NANO102ZC2AN	32K	8K	Configurable	4K	up to 27	4	3	2	2	2	4	2	√	√	4	-	1	√	QFN33	-40 to +85
NANO102LB1AN	16K	4K	Configurable	4K	up to 40	4	4	2	2	2	4	7	√	√	4	-	2	√	LQFP48	-40 to +85
NANO102LC2AN	32K	8K	Configurable	4K	up to 40	4	4	2	2	2	4	7	√	√	4	-	2	√	LQFP48	-40 to +85
NANO102SC2AN	32K	8K	Configurable	4K	up to 58	4	4	2	2	2	4	7	√	√	4	-	2	√	LQFP64*	-40 to +85

QFN33: 5x5mm
LQFP48: 7x7mm
LQFP64*: 7x7mm

4.2.2 NuMicro™ Nano112 LCD Line Selection Guide

Part No.	Flash	SRAM	Data Flash	ISP ROM	I/O	Timer (32-bit)	Connectivity			Comp	PWM (16-bit)	ADC (12-bit)	RTC	IRC 10KHz / 12MHz / 16MHz	PDMA	LCD	ISO-7816-3	ISP ICP	Package	Maximum Operating Temp. Range (°C)
							UART	SPI	I²C											
NANO112LB1AN	16K	4K	Configurable	4K	up to 40	4	4	2	2	2	4	7	√	√	4	4x20, 6x18	2	√	LQFP48	-40 to +85
NANO112LC2AN	32K	8K	Configurable	4K	up to 40	4	4	2	2	2	4	7	√	√	4	4x20, 6x18	2	√	LQFP48	-40 to +85
NANO112SB1AN	16K	4K	Configurable	4K	up to 58	4	4	2	2	2	4	7	√	√	4	4x32, 6x30	2	√	LQFP64	-40 to +85
NANO112SC2AN	32K	8K	Configurable	4K	up to 58	4	4	2	2	2	4	7	√	√	4	4x32, 6x30	2	√	LQFP64	-40 to +85
NANO112RB1AN	16K	4K	Configurable	4K	up to 58	4	4	2	2	2	4	7	√	√	4	4x32, 6x30	2	√	LQFP64*	-40 to +85
NANO112RC2AN	32K	8K	Configurable	4K	up to 58	4	4	2	2	2	4	7	√	√	4	4x32, 6x30	2	√	LQFP64*	-40 to +85
NANO112VC2AN	32K	8K	Configurable	4K	up to 80	4	4	2	2	2	4	8	√	√	4	4x36, 6x34	2	√	LQFP100	-40 to +85

LQFP48: 7x7mm
LQFP64: 7x7mm
LQFP64*: 10x10mm

4.3 Pin Configuration

4.3.1 NuMicro™ Nano102 Pin Diagrams

4.3.1.1 NuMicro™ Nano102 LQFP 64-pin

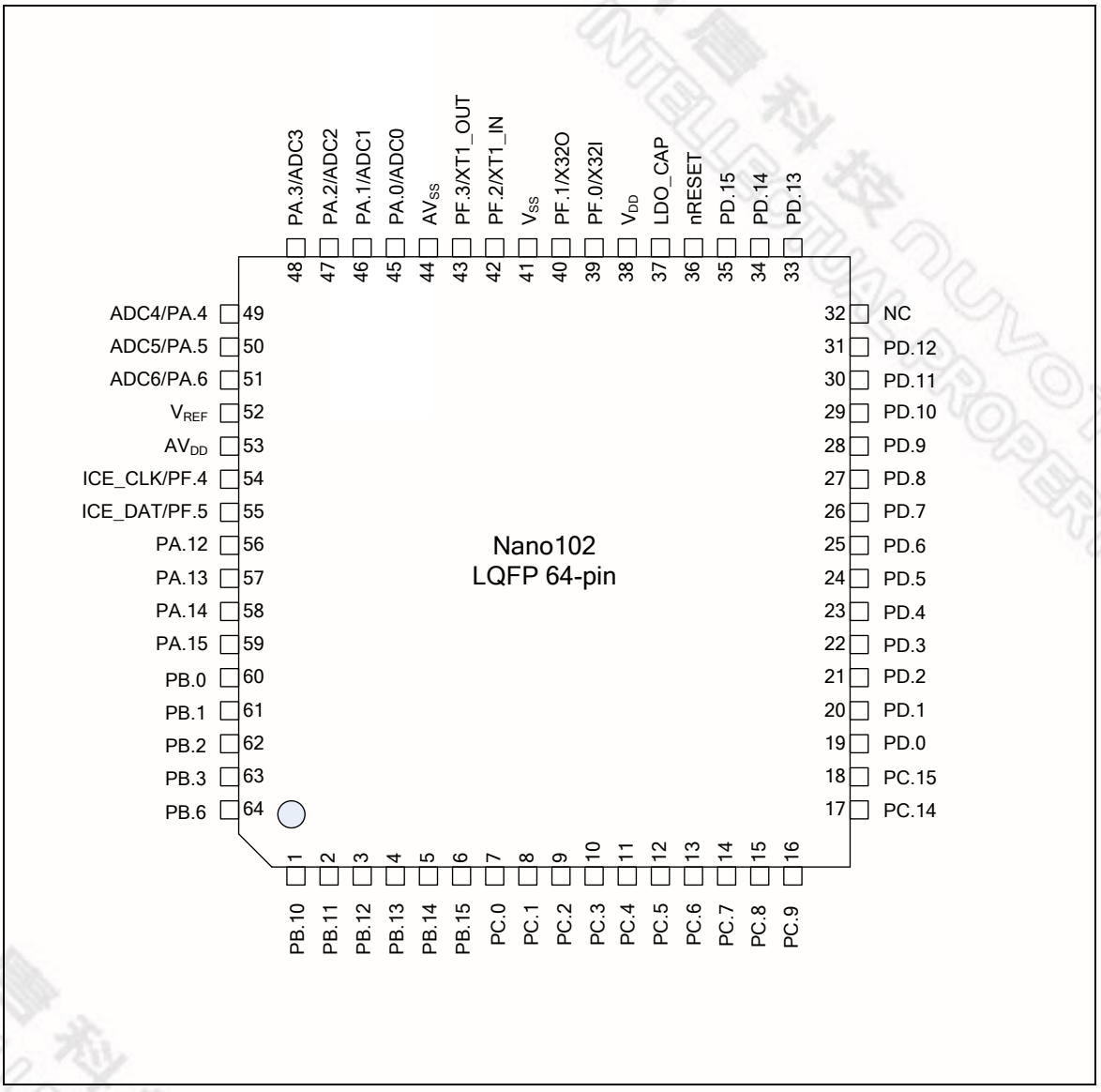


Figure 4- 2 NuMicro™ Nano102 LQFP 64-pin Diagram

4.3.1.2 NuMicro™ Nano102 LQFP 48-pin

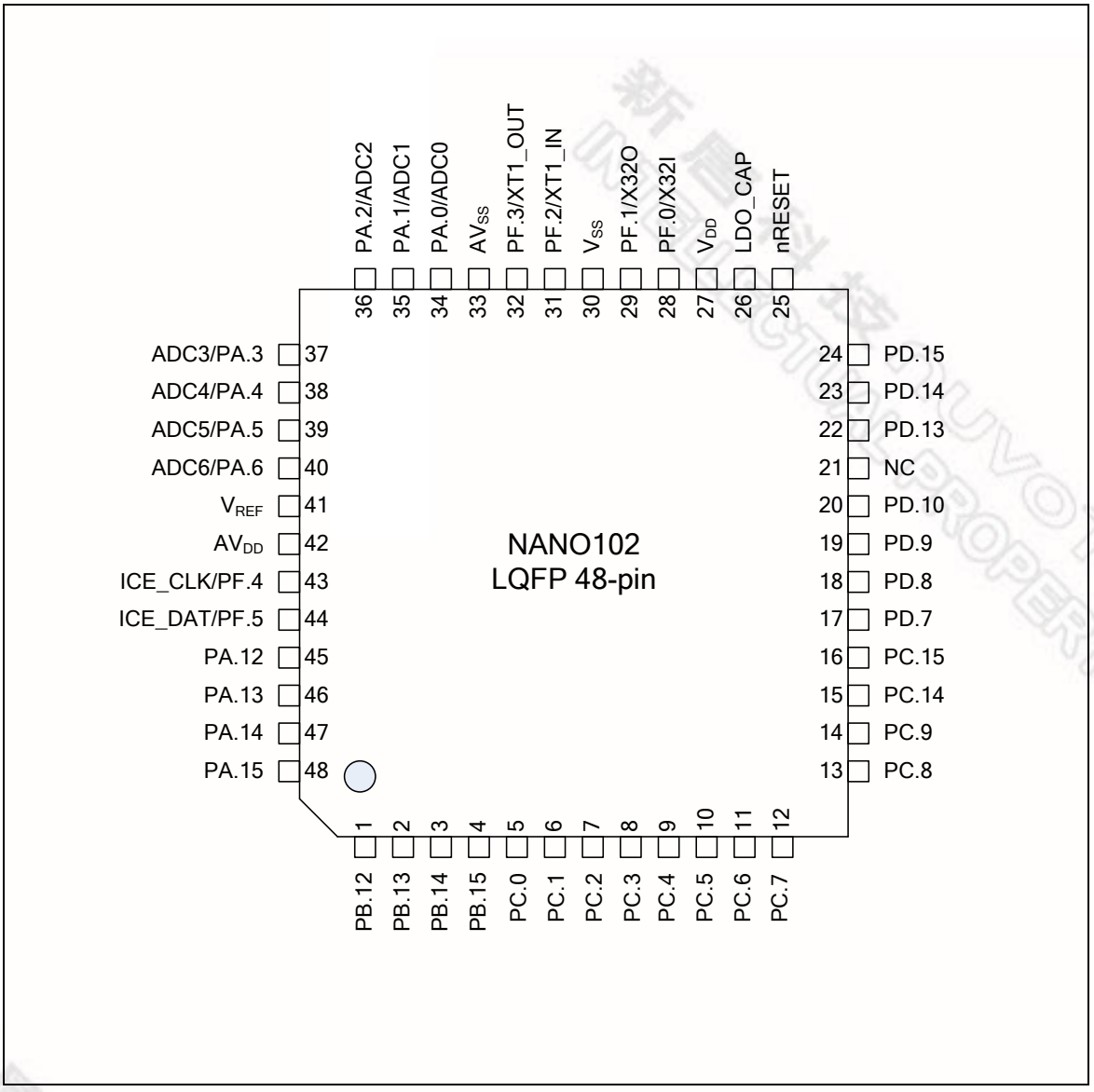


Figure 4-3 NuMicro™ Nano102 LQFP 48-pin Diagram

4.3.1.3 NuMicro™ Nano102 QFN 33-pin

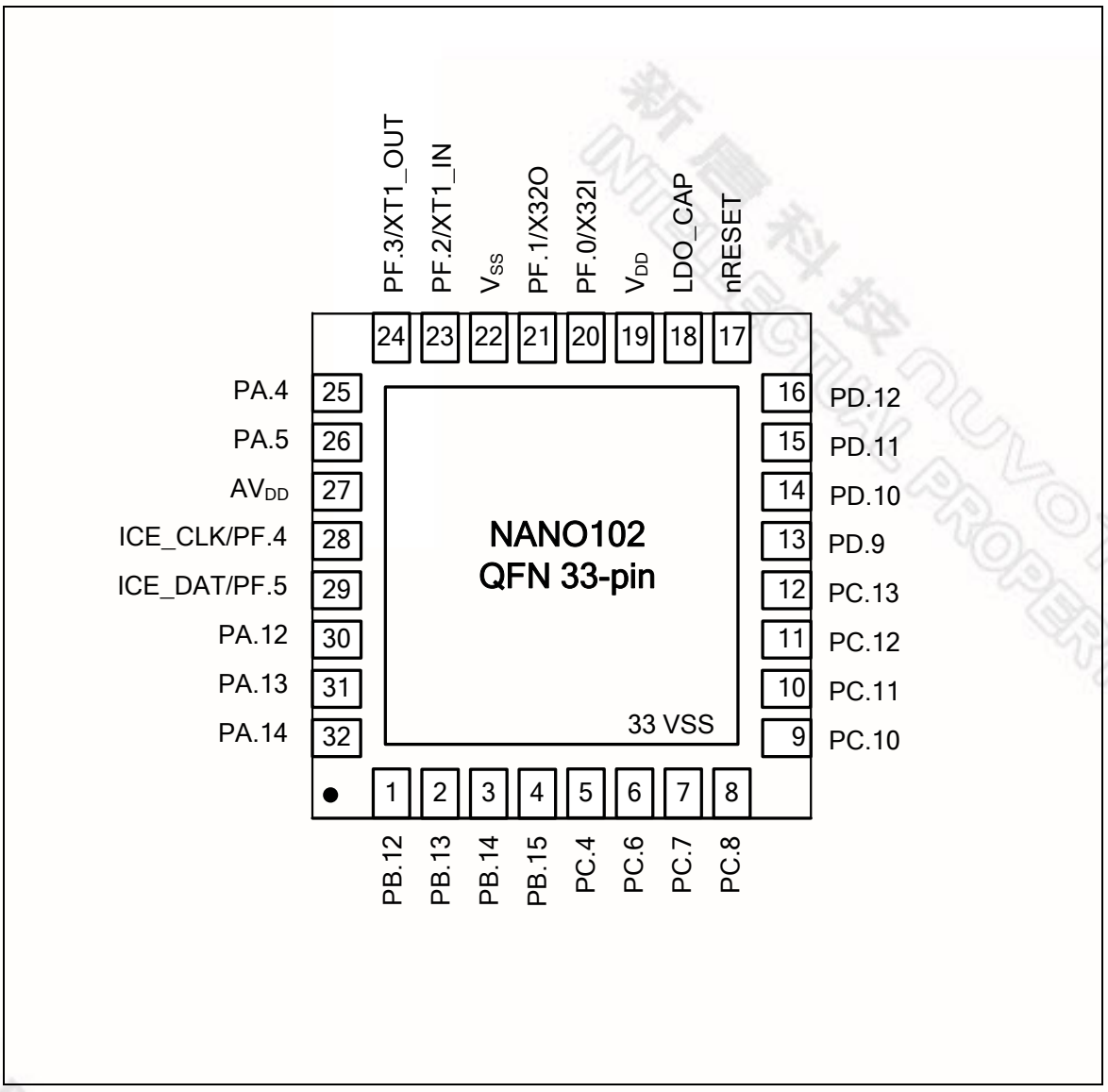


Figure 4-4 NuMicro™ Nano102 QFN 32-pin Diagram

4.3.2 NuMicro™ Nano112 Pin Diagrams

4.3.2.1 NuMicro™ Nano112 LQFP 100-pin

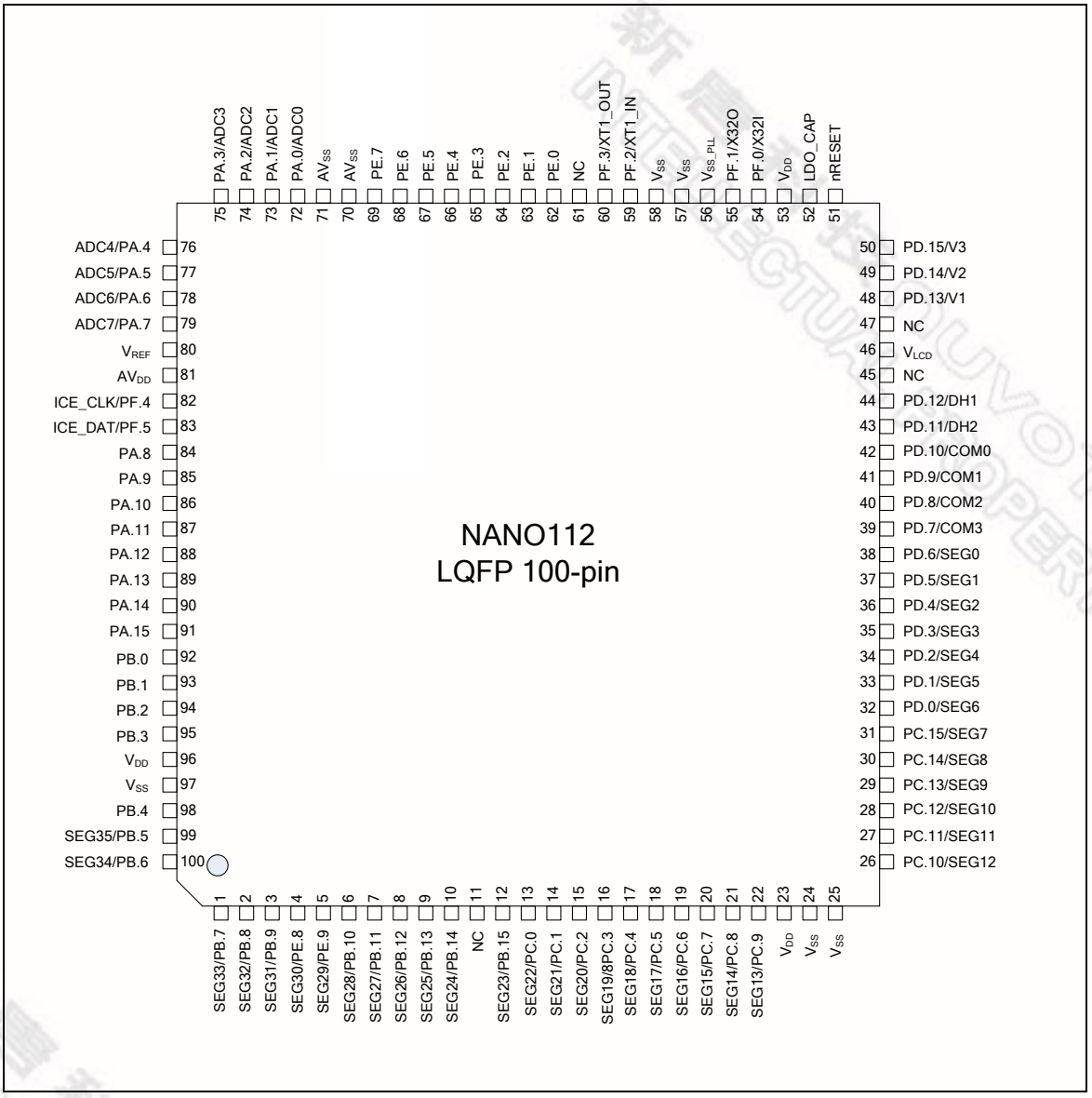


Figure 4-5 NuMicro™ Nano112 LQFP 100-pin Diagram

4.3.2.2 NuMicro™ Nano112 LQFP 64-pin

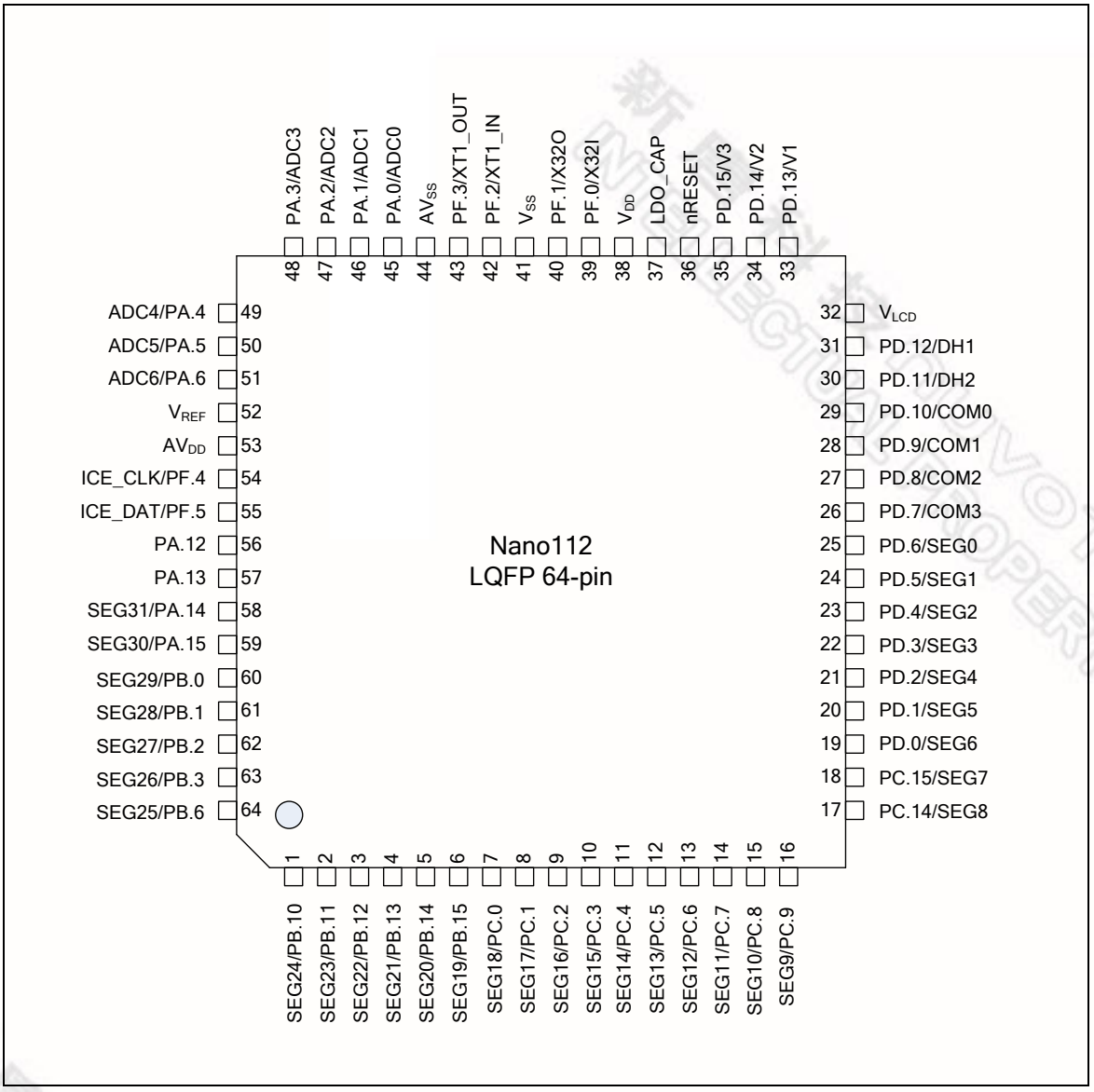


Figure 4-6 NuMicro™ Nano112 LQFP 64-pin Diagram

4.3.2.3 NuMicro™ Nano112 LQFP 48-pin

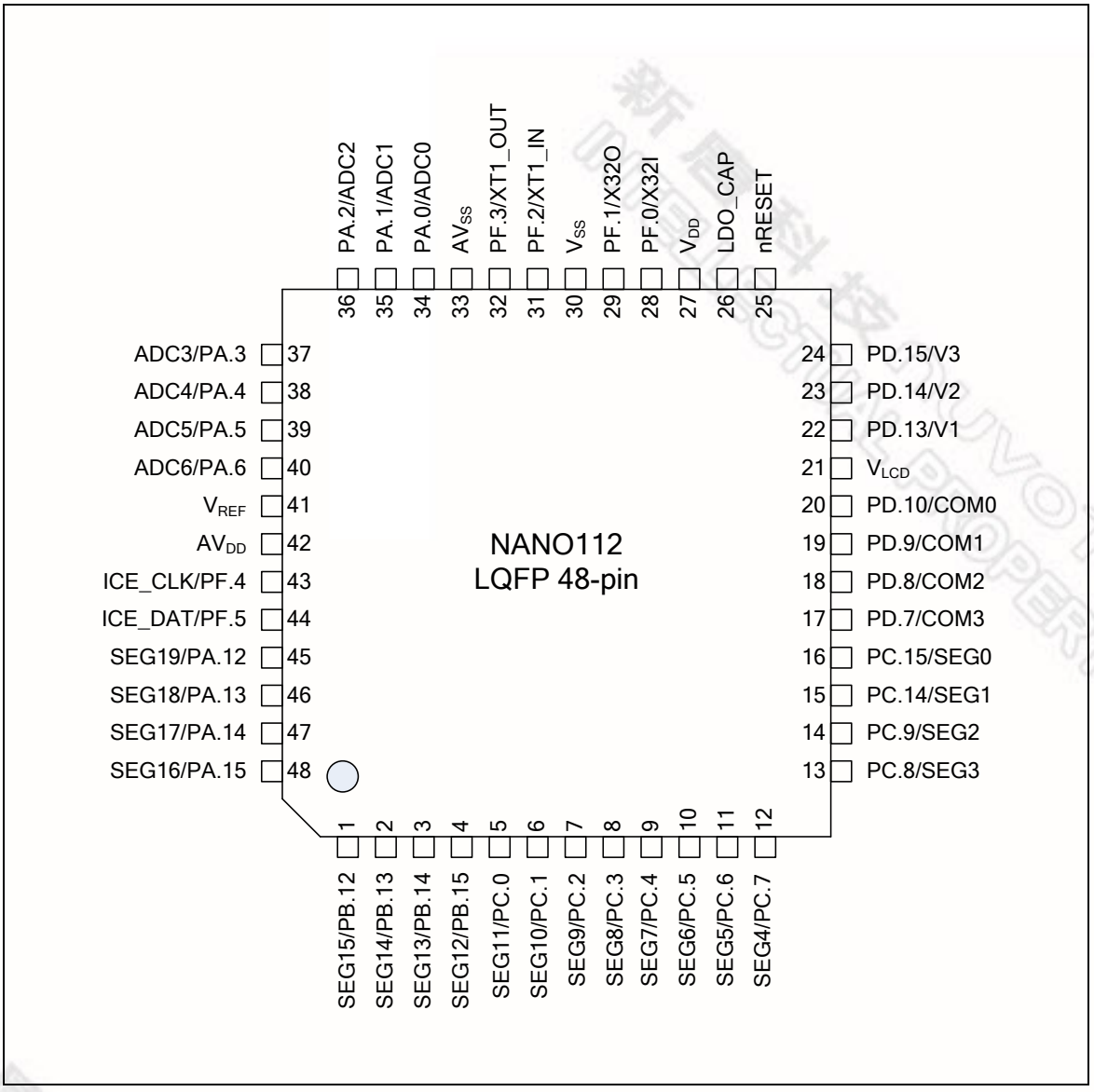


Figure 4-7 NuMicro™ Nano112 LQFP 48-pin Diagram

4.4 Pin Description

4.4.1 NuMicro™ Nano102 Pin Description

Pin No.			Pin Name	Pin Type	Description
64-pin	48-pin	32-pin			
1			PB.10	I/O	General purpose digital I/O pin
			UART1_RXD	I	UART1 Data receiver input pin
			SPI0_MOSI1	I/O	SPI0 2nd MOSI (Master Out, Slave In) pin
2			PB.11	I/O	General purpose digital I/O pin
			UART1_RTSn	O	UART1 Request to Send output pin
			SPI0_MISO1	I/O	SPI0 2rd MISO (Master In, Slave Out) pin
			TM1	I/O	Timer1 external counter input or Timer1 toggle out
3	1	1	PB.12	I/O	General purpose digital I/O pin
			UART0_RTSn	O	UART0 Request to Send output pin
			SPI0_MOSI0	I/O	SPI0 1st MOSI (Master Out, Slave In) pin
			TM0	I/O	Timer0 external counter input or Timer0 toggle out.
			FCLK0	O	Frequency Divider0 output pin
4	2	2	PB.13	I/O	General purpose digital I/O pin
			UART0_RXD	I	UART0 Data receiver input pin
			SPI0_MISO0	I/O	SPI0 1st MISO (Master In, Slave Out) pin
5	3	3	PB.14	I/O	General purpose digital I/O pin
			UART0_TXD	O	UART0 Data transmitter output pin (This pin could be modulated with PWM0 output.)
			SPI0_CLK	I/O	SPI0 serial clock pin
6	4	4	PB.15	I/O	General purpose digital I/O pin
			UART0_CTSn	I	UART0 Clear to Send input pin
			SPI0_SS0	I/O	SPI0 1st slave select pin
7	5		PC.0	I/O	General purpose digital I/O pin
			SPI0_SS1	I/O	SPI0 2nd slave select pin
			I2C0_SCL	I/O	I2C0 clock pin
			PWM0_CH0	I/O	PWM0 Channel0 output
8	6		PC.1	I/O	General purpose digital I/O pin
			I2C0_SDA	I/O	I2C0 data I/O pin

Pin No.			Pin Name	Pin Type	Description
64-pin	48-pin	32-pin			
			PWM0_CH1	I/O	PWM0 Channel1 output
9	7		PC.2	I/O	General purpose digital I/O pin
			I2C1_SCL	O	I^2C1 clock pin
			PWM0_CH2	I/O	PWM0 Channel2 output
10	8		PC.3	I/O	General purpose digital I/O pin
			I2C1_SDA	I/O	I^2C1 data I/O pin
			PWM0_CH3	I/O	PWM0 Channel3 output
11	9	5	PC.4	I/O	General purpose digital I/O pin
			UART1_CTSn	I	UART1 Clear to Send input pin
			SC0_CLK	O	SmartCard0 clock pin (SC0_UART_TXD)
			INT0	I	External interrupt0 input pin
12	10		PC.5	I/O	General purpose digital I/O pin
			SC0_CD	I	SmartCard0 card detect pin
13	11	6	PC.6	I/O	General purpose digital I/O pin
			UART1_RTSn	O	UART1 Request to Send output pin
			SC0_DAT	I/O	SmartCard0 DATA pin (SC0_UART_RXD)
14	12	7	PC.7	I/O	General purpose digital I/O pin
			UART1_RXD	I	UART1 Data receiver input pin
			SC0_PWR	O	SmartCard0 Power pin
15	13	8	PC.8	I/O	General purpose digital I/O pin
			UART1_TXD	O	UART1 Data transmitter output pin (This pin could be modulated with PWM0 output.)
			SC0_RST	O	SmartCard0 RST pin
16	14		PC.9	I/O	General purpose digital I/O pin
		9	PC.10	I/O	General purpose digital I/O pin
			I2C1_SCL	I/O	I^2C1 clock pin
			SC1_CD	I	SmartCard1 card detect
		10	PC.11	I/O	General purpose digital I/O pin
			I2C1_SDA	I/O	I^2C 1 data I/O pin
			SC1_PWR	O	SmartCard1 PWR pin
		11	PC.12	I/O	General purpose digital I/O pin
			SC1_CLK	O	SmartCard1 clock pin (SC1_UART_TXD)

Pin No.			Pin Name	Pin Type	Description
64-pin	48-pin	32-pin			
		12	PC.13	I/O	General purpose digital I/O pin
			SC1_DAT	I/O	SmartCard1 DATA pin (SC1_UART_RXD)
17	15		PC.14	I/O	General purpose digital I/O pin
			SC1_CD	I	SmartCard1 card detect
18	16		PC.15	I/O	General purpose digital I/O pin
			SC1_PWR	O	SmartCard1 PWR pin
19			PD.0	I/O	General purpose digital I/O pin
20			PD.1	I/O	General purpose digital I/O pin
21			PD.2	I/O	General purpose digital I/O pin
22			PD.3	I/O	General purpose digital I/O pin
23			PD.4	I/O	General purpose digital I/O pin
			SC1_RST	O	SmartCard1 RST pin
24			PD.5	I/O	General purpose digital I/O pin
25			PD.6	I/O	General purpose digital I/O pin
26	17		PD.7	I/O	General purpose digital I/O pin
			SC1_CLK	O	SmartCard1 clock pin (SC1_UART_TXD)
27	18		PD.8	I/O	General purpose digital I/O pin
			SC1_DAT	I/O	SmartCard1 DATA pin (SC1_UART_RXD)
28	19	13	PD.9	I/O	General purpose digital I/O pin
			SC1_RST	O	SmartCard1 RST pin
			PWM0_CH3	I/O	PWM0 Channel3 output
29	20	14	PD.10	I/O	General purpose digital I/O pin
			PWM0_CH2	I/O	PWM0 Channel2 output
			TC1	I	Timer1 capture input
30		15	PD.11	I/O	General purpose digital I/O pin
			PWM0_CH1	I/O	PWM0 Channel1 output
			TC0	I	Timer0 capture input
31		16	PD.12	I/O	General purpose digital I/O pin
			CLK_Hz	O	1, 1/2, 1/4, 1/8, 1/16 Hz clock output
			PWM0_CH0	I/O	PWM0 Channel0 output
			TM1	I/O	Timer1 external counter input or Timer1 toggle out

Pin No.			Pin Name	Pin Type	Description
64-pin	48-pin	32-pin			
			FCLK0	**O**	Frequency Divider0 output pin
32	21				NC
33	22		PD.13	**I/O**	General purpose digital I/O pin
			INT1	**I**	External interrupt 1 input pin
34	23		PD.14	**I/O**	General purpose digital I/O pin
35	24		PD.15	**I/O**	General purpose digital I/O pin
36	25	17	nRESET	**I**	External reset input: low active. Setting this pin low will reset chip to initial state. With internal pull-up.
37	26	18	LDO_CAP	**P**	LDO capacitor pin
38	27	19	V_{DD}	**P**	Power supply for I/O ports and LDO source
39	28	20	PF.0	**I/O**	General purpose digital I/O pin
			X32I	**I**	External 32.768 kHz crystal input pin (default)
			TM3	**I/O**	Timer3 external counter input or Timer3 toggle out.
40	29	21	PF.1	**I/O**	General purpose digital I/O pin
			X32O	**O**	External 32.768 kHz crystal output pin (default)
			TM2	**I/O**	Timer2 external counter input or Timer2 toggle out.
41	30	22	V_{SS}	**G**	Ground for digital circuit
42	31	23	PF.2	**I/O**	General purpose digital I/O pin
			XT1_IN	**AI**	External 4~24 MHz crystal input pin (default)
			UART1_RXD	**I**	UART1 Data receiver input pin
			TC3	**I**	Timer3 capture input
			INT1	**I**	External interrupt1 input pin
43	32	24	PF.3	**I/O**	General purpose digital I/O pin
			XT1_OUT	**AO**	External 4~24 MHz crystal output pin
			UART1_TXD	**O**	UART1 Data transmitter output pin (This pin could be modulated with PWM0 output.)
			TC2	**I**	Timer2 capture input
			INT0	**I**	External interrupt0 input pin
44	33		AV_{SS}	**G**	Ground for ADC and comparators
45	34		PA.0	**I/O**	General purpose digital I/O pin

Pin No.			Pin Name	Pin Type	Description
64-pin	48-pin	32-pin			
			AD0	AI	ADC analog input0
46	35		PA.1	I/O	General purpose digital I/O pin
			AD1	AI	ADC analog input1
			ACMP0_P3	AI	Comparator0 P-end input3
			ACMP0_CHDIS	O	Comparator0 charge/discharge path
47	36		PA.2	I/O	General purpose digital I/O pin
			SC0_CLK	O	SmartCard0 clock pin (SC0_UART_TXD)
			INT0	I	External interrupt0 input pin
			AD2	AI	ADC analog input2
			ACMP0_P2	AI	Comparator0 P-end input2
			ACMP0_CHDIS	O	Comparator0 charge/discharge path
48	37		PA.3	I/O	General purpose digital I/O pin
			SC0_DAT	I/O	SmartCard0 DATA pin(SC0_UART_RXD)
			INT1	I	External interrupt 1
			AD3	AI	ADC analog input3
			ACMP0_P1	AI	Comparator0 P-end input1
			ACMP0_CHDIS	O	Comparator0 charge/discharge path
49	38	25	PA.4	I/O	General purpose digital I/O pin
			SC0_CD	I	SmartCard0 card detect pin
			AD4	AI	ADC analog input4
			ACMP0_P0	AI	Comparator0 P-end input0
			ACMP0_CHDIS	O	Comparator0 charge/discharge path
50	39	26	PA.5	I/O	General purpose digital I/O pin
			SPI1_SS0	I/O	SPI1 1st slave select pin
			I2C1_SDA	I/O	I^2C1 data I/O pin
			SC0_PWR	O	SmartCard0 Power pin
			AD5	AI	ADC analog input5
			ACMP0_N	AI	Comparator0 N-end input0
			ACMP0_CHDIS	O	Comparator0 charge/discharge path
51	40		PA.6	I/O	General purpose digital I/O pin
			ACMP0_CHDIS	O	Comparator0 charge/discharge path
			SC0_RST	O	SmartCard0 RST pin

Pin No.			Pin Name	Pin Type	Description
64-pin	48-pin	32-pin			
			ACMP0_OUT	O	Comparator0 output
			AD6	AI	ADC analog input6
52	41		V_{REF}	A	ADC/Comparator reference voltage
53	42	27	AV_{DD}	P	Power supply for ADC and comparators
54	43	28	PF.4	I/O	General purpose digital I/O pin
			ICE_CLK	I	Serial Wired Debugger Clock pin
			CLK_Hz	O	1, 1/2, 1/4, 1/8, 1/16 Hz clock output
			PWM0_CH2	O	PWM0 Channel2 output
			TC1	I	Timer1 capture input
			FCLK1	O	Frequency Divider1 output pin
55	44	29	PF.5	I/O	General purpose digital I/O pin
			ICE_DAT	I/O	Serial Wired Debugger Data pin
			PWM0_CH3	I/O	PWM0 Channel3 output
			TC0	I	Timer0 capture input
			ACMP0_CHDIS	O	Comparator0 charge/discharge path
56	45	30	PA.12	I/O	General purpose digital I/O pin
			UART0_TXD	O	UART0 Data transmitter output pin (This pin could be modulated with PWM0 output.)
			SPI1_MOSI0	I/O	SPI1 1st MOSI (Master Out, Slave In) pin
			I2C0_SCL	I/O	I^2C 0 clock pin
			ACMP1_P	AI	Comparator1 P-end input
57	46	31	PA.13	I/O	General purpose digital I/O pin
			UART0_RXD	I	UART0 Data receiver input pin
			SPI1_MISO0	I/O	SPI1 1st MISO (Master In, Slave Out) pin
			I2C0_SDA	I/O	I^2C0 data I/O pin
			ACMP1_N	AI	Comparator1 N-end input
58	47	32	PA.14	I/O	General purpose digital I/O pin
			SPI1_CLK	I/O	SPI1 serial clock pin
			I2C1_SCL	I/O	I^2C1 clock pin
			ACMP0_CHDIS	O	Comparator0 charge/discharge path
59	48		PA.15	I/O	General purpose digital I/O pin
			SPI1_SS0	I/O	SPI1 1st slave select pin

Pin No.			Pin Name	Pin Type	Description
64-pin	48-pin	32-pin			
			I2C1_SDA	I/O	I^2C1 data I/O pin
			TC3	I	Timer3 capture input
			ACMP1_OUT	O	Comparator1 output
60			PB.0	I/O	General purpose digital I/O pin
			UART0_TXD	O	UART0 Data transmitter output pin(This pin could modulate with PWM0 output)
			FCLK1	O	Frequency Divider1 output pin
61			PB.1	I/O	General purpose digital I/O pin
			UART0_RXD	I	UART0 Data receiver input pin
			TC2	I	Timer 2 capture input
			INT1	I	External interrupt1 input pin
62			PB.2	I/O	General purpose digital I/O pin
			UART0_RTSn	O	UART0 Request to Send output pin
			SPI1_MOSI1	I/O	SPI1 2nd MOSI (Master Out, Slave In) pin
			I2C0_SCL	I/O	I^2C0 clock pin
			TM3	I/O	Timer3 external counter input or Timer3 toggle out.
63			PB.3	I/O	General purpose digital I/O pin
			UART0_CTSn	I	UART0 Clear to Send input pin
			SPI1_MISO1	I/O	SPI1 2nd MISO (Master In, Slave Out) pin
			I2C0_SDA	I/O	I^2C0 data I/O pin
			TM2	I/O	Timer2 external counter input or Timer2 toggle out.
64			PB.6	I/O	General purpose digital I/O pin
			UART1_TXD	O	UART1 Data transmitter output pin (This pin could be modulated with PWM0 output.)
			SPI1_SS1	I/O	SPI1 2nd slave select pin
			FCLK0	O	Frequency Divider0 output pin

Note: Pin Type: I = Digital Input, O = Digital Output; AI = Analog Input; AO = Analog Output; P = Power Pin; AP = Analog Power.

4.4.2 NuMicro™ Nano112 Pin Description

Pin No.			Pin Name	Pin Type	Description
100-pin	64-pin	48-pin			
1			PB.7	I/O	General purpose digital I/O pin
			LCD_SEG33	O	LCD segment output 33 at 100-pin
			UART1_CTSn	I	UART1 Clear to Send input pin
			SC0_CD	I	SmartCard0 card detect
2			PB.8	I/O	General purpose digital I/O pin
			LCD_SEG32	O	LCD segment output 32 at 100-pin
			SNOOPER	I	Snooper pin
			PWM0_CH0	I/O	PWM0 Channel0 output
			TM0	I/O	Timer0 external counter input or Timer0 toggle out.
			INT1	I	External interrupt1 input pin
3			PB.9	I/O	General purpose digital I/O pin
			LCD_SEG31	O	LCD segment output 31 at 100-pin
			PWM0_CH1	I/O	PWM0 Channel1 output
4			PE.8	I/O	General purpose digital I/O pin
			LCD_SEG30	O	LCD segment output 30 at 100-pin
			PWM0_CH2	I/O	PWM0 Channel2 output
5			PE.9	I/O	General purpose digital I/O pin
			LCD_SEG29	O	LCD segment output 29 at 100-pin
			PWM0_CH3	I/O	PWM0 Channel3 output
6	1		PB.10	I/O	General purpose digital I/O pin
			LCD_SEG28	O	LCD segment output 28 at 100-pin
			LCD_SEG24	O	LCD segment output 24 at 64-pin
			UART1_RXD	I	UART1 Data receiver input pin
			SPI0_MOSI1	I/O	SPI0 2nd MOSI (Master Out, Slave In) pin
7	2		PB.11	I/O	General purpose digital I/O pin
			LCD_SEG27	O	LCD segment output 27 at 100-pin
			LCD_SEG23	O	LCD segment output 23 at 64-pin
			UART1_RTSn	O	UART1 Request to Send output pin
			SPI0_MISO1	I/O	SPI0 2rd MISO (Master In, Slave Out) pin
			TM1	I/O	Timer1 external counter input or Timer1 toggle out
8	3	1	PB.12	I/O	General purpose digital I/O pin

Pin No.			Pin Name	Pin Type	Description
100-pin	64-pin	48-pin			
			LCD_SEG26	O	LCD segment output 26 at 100-pin
			LCD_SEG22	O	LCD segment output 22 at 64-pin
			LCD_SEG15	O	LCD segment output 15 at 48-pin
			UART0_RTSn	O	UART0 Request to Send output pin
			SPI0_MOSI0	I/O	SPI0 1st MOSI (Master Out, Slave In) pin
			TM0	I/O	Timer0 external counter input or Timer0 toggle out.
			FCLK0	O	Frequency Divider0 output pin
9	4	2	PB.13	I/O	General purpose digital I/O pin
			LCD_SEG25	O	LCD segment output 25 at 100-pin
			LCD_SEG21	O	LCD segment output 21 at 64-pin
			LCD_SEG14	O	LCD segment output 14 at 48-pin
			UART0_RXD	I	UART0 Data receiver input pin
			SPI0_MISO0	I/O	SPI0 1st MISO (Master In, Slave Out) pin
10	5	3	PB.14	I/O	General purpose digital I/O pin
			LCD_SEG24	O	LCD segment output 24 at 100-pin
			LCD_SEG20	O	LCD segment output 20 at 64-pin
			LCD_SEG13	O	LCD segment output 13 at 48-pin
			UART0_TXD	O	UART0 Data transmitter output pin (This pin could be modulated with PWM0 output.)
			SPI0_CLK	I/O	SPI0 serial clock pin
11			NC		
12	6	4	PB.15	I/O	General purpose digital I/O pin
			LCD_SEG23	O	LCD segment output 23 at 100-pin
			LCD_SEG19	O	LCD segment output 19 at 64-pin
			LCD_SEG12	O	LCD segment output 12 at 48-pin
			UART0_CTSn	I	UART0 Clear to Send input pin
			SPI0_SS0	I/O	SPI0 1st slave select pin
13	7	5	PC.0	I/O	General purpose digital I/O pin
			LCD_SEG22	O	LCD segment output 24 at 100-pin
			LCD_SEG18	O	LCD segment output 18 at 64-pin
			LCD_SEG11	O	LCD segment output 11 at 48-pin
			SPI0_SS1	I/O	SPI0 2nd slave select pin
			I2C0_SCL	I/O	I^2C0 clock pin

Pin No.			Pin Name	Pin Type	Description
100-pin	64-pin	48-pin			
			PWM0_CH0	**I/O**	PWM0 Channel0 output
14	8	6	PC.1	**I/O**	General purpose digital I/O pin
			LCD_SEG21	**O**	LCD segment output 21 at 100-pin
			LCD_SEG17	**O**	LCD segment output 17 at 64-pin
			LCD_SEG10	**O**	LCD segment output 10 at 48-pin
			I2C0_SDA	**I/O**	I^2C0 data I/O pin
			PWM0_CH1	**I/O**	PWM0 Channel1 output
15	9	7	PC.2	**I/O**	General purpose digital I/O pin
			LCD_SEG20	**O**	LCD segment output 20 at 100-pin
			LCD_SEG16	**O**	LCD segment output 16 at 64-pin
			LCD_SEG9	**O**	LCD segment output 9 at 48-pin
			I2C1_SCL	**O**	I^2C1 clock pin
			PWM0_CH2	**I/O**	PWM0 Channel2 output
16	10	8	PC.3	**I/O**	General purpose digital I/O pin
			LCD_SEG19	**O**	LCD segment output 19 at 100-pin
			LCD_SEG15	**O**	LCD segment output 15 at 64-pin
			LCD_SEG8	**O**	LCD segment output 8 at 48-pin
			I2C1_SDA	**I/O**	I^2C1 data I/O pin
			PWM0_CH3	**I/O**	PWM0 Channel3 output
17	11	9	PC.4	**I/O**	General purpose digital I/O pin
			LCD_SEG18	**O**	LCD segment output 18 at 100-pin
			LCD_SEG14	**O**	LCD segment output 14 at 64-pin
			LCD_SEG7	**O**	LCD segment output 7 at 48-pin
			UART1_CTSn	**I**	UART1 Clear to Send input pin
			SC0_CLK	**O**	SmartCard0 clock pin (SC0_UART_TXD)
			INT0	**I**	External interrupt0 input pin
18	12	10	PC.5	**I/O**	General purpose digital I/O pin
			LCD_SEG17	**O**	LCD segment output 17 at 100-pin
			LCD_SEG13	**O**	LCD segment output 13 at 64-pin
			LCD_SEG6	**O**	LCD segment output 6 at 48-pin
			SC0_CD	**I**	SmartCard0 card detect pin
19	13	11	PC.6	**I/O**	General purpose digital I/O pin
			LCD_SEG16	**O**	LCD segment output 16 at 100-pin

Pin No.			Pin Name	Pin Type	Description
100-pin	64-pin	48-pin			
			LCD_SEG12	**O**	LCD segment output 12 at 64-pin
			LCD_SEG5	**O**	LCD segment output 5 at 48-pin
			UART1_RTSn	**O**	UART1 Request to Send output pin
			SC0_DAT	**I/O**	SmartCard0 DATA pin (SC0_UART_RXD)
20	14	12	PC.7	**I/O**	General purpose digital I/O pin
			LCD_SEG15	**O**	LCD segment output 15 at 100-pin
			LCD_SEG11	**O**	LCD segment output 11 at 64-pin
			LCD_SEG4	**O**	LCD segment output 4 at 48-pin
			UART1_RXD	**I**	UART1 Data receiver input pin
			SC0_PWR	**O**	SmartCard0 Power pin
21	15	13	PC.8	**I/O**	General purpose digital I/O pin
			LCD_SEG14	**O**	LCD segment output 14 at 100-pin
			LCD_SEG10	**O**	LCD segment output 10 at 64-pin
			LCD_SEG3	**O**	LCD segment output 3 at 48-pin
			UART1_TXD	**O**	UART1 Data transmitter output pin (This pin could be modulated with PWM0 output.)
			SC0_RST	**O**	SmartCard0 RST pin
22	16	14	PC.9	**I/O**	General purpose digital I/O pin
			LCD_SEG13	**O**	LCD segment output 13 at 100-pin
			LCD_SEG9	**O**	LCD segment output 9 at 64-pin
			LCD_SEG2	**O**	LCD segment output 2 at 48-pin
23			V_{DD}	**P**	Power supply for I/O ports and LDO source
24			V_{SS}	**G**	Ground for digital circuit
25			V_{SS}	**G**	Ground for digital circuit
26			PC.10	**I/O**	General purpose digital I/O pin
			LCD_SEG12	**O**	LCD segment output 12 at 100-pin
			I2C1_SCL	**I/O**	I^2C1 clock pin
			SC1_CD	**I**	SmartCard1 card detect pin
27			PC.11	**I/O**	General purpose digital I/O pin
			LCD_SEG11	**O**	LCD segment output 11 at 100-pin
			I2C1_SDA	**I/O**	I^2C 1 data I/O pin
			SC1_PWR	**O**	SmartCard1 PWR pin

Pin No.			Pin Name	Pin Type	Description
100-pin	64-pin	48-pin			
28			PC.12	I/O	General purpose digital I/O pin
			LCD_SEG10	O	LCD segment output 10 at 100-pin
			SC1_CLK	O	SmartCard1 clock pin (SC1_UART_TXD)
29			PC.13	I/O	General purpose digital I/O pin
			LCD_SEG9	O	LCD segment output 9 at 100-pin
			SC1_DAT	I/O	SmartCard1 DATA pin (SC1_UART_RXD)
30	17	15	PC.14	I/O	General purpose digital I/O pin
			LCD_SEG8	O	LCD segment output 8 at 100-pin
			LCD_SEG8	O	LCD segment output 8 at 64-pin
			LCD_SEG1	O	LCD segment output 1 at 48-pin
			SC1_CD	I	SmartCard1 card detect
31	18	16	PC.15	I/O	General purpose digital I/O pin
			LCD_SEG7	O	LCD segment output 7 at 100-pin
			LCD_SEG7	O	LCD segment output 7 at 64-pin
			LCD_SEG0	O	LCD segment output 0 at 48-pin
			SC1_PWR	O	SmartCard1 PWR pin
32	19		PD.0	I/O	General purpose digital I/O pin
			LCD_SEG6	O	LCD segment output 6 at 100-pin
			LCD_SEG6	O	LCD segment output 6 at 64-pin
33	20		PD.1	I/O	General purpose digital I/O pin
			LCD_SEG5	O	LCD segment output 5 at 100-pin
			LCD_SEG5	O	LCD segment output 5 at 64-pin
34	21		PD.2	I/O	General purpose digital I/O pin
			LCD_SEG4	O	LCD segment output 4 at 100-pin
			LCD_SEG4	O	LCD segment output 4 at 64-pin
35	22		PD.3	I/O	General purpose digital I/O pin
			LCD_SEG3	O	LCD segment output 3 at 100-pin
			LCD_SEG3	O	LCD segment output 3 at 64-pin
36	23		PD.4	I/O	General purpose digital I/O pin
			LCD_SEG2	O	LCD segment output 2 at 100-pin
			LCD_SEG2	O	LCD segment output 2 at 64-pin
			SC1_RST	O	SmartCard1 RST pin

Pin No.			Pin Name	Pin Type	Description
100-pin	64-pin	48-pin			
37	24		PD.5	**I/O**	General purpose digital I/O pin
			LCD_SEG1	**O**	LCD segment output 1 at 100-pin (or as LCD_COM5)
			LCD_SEG1	**O**	LCD segment output 1 at 64-pin (or as LCD_COM5)
38	25		PD.6	**I/O**	General purpose digital I/O pin
			LCD_SEG0	**O**	LCD segment output 0 at 100-pin(or as LCD_COM4)
			LCD_SEG0	**O**	LCD segment output 0 at 64-pin (or as LCD_COM4)
39	26	17	PD.7	**I/O**	General purpose digital I/O pin
			LCD_COM3	**O**	LCD common output 3 at 100-pin
			LCD_COM3	**O**	LCD common output 3 at 64-pin
			LCD_COM3	**O**	LCD common output 3 at 48-pin
			SC1_CLK	**O**	SmartCard1 clock pin (SC1_UART_TXD)
40	27	18	PD.8	**I/O**	General purpose digital I/O pin
			LCD_COM2	**O**	LCD common output 2 at 100-pin
			LCD_COM2	**O**	LCD common output 2 at 64-pin
			LCD_COM2	**O**	LCD common output 2 at 48-pin
			SC1_DAT	**I/O**	SmartCard1 DATA pin (SC1_UART_RXD)
41	28	19	PD.9	**I/O**	General purpose digital I/O pin
			LCD_COM1	**O**	LCD common output 1 at 100-pin
			LCD_COM1	**O**	LCD common output 1 at 64-pin
			LCD_COM1	**O**	LCD common output 1 at 48-pin
			SC1_RST	**O**	SmartCard1 RST pin
			PWM0_CH3	**I/O**	PWM0 Channel3 output
42	29	20	PD.10	**I/O**	General purpose digital I/O pin
			LCD_COM0	**O**	LCD common output 0 at 100-pin
			LCD_COM0	**O**	LCD common output 0 at 64-pin
			LCD_COM0	**O**	LCD common output 0 at 48-pin
			PWM0_CH2	**I/O**	PWM0 Channel2 output
			TC1	**I**	Timer1 capture input
43	30		PD.11	**I/O**	General purpose digital I/O pin
			LCD_DH2	**O**	LCD external capacitor pin of charge pump circuit at 100-pin

Pin No.			Pin Name	Pin Type	Description
100-pin	64-pin	48-pin			
			LCD_DH2	**O**	LCD external capacitor pin of charge pump circuit at 64-pin
			PWM0_CH1	**I/O**	PWM0 Channel1 output
			TC0	**I**	Timer0 capture input
44	31		PD.12	**I/O**	General purpose digital I/O pin
			CLK_Hz	**O**	1, 1/2, 1/4, 1/8, 1/16 Hz clock output
			LCD_DH1	**O**	LCD external capacitor pin of charge pump circuit at 100-pin
			LCD_DH1	**O**	LCD external capacitor pin of charge pump circuit at 64-pin
			PWM0_CH0	**I/O**	PWM0 Channel0 output
			TM1	**I/O**	Timer1 external counter input
			FCLK0	**O**	Frequency Divider0 output pin
45					NC
46	32	21	V_{LCD}	**P**	LCD power supply pin
47					NC
48	33	22	PD.13	**I/O**	General purpose digital I/O pin
			LCD_V1	**I**	Input pin of the 1st most positive LCD level at 100-pin
			LCD_V1	**I**	Input pin of the 1st most positive LCD level at 64-pin
			LCD_V1	**I**	Input pin of the 1st most positive LCD level at 48-pin
			INT1	**I**	External interrupt 1 input pin
49	34	23	PD.14	**I/O**	General purpose digital I/O pin
			LCD_V2	**I**	Input pin of the 2nd most positive LCD level at 100-pin
			LCD_V2	**I**	Input pin of the 2nd most positive LCD level at 64-pin
			LCD_V2	**I**	Input pin of the 2nd most positive LCD level at 48-pin
50	35	24	PD.15	**I/O**	General purpose digital I/O pin
			LCD_V3	**I**	Input pin of the 3rd most positive LCD level at 100-pin
			LCD_V3	**I**	Input pin of the 3rd most positive LCD level at 64-pin
			LCD_V3	**I**	Input pin of the 3rd most positive LCD level at 48-pin

Pin No.			Pin Name	Pin Type	Description
100-pin	64-pin	48-pin			
51	35	25	nRESET		External reset input: low active. Setting this pin low will reset chip to initial state. With internal pull-up.
52	37	26	LDO_CAP	**P**	LDO capacitor pin
53	38	27	V_{DD}	**P**	Power supply for I/O ports and LDO source
54	38	28	PF.0	**I/O**	General purpose digital I/O pin
			X32I	**I**	External 32.768 kHz crystal input pin(default)
			TM3	**I/O**	Timer3 external counter input or Timer3 toggle out.
55	40	29	PF.1	**I/O**	General purpose digital I/O pin
			X32O	**O**	External 32.768 kHz crystal output pin(default)
			TM2	**I/O**	Timer2 external counter input or Timer2 toggle out.
56			V_{SS_PLL}	**G**	Ground for PLL
57	41	30	V_{SS}	**G**	Ground for digital circuit
58			V_{SS}	**G**	Ground for digital circuit
59	42	31	PF.2	**I/O**	General purpose digital I/O pin
			XT1_IN	**AI**	External 4~24 MHz crystal input pin(default)
			UART1_RXD	**I**	UART1 Data receiver input pin
			TC3	**I**	Timer3 capture input
			INT1	**I**	External interrupt1 input pin
60	43	32	PF.3	**I/O**	General purpose digital I/O pin
			XT1_OUT	**AO**	External 4~24 MHz crystal output pin
			UART1_TXD	**O**	UART1 Data transmitter output pin (This pin could be modulated with PWM0 output.)
			TC2	**I**	Timer 2 capture input
			INT0	**I**	External interrupt0 input pin
61					NC
62			PE.0	**I/O**	General purpose digital I/O pin
			SPI0_MOSI0	**I/O**	SPI0 1st MOSI (Master Out, Slave In) pin
63			PE.1	**I/O**	General purpose digital I/O pin
			SPI0_MISO0	**I/O**	SPI0 1st MISO (Master In, Slave Out) pin
64			PE.2	**I/O**	General purpose digital I/O pin

Pin No.			Pin Name	Pin Type	Description
100-pin	64-pin	48-pin			
			SPI0_CLK	**I/O**	SPI0 serial clock pin
65			PE.3	**I/O**	General purpose digital I/O pin
			SPI0_SS0	**I/O**	SPI0 1st slave select pin
66			PE.4	**I/O**	General purpose digital I/O pin
			SC1_RST	**O**	SmartCard1 RST pin
67			PE.5	**I/O**	General purpose digital I/O pin
			SC1_PWR	**O**	SmartCard1 PWR pin
68			PE.6	**I/O**	General purpose digital I/O pin
			SC1_CLK	**O**	SmartCard1 clock pin (SC1_UART_TXD)
69			PE.7	**I/O**	General purpose digital I/O pin
			SC1_DAT	**I/O**	SmartCard1 DATA pin (SC1_UART_RXD)
70	44	33	AV_{SS}	**G**	Ground for ADC and comparators
71			AV_{SS}	**G**	Ground for ADC and comparators
72	45	34	PA.0	**I/O**	General purpose digital I/O pin
			AD0	**AI**	ADC analog input0
73	46	35	PA.1	**I/O**	General purpose digital I/O pin
			ACMP0_CHDIS	**O**	Comparator0 charge/discharge path
			ACMP0_P3	**AI**	Comparator0 P-end input3
			AD1	**AI**	ADC analog input1
74	47	36	PA.2	**I/O**	General purpose digital I/O pin
			ACMP0_CHDIS	**O**	Comparator0 charge/discharge path
			SC0_CLK	**O**	SmartCard0 clock pin (SC0_UART_TXD)
			ACMP0_P2	**AI**	Comparator0 P-end input2
			AD2	**AI**	ADC analog input2
			INT0	**I**	External interrupt0 input pin
75	48	37	PA.3	**I/O**	General purpose digital I/O pin
			ACMP0_CHDIS	**O**	Comparator0 charge/discharge path
			SC0_DAT	**I/O**	SmartCard0 DATA pin (SC0_UART_RXD)
			ACMP0_P1	**AI**	Comparator0 P-end input1
			AD3	**AI**	ADC analog input3
			INT1	**I**	External interrupt 1

Pin No.			Pin Name	Pin Type	Description
100-pin	64-pin	48-pin			
76	49	38	PA.4	**I/O**	General purpose digital I/O pin
			ACMP0_CHDIS	**O**	Comparator0 charge/discharge path
			SC0_CD	**I**	SmartCard0 card detect pin
			ACMP0_P0	**AI**	Comparator0 P-end input0
			AD4	**AI**	ADC analog input4
77	50	39	PA.5	**I/O**	General purpose digital I/O pin
			ACMP0_CHDIS	**O**	Comparator0 charge/discharge path
			SPI1_SS0	**I/O**	SPI1 1st slave select pin
			I2C1_SDA	**I/O**	I^2C1 data I/O pin
			SC0_PWR	**O**	SmartCard0 Power pin
			ACMP0_N	**AI**	Comparator0 N-end input0
			AD5	**AI**	ADC analog input5
78	51	40	PA.6	**I/O**	General purpose digital I/O pin
			ACMP0_CHDIS	**O**	Comparator0 charge/discharge path
			SC0_RST	**O**	SmartCard0 RST pin
			ACMP0_OUT	**O**	Comparator0 output
			AD6	**AI**	ADC analog input6
79			PA.7	**I/O**	General purpose digital I/O pin
			SC1_CD	**I**	SmartCard1 card detect
			AD7	**AI**	ADC analog input7
80	52	41	V_{REF}	**A**	ADC/Comparator reference voltage
81	53	42	AV_{DD}	**P**	Power supply for ADC and comparators
82	54	43	PF.4	**I/O**	General purpose digital I/O pin
			ICE_CLK	**I**	Serial Wired Debugger Clock pin
			CLK_Hz	**O**	1, 1/2, 1/4, 1/8, 1/16 Hz clock output
			PWM0_CH2	**O**	PWM0 Channel2 output
			TC1	**I**	Timer1 capture input
			FCLK1	**O**	Frequency Divider1 output pin
83	55	44	PF.5	**I/O**	General purpose digital I/O pin
			ICE_DAT	**I/O**	Serial Wired Debugger Data pin
			ACMP0_CHDIS	**O**	Comparator0 charge/discharge path
			PWM0_CH3	**I/O**	PWM0 Channel3 output
			TC0	**I**	Timer0 capture input

Pin No.			Pin Name	Pin Type	Description
100-pin	64-pin	48-pin			
84			PA.8	**I/O**	General purpose digital I/O pin
			SC0_PWR	**O**	SmartCard0 Power pin
85			PA.9	**I/O**	General purpose digital I/O pin
			SC0_RST	**O**	SmartCard0 RST pin
86			PA.10	**I/O**	General purpose digital I/O pin
			SC0_CLK	**O**	SmartCard0 clock pin (SC0_UART_TXD)
87			PA.11	**I/O**	General purpose digital I/O pin
			SC0_DAT	**I/O**	SmartCard0 DATA pin(SC0_UART_RXD)
			STADC	**I**	ADC external trigger input.
88	56	45	PA.12	**I/O**	General purpose digital I/O pin
			LCD_SEG19	**O**	LCD segment output 19 at 48-pin
			UART0_TXD	**O**	UART0 Data transmitter output pin (This pin could be modulated with PWM0 output.)
			SPI1_MOSI0	**I/O**	SPI1 1st MOSI (Master Out, Slave In) pin
			I2C0_SCL	**I/O**	I^2C 0 clock pin
			ACMP1_P	**AI**	Comparator1 P-end input
89	57	46	PA.13	**I/O**	General purpose digital I/O pin
			LCD_SEG18	**O**	LCD segment output 18 at 48-pin
			UART0_RXD	**I**	UART0 Data receiver input pin
			SPI1_MISO0	**I/O**	SPI1 1st MISO (Master In, Slave Out) pin
			I2C0_SDA	**I/O**	I^2C0 data I/O pin
			ACMP1_N	**AI**	Comparator1 N-end input
90	58	47	PA.14	**I/O**	General purpose digital I/O pin
			ACMP0_CHDIS	**O**	Comparator0 charge/discharge path
			LCD_SEG31	**O**	LCD segment output 31 at 64-pin
			LCD_SEG17	**O**	LCD segment output 17 at 48-pin
			SPI1_CLK	**I/O**	SPI1 serial clock pin
			I2C1_SCL	**I/O**	I^2C1 clock pin
91	59	48	PA.15	**I/O**	General purpose digital I/O pin
			LCD_SEG30	**O**	LCD segment output 30 at 64-pin
			LCD_SEG16	**O**	LCD segment output 16 at 48-pin
			SPI1_SS0	**I/O**	SPI1 1st slave select pin

Pin No.			Pin Name	Pin Type	Description
100-pin	64-pin	48-pin			
			I2C1_SDA	**I/O**	I^2C1 data I/O pin
			ACMP1_OUT	**O**	Comparator1 output
			TC3	**I**	Timer3 capture input
92	60		PB.0	**I/O**	General purpose digital I/O pin
			LCD_SEG29	**O**	LCD segment output 29 at 64-pin
			UART0_TXD	**O**	UART0 Data transmitter output pin (This pin could be modulated with PWM0 output.)
			FCLK1	**O**	Frequency Divider1 output pin
93	61		PB.1	**I/O**	General purpose digital I/O pin
			LCD_SEG28	**O**	LCD segment output 28 at 64-pin
			UART0_RXD	**I**	UART0 Data receiver input pin
			TC2	**I**	Timer 2 capture input
			INT1	**I**	External interrupt1 input pin
94	62		PB.2	**I/O**	General purpose digital I/O pin
			LCD_SEG27	**O**	LCD segment output 27 at 64-pin
			UART0_RTSn	**O**	UART0 Request to Send output pin
			SPI1_MOSI1	**I/O**	SPI1 2nd MOSI (Master Out, Slave In) pin
			I2C0_SCL	**O**	I^2C0 clock pin
			TM3	**I/O**	Timer3 external counter input or Timer3 toggle out.
95	63		PB.3	**I/O**	General purpose digital I/O pin
			LCD_SEG26	**O**	LCD segment output 26 at 64-pin
			UART0_CTSn	**I**	UART0 Clear to Send input pin
			SPI1_MISO1	**I/O**	SPI1 2nd MISO (Master In, Slave Out) pin
			I2C0_SDA	**I/O**	I^2C0 data I/O pin
			TM2	**I/O**	Timer2 external counter input or Timer2 toggle out.
96			V_{DD}	**P**	Power supply for I/O ports and LDO source
97			V_{SS}	**G**	Ground for digital circuit
98			PB.4	**I/O**	General purpose digital I/O pin
			UART1_RTSn	**O**	UART1 Request to Send output pin
			SPI1_MISO1	**I/O**	SPI1 2nd MISO (Master In, Slave Out) pin
99			PB.5	**I/O**	General purpose digital I/O pin
			LCD_SEG35	**O**	LCD segment output 35 at 100-pin

Pin No.			Pin Name	Pin Type	Description
100-pin	64-pin	48-pin			
			UART1_RXD	**I**	UART1 Data receiver input pin
			SPI1_MOSI1	**I/O**	SPI1 2nd MOSI (Master Out, Slave In) pin
100	64		PB.6	**I/O**	General purpose digital I/O pin
			LCD_SEG34	**O**	LCD segment output 34 at 100-pin
			LCD_SEG25	**O**	LCD segment output 25 at 64-pin
			UART1_TXD	**O**	UART1 Data transmitter output pin (This pin could be modulated with PWM0 output.)
			SPI1_SS1	**I/O**	SPI1 2nd slave select pin
			FCLK0	**O**	Frequency Divider0 output pin

Note: Pin Type: I = Digital Input, O=Digital Output; AI=Analog Input; AO= Analog Output; P=Power Pin; AP=Analog Power.

5 BLOCK DIAGRAM

5.1 Nano102 Block Diagram

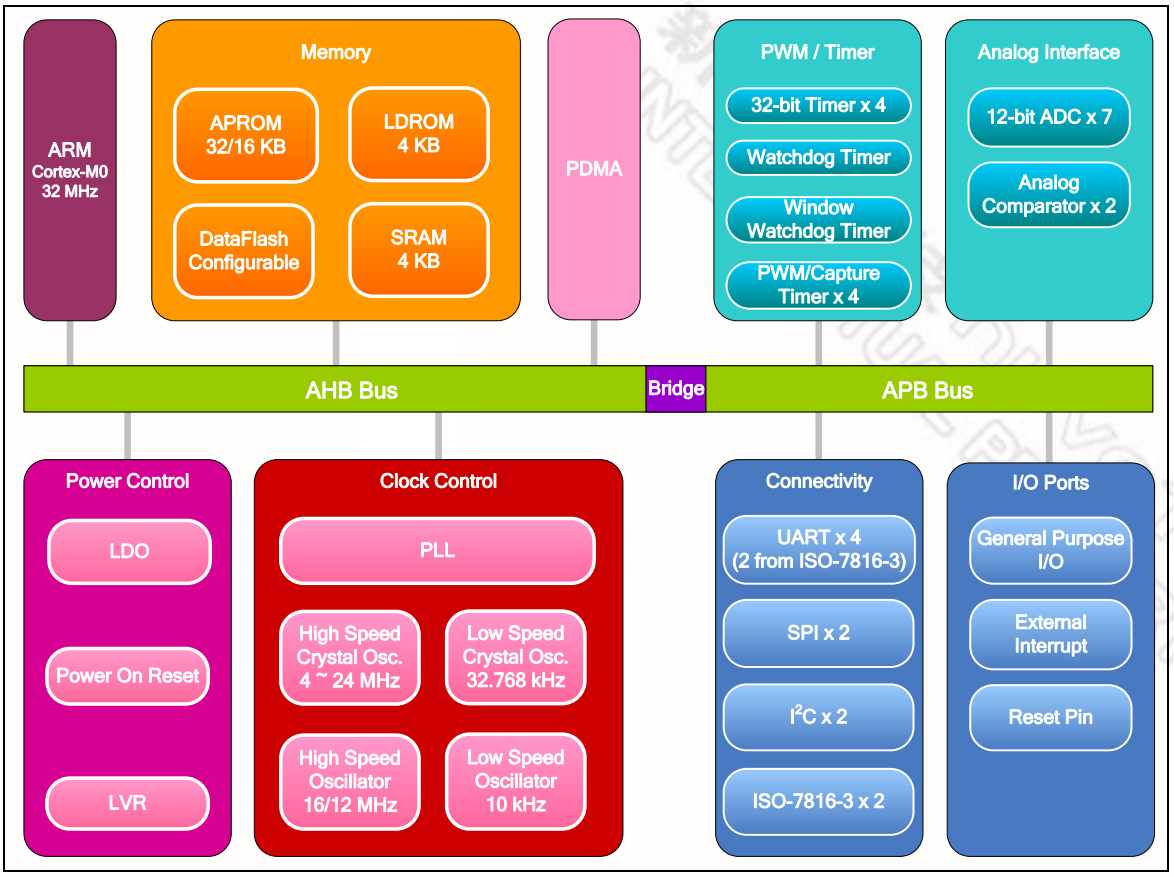


Figure 5-1 NuMicro™ Nano102 Block Diagram

5.2 Nano112 Block Diagram

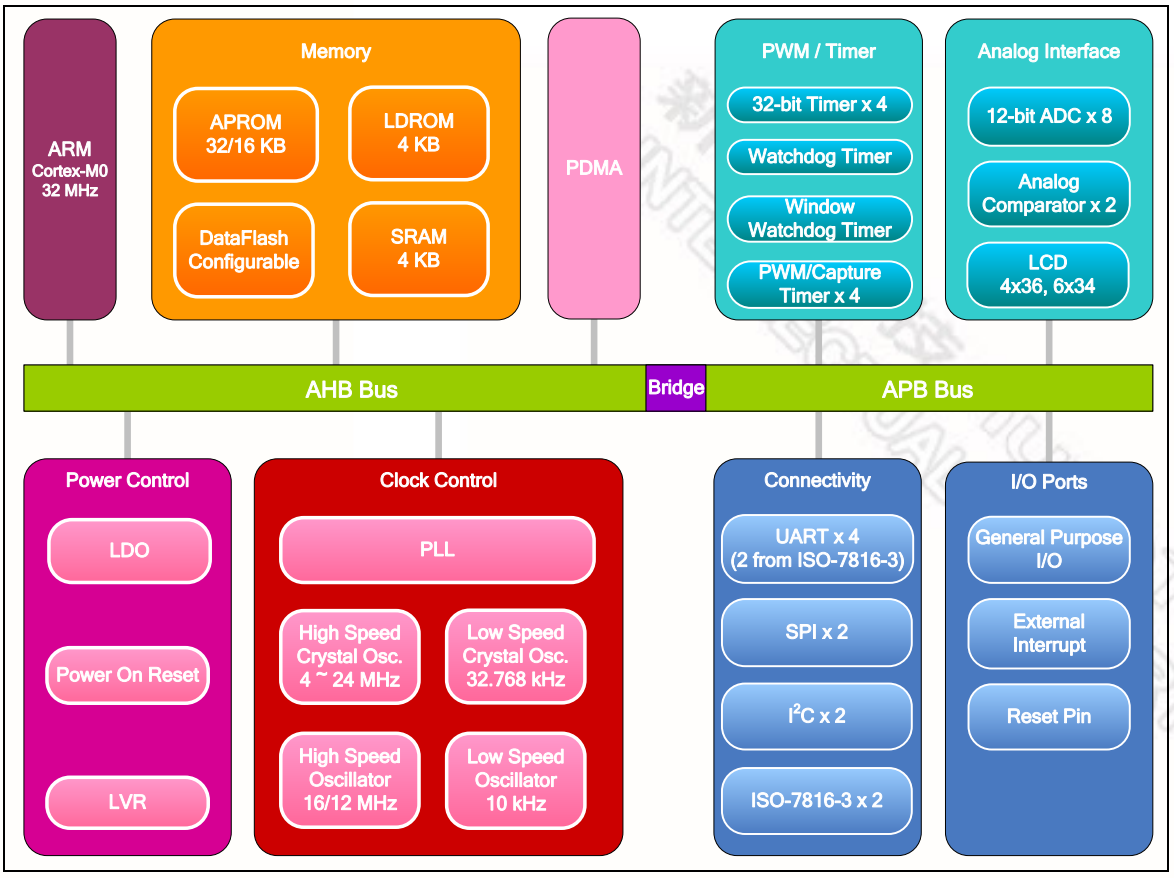


Figure 5-2 NuMicro™ Nano112 Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 ARM® Cortex™-M0 Core

The Cortex™-M0 processor is a configurable, multistage, 32-bit RISC processor, which has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex™-M profile processor. The profile supports two modes –Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. The following figure shows the functional controller of processor.

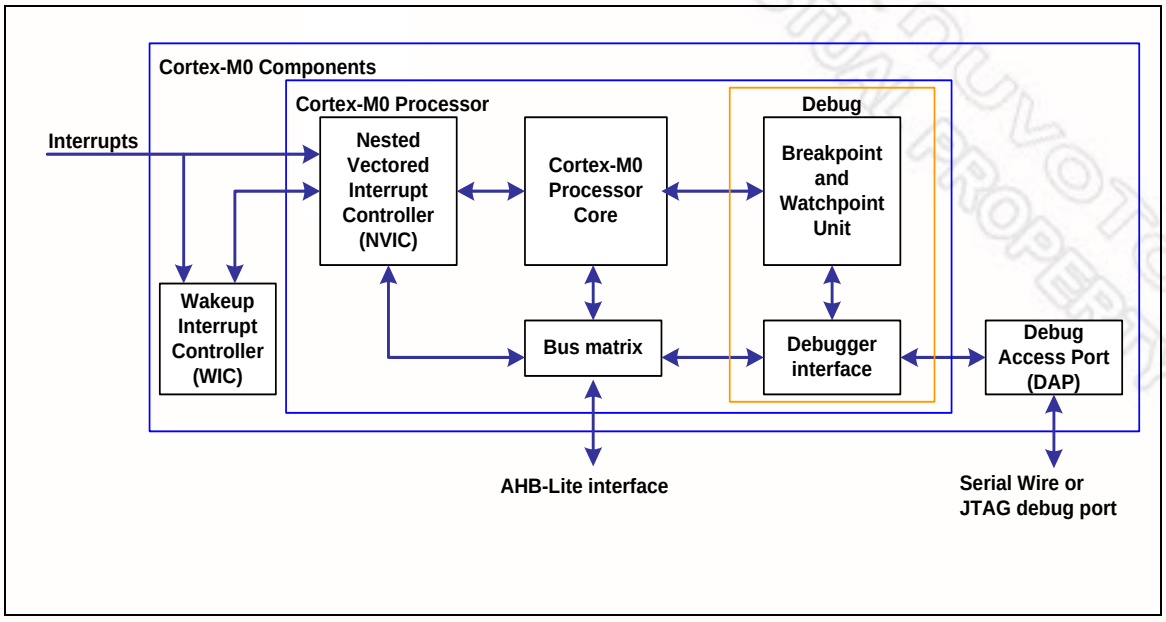


Figure 6-1 Functional Block Diagram

The implemented device provides:

- A low gate count processor:
  - ARMv6-M Thumb® instruction set
  - Thumb-2 technology
  - ARMv6-M compliant 24-bit SysTick timer
  - A 32-bit hardware multiplier
  - System interface supported with little-endian data accesses
  - Ability to have deterministic, fixed-latency, interrupt handling
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - C Application Binary Interface compliant exception model. This is the ARMv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
  - Low Power Sleep mode entry using the Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or return from interrupt sleep-on-exit feature

- NVIC:
  - 32 external interrupt inputs, each with four levels of priority
  - Dedicated Non-maskable Interrupt (NMI) input
  - Supports for both level-sensitive and pulse-sensitive interrupt lines
  - Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Sleep mode
- Debug support:
  - Four hardware breakpoints
  - Two watchpoints
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the DAP (Debug Access Port)

6.2 Memory Organization

6.2.1 Overview

The Nano112 provides 4G-byte addressing space. The memory locations assigned to each on-chip modules are shown in following. The detailed register definition, memory space, and programming detailed will be described in the following sections for each on-chip module. The Nano112 series only supports little-endian data format.

6.3 Nested Vectored Interrupt Controller (NVIC)

6.3.1 Overview

The Cortex-M0 provides an interrupt controller as an integral part of the exception mode, named as “Nested Vectored Interrupt Controller (NVIC)”. It is closely coupled to the processor kernel and provides following features:

6.3.2 Features

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Dynamic priority changing
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in “Handler Mode”. This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one’s priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When any interrupts is accepted, the starting address of the interrupt service routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers “PC, PSR, LR, R0~R3, R12” to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports “Tail Chaining” which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports “Late Arrival” which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the “ARM® Cortex™-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

6.4 System Manager

6.4.1 Overview

System manager mainly controls the power modes, wake-up sources, system resets, scalable LDO and system memory map. It also provides information about product ID, chip reset, IP reset, and multi-function pin control.

6.4.2 Features

- Power modes and wake-up sources
- System Power Architecture
- System resets
- Scalable LDO
- System Memory Map
- System manager registers for :
  - Part Number ID
  - Chip and IP reset
  - Multi-functional pin control

6.5 Clock Controller

6.5.1 Overview

The clock controller generates clocks for the whole chip, Iincluding system clocks (CPU clock, HCLKx, and PCLKx) and all peripheral module clocks. HCLKx means AHB bus clock for peripherals on AHB bus. PCLKx means APB bus clock for peripherals on APB bus. PCLKx can be the same as HCLKx or devided from HCLKx. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and a 4-bit clock divider. The chip will not enter power-down mode until CPU sets the power down enable bit PD_EN(PWRCTL[6]) and executes the WFI instruction. In the Power-down mode, clock controller turns off the external high frequency crystal, internal high frequency oscillator, and system clocks (CPU clock, HCLKx, and PCLKx) to reduce the power consumption.

The clock controller consists of 5 sources as listed below:

- 32768Hz external low speed crystal oscillator (LXT)
- 4~ 24 MHz external high speed crystal oscillator (HXT)
- 12/16 MHz internal high speed RC oscillator (HIRC)
- One programmable PLL FOUT (PLL source can be selected from HXT or HIRC)
- 10 kHz internal low speed RC oscillator (LIRC)

6.5.2 Features

- Generates clocks for system clocks and all peripheral module clocks.
- Each peripheral module clock can be turned on/off.
- High frequency crystal, internal high frequency oscillator, and system clocks will be turned off when chip is in Power-down mode.

6.6 Flash Memory Controller (FMC)

6.6.1 Overview

This chip is equipped with 16/32 Kbytes on-chip embedded flash memory for application program memory (APROM) that can be updated through ISP/IAP procedure. In System Programming (ISP) function enables user to update program memory when chip is soldered on PCB. After chip powered on Cortex-M0 CPU fetches code from APROM or LDROM decided by boot select (CBS) in Config0. By the way, this chip also provides Data Flash Region, the Data Flash is shared with original program memory and its start address is configurable and defined by user in Config1. The Data Flash size is defined by user application request.

6.6.2 Features

- 16/32 Kbytes application program memory (APROM)
- 4 Kbytes in system programming (ISP) loader program memory (LDROM)
- Programmable Data Flash start address and memory size with 512 bytes page erase unit
- 512 bytes system program memory (SPROM)
- In System Program (ISP)/In Application Program (IAP) to update on chip flash memory

6.7 General Purpose I/O Controller

6.7.1 Overview

The NuMicro Nano112™ series have up to 80 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 80 pins are arranged in 6 ports named with GPIOA, GPIOB, GPIOC, GPIOD, GPIOE and GPIOF. Each one of the 80 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be independently software configured as input, output, and open-drain mode. Each I/O pin has a very weak individual pull-up resistor which is about 110 KΩ~300 KΩ for V_{DD} from 1.8 V to 3.6 V.

6.7.2 Features

- Three I/O modes:
  - Schmitt trigger Input-only with high impendence
  - Push-pull output
  - Open-drain output
- I/O pin configured as interrupt source with edge/level setting
- Enabling the pin interrupt function will also enable the pin wake-up function

6.8 DMA Controller

6.8.1 Overview

The NuMicro™ NANO112 series DMA contains four-channel peripheral direct memory access (PDMA) controller and a cyclic redundancy check (CRC) generator.

The PDMA that transfers data to and from memory or transfer data to and from peripherals. For PDMA channel (PDMA CH1~CH4), there is one-word buffer as transfer buffer between the Peripherals APB devices and Memory. User can stop the PDMA operation by disable PDMACEN (PDMA_CSRx[0]). User can polling TD_IS (PDMA_ISRx[1]) or enable BLKD_IE (PDMA_IERx[1]) and wait interrupt to check PDMA transfer complete . The DMA controller can increase source or destination address, fixed or wrap around them as well.

The DMA controller contains a cyclic redundancy check (CRC) generator that can perform CRC calculation with programmable polynomial settings. The CRC engine supports CPU mode and DMA transfer mode.

6.8.2 Features

- Supports four PDMA channels (CH1 ~ CH4) and one CRC channel. Each PDMA channel can support a unidirectional transfer
- AMBA AHB master/slave interface compatible, for data transfer and register read/write
- Hardware round robin priority scheme. DMA channel 1 has the highest priority and channel 4 has the lowest priority
- PDMA
  - Peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer
  - Supports word boundary address
  - Supports word alignment transfer length in memory-to-memory mode
  - Supports word/half-word/byte alignment transfer length in peripheral-to-memory and memory-to-peripheral mode
  - Supports word/half-word/byte transfer data width from/to peripheral
  - Supports address direction: increment, fixed, and wrap around
  - Supports time-out function in all channel
- Cyclic Redundancy Check (CRC)
  - Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
    - CRC-CCITT: X16 + X12 + X5 + 1
    - CRC-8: X8 + X2 + X + 1
    - CRC-16: X16 + X15 + X2 + 1
    - CRC-32: X32 + X26 + X23 + X22 + X16 + X12 + X11 + X10 + X8 + X7 + X5 + X4 + X2 + X + 1
  - Programmable seed value
  - Supports programmable order reverse setting for input data and CRC checksum
  - Supports programmable 1's complement setting for input data and CRC checksum
  - Supports CPU mode or DMA transfer mode
  - Supports 8/16/32-bit of data width in CRC CPU mode
    - 8-bit write mode: 1-AHB clock cycle operation
    - 16-bit write mode: 2-AHB clock cycle operation
    - 32-bit write mode: 4-AHB clock cycle operation
  - Supports byte alignment transfer length in CRC DMA mode

6.9 Timer Controller

6.9.1 Overview

This chip is equipped with four timer modules including TIMER0, TIMER1, TIMER2 and TIMER3, which allow user to easily implement a counting scheme or timing control for applications. The timer can perform functions like frequency measurement, event counting, interval measurement, clock generation, delay timing, and so on. The timer can generate an interrupt signal upon timeout, or provide the current value of count during operation.

6.9.2 Features

- Independent Clock Source for each Timer (TMRx_CLK, x= 0, 1,2,3)
- Time-out period = (Period of timer clock input) * (8-bit pre-scale counter + 1) * (24-bit TCMP)
- Counting cycle time = (1 / TMRx_CLK) * (2^8) * (2^24)
- Internal 8-bit pre-scale counter
- Internal 24-bit up counter is readable through TDR (Timer Data Register)
- Supports One-shot, Periodic, Output Toggle and Continuous Counting Operation mode
- Supports external pin capture for interval measurement
- Supports external pin capture for timer counter reset
- Supports Inter-Timer trigger
- Supports event generator in TIMER 0 and TIMER 2 to generate event to TIMER1 and TIMER3, respectively.
- Supports Internal trigger event to ADC and PDMA

6.10 Pulse Width Modulation (PWM)

6.10.1 Overview

This chip has one PWM controller, which includes 4 independent PWM outputs, CH0~CH3, or as 2 complementary PWM pairs, (CH0, CH1), (CH2, CH3) with 2 programmable dead-zone generators.

Each of the two PWM outputs, (CH0, CH1), (CH2, CH3), share the same 8-bit prescaler, clock divider providing 5 divided frequencies (1, 1/2, 1/4, 1/8, 1/16). Each PWM output has independent 16-bit PWM counter which has two counting modes for PWM period control. The PWM counter operates as down counting in edge-aligned mode and up-down counting in center-aligned mode only. Each PWM output also has a 16-bit comparator for PWM duty control. Each dead-zone generator has two outputs. The first dead-zone generator output is CH0 and CH1, and for the second dead-zone generator, the output is CH2 and CH3. The PWM controller total provide four independent PWM interrupt flags which are set by hardware when the corresponding PWM period down counter in edge-aligned mode (or up-down counter in center-aligned mode) reaches 0. PWM interrupt will be asserted when both PWM interrupt source and its corresponding enable bit are active. Each PWM output can be configured as one-shot mode to produce only one PWM cycle signal or continuous mode to output PWM waveform continuously.

When DZEN01(PWM_CTL[4]) is set, CH0 and CH1 perform complementary PWM paired function; the paired PWM timing, period, duty and dead-time are determined by PWM channel 0 timer and Dead-zone generator 0. Similarly, When DZEN23(PWM_CTL[5]) is set the complementary PWM pair of (CH2, CH3) is controlled by PWM channel 2.

To prevent PWM driving output pin with unsteady waveform, the 16-bit period down counter and 16-bit comparator are implemented with double buffer. When user writes data to counter/comparator buffer registers the updated value will be loaded into the 16-bit down counter/ comparator at the time down counter reaching 0. The double buffering feature avoids glitch at PWM outputs.

When the 16-bit period down counter reaches 0, the interrupt request is generated. If PWM output is set as continuous mode, when the down counter reaches 0, it is reloaded with CN of PWM_DUTYy(y=0~3) Register automatically then start decreases, repeatedly. If the PWM output is set as one-shot mode, the down counter will stop and generate one interrupt request when it reaches 0.

The value of PWM counter comparator is used for pulse width modulation. The counter control logic changes the output level when down-counter value matches the value of compare register.

The alternate feature of the PWM is digital input capture function. If capture function is enabled the PWM output pin is switched as capture input pin. The capture channel 0 and PWM CH0 share one timer; and the capture channel 1 and PWM CH1 share one timer, and etc. Therefore user must set up the PWM timer before enabling capture feature. After capture feature of channel 0 is enabled, the capture always latches PWM CH0 timer value to Capture Rising Latch Register CRL (PWM_CRL0[15:0]) when input channel has a rising transition and latches PWM CH0 timer value to Capture Falling Latch Register CFL (PWM_CFL0[15:0]) when input channel has a falling transition. Capture channel 0 interrupt is programmable by setting CRL_IE0(PWM_CAPINTEN[0]) for rising transition or CFL_IE0 (PWM_CAPINTEN[1]) for falling transition. Whenever Capture rising event latched for channel 0, the PWM CH0 timer will be reload at this moment if the corresponding reload enable bit CAPRELOADREN0 (PWM_CAPCTL[6]) is set.

The maximum captured frequency that PWM can capture is dominated by the capture interrupt latency. When capture interrupt occurs, software will do at least three steps, they are: Read PWMINTSTS to tell it from interrupt source and Read PWM_CRLy/PWM_CFLy(y=0~3) to get capture value and finally write 1 to clear PWM_INTSTS. If interrupt latency will take time T0 to finish, the capture signal mustn't transient during this interval. In this case, the maximum capture frequency will be 1/T0.

6.10.2 Features

6.10.2.1 PWM Function:

- PWM controllers has 4 independent PWM outputs, CH0~CH3, or as 2 complementary PWM pairs, (CH0, CH1), (CH2, CH3) with 2 programmable dead-zone generators
- Up to 4 PWM channels or 2 PWM paired channels
- Up to 16 bits PWM counter width
- PWM Interrupt request synchronous with PWM period
- Single-shot or Continuous mode
- Two Dead-Zone generators

6.10.2.2 Capture Function:

- Timing control logic shared with PWM timer.
- 4 Capture input channels shared with 4 PWM output channels.
- Each channel supports one rising latch register CRL (PWM_CRL0[15:0]), one falling latch register CFL (PWM_CFL0[15:0]) and Capture interrupt flag CAPIF0 (PWM_CAPINTSTS[0]).
- Four 16-bit counters for four capture channels or two 32-bit counter for two capture channels when cascade is enabled: when CH01CASKEN (PWM_CAPCTL[13]) is set, the original 16-bit counter of channel 1 will combine with channel 0's 16 bit counter for channel 0 input capture counting and so does CH23CASKEN(PWM_CAPCTL[29]) for channel 2, 3
- Supports PDMA transfer function for PWM channel 0, 2

6.11 Watchdog Timer Controller

6.11.1 Overview

The purpose of Watchdog Timer is to perform a system reset after the software running into a problem. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake-up CPU from power-down mode. The watchdog timer includes an 18-bit free running counter with programmable time-out intervals.

6.11.2 Features

- 18-bit free running WDT counter for Watchdog timer time-out interval.
- Selectable time-out interval (2^4 ~ 2^18) and the time-out interval is 104 ms ~ 26.316 s (if WDT_CLK = 10 kHz).
- Reset period = (1 / 10 kHz) * 63, if WDT_CLK = 10 kHz.

6.12 Window Watchdog Timer Controller

6.12.1 Overview

The purpose of Window Watchdog Timer is to perform a system reset within a specified window period to prevent software run to uncontrollable status by any unpredictable condition.

6.12.2 Features

- 6-bit down counter and 6-bit compare value to make the window period flexible
- Selectable WWDT clock pre-scale counter to make WWDT time-out interval variable

6.13 RTC

6.13.1 Overview

Real Time Clock (RTC) unit provides user the real time and calendar message. The Clock Source (LXT) of RTC is from an external 32.768 kHz crystal connected at pins X32I and X32O (reference to pin Description) or from an external 32.768 kHz oscillator output fed at pin X32I. The RTC unit provides the time message (second, minute, hour) in Time Loading Register (TLR) as well as calendar message (day, month, year) in Calendar Loading Register (CLR). The data message is expressed in BCD format. This unit offers alarm function that user can preset the alarm time in Time Alarm Register (TAR) and alarm calendar in Calendar Alarm Register (CAR).

The RTC unit supports periodic Time Tick and Alarm Match interrupts. The periodic interrupt has 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second which are selected by TTR (RTC_TTR[2:0]). When RTC counter in TLR and CLR is equal to alarm setting time registers TAR and CAR, the alarm interrupt status (AIS (RTC_RIIR[0])) is set and the alarm interrupt is requested if the alarm interrupt is enabled (AIER (RTC_RIER[0])=1). The RTC Time Tick (if wake-up CPU function is enabled, (TWKE (RTC_TTR[3]) high) and Alarm Match can cause CPU wake-up from idle or Power-down mode.

6.13.2 Features

- One time counter (second, minute, hour) and calendar counter (day, month, year) for user to check the time
- Alarm register (second, minute, hour, day, month, year)
- 12-hour or 24-hour mode is selectable
- Leap year compensation automatically
- Day of week counter
- Frequency compensate register (FCR)
- All time and calendar message is expressed in BCD code
- Supports periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
- Supports 1, 2, 4, 8 and 16 seconds clock output (CLK_Hz) for frequency measuring
- Supports RTC Time Tick and Alarm Match interrupt
- Supports wake-up CPU from Power-down mode
- Supports 80 bytes spare registers and a snoop pin to clear the content of these spare registers

6.14 UART Controller

6.14.1 Overview

The UART Controller provides up to two channels of Universal Asynchronous Receiver/Transmitter (UART) modules and performs Normal Speed UART, and supports flow control function. The Universal Asynchronous Receiver/Transmitter (UART) performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU.

The UART controller also supports IrDA (SIR), LIN Master/Slave and RS-485 function modes.

There are four conditions to wake-up the system and it also supports PWM channel source selection to modulate the PWM and the UART transmitter.

6.14.2 Features

- Full duplex, asynchronous communications.
- Separate receiving / transmitting 16 bytes entry FIFO for data payloads.
- Supports hardware auto-flow control/flow control function (CTSn, RTSn) and programmable (CTSn, RTSn) flow control trigger level.
- Supports programmable baud rate generator.
- Supports auto-baud rate detect and baud rate compensation function.
- Supports programmable receiver buffer trigger level.
- Supports incoming data or CTSn or received FIFO is equal to the RFITL or RS-485 AAD mode address matched to wake-up function.
- Supports 9 bit receiver buffer time-out detection function.
- All UART Controller can be served by the PDMA.
- Programmable transmitting data delay time between the last stop bit leaving the TX-FIFO and the de-assertion by setting DLY (UART_TMCTL[23:16]) register.
- Supports IrDA SIR function mode
- Supports LIN function mode.
- Supports RS-485 function mode.
- Supports PWM modulation

6.15 Smart Card Host Interface (SC)

6.15.1 Overview

The Smart Card Interface controller (SC controller) is based on ISO/IEC 7816-3 standard and fully compliant with PC/SC Specifications. It also provides status of card insertion/removal.

6.15.2 Features

- ISO-7816-3 T = 0, T = 1 compliant.
- EMV2000 compliant
- Up to two ISO-7816-3 ports
- Separates receive/transmit 4 byte entry FIFO for data payloads.
- Programmable transmission clock frequency.
- Programmable receiver buffer trigger level.
- Programmable guard time selection (11 ETU ~ 267 ETU).
- A 24-bit and two 8 bit timers for Answer to Request (ATR) and waiting times processing.
- Supports auto inverse convention function.
- Supports transmitter and receiver error retry and error number limitation function.
- Supports hardware activation sequence process.
- Supports hardware warm reset sequence process.
- Supports hardware deactivation sequence process.
- Supports hardware auto deactivation sequence when detected the card removal.
- Supports UART mode
  - Full duplex, asynchronous communications.
  - Separates receiving / transmitting 4 bytes entry FIFO for data payloads.
  - Supports programmable baud rate generator for each channel.
  - Supports programmable receiver buffer trigger level.
  - Programmable transmitting data delay time between the last stop bit leaving the TX-FIFO and the de-assertion by setting SC_EGTR register.
  - Programmable even, odd or no parity bit generation and detection.
  - Programmable stop bit, 1 or 2 stop bit generation

6.16 I²C

6.16.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously. Serial, 8-bit oriented bi-directional data transfers can be made up to 1 Mbps.

Data is transferred between a Master and a Slave synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8-bit long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte.

A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL.

The controller's on-chip I²C logic provides the serial interface that meets the I²C bus standard mode specification. The I²C controller handles byte transfers autonomously. Pull up resistor is needed for I²C operation as these are open drain pins.

The I²C controller is equipped with two slave address registers. The contents of the registers are irrelevant when I²C is in Master mode. In the Slave mode, the seven most significant bits must be loaded with the user's own slave address. The I²C hardware will react if the contents of I2CADDR are matched with the received slave address.

This controller supports the "General Call (GC)" function. If the GCALL (I2CSADDR[0]) bit is set this controller will respond to General Call address (00H). Clear GC bit to disable general call function. When GCALL bit is set and the I²C is in Slave mode, it can receive the general call address which is equal to 00H after master sends general call address to the I²C bus, then it will follow status of GC mode. If it is in Master mode, the ACK bit must be cleared when it sends general call address of 00H to the I²C bus.

The I²C-bus controller supports multiple address recognition with two address mask register. When the bit in the address mask register is set to one, it means the received corresponding address bit is don't-care. If the bit is set to 0, that means the received corresponding register bit should be exact the same as address register.

6.16.2 Features

- Supports two I2C channels and both of them can acts as Master or Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- One built-in 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflows.
- Programmable clock divider allows versatile rate control
- Supports 7-bit addressing mode

- Supports multiple address recognition (Two slave addresses with mask option)
- Supports Power-down wake-up function
- Supports two-Level FIFO

6.17 SPI

6.17.1 Overview

The Serial Peripheral Interface (SPI) is a synchronous serial data communication protocol. Devices communicate in Master/Slave mode with 4-wire bi-direction interface. It is used to perform a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. The SPI controller can be configured as a master or a slave device.

The SPI controller supports wake-up function. When this chip stays in Power-down mode, it can be waked up by off-chip device.

This controller supports variable serial clock function for special application and 2-bit transfer mode to connect 2 off-chip slave devices. The SPI controller also supports PDMA function to access the data buffer.

6.17.2 Features

- Up to two sets of SPI controllers
- Supports Master (max. 32 MHz) or Slave (max. 16 MHz) mode operation
- Supports 1 bit and 2 bit transfer mode
- Support Dual IO transfer mode
- Configurable bit length of a transaction from 8 to 32-bit
- Supports MSB first or LSB first transfer sequence
- Two slave select lines supported in Master mode
- Configurable byte or word suspend mode
- Supports byte re-ordering function
- Supports variable serial clock in Master mode
- Provide separate 8-level depth transmit and receive FIFO buffer
- Supports wake-up function
- Supports PDMA transfer
- Supports 3-wires, no slave select signal, bi-direction interface

6.18 LCD Display Driver

6.18.1 Overview

The LCD driver can directly drive a LCD glass by creating the ac segment and common voltage signals automatically. It can support static, 1/2 duty, 1/3 duty, 1/4 duty, 1/5 duty and 1/6 duty LCD glass with up to 3 segments with 6 COM (segment 0 is used as LCD_COM4 and segment 1 is used as LCD_COM5) or 36 segments with 4 COM (LCD_COM0 ~ LCD_COM3).

A built-in charge pump function can be enabled to provide the LCD glass with higher voltage than the system voltage. The LCD driver would generate voltage higher than the threshold voltage in older to darken a segment and a voltage lower than threshold to make a segment clear. However, the LCD display segment will degrade if the applied voltage has a DC-component. To avoid this, the generated waveform by LCD driver are arranged such that average voltage of each segment is 0 and the RMS(root-mean-square) voltage applied on a LCD segment lower than the segment threshold making LCD clear and RMS voltage higher than the segment threshold making LCD dark.

6.18.2 Features

- Supports Segment/Com:
  - 108 dots (6x18) or 80 dots (4x20) in LQFP48 package
  - 108 dots (6x18) or 80 dots (4x20) or 132 dots (6x 22) or 96 dots (4x24) or 180 dots (6x30) or 128 dots (4x32) in LQFP64 package
  - 204 dots (6x34) or 144 dots (4x36) in LQFP100 package
- Common 0-5 multiplexing functions with GPI/O pins
- Segment 0-35 multiplexing function with GPI/O pins
- Supports Static,1/2 bias and 1/3 bias voltage
- Six display modes: Static,1/2 duty, 1/3 duty, 1/4 duty, 1/5 duty or 1/6 duty Selectable LCD frequency by frequency divider
- Configurable frame frequency
- Internal Charge pump, adjustable contrast adjustment
- Embedded LCD bias reference ladder (R-Type, 200/300/400 kΩ resisters)
- Configurable Charge pump frequency
- Blinking capability
- Supports R/C/Ext_C-type method
- LCD frame interrupt

6.19 Analog to Digital Converter (ADC)

6.19.1 Overview

The Nano112 series contains one 12-bit successive approximation analog-to-digital converter (SAR A/D converter) with 8 external input channels and 4 internal channels. The A/D converter supports three operation modes: Single, Single-cycle Scan and Continuous Scan mode, and can be started by software, external STADC(PA.11) pin, timer event start and PWM trigger.

Note that the I/O pins used as ADC analog input pins must configure the Pin Function (PA_L_MFP) to ADC input and off digital function (GPIOA_OFFD) should be turned on before ADC function is enabled.

6.19.2 Features

- Analog input voltage range: 0~V_{REF} (Max to AV_{DD})
- Selectable 12-bits, 10-bits, 8-bits and 6-bits resolution
- Supports sampling time settings for channel 0~7 individually (ADCCHSAMP0 register) and channel 14~17 share the same one sampling time setting (ADCCHSAMP1 register)
- Supports two power-down modes:
  - Power-down mode
  - Standby mode
- Up to 8 external analog input channels (channel0 ~ channel7), and 4 internal channels (channel14~channel17) converting four voltage sources (internal band-gap voltage, internal temperature sensor output, AV_{DD}, and AV_{SS}).
- Maximum ADC clock frequency is 32 MHz and each conversion is 19 clocks+ sampling time depending on the input resistance (Rin).
- Three operating modes:
  - Single mode: A/D conversion is performed one time on a specified channel.
  - Single-cycle Scan mode: A/D conversion is performed one cycle on all specified channels with the sequence from the lowest numbered channel to the highest numbered channel.
  - Continuous Scan mode: A/D converter continuously performs Single-cycle scan mode until software stops A/D conversion.
- An A/D conversion can be started by:
  - Software write 1 to ADST bit
  - External pin STADC
  - PWM trigger
  - Selects one from four timer events (TMR0, TMR1, TMR2 and TMR3) that enable ADC and transfer AD results by PDMA
- Conversion results held in data registers for each channel
- Supports digital comparator: Conversion result can be compared with a specified value and user can select whether to generate an interrupt when conversion result is equal to the compare register setting.
- Supports Calibration and load Calibration words capability.

6.20 Analog Comparator Controller (ACMP)

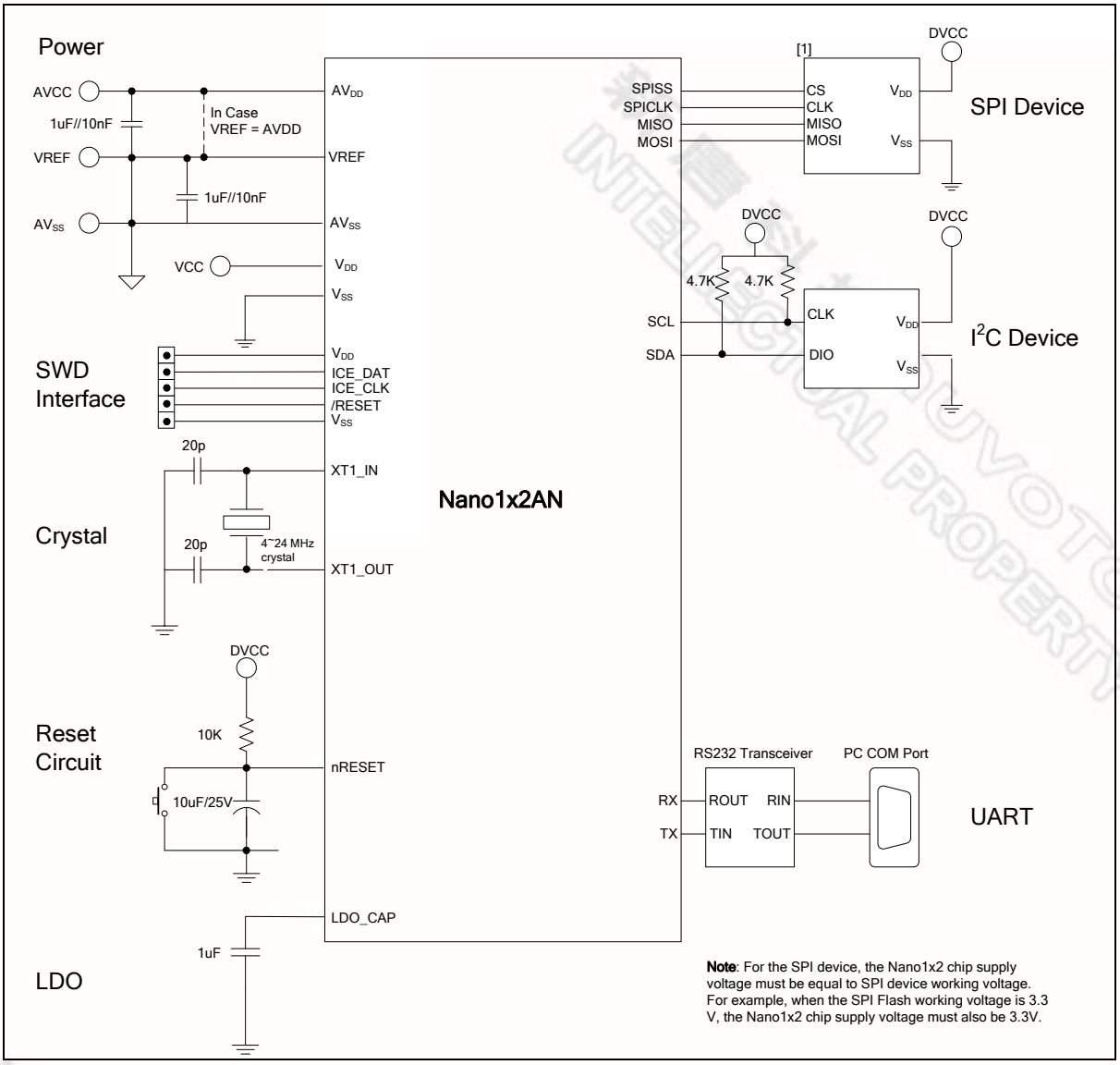
6.20.1 Overview

The Nano112 series contains two comparators. The comparator output is logic 1 when positive input is greater than negative input; otherwise, the output is 0. Each comparator can be configured to generate an interrupt when the comparator output value changes. The comparator ACMP0 can be used as normal comparator or it can emulate ADC function. The comparator ACMP1 can be used as normal comparator only.

6.20.2 Features

- Analog input voltage range: 0 ~ AV_{DD}
- Supports hysteresis function
- Supports wake-up function
- Comparator ACMP0 supports
  - 4 positive sources(ACMP0_Px)
    - PA.1, PA.2, PA.3, or PA.4
  - 4 negative sources
    - PA.5 (ACMP0_N)
    - Comparator Reference Voltage (CRV)
    - Int_V_{REF}
    - AGND
- Comparator ACMP1 supports
  - 1 positive source
    - PA.12(ACMP1_P)
  - 4 negative sources
    - PA.13(ACMP1_N)
    - Comparator Reference Voltage (CRV)
    - Int_V_{REF}
    - AGND
- Comparator ACMP0 supports three operation modes:
  - Normal Comparator mode
  - Single Slope ADC mode: Resistance measurement (e.g. PTC, NTC, PT1000)
    - Supports to measure 7 channels resistor
  - Sigma-Delta ADC mode
    - Supports up to 4 channel voltage input from ACMP0_Px

7 APPLICATION CIRCUIT



8 POWER COMSUMPTION

Part No	Test Condition		VDD	CPU clock	Current
Nano102/112 series	Operating Mode: CPU run while(1) in FLASH ROM Clock = 12MHz Crystal Oscillator Disable all peripheral Set LDO output = 1.6V		3.3V	12 MHz	1.89mA 157uA/MHz
	Idle Mode: CPU stop Clock = 12MHz Crystal Oscillator Disable all peripheral Set LDO output = 1.6V		3.3V	12 MHz	800uA 67uA/MHz
	Operating Mode: CPU run while(1) in FLASH ROM Clock = 12MHz Internal RC Oscillator Disable all peripheral Set LDO output = 1.6V		3.3V	12 MHz	1.65mA 137uA/MHz
	Idle Mode: CPU stop Clock = 12MHz Internal RC Oscillator Disable all peripheral Set LDO output = 1.6V		3.3V	12 MHz	560uA 46uA/MHz
	RTC + LCD Mode: (RAM retention) (Power down with LXT and LCD enable) CPU stop Clock = 32.768KHz Crystal Oscillator Disable all peripheral except RTC and LCD circuit. Without panel loading Set LDO output = 1.6V Only for Nano112 LCD series	InternL C-Type (With internal Charge pump)	3.3V	Stop	9.5uA
		InternL R-Type (With internal resistor ladder) 200kΩ			8.3uA
		InternL R-Type (With internal resistor ladder) 300kΩ			6.4uA
		InternL R-Type (With internal resistor ladder) 400kΩ			5.5uA
		External C-Type (With 0.1uF cap. ladder)			2.5uA
		External R-type (With 1MΩ resister ladder)			3.7uA
	RTC Mode: (RAM retention) (Power down with LXT enable) CPU stop Clock = 32.768KHz Crystal Oscillator Disable all peripheral except RTC circuit Set LDO output = 1.6V		3.3V	Stop	1.5uA
	Power Down Mode: (RAM retention) CPU and all clocks stop Set LDO output = 1.6V		3.3V	Stop	0.65uA
	Wake-Up time from Power Down Mode Clock = Internal 12 MHz RC Oscillator (from wake-up event to first CPU core valid clock)		3.3V	12 MHz	6us
	Wake-Up time from Power Down Mode Clock = Internal 12 MHz RC Oscillator (from interrupt event to interrupt service routine first instruction)		3.3V	12 MHz	7us

9 ELECTRICAL CHARACTERISTIC

9.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
DC Power Supply	V_{DD}-V_{SS}	-0.3	+3.6	V
Input Voltage on 5V Tolerance Pin	V_{IN}	V_{SS} -0.3	5.5	V
Input Voltage on Any Other Pin without 5V Tolerance Pin	VI_N	V_{SS} -0.3	V_{DD} +0.3	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	T_A	-40	+85	°C
Storage Temperature	T_{ST}	-55	+150	°C
Maximum Current into VDD		-	150	mA
Maximum Current out of VSS		-	150	mA
Maximum Current sunk by a I/O Pin		-	25	mA
Maximum Current Sourced by a I/O Pin		-	25	mA
Maximum Current Sunk by Total I/O Pins		-	100	mA
Maximum Current Sourced by Total I/O Pins		-	100	mA

9.2 Nano102/Nano112 DC Electrical Characteristics

(VDD-VSS=3.3V, TA = 25°C, FOSC = 32 MHz unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operation voltage	V_{DD}	1.8	-	3.6	V	V_{DD} =1.8V up to 32 MHz
Power Ground	V_{SS} AV_{SS}	-0.3	-		V	
LDO Output Voltage	V_{LDO1}	1.62	1.8	1.98	V	MCU operating in Run or Idle mode
		1.44	1.6	1.76	V	Set LDO_LEVEL(LDO_CTL[3:2]) = 0x1
	V_{LDO2}	1.49	1.66	1.83	V	MCU operating in Power-down mode
	C_{LDO}		1		uF	Connect to LDO_CAP pin
Analog Operating Voltage	AV_{DD}		V_{DD}		V	
Operating Current Normal Run Mode HCLK =32 MHz wkhile(1){}executed from flash V_{LDO1}=1.8 V	I_{DD5}		11.7		mA	V_{DD}: 3.3 V; HXT: 12 MHz; HIRC: X; PLL: V; All digital module: V
	I_{DD6}		5.8		mA	3.3 V; 12 MHz; X; V; X
	I_{DD7}		10.9		mA	1.8 V; 12 MHz; X; V; V
	I_{DD8}		5.6		mA	1.8 V; 12 MHz; X; V; X
Operating Current Normal Run Mode HCLK =32 MHz while(1){}executed from flash V_{LDO1}=1.6 V	I_{DD9}		3.9		mA	3.3 V; 12 MHz; X; X; V
	I_{DD10}		1.9		mA	3.3 V; 12 MHz; X; X; X
	I_{DD11}		3.8		mA	1.8 V; 12 MHz; X; X; V
	I_{DD12}		1.9		mA	1.8 V; 12 MHz; ; ;

Operating Current Normal Run Mode HCLK =16 MHz while(1){}executed from flash V_{LDO1}=1.6 V	I_{DD131}		5.8		mA	3.3 V	X	16 MHz	X	V
	I_{DD141}		2.3		mA	3.3 V	X	16 MHz	X	X
	I_{DD151}		5.7		mA	1.8 V	X	16 MHz	X	V
	I_{DD161}		2.3		mA	1.8 V	X	16 MHz	X	X
Operating Current Normal Run Mode HCLK =12 MHz while(1){}executed from flash V_{LDO1}=1.6 V	I_{DD132}		4.0		mA	3.3 V	X	12 MHz	X	V
	I_{DD142}		1.7		mA	3.3 V	X	12 MHz	X	X
	I_{DD152}		4.0		mA	1.8 V	X	12 MHz	X	V
	I_{DD162}		1.7		mA	1.8 V	X	12 MHz	X	X
Operating Current Normal Run Mode HCLK =12 MHz while(1){}executed from flash V_{LDO1}=1.6 V	I_{DD13}		3.8		mA	3.3 V	12 MHz	X	X	V
	I_{DD14}		1.9		mA	3.3 V	12 MHz	X	X	X
	I_{DD15}		3.8		mA	1.8 V	12 MHz	X	X	V
	I_{DD16}		1.9		mA	1.8 V	12 MHz	X	X	X
Operating Current Normal Run Mode xHCLK =4 MHz while(1){}executed from flash V_{LDO1}=1.6 V	I_{DD17}		1.3		mA	3.3 V	4 MHz	X	X	V
	I_{DD18}		0.7		mA	3.3 V	4 MHz	X	X	X
	I_{DD19}		1.3		mA	1.8 V	4 MHz	X	X	V
	I_{DD20}		0.7		mA	1.8 V	4 MHz	X	X	X
Operating Current Normal Run Mode HCLK =32.768 kHz wkhile(1){}executed from flash V_{LDO1}=1.6 V	I_{DD21}		99		uA	V_{DD}	LXT (kHz)	HIRC	PLL	All digital module
						3.3 V	32.768	X	X	V
	I_{DD22}		93		uA	3.3 V	32.768	X	X	X
	I_{DD23}		95		uA	1.8 V	32.768	X	X	V
	I_{DD24}		89		uA	1.8 V	32.768	X	X	X
Operating Current kNormal Run Mode HCLK =32 kHz wkhile(1){}executed from flash V_{LDO1}=1.6 V	I_{DD25}		91		uA	V_{DD}	HXT/LXT	LIRC (kHz)	PLL	All digital module
						3.3 V	X	10	X	V
	I_{DD26}		90		uA	3.3 V	X	10	X	X
	I_{DD27}		87		uA	1.8 V	X	10	X	V
	I_{DD28}		85		uA	1.8 V	X	10	X	X
Operating Current Idle Mode HCLK =32 MHz V_{LDO1}=1.8 V	I_{IDLE5}		8.4		mA	V_{DD}	HXT	HIRC	PLL	All digital module
						3.3 V	12 MHz	X	V	V
	I_{IDLE6}		2.6		mA	3.3 V	12 MHz	X	V	X
	I_{IDLE7}		8.0		mA	1.8 V	12 MHz	X	V	V
	I_{IDLE8}		2.5		mA	1.8 V	12 MHz	X	V	X

Operating Current Idle Mode HCLK =12 MHz V_{LDO1}=1.6 V	I_{IDLE9}		2.8		mA	3.3 V	12 MHz	X	X	V
	I_{IDLE10}		0.8		mA	3.3 V	12 MHz	X	X	X
	I_{IDLE11}		2.8		mA	1.8 V	12 MHz	X	X	V
	I_{IDLE12}		0.8		mA	1.8 V	12 MHz	X	X	X

Operating Current Idle Mode HCLK =16 MHz V_{LDO1}=1.6 V	$I_{IDLE131}$		4.2		mA	3.3 V	X	16 MHz	X	V
	$I_{IDLE141}$		0.7		mA	3.3 V	X	16 MHz	X	X
	$I_{IDLE151}$		4.1		mA	1.8 V	X	16 MHz	X	V
	$I_{IDLE161}$		0.7		mA	1.8 V	X	16 MHz	X	X
Operating Current Idle Mode HCLK =12 MHz V_{LDO1}=1.6 V	$I_{IDLE132}$		2.9		mA	3.3 V	X	12 MHz	X	V
	$I_{IDLE142}$		0.6		mA	3.3 V	X	12 MHz	X	X
	$I_{IDLE152}$		2.9		mA	1.8 V	X	12 MHz	X	V
	$I_{IDLE162}$		0.6		mA	1.8 V	X	12 MHz	X	X
Operating Current Idle Mode HCLK =12 MHz V_{LDO1}=1.6 V	I_{IDLE13}		2.8		mA	3.3 V	12 MHz	X	X	V
	I_{IDLE14}		0.8		mA	3.3 V	12 MHz	X	X	X
	I_{IDLE15}		2.8		mA	1.8 V	12 MHz	X	X	V
	I_{IDLE16}		0.8		mA	1.8 V	12 MHz	X	X	X
Operating Current Idle Mode HCLK =4 MHz V_{LDO1}=1.6 V	I_{IDLE17}		1.0		mA	3.3 V	4 MHz	X	X	V
	I_{IDLE18}		0.3		mA	3.3 V	4 MHz	X	X	X
	I_{IDLE19}		1.0		mA	1.8 V	4 MHz	X	X	V
	I_{IDLE20}		0.3		mA	1.8 V	4 MHz	X	X	X
Operating Current Idle Mode HCLK =32.768 kHz V_{LDO1}=1.6 V	I_{IDLE21}		96		uA	V_{DD}	LXT (kHz)	HIRC	PLL	All digital module
						3.3 V	32.768	X	X	V
	I_{IDLE22}		90		uA	3.3 V	32.768	X	X	X
	I_{IDLE23}		92		uA	1.8 V	32.768	X	X	V
	I_{IDLE24}		86		uA	1.8 V	32.768	X	X	X
Operating Current Idle Mode HCLK =10 kHz V_{LDO1}=1.6 V	I_{IDLE25}		90		uA	V_{DD}	HXT/LXT	LIRC (kHz)	PLL	All digital module
						3.3 V	X	10	X	V
	I_{IDLE26}		89		uA	3.3 V	X	10	X	X
	I_{IDLE27}		86		uA	1.8 V	X	10	X	V
	I_{IDLE28}		84		uA	1.8 V	X	10	X	X
Standby Current Power-down Mode V_{LDO1}=1.6 V	I_{PWD1}		0.65		uA	V_{DD}	HXT/HIRC PLL	LXT (kHz)	RTC	RAM retension
						3.3 V	X	X	X	V
	I_{PWD2}		0.65		uA	1.8 V	X	X	X	V
	I_{PWD3}		1.5		uA	3.3 V	X	32.768	V	V
	I_{PWD4}		1.5		uA	1.8 V	X	32.768	V	V

Input Pull Up Resistor PA, PB, PC, PD, PE, PF	R_{IN}		43		KΩ	V_{DD} = 3.3V
			108		KΩ	V_{DD} = 1.8V
Input Leakage Current PA, PB, PC, PD, PE, PF	I_{LK}	-0.1	-	+0.1	μA	V_{DD} = 3.3V, 0<V_{IN}<V_{DD}
Input Low Voltage PA, PB, PC, PD, PE, PF (Schmitt input)	V_{IL1}		-	0.4V_{DD}	V	
Input High Voltage PA, PB, PC, PD, PE, PF (Schmitt input)	V_{IH1}	0.6V_{DD}		5.5	V	ADC and DAC shared pins without Input 5V tolerance.
Hysteresis voltage of PA~PF (Schmitt input)	V_{HY}		0.2V_{DD}		V	
Input Low Voltage XT1[*2]	V_{IL2}	0	-	0.4		V_{DD} = 3.3V
Input High Voltage XT1[*2]	V_{IH2}	1.5	-	V_{DD} +0.2	V	V_{DD} = 3.3V
Input Low Voltage X32I[*2]	V_{IL4}	0	-	0.3	V	
Input High Voltage X32I[*2]	V_{IH4}	1.5	-	1.98	V	
Negative going threshold (Schmitt input), /RESET	V_{ILS}	1.03	1.08	1.13	V	V_{DD} = 3.3V
Positive going threshold (SchmittIput), /RESET	V_{IHS}	1.75	2.01	2.25	V	V_{DD} = 3.3V
Source Current PA, PB, PC, PD, PE, PF (Push-pull Mode)	I_{SR21}	-10	-14	-	mA	V_{DD} = 3.3V, V_S = Vdd-0.7V
	I_{SR22}	-3	-5	-	mA	V_{DD} = 1.8V, V_S = Vdd-0.45V
Sink Current PA, PB, PC, PD, PE, PF (Push-pull Mode)	I_{SK21}	10	15	-	mA	V_{DD} = 3.3V, V_S = 0.7V
	I_{SK22}	3	6	-	mA	V_{DD} = 1.8V, V_S = 0.45V

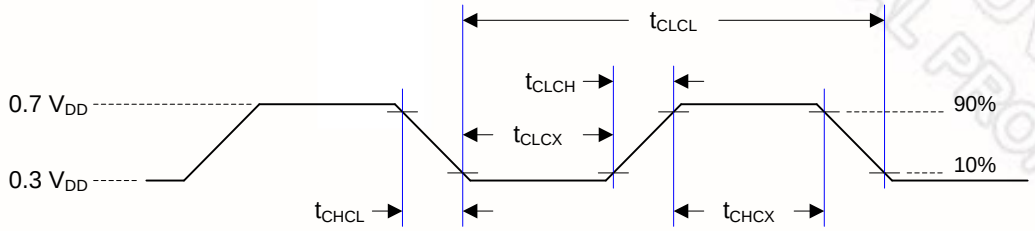
Note:

1. /RESET pin is a Schmitt trigger input.
2. Crystal Input is a CMOS input.
3. It is recommended that a 10uF or higher capacitor and a 100nF bypass capacitor are connected between VDD and the closest VSS pin of the device.
4. For ensuring power stability, a 1uF or higher capacitor must be connected between LDO pin and the closest VSS pin of the device. Also a 100nF bypass capacitor between LDO and VSS help suppressing output noise.
5. All peripherals' clock source is from HXT (12 MHz), except SPI from HCLK.

9.3 AC Electrical Characteristics

9.3.1 External Input Clock

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Clock High Time	t_{CHCX}	10	-		nS	
Clock Low Time	t_{CLCX}	10	-		nS	
Clock Rise Time	t_{CLCH}	2	-	15	nS	
Clock Fall Time	t_{CHCL}	2	-	15	nS	



Note: Duty cycle is 50%.

9.3.2 External 4~24 MHz XTAL Oscillator

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Oscillator frequency	f_{HXT}	4	12	24	MHz	VDD = 1.8V ~ 3.6V
Temperature	T_{HXT}	-40	-	+85	°C	
Operating current	I_{HXT}		0.3		mA	VDD = 3.0V

9.3.2.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R1
4MHz ~ 24 MHz	20pF	20pF	without

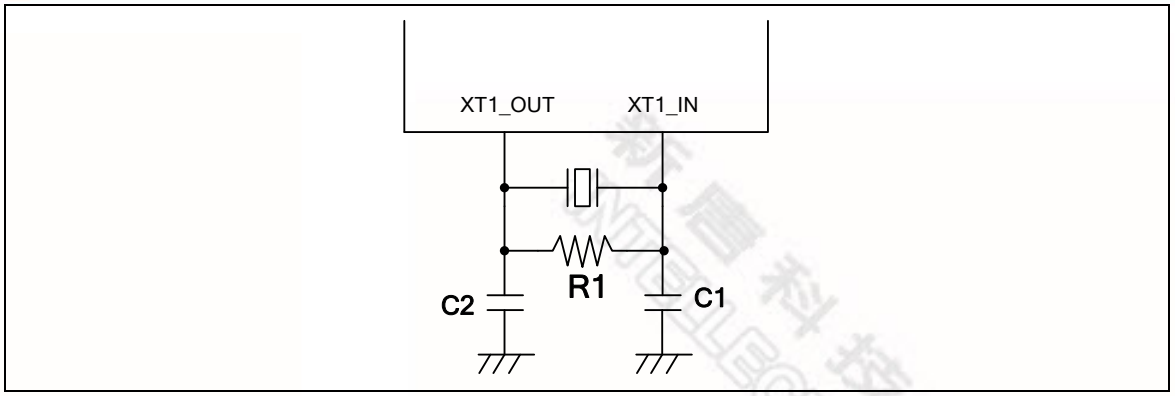


Figure 9-1 Typical Crystal Application Circuit

9.3.3 External 32.768 kHz Crystal

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Oscillator frequency	f_{LXT}		32.768		kHz	VDD = 1.8V ~ 3.6V
Temperature	T_{LXT}	-40	-	+85	°C	
Operating current	I_{LXT}		1		μA	VDD = 3.0V

9.3.3.1 Typical Crystal Application Circuits

CRYSTAL	C3	C4	R2
32.768 kHz	20pF	20pF	without

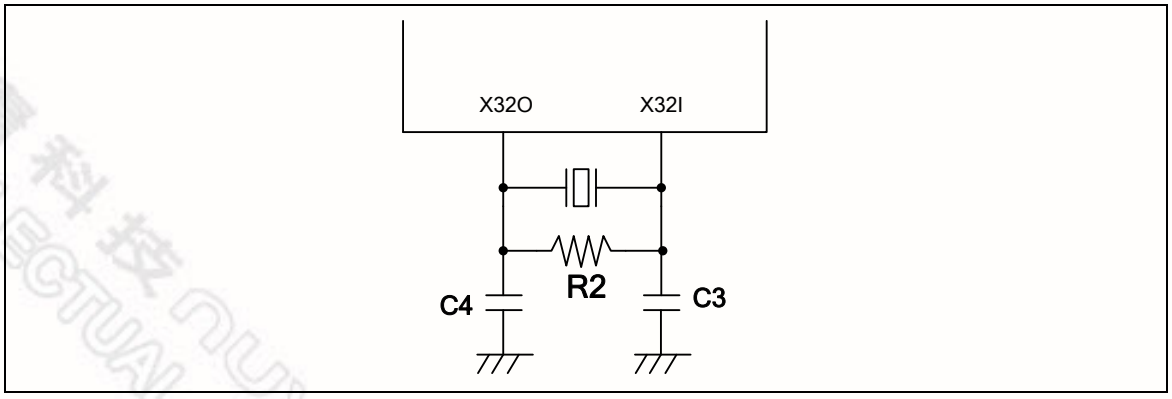


Figure 9-2 Typical Crystal Application Circuit

9.3.4 Internal 12 MHz Oscillator

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Supply voltage[1]	V_{HRC}		1.8		V	
Calibrated Internal Oscillator Frequency	F_{HRC}	11.88	12	12.12	MHz	25°C, VDD = 3.3V
		11.76	12	12.24	MHz	-40°C ~ +85°C, VDD = 1.8V~3.6V
		11.88	12	12.12	MHz	-40°C ~ +85 °C, VDD = 1.8V~3.6V Enable 32.768K crystal oscillator and set TRIM_SEL[1:0]=”10”
Operating current	I_{HRC}		250		μA	

Note: Internal oscillator operation voltage comes from LDO.

9.3.5 Internal 10 kHz Oscillator

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Supply voltage[1]	V_{LRC}		1.8		V	
Center Frequency	F_{LRC}	7	10	13	kHz	25°C, VDD = 3V
		5	10	15	kHz	-40°C ~+85 °C, VDD = 1.8V~3.6V
Operating current	I_{LRC}		0.3		μA	VDD = 3V

Note: Internal oscillator operation voltage comes from LDO.

9.4 Analog Characteristics

9.4.1 12-bit ADC

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Operating voltage	AV_{DD}	1.8		3.6	V	$AV_{DD} = V_{DD}$
Operating current (AV_{DD} current) (Enable ADC and disable all	I_{ADC32}		120		μA	$AV_{DD} = V_{DD}$ = 3.0V ADC_VREF = AV_{DD} ADC Clock Rate = 32 MHz

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
other analog modules)	I_{ADC2}		30		μA	AV_{DD} = V_{DD} = 3.0V ADC_VREF = AV_{DD} ADC Clock Rate = 2 MHz
Resolution	R_{ADC}			12	Bit	
Reference voltage	V_{REF}	1.8		A_{VDD}	V	
Reference input current (Avg.)	I_{REF}			1	μA	
ADC input voltage	V_{IN}	0		V_{REF}	V	
Conversion time	T_{CONV}	1			μS	
Conversion Rate	F_{SPS}			1.5M	Hz	V_{DD} = 3V
Integral Non-Linearity Error	INL		±1		LSB	V_{REF} is external Vref pin
Differential Non-Linearity	DNL		±0.8		LSB	V_{REF} is external Vref pin
Gain error	E_G		±2		LSB	V_{REF} is external Vref pin
Offset error	E_{OFFSET}		±1.5		LSB	V_{REF} is external Vref pin
Absolute error	E_{ABS}		-	±6	LSB	V_{REF} is external Vref pin
ADC Clock frequency	F_{ADC}	0.25		32	MHz	
Clock cycle	AD_{CYC}	20			Cycle	
Internal Capacitance	C_{IN}	-	5	-	pF	
Monotonic	-	Guaranteed			-	

9.4.2 Brown-out Detector

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
AV_{DD}	Supply Voltage	0	-	3.6	V	-
T_A	Temperature	-40	25	85	℃	-
I_{BOD}	Quiescent Current	-	1		μA	AV_{DD} = 3V
V_{BOD}	Brown-out Voltage 25℃	2.4	2.5	2.6	V	BODCTL[2] = 1
		1.9	2.0	2.1	V	BODCTL[1] = 1
		1.6	1.7	1.8	V	BODCTL[0] = 1

9.4.3 Power-on Reset

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	25	85	℃	-
V_{POR}	Reset Voltage		1.6		V	-

9.4.4 Temperature Sensor

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION (supply voltage = 3V)
		MIN.	TYP.	MAX.	UNIT	
Detection Temperature	T_{DET}	-40		+85	^oC	
Operating current	I_{TEMP}	-	5	-	μA	
Gain	V_{TG}	-1.76	-1.68	-1.60	mV/^oC	
Offset	V_{TO}	735	745	755	mV	Tempeature at 0 ^oC

Note: Internal operation voltage comes form LDO.

9.4.5 LCD

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Operating voltage	V_{DD}	1.8	-	3.6	V	
VLCD voltage	V_{LCD34}	-	3.4	-	V	CPUMP_VOL_SET=111, no loading
VLCD voltage	V_{LCD33}	-	3.3	-	V	CPUMP_VOL_SET=110, no loading
VLCD voltage	V_{LCD32}	-	3.2	-	V	CPUMP_VOL_SET=101, no loading
VLCD voltage	V_{LCD31}	-	3.1	-	V	CPUMP_VOL_SET=100, no loading
VLCD voltage	V_{LCD30}	-	3.0	-	V	CPUMP_VOL_SET=011, no loading
VLCD voltage	V_{LCD29}	-	2.9	-	V	CPUMP_VOL_SET=010, no loading
VLCD voltage	V_{LCD28}	-	2.8	-	V	CPUMP_VOL_SET=001, no loading
VLCD voltage	V_{LCD27}	-	2.7	-	V	CPUMP_VOL_SET=000, no loading
Operating current (Include 32.768 KHz crystal OSC and RTC operating)	I_{LCDint}	-	9.5	-	μA	V_{DD} = 3V, frame rate = 64Hz Without loading (internal C type, with 0.1uF)
	I_{LCDext}	I_{LCDint}	2.5	-	μA	V_{DD} = 3V, frame rate = 64Hz Without loading (external C type with 0.1uF)

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
	$I_{LCDintR}$		8.3		μA	V_{DD} = 3V, frame rate = 64Hz Without loading (internal R type with internal 200KΩ resistor ladder)
			6.4		μA	V_{DD} = 3V, frame rate = 64Hz Without loading (internal R type with internal 300KΩ resistor ladder)
			5.5		μA	V_{DD} = 3V, frame rate = 64Hz Without loading (internal R type with internal 400KΩ resistor ladder)
	$I_{LCDextR}$		3.7		μA	V_{DD} = 3V, frame rate = 64Hz Without loading (external R type with external 1MΩ resistor ladder)

9.4.6 Internal Voltage Reference

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Operating voltage	AV_{DD}	1.8	-	3.6	V	
1.5V voltage reference	V_{REF1}	1.44	1.5	1.56	V	AV_{DD} ≥ 1.8V (-40°C ~85°C)
1.8V voltage reference	V_{REF2}	1.69	1.8	1.87	V	AV_{DD} ≥ 2.0V (-40°C ~85°C)
2.5V voltage reference	V_{REF3}	2.35	2.5	2.60	V	AV_{DD} ≥ 2.8V (-40°C ~85°C)
Stable Time	T_{REFTAB}	-	1	-	ms	
Operating current	I_{VREF}	-	30	-	μA	AV_{DD} = 3V

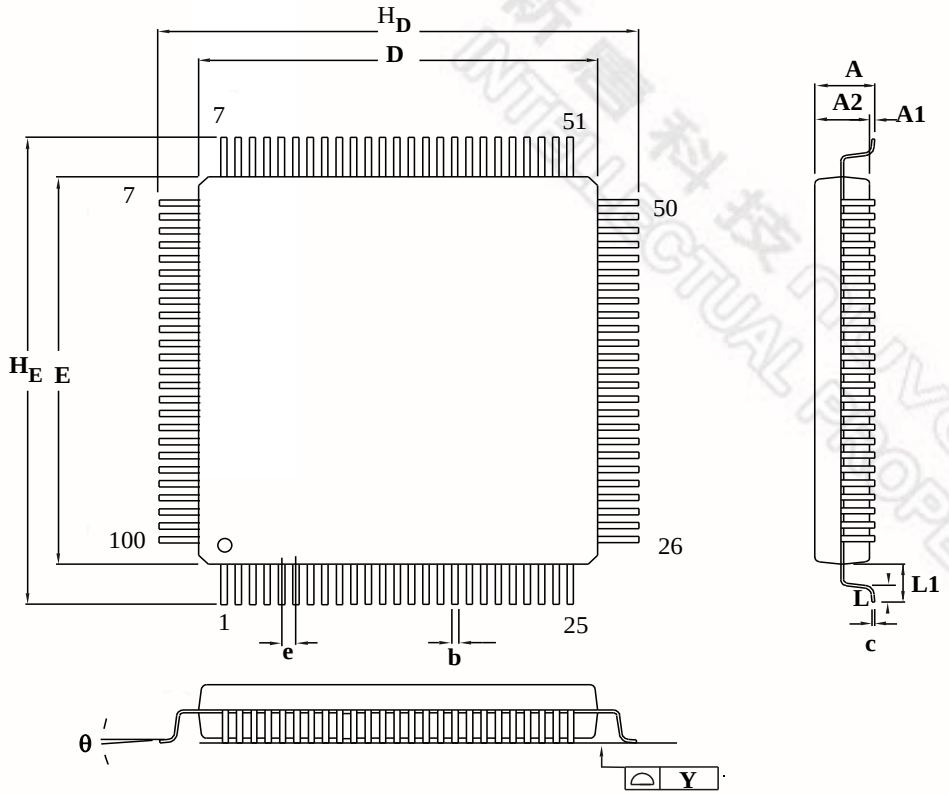
9.4.7 Comparator

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{CMP}	Supply Voltage	1.8		3.6	V	
T_A	Temperature	-40	25	85	℃	-
I_{CMP}	Operation Current	-	40		μA	AV_{DD} = 3 V
V_{OFF}	Input Offset Voltage		10	20	mV	-
V_{SW}	Output Swing	0.1	-	AV_{DD} - 0.1	V	-

V_{COM}	Input Common Mode Range	0.1	-	AV_{DD} – 0.1	V	-
-	DC Gain	40	70	-	dB	-
T_{PGD}	Propagation Delay	-	200	-	ns	V_{DIFF} = 100mV
V_{HYS}	Hysteresis	-	±10	-	mV	
T_{STB}	Stable time	-	-	1	µs	

10 PACKAGE DIMENSIONS

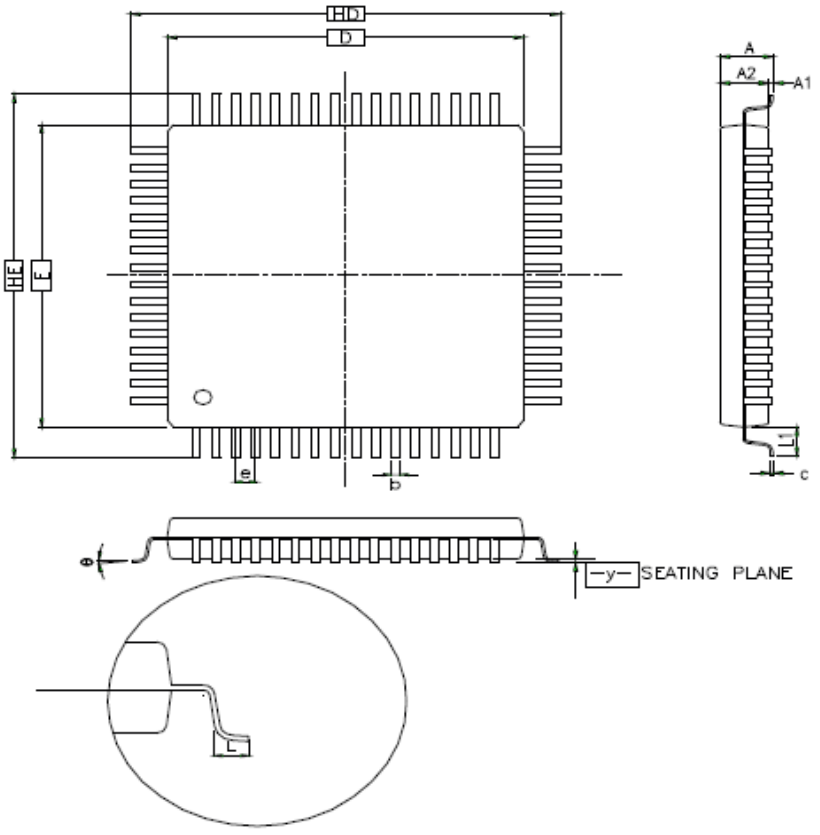
10.1 100L LQFP (14x14x1.4 mm footprint 2.0 mm)



Controlling Dimension : Millimeters

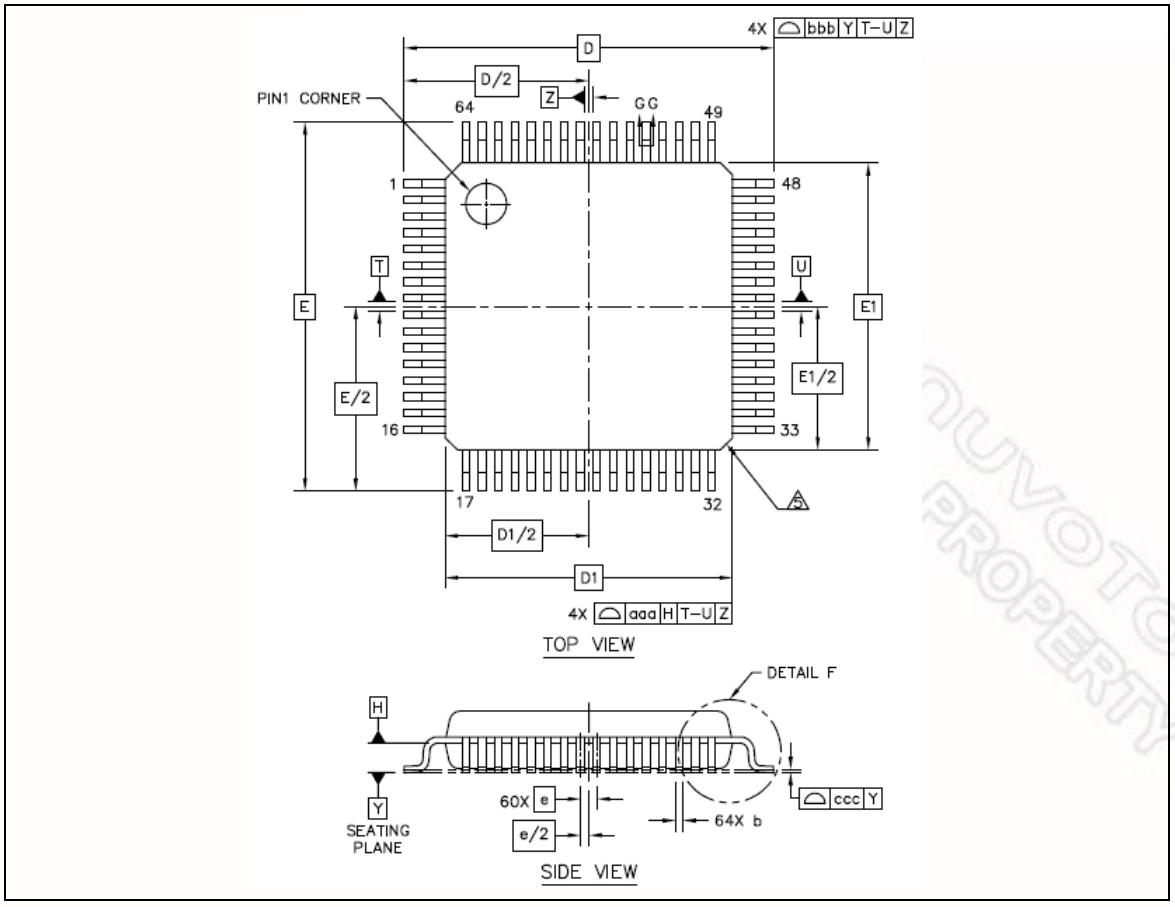
Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A1	0.002	—	—	0.05	—	—
A2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.547	0.551	0.556	13.90	14.00	14.10
E	0.547	0.551	0.556	13.90	14.00	14.10
e	—	0.020	—	—	0.50	—
H_D	0.622	0.630	0.638	15.80	16.00	16.20
H_E	0.622	0.630	0.638	15.80	16.00	16.20
L	0.018	0.024	0.030	0.45	0.60	0.75
L1	—	0.039	—	—	1.00	—
y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

10.2 64R LQFP(10x10x1.4 mm footprint 2.0 mm)

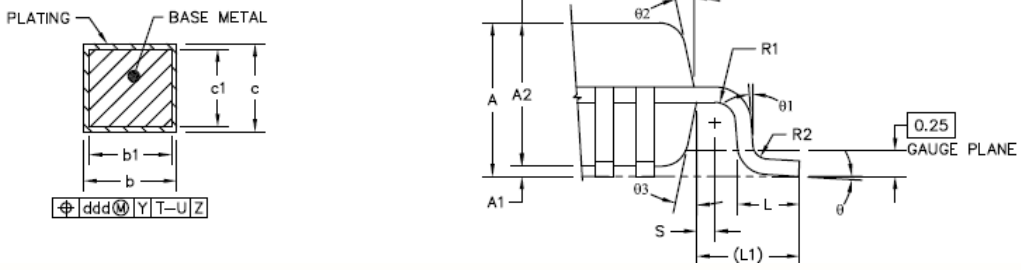


Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A_1	0.002	—	0.006	0.05	—	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.008	0.011	0.17	0.20	0.27
c	0.004	—	0.008	0.09	—	0.20
D	—	0.393	—	—	10.00	—
E	—	0.393	—	—	10.00	—
e	—	0.020	—	—	0.50	—
H_D	—	0.472	—	—	12.00	—
H_E	—	0.472	—	—	12.00	—
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
y	—	0.004	—	—	0.10	—
θ	0°	3.5°	7°	0°	3.5°	7°

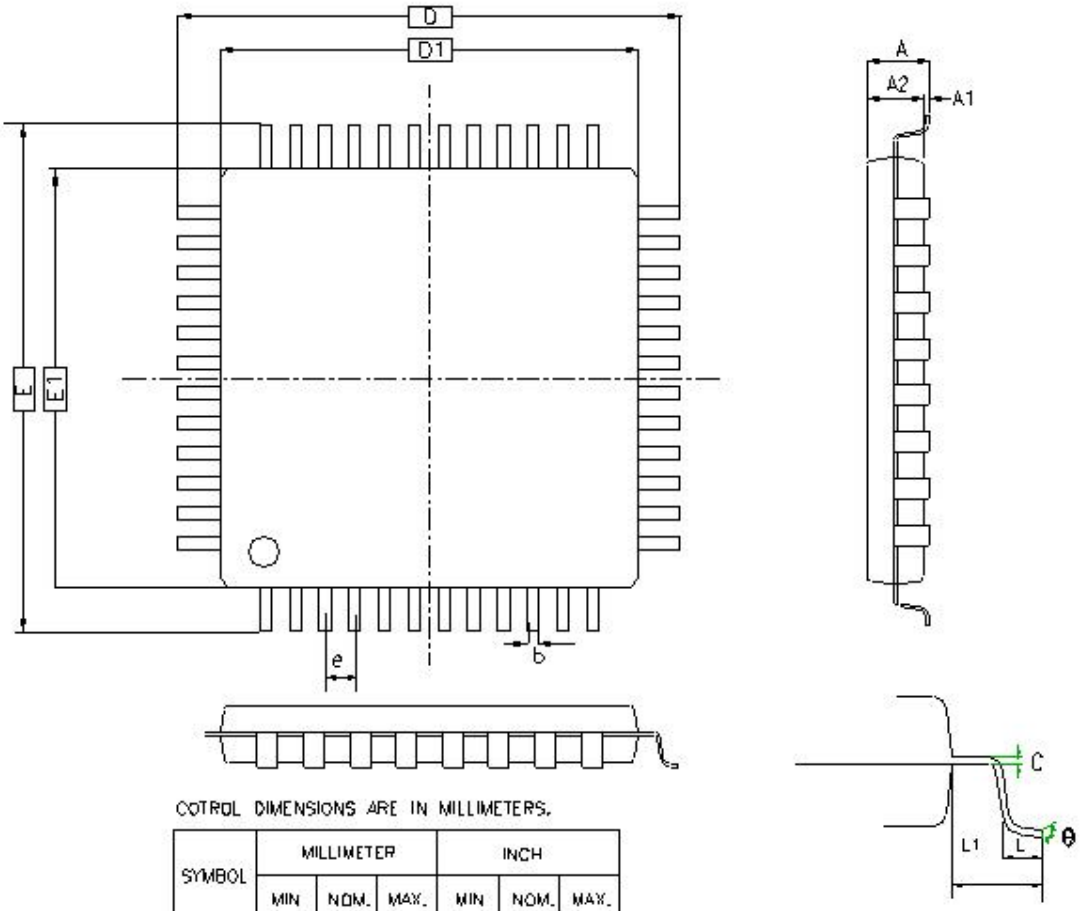
10.3 64S LQFP (7x7x1.4 mm footprint 2.0 mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
	X	D	9 BSC		
	Y	E	9 BSC		
BODY SIZE	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		



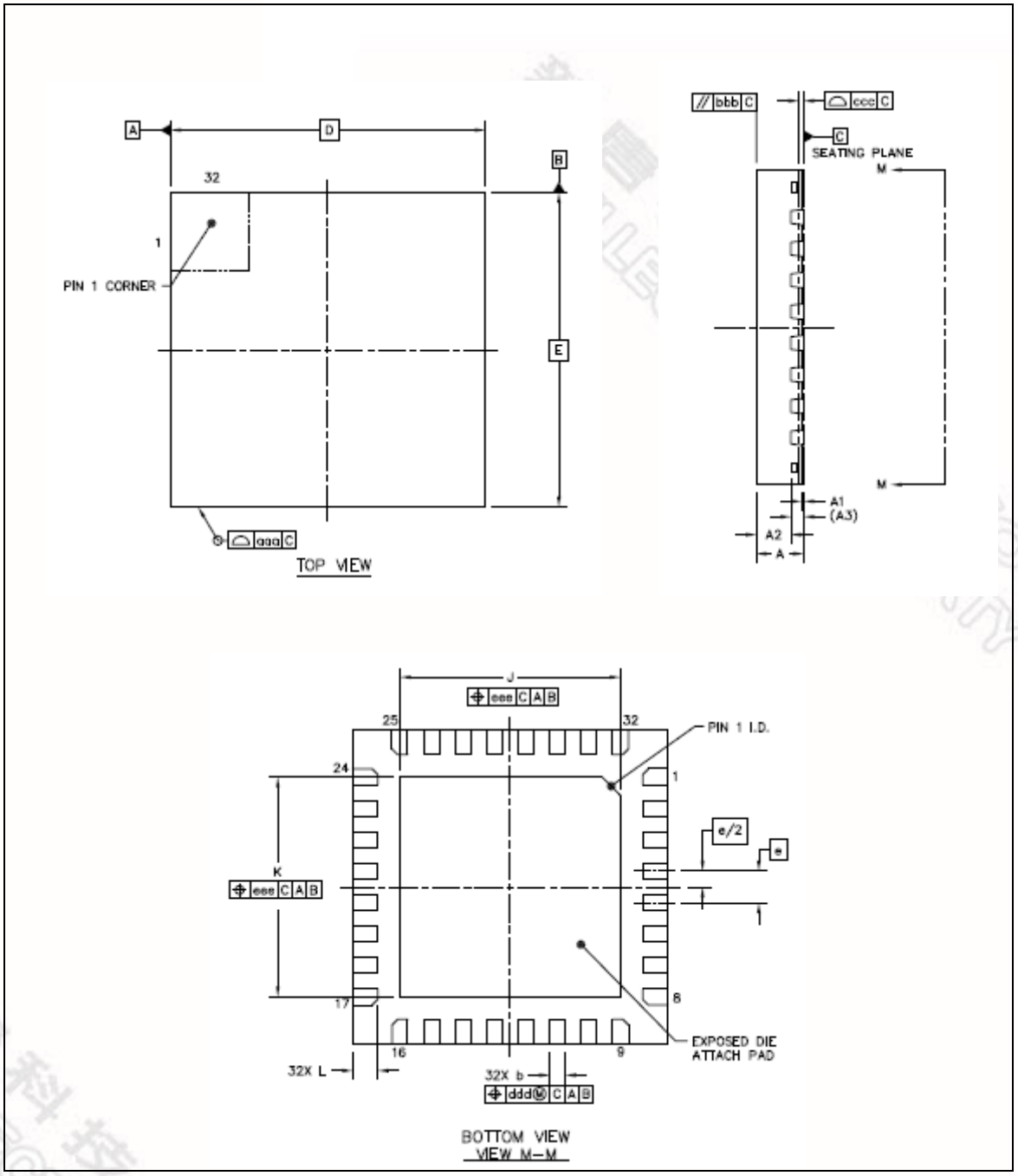
10.4 48L LQFP (7x7x1.4 mm footprint 2.0 mm)



CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN	NOM.	MAX.	MIN	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D1	6.90	7.00	7.10	0.272	0.276	0.280
E1	6.90	7.00	7.10	0.272	0.276	0.280
e	0.35	0.50	0.65	0.014	0.020	0.260
D	8.9	9.00	9.10	0.350	0.354	0.358
E	8.9	9.00	9.10	0.350	0.354	0.358
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	—	1.00	—	—	0.039	—
C	0.09	—	0.20	0.0035	—	0.0079
θ	0°	—	7°	0°	—	7°
b	0.17	0.22	0.27	0.007	0.0087	0.011

10.5 33L QFN (5x5x1.4 mm footprint 2.0 mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	3.4	3.5	3.6
	Y	K	3.4	3.5	3.6
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

11 REVISION HISTORY

Date	Revision	Description
2014.03.28	1.00	1. Initial release
2014.05.08	1.01	1. Modified some typos and format.
2014.09.02	1.02	1. Modified the pin description for LCD_Vx in section 4.4. 2. Modified all PWM1 group to PWM0 group in section 6.10. 3. Modified “PWM1 channel 2 and 3” to “PWM0 channel 2 and 3” in section 6.10. 4. Modified some typos and format.
2015.01.15	1.03	1. Updated ADC channel number in NANO102 feature list in Chapter 2. 2. Corrected typo in NANO102 64-pin sequence in section 4.4. 3. Updated all power related pins from “VDD, VSS, AVDD, AVSS, VTEMP and VLCD” to “V_{DD}, V_{SS}, AV_{DD}, AV_{SS}, V_{TEMP} and V_{LCD}” in the Datashhet.

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