



# Hardware Reference Manual

REV. March 2019

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## Liger (VL-EPM-43)

Intel® Core™-based Single Board Computer with Dual Ethernet, Video, USB, SATA, Serial I/O, Digital I/O, Trusted Platform Module security, Counter/Timers, Mini PCIe, mSATA, SPX, and PC/104-Plus Expansion





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## Product Release Notes

- Rev 1.0** Production release for the Rev 1.0 board
- Rev 1.1** Updated pinout on figure 14. Updated Web links
- Rev 1.2** Updated J2 cable information in table 2

## Support Page

The [Liger Support Page](#) contains additional information and resources for this product including:

- Operating system information and software drivers
- Data sheets and manufacturers' links for chips used in this product
- BIOS information and upgrades

## VersaTech KnowledgeBase

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- Steps you have taken to resolve or recreate the problem
- The return shipping address

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**Note:** Mark the RMA number clearly on the outside of the box before returning.

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# Introduction

# 1

## Description

### Features and Construction

The Liger is a feature-packed single board computer (SBC) designed to support OEM applications where high reliability and long-term availability are required. Its features include:

- Intel® Core “Kaby Lake”, dual core processor with clock rates up to 2.8 GHz
- PC/104-Plus expansion site (ISA + PCI)
- Integrated IntelGen9 graphics core, supporting DirectX11, Open GL3, and H.264, MPEG-2 encoding/decoding
- DisplayPort\* video outputs
- Up to 16 GB DDR3L memory
- Dual Ethernet ports, auto-detect 10Base-T / 100Base-TX / 1000Base-T
- Two USB 3.0 ports and four USB 2.0 ports
- Trusted Platform Module
- 2 RS-232/422/485 serial ports
- 2 RS-232 serial ports
- Three 8254 timer/counters
- Eight digital I/O lines
- 2 SATA ports, 6 Gb/s
- Mini PCIe / mSATA socket, supports Wi-Fi modems, GPS receivers, flash storage, and other modules
- SPX expansion
- PC/104-Plus expansion
- Customization available

The Liger is compatible with popular operating systems such as Microsoft® Windows®, Windows Embedded, Linux and VxWorks®.

VL-EPM-43 boards are subjected to complete functional testing and are backed by a limited five-year warranty. Careful parts sourcing and US-based technical support ensure the highest possible quality, reliability, service, and product longevity for this exceptional single-board computer (SBC).

Figure 1 and Figure 2 show the locations of the Liger board’s connectors and major components on the top side and bottom side of the board, respectively



Figure 1. Major Components and Connectors (Top Side)

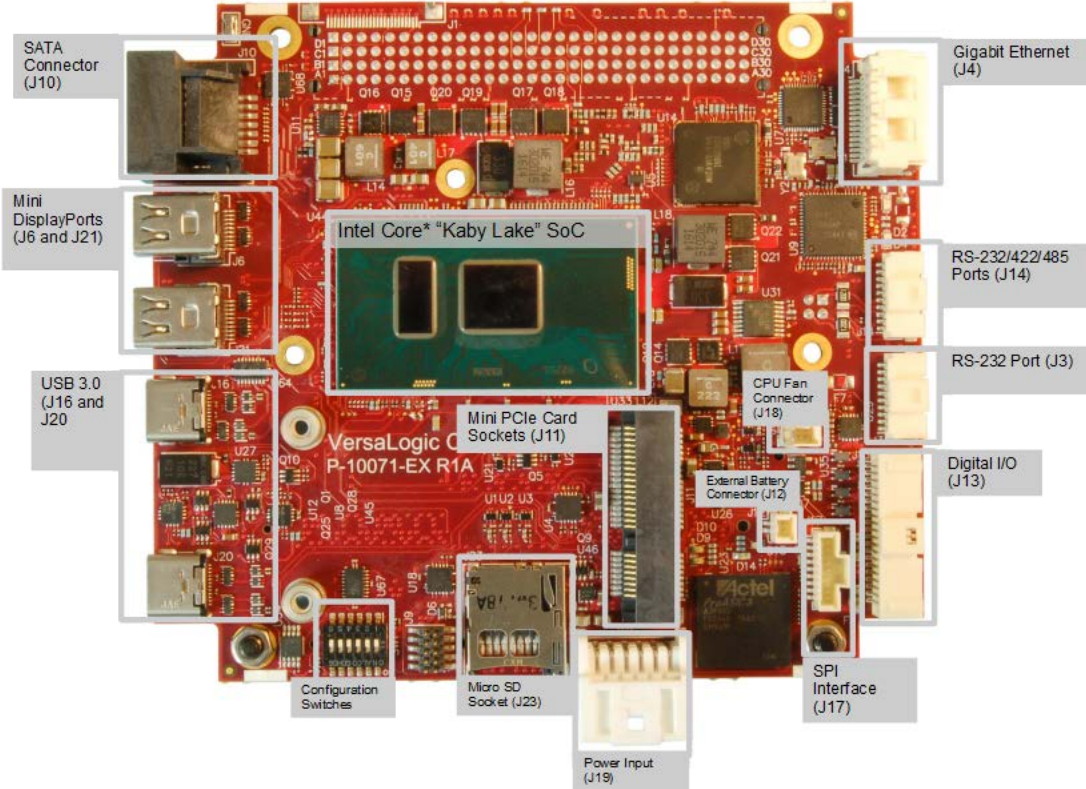


Figure 2. Major Components and Connectors (Bottom Side)



## Technical Specifications

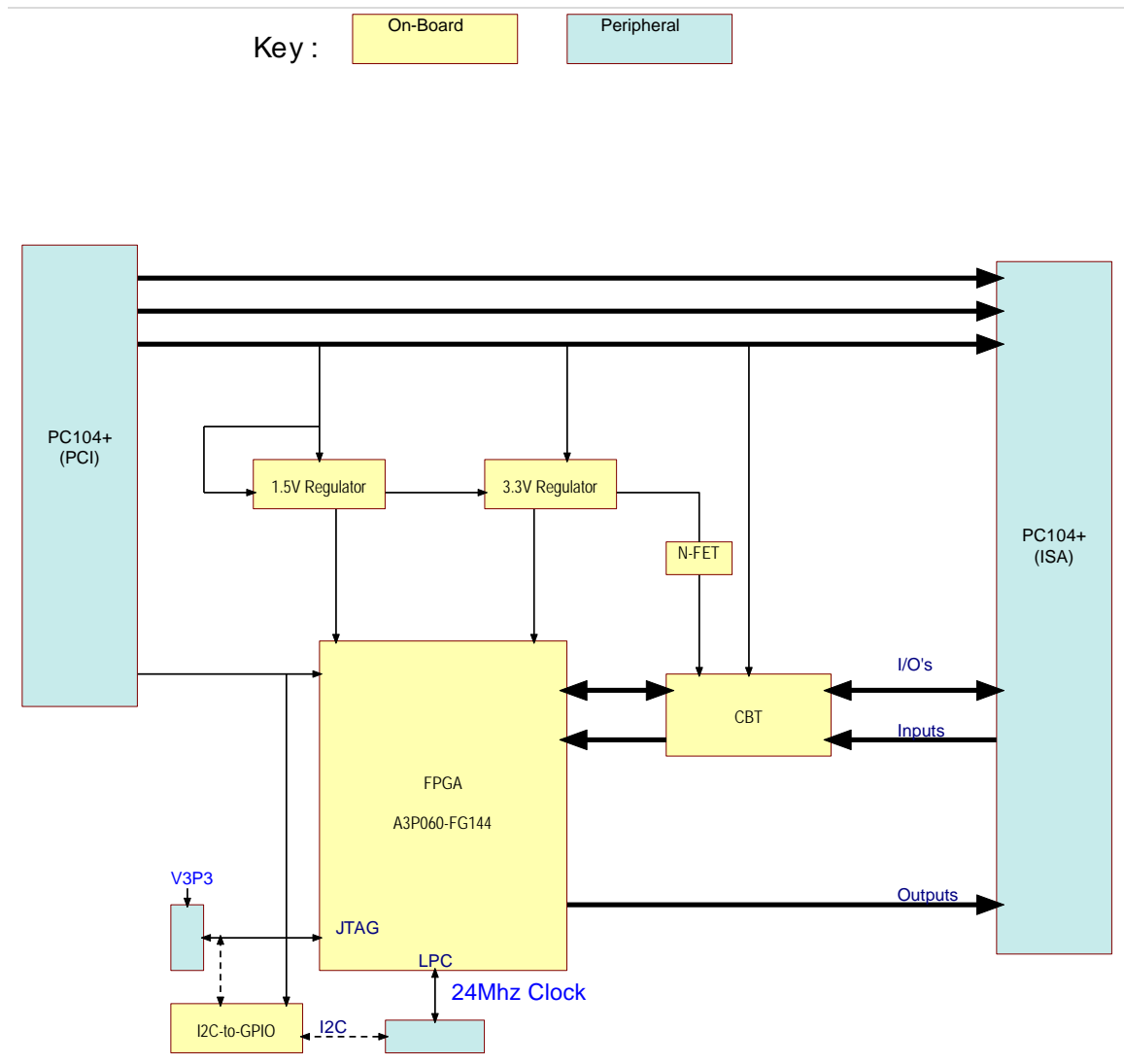
See the [Liger Data Sheet](#) for complete specifications.

## Thermal Considerations

The operating temperature for the Liger is -40°C to +85°C, de-rated -1.1 °C per 305m (1,000 ft.) above 2,300m (7,500 ft.). All Liger models include a rigid-mount heat plate thermal solution. Refer to Chapter 6 for information on additional thermal solutions.



Figure 4. Liger A-EPM43S (Lower) Board Block Diagram



## Cautions

### Electrostatic Discharge

**CAUTION:**

Electrostatic discharge (ESD) can damage circuit boards, disk drives, and other components. Handle circuit board at an ESD workstation. If an approved station is not available, wearing a grounded antistatic wrist strap provides some measure of protection. Keep all plastic away from the board, and do not slide the board over any surface.

After removing the board from its protective wrapper, place the board on a grounded, static-free surface, component side up. Use an antistatic foam pad if available.

Ship and store the board inside a closed metallic antistatic envelope for protection.

**Note:** The exterior coating on some metallic antistatic bags is sufficiently conductive to cause excessive battery drain if the bag comes in contact with the bottom side of the Liger.

### Handling Care

**CAUTION:**

Avoid touching the exposed circuitry with your fingers when handling the board. Though it will not damage the circuitry, it is possible that small amounts of oil or perspiration on the skin could have enough conductivity to cause the contents of CMOS RAM to become corrupted through careless handling, resulting in CMOS resetting to factory defaults.

### Earth Ground Requirement

**CAUTION:**

All mounting standoffs (four on PC/104 boards, eight on EBX and EPIC boards) should be connected to earth ground (chassis ground). This provides proper grounding for EMI purposes.

# Configuration and Setup

## Initial Configuration

Use the following components for a typical development system:

- Liger (VL-EPM-43) computer
- VL-ATX power supply
- DDR3L SO-DIMM module (installed)
- Display with DisplayPort input
- Standard I/O paddleboard (VL-CBR-4005)
- USB keyboard and mouse
- USB CD-ROM drive (optional)
- USB SSD or floppy disk drive (optional)
- VL-HD35-xxx SATA hard drive (optional)

Use the following VersaLogic cables:

- VL-EPH-V6 Mini DisplayPort converter
- VL-CBR-0702 – SATA data cable
- VL-CBR-1205 – Main power cable
- You will also need an operating system (OS) installation CD-ROM and a VL-HDW-413 Heat Sink and fan.

## Basic Setup

The following steps outline the procedure for setting up a typical development system. The Liger should be handled at an ESD workstation or while wearing a grounded antistatic wrist strap.

Before you begin, unpack the Liger and accessories. Verify that you received all the items you ordered. Inspect the system visually for any damage that may have occurred in shipping. Contact [Support@VersaLogic.com](mailto:Support@VersaLogic.com) immediately if any items are damaged or missing.

Gather all the peripheral devices you plan to attach to the Liger and their interface and power cables.

Attach standoffs to the board to stabilize the board and make it easier to work with.

### 1. Attach Cables and Peripherals

- Attach a DisplayPort enabled display to one of the Mini DisplayPort connectors at J6 or J21. The VL-EPH-V6 video adapter card converts DisplayPort output to LVDS.
- Plug the VL-CBR-4005 paddleboard into Main User I/O connector.
- Plug a USB CD-ROM drive, USB keyboard, and USB mouse into any of the USB connectors at J3 and J4 of the paddleboard.
- Plug the SATA data cable VL-CBR-0702 into one of the SATA connector. Attach a hard drive to the connector on the cable.
- Optionally, attach a LAN cable to one of the Ethernet connectors on the Liger using the VL-CBR-1604 dual RJ-45 adapter cable.

## 2. Attach Thermal Solution

- Attach the thermal solution (See [Installing the VersaLogic Thermal Solutions](#)).

## 3. Attach Power

- Plug the power adapter cable VL-CBR-1205 into socket J19. Attach the motherboard connector of the ATX power supply to the adapter.

## 4. Review Configuration

- Before you power up the system, double-check all the connections. Make sure all cables are oriented correctly and that there is adequate power to the VL-EPM-43 and peripheral devices.

## 5. Power On

- Turn on the ATX power supply and the video monitor. The presence of a video signal indicates proper configuration of the system.

## 6. Select a Boot Drive

- During startup, press <CTRL> <B> to display the boot menu. Insert the OS installation CD in the CD-ROM drive and select to boot from the CD-ROM drive.

## 7. Install Operating System

- Install the operating system according to the instructions provided by the operating system manufacturer. (See Operating System Installation.)

## BIOS Setup Utility

Refer to the *BIOS Reference Manual* (available on the [Liger Product Support Page](#)) for information on accessing and configuring settings in the BIOS Setup utility. The *BIOS Reference Manual* contains descriptions of all BIOS menus, submenus, and configuration options.

## Operating System Installation

The standard PC architecture used on the VL-EPM-43 makes the installation and use of most of the standard x86-based operating systems very simple. The operating systems listed on the [VersaLogic OS Compatibility Chart](#) use the standard installation procedures provided by the maker of the OS. Special optimized hardware drivers for a particular OS, or a link to the drivers, are available at the [Liger Product Support Page](#).

# Physical Layout

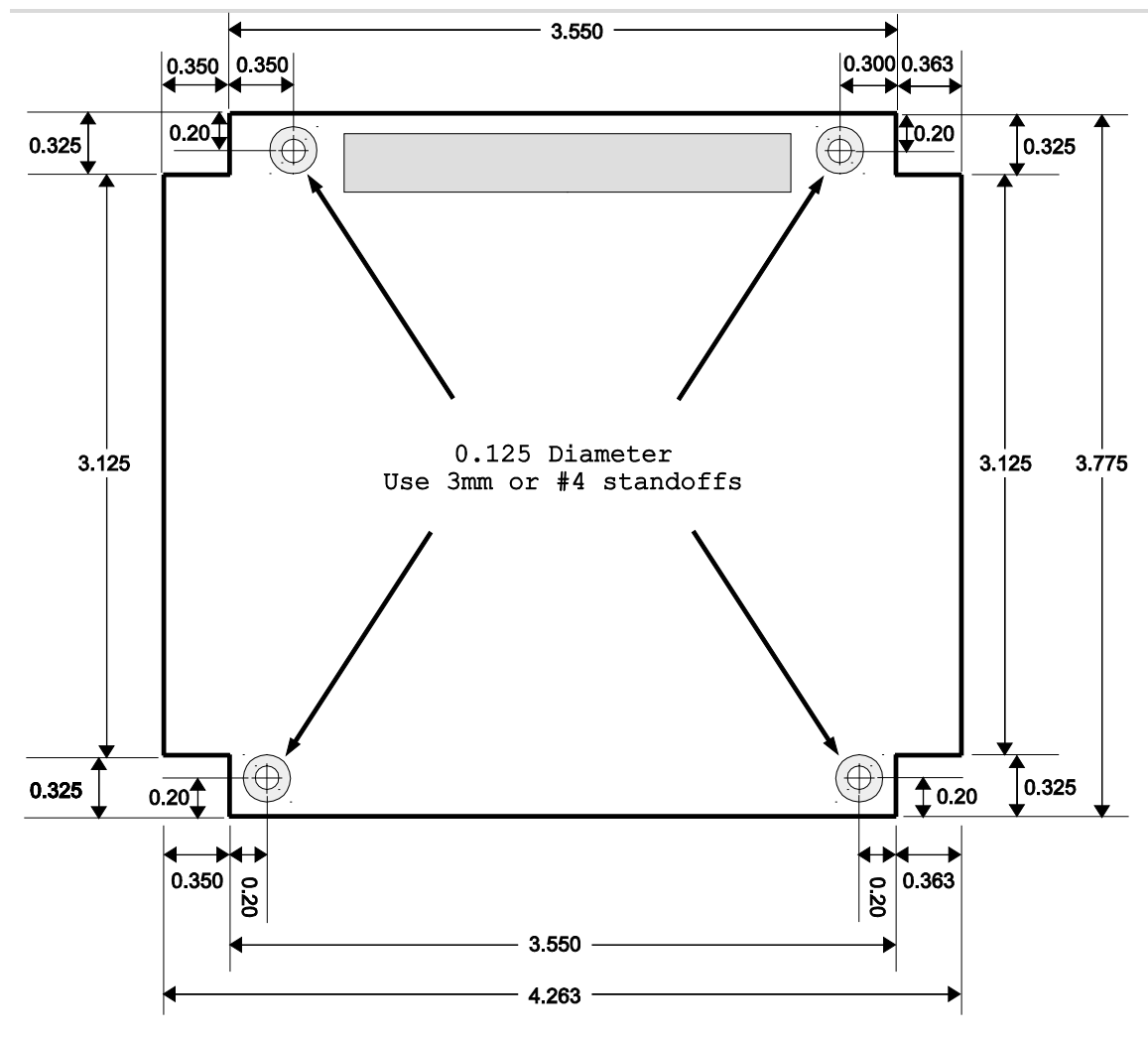
## Dimensions and Mounting

### Liger Dimensions

The Liger complies with PC/104-Plus dimensional standards. The figure below shows the boards dimensions to help with pre-production planning and layout.

**Figure 5. Liger North Board Dimensions and Mounting Holes**

(Not to scale. All dimensions in inches.)





## Hardware Assembly

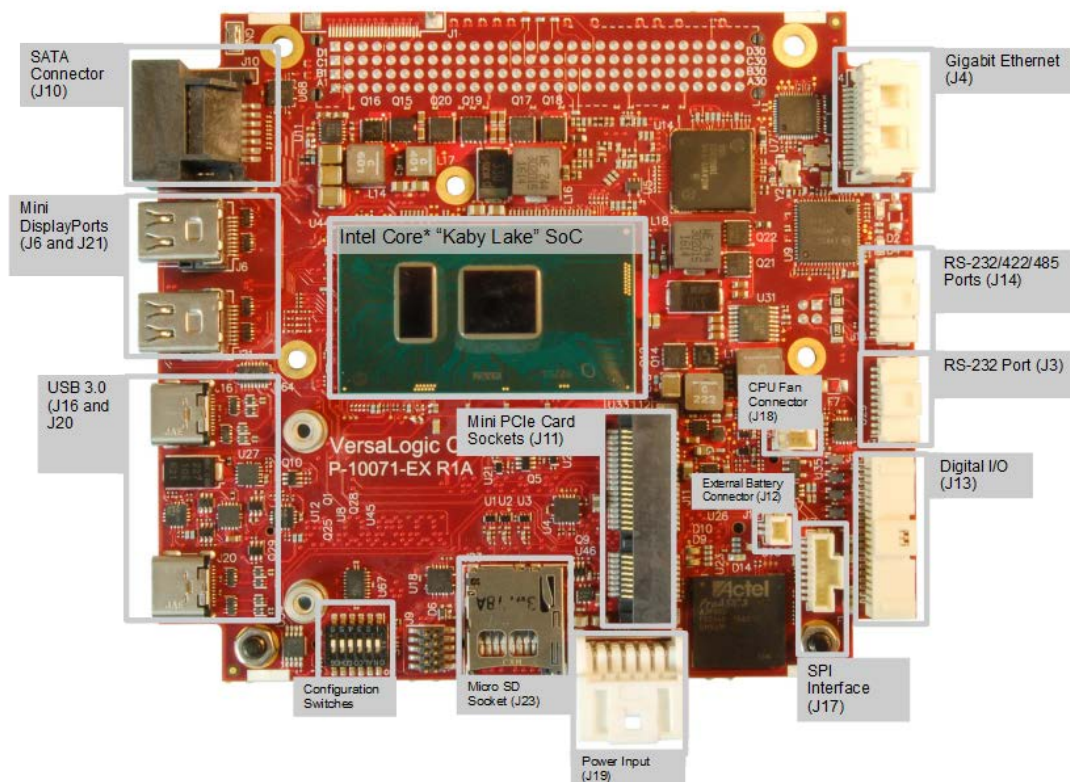
The Liger provides both PCI connectors for adding expansion modules to the bottom of the stack.

The entire assembly can fit on a tabletop or be secured to a base plate. When bolting the unit down, make sure to secure all four standoffs to the mounting surface to prevent circuit board flexing. Standoffs secure the top circuit board using four pan head screws. Standoffs and screws are available as part number VL-HDW-106.

An extractor tool is available (part number VL-HDW-203) to separate the expansion modules from the stack. Use caution when using the extractor tool not to damage any board components.

## External Connectors

Figure 6. Connector Locations (Top Side)





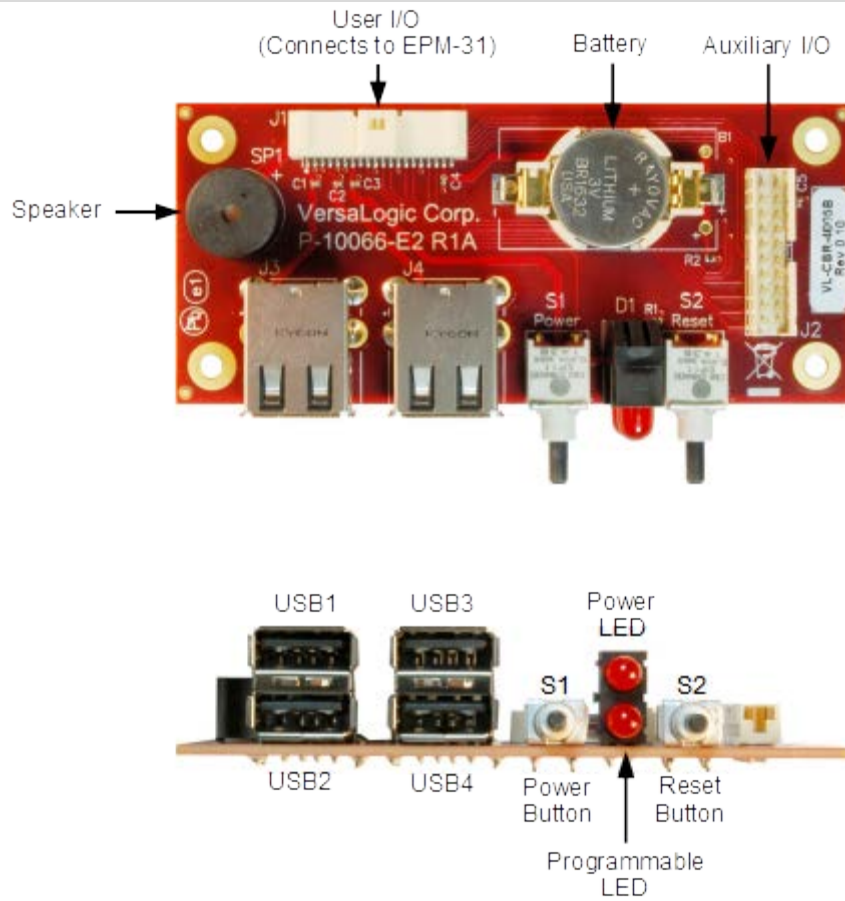
## Liger Connector Functions and Interface Cables

The table below provides information about the function, mating connectors, and transition cables for Liger connectors. Page numbers indicate where additional information is available.

**Table 1. Connector Functions and Interface Cables**

Connector (Note)	Function	Mating Connector	Transition Cable	Cable Description
J1	PCI Bus (A-EPM43S)			
J2	ISA Bus (A-EPM43S)	—	—	—
J3	COM Ports 3 & 4	Molex 501330-1000	VL-CBR-1014	12" 1mm 10-pin Pico-Clasp to dual DB-9 Cable
J4	Dual Gigabit Ethernet	Molex 503149-1600	VL-CBR-1604	12" 16-pin to dual RJ-45 Ethernet cable
J6	Mini DisplayPort 1	—	—	—
J10	SATA	Standard SATA	VL-CBR-0702	20" SATA Cable
J11	PCIe Minicard / mSATA socket	Mini PCIe card or VL-MPEs-F1E series mSATA Flash Drive	—	—
J12	Battery connector	Molex 501330-0200 mating connector housing Molex 501334-0100 mating connector crimp pin for 28-32 gauge wire	—	—
J13	User I/O: USB, PLED, power LED, push-button reset, power button, PC speaker, battery input, I <sup>2</sup> C, GPIO	Molex 501189-4010	VL-CBR-4005A	12" 1 mm Pico-Clasp Cable 40-pin to 40-pin on VL-CBR-4005B paddleboard
J14	COM Ports 1 & 2	Molex 501330-1000	VL-CBR-1014	12" 1mm 10-pin Pico-Clasp to dual DB-9 Cable
J16	Micro USB 3.0	USB 3.0 Micro-C	VL-CBR-2402	USB 3.0 Type-C to Type-A plug cable
J17	SPI	Molex 501330-0900	VL-CBR-0901	8" 9-pin Pico-Clasp to Dual SPX (SPI) Cable
J18	CPU fan	Provided with HDW-413 fan assembly (if used)	—	Fan power cable with 3-pin connector
J19	Main power input	Molex 51353-1200	VL-CBR-1205	Interface from standard ATX power supply
J20	Micro USB 3.0	USB 3.0 Micro-C	VL-CBR-2402	USB 3.0 Type-C to Type-A plug cable
J21	Mini DisplayPort 2	—	VL-CBR-2032  VL-CBR-2033	6" Mini DisplayPort to Mini DisplayPort  Mini DisplayPort to HDMI Active Adapter, 6"
J23	Micro SD socket	VL-F41-xxxx micro SD Flash Drive (SLC)	—	—

Figure 8. VL-CBR-4005 Connectors



## VL-CBR-4005 Connector Functions

Table 2. VL-CBR-4005 Functions

Reference	Function	PCB Connector	Description
B1	Provides power to CMOS RAM and RTC registers when main power is off.	—	Back-up battery
J1	Paddleboard adapter	<ul style="list-style-type: none"> <li>• FCI 20021511-00050T1LF</li> <li>• Oupiin 3216-A50G00SBA</li> <li>• Samtec SHF-125-01-F-D-TH</li> </ul>	1.27 mm, 50-pin keyed header
J2	Auxiliary I/O (I <sup>2</sup> C, GPIO, Ethernet LED, LED power)	FCI 98414-F06-20ULF	2 mm, 20-pin keyed header
J3	USB1 (top), USB2 (bottom)	USB Type A	USB Host
J4	USB3 (top), USB4 (bottom)	USB Type A	USB Host
D1	Programmable LED (top) Power LED (bottom)	LED	—
S1	Power button	Pushbutton	—
S2	Reset button	Pushbutton	—
SP1	Speaker	Piezo speaker	—

### User I/O Connector

The 40-pin J13 I/O connector incorporates the signals for the following:

- Four USB ports
- Eight GPIO lines
- Three LEDs (two Ethernet link status LEDs and a programmable LED)
- I<sup>2</sup>C clock and data signals
- Push-button power switch
- Push-button reset switch
- Speaker output

This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

Table 3 provides the pinout of the user I/O connector.

Figure 9. Location and Pin Orientation of the User I/O Connector

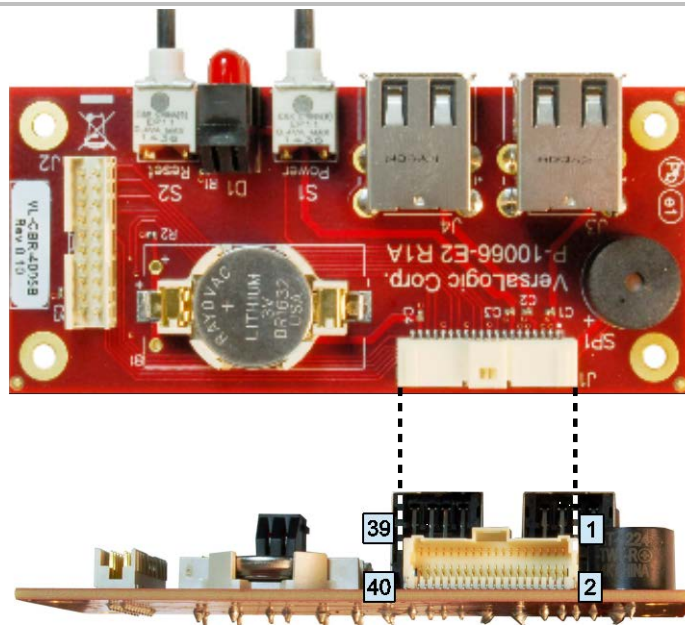


Table 3. User I/O Connector Pinout

Pin	Signal	Pin	Signal
1	V5_USB1-2	2	GND
3	USB1_P	4	USB2_P
5	USB1_N	6	USB2_N
7	V5_USB3-4	8	GND
9	USB3_P	10	USB4_P
11	USB3_N	12	USB4_N
13	V3P3_S0	14	GND
15	SPKR#	16	PLED#
17	PWR_BTN#	18	RST_BTN#
19	GND	20	GND
21	I2C_SCK	22	V_BATT
23	I2C_SDA	24	RETURN_BATT
25	GND	26	GND
27	GPIO1	28	GPIO2
29	GPIO3	30	GPIO4
31	GND	32	GND
33	GPIO5	34	GPIO6
35	GPIO7	36	GPIO8
37	V3P3_AUX_SX	38	GND
39	ETH0_LINKSTAT_LED	40	ETH1_LINKSTAT_LED

## Cabling

An adapter cable, part number CBR-4005A, is available for connecting the CBR-4005B paddleboard to the EPM-43. This is a 12-inch, Pico-Clasp 40-pin to 40-pin cable. The CBR-4005 I/O Cable Assembly consists of both the CBR-4005A cable and the CBR-4005B Paddleboard.

If your application requires a custom cable, the following information will be useful:

CBR-4005B Board Connector	Mating Connector
Molex 501571-4007	Molex 501189-4010

## On-board Battery



### CAUTION:

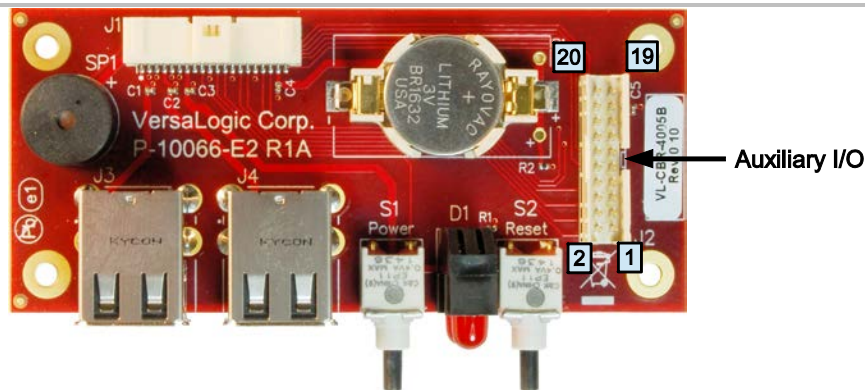
To prevent shorting, premature failure or damage to the Lithium battery, do not place the board on a conductive surface such as metal, black conductive foam or the outside surface of a metalized ESD protective pouch. The Lithium battery may explode if mistreated. Do not recharge, disassemble, or dispose of the battery in fire. Dispose of used batteries promptly.

Nominal battery voltage is 3.0 V. If the voltage drops below 2.7 V, contact the factory for a replacement. The life expectancy under normal use is approximately five years.

## Auxiliary I/O Connector

The next figure shows the location and pin orientation of the auxiliary I/O connector.

**Figure 10. Location and Pin Orientation of Auxiliary I/O Connector**



**Table 4. Auxiliary I/O Connector Pinout**

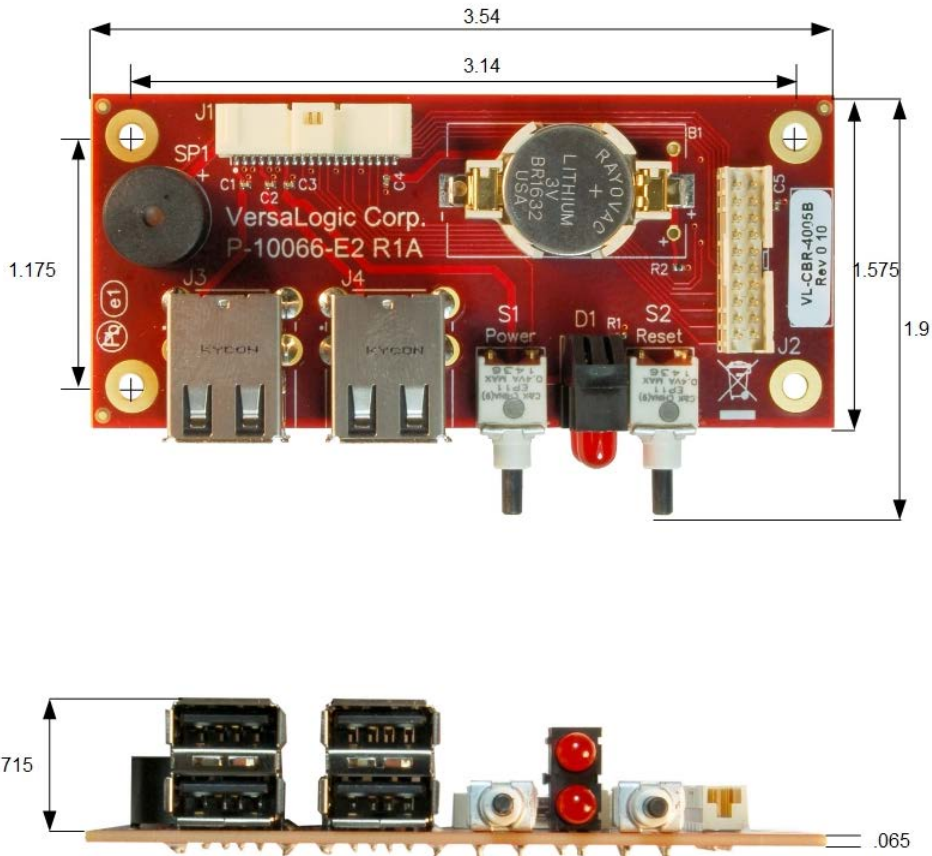
Pin	Signal	Pin	Signal
1	I2C_SCK	2	V_BATT
3	I2C_SDA	4	V_BATT_RETURN
5	GND	6	GND
7	GPIO1	8	GPIO2
9	GPIO3	10	GPIO4
11	GND	12	GND
13	GPIO5	14	GPIO6
15	GPIO7	16	GPIO8
17	V3P3_AUX_SX	18	GND
19	ETH0_LINKSTAT_LED	20	ETH1_LINKSTAT_LED

**VL-CBR-4005 Dimensions**

The figure below shows the dimensions and mounting holes for the VL-CBR-4005.

- All dimensions are in inches
- Illustration is not to scale

**Figure 11. VL-CBR-4005 Dimensions and Mounting Holes**

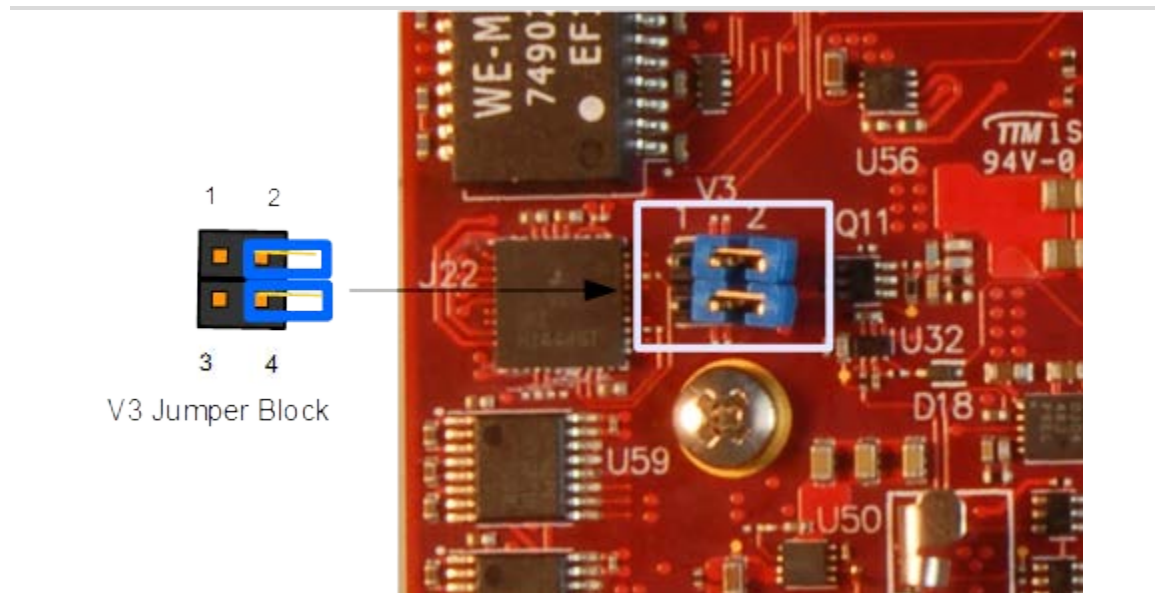




## Jumper Blocks

Jumper block V3 is located on the bottom side of the board. The board ships with two jumpers installed, but only one side of each jumper is placed on a pin of the V3 jumper block. In this configuration, the jumpers do not connect any signals. They are placed this way in case you need to configure the COM ports for RS-485 termination.

**Figure 12. As-Shipped Jumper Settings**



**Table 5. Jumper Summary**

Jumper Block	Description
V3[1-2]	<p><b>COM1 Rx End-point Termination (see page 25)</b></p> <p>In – RS-485 termination  <b>Out – No termination, RS-232 (default)</b></p> <p>Places terminating resistor across COM1 RS-485 TXRX+/TXRX- or RS-422 RX+/RX- differential pair. Jumper must be out for RS-232 operation.</p>
V3[3-4]	<p><b>COM2 Rx End-point Termination (see page 25)</b></p> <p>In – RS-485 termination  <b>Out – No termination, RS-232 (default)</b></p> <p>Places terminating resistor across COM2 RS-485 TXRX+/TXRX- or RS-422 RX+/RX- differential pair. Jumper must be out for RS-232 operation.</p>



### Integrator's Note:

No jumper is required for RS-422. You may use a terminator at the receiver, but it is not required. A jumper should be used for RS-485 only when the port is used as an endpoint.

## Configuration Switches

The next figure shows the as-shipped switch configuration with all switches in the Off position. The Off position is toward the center of the board.

Figure 13. Location of SW1 Configuration Switch Block

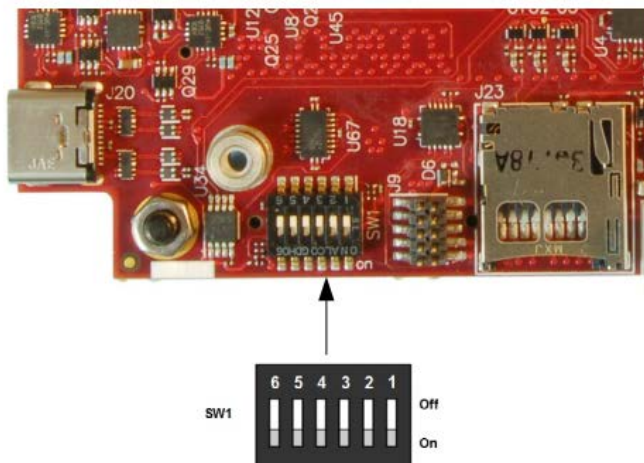


Table 6. Switch Setting Summary

SW1 Switch Position	Description
Position 1	<b>Clear CMOS RAM and Clears Real-Time Clock</b> Off – Normal operation (default) On – Clears battery backed up CMOS
Position 2	<b>No Battery Switch</b> (see Integrator's Note below) Off – A battery is being used (default) On – A battery is not being used
Position 3	<b>Reset BIOS to factory defaults</b> Off – Normal operation (default) On – Resets BIOS to factory defaults when the board boots.
Position 4	<b>For factory use only. Always leave in the Off position.</b>
Position 5	<b>SPI Flash Security</b> – Not supported.
Position 6	<b>BIOS select</b> Off – Primary BIOS (default) On – Backup BIOS

**Integrator's Note:**

- **If a battery is installed** (on the CBR-4005 paddleboard or externally using the J8 connector), switch position 2 must be set to the Off position. If it is set to On, the battery will discharge quickly.
- **If you do not use a battery**, switch position 2 should be set to the ON position. Otherwise, boot times could increase (by as much as 30 seconds in low temperature environments).

# System Features

## Power Supply

### Power Connectors

Main power is applied to the Liger through a 12-pin polarized connector (J19), with mating connector Berg 69176-010 (housing) + Berg 47715-000 (pins). See the table below for connector pinout.



#### CAUTION:

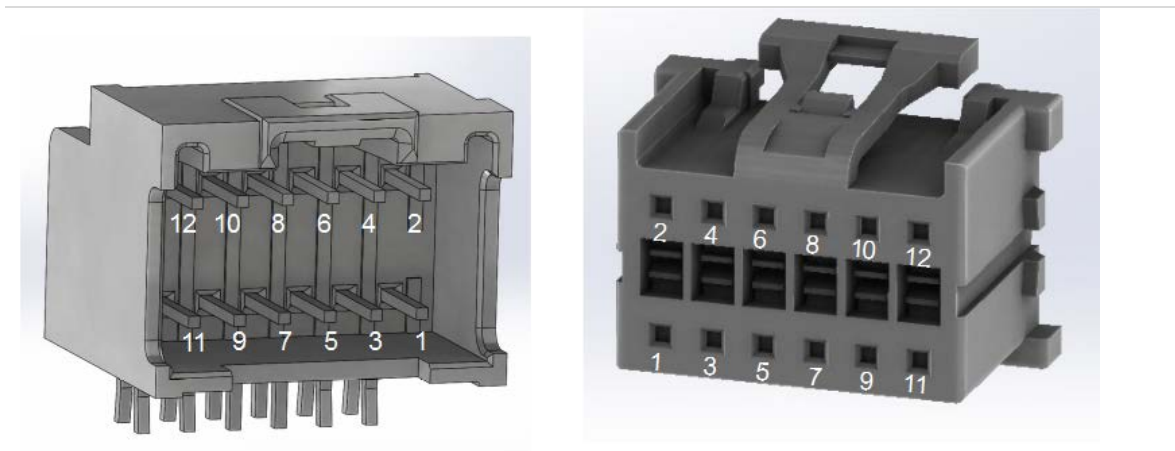
To prevent severe and possibly irreparable damage to the system, it is critical that the power connectors are wired correctly. Make sure to use all +5 V<sub>DC</sub> pins and all ground pins to prevent excess voltage drop. The power connector is not fuse or diode protected. Proper polarity must be followed otherwise damage will occur.

**Table 7. J19 Main Power Connector Pinout**

Pin	Signal	Pin	Signal
1	+5 V <sub>DC</sub>	2	Ground
3	+5 V <sub>DC</sub>	4	Ground
5	+5 V <sub>DC</sub>	6	Ground
7	+5 V <sub>DC</sub>	8	Ground
9	+3.3 V <sub>DC</sub>	10	Ground
11	+12 V <sub>DC</sub>	12	-12 V <sub>DC</sub>

The next figure shows the VersaLogic standard pin numbering for this type of 12-pin power connector and the corresponding mating connector.

Figure 14. J19 and VL-CBR-1205 Pin Numbering



### Power Requirements

The Liger requires only +5.15 VDC ( $\pm 2\%$ ) for proper operation, as required by the PC/104-Plus specification. Variable low-voltage supply circuits provide power to the CPU and other on-board devices.

The exact power requirement of the VL-EPM-43 depends on several factors, including memory configuration, CPU clock rate, peripheral connections, and the type and number of expansion modules and attached devices. For example, driving long RS-232 lines at high speed can increase power demand.

### Power Delivery Considerations

Using the VersaLogic approved power supply (VL-PS- ATX12-300A) and power cable (VL-CBR-1205) ensures high quality power delivery to the board. Customers who design their own power delivery methods should take into consideration the guidelines below to ensure good power connections.

In addition, the specifications for typical operating current do not include any off-board power usage that may be fed through the Liger power connector. Expansion boards and USB devices plugged into the board will source additional power through the Liger power connector.

- Do not use wire smaller than 22 AWG. Use high quality UL 1007 compliant stranded wire.
- The length of the wire should not exceed 18 inches.
- Avoid using any additional connectors in the power delivery system.
- The power and ground leads should be twisted together, or as close together as possible to reduce lead inductance.
- A separate conductor must be used for each of the power pins.
- All power input pins and all ground pins must be independently connected between the power source and the power connector.
- Use a high quality power supply that can supply a stable voltage while reacting to widely varying current draws.

## CPU

The Liger uses one of three Intel Core\* (formerly “Kaby Lake”) system-on-chip (SoC) processors:

- i7-7600U (dual core) – 4 MB Cache - [Specifications](#)
- i5-7300U (dual core) – 3 MB Cache - [Specifications](#)
- i3-7100U (dual core) – 3 MB Cache - [Specifications](#)

These processors support Intel 64-bit instructions, AES Instructions, Execute Disable Bit, and Virtualization Technology.



### Integrator’s Note:

The EPM-43EAP SKUs using the i3-7100U processor do not support Intel vPRO Technology\* (which includes Active Management Technology or Intel AMT\*). The i5-7300U (EPM-43EBP) and i7-7600U (EPM-43ECP) processor SKUs support Intel vPRO Technology.

## System RAM

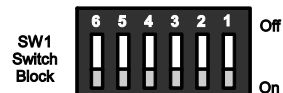
The Liger ships with one 204-pin SO-DIMM memory module (J2 connector) with the following characteristics:

- Size Up to 16 GB, 1600 MHz, CPU dependent
- Voltage 1.35 V
- Type DDR3L (VersaLogic VL-MM9 Series modules)

## Resetting BIOS to Factory Defaults

Reset the BIOS to default settings using the following the instructions:

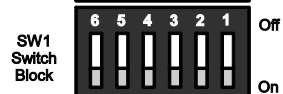
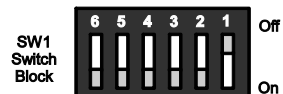
1. Power off the Liger and set SW1 switch position 3 to the On position (toward the outer edge of the board). →
2. Power on the Liger.
3. After the system boots, power off the Liger and set the switch back to the Off position (toward the center of the board). →
4. Power on the Liger.



## Clearing CMOS RAM and RTC Registers

Clear the CMOS RAM and RTC registers (which includes the date/time) using the following the instructions:

1. Power off the Liger.
2. Set SW1 switch position 1 to the On position (toward the outer edge of the board). →
3. Wait at least two seconds and set the switch back to the Off position (toward the center of the board). →



4. Power on the Liger.

## Real Time Clock (RTC)

The Liger features a real-time clock/calendar (RTC) circuit. The RTC can be set using the BIOS Setup utility.

The Liger supplies RTC voltage in S5, S3, and S0 states, but requires an external +2.75 V to +3.3 V battery connection to maintain RTC functionality and RTC CMOS RAM when the Liger is not powered. The battery connection can be made to either (but not both) of the following:

- J8 battery connector
- Pin 17 of the J18 connector



### Integrator's Note:

There is no on-board battery. The Liger board will operate without a battery, but to save the date and time, use a VL-CBR-4005 paddleboard (which includes a battery).

## Expansion Bus

### PC/104-Plus

The EPM-43 provides a legacy stack-down PCI connector at locations J1 (for PCI) and J2 (for ISA) on the bottom side of the board for PC/104-Plus (PCI +ISA) as well as PCI-104 (PCI only) and PC/104 (ISA only) expansion modules.

The table below lists the maximum PC/104-Plus slot current rating on the EPM-43. This is the aggregate power available to both the PCI and ISA connectors. ISA does not use +3.3 V power, so all of the +3.3 V power is available for the PCI connector.

**Table 8: PCI/104-Plus Connector (PCI) Maximum Current**

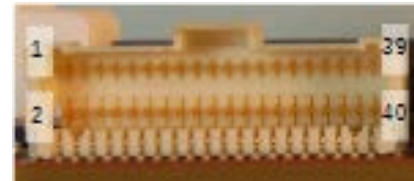
Voltage	Maximum Current
+5 V	4.0 A
+3.3 V	3.0 A
+12 V	1.0 A
-12 V	0.5 A

## User I/O Connector

The table below lists the pinout of the 40-pin User I/O connector (J13).

**Table 9. J13 User I/O Connector Pinout**

Pin	Signal	Pin	Signal
1	V5_USB1-2	2	GND
3	USB1_P	4	USB2_P
5	USB1_N	6	USB2_N
7	V5_USB3-4	8	GND
9	USB3_P	10	USB4_P
11	USB3_N	12	USB4_N
13	V3P3_S0	14	GND
15	SPKR#	16	PLED#
17	PWR_BTN#	18	RST_BTN#
19	GND	20	GND
21	I2C_SCK	22	V_BATT
23	I2C_SDA	24	RETURN_BATT
25	GND	26	GND
27	GPIO1	28	GPIO2
29	GPIO3	30	GPIO4
31	GND	32	GND
33	GPIO5	34	GPIO6
35	GPIO7	36	GPIO8
37	V3P3_AUX_SX	38	GND
39	ETH0_LINKSTAT_LED	40	ETH1_LINKSTAT_LED



## Serial Ports

The Liger features two on-board 16550-based serial communications channels located at standard PC I/O addresses. The serial ports can be operated in RS-232 4-wire, RS-422, or RS-485 modes. I/O addresses and IRQ interrupts are chosen in the BIOS Setup utility. Each COM port can be independently enabled, disabled, or assigned a different I/O base address in the BIOS Setup utility.

## COM Port Configuration

Use the BIOS Setup utility to select between RS-232 and RS-422/485 operating modes.

Jumper block V1 configures the serial ports for RS-422/485 operation. See [Jumper Summary](#) for details. The 120  $\Omega$  termination resistor should be enabled RS-485 endpoint stations; termination is optional for RS-422. It must be disabled for all RS-232 modes and RS-485 intermediate stations.

If RS-485 half-duplex mode is used, the differential twisted pair (TxD+/RxD+ and TxD-/RxD-) is formed by connecting TxD+ to RxD and TxD- to RxD-.

## RS-485 Mode Line Driver Control

The transmit line driver can be automatically turned on and off based on data availability in the UART output FIFO. This mode can be enabled in the BIOS Setup utility. The transmit line driver can be enabled in the BIOS Setup utility.

## Serial Port Connectors

The pinouts of the DB9M connectors apply to the serial connectors on the VL-CBR-1014 adapter cable.

These connectors use IEC 61000-4-2-rated TVS components to help protect against ESD damage.

**Table 10. COM1-2 Pinout – VL-CBR-1014 Adapter Cable J14**

Pin	RS-232 Signal	RS-422/485 Signal	Description
1	RTS1	TXD1+	
2	TXD1#	TXD1-	
3	CTS1	RXD1+	
4	RXD1#	RXD1-	
5	GND	GND	Signal Ground
6	RTS2	TXD2+	
7	TXD2#	TXD2-	
8	CTS2	RXD2+	
9	RXD2#	RXD2-	
10	GND	GND	Signal Ground



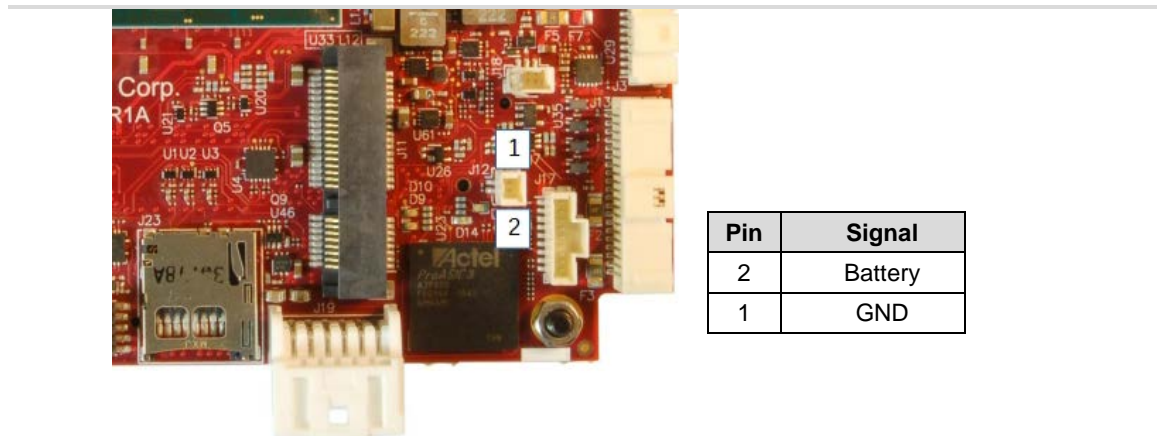
**Table 11. COM3-4 Pinout – VL-CBR-1014 Adapter Cable J3**

Pin	Signal	Description
1	RTS3	
2	TXD3#	
3	CTS3	
4	RXD3#	
5	GND	Signal Ground
6	RTS4	
7	TXD4#	
8	CTS4	
9	RXD4#	
10	GND	Signal Ground

## Battery Connector

Connector J12 can be used to connect an external battery to the Liger board. A compatible battery is available from VersaLogic, part number VL-CBR-0203.

**Figure 15. Location and Pin Configuration of J8 Battery Connector**



### VL-CBR-0203 External Battery Module

The VL-CBR-0203 is an external battery module compatible with the Liger board. For more information, contact [Sales@VersaLogic.com](mailto:Sales@VersaLogic.com).

Figure 16. VL-CBR-0203 Latching Battery Module



## USB Interfaces

The table below lists the pinouts of the USB Type C basic connectors.

Table 12. USB 3.0 J16, J20 Connector Pinout

Pin	Signal	Direction	Description	Pin	Signal	Direction	Description
A1	GND	--	Signal Ground	B12	GND	--	Signal Ground
A2	SSTXp1	Out	Positive Tx Diff Pair ("A" Side)	B11	SSRXp2	In	Positive Rx Diff Pair ("B" Side)
A3	SSTXn1	Out	Negative Tx Diff Pair ("A" Side)	B10	SSRXn2	In	Negative Rx Diff Pair ("B" Side)
A4	+5V	Out	VBUS Voltage (max 900mA)	B9	+5V	Out	VBUS Voltage (max 900mA)
A5	CC1	I/O, Power	"A" side CC signal used to detect power levels, device connector and to provide VCONN power	B8	SBU2	Not Connected	"B" Side Sideband Signal used in Alternate Modes. These are not connected on the EPM-43
A6	Dp1	I/O	USB 2.0 Diff pair positive ("A" Side) See Note	B7	Dn2	I/O	USB 2.0 Diff pair negative ("B" Side) See Note
A7	Dn1	I/O	USB 2.0 Diff pair negative ("A" Side) See Note	B6	Dp2	I/O	USB 2.0 Diff pair positive ("B" Side) See Note
A8	SBU1	Not Connected	"A" Side Sideband Signal used in Alternate Modes. These are not connected on the EPM-43	B5	CC2	I/O, Power	"B" side CC signal used to detect power levels, device connector and to provide VCONN power
A9	+5V	Out	VBUS Voltage (max 900mA)	B4	+5V	Out	VBUS Voltage (max 900mA)
A10	SSRXn1	In	Negative Rx Diff Pair ("A" Side)	B3	SSTXn1	Out	Negative Tx Diff Pair ("B" Side)
A11	SSRXp1	In	Positive Rx Diff Pair ("A" Side)	B2	SSTXp1	Out	Positive Tx Diff Pair ("B" Side)
A12	GND	--	Signal Ground	B1	GND	--	Signal Ground

**Note:** Dp1 and Dp2 are connected to each other on the board. Dn1 and Dn2 are connected to each other on the board.

The Kaby Lake-U uses a xHCI USB controller (there is no legacy EHCI USB controller). Some older operating systems (such as MS-DOS) may not support xHCI.

The VersaLogic VL-CBR-2402 cable is a USB 3.0 Micro-C to Type-A adapter. The VL-CBR-2402 cable can be used to connect the Liger to any certified USB 3.0 hubs.

## LEDs

### FPGA Controlled LEDs

The FPGA controls three LEDs (the Blue is an individual LED and the Green/Yellow is a dual-package):

- Blue – used for SATA (and mSATA) activity indication.
- Green – used for Power-Good indication when in S0 (and will do a very low duty cycle pulse when in sleep modes as an indication that the board is still powered).
- Yellow – used for errors or debug (software enables this).

The Yellow LED can be also used for debug purposes.

### Power LEDs

The power LED on the VL-CBR-4005 indicates that the paddleboard is being powered by the 3.3 V supply (though it does not indicate that all S0 power supplies are within specified limits). The LED is lit only when the board is in the S0 power state. If the board enters a Sleep (S3) or Hibernate (S4) mode, the LED will not be lit.

## Power Button

Connector J13 includes an input for a power button. Shorting J13 (pin 17) to ground causes the board to enter an S5 power state (similar to the Windows Shutdown state). Shorting it again returns the board to the S0 power state and reboots the board. The button can be configured in Windows to enter an S3 power state (Sleep, Standby, or Suspend-to-RAM), an S4 power state (Hibernate or Suspend-to-Disk), or an S5 power state (Shutdown or Soft-Off).

The input can be connected to ground using the normally open contacts of a pushbutton switch or a relay, or with a switching transistor (open-collector or open-drain) capable of sinking 1 mA. The input must be driven to a voltage between 0 V and 500 mV to be recognized by the Liger. Do not add an external pull-up resistor to this signal.

This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

In configurations where a power button is not connected to the board, if the system is put into an S5 state, power can be restored by turning off the power supply and turning it back on. This behavior is set by default in the BIOS.

## Supported Power States

The table below lists the supported power states.

**Table 13. Supported Power States**

Power state	Description
S0 (G0)	Working
S1 (G1-S1)	All processor caches are flushed, and the CPUs stop executing instructions. Power to the CPUs and RAM is maintained. Devices that do not indicate they must remain on may be powered down.
S3 (G1-S3)	Commonly referred to as Standby, Sleep, or Suspend-to-RAM. RAM remains powered.
S4 (G1-S4)	Hibernation or Suspend-to-Disk. All content of main memory is saved to non-volatile memory, such as a hard drive, and is powered down.
S5 (G2)	Soft Off. Almost the same as G3 Mechanical Off, except that the power supply still provides power, at a minimum, to the power button to allow return to S0. A full reboot is required. No previous content is retained. Other components may remain powered so the computer can "wake" on input from the keyboard, clock, modem, LAN, or USB device.
G3	Mechanical off (ATX supply switch turned off).

## Pushbutton Reset

Connector J13 includes an input for a pushbutton reset switch. Shorting J13 (pin 18) to ground causes the Liger to reboot.

The input can be connected to ground using the normally open contacts of a pushbutton switch or a relay, or with a switching transistor (open-collector or open-drain) capable of sinking 1 mA. The input must be driven to a voltage between 0 V and 500 mV to be recognized by the Liger. Do not add an external pull-up resistor to this signal.

This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

## Speaker

Connector J13 includes a speaker output signal at pin 15. The VL-CBR-4005 paddleboard provides a Piezo-electric speaker (as shown in Figure 8).

## Video Interfaces

The two mini DisplayPort video interfaces support Extended Desktop, Clone, and Twin display modes.

The optional VL-EPH-V6 video adapter card converts DisplayPort output to LVDS for flat panel operation.

### DisplayPort

The two DisplayPort ++ connections provided use two 20-pin mini DisplayPort connectors. DisplayPort consists of three interfaces:

- Main Link – transfers high-speed isochronous video and audio data.
- Auxiliary channel – used for link management and device control; the EDID is read over this interface.

- Hot Plug Detect – indicates that a cable is plugged in.

**Table 14. Mini DisplayPort Connector Pinout**

Pin	Signal	Direction	Description
1	GND	--	Ground
2	HPDETECT	Input	Hot Plug Detect (used to determine if a far end device is connected to the port)
3	ML_LANE0_P	Output	DisplayPort Lane 0 (positive)
4	CONFIG1	Input	0 - for DisplayPort, 1 - For HDMI passive adapter
5	ML_LANE0_N	Output	DisplayPort Lane 0 (negative)
6	CONFIG2	Output	
7	GND	--	Ground
8	GND	--	Ground
9	ML_LANE1_P	Output	DisplayPort Lane 1 (positive)
10	ML_LANE3_P	Output	DisplayPort Lane 3 (negative)
11	ML_LANE1_N	Output	DisplayPort Lane 1 (negative)
12	ML_LANE3_N	Output	DisplayPort Lane 3 (positive)
13	GND	--	Ground
14	GND	--	Ground
15	ML_LANE2_P	Output	DisplayPort Lane 2 (positive)
16	DDC_AUX_P	I/O	For DisplayPort, this is the AUX control channel (positive). For HDMI this is the DDC control channel Clock
17	ML_LANE2_N	Output	DisplayPort Lane 2 (negative)
18	DDC_AUX_N	I/O	For DisplayPort, this is the AUX control channel (negative). For HDMI, this is the DDC control channel Data.
19	GND	--	Ground
20	+3.3V	Output	3.3V power to DisplayPort. Tied to V3P3_S0 through a PTC

**Console Redirection**

The Liger board can be configured for remote access by redirecting the console to a serial communications port. The BIOS Setup utility and some operating systems (such as MS-DOS) can use this console for user interaction.

The default settings for the redirected console are 115.2 kbps, 8 data bits, 1 stop bit, no parity, and no flow control.

## Ethernet

The Liger features a standard Ethernet interface for 1000Base-T, 100Base-TX, and 10Base-T applications. Drivers are available to support a variety of operating systems. These interfaces are protected against ESD damage.

### Ethernet Connectors

Two Ethernet interfaces are provided at connector location J4. The I219 Ethernet controller (Ethernet 0) and I210-IT Ethernet controller (Ethernet 1) auto-negotiate connection speed. VersaLogic cable VL-CBR-1604 adapts the 8-pin Ethernet connector to an RJ-45 connector. The tables below list the pinout of the Ethernet connectors.

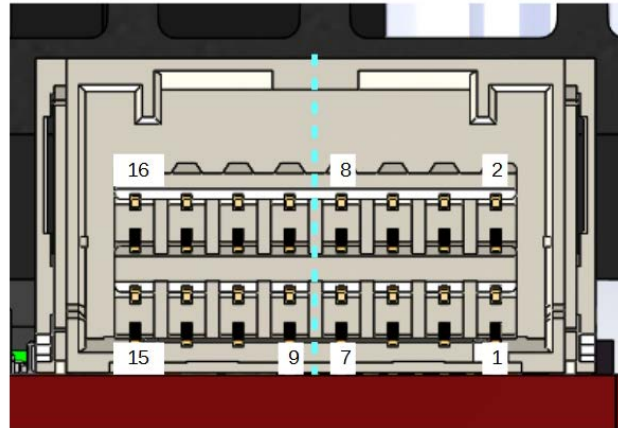
**Table 15. Ethernet 0 Connector Pinout**

J4 Pin	10/100 Signal Name	10/100/1000 Signal Name	VL-CBR-1604 RJ-45 Pin
1	- Auto Switch (Tx or Rx)	BI_DD-	8
2	+ Auto Switch (Tx or Rx)	BI_DD+	7
3	- Auto Switch (Tx or Rx)	BI_DB-	6
4	+ Auto Switch (Tx or Rx)	BI_DB+	3
5	- Auto Switch (Tx or Rx)	BI_DC-	5
6	+ Auto Switch (Tx or Rx)	BI_DC+	4
7	- Auto Switch (Tx or Rx)	BI_DA-	2
8	+ Auto Switch (Tx or Rx)	BI_DA+	1

**Table 16. Ethernet 1 Connector Pinout**

J4 Pin	10/100 Signal Name	10/100/1000 Signal Name	VL-CBR-1604 RJ-45 Pin
9	- Auto Switch (Tx or Rx)	BI_DD-	8
10	+ Auto Switch (Tx or Rx)	BI_DD+	7
11	- Auto Switch (Tx or Rx)	BI_DB-	6
12	+ Auto Switch (Tx or Rx)	BI_DB+	3
13	- Auto Switch (Tx or Rx)	BI_DC-	5
14	+ Auto Switch (Tx or Rx)	BI_DC+	4
15	- Auto Switch (Tx or Rx)	BI_DA-	2
16	+ Auto Switch (Tx or Rx)	BI_DA+	1

Figure 17. Ethernet Connector Pinout



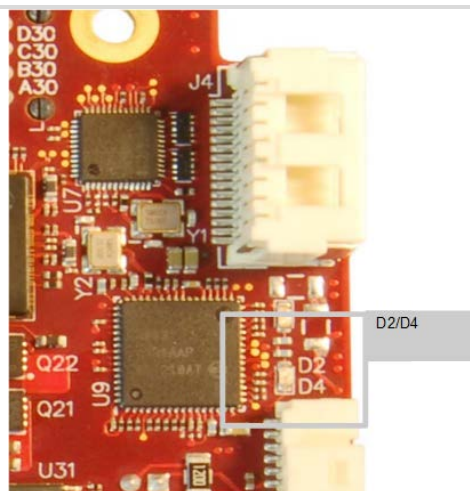
**Ethernet Status LED**

An On-board status LED is provided at location D4 (single green). The table below lists the states of the Ethernet status LED. The next figure shows the location of the Ethernet status LEDs.

Table 17. Ethernet Status LEDs

LED	Ref Des	State	Description
Green (Activity)	D2	On	Cable connected (pulses with activity)
		Off	Cable not connected
Green (Activity)	D4	On	Cable connected (pulses with activity)
		Off	Cable not connected

Figure 18. Location of Ethernet Status LED



## SATA Port

The Liger provides a latching SATA connector.

**Table 18. SATA Port Pinout**

Pin	Signal	Direction
1	Signal Ground	--
2	SATA0_TX_P	Out
3	SATA0_TX_N	Out
4	Signal Ground	--
5	SATA0_RX_N	In
6	SATA0_RX_P	In
7	Signal Ground	--

## PCIe Mini Card / mSATA

The mini PCIe/mSATA socket accepts a full-height PCI Express Mini Card or an mSATA module.

The PCIe Mini Card interface includes one PCIe x1 lane, one USB 2.0 channel, and the SMBus interface. The socket is compatible with plug-in Wi-Fi modems, GPS receivers, Flash data storage, and other cards for added flexibility. An Intel Centrino Advanced-N 6205 Wireless Express Mini Card (VL-MPEe-W2) is available from VersaLogic. A Wi-Fi antenna (VL-CBR-ANT01) and a 12-inch Wi-Fi card to bulkhead RP-SMA transition cable (VL-CBR-0201) are also available. For more information, contact [Sales@VersaLogic.com](mailto:Sales@VersaLogic.com).

The VL-MPEs-F1E series of mSATA modules provide flash storage of 4 GB, 16 GB, or 32 GB.

To secure a Mini Card or mSATA module to the on-board standoffs, use two M2.5 x 6mm pan head Philips nylon screws. These screws are available in quantities of 10 in the VL-HDW-108 hardware kit from VersaLogic.

**Table 19. PCIe Mini Card / mSATA Pinout**

J11 Pin	PCIe Mini Card Signal Name	PCIe Mini Card Function	mSATA Signal Name	mSATA Function
1	WAKE#	Wake	Reserved	Not connected
2	3.3VAUX	3.3V auxiliary source	+3.3V	3.3V source
3	NC	Not connected	Reserved	Not connected
4	GND	Ground	GND	Ground
5	NC	Not connected	Reserved	Not connected
6	1.5V	1.5V power	+1.5V	1.5V power
7	NC	Not connected	Reserved	Not connected
8	NC	Not connected	Reserved	Not connected
9	GND	Ground	GND	Ground
10	NC	Not connected	Reserved	Not connected
11	REFCLK-	Reference clock input –	Reserved	Not connected
12	NC	Not connected	Reserved	Not connected
13	REFCLK+	Reference clock input +	Reserved	Not connected



J11 Pin	PCIe Mini Card Signal Name	PCIe Mini Card Function	mSATA Signal Name	mSATA Function
14	NC	Not connected	Reserved	Not connected
15	GND	Ground	GND	Ground
16	NC	Not connected	Reserved	Not connected
17	NC	Not connected	Reserved	Not connected
18	GND	Ground	GND	Ground
19	NC	Not connected	Reserved	Not connected
20	W_DISABLE#	Wireless disable	Reserved	Not connected
21	GND	Ground	GND	Ground
22	PERST#	Card reset	Reserved	Not connected
23	PERn0	PCIe receive –	+B	Host receiver diff. pair +
24	3.3VAUX	3.3V auxiliary source	+3.3V	3.3V source
25	PERp0	PCIe receive +	-B	Host receiver diff. pair –
26	GND	Ground	GND	Ground
27	GND	Ground	GND	Ground
28	1.5V	1.5V power	+1.5V	1.5V power
29	GND	Ground	GND	Ground
30	SMB_CLK	SMBus clock	Two Wire I/F	Two wire I/F clock
31	PETn0	PCIe transmit –	-A	Host transmitter diff. pair –
32	SMB_DATA	SMBus data	Two Wire I/F	Two wire I/F data
33	PETp0	PCIe transmit +	+A	Host transmitter diff. pair +
34	GND	Ground	GND	Ground
35	GND	Ground	GND	Ground
36	USB_D-	USB data –	Reserved	Not connected
37	GND	Ground	GND	Ground
38	USB_D+	USB data +	Reserved	Not connected
39	3.3VAUX	3.3V auxiliary source	+3.3V	3.3V source
40	GND	Ground	GND	Ground
41	3.3VAUX	3.3V auxiliary source	+3.3V	3.3V source
42	LED_WWAN#	Wireless WAN LED	Reserved	Not connected
43	GND	mSATA detect ( <b>Note 1</b> )	GND/NC	Ground/not connected ( <b>Note 2</b> )
44	LED_WLAN#	Wireless LAN LED	Reserved	Not connected
45	NC	Not connected	Vendor	Not connected
46	LED_WPAN#	Wireless PAN LED	Reserved	Not connected
47	NC	Not connected	Vendor	Not connected
48	1.5V	1.5V power	+1.5V	1.5V power
49	Reserved	Reserved	DA/DSS	Device activity ( <b>Note 3</b> )
50	GND	Ground	GND	Ground
51	Reserved	Reserved	GND	Ground ( <b>Note 4</b> )
52	3.3VAUX	3.3V auxiliary source	+3.3V	3.3V source

**Notes:**

1. This pin is not grounded since it can be used to detect the presence of an mSATA module versus a PCIe Mini Card. Grounding this pin is available as an option on custom boards.
2. This pin is not grounded to make it available for mSATA module detection.

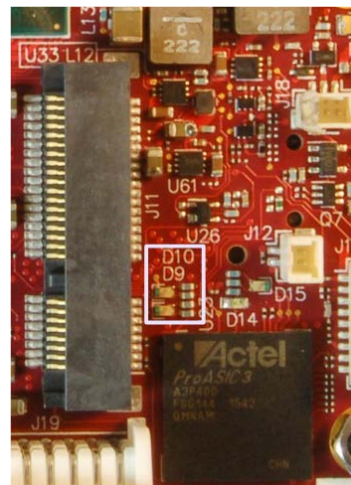
3. This signal drives the blue LED activity indicator. This LED activates with mSATA disk activity, if supported by the mSATA module.
4. Some PCIe modules use this signal as a second Mini Card wireless disable input. This signal is available for use for mSATA versus PCIe Mini Card detection. There is an option in BIOS setup for setting the mSATA detection method.

### PCIe Mini Card LEDs

Two dual-colored PCIe Mini Card LEDs are provided on the Liger at locations D8 and D9. The next table lists the states of the LEDs.

**Table 20. PCIe Mini Card LED States**

LED	Color	Status (when lit)
D9	Green	Activity on Wireless WAN (Note)
	Yellow	Activity on Wireless LAN (Note)
D10	Green	Activity on Wireless PAN (Note)
	Yellow	Illuminates when the 3.3 V power to the Mini Card is on. It alerts users to not hot-plug the Mini Card. By default, Mini Card power stays on when the processor is in sleep modes.



**Note:** These LEDs will illuminate when the associated device is installed and capable of transmitting. Their function is determined by the installed device.



#### **Integrator's Note:**

The 3.3 V power to the Mini Card can be controlled by the FPGA. By default, the power is always on, but there is a register setting that turns this power off in sleep modes. The 1.5 V power is always turned off in sleep modes.

# Expansion Interfaces

# 6

## SPX Expansion Bus

Up to two serial peripheral expansion (SPX) devices can be attached to the Liger at connector J17 using a VL-CBR-0901 cable. The SPX interface provides the standard serial peripheral interface (SPI) signals: SCLK, MISO, and MOSI, as well as two chip selects, SS0# – SS1#

The +5 V power provided to pin 1 of J17 is protected by a 1 A resettable fuse.

**Table 21. SPX Expansion Bus Pinout**

Pin	Signal/ Function	Direction	Description
1	VCC	Out	5V Power (S0 power in this product)
2	SCLK	Out	SPX Clock
3	GND	--	
4	MISO	In	Serial Data input
5	GND	--	
6	MOSI	Out	Serial Data output
7	GND	--	
8	SS0#	Out	Chip Select 0 (low true)
9	SS1#	Out	Chip Select 1 (low true)

SPI is, in its simplest form, a three wire serial bus. One signal is a clock, driven only by the permanent master device on-board. The others are Data In and Data Out with respect to the master. The SPX implementation adds additional features, such as chip selects. The master device initiates all SPI transactions. A slave device responds when its chip select is asserted and it receives clock pulses from the master.

The SPI clock rate can be software configured to operate at speeds between 0.75 MHz and 6 MHz. Because this clock is divided from a 24Mhz LPC clock. All four common SPI modes are supported through the use of clock polarity and clock idle state controls.

## PC/104-Plus Expansion Bus

The EPM-43 provides a legacy stack-down PCI connector at locations J1 (for PCI) and J2 (for ISA) on the bottom side of the board for PC/104-Plus (PCI +ISA) as well as PCI-104 (PCI only) and PC/104 (ISA only) expansion modules.

### Integrator's Notes:

- PC/104 ISA only modules (those that have no PCI connector) must be positioned below the PC/104-Plus (PCI+ISA) modules in the stack.
- Modules with PCI interfaces must be above those with only ISA interfaces.
- PCI-104 PCI only modules (those with no ISA connector) must be positioned below the PC/104-Plus (PCI+ISA) modules in the stack.
- In general, PC/104 (ISA only) and PCI-104 (PCI only) cards can never be used together in a stack.

The table below lists the maximum PC/104-Plus slot current rating on the EPM-43. This is the aggregate power available to both the PCI and ISA connectors. ISA does not use +3.3 V power, so all of the +3.3 V power is available for the PCI connector.

**Table 22: PCI/104-Plus Connector (PCI) Maximum Current**

Voltage	Maximum Current
+5 V	4.0 A
+3.3 V	3.0 A
+12 V	1.0 A
-12 V	0.5 A

### ISA Bus (on PC/104-Plus and PC/104 Expansion Modules)

Refer to the ISA sections of the [PC/104-Plus Specification](#) for a complete description of this interface.

The EPM-43 implements the ISA bus on PC/104-Plus and PC/104 expansion modules using an LPC-to-ISA bridge implemented in the FPGA. This LPC-to-ISA bridge supports all features except the following:

- The ISA bus must not be mastered by an external module. The EPM-43 is always the bus master. The MASTER signal on pin D17 of J2 is not connected.
- The REFRESH output signal on B19 of J2 is not supported; it is pulled up to a high logic level.
- DMA is not supported. The seven DACKx outputs on pins B15, B17, B26, D8, D10, D12, and D14 on J2 are pulled up to a high logic level. The seven DRQx inputs on pins B6, B16, B18, D9, D11, D13, and D15 on J10 are not connected. The Terminal Count (TC) output on pin B27 of J2 is pulled low.
- -5.0V power is not provided on J2 pin B5. This pin is not connected.

Most PC/104-Plus (PCI +ISA) or PC/104 (ISA only) expansion modules will work, but be sure to check the requirements of your PC/104 card against the list above.

## ISA I/O Support

Both 8-bit and 16-bit I/O cycles are supported, but for 16-bit cycles the PC/104 (ISA) module must be 16-bit capable and must assert IOCS16#.

The table below lists the I/O ranges available on the ISA bus unless there is a device claiming the range on the LPC or PCI bus. The FPGA on the EPM-43 uses I/O addresses 0xC80-0xCBF and, if enabled, the FPGA has two COM ports and three LPC I/O regions that can be configured in the BIOS Setup utility to map to various address ranges.

By default, the two COM ports in the FPGA are enabled and occupy the I/O address ranges of 0x3F8-0x3FF and 0x2F8-0x2FF. The following are the I/O address ranges available on the ISA bus when the BIOS is configured to factory defaults.

**Table 23: Available ISA Bus I/O Ranges**

- |           |             |
|-----------|-------------|
| ▪ 2E - 2F | ▪ 98        |
| ▪ 4E - 4F | ▪ 9C - 9E   |
| ▪ 62      | ▪ C00 - C7F |
| ▪ 66      | ▪ CD0 - CF8 |
| ▪ 90      | ▪ CFA - CFB |
| ▪ 94 - 96 |             |

Assuming the COM ports in the FPGA are disabled, the available I/O base addresses for COM ports on the ISA bus are as follows:

- |         |         |         |
|---------|---------|---------|
| ▪ 0x200 | ▪ 0x228 | ▪ 0x338 |
| ▪ 0x208 | ▪ 0x238 | ▪ 0x3E8 |
| ▪ 0x220 | ▪ 0x2E8 | ▪ 0x3F8 |

Each COM port in the FPGA that is enabled will use one of these I/O base addresses and, in that case, that 8 byte I/O range will not be available on the ISA bus. PCI devices may be assigned I/O space, but that usually occurs at I/O address 0x1000 or higher so as to not conflict with legacy I/O devices.

## ISA Memory Support

The following memory addresses can be enabled in BIOS on the ISA bus:

- 0xD0000-DFFFF

### **ISA IRQ Support**

The following IRQs are supported on the ISA bus:

- IRQ3      ▪ IRQ9
- IRQ4      ▪ IRQ10
- IRQ5      ▪ IRQ11
- IRQ6      ▪ IRQ12
- IRQ7      ▪ IRQ15

Each of the IRQs must be enabled in the BIOS Setup utility before they can be used. (All are disabled by default.)

Because ISA IRQ sharing is not supported, IRQs may not be available to the ISA bus due to operating system limitations.

### **PCI Bus (on PC/104-Plus and PCI-104 Expansion Modules)**

Refer to the PCI sections of the [PC/104-Plus Specification](#) for a complete description of this interface.

Make sure to correctly configure the PCI slot position jumpers on each PC/104-Plus or PCI-104 module appropriately.

The BIOS automatically allocates I/O, memory, and interrupt resources.

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# Thermal Considerations

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This chapter discusses the following topics related to thermal issues:

- Selecting the correct thermal solution for your application (begins below)
- EPM-43 thermal characterization (begins on page 44)
- Installing the passive (HDW-406 heat sink) and active (HDW-413 Heat sink + fan) thermal solutions available from VersaLogic (begins on page 47)

## Selecting the Correct Thermal Solution for Your Application

This section provides guidelines for the overall system thermal engineering effort.

### Heat Plate

The heat plate supplied with the Liger is the basis of the thermal solution. The heat plate draws heat away from the CPU chip as well as other critical components such as the power supply / management unit, the PCIe-to-PCI Bridge, and the Ethernet interfaces. Other components rely on the ambient air temperature being maintained at or below the maximum specified 85°C.

The heat plate is designed with the assumption that the user's thermal solution will maintain the top surface of the heat plate at 90 °C or less. If that temperature threshold is maintained, the CPU (and the other noted components) will remain safely within their operating temperature limits.



#### **CAUTION:**

By itself, the heat plate is not a complete thermal solution. Integrators should either implement a thermal solution using the accessories available from VersaLogic or develop their own thermal solution that attaches to the heat plate, suitable for environments in which the EPM-43 will be used. As stated above, any thermal solution must be capable of keeping the top surface of the heat plate at or below 90°C and the air surrounding the components in the assembly at or below 85 °C.

The heat plate is permanently affixed to the Liger and must not be removed. Removal of the heat plate voids the product warranty. Attempting to operate the Liger without the heat plate voids the product warranty and can damage the CPU.

### System-level Considerations

The EPM-43 thermal solutions – either the HDW-406 heat sink alone or with the HDW-413 heat sink + fan – are part of the larger thermal system of the application. Other PC/104 boards stacked under the Liger and any other nearby heat sources (power supplies or other circuits), all contribute to how the EPM-43 will perform from a thermal standpoint.

The ambient air surrounding the EPM-43 needs to be maintained at 85°C or below. This can prove to be challenging depending on how and where the EPM-43 is mounted in the end user system. Standard methods for addressing this requirement include the following:

- Provide a typical airflow of 100 linear feet per minute (LFM) / 0.5 linear meters per second (as described in the section titled EPM-43 Thermal Characterization, beginning on page 44) within the enclosure
- Position the EPM-43 board to allow for convective airflow
- Lower the system level temperature requirement as needed

The decision as to which thermal solution to use can be based on several factors including (but not limited to) the following:

- Number of CPU cores in the SoC (single, dual, or quad)
- CPU core program utilization
- Temperature range within which the EPM-43 will be operated
- Air movement (or lack of air movement)
- Video processing intensity
- Memory access demands
- High speed I/O usage (PCIe, USB 3.0, SATA usage)

Most of these factors involve the demands of the user application on the EPM-43 and cannot be isolated from the overall thermal performance. Due to the interaction of the user application, the Liger thermal solution, and the overall environment of the end system, thermal performance cannot be rigidly defined.



### CPU Thermal Trip Points

The CPU cores in the Liger have their own thermal sensors. Coupled with these sensors are specific reactions to four thermal trip points. The table below describes the four thermal trip points.

**Table 24. CPU Thermal Trip Points**

Trip Point	Description
Active (Note 1)	The fan is turned on when this temperature is reached
Passive (Note 2)	At this temperature, the CPU cores throttle back to a lower speed. This reduces the power draw and the temperature.
Critical (Note 3)	At this temperature, the operating system typically puts the board into a sleep or other low-power state.
Maximum core temperature	The CPU turns itself off when this temperature is reached. This is a fixed trip point and cannot be adjusted.

**Notes:**

1. The default value in the BIOS Setup utility for this trip point is 55°C.
2. The default value in the BIOS Setup utility for this trip point is 105°C.
3. The default value in the BIOS Setup utility for this trip point is 110°C.

These trip points allow maximum CPU operational performance while maintaining the lowest CPU temperature possible. The long-term reliability of any electronic component is degraded when it is continually run near its maximum thermal limit. Ideally, the CPU core temperatures would be kept well below 100°C with only brief excursions above.

CPU temperature monitoring programs are available to run under both Windows and Linux. The table below lists some of these hardware monitoring programs.

**Table 25. Temperature Monitoring Programs**

Operating System	Program Type	Description
Windows	Core Temperature	<a href="http://www.alcpu.com/CoreTemp/">http://www.alcpu.com/CoreTemp/</a>
	Hardware Monitor	<a href="http://www.cpubid.com/software/hwmonitor.html">http://www.cpubid.com/software/hwmonitor.html</a>
	Open Hardware Monitor	<a href="http://openhardwaremonitor.org/">http://openhardwaremonitor.org/</a>
Linux	lm-sensors	<a href="http://en.wikipedia.org/wiki/Lm_sensors">http://en.wikipedia.org/wiki/Lm_sensors</a>

## Thermal Specifications, Restrictions, and Conditions

Graphical test data is in the section titled EPM-43 Thermal Characterization, beginning on page 44. Refer to that section for the details behind these specifications. These specifications are the thermal limits for using the EPM-43 with one of the defined thermal solutions.

Due to the unknown nature of the entire thermal system, or the performance requirement of the application, VersaLogic cannot recommend a particular thermal solution. This information is provided for user guidance in the design of their overall thermal system solution.

**Table 26. Absolute Minimum and Maximum Air Temperatures**

Board	With Heat Plate	With Heat Sink (HDW-406)	With Heat Sink + Fan (HDW-413)
VL-EPM-43EAP	-40° to +85 °C	-40° to +85°C	-40° to +85°C
VL-EPM-43EBP	-40° to +85°C	-40° to +85°C	-40° to +85°C
VL-EPM-43ECP	-40° to +85°C	-40° to +85°C	-40° to +85°C

### Overall Restrictions and Conditions

- Ranges shown assume less than 90% CPU utilization.
- Keep the maximum CPU core temperature below 100°C.
- The ambient air surrounding the EPM-43 needs to be maintained at 85°C or below. This includes the space between this CPU board and any board it is stacked on top of it. Included is the space beneath an installed mini PCIe expansion board and the installed SODIMM. A recommended overall air flow of 100 Linear Feet per Minute (LFM) / 0.5 Linear Meters per Second (LMS) addresses this requirement. If this air flow is not provided, other means to keep the adjacent air at 85°C or below must be implemented.

### Heat Plate Only Restrictions and Conditions:

- The heat plate must be kept below 90°C. This applies to a heat plate mounted directly to another surface.

### Heat Sink Only Considerations:

- At 85°C air temperature and 90% CPU utilization, there will be little – if any – thermal margin to a CPU core temperature of 100°C or the passive trip point (see test data). If this is the use case, consider adding a fan or other additional airflow.

### Heat Sink with Fan Considerations:

- The heat sink and fan combination cools the CPU when it is running in high temperature environments, or when the application software is heavily utilizing the CPU or video circuitry. The fan assists in cooling the heat sink and provides additional air movement within the system.



#### Integrator's Note:

The ambient air surrounding the EPM-43 needs to be maintained at 85°C or below.

## EPM-43 Thermal Characterization

The EPM-43 board underwent the following thermal characterization tests:

- Test Scenario 1: Dual core EPM-43EAP (Core i3 processor) with passive and active thermal solutions
- Test Scenario 2: Dual core EPM-43EBP (Core i5 processor) with passive and active thermal solutions
- Test Scenario 3: Dual core EPM-43ECP (Core i7 processor) with passive and active thermal solutions
- The table below describes the thermal testing setup for the board.

**Table 27. EPM-43 Thermal Testing Setup**

<b>Hardware Configuration</b>	EPM-43 (Liger) dual core CPU with: <ul style="list-style-type: none"> <li>▪ 8 GB of DDR3 DRAM</li> <li>▪ HDW-413 (heat sink and fan)</li> <li>▪ One attached DisplayPort device</li> <li>▪ Two RS-232 ports in loopback configuration</li> <li>▪ Two active Ethernet ports</li> <li>▪ Three USB 2.0 ports in loopback configuration</li> </ul>
<b>BIOS</b>	<ul style="list-style-type: none"> <li>▪ ID string: Liger_3.1.0.334.r1.01</li> <li>▪ Passive thermal trip point setting: 105°C</li> <li>▪ Critical thermal trip point setting: 110°C</li> </ul>
<b>Operating System</b>	<ul style="list-style-type: none"> <li>▪ Microsoft Windows* 10 Enterprise</li> </ul>
<b>Test Software</b>	<ul style="list-style-type: none"> <li>▪ Passmark* BIT v8.1 Pro               <ul style="list-style-type: none"> <li>- CPU utilization ~90%</li> </ul> </li> <li>▪ Intel Thermal Analysis Tool* (TAT) v5.0.1026               <ul style="list-style-type: none"> <li>- Primarily used to read the CPU core temperature</li> </ul> </li> </ul>
<b>Test Environment</b>	<ul style="list-style-type: none"> <li>▪ Thermal chamber</li> </ul>

The test results reflect the test environment within the temperature chamber used. This particular chamber has an airflow of about 0.5 meters per second (~100 linear feet per minute). Thermal performance can be greatly enhanced by increasing the overall airflow beyond 0.5 meters per second.

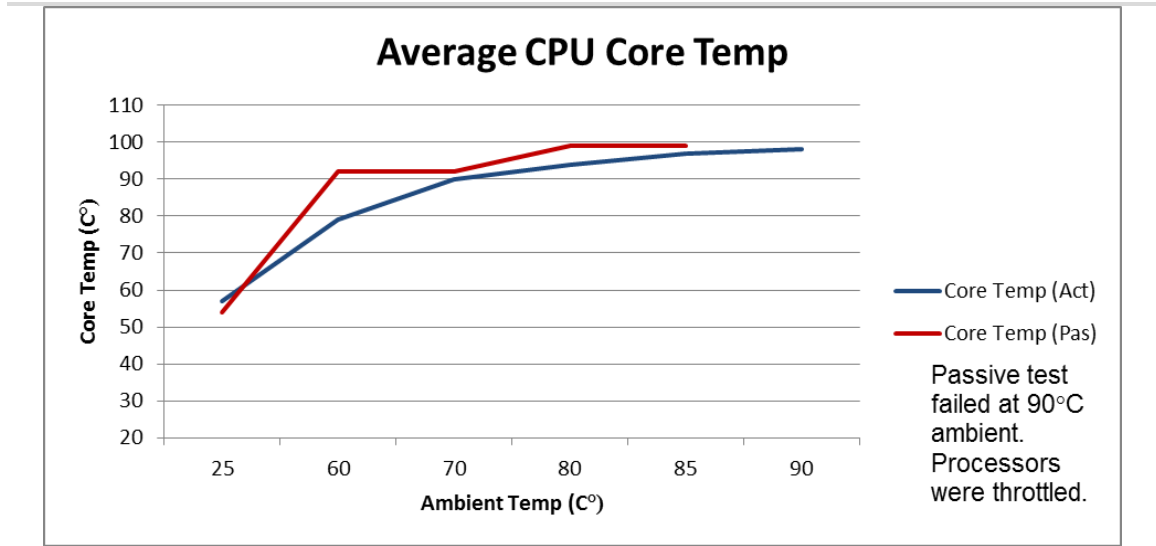
The system power dissipation is primarily dependent on the application program - that is, its use of computing or I/O resources. The stress levels used in this testing are considered to be at the top of the range of a typical user's needs.

**Test Results**

**Test Scenario 1: Dual Core EPM-43EAP - Passive and Active Performance**

The figure below shows the thermal performance of the EPM-43EAP using the Core i3 processor.

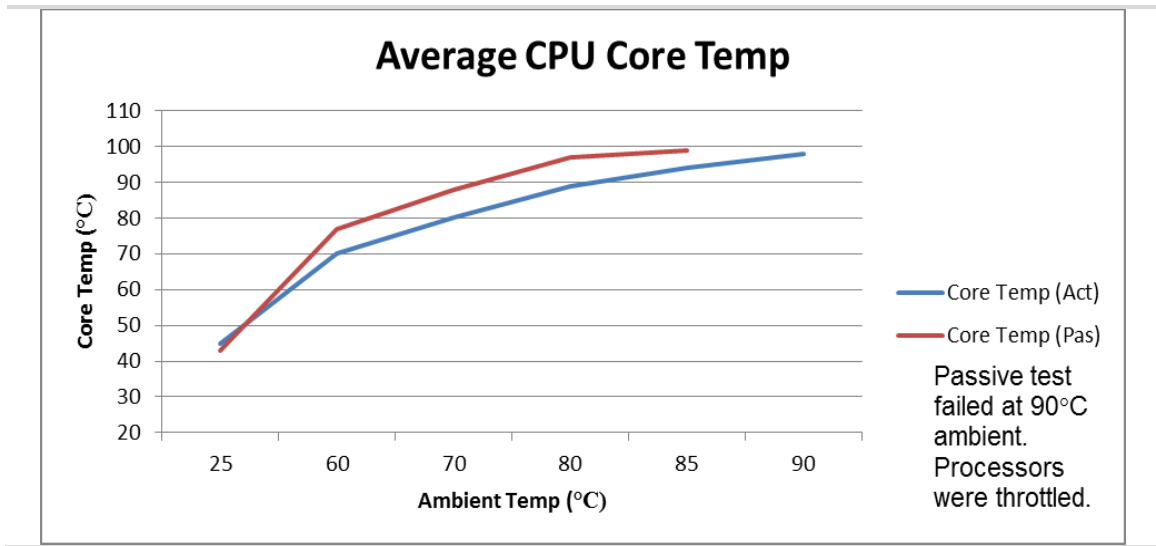
**Figure 19. EPM-43EAP CPU Core Temperature Relative to Ambient Temperature**



**Test Scenario 2: Dual Core EPM-43EBP - Passive and Active Performance**

This figure shows the thermal performance of the EPM-43EBP using the Core i5 processor.

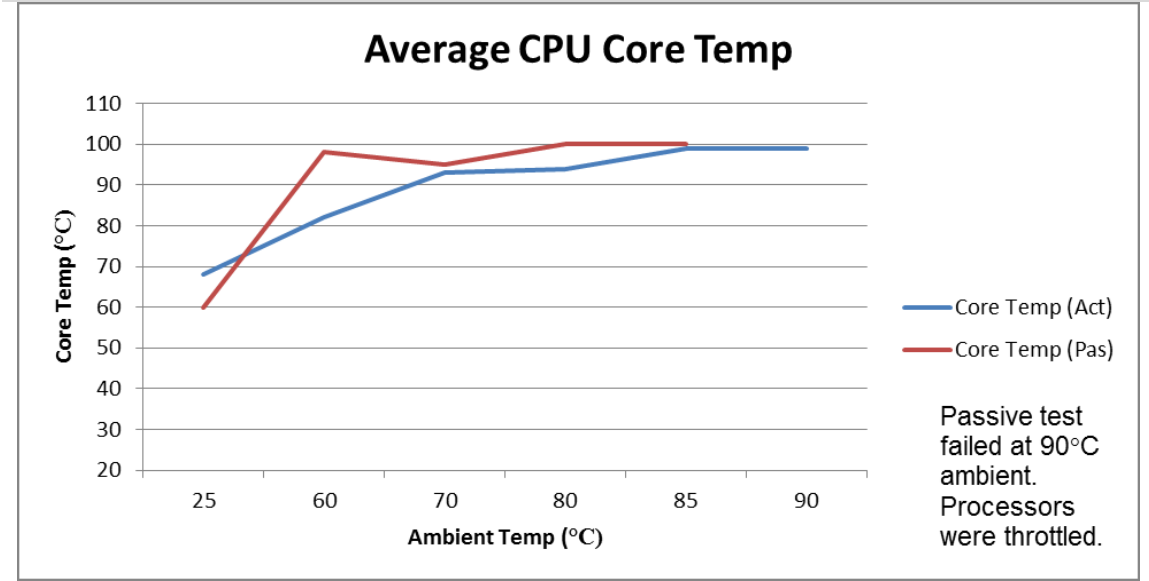
**Figure 20. EPM-43EBP CPU Core Temperature Relative to Ambient Temperature**



**Test Scenario 3: Dual Core EPM-43ECP - Passive and Active Performance**

The active and passive performance of the Core i7 version of the Liger will typically require a heat sink + fan for operation above 80°C, at >90% CPU utilization.

**Figure 21. EPM-43ECP CPU Core Temperature Relative to Ambient Temperature**



## Installing the VersaLogic Thermal Solutions

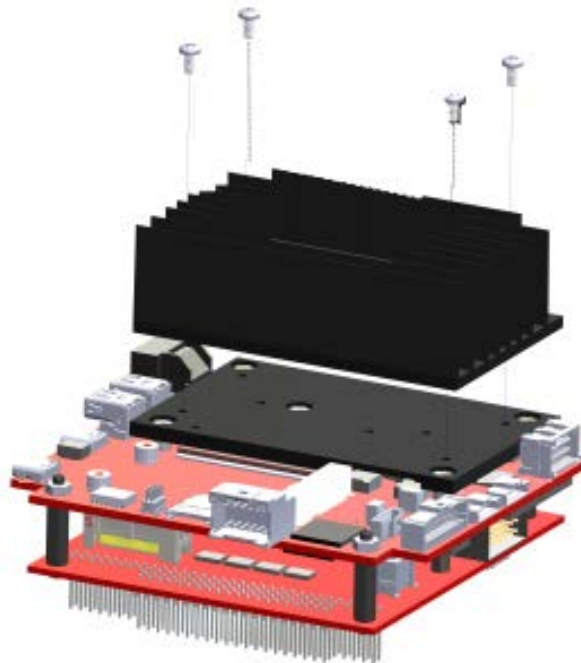
The following thermal solution accessories are available from VersaLogic:

- VL-HDW-401 Thermal Compound Paste - used to mount the heat sink to the heat plate
- VL-HDW-406 Passive Heat Sink
- VL-HDW-413 Passive Heat Sink/Fan kit – mounts to standard product.
- VL-HDW-408 Heat Pipe Block.

### Installing the Passive Heat Sink

Figure 22. Thermal Heat Sink Solution Installation

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Install the passive heat sink (VL-HDW-406) using these steps:

#### 1. Apply the Arctic Silver<sup>®</sup> Thermal Compound

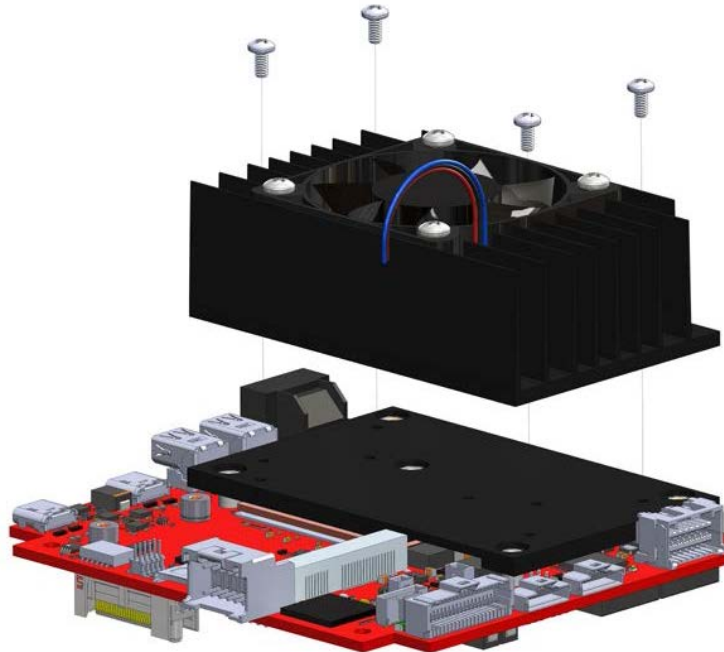
- Apply the thermal compound to the heat plate using the method described on the Arctic Silver website - <http://www.arcticsilver.com/>

#### 2. Position the passive heat sink

- Using the figure above as a guide, align the four mounting holes of the heat sink with the heat plate.

#### 3. Secure the passive heat sink to the heat plate

- Affix the passive heat sink to the heat plate using four M2.5 pan head screws.
- Using a torque screwdriver, tighten the screws to 4.0 inch-pounds.

**Figure 23. Thermal Fan Solution Installation**

### Installing the Heat Sink Fan

Install the heat sink and fan (VL-HDW-413) using these steps:

#### 1. Apply the Arctic Silver<sup>®</sup> Thermal Compound

- Apply the thermal compound to the heat plate using the method described on the Arctic Silver website - <http://www.arcticsilver.com/>

#### 2. Position the fan assembly

- Using the figure above as a guide, align the mounting holes of the heat sink fan with the four holes in the passive heat sink. Position the fan so that its power cable is on the side nearest the J18 CPU fan connector.

#### 3. Secure the fan to the heat sink

- Affix the heat sink fan using four M3 pan head screws.
- Using a torque screwdriver, tighten the screws to 4.0 inch-pounds.

#### 4. Connect power to the fan

- Connect the fan's power cable to the J18 CPU fan connector on the Liger board.

# Appendix A – References

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## Processor

- i7-7600U (dual core) – 4 MB Cache - [Specifications](#)
- i5-7300U (dual core) – 3 MB Cache - [Specifications](#)
- i3-7100U (dual core) – 3 MB Cache - [Specifications](#)

## Ethernet Controller

- *Intel I210-IT Gigabit Ethernet Controller* - [Intel I210-IT Datasheet](#)
- *Intel I219-IT Gigabit Ethernet Controller* - [Intel I219-IT Datasheet](#)
- *PC/104-Plus* - [PC/104-Plus Specification](#)



## KNOWN ISSUES

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### Hardware

- Power – maintain >5V input power...optimal is 5.1V +/- 2%
- CPU fan does not turn off at low temperatures.
- Sometimes hangs when entering S3 sleep.

### Operating Systems

- Windows 7 – SD card not currently usable
- Windows 7 – Special install steps required to install since Windows 7 install does not support xHCI and Liger only supports xHCI.