User's Guide

TMUXRUM-RRPEVM User's Guide

ABSTRACT

This document is the EVM user's guide for the TMUXRUM-RRPEVM, which provides a quick way to evaluate TI devices that use a 16-pin RUM or RRP package.

Table of Contents

List of Figures

List of Tables

Trademarks

1 Introduction

This user's guide describes the TMUXRUM-RRPEVM evaluation module (EVM) and its intended use. This board allows for the quick prototyping and DC characterization of TI's line of TMUX products that use 16-pin QFN packages (RUM or RRP).

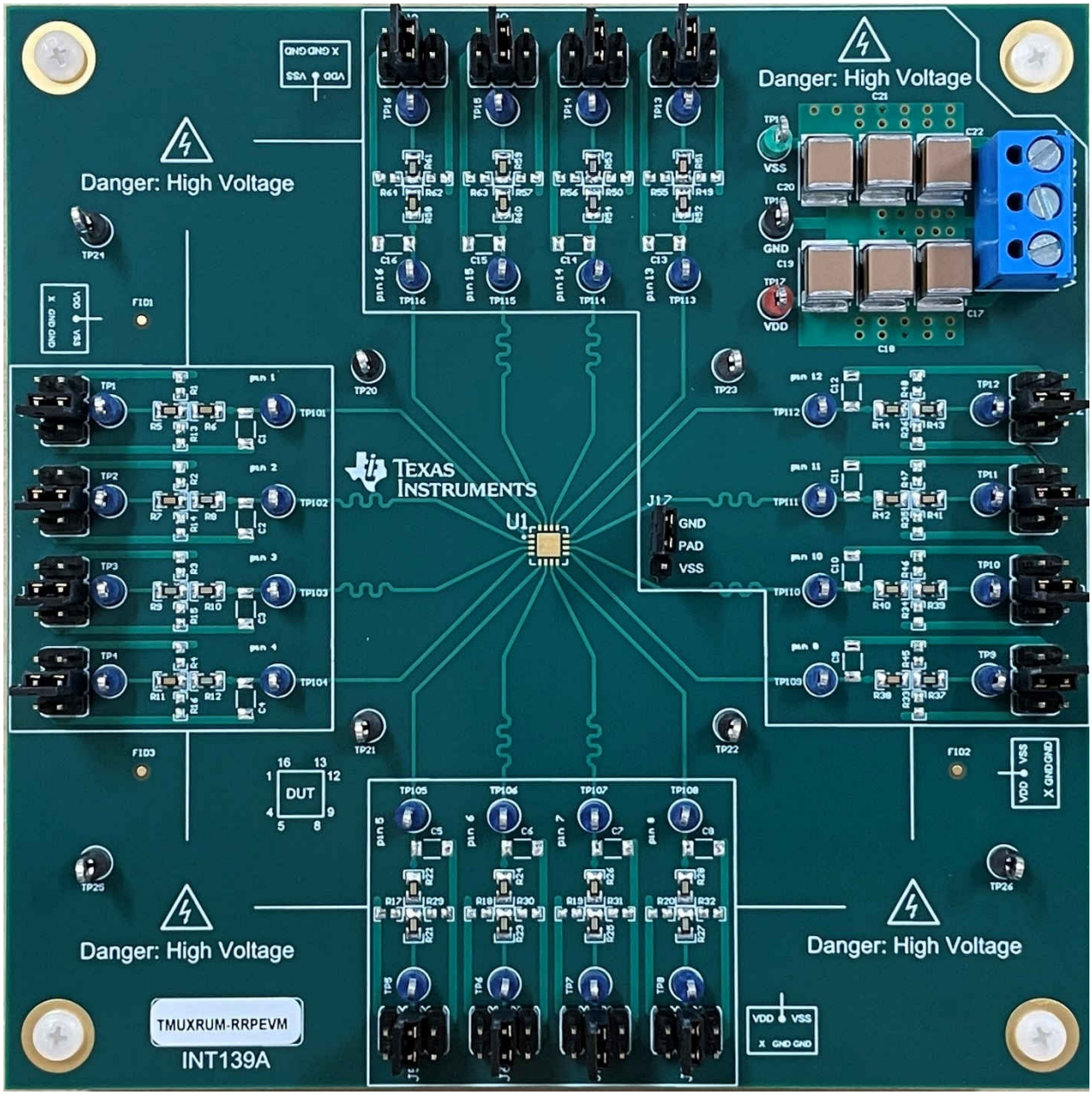

Figure 1-1. TMUXRUM-RRPEVM Top View

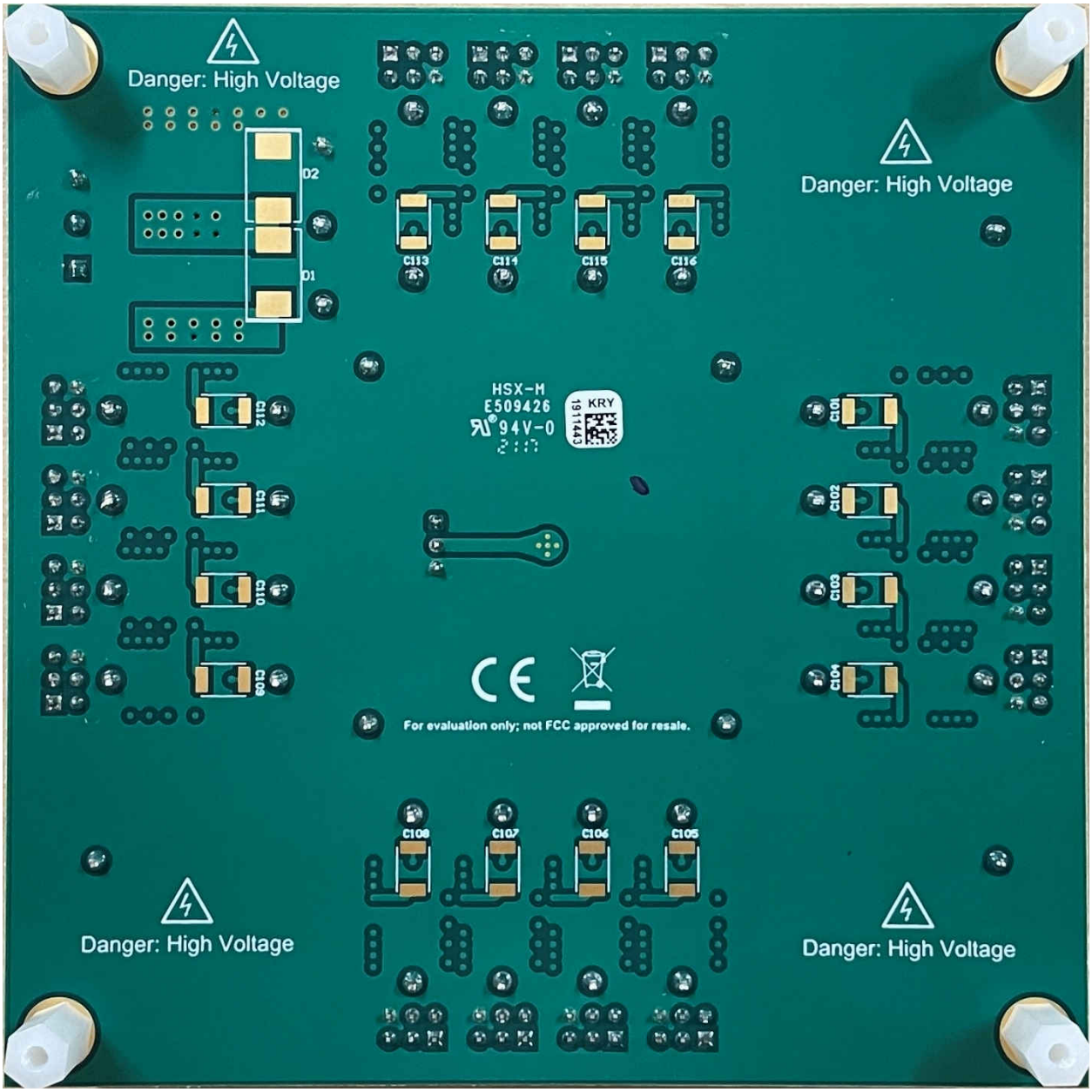

Figure 1-2. TMUXRUM-RRPEVM Bottom View

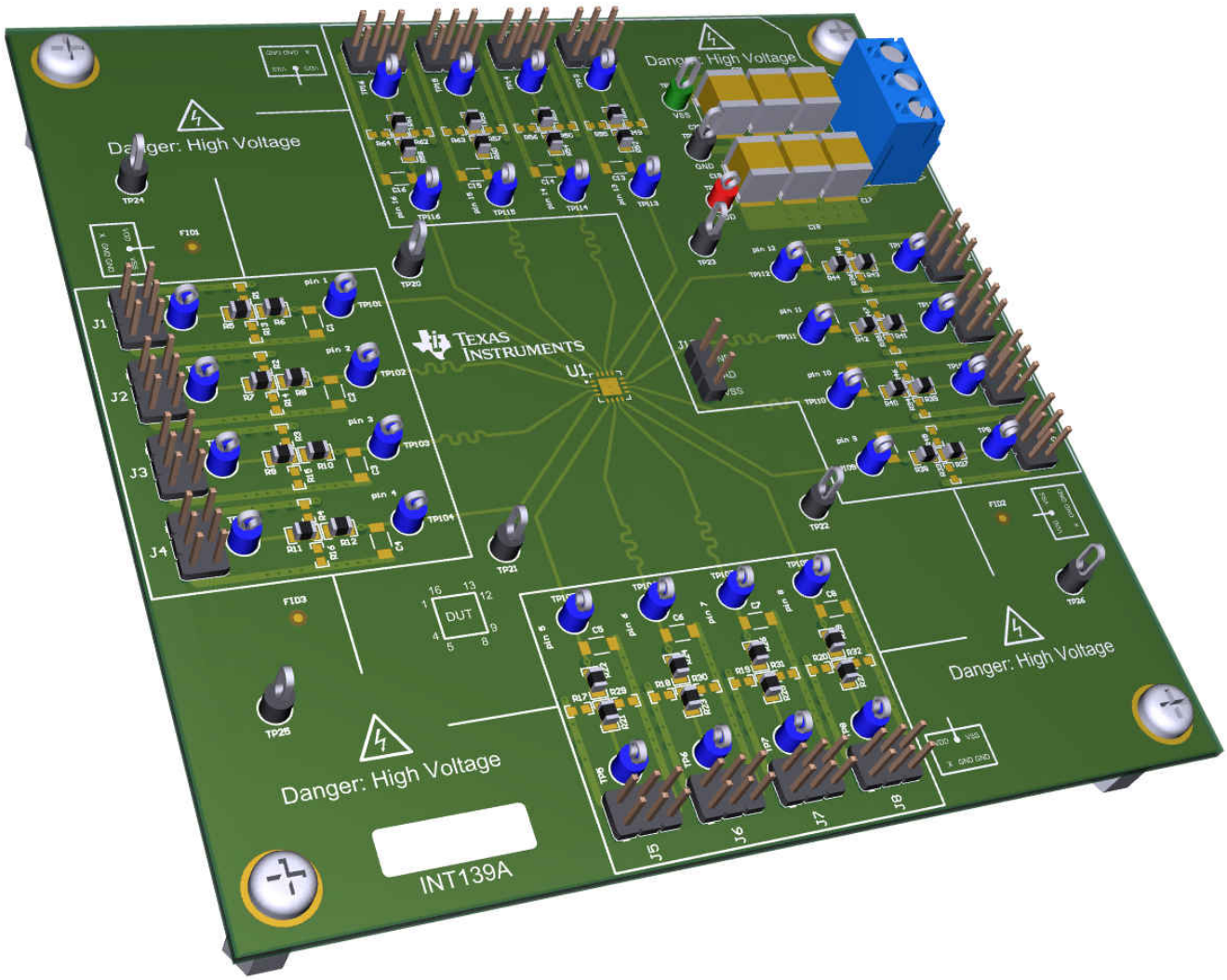

Figure 1-3. TMUXRUM-RRPEVM 3D View

2 General Texas Instruments High Voltage Evaluation Module (TI HV EVM) User Safety Guidelines

Always follow TI's setup and application instructions, including use of all interface components within their recommended electrical rated voltage and power limits. Always use electrical safety precautions to help ensure your personal safety and those working around you. Contact TI's Product Information Center http://support/ti./com for further information.

Save all warnings and instructions for future reference.

> **WARNING**
> Failure to follow warnings and instructions may result in personal injury, property damage or death due to electrical shock and burn hazards.

The term TI HV EVM refers to an electronic product typically provided as an open framed, unenclosed printed circuit board assembly. It is *intended strictly for use in development laboratory environments, solely for qualified professional users having training, expertise and knowledge of electrical safety risks in development and application of high voltage electrical circuits. Any other use or application are strictly prohibited by Texas Instruments.* If you are not suitably qualified, you should immediately stop from further use of the HV EVM.

1. Work Area Safety
   a. Keep work area clean and orderly.
   b. One or more qualified observers must be present anytime circuits are energized.
   c. Effective barriers and signage must be present in the area where the TI HV EVM and its interface electronics are energized, indicating operation of accessible high voltages may be present, for the purpose of protecting inadvertent access.
   d. All interface circuits, power supplies, evaluation modules, instruments, meters, scopes and other related apparatus used in a development environment exceeding 50Vrms/75VDC must be electrically located within a protected Emergency Power Off EPO protected power strip.
   e. Use stable and nonconductive work surface.
   f. Use adequately insulated clamps and wires to attach measurement probes and instruments. No freehand testing whenever possible.
2. Electrical Safety
   As a precautionary measure, it is always a good engineering practice to assume that the entire EVM may have fully accessible and active high voltages.
   a. De-energize the TI HV EVM and all its inputs, outputs and electrical loads before performing any electrical or other diagnostic measurements. Revalidate that TI HV EVM power has been safely de-energized.
   b. With the EVM confirmed de-energized, proceed with required electrical circuit configurations, wiring, measurement equipment connection, and other application needs, while still assuming the EVM circuit and measuring instruments are electrically live.
   c. After EVM readiness is complete, energize the EVM as intended.

   > **WARNING**
   > While the EVM is energized, never touch the EVM or its electrical circuits, as they could be at high voltages capable of causing electrical shock hazard.
3. Personal Safety
   a. Wear personal protective equipment (for example, latex gloves or safety glasses with side shields) or protect EVM in an adequate lucent plastic box with interlocks to protect from accidental touch.

Limitation for safe use:

EVMs are not to be used as all or part of a production unit.

3 Information About Cautions and Warnings

The information in the warning statement is provided for personal protection and the information in the caution statement is provided to protect the equipment from damage. Read each caution and warning statement carefully.

CAUTION

This EVM contains components that can potentially be damaged by electrostatic discharge. Always transport and store the EVM in its supplied ESD bag when not in use. Handle using an antistatic wristband. Operate on an antistatic work surface. For more information on proper handling, see Electrostatic Discharge (ESD).

4 Features

The TMUXRUM-RRPEVM has the following features:

- 3 power supply decoupling capacitors from V_{DD} to GND (three 3.3 µF capacitors)
- 1 protection diode pad from V_{DD} to GND available near power supply (6.9 mm × 5.8 mm)
- 3 power supply decoupling capacitors from V_{SS} to GND (three 3.3 µF capacitors)
- 1 protection diode pad from V_{SS} to GND available near power supply (6.9 mm × 5.8 mm)
- Terminal block power supply connection
- DUT footprint compatible with 16-pin RUM and RRP (WQFN) packages
- 16 length-matched signal inputs corresponding to the 16 pins of the DUT
- Selectable connections to V_{DD}, V_{SS}, or GND for each signal input using 2.54 mm shunt
- Footprints for pull-up and pull-down resistors for each signal input (2 × 0603 footprint on each of 24 signals)
- Footprints for series resistors for each signal input (two 0805 footprints on each of 16 signals)
- Footprints for decoupling capacitors for each input (one 1206 footprint and one 1812 footprint on each of 16 signals)
- 2 test points for each signal input
- Selectable thermal pad connection
- Multiple GND test point connections around board

5 Header Connections and Test Points

There are 16 headers located around the board with designators J1 through J16. These 3-by-2 headers serve as connections to power planes and to signals of the DUT (U1). Each pin of the DUT has similar header and test point configuration. At four different locations around the board, a legend shows the connections of the pins of the nearby four headers. Figure 5-1 shows a representation of the header associated with pin 1 of U1.

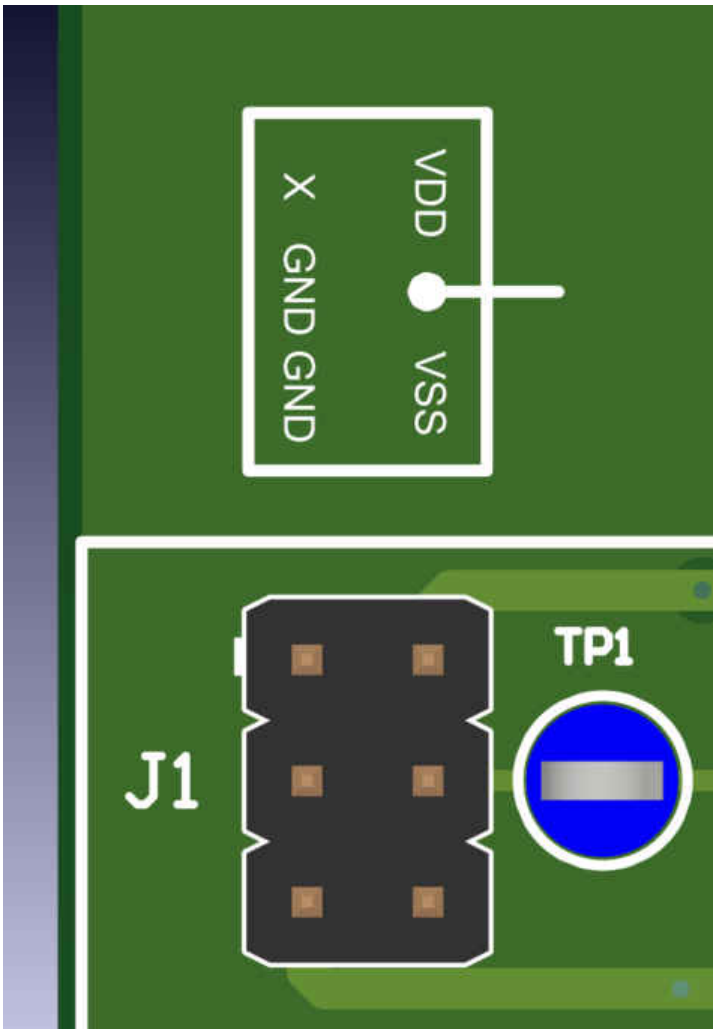

Figure 5-1. Header J1 for U1.1

The silkscreen legend represents the connections of the pins of J1. Figure 5-2 shows the pin numbers of this header from this same perspective.

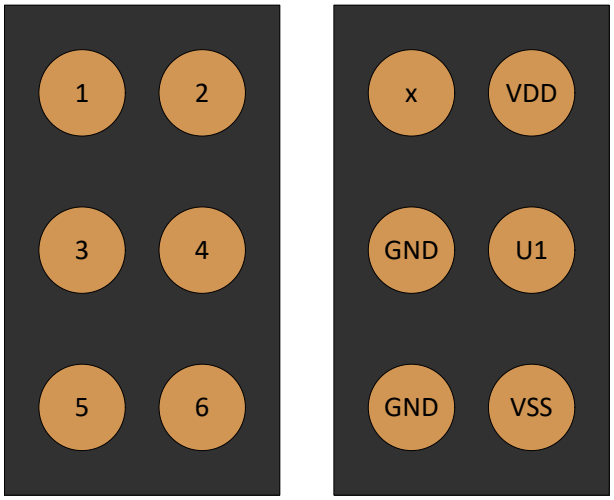

Figure 5-2. Pinout of Headers

Table 5-1 also shows the connections.

Table 5-1. Connections by Header Pin Number

Header pin number	Connection
1	No connection
2	V_{DD}
3	GND
4	U1
5	GND
6	V_{SS}

For all headers J1 through J16, the connections are the same, but are rotated by a multiple of 90° according to their position on the board. A legend is included for each rotation.

There is one 3-by-1 header located near the DUT (J17). Pin 2 of this header is connected to the thermal pad of the DUT. Pin 1 of this header is connected to GND, and pin 3 of this header is connected to V_{SS}.

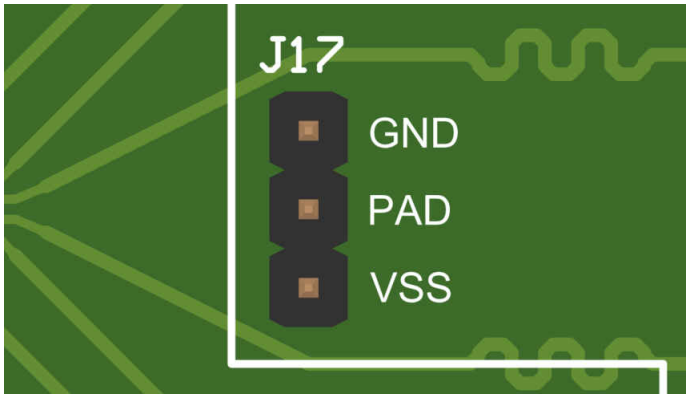

Figure 5-3. Thermal Pad Selector

The connections of J17 are also labeled on the board's silkscreen layer next to the header.

In addition to headers, multiple test points are located around the board. Black test points (TP18 and TP20-TP26) are connected to GND, the red test point (TP17) is connected to V_{DD}, and the green test point (TP19) is connected to V_{SS}. The remaining blue test points (TP1-TP16 and TP101-TP116) are connected along the signal paths of the pins of U1.

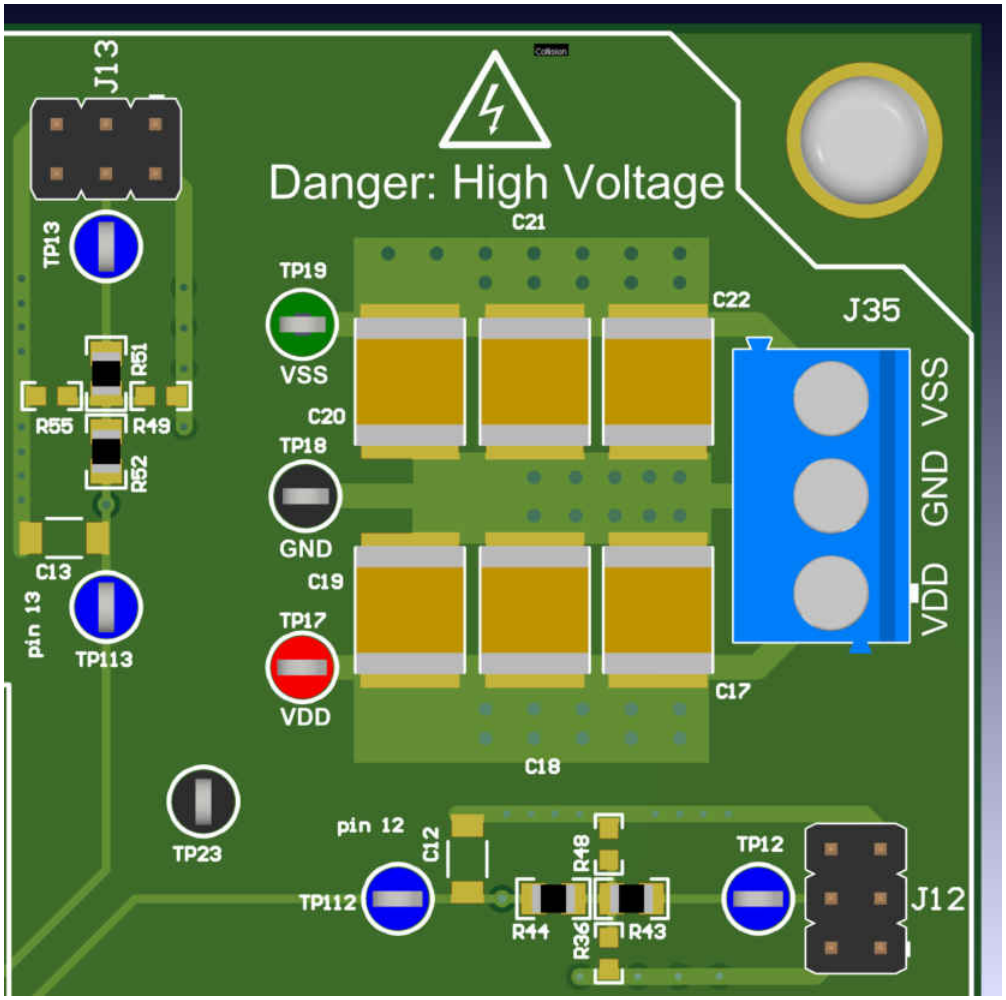

Figure 5-4. Test Point Colors

The last two digits of the blue test point number represent the pin with which the test point is associated. For example, TP16 and TP116 are both pin 16 of U1.

Table 5-2 shows the test point connections.

Table 5-2. Test Point Connections

Designator	Connection
TP1	J1.4
TP2	J2.4
TP3	J3.4
TP4	J4.4
TP5	J5.4
TP6	J6.4
TP7	J7.4
TP8	J8.4
TP9	J9.4
TP10	J10.4
TP11	J11.4
TP12	J12.4

Table 5-2. Test Point Connections (continued)

Designator	Connection
TP13	J13.4
TP14	J14.4
TP15	J15.4
TP16	J16.4
TP17	V_{DD}
TP18	GND
TP19	V_{SS}
TP20	GND
TP21	GND
TP22	GND
TP23	GND
TP24	GND
TP25	GND
TP26	GND
TP101	U1.1
TP102	U1.2
TP103	U1.3
TP104	U1.4
TP105	U1.5
TP106	U1.6
TP107	U1.7
TP108	U1.8
TP109	U1.9
TP110	U1.10
TP111	U1.11
TP112	U1.12
TP113	U1.13
TP114	U1.14
TP115	U1.15
TP116	U1.16

Terminal block J35 is the power input for the board. Three power rails (V_{SS}, GND, and V_{DD}) are labeled on the board's silkscreen layer, indicating the identities of the input pins of the header. Connect the power supply rails at this terminal block to power the board.

6 Setup

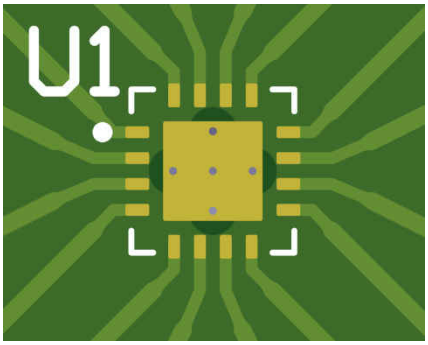

Figure 6-1. DUT Footprint U1

The TMUXRUM-RRPEVM will not have any device connected at footprint U1, and no devices are included with the EVM for this footprint. Attach any compatible Texas Instruments 16-pin TMUX device to this location, which will serve as the Device Under Test (DUT). Compatible devices include parts with RUM or RRP package names.

By default, the TMUXRUM-RRPEVM will have shunts on headers J1 through J16 connected such that the pins of U1 are connected to GND. Remove these shunts from J1 through J16 as necessary if these connections are not desired. Alternatively, the pins of U1 can be shorted to V_{DD} or V_{SS} by connecting between pin 4 of the header and one of the other pins on the header. Figure 5-2 and Table 5-1 includes detailed descriptions of the connections on J1 through J16.

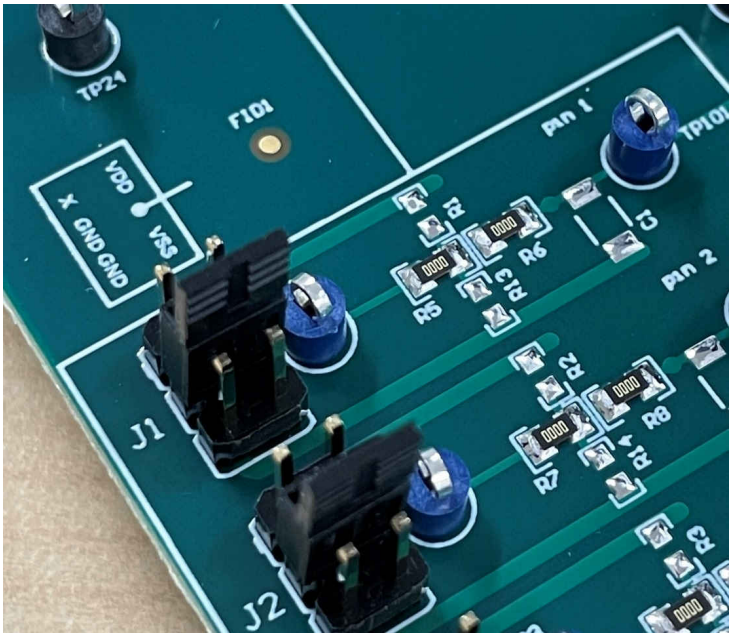

Figure 6-2. Signal Line Circuitry (3D)

As shown in Figure 6-2 and Figure 6-3 as R5 and R6 on the J1 (pin 1 of U1) signal line, the TMUXRUM-RRPEVM includes 0 Ω series resistors (0805 package) on each signal line.

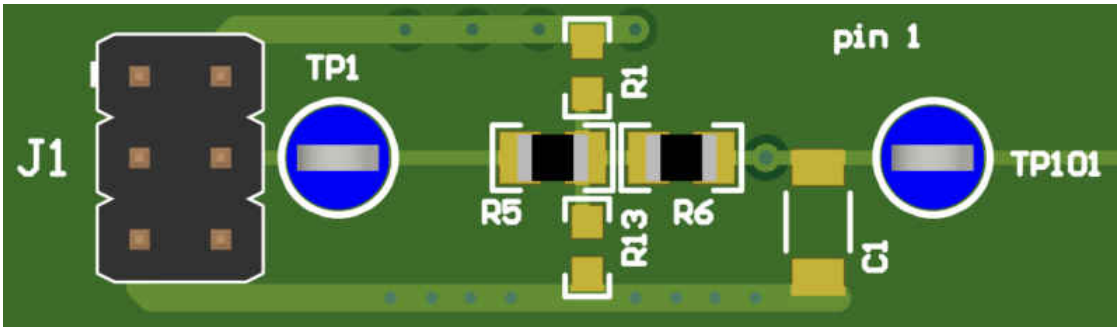

Figure 6-3. Signal Line Circuitry

These can be substituted for different resistors as desired. Additionally, there are pads for pull-up and pull-down resistors to V_{DD} and GND respectively. Add any 0603 resistor to the footprint shown as R1 to provide pull-up to V_{DD}, and add any 0603 resistor to the footprint shown as R13 to provide pull-down to GND.

Each signal line also includes two footprints that allow for the user to attach capacitors or other devices with matching footprints. On the top side of the board, shown in Figure 6-2 and Figure 6-3 as C1, a standard 1206 footprint exists between the U1 pin signal and the GND signal. The user can solder a capacitor to this footprint to provide capacitance to the signal line.

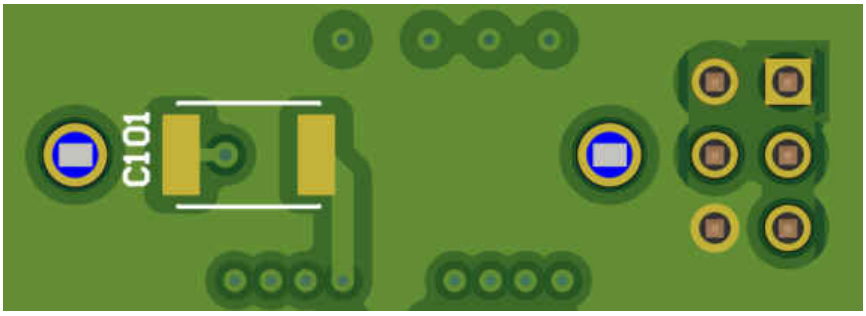

Figure 6-4. Signal Line Circuitry Bottom Layer

Figure 6-4 shows that a standard 1812 footprint exists as C101 on the backside of the board, which also allows a capacitor to be connected between the U1 pin signal and GND. The user can solder a capacitor to this footprint to provide capacitance to the signal line.

The user has the ability to select the connection of the thermal pad of U1 by using the three-by-one header located near U1 (J17).

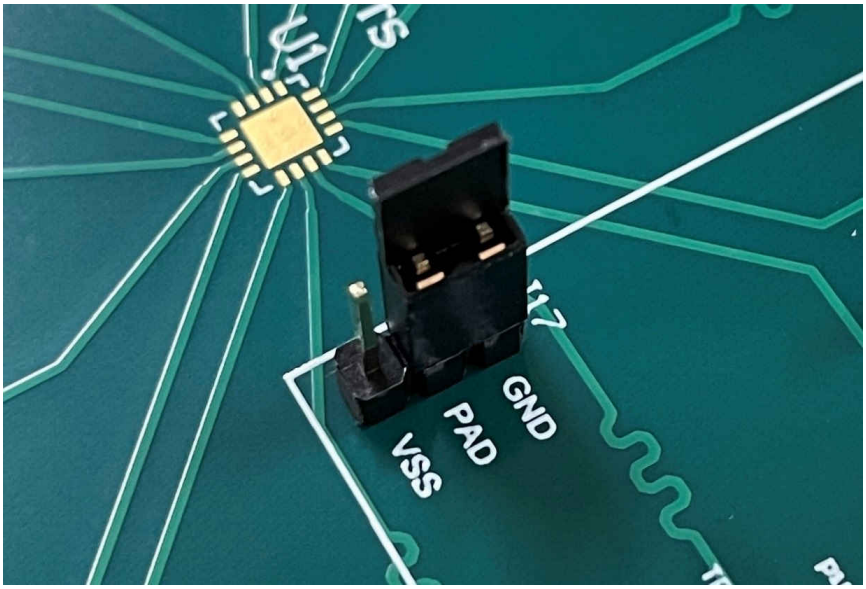

Figure 6-5. Thermal Pad Selector with Shunt

Connecting a shunt between pins 1 and 2 of this header will tie the thermal pad of U1 to GND, while connecting pins 2 and 3 will tie the thermal pad of U1 to V_{SS}. Leave pin 2 of this header unconnected to allow the thermal pad to float, or use an external connection to tie the thermal pad to any other potential.

7 Layout

Figure 7-1 shows the layout of the EVM PCB.

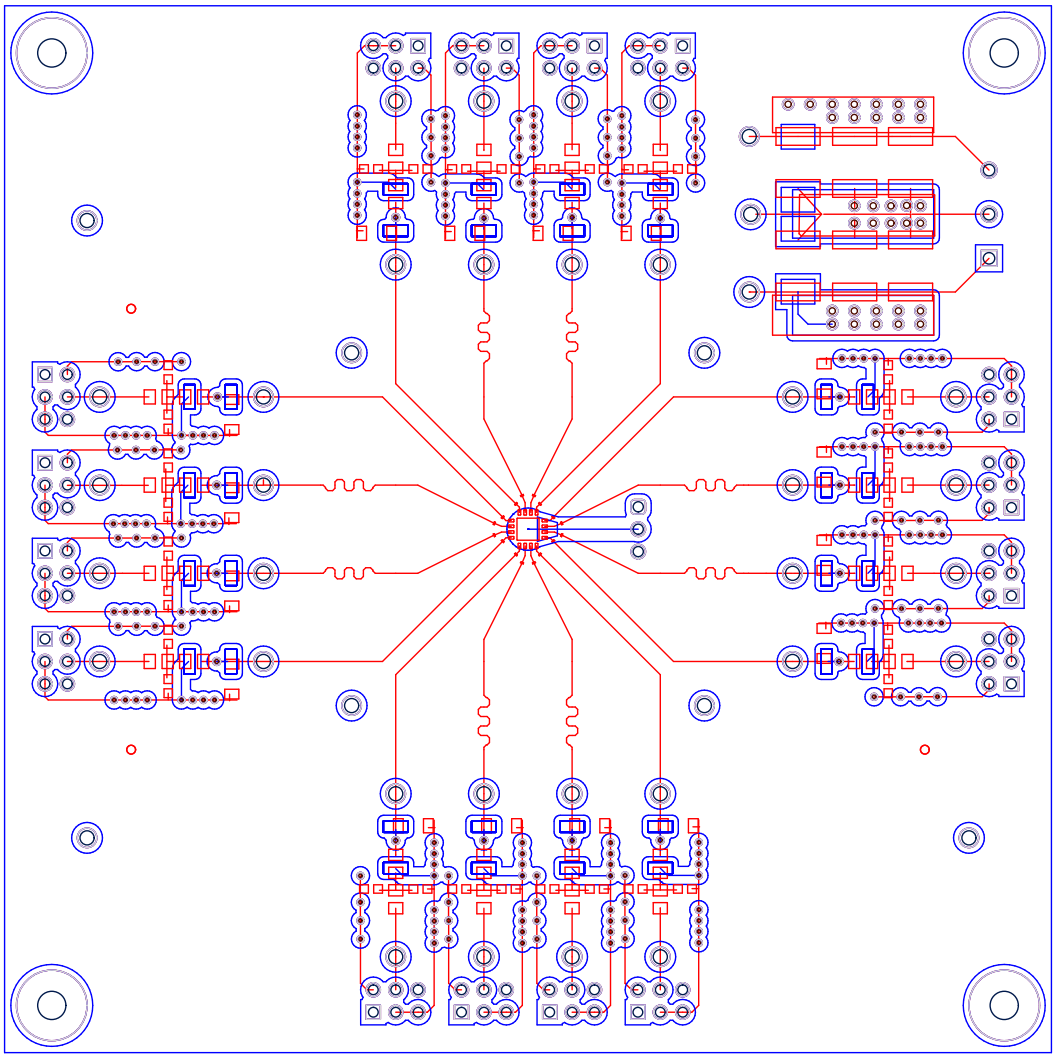

Figure 7-1. Illustration of TMUXRUM-RRPEVM Layout

8 Schematics

Figure 8-1 and Figure 8-2 are schematic views of the TMUXRUM-RRPEVM that includes all the parts and connections.

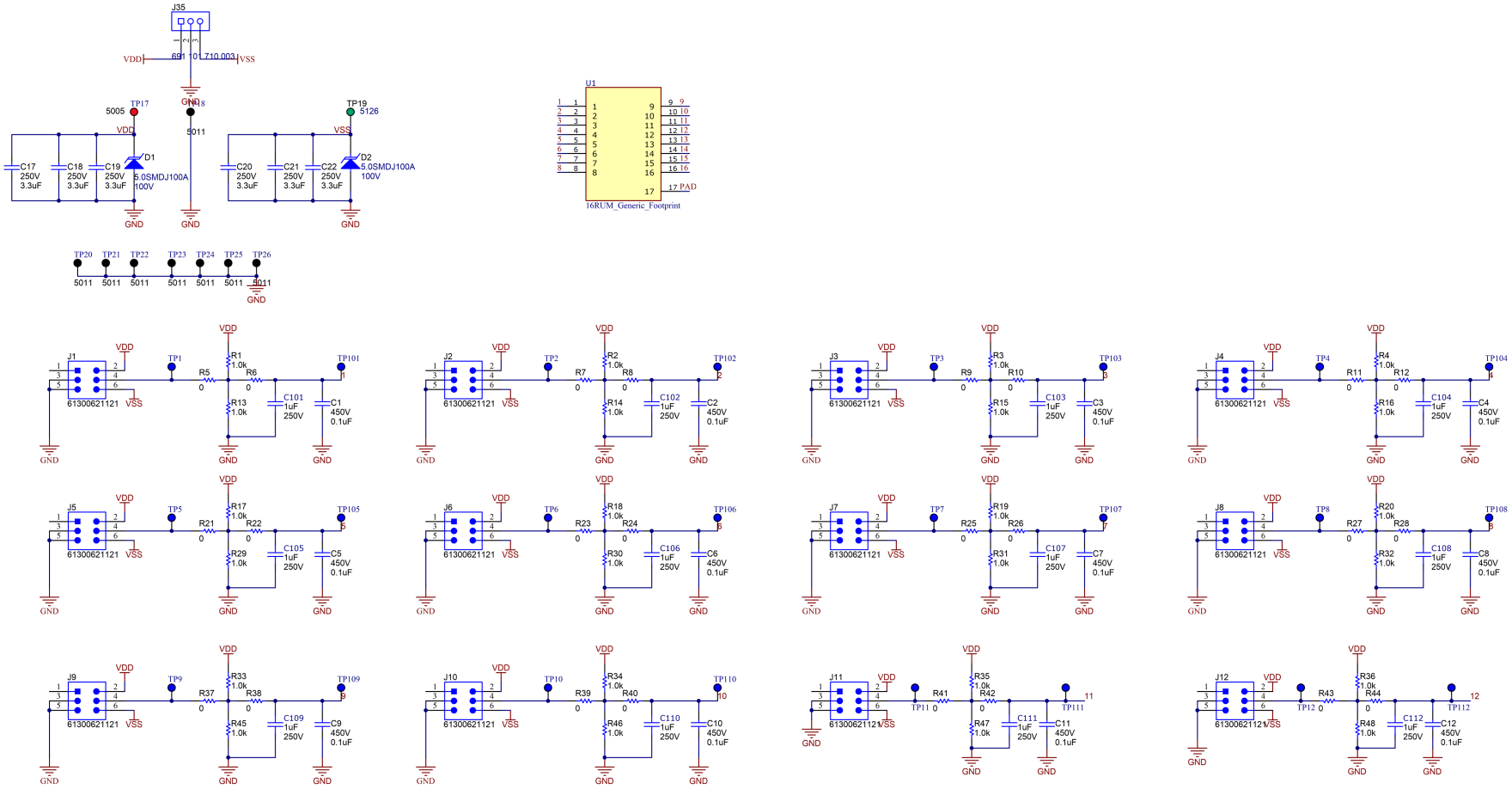

Figure 8-1. TMUXRUM-RRPEVM Schematic Page 1 (Editor View)

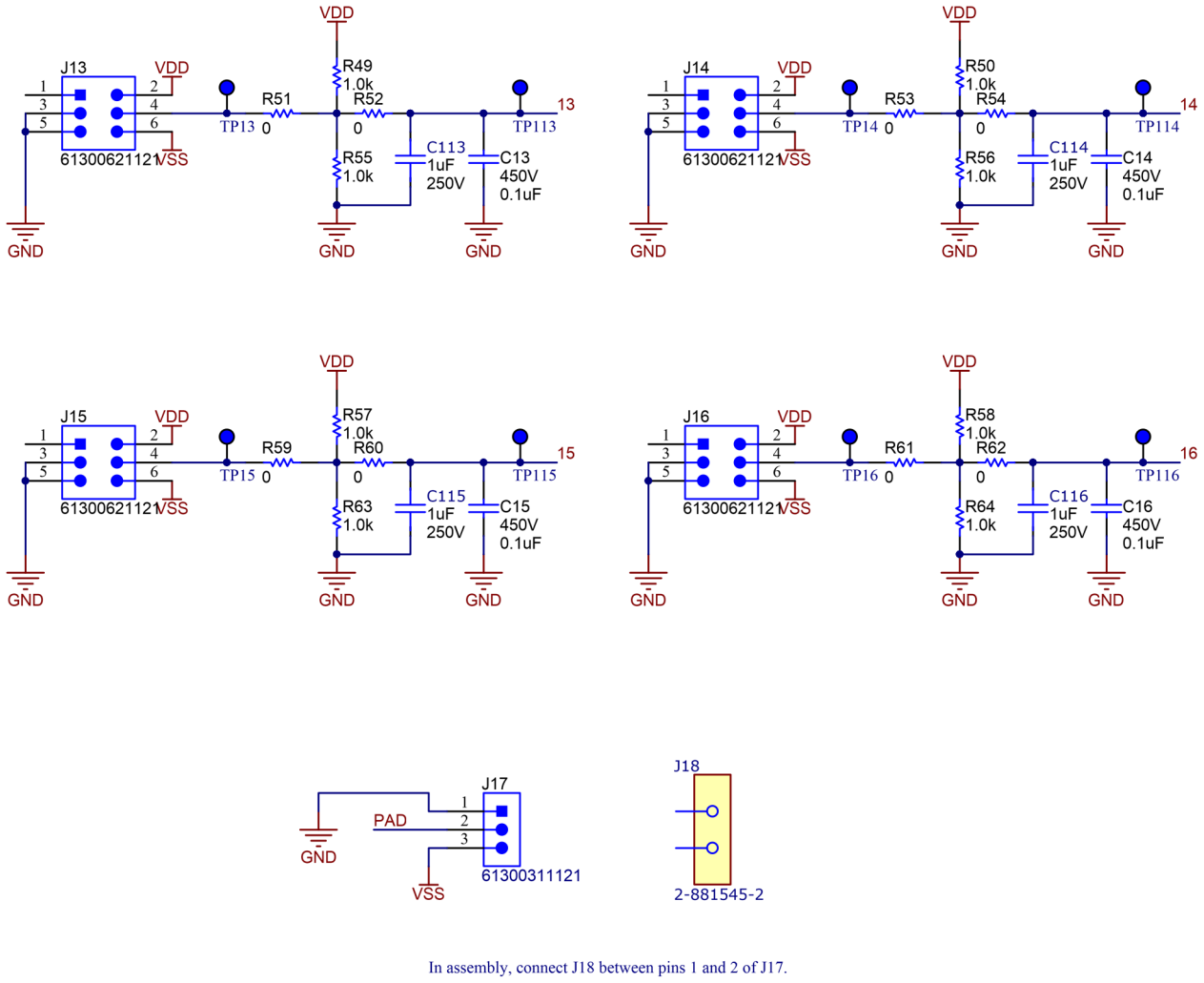

Figure 8-2. TMUXRUM-RRPEVM Schematic Page 2 (Editor View)

Figure 8-3 and Figure 8-4 are schematic views of the TMUXRUM-RRPEVM that show only the parts that are included in the EVM and excludes the parts that are DNI.

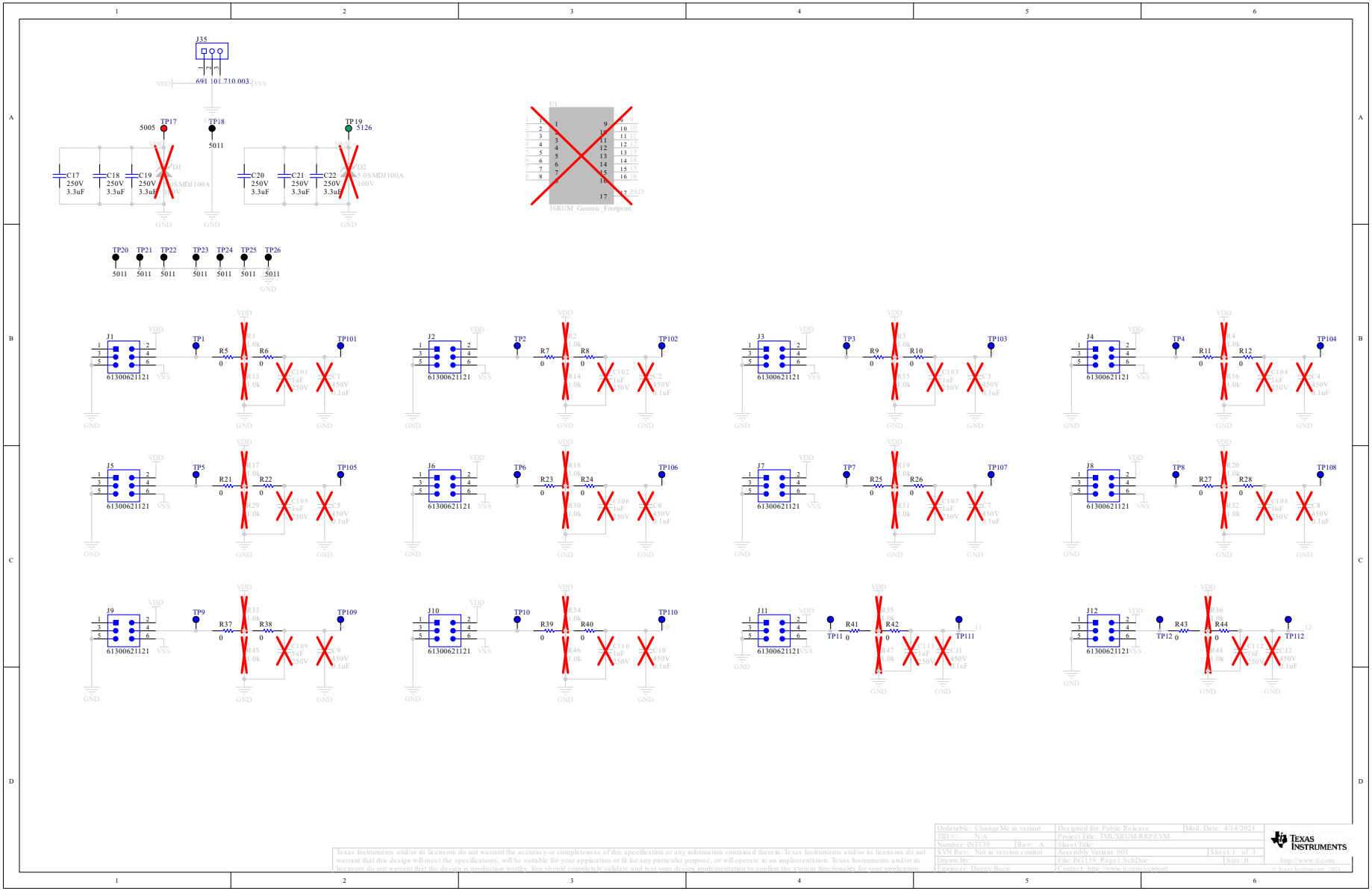

Figure 8-3. TMUXRUM-RRPEVM Schematic Page 1 (DNI)

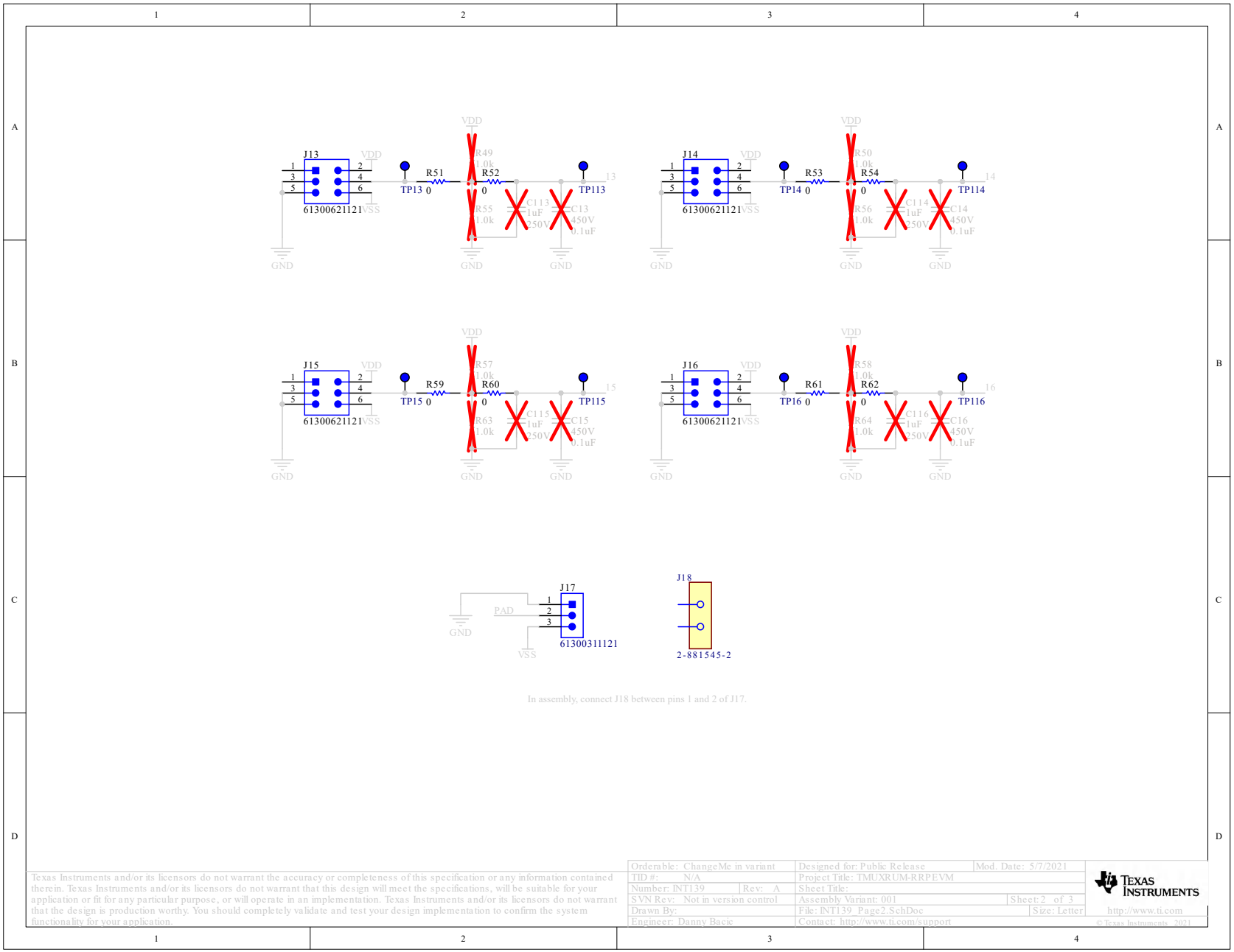

Figure 8-4. TMUXRUM-RRPEVM Schematic Page 2 (DNI)

9 Bill of Materials

Table 9-1. TMUXRUM-RRPEVM Bill of Materials

Designator	PartNumber	Manufacturer	Description	Quantity
C17, C18, C19, C20, C21, C22	CKG57NX7T2E335M500JH	TDK	CAP, CERM, 3.3 µF, 250 V, ± 20%, X7T, AEC-Q200 Grade 1, 6 × 5 × 5 mm	6
H1, H2, H3, H4	NY PMS 440 0025 PH	B&F Fastener Supply	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	4
H5, H6, H7, H8	1902C	Keystone	Standoff, Hex, 0.5"L #4-40 Nylon	4
J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16	61300621121	Wurth Elektronik	Header, 2.54 mm, 3×2, Gold, TH	16
J17	61300311121	Wurth Elektronik	Header, 2.54 mm, 3×1, Gold, TH	1
J18	2-881545-2	TE	Default shunt positioning: between pins 1 and 2 of J17.	1
J19, J20, J21, J22, J23, J24, J25, J26, J27, J28, J29, J30, J31, J32, J33, J34	2-881545-2	TE	Default shunt positioning: between pins 3 and 4 of J1-J16.	16
J35	691 101 710 003	Wurth Elektronik	Terminal Block, 5 mm, 3×1, Tin, TH	1
LBL1	THT-14-423-10	Brady	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	1
R5, R6, R7, R8, R9, R10, R11, R12, R21, R22, R23, R24, R25, R26, R27, R28, R37, R38, R39, R40, R41, R42, R43, R44, R51, R52, R53, R54, R59, R60, R61, R62	PMR10EZPJ000	Rohm	RES, 0, 0%, W, AEC-Q200 Grade 0, 0805	32
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP101, TP102, TP103, TP104, TP105, TP106, TP107, TP108, TP109, TP110, TP111, TP112, TP113, TP114, TP115, TP116	5122	Keystone	Test Point, Compact, Blue, TH	32
TP17	5005	Keystone	Test Point, Compact, Red, TH	1
TP18, TP20, TP21, TP22, TP23, TP24, TP25, TP26	5011	Keystone	Test Point, Multipurpose, Black, TH	8
TP19	5126	Keystone	Test Point, Multipurpose, Green, TH	1

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265