



PRODUCT/PROCESS CHANGE NOTIFICATION

PCN IPD-PWR/13/8040
Dated 02 Aug 2013

**SOT-23 ECOPACK 2 graded moulding compound assembly
capacity expansion - Nantong Fujitsu Microelectronics
(China) Subcontractor.**

Table 1. Change Implementation Schedule

Forecasted implementation date for change	26-Jul-2013
Forecasted availability date of samples for customer	26-Jul-2013
Forecasted date for STMicroelectronics change Qualification Plan results availability	26-Jul-2013
Estimated date of changed product first shipment	01-Nov-2013

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	see attached list
Type of change	Package assembly location change, Testing location change
Reason for change	To increase capacity on SOT-23 package.
Description of the change	Continuing in the program to introduce ECOPACK 2, graded Moulding Compound products and in order to be ready to support the market demand of Power Bipolar Transistors, the products listed in this PCN will be manufactured also in Nantong Fujitsu Microelectronics (China) using green resin. Products are in agreement with ST standards and guarantee the same quality and the electrical characteristics as the current production. Devices used for qualification are available as Samples.
Change Product Identification	By traceability code.
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt		PCN IPD-PWR/13/8040
Please sign and return to STMicroelectronics Sales Office		Dated 02 Aug 2013
<input type="checkbox"/> Qualification Plan Denied <input type="checkbox"/> Qualification Plan Approved <input type="checkbox"/> Change Denied <input type="checkbox"/> Change Approved	Name: Title: Company: Date: Signature:	
Remark		

DOCUMENT APPROVAL

Name	Function
Mottese, Anna	Marketing Manager
Aleo, Mario-Antonio	Product Manager
Falcone, Giuseppe	Q.A. Manager

Dear Customer,

Please be informed that Power Bipolar Transistors in SOT-23 Package, currently manufactured in TSPS (KEC) Thailand Subcontractor, will be also produced in Nantong Fujitsu Microelectronics (China) using green resin.

Since Nantong Fujitsu Microelectronics does not process Hard Solder, named also Eutectics Solder, the die bonding is done with Power Glue.

The involved product series and affected packages are listed in the table below:

Product Family	Package	Commercial Product / Series
Power Bipolar Transistors	SOT-23	2STRxxx

Any other Product related to the above series, manufactured in SOT-23 package, even if not expressly included or partially mentioned in the attached table, is affected by this change.

Qualification program and results availability:

The reliability test report is provided in attachment to this document.

Samples availability:

Samples of the test vehicle devices will be available on request starting from week 30-2013.

Any other sample request will be processed and scheduled by Power Transistor Division upon request.

Product Family	Package	Part Number - Test Vehicle
Power Bipolar Transistors	SOT-23	3STR1630 MMBTA92 STR1550 STR2550

Change implementation schedule:

The production start and first shipment will be implemented according to our work in progress and materials availability:

Product Family	1 st Shipment
Power Bipolar Transistors	From Week 43-2013

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change. After acknowledgement, lack of additional response within the 90 days period will constitute acceptance of the change (Jedec Standard No. 46-C). In any case, first shipment may start earlier with customer written agreement.

Marking and traceability:

Unless otherwise stated by customer specific requirement, traceability of SOT-23 graded Moulding Compound, manufactured in FUJITSU (China), will be ensured by the 1st two digits of the traceability code "GF".

Sincerely Yours.

SOT-23 **ST** Vs **NFME** mechanical data & comparison

COMPARISON	ST			NFME			Dim.
	mm.			mm.			
Dim.	Min.	Typ.	Max.	Min.	Typ.	Max.	Dim.
A	0.89		1.4	/	/	1.25	A
A1	0		0.1	0	/	0.15	A1
B	0.3		0.51	0.36	/	0.50	b
C	0.085		0.18	0.14	/	0.20	c
D	2.75		3.04	2.826	2.926	3.026	D
e	0.85		1.05	0.95BSC			e
e1	1.7		2.1	1.90BSC			e1
E	1.2		1.6	1.526	1.626	1.726	E1
H	2.1		2.75	2.60	2.80	3.00	E
L		0.6		0.59REF			L1
S	0.35		0.65	/			not defined

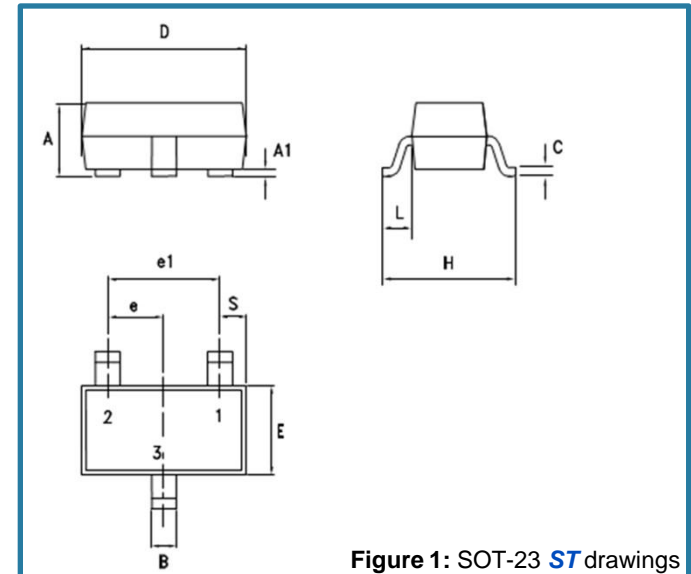


Figure 1: SOT-23 **ST** drawings

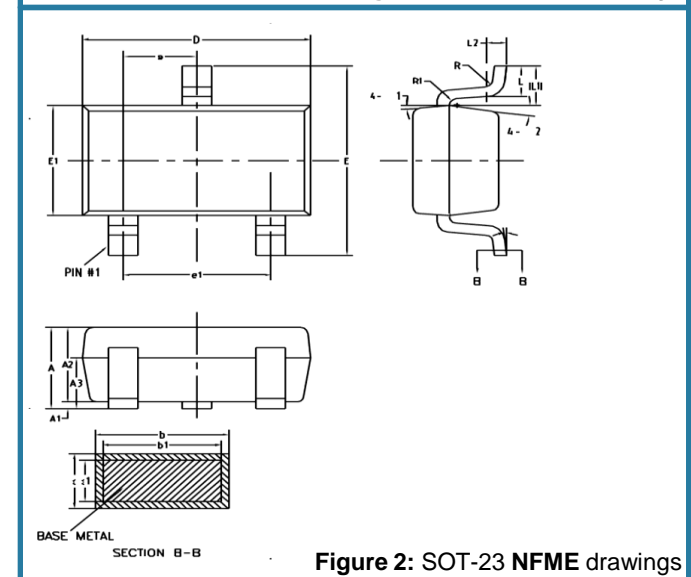


Figure 2: SOT-23 **NFME** drawings

Reliability Report

SOT-23 ECOPACK[®]2 graded molding compound
 assembly capacity expansion – Nantong Fujitsu
 Microelectronics (China) Subcontractor

General Information		Locations	
Product Lines:	MA01 / BV85 / BX09 / 0054	Wafer Diffusion Plants:	<i>Ang Mo Kio (Singapore)</i>
Product Families:	Power Bipolar Transistors	EWS Plants:	<i>Ang Mo Kio (Singapore)</i>
P/Ns:	3STR1630 (MA01) STR1550 (BV85) STR2550 (BX09) MMBTA92 (0054)	Assembly plant:	<i>Nantong Fujitsu Microelectronics (China)</i>
Product Group:	IMS - IPD	Reliability Lab:	<i>IMS-IPD Catania Reliability Lab.</i>
Product division:	Power Transistor Division		
Package:	SOT-23		
Silicon Process techn.:	PLANAR Power Bipolar		

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	July 2013	9	C. Cappello	G.Falcone	First issue

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size
HF	Halogen Free

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Qualification of the SOT-23 package graded Molding Compound manufactured in Nantong Fujitsu Microelectronics (China) Subcontractor.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

PLANAR Power Bipolar.

4.2 Construction note

D.U.T.: 3STR1630 LINE: MA01 PACKAGE: SOT-23

Wafer/Die fab. information	
Wafer fab manufacturing location	Ang Mo Kio (Singapore)
Technology	PLANAR Power Bipolar
Die finishing back side	SUPER DASP
Die size	910 x 860 μm^2
Metal	Al/Si
Passivation type	Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Ang Mo Kio (Singapore)
Test program	WPIS

Assembly information	
Assembly site	Nantong Fujitsu Microelectronics (China)
Package description	SOT-23
Molding compound	HF Epoxy Resin
Frame material	Cu
Die attach process	Power Glue
Wire bonding process	Ultrasonic
Wires bonding materials	Cu 1 mils
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	Nantong Fujitsu Microelectronics (China)
Tester	IPTTEST

D.U.T.: STR1550
LINE: BV85
PACKAGE: SOT-23

Wafer/Die fab. information	
Wafer fab manufacturing location	Ang Mo Kio (Singapore)
Technology	PLANAR Power Bipolar
Die finishing back side	SUPER DASP
Die size	900 x 860 μm^2
Metal	Al/Si
Passivation type	Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Ang Mo Kio (Singapore)
Test program	WPIS

Assembly information	
Assembly site	Nantong Fujitsu Microelectronics (China)
Package description	SOT-23
Molding compound	HF Epoxy Resin
Frame material	Cu
Die attach process	Power Glue
Wire bonding process	Ultrasonic
Wires bonding materials	Cu 1 mils
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	Nantong Fujitsu Microelectronics (China)
Tester	IPTTEST

D.U.T.: STR2550
LINE: BX09
PACKAGE: SOT-23

Wafer/Die fab. information	
Wafer fab manufacturing location	Ang Mo Kio (Singapore)
Technology	PLANAR Power Bipolar
Die finishing back side	SUPER DASP
Die size	900 x 860 μm^2
Metal	Al/Si
Passivation type	Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Ang Mo Kio (Singapore)
Test program	WPIS

Assembly information	
Assembly site	Nantong Fujitsu Microelectronics (China)
Package description	SOT-23
Molding compound	HF Epoxy Resin
Frame material	Cu
Die attach process	Power Glue
Wire bonding process	Ultrasonic
Wires bonding materials	Cu 1 mils
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	Nantong Fujitsu Microelectronics (China)
Tester	IPTST

D.U.T.: MMBTA92 LINE: 0054 PACKAGE: SOT-23

Wafer/Die fab. information	
Wafer fab manufacturing location	Ang Mo Kio (Singapore)
Technology	PLANAR Power Bipolar
Die finishing back side	SUPER DASP
Die size	650 x 650 μm^2
Metal	Al/Si
Passivation type	PVAPOX

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Ang Mo Kio (Singapore)
Test program	WPIS

Assembly information	
Assembly site	Nantong Fujitsu Microelectronics (China)
Package description	SOT-23
Molding compound	HF Epoxy Resin
Frame material	Cu
Die attach process	Power Glue
Wire bonding process	Ultrasonic
Wires bonding materials	Cu 0.8 mils
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	Nantong Fujitsu Microelectronics (China)
Tester	IPTTEST

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1	3STR1630	MA01	Power BIPOLAR
2	STR1550	BV85	Power BIPOLAR
3	STR2550	BX09	Power BIPOLAR
4	MMBTA92	0054	Power BIPOLAR

5.2 Reliability test plan summary

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS				Note
						LOT1 MA01	LOT2 BV85	LOT3 BX09	LOT4 0054	
Die Oriented Tests										
HTRB	N	JESD22 A-108	TA = 150°C, BIAS=24V (MA01) BIAS=400V (BV85) BIAS=400V (BX09) BIAS=160V (0054)	77 x 4 lots	168 H	0/77	0/77	0/77	0/77	
					500 H	0/77	0/77	0/77	0/77	
					1000 H	0/77	0/77	0/77	0/77	
HTSL	N	JESD22 A-103	TA = 150°C	77 x 4 lots	168 H	0/77	0/77	0/77	0/77	
					500 H	0/77	0/77	0/77	0/77	
					1000 H	0/77	0/77	0/77	0/77	
Package Oriented Tests										
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Oven Reflow @ Tpeak=260°C for 3 times	251 x 4 lots	Final	0/251	0/251	0/251	0/251	
AC	Y	JESD22 A-102	Pa=2Atm / TA=121°C	77 x 4 lots	96 H	0/77	0/77	0/77	0/77	
TC	Y	JESD22 A-104	TA = -65°C to 150°C	77 x 4 lots	100 cy	0/77	0/77	0/77	0/77	
					200 cy	0/77	0/77	0/77	0/77	
					500 cy	0/77	0/77	0/77	0/77	
TF/IOL	Y	Mil-Std 750D Method 1037	ΔTC=105°C – Ton/Toff=5min	20 x 4 lots	6Kcy	0/77	0/77	0/77	0/77	
H3TRB	Y	JESD22 A-101	TA=85°C , RH=85% , BIAS=30V (MA01) BIAS=100V (BV85) BIAS=100V (BX09) BIAS=100V (0054)	77 x 4 lots	168 H	0/77	0/77	0/77	0/77	
					500 H	0/77	0/77	0/77	0/77	
					1000 H	0/77	0/77	0/77	0/77	

6 ANNEXES 6.0

6.1 Tests Description

Test name	Description	Purpose
Die Oriented		
HTRB High Temperature Reverse Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: low power dissipation; max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
AC Auto Clave	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
TF / IOL Thermal Fatigue / Intermittent Operating Life	The device is submitted to cycled temperature excursions generated by power cycles (ON/OFF) at T ambient.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
H3TRB / THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	To verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.

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