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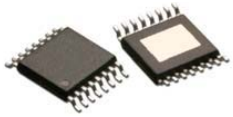
Preliminary

CGA-0116(Z)

3-OUTPUT ACTIVE SPLITTER FOR CATV



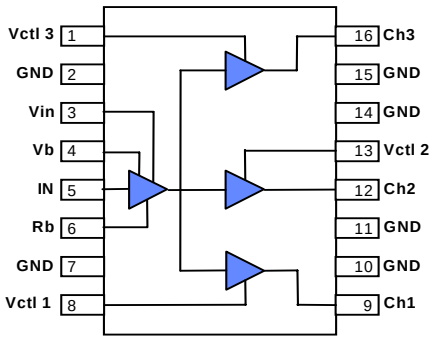
RFMD Green, RoHS Compliant, Pb-Free (Z Part Number)
Package: TSSOP, 16-pin

Product Description

Consumer products, such as Set-Top boxes, PVR's, Home Gateways, and Cable Modems, often require a technique for "splitting" the incoming RF CATV signal, to perform various functions, such as picture-inpicture, VOIP, data, and video recording. RFMD's CGA-0116 is a high performance 3-output broadband CATV active splitter-amplifier, designed for operation at 5V. It offers flat gain, high isolation, high IP_2, and low power consumption. This RFIC uses the latest Silicon Germanium Heterostructure Bipolar Transistor (SiGe HBT) process featuring 2 micron emitters. The matte tin finish on the lead-free package utilizes a post annealing process to mitigate tin whisker formation and is RoHS compliant per EU directive 2002/95. This package is also manufactured with green molding compounds that contain no antimony trioxide nor halogenated fire retardants.

Optimum Technology Matching® Applied

- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ InGaP HBT
- ☐ SiGe BiCMOS
- ☐ Si BiCMOS
- ☑ SiGe HBT
- ☐ GaAs pHEMT
- ☐ Si CMOS
- ☐ Si BJT
- ☐ GaN HEMT
- ☐ RF MEMS



Features

- Available in Lead Free, RoHS compliant, and Green packaging
- Broad Frequency Band: 50MHz to 870MHz
- Flat Gain Response: < ±0.5dB Variance
- Internally Matched to 75Ω
- High Isolation between Output Ports: >35dB
- High IP_2: >149dBμV
- Single Voltage Supply
- Patent Pending

Applications

- Set-Top Box
- Cable Modem
- PVR

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Frequency of Operation	50.0		870.0	MHz	
Current	135.0	150.0	165.0		
Output Power at 1dB Compression	114.5	116.0		dBμV	Channels 1 and 2 @ 500MHz
Output Power at 1dB Compression	118.5	120.0		dBμV	Channel 3 @ 870MHz
Small Signal Gain	1.8	2.3	2.8	dB	Channels 1 and 2 @ 870MHz
Small Signal Gain	6.5	7.5	8.5	dB	Channel 3 @ 870MHz
Input Return Loss	7.5	9.0		dB	50MHz to 870MHz
Output Return Loss	11.0	13.0		dB	50MHz to 870MHz
Output Third Order Intercept Point	127.0	129.0		dBμV	Channels 1 and 2 @ 500MHz
Output Third Order Intercept Point	132.0	134.0		dBμV	Channel 3 @ 500MHz
Output Second Order Intercept Point	146.0	149.0		dBμV	Channels 1 and 2 @ 500MHz
Output Second Order Intercept Point	152.0	155.0		dBμV	Channel 3 @ 500MHz
Noise Figure		7.5	8.5	dB	Channels 1 and 2 @ 870MHz
Noise Figure		7.5	8.5	dB	Channel 3 @ 870MHz
Isolation	32.0	35.0		dB	Channel-to-Channel 50MHz to 870MHz
Isolation	37.0	40.0		dB	Output-to-Input 50MHz to 870MHz
Thermal Resistance		70		°C/W	junction to backside

Test Conditions: Z_O=75Ω, V_{CC}=5V, I=150mA, T_{BP}=30°C

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Absolute Maximum Ratings

Parameter	Rating	Unit
Max Device Current (I_D)	200	mA
Max Device Voltage (V_D)	6	V
Max RF Input Power	15	dBm
Max Dissipated Power	1.2	W
Max Junction Temperature (T_J)	150	°C
Operating Temperature Range (T_L)	-40 to +85	°C
Max Storage Temperature	-40 to +150	°C

Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation, the device voltage and current must not exceed the maximum operating values specified in the table on page one.

Bias Conditions should also satisfy the following expression:

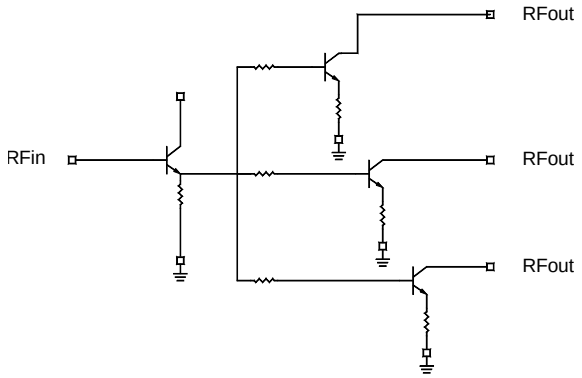
$I_D V_D < (T_J - T_L)/R_{TH}$, j-l

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EU Directive 2002/95/EC (at time of this document revision).

Simplified Device Schematic



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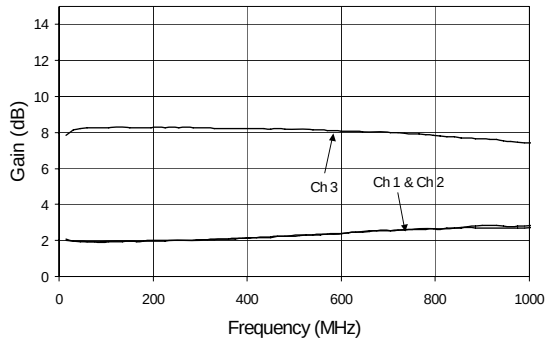
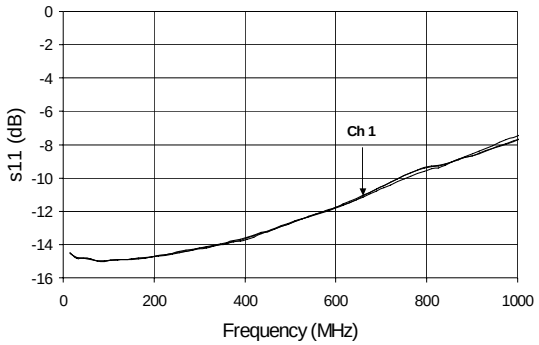
Evaluation Board Data (V_{CC} = 5.0V, I_{CC} = 150mA)

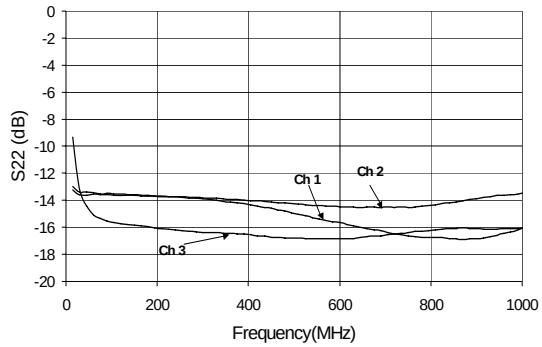
Gain vs Frequency



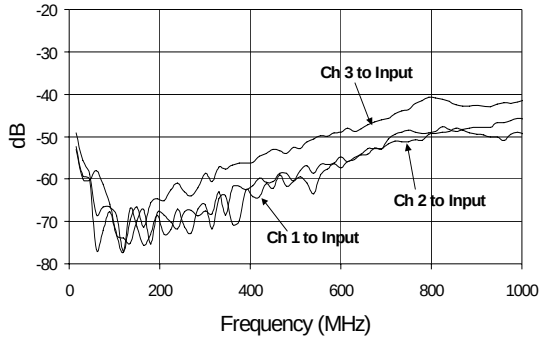
Input Return Loss Vs. Freq



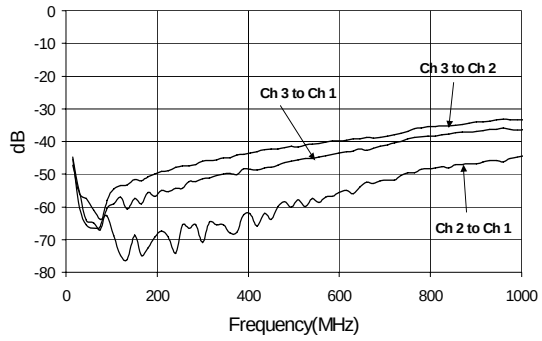
Output Return Loss vs Frequency



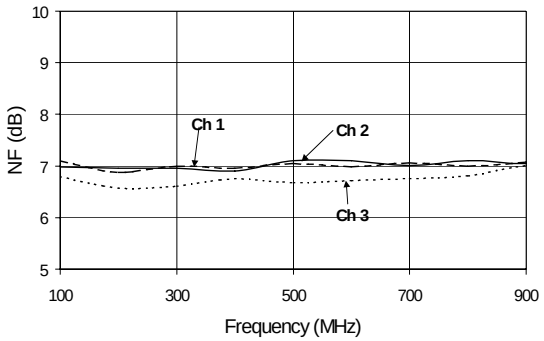
Isolation Channel Output to RF Input



Isolation vs Frequency

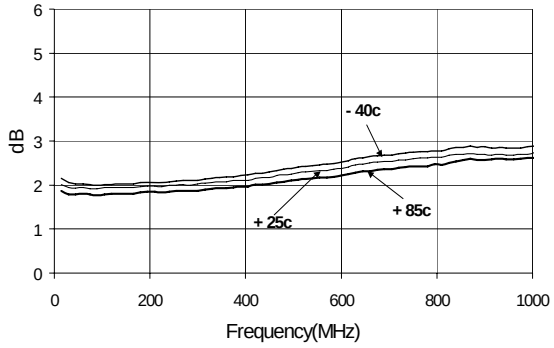


Noise Figure vs Frequency

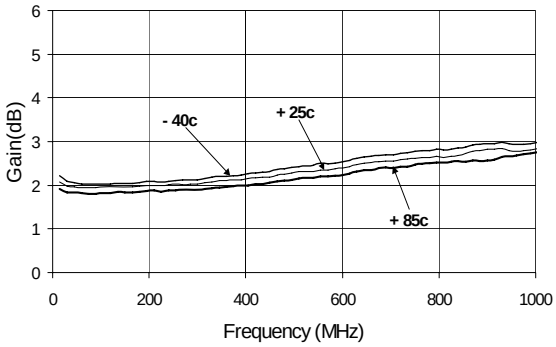


Evaluation Board Data (V_{CC} = 5.0V, I_{CC} = 150mA)

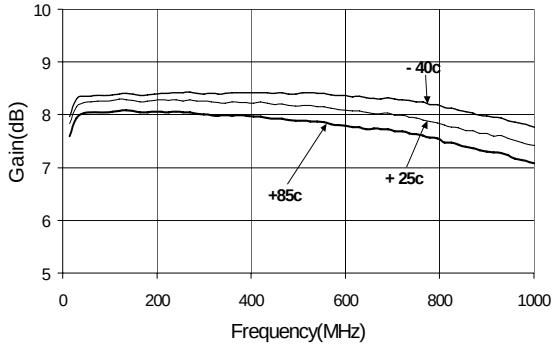
Channel 1 Gain vs Temperature



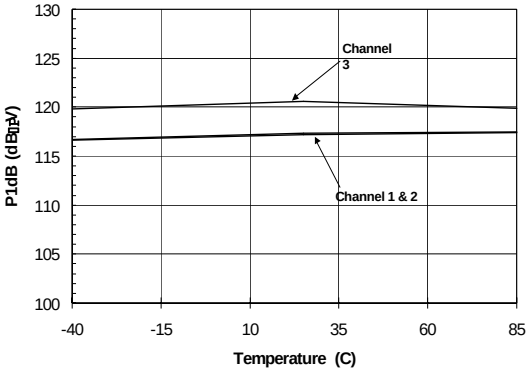
Channel 2 Gain vs Temperature



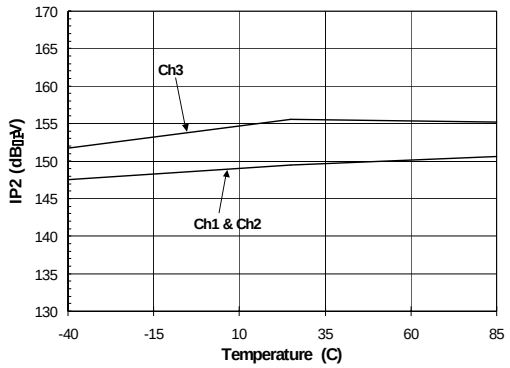
Ch 3 Gain vs Temperature



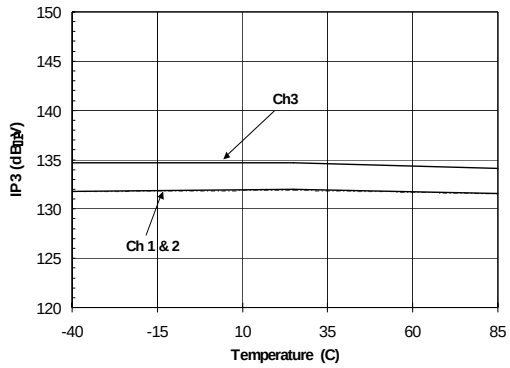
P1dB vs. Temperature (500 MHz)



IP2 vs. Temperature (500 MHz)



IP3 vs. Temperature (500 MHz)



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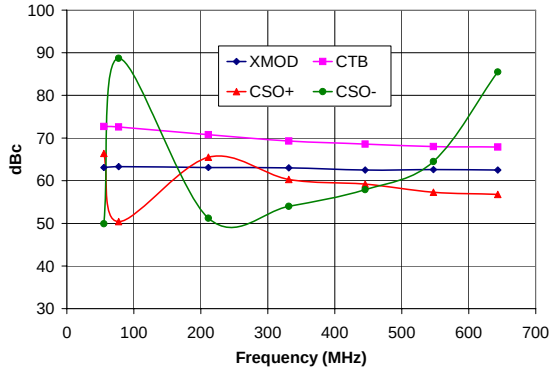
Channel 1 and 2 Composite Performance:

Evaluation Board Data (V_{CC} = 5.0V, I_{CC} = 150mA)

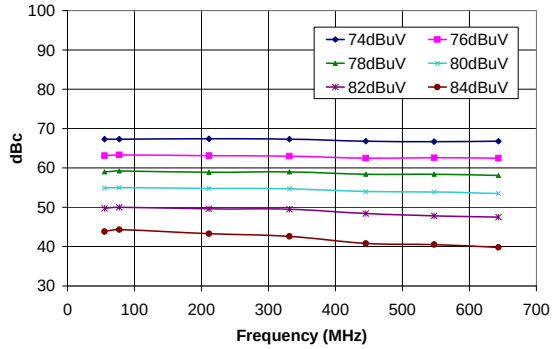
Ch. 1 Measured Data Shown

CTB/CSO/XMOD, Ch. 1 & 2
Input Power 76 dBuV/Ch., 100 Ch., Flat

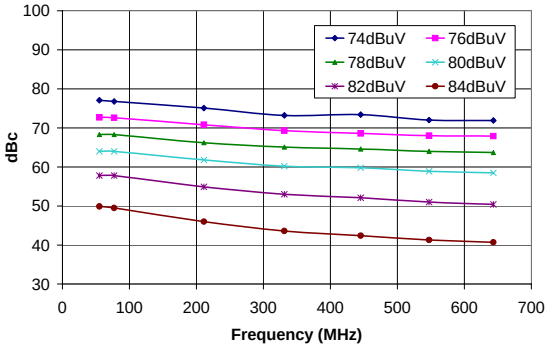


Channel 1 & 2 Composite Performance vs. Input Power Level, 100 Ch., Flat:

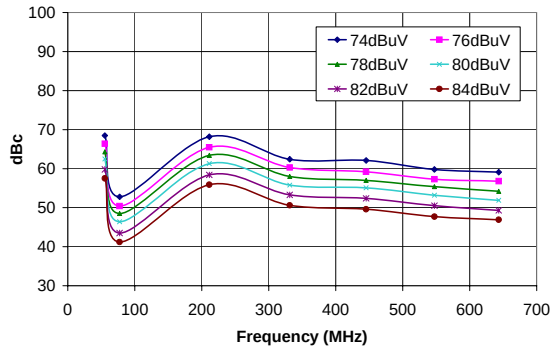
CGA-0116 Ch. 1 & 2: XMOD vs. Pin and Freq.



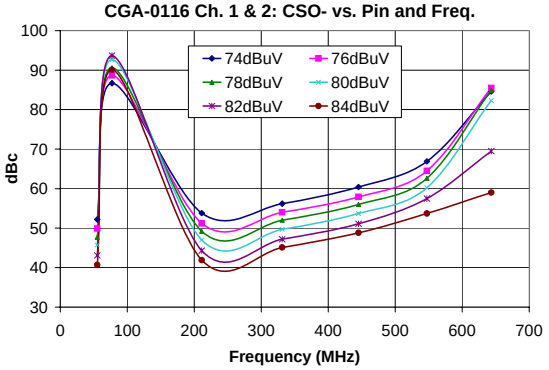
CGA-0116 Ch. 1 & 2: CTB vs. Pin and Freq.



CGA-0116 Ch. 1 & 2: CSO+ vs. Pin and Freq.

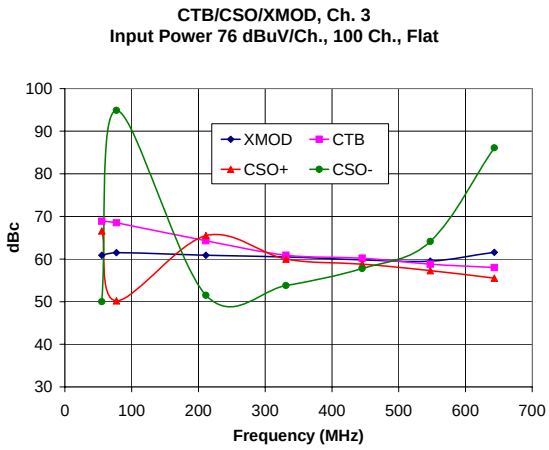


CGA-0116 Ch. 1 & 2: CSO- vs. Pin and Freq.

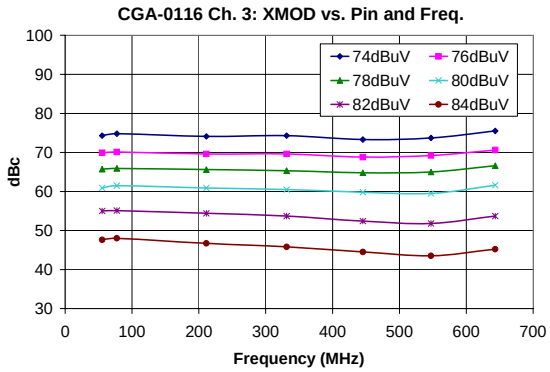


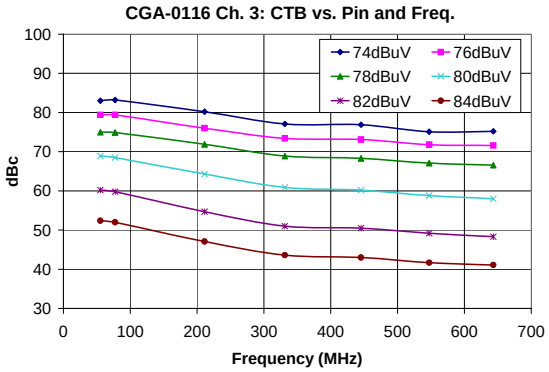
Channel 3 Composite Performance:

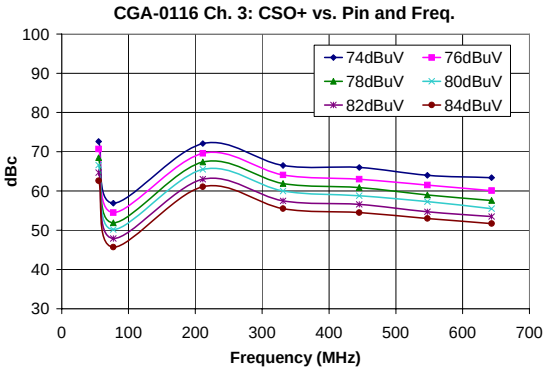
Evaluation Board Data (V_{CC} = 5.0V, I_{CC} = 150mA)

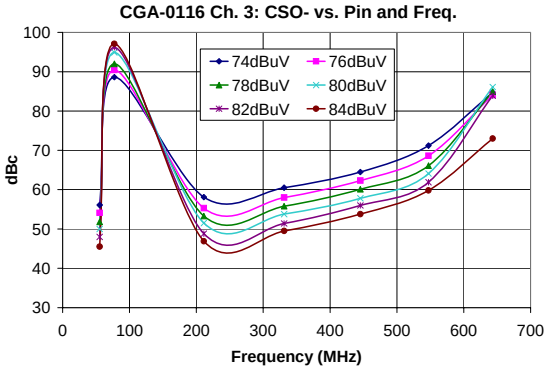


Channel 3 Composite Performance vs. Input Power Level, 100 Ch., Flat:









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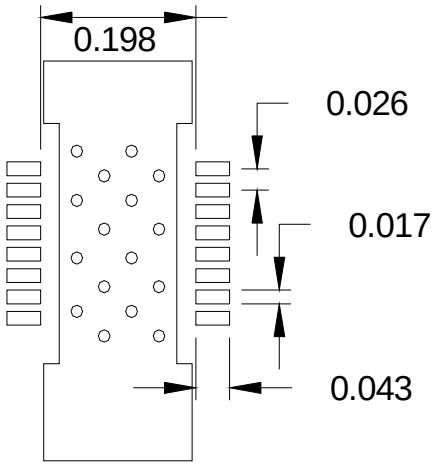
Pin	Function	Description
1	VCTL 3	Gain adjust for Output 3. This pin should be bypassed to ground for max gain
2, 7, 10, 11, 14, 15	GND	Connection to ground.
3	VIN	Voltage supply connection for input. This pin should be bypassed with a suitable capacitor.
4	VB	Bias connection for input. This pin should be bypassed with a suitable capacitor
5	IN	RF input pin. This pin requires a DC blocking capacitor
6	RB	Input bias resistor connection for setting bias current. This pin should be connected to groung for specified operation.
8	VCTL 1	Gain adjust for Output 3. This pin should be bypassed to ground for max gain
9	Ch. 1	RF Output 1 and DC supply pin. This pin required the use of an external blocking capacitor and RF choke.
12	Ch. 2	RF Output 2 and DC supply pin. This pin required the use of an external blocking capacitor and RF choke.
13	VCTL 2	Gain adjust for Output 3. This pin should be bypassed to ground for max gain
16	Ch. 3	RF Output 3 and DC supply pin. This pin required the use of an external blocking capacitor and RF choke.
Back-side	GND	The exposed backside paddle needs to be well grounded with multiple vias. This is the main electrical GND and the main thermal path.

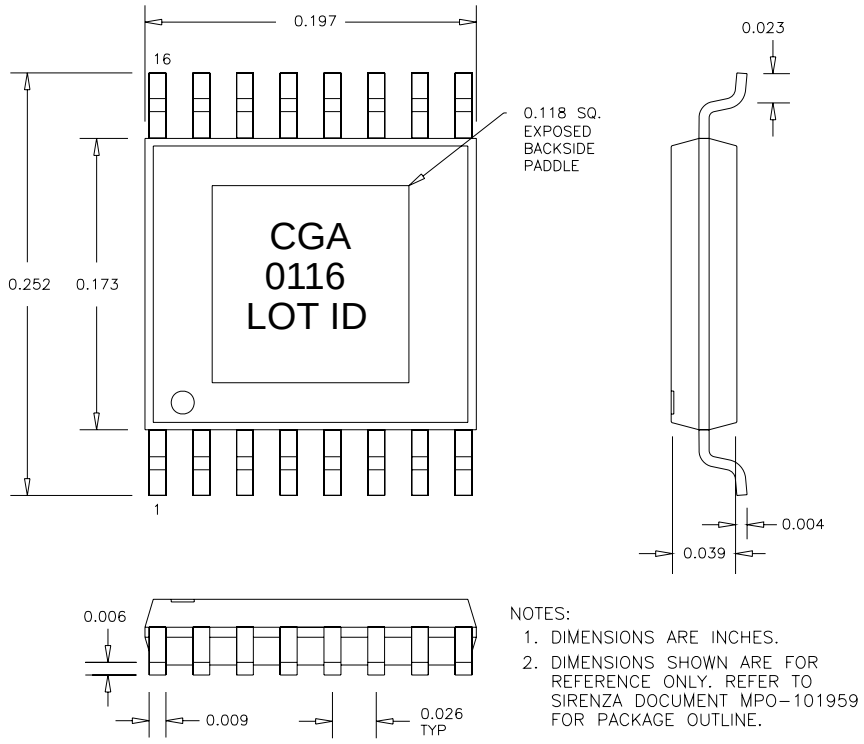
Recommended Land Pattern



Note 1: Dimensions are in inches

Package Drawing

Dimensions in inches (millimeters)
Refer to drawing posted at www.rfmd.com for tolerances.



NOTES:
1. DIMENSIONS ARE INCHES.
2. DIMENSIONS SHOWN ARE FOR REFERENCE ONLY. REFER TO SIRENZA DOCUMENT MPO-101959 FOR PACKAGE OUTLINE.

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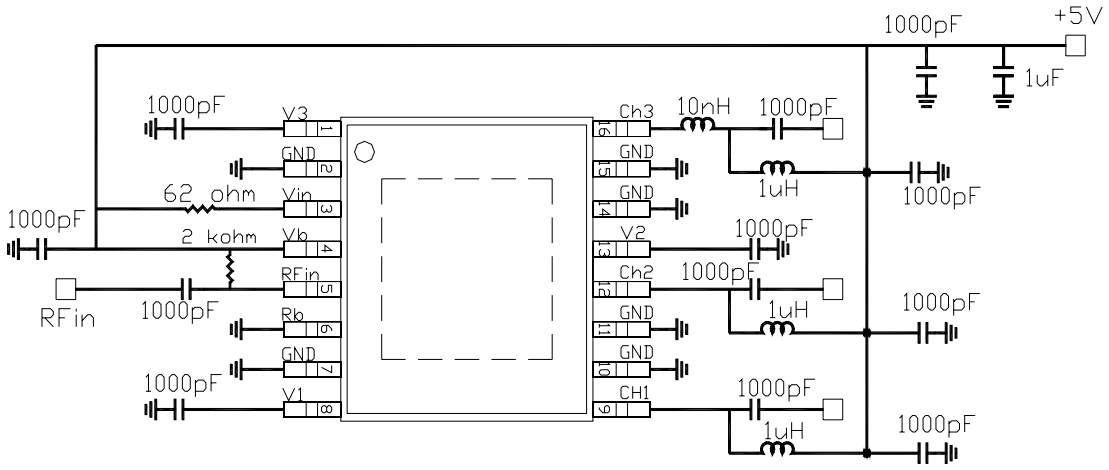
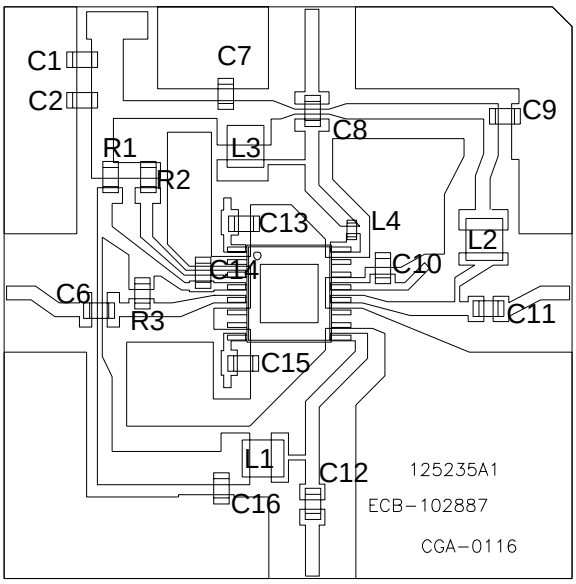
Evaluation Board Schematic



Evaluation Board Layout and Bill of Materials



Component	Value
C1	0.1uF
C2,C6,C7,C8,C9,C10,C11, C12,C13,C14,C15,C16	1000pF
L1,L2,L3	1uH
R1	0 ohm
R2	62 ohm
R3	2K ohm
L4	10nH 0402 size

NOTE: VIAS NOT SHOWN

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