PCN Number:	20170316002	**PCN Date:**	March 21, 2017
Title:	ADC12J16/27/40xx and LM15851 Product Family Design Revision and Transfer of NKE packages to Amkor P1		
Customer Contact:	PCN Manager	**Dept:**	Quality Services
Proposed 1st Ship Date:	June 21, 2017	**Estimated Sample Availability:**	Date provided at sample request.
Change Type:			

☒	Assembly Site	☒	Design	☐	Wafer Bump Site
☐	Assembly Process	☐	Data Sheet	☐	Wafer Bump Material
☐	Assembly Materials	☐	Part number change	☐	Wafer Bump Process
☐	Mechanical Specification	☐	Test Site	☐	Wafer Fab Site
☐	Packing/Shipping/Labeling	☐	Test Process	☐	Wafer Fab Materials
				☐	Wafer Fab Process

PCN Details

Description of Change:

This notification is to inform of a design revision change to the ADC12J1600NKE, ADC12J2700NKE, ADC12J4000NKE and LM15851NKE devices. A metal mask change was performed to fix loss of data alignment as a result of disabling SYSREF processing.

Problem description

- Two customers reported loss of deterministic latency / loss of data alignment between two ADC12J4000 as a result of disabling SYSREF processing.
  - SYSREF processing needs to be disabled before powering down the SYSREF receiver (this saves about 40 mA from the 1.2V supply).
  - SYSREF processing needs to be disabled if the SYSREF signal routing on board is to be used additionally for a different signaling purpose.
- The problem can be reproduced on the design evaluation board on approximately half the ADC12J4000 parts.
  - Bad parts don't always fail: the latency shifts about half the time the SYSREF processing is disabled on very bad parts.
    - Unfortunately, there is no SPI-readable diagnostic that the shift occurred.
  - Good parts do not show a latency shift when tested with 10,000 cycles of SYSREF processor enable / disable, including testing over the weekend with 300,000 cycles.
  - Good parts appear to be always good and bad parts always bad (i.e., latency shifts about ½ the time). This seems independent of:
    - SYSREF being high / low or switching when disabling SYSREF processing.
    - Clock speed between 1.6 GSPS and 4 GSPS (customer saw more failures for slower clock!)
    - VA12 supply voltage between 0.9V and 1.5V
    - Temperature – however, latency shifts are much more frequent at cold vs. hot.

Root cause

- The root cause of the latency shift when disabling SYSREF processing is in the analog CML clock block where CMOS levels are used to asynchronously reset a CML DFF.
  - The CML DFF in question re-latches the signal "sample" which samples the SYSREF rising edge and is used after SYSREF positive-edge detection to reset the divide-by-4 clock generator.
  - The *asynchronous reset* does not pose a design issue, because the signal path is only active during a retiming event which should not be the case at the time SYSREF processing is disabled.
  - The circuit is robustly designed, and signal "sample" is triple-re-latched before feeding the divide-by-4 clock generator.
  - Unfortunately, even though differential CMOS levels can be used to reset CML DFFs, *care must be taken to avoid the differential reset signal from being under-lapped low*.
    - If both differential reset inputs are low, then the CML DFF becomes current starved, and both Q and Qb outputs become high, an undefined output.

- The following re-latching stage clocks in an undefined value, which gets resolved by the offsets of this latter DFF. An output high will create a clock phase disturbance if it occurs out-of-phase with the divide-by-4 clock generator.

Solution

- Actual Fix:
  - The fix chosen is the simplest, disabling the CMOS-levels differential reset on DFFSAMDLY.
  - Only one of a series of pipelined DFFs requires an asynchronous reset.
    - The previous DFFSAMPLE already receives the required reset, and since it is driven by a CML OR gate, the levels are CML, avoiding the glitch issue.
  - Specifically, rp is hard-wired to GNDD, and rm is hard-wired to VD12.
  - The change was implemented with a single Metal-5 mask change.

Verification

- Design
  - The one-Metal Fix was implemented and reviewed by design. Clock Level simulations (including C-only QRC layout parasitics and Monte Carlo runs) verified that the latency bug was fixed without changing any other functionality or timing. I.e., the SYSREF processing works exactly as before with the exception of no latency shift when SYSREF processing disabled.
  - Layout has passed all verification.

- Test
  - SWR material run is complete. Test yield and failure bin paredo are reviewed and validated by design verification team.
  - The design change has been approved

This change did not necessitate a manufacturing or silicon process requalification. However, a full test yield and bin analysis was required from one product from family.

There will be no accompanying changes to the device datasheet.

Group 1 Devices: Design Revision and assembly site change

Group 2 Devices: Assembly site change only

No Material differences between sites

Assembly Site	Assembly Site Origin	Assembly Country Code	Assembly Site City
Amkor K1	AMN	KOR	Seoul
Amkor P1	**AKR**	**PHL**	Cupang, Muntinlupa City

Reason for Change:

To fix design latency shift and transfer due to factory shutdown.

Anticipated impact on Form, Fit, Function, Quality or Reliability (positive / negative):

None

Anticipated impact on Material Declaration

☒	No Impact to the Material Declaration	☐	Material Declarations or Product Content reports are driven from production data and will be available following the production release. Upon production release the revised reports can be obtained at the site link below http://www.ti.com/quality/docs/materialcontentsearch.tsp

Changes to product identification resulting from this PCN:

Die Rev designator and assembly site codes for the affected devices will change as shown in the tables and sample label below:

Current	New
Die Rev [2P]	**Die Rev [2P]**
A	**B**

Assembly Site		ASO:
Amkor K1	Assembly Site Origin (22L)	AMN
Amkor P1	Assembly Site Origin (22L)	**AKR**

Sample product shipping label (not actual product label)

ASSEMBLY SITE CODES: AMN = 7, AKR = 4

Product Affected: Group 1 Devices

ADC12J1600NKE	ADC12J2700NKE	ADC12J4000NKE	LM15851NKE
ADC12J2700NKER	ADC12J2700NKER	ADC12J4000NKER	LM15851NKER
ADC12J1600NKET	ADC12J2700NKET	ADC12J4000NKET	LM15851NKET

Product Affected: Group 2 Devices

ADC12EU050CIPLQ/NOPB	ADC16DV160CILQE/NOPB	LM98640CILQ/NOPB
ADC16DV160CILQ/NOPB	ADC16DV160CILQX/NOPB	

Qualification Report

ADC12J4000NKE Metal 5 PG Fix

Product Attributes

Attributes	Qual Device: ADC12J4000	QBS Product Reference: LM15851	QBS Process Reference: F771558
Assembly Site	AMK-K1	AMK-K1	TIPI
Package Family	VQFN	VQFN	PBGA
Flammability Rating	UL 94 V-0	UL 94 V-0	UL 94 V-0
Wafer Fab Supplier	UMC 12A	UMC12A	UMC12A
Wafer Process	UMC65NMLL	UMC65NMLL	1218C021.M6

- QBS: Qual By Similarity
- Qual Device ADC12J4000 is qualified at LEVEL3-260C

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	Test Name / Condition	Duration	Qual Device: ADC12J4000	QBS Product LM15851	QBS Process F771558
ELFR	Early Life Failure Rate, 85C	48 Hours	-	16/1840/0	-
AC	Autoclave 121C	96 Hours	-	3/228/0	-
ED	Electrical Characterization	Per Datasheet Parameters	-	Pass	-
HAST	Biased HAST, 130C/85%RH	96 Hours	-	3/231/0	-
HBM	ESD - HBM	2000V	-	-	1/3/0
HBM	ESD - HBM	2500 V	-	3/9/0	-
CDM	ESD - CDM	500V	-	-	1/3/0
CDM	ESD - CDM	750 V	-	3/9/0	-
HTOL	Life Test	1000 Hours	-	3/231/0	3/231/0
HTSL	High Temp. Storage Bake, 150C	1000 Hours	-	-	3/231/0
HTSL	High Temp. Storage Bake, 170C	420 Hours	-	3/231/0	-
LU	Latch-up (25C, 85C)	(per JESD78)	-	3/18/0	-
MQ	Manufacturability (Assembly)	(per mfg. Site specification)	-	Pass	-
TC	Temperature Cycle, -55/125C	1000 Cycles	-	-	3/231/0
TC	Temperature Cycle, -65/150C	500 Cycles	-	3/227/0	-
UHAST	Unbiased HAST, 110C/85%RH	192 Hours	-	-	3/231/0

- Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
- The following are equivalent HTOL options based on activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
- The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours
- The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Quality and Environmental data is available at TI's external Web site: http://www.ti.com/

Green/Pb-free Status:

Qualified Pb-Free(SMT) and Green

Qualification Report

Offload of 68-pin NKE Package from Amkor K1 to Amkor P1

Product Attributes

Attributes	Qual Device: ADC12J4000NKER / LM15851
Assembly Site	AMK P1
Package Family	VQFNP
Flammability Rating	UL 94 V-0
Wafer Fab Supplier	UMC 12A
Wafer Process	UMC65NMLL

- Qual Device ADC12J4000NKER / LM15851 is qualified at LEVEL3-260C

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	Test Name / Condition	Duration	Qual Device: ADC12J4000NKER / LM15851
AC	Autoclave, 121C	96 Hours	3/77/0
HAST	Biased HAST, 130C/85%RH	96 Hours	1/77/0
HTSL	High Temp. Storage Bake, 170C	420 Hours	3/77/0
MQ	Manufacturability	(per mfg. Site specification)	PASS
MSL	Thermal Path Integrity	(Level 3 at 260C +5/-0C)	1/12/0

Type	Test Name / Condition	Duration	Qual Device: ADC12J4000NKER / LM15851
TC	Temperature Cycle, -65C/150C	500 Cycles	3/77/0

- Preconditioning was performed for Autoclave, Unbiased HAST, Temperature Cycle, and HTSL.
- The following are equivalent HTSL options based on an activation energy of 0.7eV: 150C/1k Hours, and 170C/420 Hours
- The following are equivalent Temp Cycle options per JESD47: -55C/125C/700 Cycles and -65C/150C/500 Cycles

Quality and Environmental data is available at TI's external Web site: http://www.ti.com/

Green/Pb-free Status:

Qualified Pb-Free(SMT) and Green

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