AN11817

BGA3131 DOCSIS 3.1 upstream amplifier

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Document information

Info	Content
Keywords	BGA3131, Evaluation board, DOCSIS 3.1
Abstract	This application note provides circuit schematic, PCB layout, BOM and typical EVB performance of the *BGA3131 DOCSIS 3.1 upstream amplifier*.
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1. Introduction

The BGA3131 is an upstream amplifier meeting the Data Over Cable Service Interface Specifications 3.1. It is designed for cable modems, CATV set top box and VoIP modem applications.

It amplifies the modulated signals coming from the SoC to a defined power level at the F-connector towards the network.

The device can handle signals between 5 MHz to 205 MHz. The BGA3131 provides 58 dB gain control range in 1 dB increments with high incremental accuracy. Its maximum gain setting delivers 37 dB voltage gain and a superior linear performance.

It supports the DOCSIS 3.1 output power levels of 68dBmV (RMS) while meeting the stringent ACLR requirements.

The current consumption and gain settings are controlled through a digital serial interface (SPI)

The BGA3131 is housed in 20 pins 5 mm x 5 mm leadless HVQFN package and don't need additional heatsink.

Fig 1. Picture of evaluation board

2. Product description

The BGA3131 operates at 5 V supply. The gain is controlled via 3-wire SPI-interface.

The current consumption can be reduced in 4 steps via the serial interface. This interface enables the user to optimize between DC power efficiency and linearity. In addition, the current is automatically reduced at lower gain settings while preserving the linearity performance. In disable mode, the device draws typically 25 mA while it can be still programmed to new gain and current settings.

BGA3131 key features and benefits:

- Low Power consumption of 3.3 W (typical) at highest current and gain setting
- 58 dB gain control range in 1 dB steps using a 3-wire serial interface
- 5 MHz to 205 MHz frequency operating range
- ± 0.4 dB incremental gain step accuracy
- Maximum voltage gain 37 dB
- Excellent IMD3 of -60 dBc at 68 dBmV total output power
- Excellent second harmonic level of -60 dBc at 68 dBmV total output power
- Excellent third harmonic level of -60 dBc at 68 dBmV total output power
- Excellent noise figure of 6.5 dB at maximum gain
- Capable of transmitting modulated carriers while meeting the DOCSIS 3.1 ACLR specification. At an output power of 65dBmV at the F-connector (assuming 3 dB of output loss), the typical ACLR is-64 dBc
- 5 V single supply operation
- Excellent ESD protection at all pins
- Unconditionally stable
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances
- (RoHS)

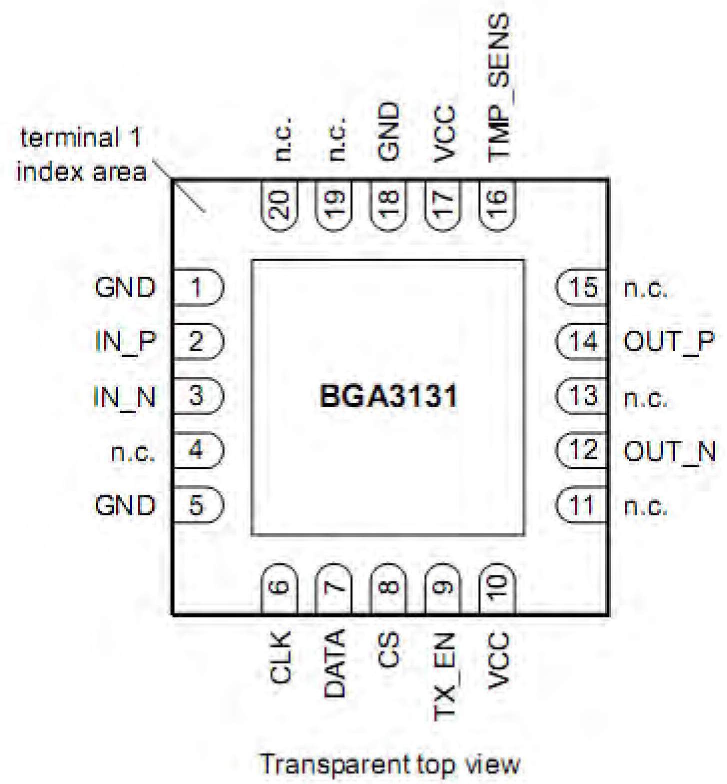


Fig 2. Pin description

3. BGA3131 DOCSIS 3.1 upstream amplifier evaluation board

The BGA3131 customer evaluation kit enables the user to evaluate the RF performance of the DOCSIS 3.1 upstream amplifier. The kit comes with a USB-interface board and customer software which allows you to use your PC to control the SPI interface of the BGA3131. You can set the gain state and advanced features as current consumption and power down of the BGA3131. The board is supplied with two SMA connectors to connect input and output to the RF test equipment in 50 Ω test system.

The Customer evaluation kit (OM17024) contains fully populated BGA3131 RF evaluation board, USB interface board, flat cable, USB flash driver (containing evaluation software, introduction,…)

The plug & play control software doesn't require additional driver for installation.

3.1 Application circuit and component selection

The application board circuit diagram that is implemented on the EVB is shown in Fig 3

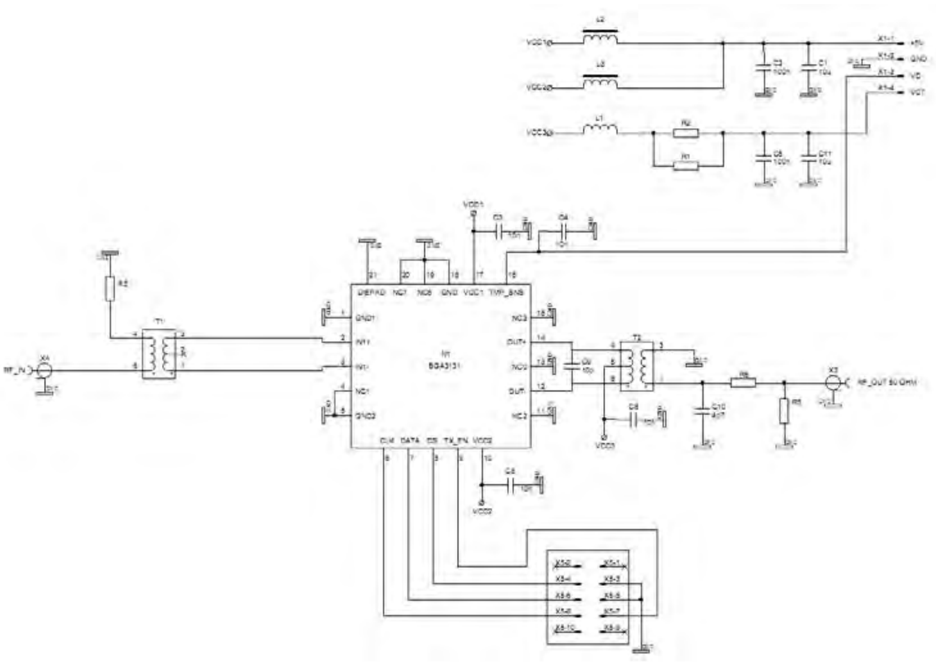


Fig 3. BGA3131 application circuit

It's important that the BGA3131 use a common supply voltage to avoid delays between the different supply pins of the BGA3131.
No bias inductors needed (if needed ferrite beads or inductors can be used to reduce the noise on VCC). Keep the supply decoupling capacitors close by the VCC pins.

For measurements in a 50 Ω system R5 and R6 at RF-output, a 1:4 transformer at RF-input are added for impedance transformation from 75 Ω to 50 Ω. These are not required in the final application.

In the final application the balanced output (37.5 Ω differential) of the BGA3131 needs to be matched to a single-ended 75 Ω load using a 1:2 ratio transformer.

The output transformer (1:2) ratio is needed on the final application, MACOM MABA-011056 or Murata #617PT-2291=P3 can be used.

The transformer also cancels even mode distortion products and common mode signals, such as the voltage transients that occur while enabling and disabling the amplifiers.

BGA3131 pin 13 isn't used and also not internal connected, it can be left open, grounded or connected to VCC.

It's advised to place 2 additional matching capacitors C9 (10pF) and C10 (4.7pF) for optimal RF performance.

Control line:
The maximum clock frequency is 25 MHz and the maximum load on Data line is 30 pF.

3.2 PCB layout information

The supply decoupling capacitors are placed close to the supply pins.

Combine all the BGA3131 supply voltages on one common 5V supply to avoid delays between the supply pins!

The evaluation board uses grounded micro strip lines using different impedances for input and output lines.

Consider the losses of the used transformers and 5.7dB for the output matching resistors (R5 & R6) for deembedding.

Use thermal vias (25 cu filled vias recommended) below the BGA313, for better heatsink keep the areas (as huge as possible) on all layers below the BGA3131 with cupper.

For more info see application note AN11753 "Thermal considerations BGA3131".

The layout and component placement of the BGA3131 evaluation board is given in Fig 4

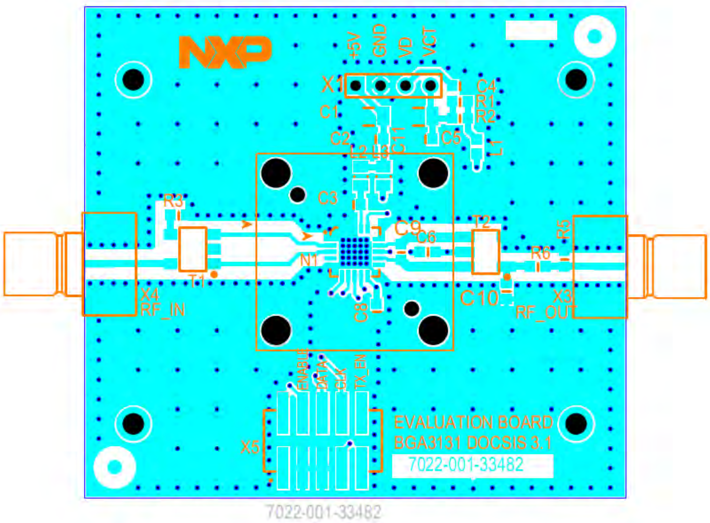


Fig 4. BGA3131 evaluation board layout and component placement

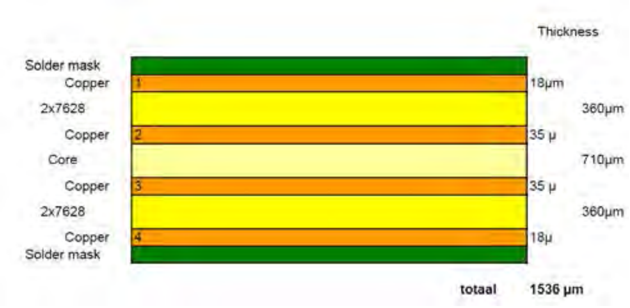
3.3 PCB stack and recommended footprint

The used PCB material is 4 layer FR4 printed circuit board, total height of the pcb is roughly 1.5mm.

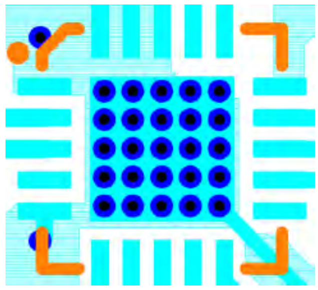
The reason for the chosen pcb stack is to have robust and good thermal behavior evaluation board.

The first layer is for RF routing + signal, second layer is for RF ground + heat sink, third layer is for signal line + heat sink and the fourth layer is again ground + heat sink.

For thermal reasons it's recommended to have 25 cu filled ground via holes of 0.3 mm as shown in Fig 5b.



a. Cross section of the layer stack



b. Recommended footprint and vias

Fig 5. PCB stack and footprint

3.4 Bill of materials

Table 1 gives the bill of materials as is used on the EVB.

Table 1. Bill of materials of evaluation board in Fig. 4

Designator	Description	Footprint	Value	Supplier Name/type	Comment/function
N1	BGA3131	HVQFN20		NXP BGA3131	DOCSIS 3.1 upstream amplifier
C1, C11	capacitor	1206	10 uF	Various	Decoupling
C2, C5	capacitor	0603	100 nF	Murata GRM1555	Decoupling
C3, C4,C6, C8	capacitor	0603	10 nF	Murata GRM1555	Decoupling
C9	capacitor	0603	10 pF	Murata GRM1555	Matching
C10	capacitor	0603	4.7 pF	Murata GRM1555	Matching
L1, L2, L3	place holder for inductor	0603	0 Ω	Various	Place holder for optional inductor 0 Ω mounted
R1, R2, R3	resistor	0603	0 Ω	Various	
R5	resistor	0603	86.6 Ω	Various	75 Ω to 50 Ω conversion for measurement purpose only
R6	resistor	0603	43.2 Ω	Various	
T1	transformer	-	-	TOKO: #617PT-1664	Input matching 1:4 (50 Ω to 200 Ω)

Designator	Description	Footprint	Value	Supplier Name/type	Comment/function
T2	transformer	-	-	MACOM: MABA-011056	Output matching 1:2 (37.5 Ω to 75 Ω)
X1	Header, 4P	-	-	-	DC connections
X3, X4	SMA connector	-	-	-	RF connections
X5	Header, 10P	-	-	-	Control interface (USB to SPI)

3.5 Summary of application / design information

- Use common supply voltage to avoid supply voltage delays between the BGA3131 supply pins
- No need on bias inductors. Ferrite beads or inductors can be used to reduce the noise on supply voltage (take care on routing, less coupling to RF-out, avoid ground loop)
- Place the supply decoupling capacitors close to the VCC pins of the BGA3131, propose to add additional to the 10 nF decoupling capacitor on the VCC pins another 10 uF to reduce distortions or noise coming from the supply.
- The output transformer 1:2 (37.5 Ω differential to 75 Ω single-ended) should cover the DOCSIS 3.1 bandwidth (5 – 205 MHz), examples are MACOM MABA-011056 or Murata #617PT-2291=P3
- For optimal RF-performance (output matching) it’s recommended to add C9 (10 pF) and C10 (4.7 pF) at RF-out.
- Pin 13 isn’t used (not internal connected), it can be left open, grounded or connected to VCC
- Input transformer 1:4 (200 Ω differential to 50 Ω single-ended), R5 and R6 (75 Ω to 50 Ω) at RF-out are only used for measurement purpose on the application board to have 50 Ω at the RF-in and RF-out sma-connector and not required on the final application
- Use thermal vias (25 cu filled vias recommended) below the BGA3131, for better heatsink keep the ground areas (as huge as possible) on all layers below the BGA3131 with cupper

4. BGA3131 evaluation board connections and control software

The BGA3131 evaluation board can be controlled via the control software and doesn't need any driver for Windows PC's.

Before starting with the evaluation following steps needs to be done:

1. Connect the interface board to the BGA3131 evaluation board (X5) using the flat cable.
2. Power the BGA3131 evaluation board with 5V at pin +5V and VCT (connect both supply pins on same 5V supply to avoid delays on the supply pins). Use a 5W power supply.
3. Insert the interface board in a free USB slot on PC.
4. Insert the USB flash driver in another free USB slot on the PC.
5. Launch the customer software BGA3131_XX by double click on the icon.
6. Now the GUI (shown in Fig 6) will appear to control the gain, current and the TX_Enable function of the BGA3131.

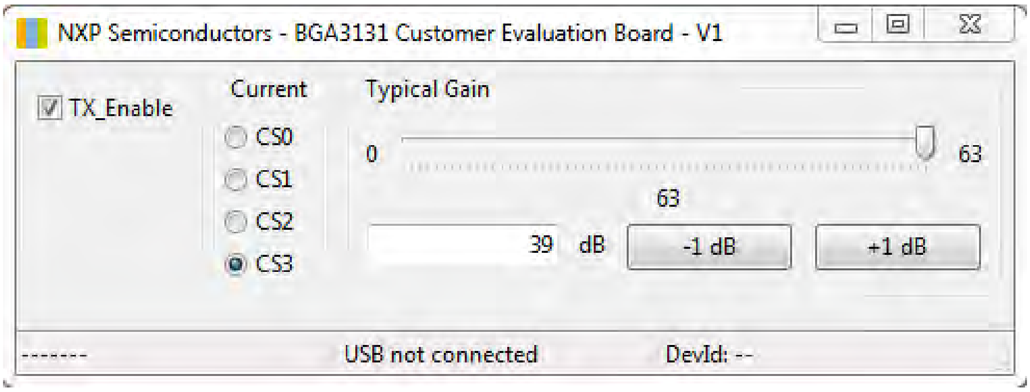


Fig 6. BGA3131 GUI control software

Gain can be set by using the slider, +/- buttons or entered (maximum gain is at setting 63).

TX can be enabled and disabled by using the TX_Enable button (typical current is 25 mA in disable mode)

Current can be set via the CS0…CS3 (see Fig 7)

Current setting at max gain (setting 63)	
Current setting	Typical supply current (mA)
CS0	350
CS1	410
CS2	480
CS3	660

Fig 7. BGA3131 GUI current setting

5. Measurement results

5.1 Static characteristics

Typical values at VCC = 5 V; current setting = 3; gain setting 50 up and including 63; T_{case} = 25 °C; $Z_{i(dif)}$ = 200 Ω; $Z_{o(se)}$ = 75 Ω; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.75	5.0	5.25	V
I_{CC}	supply current	transmit-enable mode; TX_EN = HIGH	610	660	720	mA
		transmit-disable mode; TX_EN = LOW	-	25	-	mA
V_{IH}	HIGH-level input voltage	[1]	1.8	-	V_{CC} + 0.6	V
V_{IL}	LOW-level input voltage	[1]	0	-	0.8	V
P	power dissipation		-	3.3		W

Fig 8. Typical static characteristics of the BGA3131 evaluation board

[1] Voltage on the control pins.

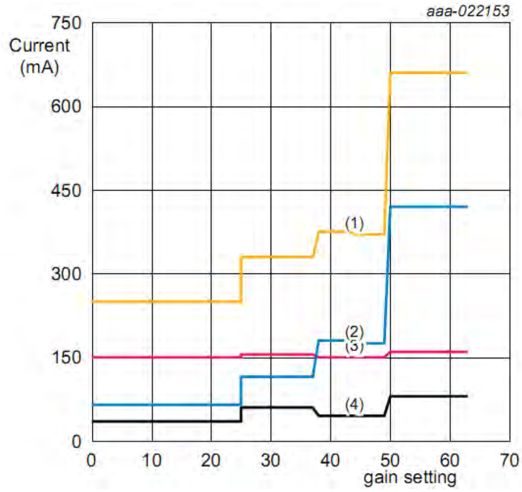


Fig 9. Typical pin DC-currents as function of gain setting of the BGA3131

VCC = 5 V; current setting = 3; Tamb = 25 °C;
(1) total current; I_{CC1} + I_{CC2} + ICT
(2) ICT; output balun center tap current
(3) I_{CC1}; current through Pin #17 (V_{CC1})
(4) I_{CC2}; current through Pin #16 (V_{CC2})

5.2 ACLR characteristics

Typical values at VCC = 5 V; current setting = 3; Gain setting 60; T_{case} = 25 °C; $Z_{i(dif)}$ = 200 Ω; $Z_{o(se)}$ = 75 Ω; channel bandwidth = 192 MHz; integration bandwidth = 9.6 MHz; f = 5 MHz to 205 MHz; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DOCSIS 3.1						
ACLR	adjacent channel leakage ratio	P_i = 34 dBmV(rms); P_L = 68 dBmV(rms)				
		channel configuration: channel bandwidth is 192 MHz, with exclusion band at 147.5 MHz, with a bandwidth of 9.6 MHz. Input signal with a PAPR of 13 dB	-	−64	−58	dBc

Fig 10. Typical ACLR characteristics of the BGA3131 evaluation board

5.3 Dynamic characteristics

The table below shows the typical values at VCC = 5 V; current setting = 3; gain setting 15 up and including 63; T_{case} = 25 °C; $Z_{i(dif)}$ = 200 Ω;$Z_{o(se)}$ = 75 Ω; voltage gain does include loss due to output transformer; unless otherwise specified. All RF parameters are measured on an application board with the circuit as shown in Fig 3 and components implemented as listed in Table 1.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_v	voltage gain	gain code = 111111 [1][2]	-	37	-	dB
		gain code = 001111 [1][2]	-	–11	-	dB
G_{flat}	gain flatness	f = 5 MHz to 205 MHz [1]	-	± 0.5	-	dB
RL_{out}	output return loss	transmit mode enable over all gain settings, measured in 75 Ω system	-	14	-	dB
		transmit mode disable over all gain settings, measured in 75 Ω system	-	12	-	dB
RL_{in}	input return loss	transmit mode enable overall gain settings, measured in 200 Ω system	-	20	-	dB
		transmit modes disable overall gain settings, measured in 200 Ω system	-	20	-	dB
G_{step}	gain step	[1]	-	1.0	-	dB
$E_{G(dif)}$	differential gain error	[1]	-	± 0.4	-	dB
$R_{i(dif)}$	differential input resistance		-	200	-	Ω
$R_{o(dif)}$	differential output resistance		-	37.5	-	Ω
f_{range}	frequency range		5	-	205	MHz
α_{isol}	isolation	transmit-disable mode; TX_EN = LOW; f = 205 MHz	-	60	-	dB
NF	noise figure	transmit mode; gain code = 111111	-	6.5	-	dB
		transmit mode; gain code = 100110	-	15	-	dB
$t_{sw(G)}$	gain switch time	transmit-disable/transmit-enable transient duration	-	3.0	-	μs
		transmit-enable/transmit-disable transient duration	-	0.5	-	μs
V_{trt}	transient voltage	transmit-disable/transmit-enable transient step size; peak value				
		≥ 58 dBmV output power [3][4]	-	45	-	mV
		52 dBmV output power [3][4]	-	15	-	mV
		46 dBmV output power [3][4]	-	10	-	mV
		40 dBmV output power [3][4]	-	5	-	mV
		≤ 34 dBmV output power [3][4]	-	3	-	mV
α_{2H}	second harmonic level	transmit-enable mode; gain code = 111111; P_i = 31.0 dBmV(rms); P_L = 68.0 dBmV(rms) into 75 Ω impedance	-	–65	-	dBc
α_{3H}	third harmonic level	transmit-enable mode; gain code = 111111; P_i = 31.0 dBmV(rms); P_L = 68.0 dBmV(rms) into 75 Ω impedance	-	–65	-	dBc
IMD3	third-order intermodulation distortion	transmit-enable mode; gain code = 111111; P_L = 65 dBmV(rms) per tone into 75 Ω impedance	-	–60	-	dBc
$P_{L(1dB)}$	output power at 1 dB gain compression	CW input signal RMS value; frequency = 205MHz	-	78	-	dBmV

Fig 11. Typical performance of the BGA3131 evaluation board

[1] Pi ≤ 30 dBmV.
[2] Excluding loss of resistive matching circuit, to match 75 Ω to 50 Ω.
[3] Measured at the output of the output balun.
[4] Assume 3 dB loss between by output of the balun and F-connector in the final application.

5.4 Measurement set-up

For accurate P1dB, IP3 and harmonic measurements (improve the dynamic range of the measurement setup) add bandpass- or low pass-filter on the signal generator.
Filters need good broad band matching to meet their specified filter characteristics, therefore add minimum 3 dB attenuator at bandpass or low pass filter output to have proper filtering!

6. Temperature sense using build in temperature diode

The build in temperature diode can be used to measure the junction temperature of the BGA3131 by feeding 1 mA constant current at pin 16 and measuring the voltage at pin 16.

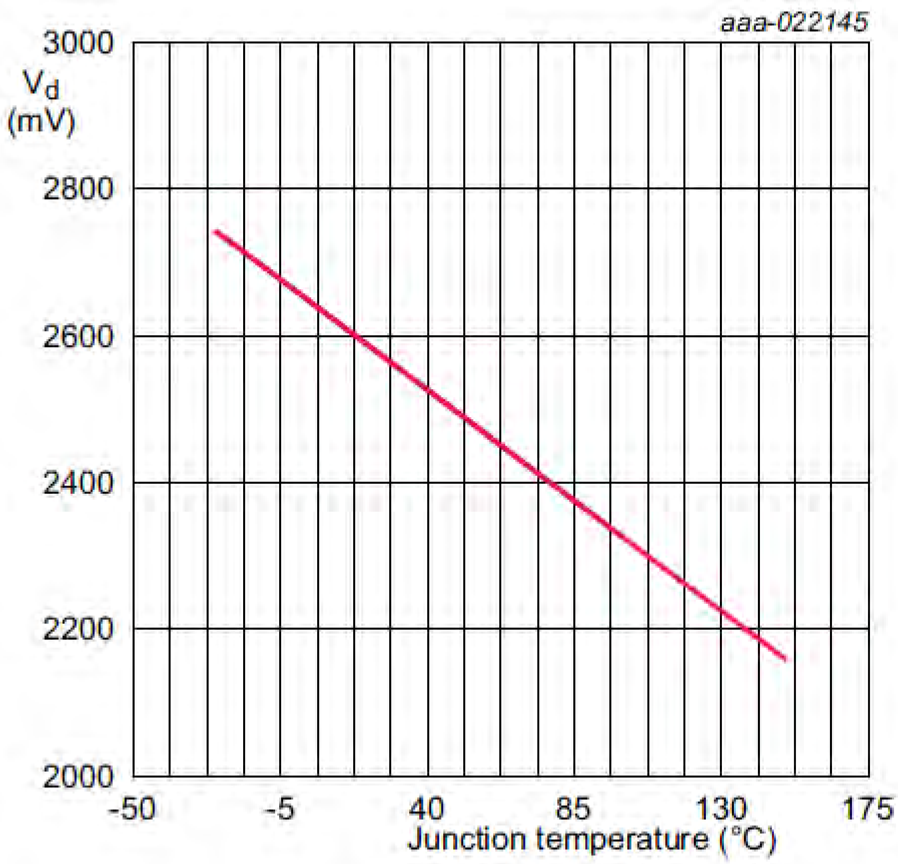


Fig 12. Thermal diode voltage as function of junction temperature : typical values VCC = 5 V; current setting = 3; TMP_SENS DC current = 1 mA; GS = 63

7. Customer Evaluation Kit

The customer evaluation kit contains:

- BGA3131 evaluation board
- Interface board (USB to SPI)
- Flat cable
- 5 loose samples of the BGA3131
- USB flash driver (contains control software, introduction)

a. b.

Fig 13. Customer evaluation KIT

8. Abbreviations

Table 2. Abbreviations

Acronym	Description
AC	Alternating Current
DC	Direct Current
RMS	Root Mean Square
ESD	Electro Static Discharge
HVQFN	Heat sink Very thin Quad Flat pack No leads
PCB	Printed Circuit Board
RF	Radio Frequency
SMD	Surface Mounted Device
CATV	Community Antenna Television
CW	Continuous Wave
OFDM	Orthogonal Frequency Division Multiplexing
PAPR	Peak-to-Average Power Ratio
SMA	Sub-Miniature version A
TX	Transmission
SoC	System on a Chip
VoIP	Voice over Internet Protocol

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