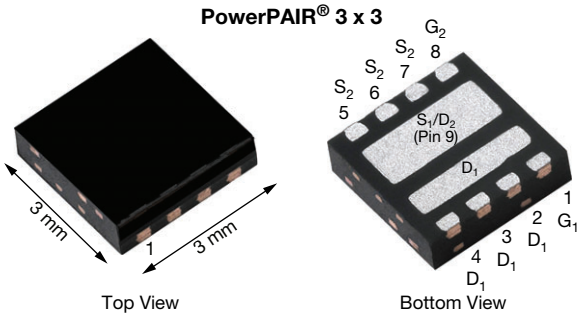
Dual N-Channel 30 V (D-S) MOSFET



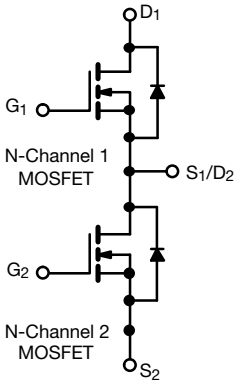
FEATURES

- TrenchFET® Gen IV power MOSFET
- High side and low side MOSFETs form optimized combination for 50 % duty cycle
- Optimized R_{DS} - Q_g and R_{DS} - Q_{gd} FOM elevates efficiency for high frequency switching
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- Synchronous buck
- DC/DC conversion
- Half bridge
- POL



PRODUCT SUMMARY	
MOSFET CHANNEL-1 AND CHANNEL-2	
V_{DS} (V)	30
$R_{DS(on)}$ max. (Ω) at V_{GS} = 10 V	0.00675
$R_{DS(on)}$ max. (Ω) at V_{GS} = 4.5 V	0.00944
Q_g typ. (nC)	6.3
I_D (A) [a, d]	30
Configuration	Dual

ORDERING INFORMATION	
Package	PowerPAIR 3 x 3
Lead (Pb)-free and halogen-free	SiZ350DT-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		CHANNEL-1 AND CHANNEL-2		
		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	30	V
Gate-source voltage		V_{GS}	+16 / -12	
Continuous drain current (T_J = 150 °C)	T_C = 25 °C	I_D	30 [a]	A
	T_C = 70 °C		30 [a]	
	T_A = 25 °C		18.5 [b, c]	
	T_A = 70 °C		14.8 [b, c]	
Pulsed drain current (t = 100 µs)		I_{DM}	100	
Continuous source current (MOSFET diode conduction)	T_C = 25 °C	I_S	13.9	
	T_A = 25 °C		3.1 [b, c]	
Single pulse avalanche current	L = 0.1 mH	I_{AS}	10	
Single pulse avalanche energy		E_{AS}	5	mJ
Maximum power dissipation	T_C = 25 °C	P_D	16.7	W
	T_C = 70 °C		10.7	
	T_A = 25 °C		3.7 [b, c]	
	T_A = 70 °C		2.4 [b, c]	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature)			260	

Notes
a. Package limited
b. Surface mounted on 1" x 1" FR4 board
c. t = 10 s
d. T_C = 25 °C

THERMAL RESISTANCE RATINGS

PARAMETER		CHANNEL-1 AND CHANNEL-2			
		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient [a, b]	t ≤ 10 s	R_{thJA}	27	34	°C/W
Maximum junction-to-case (drain)	Steady state	R_{thJC}	6	7.5	

Notes

a. Surface mounted on 1" x 1" FR4 board

b. Maximum under steady state conditions is 69 °C/W

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

PARAMETER	CHANNEL-1 AND CHANNEL-2					
	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	30	-	-	V
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1	-	2.4	
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = +16 V / -12 V	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V	-	-	1	µA
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 55 °C	-	-	5	
On-state drain current [a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	40	-	-	A
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 15 A	-	0.00563	0.00675	Ω
		V_{GS} = 4.5 V, I_D = 10 A	-	0.00787	0.00944	
Forward transconductance [a]	g_{fs}	V_{DS} = 10 V, I_D = 15 A	-	46	-	S
Dynamic [b]						
Input capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	-	940	-	pF
Output capacitance	C_{oss}		-	375	-	
Reverse transfer capacitance	C_{rss}		-	40	-	
C_{rss}/C_{iss} ratio			-	0.043	0.086	
Total gate charge	Q_g	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 18.5 A	-	13.5	20.3	nC
		V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 18.5 A	-	6.3	10	
Gate-source charge	Q_{gs}		-	2.8	-	
Gate-drain charge	Q_{gd}		-	1.2	-	
Gate resistance	R_g	f = 1 MHz	0.2	0.8	1.6	Ω
Turn-on delay time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 1 Ω, I_D ≅ 14.8 A, V_{GEN} = 10 V, R_g = 1 Ω	-	10	20	ns
Rise time	t_r		-	25	50	
Turn-off delay time	$t_{d(off)}$		-	15	30	
Fall time	t_f		-	10	20	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 1 Ω, I_D ≅ 14.8 A, V_{GEN} = 4.5 V, R_g = 1 Ω	-	15	30	
Rise time	t_r		-	45	68	
Turn-off delay time	$t_{d(off)}$		-	10	20	
Fall time	t_f		-	25	50	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**CHANNEL-1 AND CHANNEL-2**					
	SYMBOL	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Drain-source Body Diode Characteristics						
Continuous source-drain diode current	I_S	T_C = 25°C	-	-	13.9	A
Pulse diode forward current	I_{SM}		-	-	100	
Body diode voltage	V_{SD}	I_S = 14.8 A, V_{GS} = 0 V	-	0.85	1.2	V
Body diode reverse recovery time	t_{rr}	I_F = 14.8 A, di/dt = 100 A/µs, T_J = 25 °C	-	30	45	ns
Body diode reverse recovery charge	Q_{rr}		-	30	45	nC
Reverse recovery fall time	t_a		-	17	-	ns
Reverse recovery rise time	t_b		-	13	-	

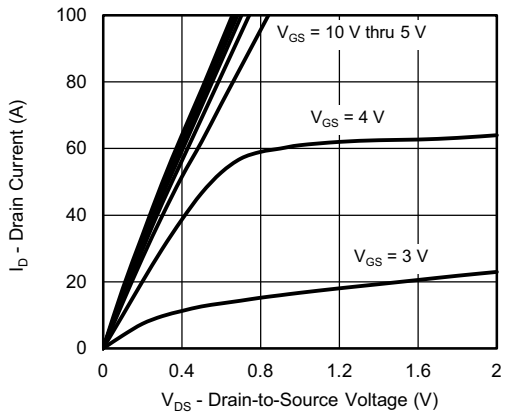
Notes

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %

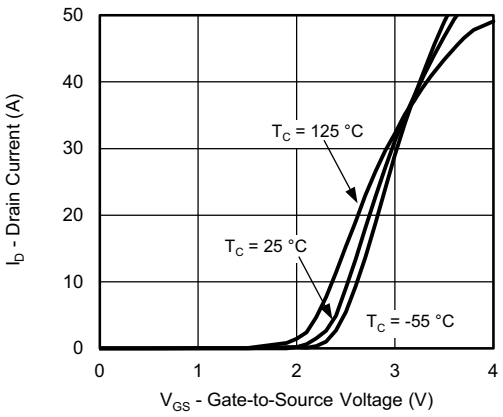
b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

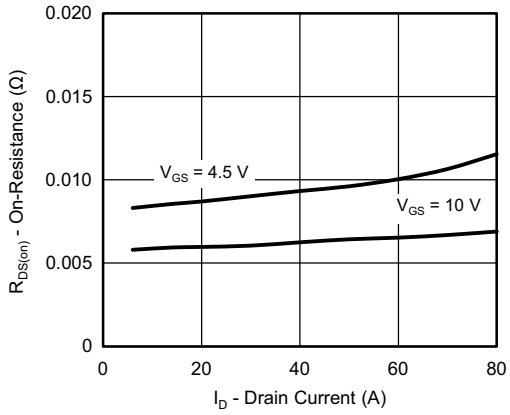
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



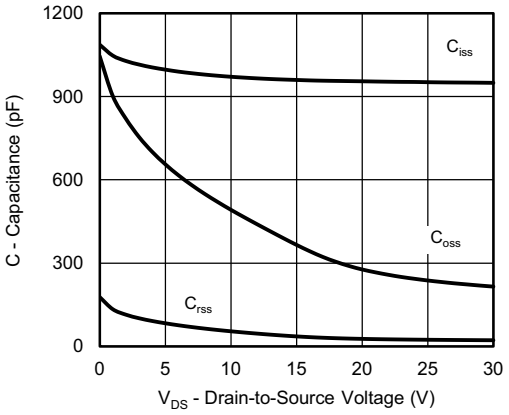
Output Characteristics



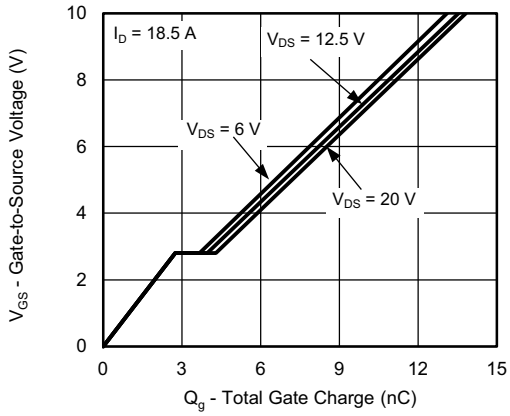
Transfer Characteristics



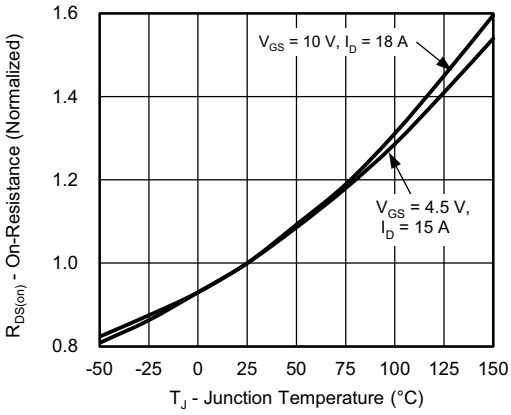
On-Resistance vs. Drain Current and Gate



Capacitance

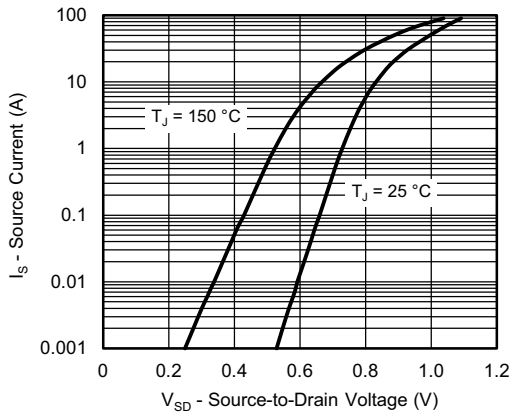


Gate Charge

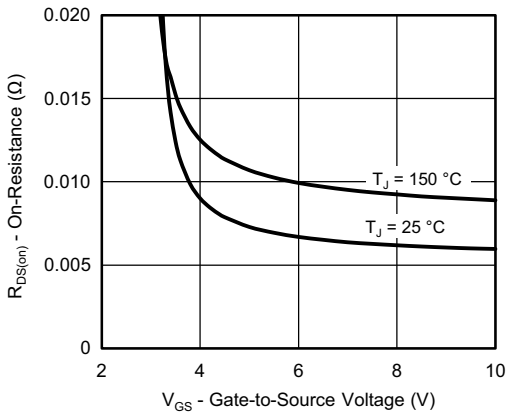


On-Resistance vs. Junction Temperature

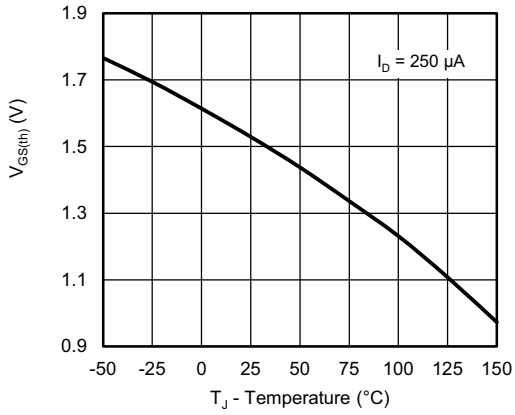
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



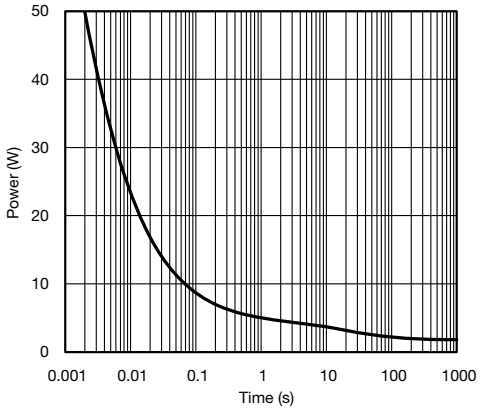
Source-Drain Diode Forward Voltage



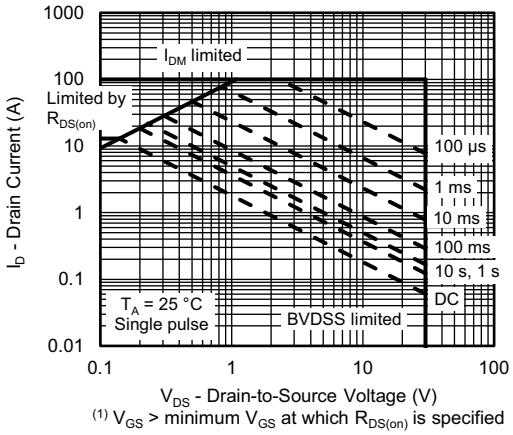
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

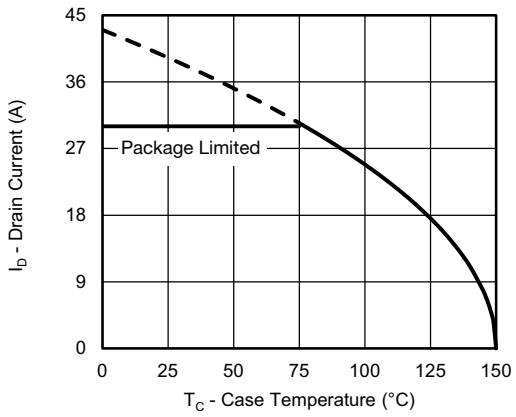


Single Pulse Power

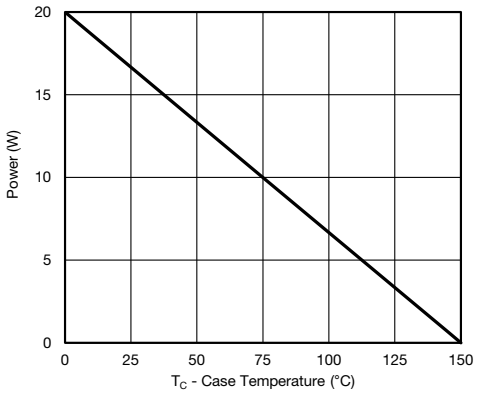


Safe Operating Area, Junction-to-Ambient

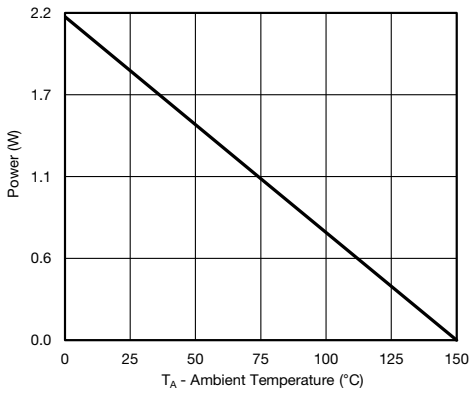
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating [a]



Power, Junction-to-Case

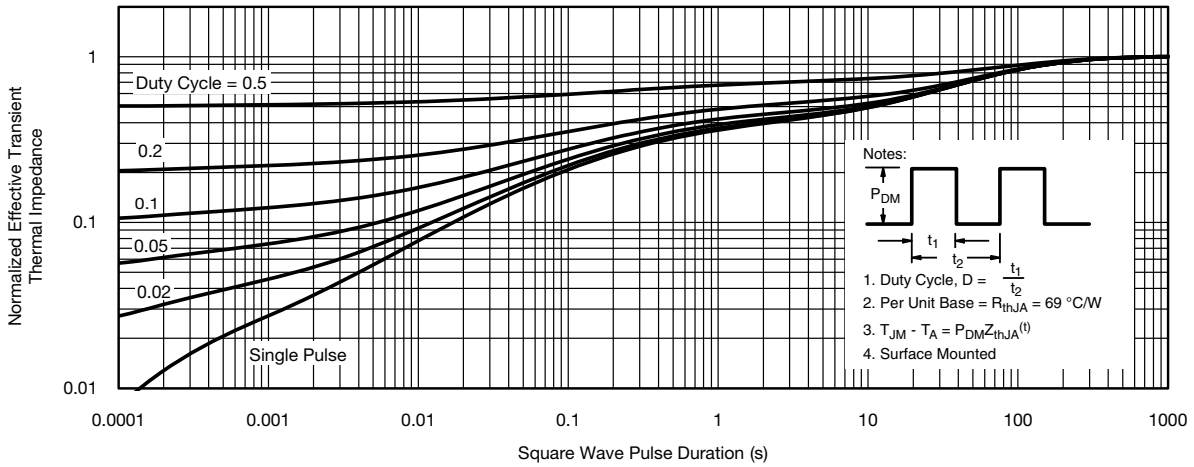


Power, Junction-to-Ambient

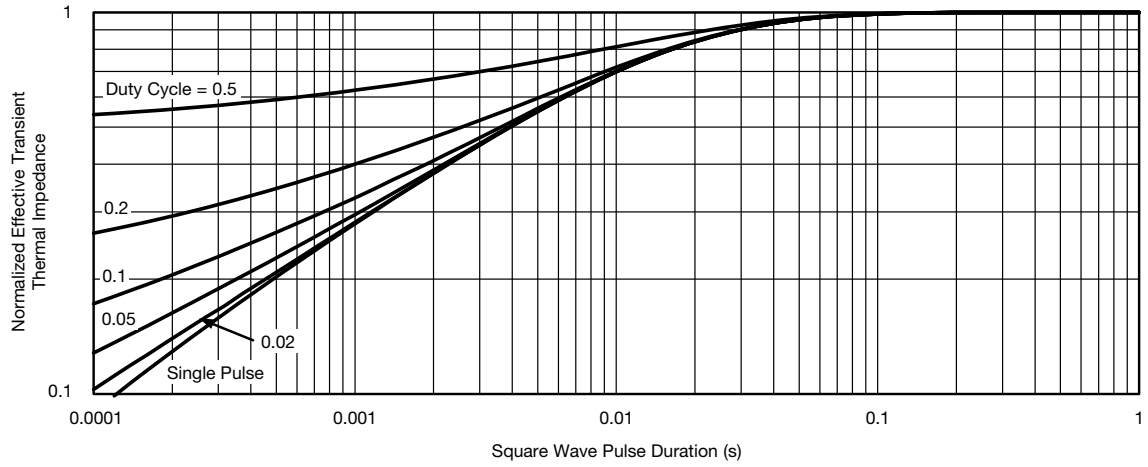
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



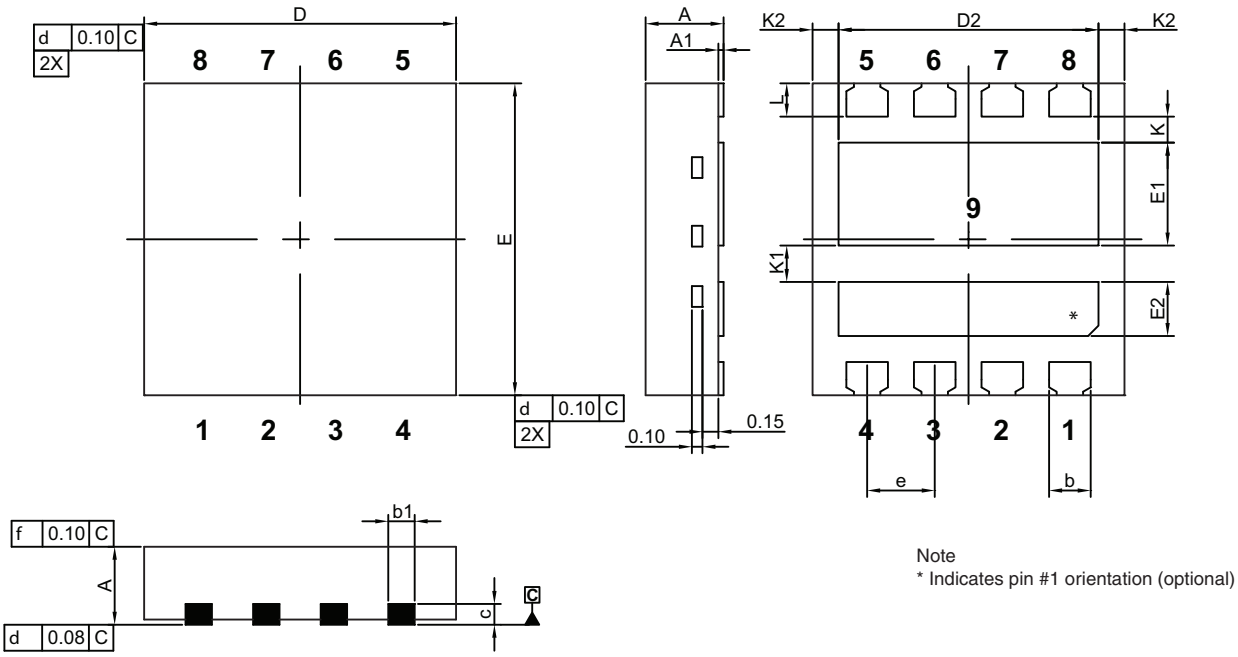
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?76540.

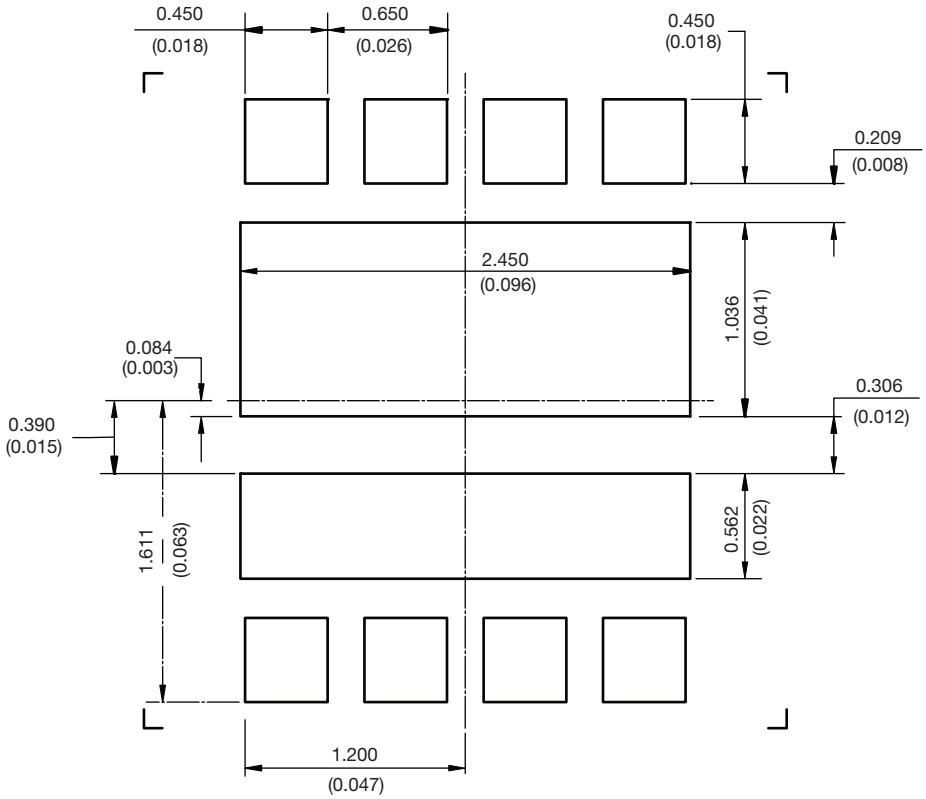
PowerPAIR® 3 x 3 Case Outline



Note
* Indicates pin #1 orientation (optional)

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00		0.05	0.000		0.002
b	0.35	0.40	0.45	0.014	0.016	0.018
b1	0.20	0.25	0.38	0.008	0.010	0.015
C	0.18	0.20	0.23	0.007	0.008	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
D2	2.35	2.40	2.45	0.093	0.094	0.096
E	2.90	3.00	3.10	0.114	0.118	0.122
E1	0.94	0.99	1.04	0.037	0.039	0.041
E2	0.47	0.52	0.57	0.019	0.020	0.022
e	0.65 BSC			0.026 BSC		
K	0.25 typ.			0.010 typ.		
K1	0.35 typ.			0.014 typ.		
K2	0.30 typ.			0.012 typ.		
L	0.27	0.32	0.37	0.011	0.013	0.015
ECN: T12-0347-Rev. C, 18-Jun-12 DWG: 5998						

RECOMMENDED MINIMUM PAD FOR PowerPAIR® 3 x 3



Recommended PAD for PowerPAIR 3 x 3

Dimensions in millimeters (inches)

Keep-Out 3.5 mm x 3.5 mm for non terminating traces

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